Oscar

	Report Section	%	E	S	D	U	
1	Introduction, background, purpose etc.	5	x				5.0
2	Identify and Formulate problem/design goals (1a)	10			x		6.7
3	Develop design/solution (1b)	15	x				15.0
4	Acquire background knowledge (e.g., Data-sheets, papers, etc.) (7a)	10			x		6.7
5	Describe design judgements regarding global, economic, environmental, and societal contexts (4b)	10			x		6.7
6	Conduct Experiments, acquire data* (6a)	15	x				15.0
7	Conduct Simulations, make predictions* (6b)	10	x				10.0
8	Interpret Results, draw inferences* (6c)	20			x		13.3
9	Summary/Conclusion	5			x		3.3
	Total	**100**					**81.7**

Report

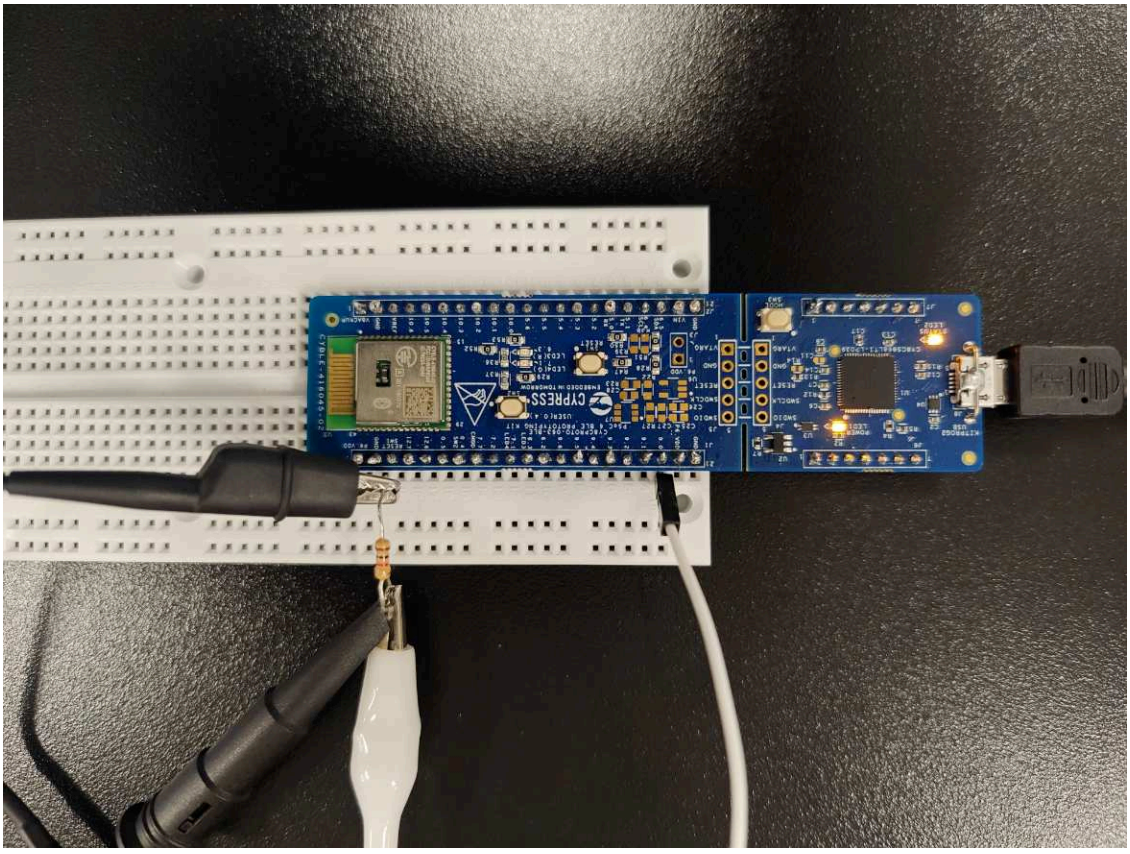
March 19, 2024

1 Lab 1 Report

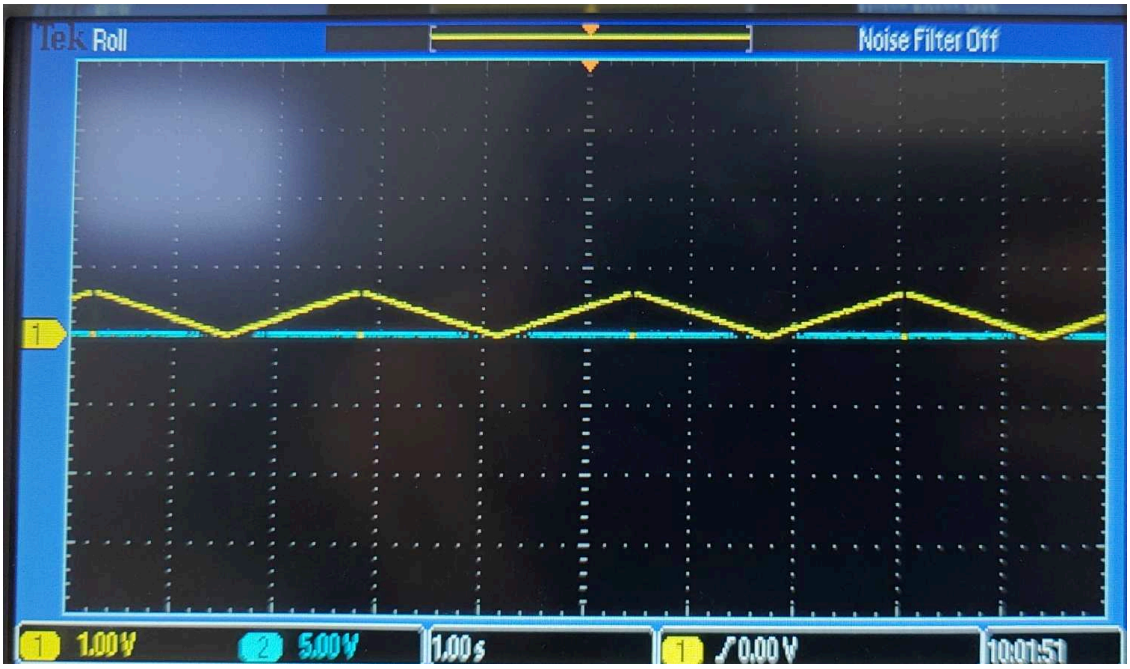
This lab is about developing a curve tracer for BJT and MOSFET transistors.

Testing the IDAC. The first test of the IDAC was to run a loop that would increment the current output to its maximum, then decrement to a minimum. This was verified by reading the voltage across a 1k resistor and reading the oscilloscope output. The oscilloscope output demonstrates that the IDAC ramp is behaving as expected; in this case, the IDAC is ramping between 0-600 uA.

IDAC Circuit



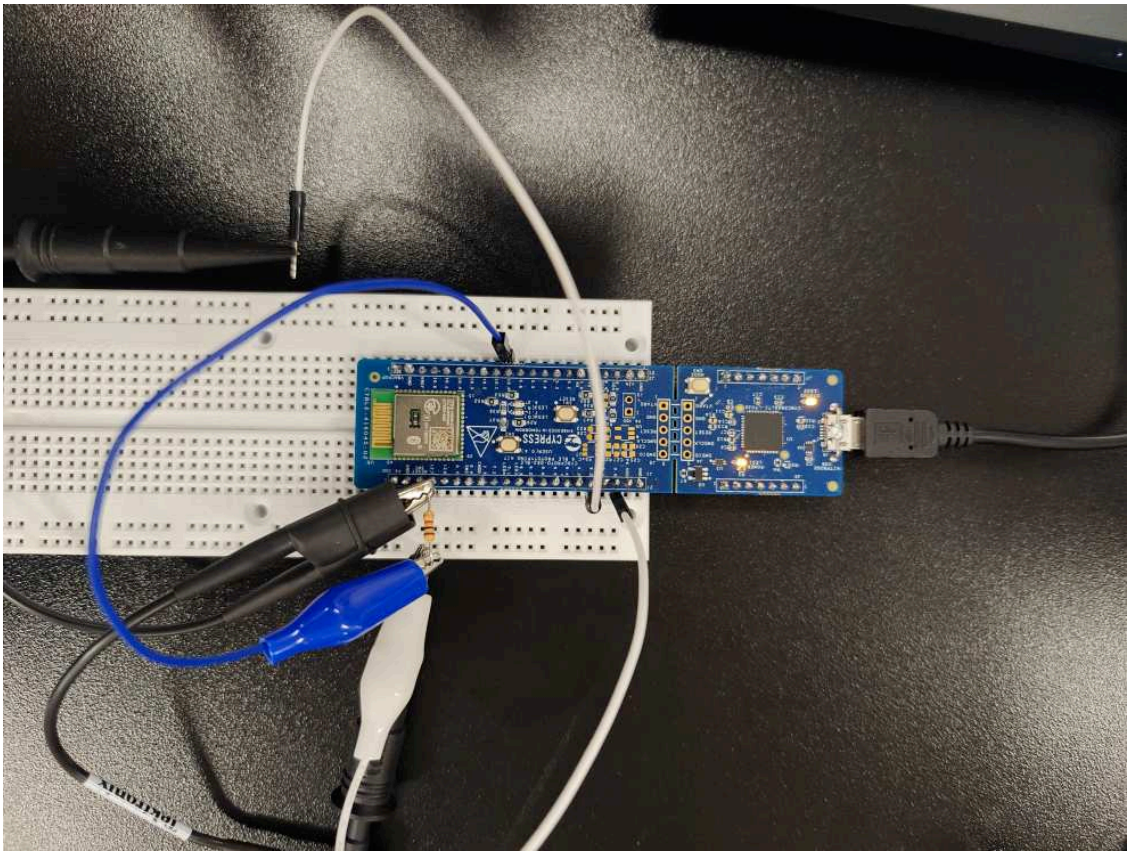
IDAC Output



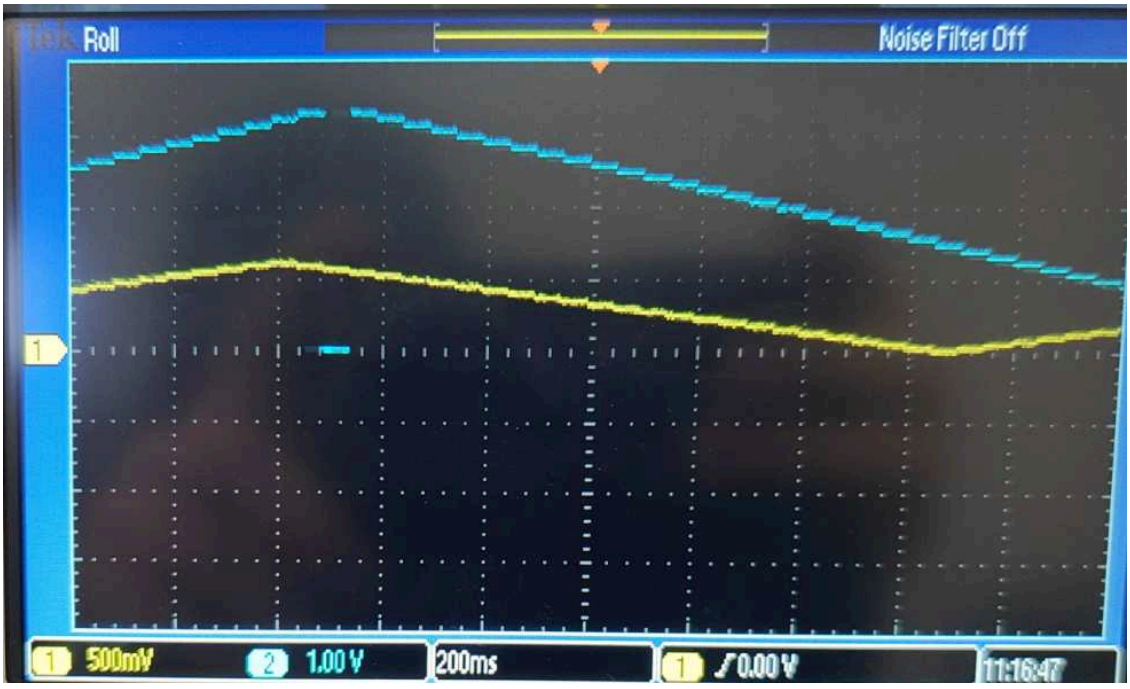
Testing the VDAC

The VDAC is configured to output a voltage level between 0-3.3 V. In the configuration below, the VDAC output is directly connected to the oscilloscope with no load. Channel 1 on the oscilloscope is measuring the IDAC output as before and Channel 2 is displaying the VDAC output which goes up to just below 3.3 Volts.

VDAC and IDAC circuit



VDAC (blue) and IDAC (yellow) output

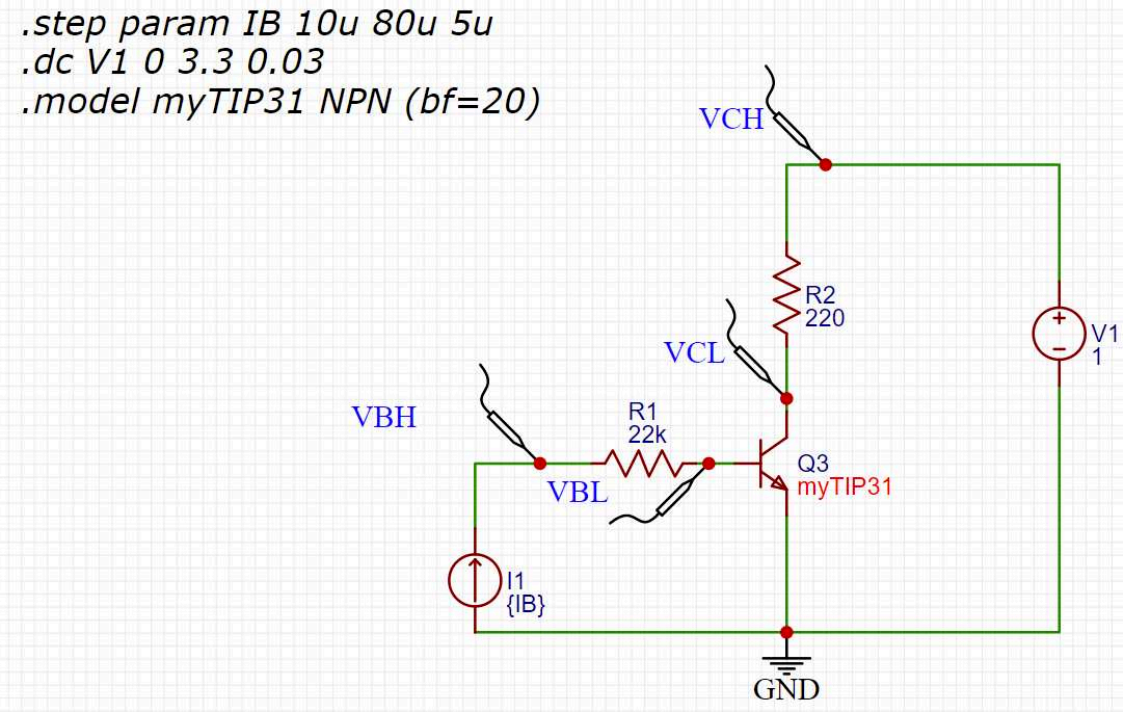


Curve Tracer With the VDAC and IDAC functioning, the next piece is to ramp the VDAC for each

increment of the IDAC. The goal at this point is to measure the variation in the collector current of a BJT transistor as the collector voltage is varied with constant base current. The circuit setup matches the circuit shown for the simulation.

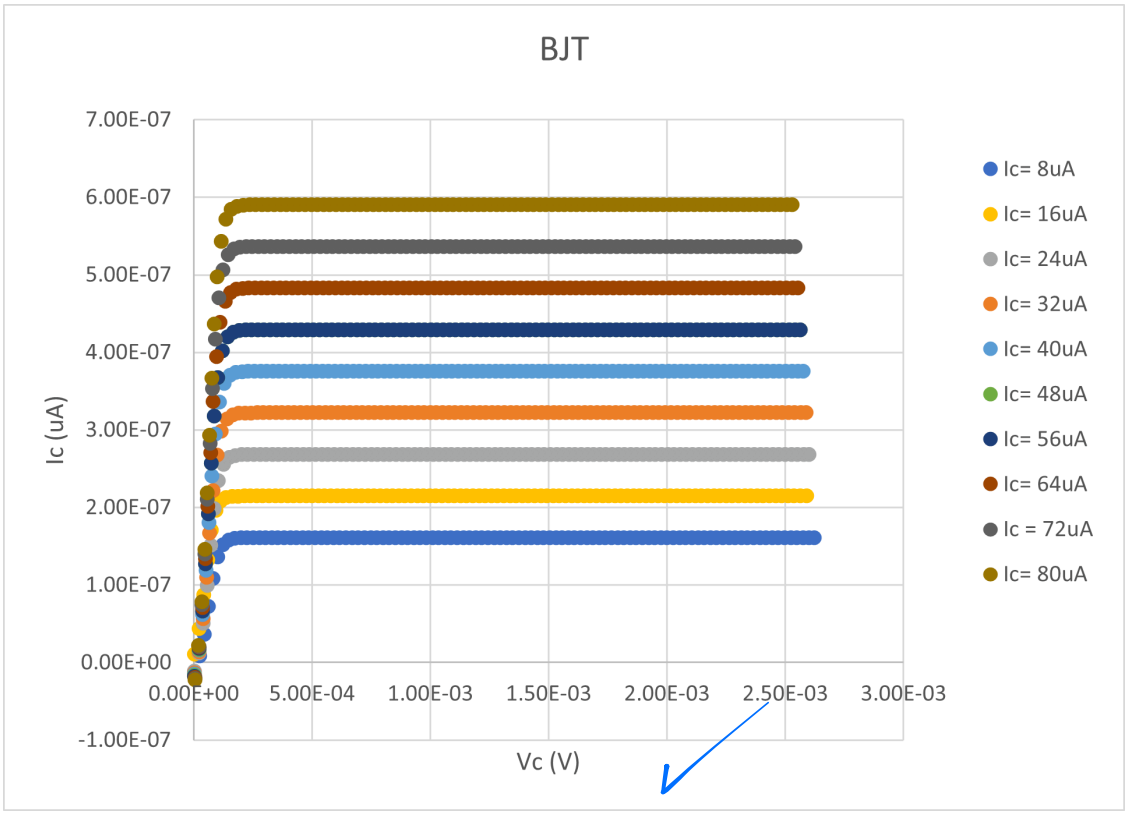
The simulation runs a dc sweep on the voltage source for every step of the current source value. The VCH, VCL, VBH, and VBL probes each correspond to ADC pins on the PSoC6 being used.

BJT Parameter Sweep Simulation circuit

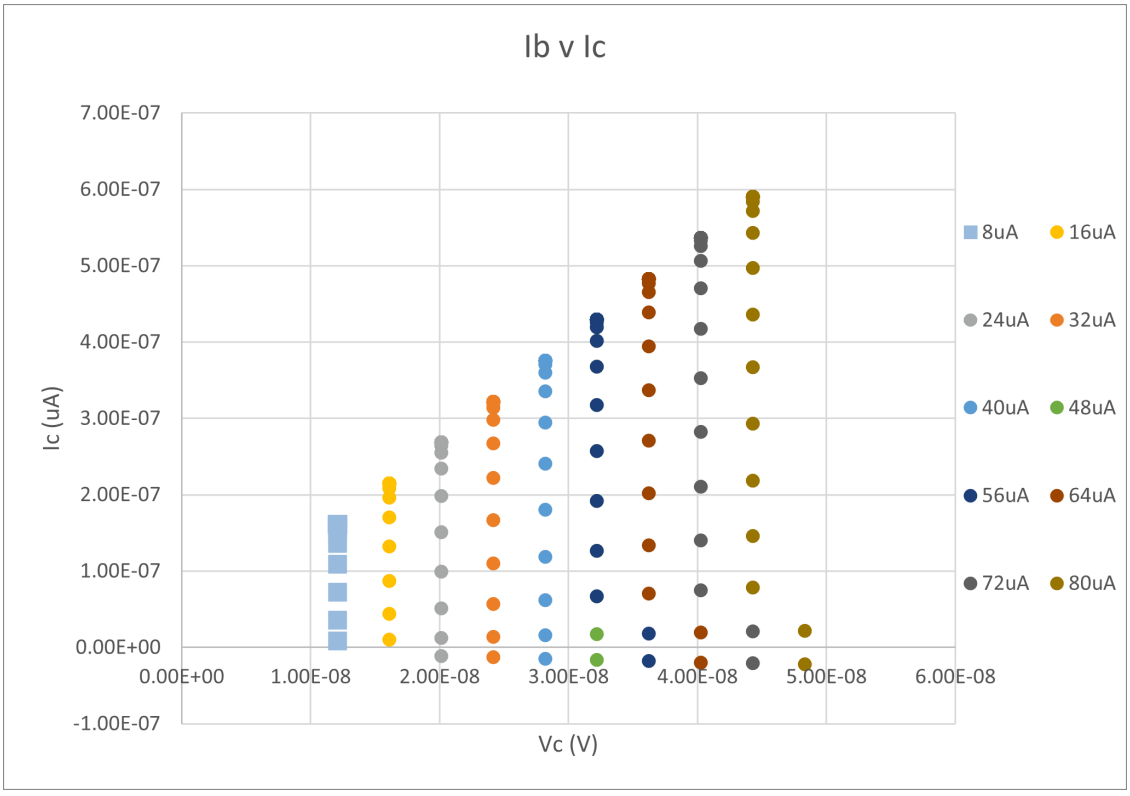


The results of this simulation are saved in a csv, then imported to an Excel spreadsheet to run the calculations. The curve trace output is shown below for the base current and collector voltage. The labels are wrong but the currents go from 10 uA to 80 uA in increments of 5 uA.

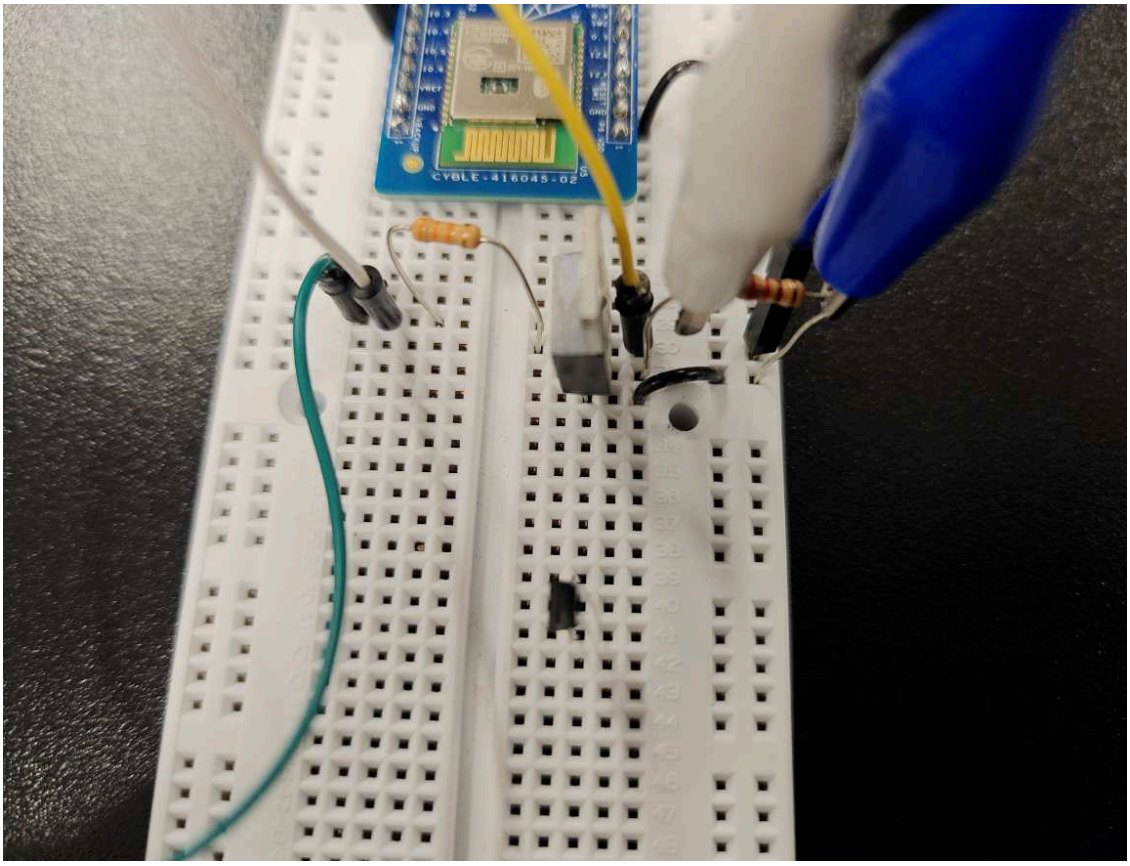
The output graph shows that the BJT in the simulation has nearly perfect curves for varying voltage.



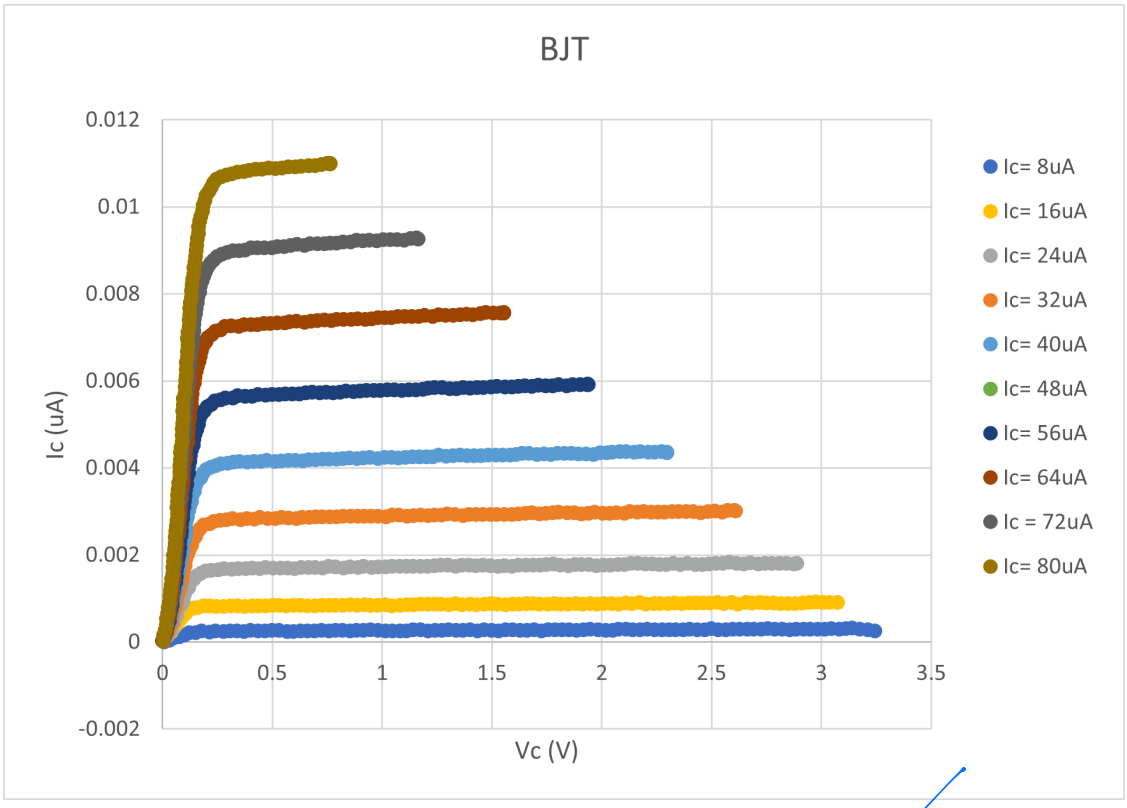
The simulation also reveals ideal current control for the BJT circuit



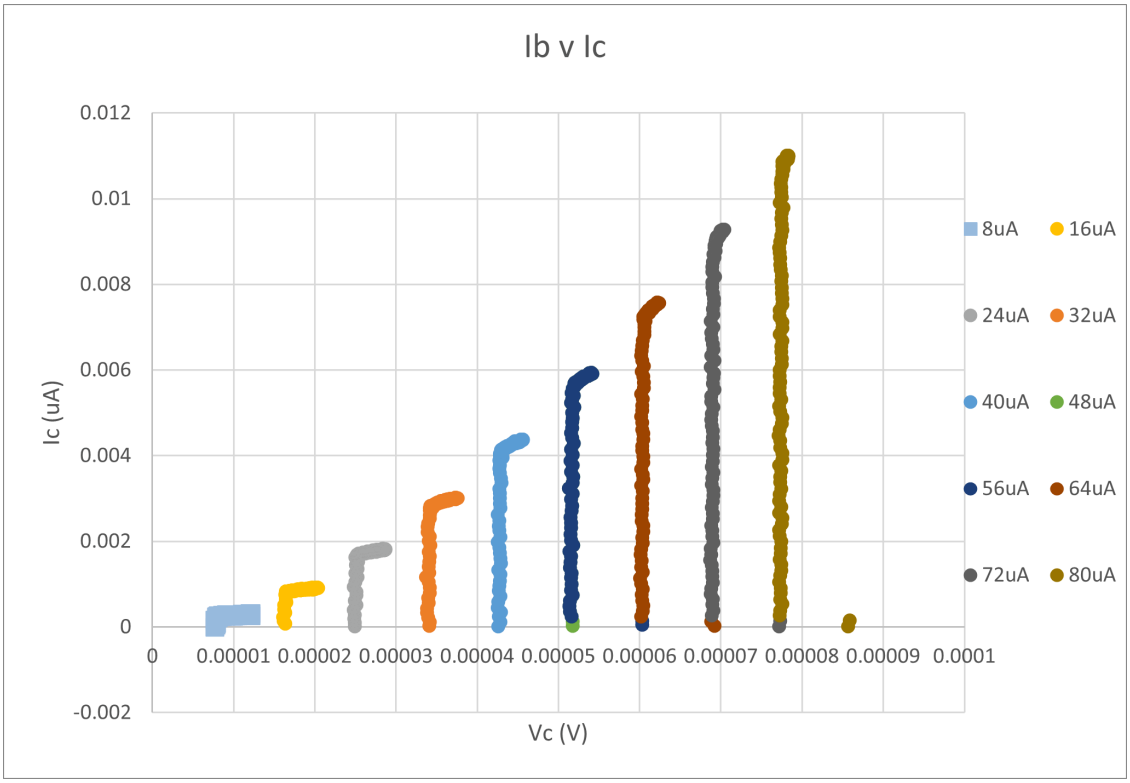
Circuit setup for BJT sweep



BJT sweep output graph



The lab data reveals imperfect current control or ADC readings



FET Simulation 22