M50930-XXXFP, M50931-XXXFP M50932-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50930-XXXFP, M50931-XXXFP and the M50932-XXXFP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 80-pin plastic molded QFP. These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

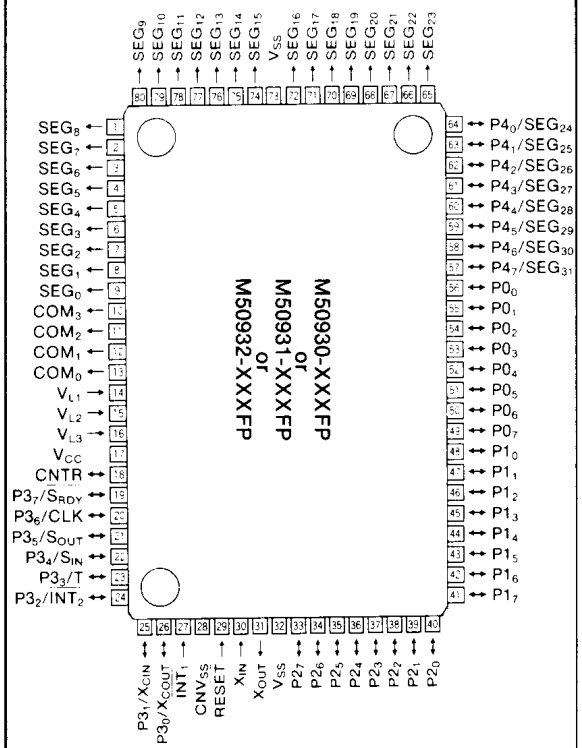
These microcomputers are also suitable for applications which require controlling LCDs.

The differences among the M50930-XXXFP, M50931-XXXFP and the M50932-XXXFP are noted below. The following explanations apply to the M50930-XXXFP. Specification variations for other chips are noted accordingly.

Type name	ROM size	RAM size
M50930-XXXFP	4096 bytes	128 bytes
M50931-XXXFP	4096 bytes	512 bytes
M50932-XXXFP	8192 bytes	512 bytes

M50932-XXXFP only has pull-up transistor option for CNTR pin.

PIN CONFIGURATION (TOP VIEW)



Outline 80P6

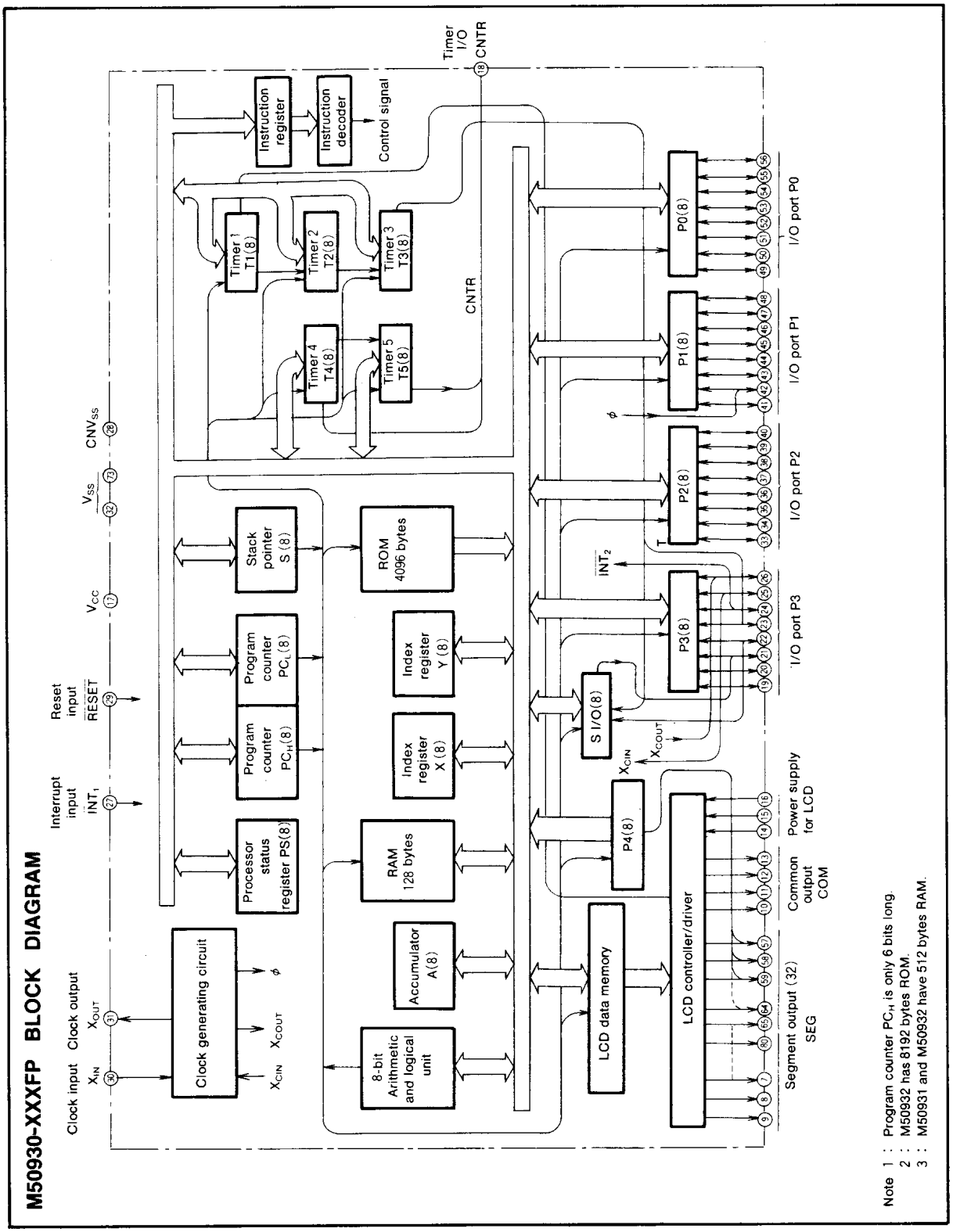
FEATURES

- Number of basic instructions 69
- Memory size
  - ROM ··· 4096 bytes (M50930-XXXFP, M50931-XXXFP)
    8192 bytes (M50932-XXXFP)
  - RAM ····· 128 bytes (M50930-XXXFP)
    512 bytes (M50931-XXXFP, M50932-XXXFP)
- Instruction execution time
  ····· 2μs (minimum instructions at 4MHz frequency)
- Single power supply
  - f(X_{IN})=4MHz ····· 5V±10%
  - f(X_{IN})=1MHz ····· 2.7V ≦ V_{CC} ≦ 5.5V(Typ.)
- Power dissipation
  - normal operation mode (at 4MHz frequency)
    ····· 15mW(V_{CC}=5V, Typ.)
  - low-speed operation mode (at 32kHz frequency for clock function) ····· 225μW (V_{CC}=5V, Typ.)
  - stop mode(at 25℃) ····· 5μW (V_{CC}=5V, Max.)
- RAM retention voltage (stop mode)
  ····· 2.0V ≦ V_{RAM} ≦ 5.5V
- Subroutine nesting ····· 64 levels (Max.)
- Interrupt ····· 8 types, 5 vectors
- 8-bit timer ····· 3 (2 when used as serial I/O)
- 16-bit timer ····· 1 (Two 8-bit timers make one set)
- Programmable I/O ports
  (Ports P0, P1, P2, P3) ····· 32
- Input ports (Port P4) ····· 8
- Serial I/O (8-bit) ····· 1
- LCD controller/driver (1/2, 1/3 bias, 1/2, 1/3, 1/4 duty)
  - segment output ····· 32
  - common output ····· 4
- Two clock generator circuits
  (One is for main clock, the other is for clock function)

APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment
Telephone

M50930-XXXFP BLOCK DIAGRAM



Note 1 : Program counter PC_H is only 6 bits long.
2 : M50932 has 8192 bytes ROM.
3 : M50931 and M50932 have 512 bytes RAM.

FUNCTIONS OF M50930-XXXFP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency).
Clock frequency			4.3MHz
Memory size	ROM		4096 bytes (8192 bytes for M50932-XXXFP)
	RAM		128 bytes (512 bytes for M50931-XXXFP and M50932-XXXFP)
	RAM for display LCD		16 bytes
Input/Output port	P0, P1, P2, P3	I/O	8-bit×4
	P4	Input	8-bit×1 (Port P4 are in common with SEG)
	SEG	LCD output	32-bit×1
	COM	LCD output	4-bit×1
Serial I/O			8-bit×1
Timers			8-bit timer×3 (2 when serial I/O is used)
			16-bit timer×1 (combination of two 8-bit timers)
LCD controller/driver	Bias		1/2, 1/3 bias selectable
	Duty ratio		1/2, 1/3, 1/4 duty selectable
	Common output		4
	Segment output		32 (SEG_{24}~SEG_{31} are in common with port P4)
Subroutine nesting			64 (max.)
Interrupt			Two external interrupts, Three timer interrupts (or two timer, one serial I/O)
Clock generating circuit			Two built-in circuits (ceramic or quartz crystal oscillator)
Supply voltage			2.7~5.5V (RAM retention voltage at clock stop is 2~5.5V)
Power dissipation	At high-speed operation V_{CC}=5V		15mW (at clock frequency X_{IN}=4MHz, typ.)
	At low-speed operation V_{CC}=5V		225μW (at clock frequency X_{CIN}=32kHz, typ.)
	At STOP mode		5μW (at clock stop, max.)
Input/Output characteristics	Input/Output voltage		5V
	Output current		I_{OH}=−2mA (V_{OH}=3V)
			I_{OL}=10mA (V_{OL}=2V)
			Pull-up current : Min. −30μA, max. −140μA, typ −70μA (V_{CC}=5V input voltage 0V)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package			80-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connect to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$, $P3_2$, $P3_1$, and $P3_0$ work as timer 3 overflow signal divided by 2 output pin (T), $\overline{INT_2}$ pin, X_{CIN} and X_{COUT} pins, respectively.
$P4_0$~$P4_7$	Input port P4	I/O	Port P4 is an 8-bit input port and can be used as segment output pins.
V_{L1}~V_{L3}	Voltage input for LCD	Input	These are voltage input pins for LCD. Supply voltage as $0V \leqq V_{L1} \leqq V_{L2} \leqq V_{L3} \leqq V_{CC}$. $0V \sim V_{L3}$ is supplied to LCD.
COM_0~ COM_3	Common output	Output	These are LCD common output pins. At 1/2 duty, COM_2 and COM_3 pins are not used. At 1/3 duty, COM_3 is not used.
SEG_0~ SEG_{23}	Segment output	Output	These are LCD segment output pins.
CNTR	Timer I/O	I/O	This is an output pin for the timer 4 and 5.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50930-XXXFP is shown in Figure 1. Address 3000_{16} to $3FFF_{16}$ are assigned for the built-in ROM area which consists of 4096 bytes (Addresses 2000_{16} to $3FFF_{16}$ are assigned for the built-in ROM area which consists of 8192 bytes for M50932-XXXFP). Addresses $3F00_{16}$ to $3FFF_{16}$ are a special address area (special page). By using the special page addressing mode of JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $3FF4_{16}$ to $3FFF_{16}$ are vector addresses used for the reset and interrupts (See interrupts chapter).

Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required.

The RAM, I/O port, timer, etc. addresses are already assigned for the zero page. Addresses 0000_{16} to $007F_{16}$ are assigned for the built-in RAM which consists of 128 bytes (Addresses 0000_{16} to $007F_{16}$ and 0100_{16} to $027F_{16}$ are assigned for the built-in RAM which consists of 512 bytes for M50931-XXXFP and M50932-XXXFP). This RAM is used as the stack during subroutine calls and interrupts, in addition to data storage.

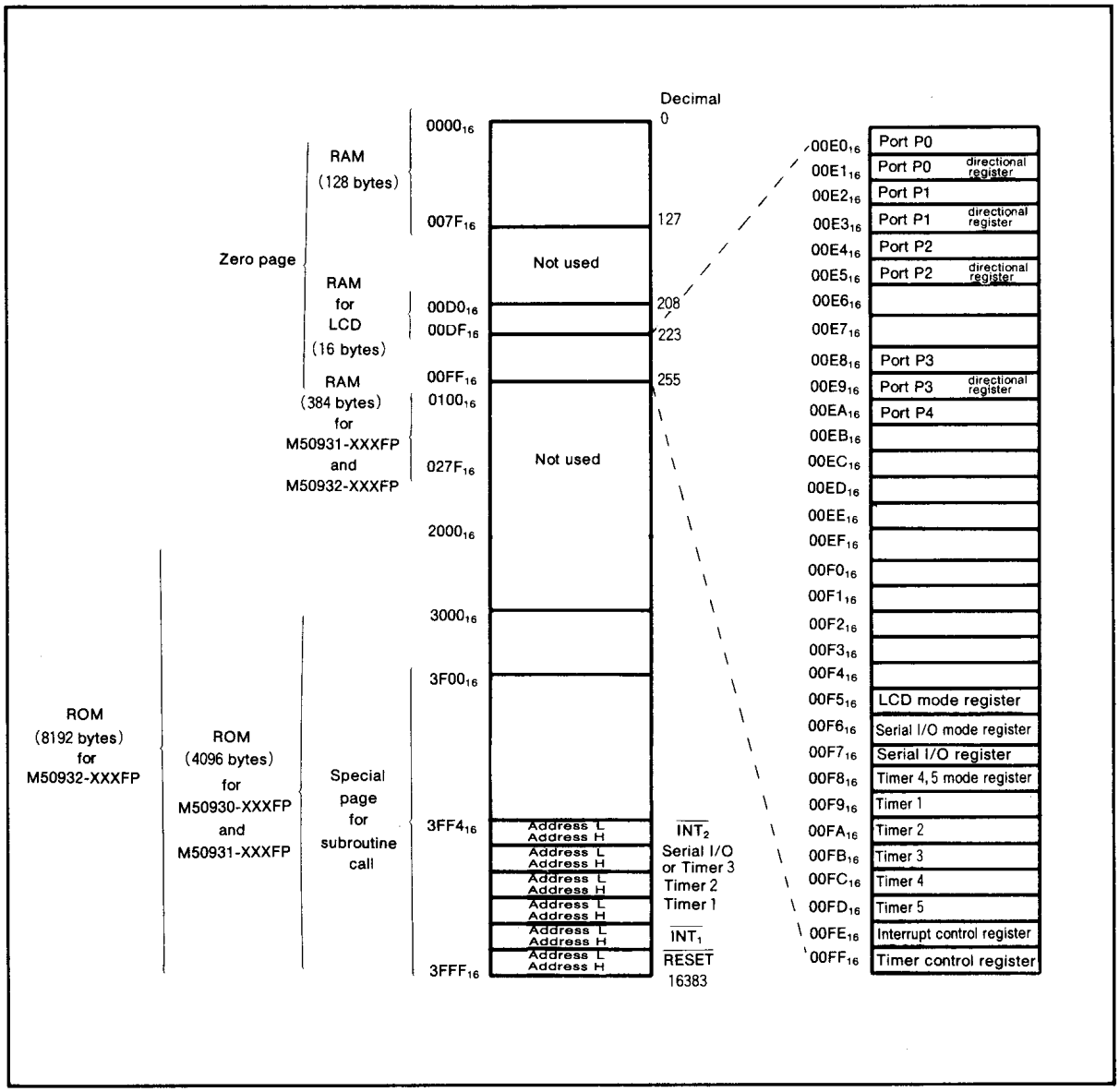


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, input/output, etc., is executed mainly through the accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register. In the index register X addressing mode, the value of the OPERAND added to the contents of the index register X specifies the real address. When the T flag in the processors status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register. In the index register Y addressing mode, the value of the OPERAND added to the contents of the index register Y specifies the real address.

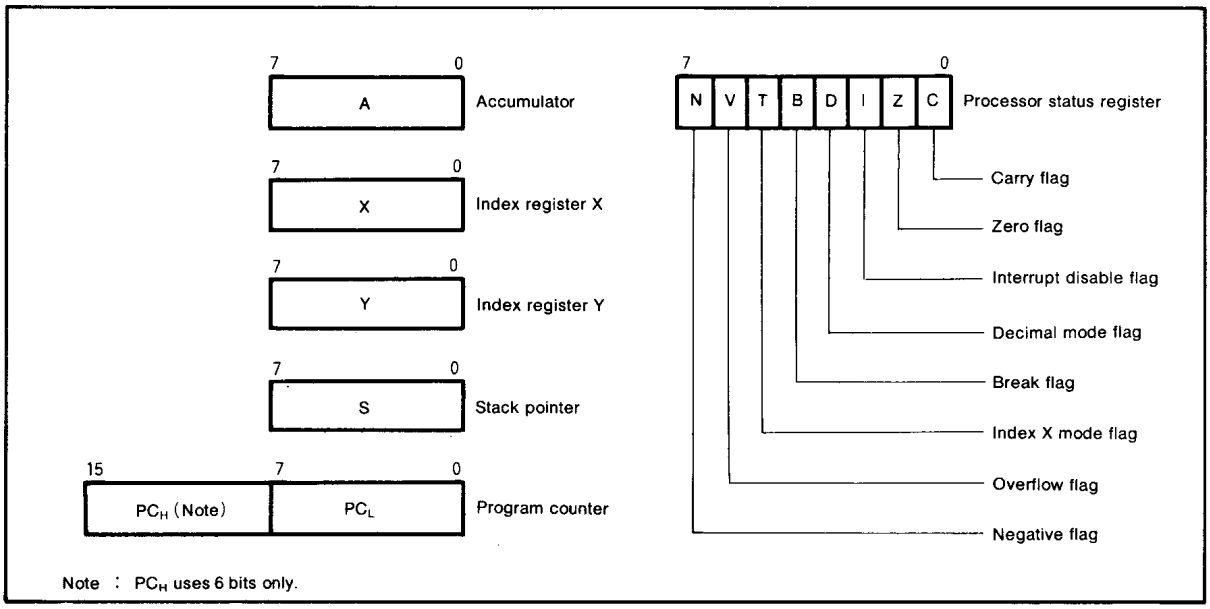


Fig.2 Register structure

STACK POINTER (S)

The stack pointer is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

When an interrupt occurs, the higher 8 bits of the program counter is pushed into the stack first, the stack pointer is decremented, and then the lower 8 bits of the program counter is pushed into the stack. Next the contents of the processor status register is pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter and processor status register data is popped off the stack in reverse order from above.

The accumulator is never pushed into the stack automatically, so a Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pop Accumulator instruction (PLA). It is executed in the reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed and popped to and from the stack with the PHP and PLP instructions, respectively.

During a subroutine call, only the Program Counter is pushed into the stack. Therefore, any registers that should not be destroyed should be pused into the stack manually. To return from a subroutine call, the RTS instruction is used.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PC_H is only 6 bits long.

PROCESSOR STATUS REGSITER (PS)

The 8-bit PS is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flags (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic Logic Unit (ALU) immediately after an operation. It is also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "0". If the result is not zero, the zero flag will be set to "1".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt is accepted, this flag is automatically set to "1" to prevent from other interrupts until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the B flag will be "1", otherwise, it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly, without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the T flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the V flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the N flag. There are no instructions for directly setting or resetting the N flag.

INTERRUPT

The M50930-XXXFP can be interrupted from eight sources; $\overline{INT_1}$, Timer 1, Timer 2, Timer 3 or Serial I/O, $\overline{INT_2}$ or Key on wake up, and BRK instruction.

The value of bit 2 of the serial I/O register (address $00F6_{16}$) determines whether the interrupt is from timer 3 or from serial I/O. When the bit 2 is "1" the interrupt is from serial I/O, and when bit 2 is "0" the interrupt is from timer 3. Also, when bit 2 is "1", parts of Port 3 are used for serial I/O. Bit 7 of the serial I/O register determines if an interrupt is from $\overline{INT_2}$ or from "Key on wake up". When bit 7 is "0", the interrupt is from $\overline{INT_2}$. When bit 7 is "1" the interrupt is from "key on wake up". "key on wake up" can only be used at power down by the STP or WIT instruction. These interrupts are vectored and thier priorities are shown in Table 1. Reset is included in this table since it has the same function as an interrupt.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, as discussed in the stack pointer section, and the interrupt disable flag (I) is set, and the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The Reset interrupt is the highest priority interrupt and can never be inhibited. Except for the Reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0". The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins go from "H" to "L"
(2) When the levels any pin of P2 goes "L" (at power down mode)
(3) When the contents of timer 1, timer 2, timer 3 or the counter of serial I/O go to "0"

These request bits can be reset by a program but can not be set.

Since the BRK instruction interrupt and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

Table 1. Interrupt vector address and priority.

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$3FFF_{16}$, $3FFE_{16}$
$\overline{INT_1}$	2	$3FFD_{16}$, $3FFC_{16}$
Timer 1	3	$3FFB_{16}$, $3FFA_{16}$
Timer 2	4	$3FF9_{16}$, $3FF8_{16}$
Timer 3 or serial I/O	5	$3FF7_{16}$, $3FF6_{16}$
$\overline{INT_2}$ or key on wake up (BRK)	6	$3FF5_{16}$, $3FF4_{16}$

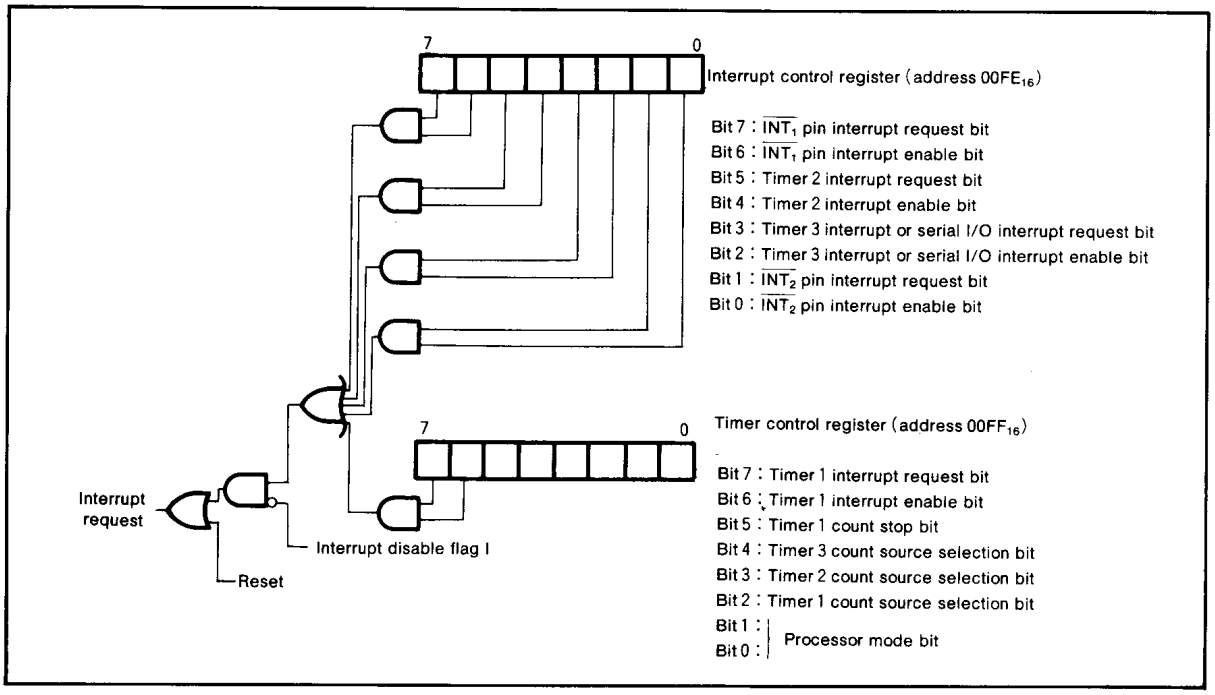


Fig. 3 Interrupt control

TIMER

The M50930-XXXFP has five timers; timer 1, timer 2, timer 3, timer 4 and timer 5. Timer 3 cannot be used when serial I/O is used (see serial I/O section). The count source for each timer can be selected by using bit 2, 3 and 4 of the timer control register (address $00FF_{16}$), as shown in Figure 4.

A block diagram of timer 1 through 5 is shown in Figure 6. All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timers is 1/(n +1), where n is the contents of timer latch.

The timer interrupt request bit is set at the next count pulse after the timer reaches "0". The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see Interrupt section). The starting and stopping of timer 1 is controlled by bit 5 of the timer control register. If bit 5 (address $00FF_{16}$) is "0", the timer starts counting. When bit 5 is "1", the timer stops.

After a STP instruction is executed, timer 2, timer 1, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 4 of the timer control register). This state is canceled if timer 2 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 1, count stop bit), bit 6 of the timer control register (timer 1 interrupt enable bit), and bit 4 of interrupt control register (timer 2 interrupt enable bit) must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

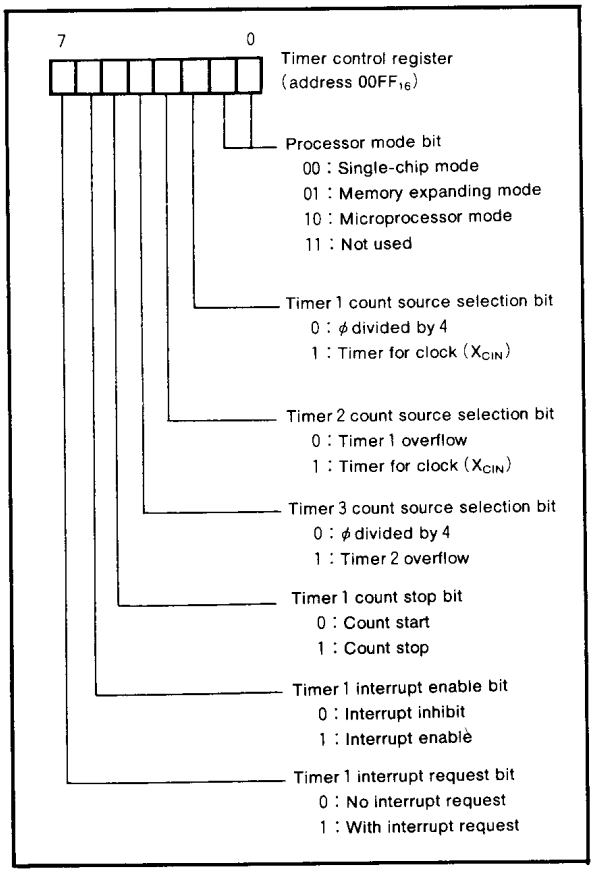


Fig.4 Structure of timer control register

TIMER 4 AND TIMER 5 MODES

(1) Timer Mode (00).
The internal clock divided by 4 is counted. When the timer counts to "0", the interrupt request bit is set to "1", the contents of the timer latch is reloaded, and the counting starts again.

(2) Pulse Output Mode (01).
The output level of the CNTR pin inverts each time the timer contents to zero.

(3) Event Counter Mode (10).
The same function is executed as that of mode "00", except that the counting source is input from the CNTR pin. The count decremented each time the CNTR input goes from "L" to "H".

(4) Pulse Width Measurement Mode (11).
This mode is used to measure the pulse width of a signal (between "L"s) input into the CNTR pin. The counting is done using the oscillation frequency divided by 4, and only while the CNTR pin is at a low level. When the contents of the counter reaches zero, the timer 5 overflow flag is set to "1", the timer is reloaded from the reload latch, and counting starts again. The overflow flag can be reset by writing a "0" to bit 7 of address $00F8_{16}$. The structure of timer 4, 5 mode register is shown in Figure 5.

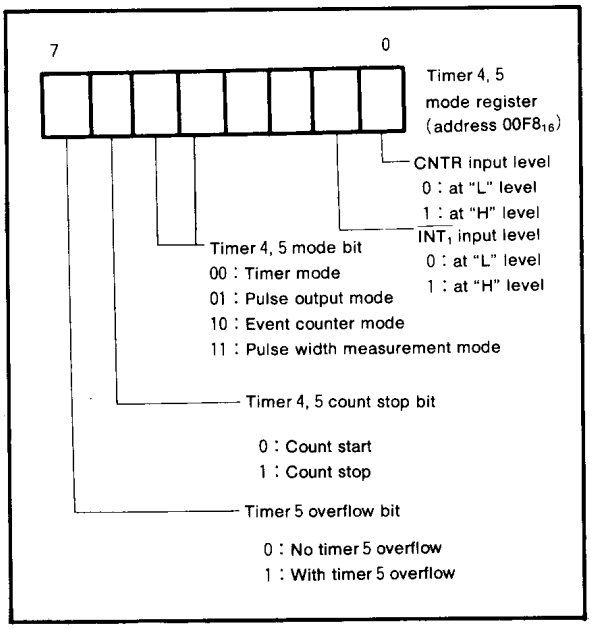


Fig.5 Structure of timer 4, 5 mode register

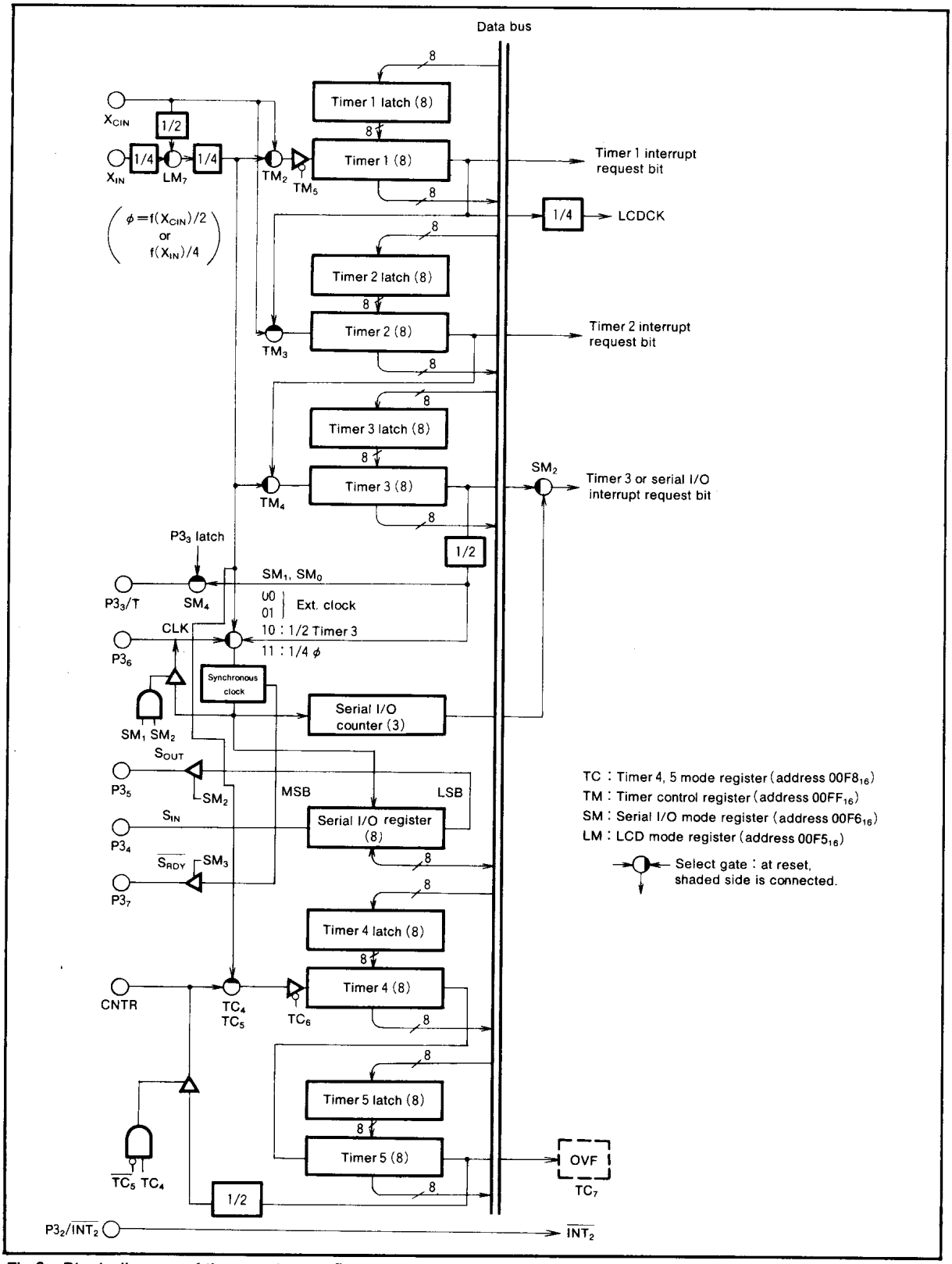


Fig.6 Block diagram of timers 1 through 5

PORT $P3_3$/TIMER 3 OUTPUT

The signal that timer 3 is divided by 2 is output from $P3_3$ (T), at the contents of bit 4 of the serial I/O mode register (address $00F6_{16}$) is "1".

WATCHDOG TIMER FUNCTION

Timer 4 and 5 can be used as a watchdog timer by connecting the CNTR pin and the $\overline{\text{RESET}}$ pin as shown in Figure 7, and by setting bit 4 and 5 of address $00F8_{16}$ to 01. At this time the output of the 1/2 divider counter (connected to timer 5) is initialized to "1" when data is written to timer 5. After a delay of 2.5 to 3.0μs (at $f(X_{IN})=4MHz$) after the reset is input, bits 4, 5, and 6 of the timer 4,5 mode register are initialized to 0. The initialization program to set the watchdog timer mode should have the following sequence:

(1) Set the pulse output mode after writing a value to timer 4 and 5 registers.

(2) If the program is running correctly, the CNTR pin should never go low due to data being continuously written to timer 5. If the program sequence is interrupted, timer 5 will overflow and the CNTR pin will output a "L" and retain this value until the Reset is executed.

(3) 2.5 to 3.5μs (at $f(X_{IN})=4MHz$) after a reset, the CNTR pin will be in high impedance state.

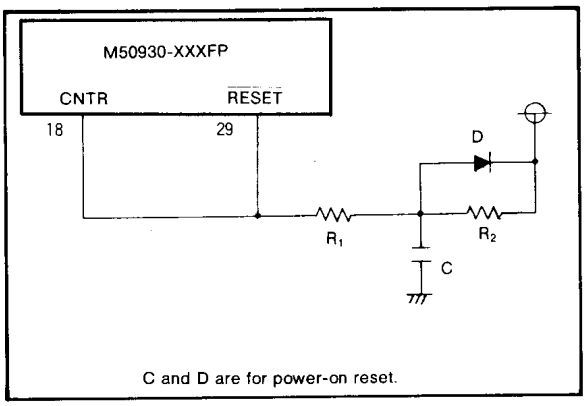


Fig.7 Reset circuit with the watchdog timer

SERIAL I/O

The block diagram of serial I/O is shown in Figure 8. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O (S_{OUT}, S_{IN}) pins are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively.

The serial I/O mode register (address $00F6_{16}$) is an 8-bit register. Bit 0 and 1 of this register is used to select a synchronous clock source. When these bits are (00) or (01), an external clock from $P3_6$ is selected. When these bits are (10), the overflow signal divided by two from timer 3 becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are (11), the internal clock ϕ divided by 4 (ie. 4μs at 4MHz) becomes the clock.

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If the external synchronous clock is selected, the clock is input to $P3_6$. And $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$, to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0"

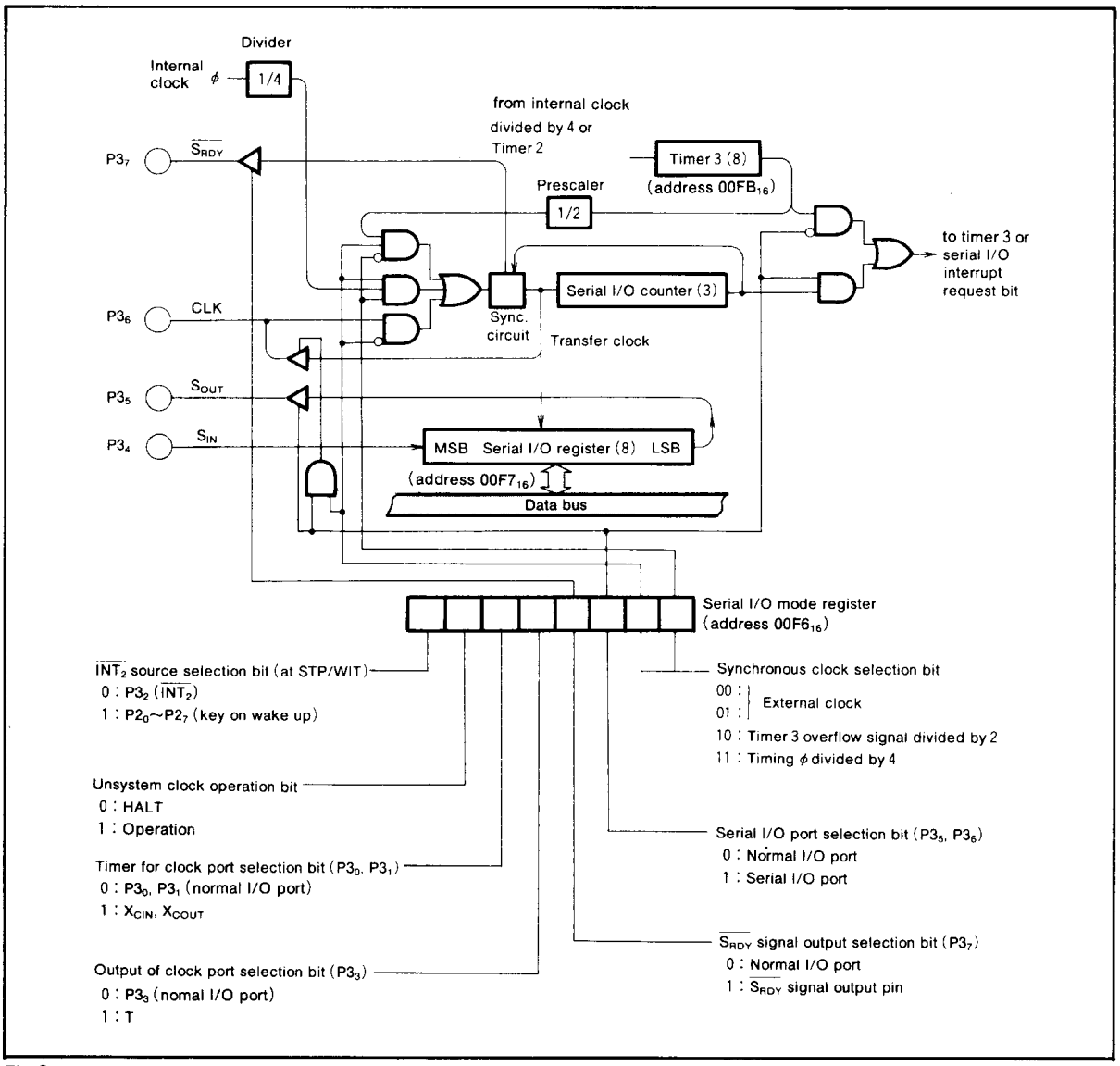


Fig.8 Block diagram of serial I/O

$P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 3. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDY}}$) or used as a nomal I/O pin (bit 3="0").

The function of serial I/O differs depending on the clock source: external clock or internal clock.

Internal clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the falling edge of write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M50930-XXXFP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock—If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 9, and connection between two M50930-XXXFPs' are shown in Figure 10. When using an external clock for transfer, the external clock must be held at "H" level when the serial I/O counter is initialized. When switching between the internal clock and external clock, the switching must not be performed during transfer. Also, the serial I/O counter must be initialized after switching.

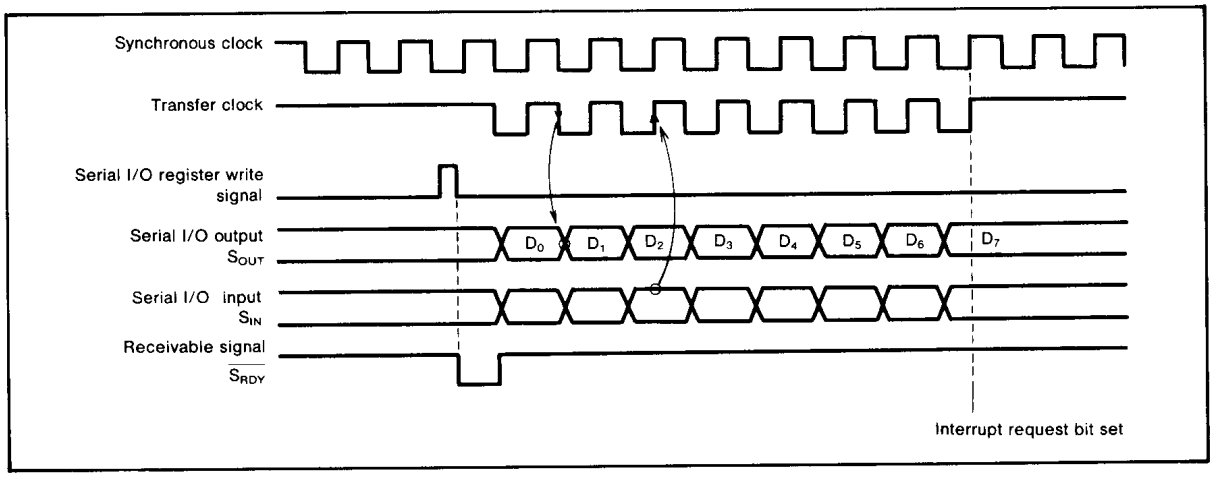


Fig.9 Serial I/O timing

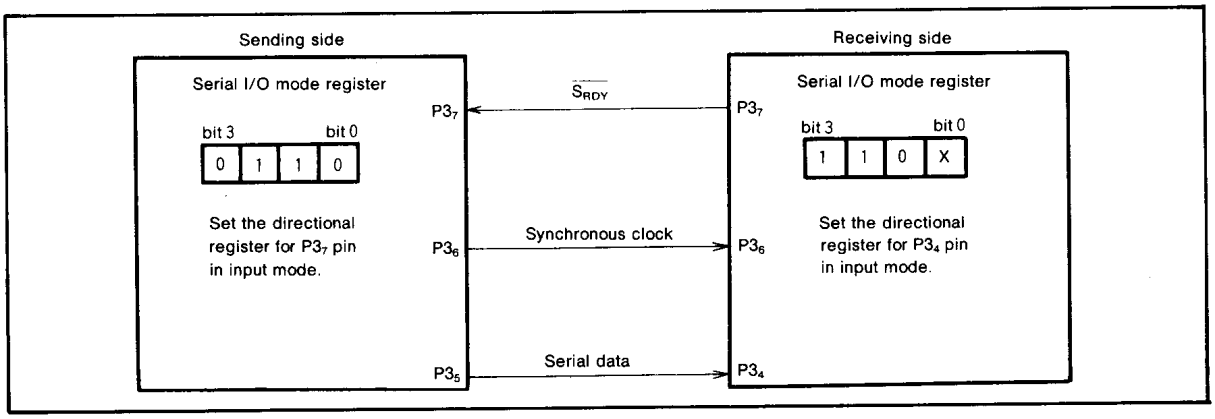


Fig.10 Example of serial I/O connection

LCD CONTROLLER/DRIVER

The M50930-XXXFP has internal LCD controllers and drivers. A Block diagram of LCD circuit is shown in Figure 13. The terminals for LCD consist of 4 common-pin and 32 segments pin. $SEG_{24} \sim SEG_{31}$ are in common with input P4. These pins are selected by bit 4 of the LCD mode register (LM_4, address $00F5_{16}$). Two biases (1/2 and 1/3) can also be selected. When bit 2 of the LCD mode register is "1", 1/2 bias is selected. When bit 2 is "0", 1/3 bias is selected. A 1/2, 1/3, or 1/4 duty cycle can also be selected. When bits 0 and 1 of the LCD mode register (LM_0, LM_1) is n, the duty ratio is 1/(n+1).

Address $00D0_{16} \sim 00DF_{16}$ is the designated RAM for the LCD display. When 1s' are written to these addresses, the corresponding segments of the LCD display panel are turned on. A map of the LCD display RAM is shown in Figure 12.

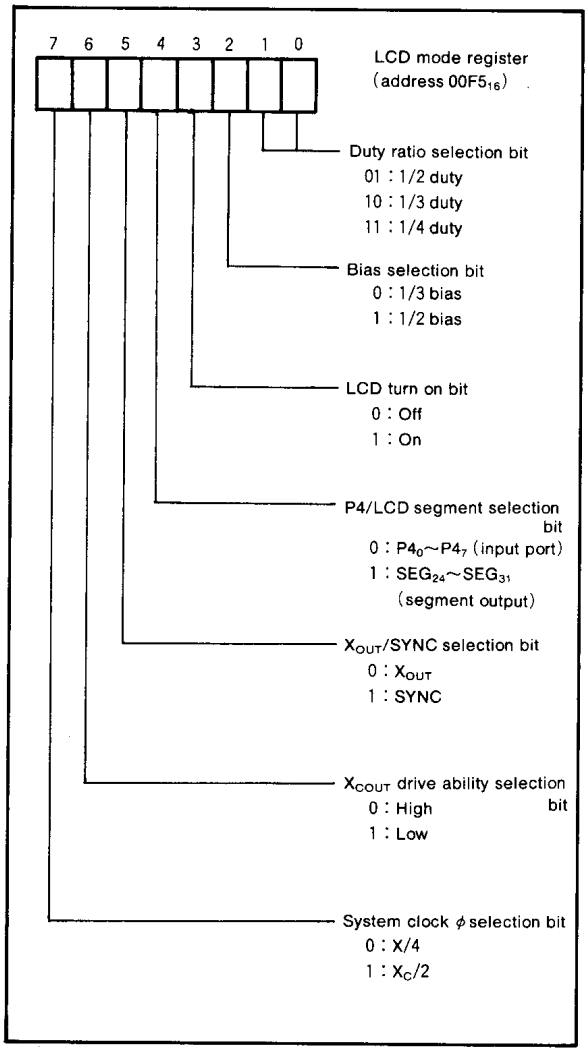


Fig.11 Structure of LCD mode register

The ON/OFF function for the LCD controller is controlled by bit 3 of the LCD mode register (LM_3). When this bit is "1" all the segments of the LCD are turned on. When this bit is "0" all the segments are turned off.

When a 1/2 bias is used, V_{L1} and V_{L2} should be shorted together. An example circuit for each bias is shown in Figure 14. Also Figure 15 shows an example of 1/2 bias, 1/4 duty drive waveforms and resulting voltage differential between SEG_n and COM_n and Figure 16 shows examples of drive waveforms for each bias and duty.

The LCDCK timing frequency (LCD driver timing) is generated internally and the frame frequency can be determined with the following equation:

$$f(LCDCK) = \frac{(\text{frequency of timer 1 count source})}{((\text{timer 1 setting}+1)\times 4)}$$

$$\text{Frame frequency} = \frac{f(LCDCK)}{n} \quad ; \text{ at 1/n duty}$$

Bit / Address	7	6	5	4	3	2	1	0
D0	1	1	1	1	0	0	0	0
D1	3	3	3	3	2	2	2	2
D2	5	5	5	5	4	4	4	4
D3	7	7	7	7	6	6	6	6
D4	9	9	9	9	8	8	8	8
D5	11	11	11	11	10	10	10	10
D6	13	13	13	13	12	12	12	12
D7	15	15	15	15	14	14	14	14
D8	17	17	17	17	16	16	16	16
D9	19	19	19	19	18	18	18	18
DA	21	21	21	21	20	20	20	20
DB	23	23	23	23	22	22	22	22
DC	25	25	25	25	24	24	24	24
DD	27	27	27	27	26	26	26	26
DE	29	29	29	29	28	28	28	28
DF	31	31	31	31	30	30	30	30
	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0

*Number in data memory area indicates corresponding segment.

Fig. 12 Map of RAM for LCD segment

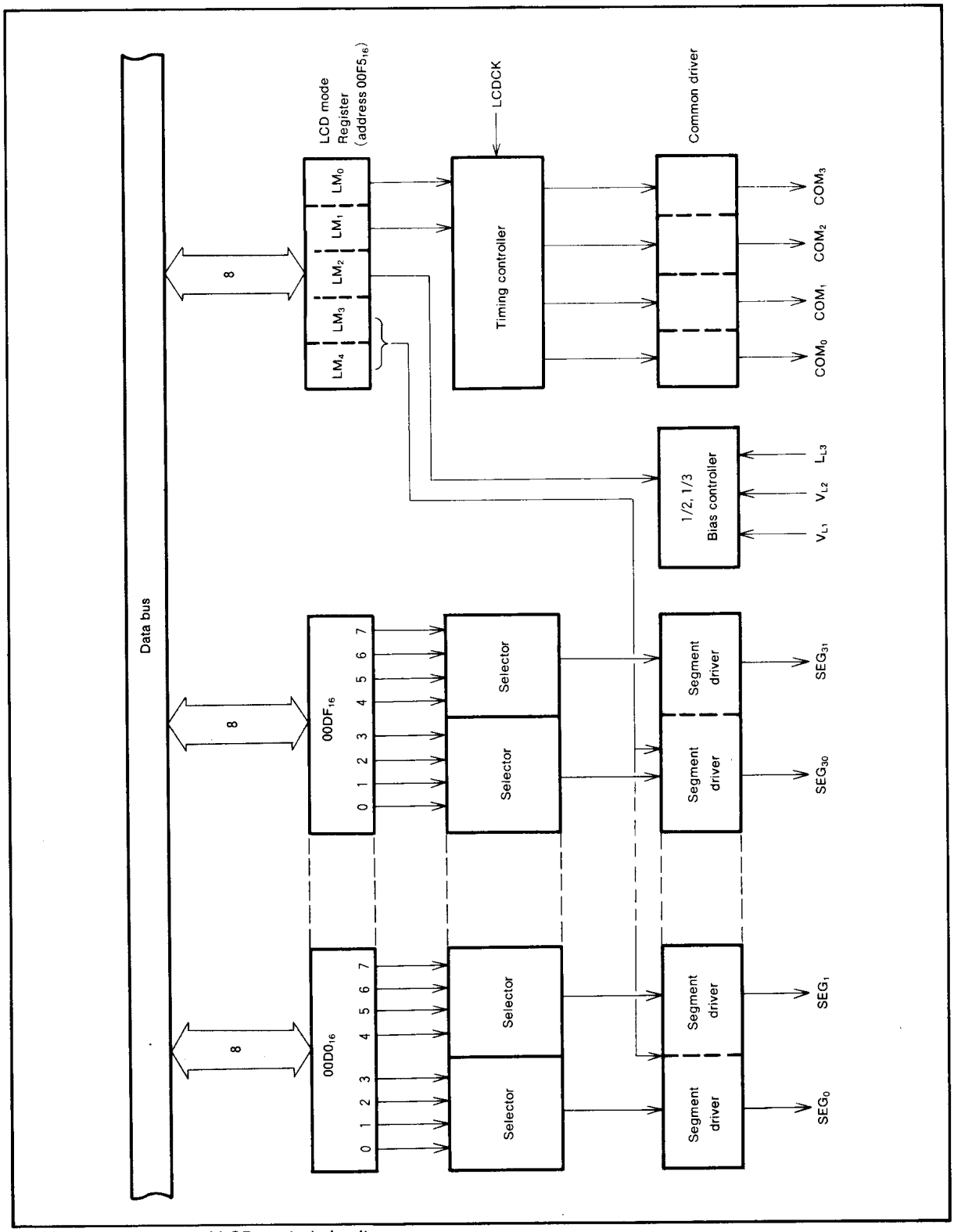


Fig.13 Block diagram of LCD control circuit

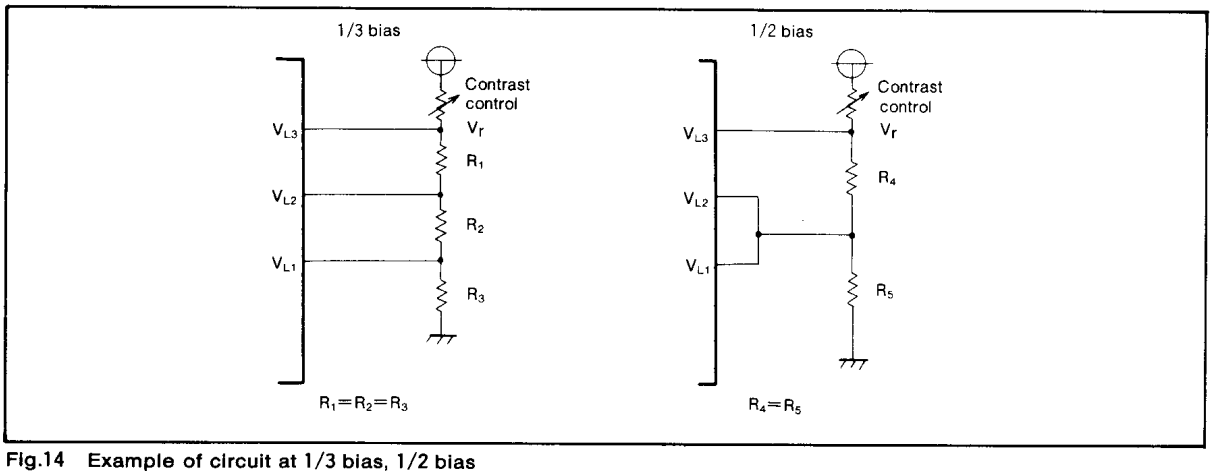


Fig.14 Example of circuit at 1/3 bias, 1/2 bias

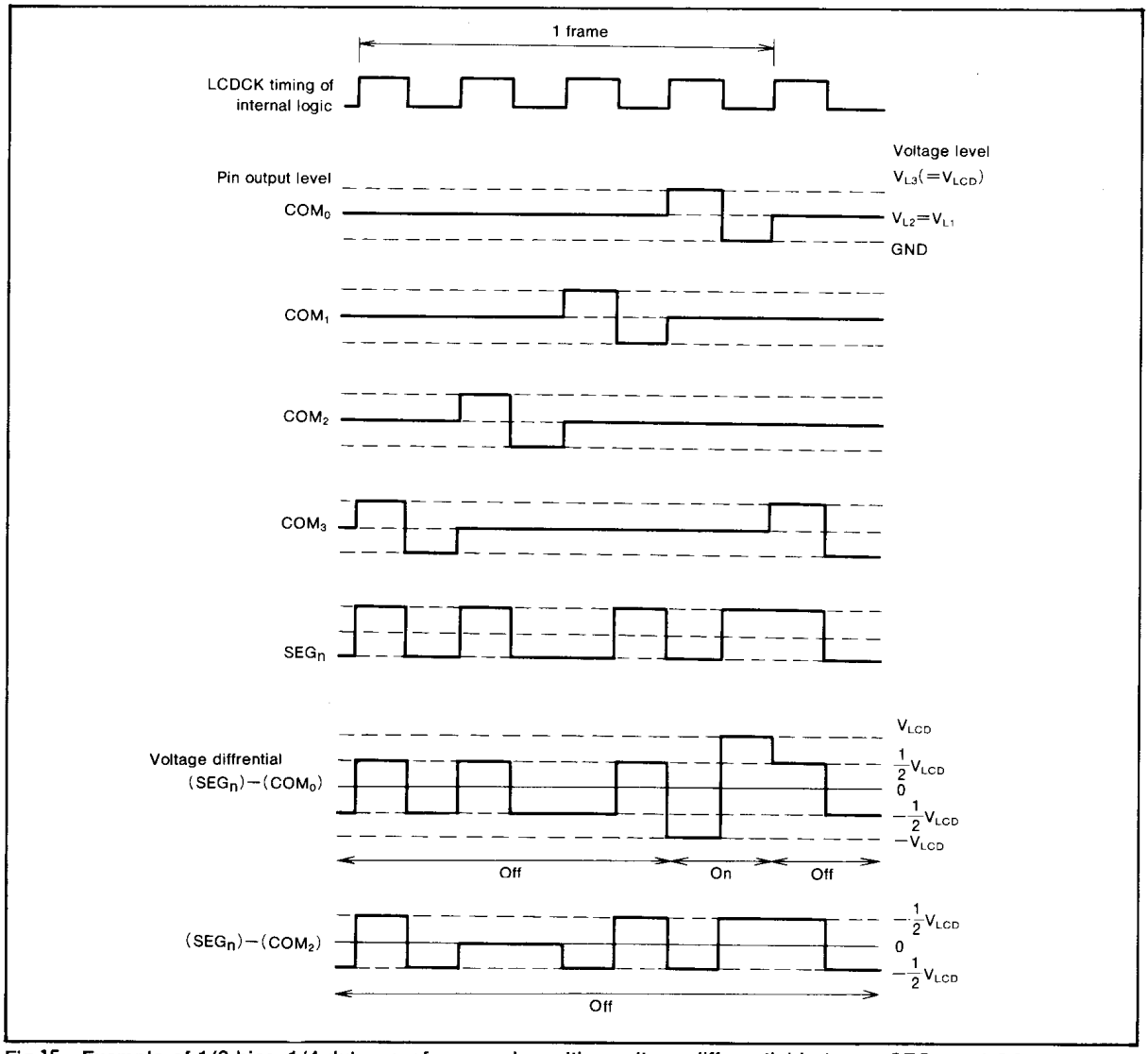


Fig.15 Example of 1/2 bias, 1/4 duty waveforms and resulting voltage differential between SEG_n and COM_n.

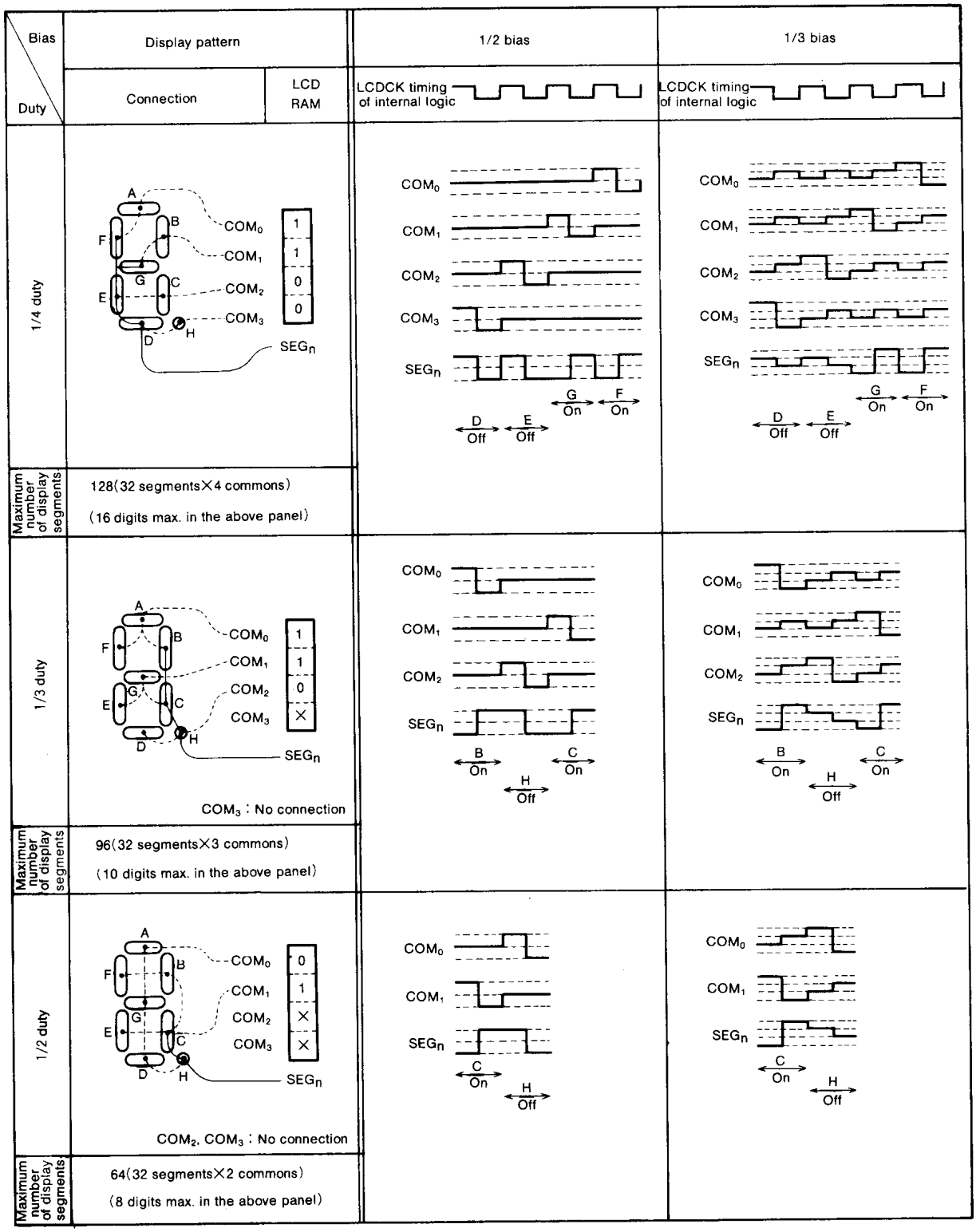


Fig.16 Example of drive waveforms for each bias and duty

KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P2 has a "L" level applied, after bit 7 of the serial I/O mode register (SM_7) is set to "1", an interrupt is generated and the microcomputer is returned to the nomal operatinge state. As shown in Figure 17, a key matrix can be connected to port P2 and the microcomputer can be returned to a normal state by pushing any key.

The key on wake up interrupt is common with the $\overline{INT}_2$ interrupt. When SM_7 is set to "1", the key on wake up function is selected. However, key on wake up cannot be used in the normal operating state. When the microcomputer is in the normal operating state, both key on wake up and $\overline{INT}_2$ are invalid.

In order to enter the power down state generated by the STP or WIT instruction at the interrupt disable flag (I) is "0" and SM_7 is "1", all of port P2 must be input "H".

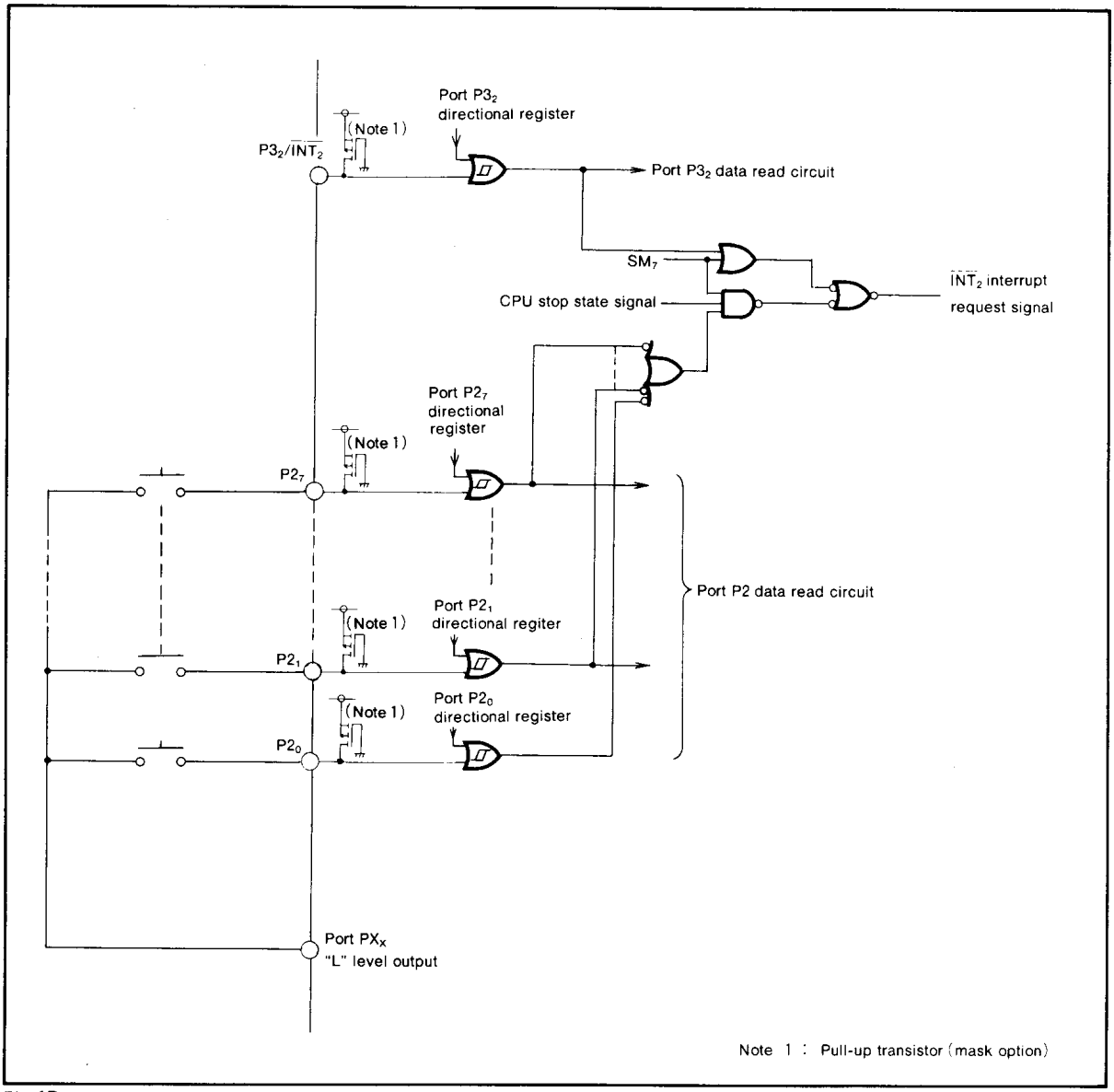


Fig.17 Block diagram of port P2 and $P3_2$, and example of wired at used key on wake up

RESET CIRCUIT

The M50930-XXXFP is reset according to the sequence shown in Figure 20. It starts the program from the address formed by using the content of address $3FFF_{16}$ as the high order address and the content of the address $3FFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for at least 8 rising edges from X_{IN} while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 18.

An example of the reset circuit is shown in Figure 19.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

		Address	
(1)	Port P0 directional register	($E1_{16}$)	00_{16}
(2)	Port P1 directional register	($E3_{16}$)	00_{16}
(3)	Port P2 directional register	($E5_{16}$)	00_{16}
(4)	Port P3 directional register	($E9_{16}$)	00_{16}
(5)	LCD mode register	($F5_{16}$)	00_{16}
(6)	Serial I/O mode register	($F6_{16}$)	00_{16}
(7)	Timer 4, 5 mode register	($F8_{16}$)	0 0 0 0
(8)	Interrupt control register	(FE_{16})	00_{16}
(9)	Timer control register	(FF_{16})	00_{16}
(10)	Interrupt disable flag for processor status register	(PS)	1
(11)	Program counter	(PC_H)	Contents of address $3FFF_{16}$
		(PC_L)	Contents of address $3FFE_{16}$

Since the contents of both registers other than those listed above (including timers and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values.

Fig.18 Internal state of microcomputer at reset

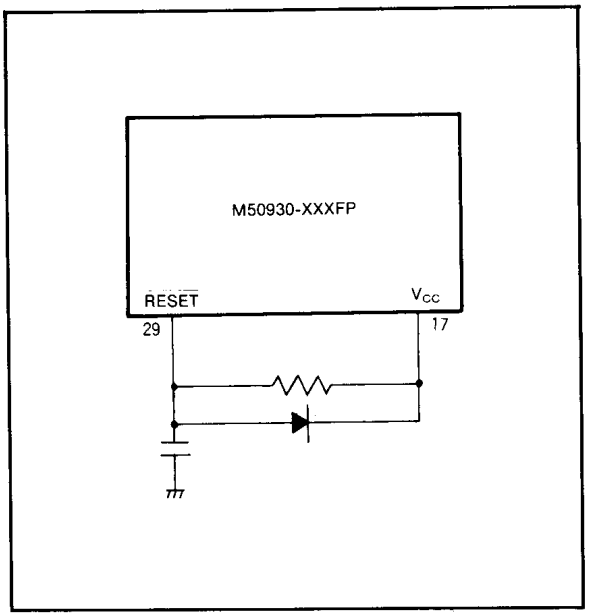
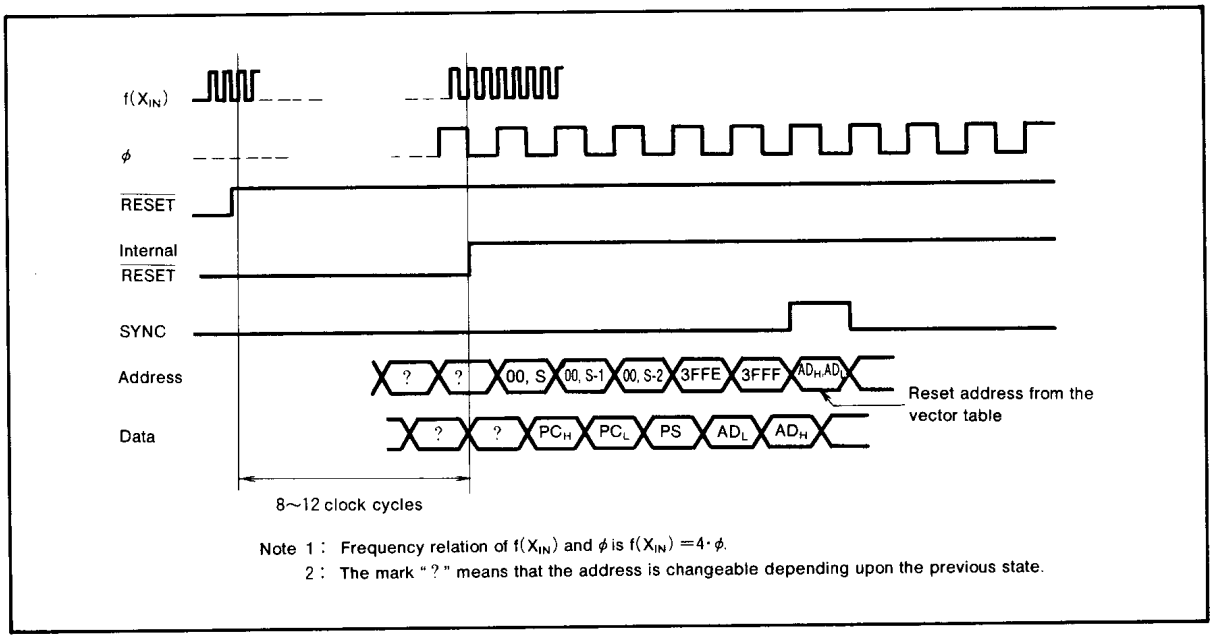


Fig.19 Example of reset circuit



Note 1 : Frequency relation of $f(X_{IN})$ and ϕ is $f(X_{IN}) = 4 \cdot \phi$.
2 : The mark " ? " means that the address is changeable depending upon the previous state.

Fig.20 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs and pull-up transistor options available. As shown in Figure 1, P0 can be accessed as memory through zero page address $00E0_{16}$. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address $00E1_{16}$) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port register and output. When data is read from the output port, the output pin level is not read, only the latched data of the port register is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state.

Depending on the status of the processor status bits (bit 0 and bit 1 of address $00FF_{16}$), three different modes can be selected; single-chip mode, memory expanding mode and microprocessor mode. For more details, refer to the timing diagram shown in Figure 24.

(2) Port P1

In the single chip mode, Port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's. For more details, see the processor mode information. Following the execution of STP or WIT instruction, P2 can be used to generate the "wake up mode". This mode is used to bring the microcomputer back in its normal operating mode after being in the power- down mode.

(4) Port P3

Port P3 has the same functions as P0 except that part of P3 is common with the serial I/O lines (ie. output of timer 3, input/output of timer clock, and interrupt input).

(5) Segment Output (SEG_0~SEG_{23})

These ports drive and control the LCD segments.

(6) Port P4

Port P4 is an 8-bit input port which can be used as a LCD segment output port.

(7) Common output (COM_0~COM_3)

These port provides output drive and control for the LCD common lines.

(8) Power Supply for LCD. (V_{L1}~V_{L3})

Supplies power to the LCD terminals.

(9) $\overline{INT_1}$

The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 7 of address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L". This input level is read into bit 1 of the timer 4 and 5 mode register (address $00F8_{16}$).

(10) $\overline{INT_2}$ ($\overline{INT_2}$/$P3_2$)

The $\overline{INT_2}$ pin is an interrupt input pin common with $P3_2$. When $P3_2$'s directional register is set for input ("0"), this pin can be used as an interrupt input. The $\overline{INT_2}$ interrupt request bit (bit 1 of address $00FE_{16}$) is automatically set to "1" when the input level of this pin changes from "H" to "L".

(11) CNTR

The CNTR pin is an I/O pin of timers 4 and 5. The input level is read into bit 0 of the timer 4 and 5's mode register (address $00F8_{16}$).

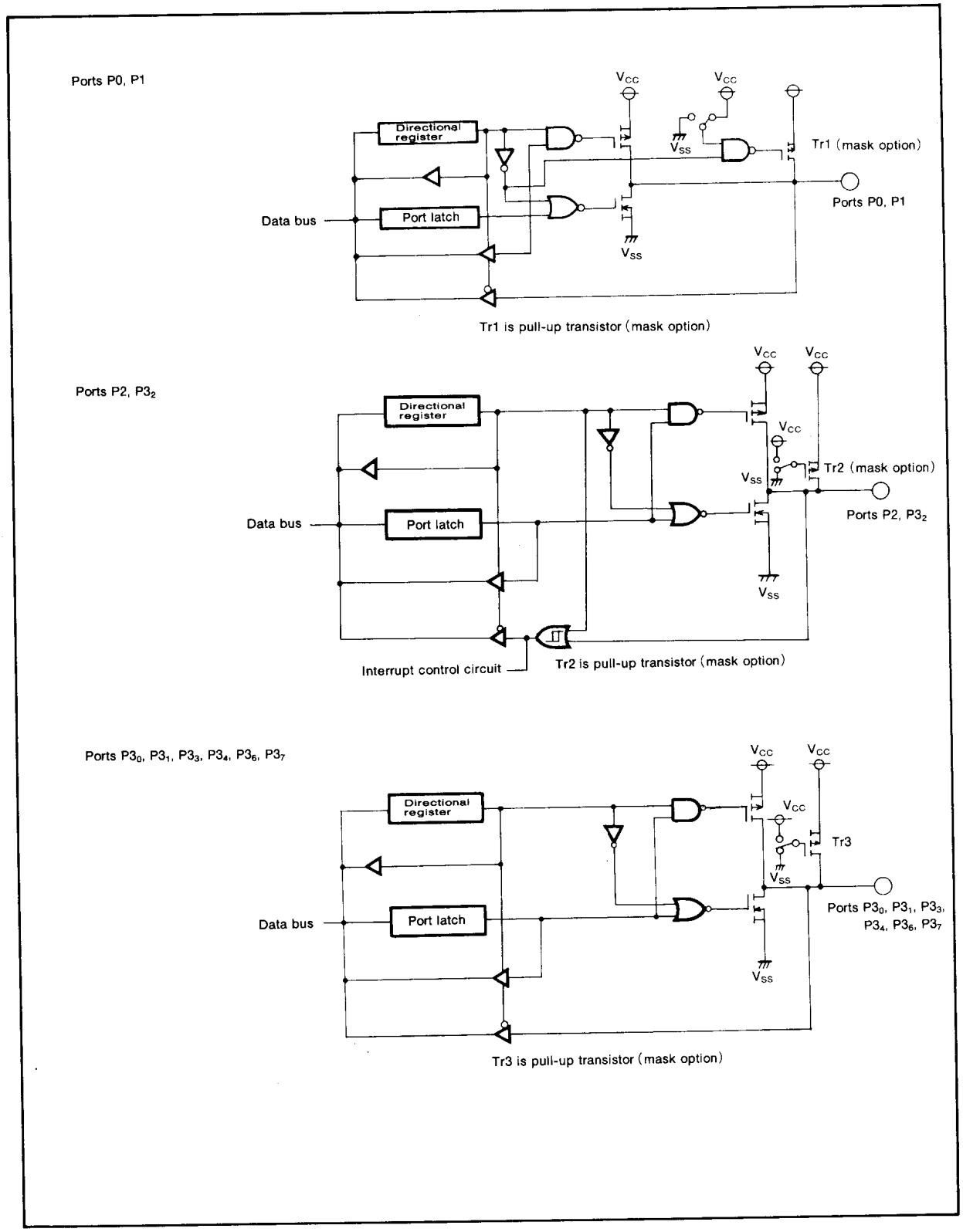
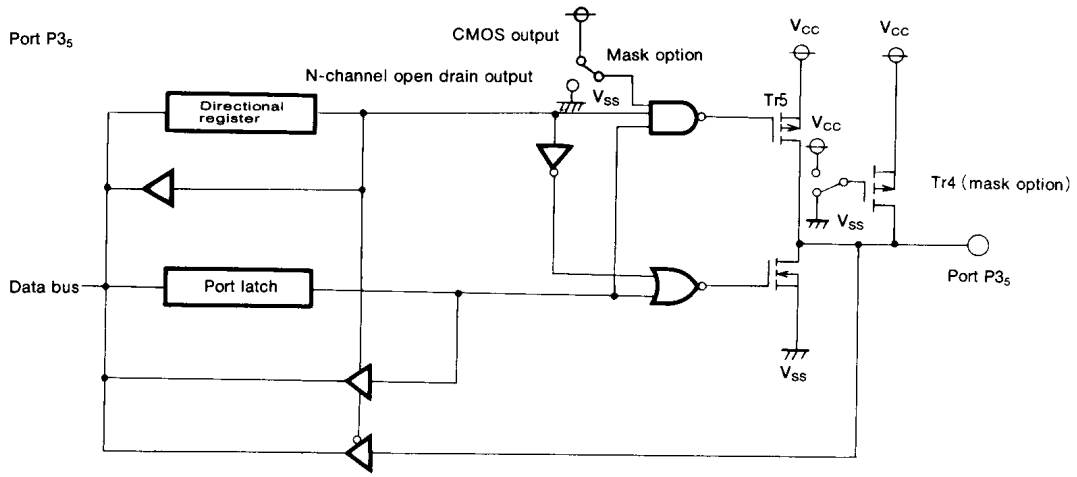
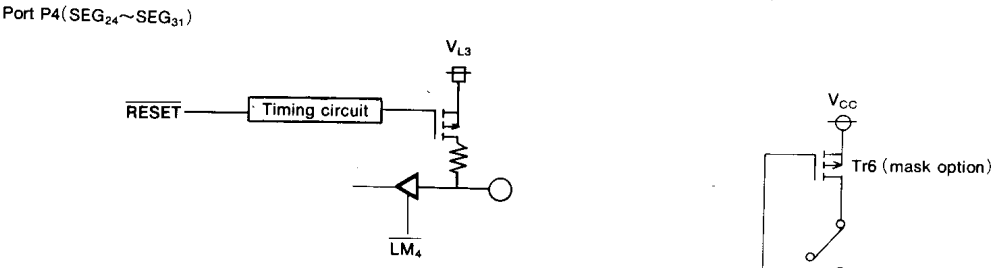


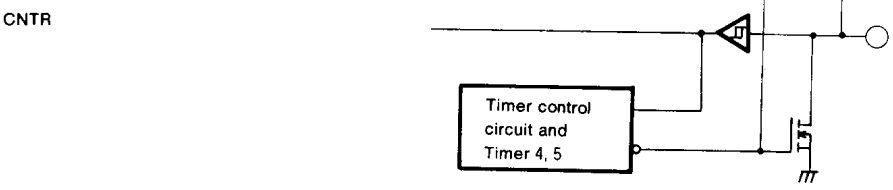
Fig.21 Block diagram of ports P0~P3



Tr4 is pull-up transistor (mask option)

Tr5 is P-channel output transistor (mask option)





Tr6 is pull-up transistor (mask option only for M50932-XXXFP)

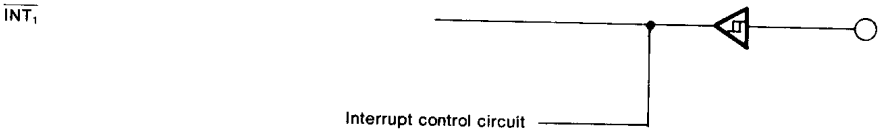
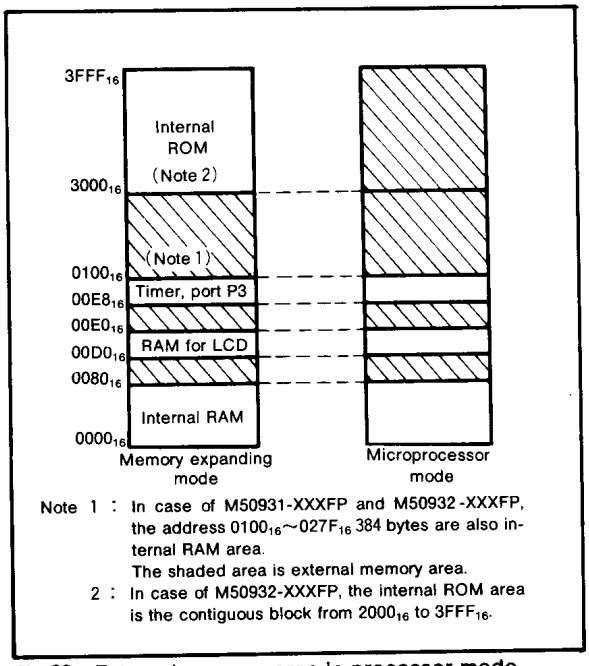


Fig.22 Block diagram of ports P3, P4, CNTR, and $\overline{INT_1}$

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 of address $00FF_{16}$), three different operation modes can be selected; single-chip mode, memory expanding mode and microprocessor mode. In the memory expanding mode and microprocessor mode, ports P0~P2 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports. The function of the X_{OUT} pin can also be changed. For more details see Figure 24.

The memory map of the single-chip mode is illustrated in Figure 1, and the other modes are shown in Figure 23. By connecting the CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode register. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. The three different modes are explained as follows:



Note 1 : In case of M50931-XXXFP and M50932-XXXFP, the address 0100_{16}~$027F_{16}$ 384 bytes are also internal RAM area.
The shaded area is external memory area.
2 : In case of M50932-XXXFP, the internal ROM area is the contiguous block from 2000_{16} to $3FFF_{16}$.

Fig.23 External memory area in processor mode

(1) Single-chip mode [00]
The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0~P2 will work as original I/O ports.

(2) Memory expanding mode [01]
The microcomputer will be changed to the memory expanding mode if CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient. Ports P0 and P1 are used as address output with the original I/O function lost. Port P2 is used as D_7~D_0 data I/O with the original I/O function lost. Port $P1_7$ and $P1_6$ works as R/$\overline{W}$ and ϕ.

(3) Microprocessor mode [10].
After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode. This mode is the same as the memory expanding mode except that the internal ROM is disable and external ROM is needed. The relationship between the input level of the CNV_{SS} and the processor mode is shown in Table 2.
The SYNC signal is output from the X_{OUT} pin in every mode except the single-chip mode, when 10V is supplied to the $\overline{RESET}$ pin or when bit 5 of the LCD mode register is set to "1". The SYNC signal becomes a synchronous signal that goes to "H" level while the Op code is being fetched. When the SYNC output signal is selected, the original function of the X_{OUT} pin is lost. In addition, if LM_7=1 and SM_6=0, the SYNC signal is not output from the X_{OUT} pin.

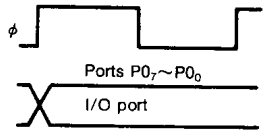
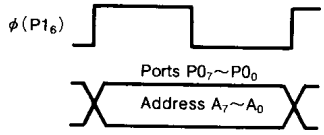
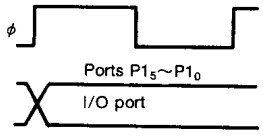
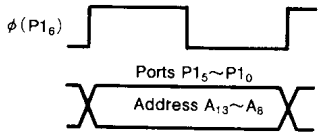
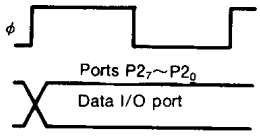
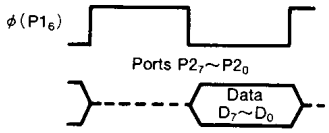
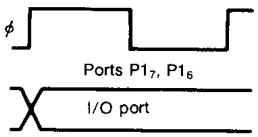
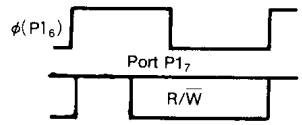
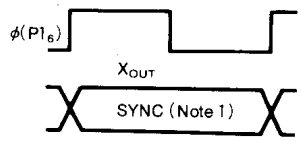
Port \ Mode	TM_1 = 0, TM_0 = 0 Single-chip mode	TM_1 = 0, TM_0 = 1 Memory expanding mode	TM_1 = 1, TM_0 = 0 Microprocessor mode
Port P0			Same as left
Port P1 lower 6 Bits			Same as left
Port P2			Same as left
Port P1 higher 2 bits			Same as left
X_{OUT}			Same as left

Fig.24 Processor mode and functions of ports P0~P2 and X_{OUT}

Note 1 : In order to use X_{OUT} pin as SYNC output, put $\overline{RESET}$ to 10V or set bit 5 of the address $00F5_{16}$ to "1".
When LM_7=1 and SM_6=0, X_{OUT} does not output SYNC.

Table 2. Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Microprocessor mode	The microprocessor mode is set by the reset.

CLOCK GENERATING CIRCUIT

The M50930-XXXFP has two internal clock generating circuit. Figure 27 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ. Bit 7 of LCD mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 25 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacture's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input form the $X_{IN}(X_{CIN})$ pin and leave the $X_{OUT}(X_{COUT})$ pin open. A circuit example is shown in Figure 26.

The M50930-XXXFP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 1 and timer 2 are forcibly connected and $\phi/4$ is selected as timer 1 input. Before executing the STP instruction, appropriate values must be set in timer 1 and timer 2 to enable the oscillator to stabilize when restarting oscillation. Before executing the STP instruction, the timer 1 count stop bit must be set to supply ("0"), timer 1 interrupt enable bit and timer 2 interrupt enable bit must be set to disable ("0"), and timer 2 interrupt request bit must be set to no request ("0").

Oscillation is resarted (release the stop mode) when INT_1, INT_2, or serial I/O interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 2 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be kept to the $\overline{RESET}$ pin until the oscillattion stabilizes because no wait time is generated.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock (45μA Typ. at $f(X_{CIN})=32kHz$). X_{IN} clock oscillation is stopped when the bit 6 of LCD mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. An "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 28 shows the transition of states for the system clock.

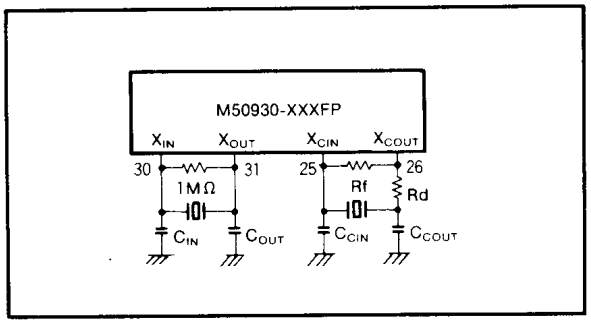


Fig.25 External ceramic resonator circuit

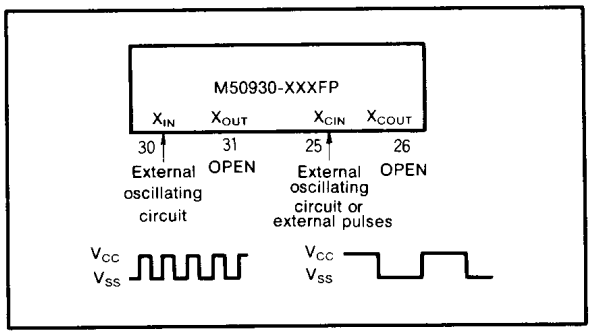


Fig.26 External clock input circuit

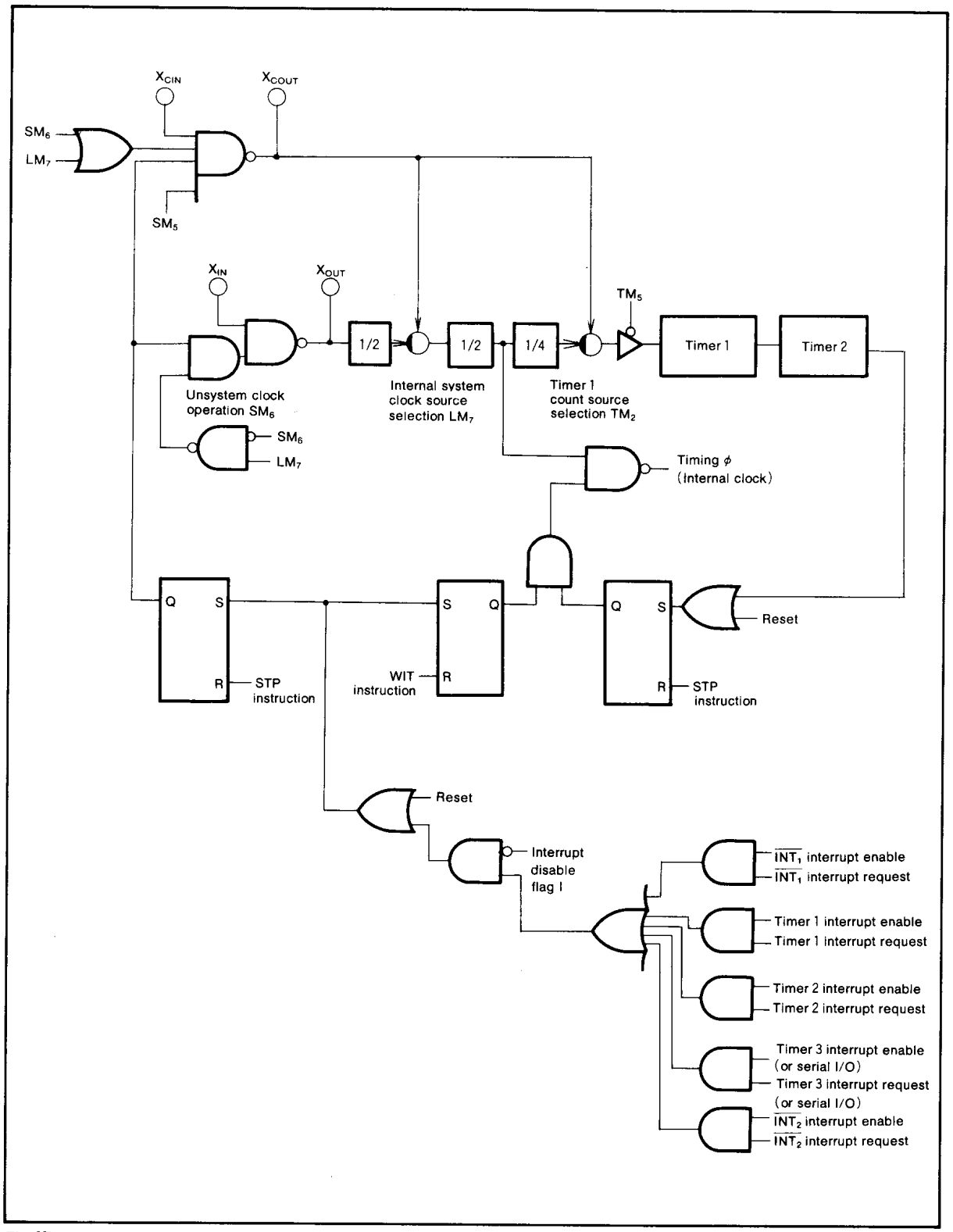
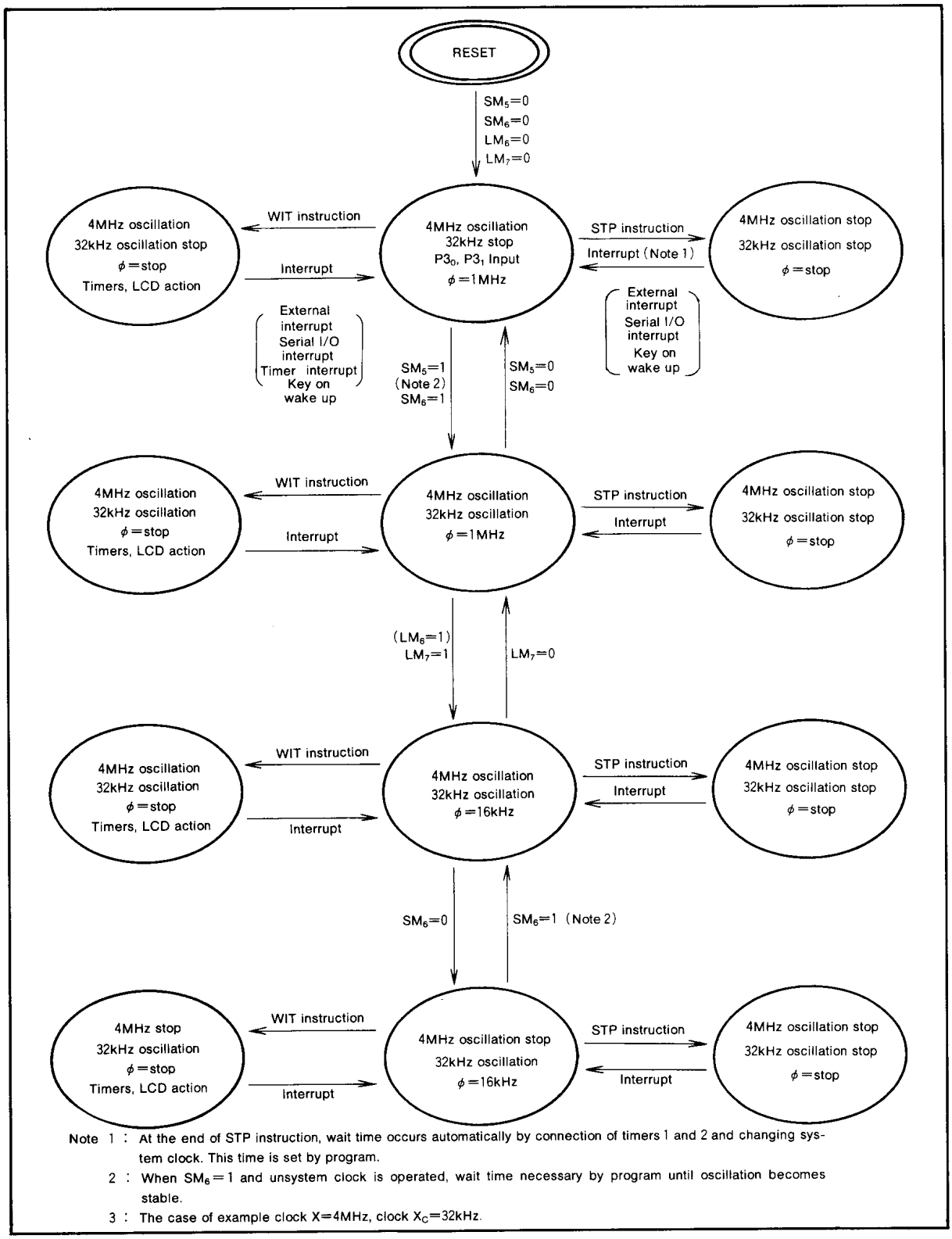


Fig.27 Block diagram of clock generating circuit



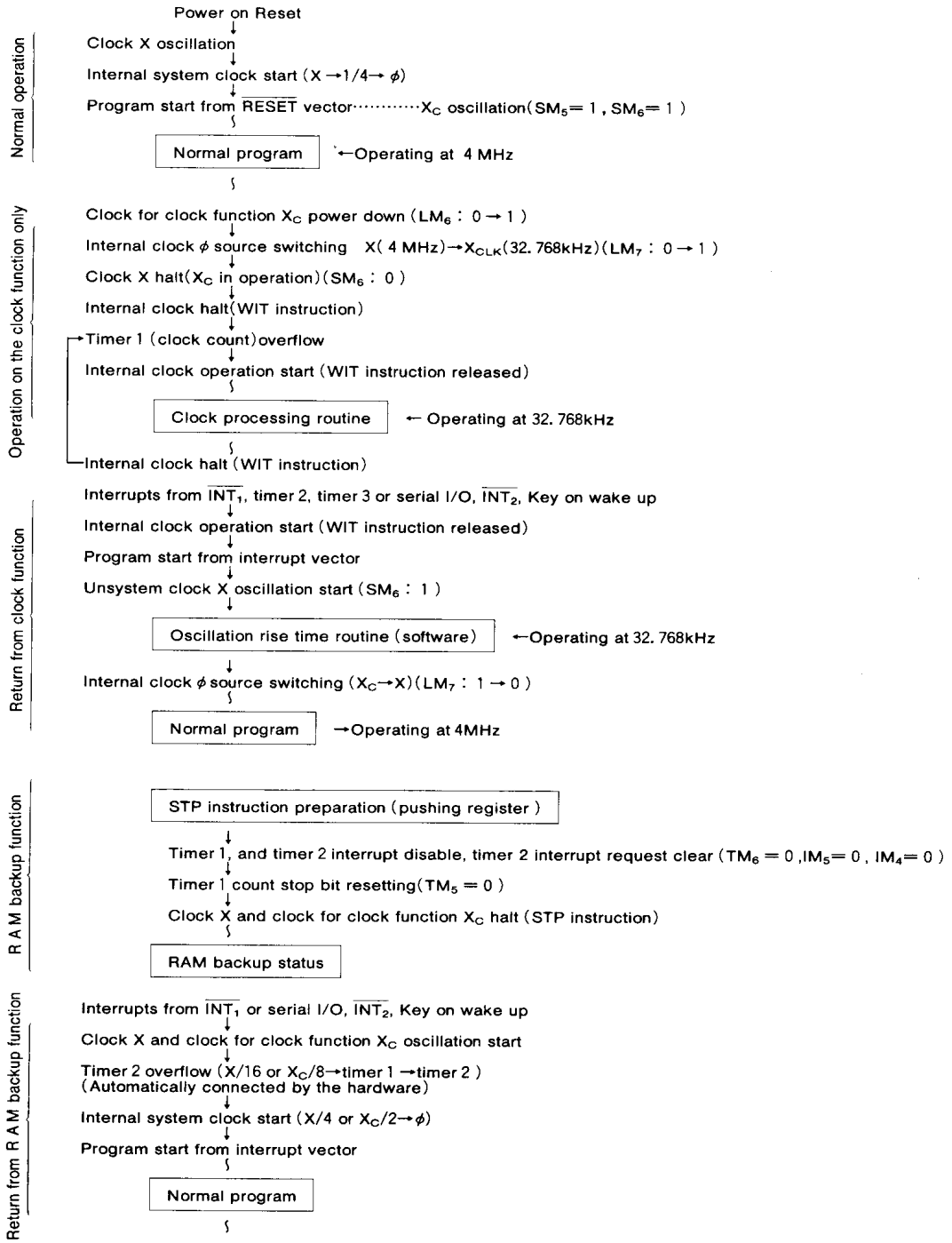
Note 1 : At the end of STP instruction, wait time occurs automatically by connection of timers 1 and 2 and changing system clock. This time is set by program.

2 : When $SM_6 = 1$ and unsystem clock is operated, wait time necessary by program until oscillation becomes stable.

3 : The case of example clock X=4MHz, clock X_C=32kHz.

Fig.28 Transition of states for the system clock

<An example of flow for system>



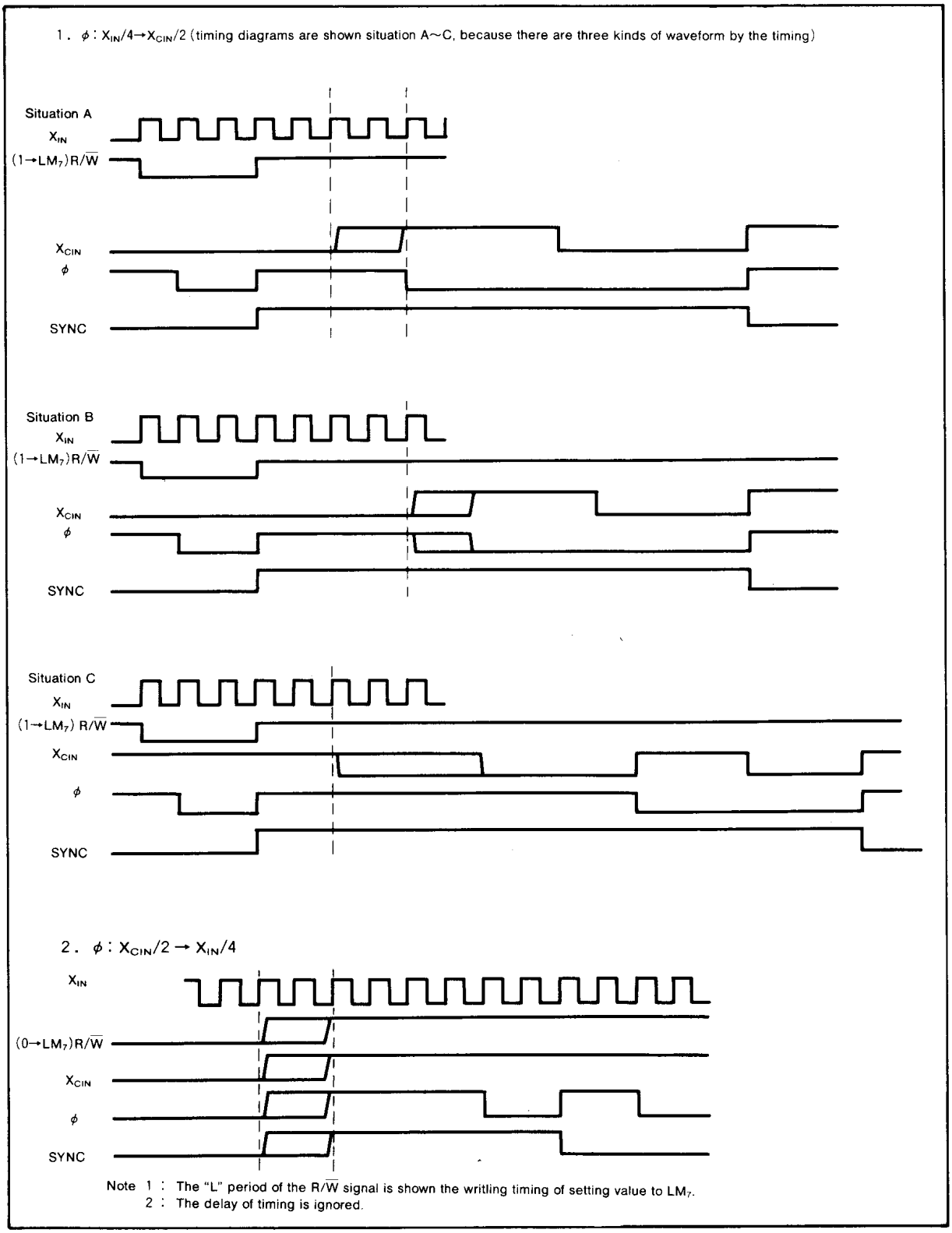


Fig.29 Timing diagram of the changing system clock

PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one insturction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) When the timer 4 and the timer 5 are used at event counter mode, read the contents of these timers either while the input of the these timers are not changing or after timer 4, 5 count stop bit (bit 6 of address $00F8_{16}$) is set to "1".
Also, when the timer 1, timer 2, or timer 3 is input the clock except $\phi/4$ or it divided by timer, control the same as above.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC,CLC, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

(6) When LCD turn-on bit (bit 3 of address $00F5_{16}$) of the LCD mode register is "1", don't stop the timers or count source for timers.

(7) The serial I/O counter must be initialized (write to $00F7_{16}$) after switching the transfer clock source.

(8) When using an external clock as the transfer clock source, the serial I/O counter must be initialized while the external clock is at "H" level.

(9) The timer 1 and timer 2 must be set the necessary value immediately before the execution of a STP instruction.

(10) When using pins $P3_0$ and $P3_1$ as clock I/O pins, the pull-up option must not be used.

(11) Notes on controlling the clock generation circuit

① When system clock is changed $X_{IN}/4$ to $X_{CIN}/2$, set LM_7 to "1" after oscillation is stable by the software in side of clock X_C.

② When system clock is changed $X_{CIN}/2$ to $X_{IN}/4$, set LM_7 to "0" after oscillation is stable by the software in side of clock X.

③ When SM_5 is "0" or when LM_7 is "0" and SM_6 is "0", LM_6 is automatically set to "0" by the hardware.

④ When system clock selection bit (bit 7 of address $00F5_{16}$) of the LCD mode register is "1", don't set SM_5 to "0".

⑤ In single-chip mode, the X_{OUT} pin uses as X_{OUT} output except setting value of LM_5.

⑥ The other than single-chip mode and the input voltage for $\overline{RESET}$ pin is 10V, X_{OUT} pin uses as SYNC output except setting value of LM_5.

Just for reference, timing diagram of the changing system clock are shown in Figure 29.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mark specification form

(3) ROM data ..... EPROM 3sets

Write the following option on the mask ROM confirmation from

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port $P3_5/S_{OUT}$ output format
- CNTR pin pull-up transistor (M50932-XXXFP only)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Output transistor are "off"	−0.3∼7	V
V_i	Supply voltage for LCD V_{L1}∼V_{L3}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, X_{IN}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $\overline{INT_1}$, CNV_{SS}		−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, CNTR		−0.3∼13	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, COM_0∼COM_3, SEG_0∼SEG_{31}, X_{OUT}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage CNTR		−0.3∼7	V
Pd	Power dissipation	T_a = 25℃	300	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Strage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=2.7∼5.5V, V_{SS}=0V, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage (Note 1)	f(X_{IN})=4.3MHz	4.5		5.5	V
		f(X_{IN})=1.1MHz	2.7		5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ (Note 2), $P3_3$∼$P3_7$ (Note3), $P4_0$∼$P4_7$, $\overline{RESET}$, X_{IN}, CNV_{SS}		0.7V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$ (Note 4), $\overline{INT_1}$, CNTR		0.74V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ (Note 2), $P3_3$∼$P3_7$ (Note 3), $P4_0$∼$P4_7$, CNV_{SS}		0		0.3V_{CC}	V
V_{IL}	"L" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$ (Note 4), $\overline{INT_1}$, CNTR		0		0.26V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16V_{CC}	V
I_{OH}	"H" output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$ (Note 5), X_{OUT}				−2	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, X_{OUT}(Note 6)				10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, X_{OUT}(Note 7)				5	mA
f(X_{IN})	Clock oscillating frequency (Note 8)	V_{CC}=4.5∼5.5V	64		4300	kHz
		V_{CC}=2.7∼5.5V	64		1100	
f(X_{CIN})	Clock oscillating frequency for clock function (Note 8)		32		50	kHz

Note 1 : When only maintaining the RAM data, minimum value of V_{CC} is 2V.
2 : When using port $P3_1$ as X_{CIN}, 0.85V_{CC}≦V_{IH}≦V_{CC}, 0≦V_{IL}≦0.15V_{CC} for port $P3_1$.
3 : In this case of using port $P3_6$ as normal input.
4 : In this case of using port $P3_6$ as CLK input.
Especially when the input oscillation frequency is more than 50kHz, recommend the following :
0.8V_{CC}≦V_{IH}≦V_{CC}, 0≦V_{IL}≦0.2V_{CC}
5 : The total of I_{OH} of port P0, P1, P2, P3 and X_{OUT} should be 35mA max.
6 : The total of I_{OL} (peak) of port P0, P1, P2, P3 should be 55mA max, and the total of I_{OL} (peak) of port P3, CNTR, and X_{OUT} should be 45mA max.
7 : I_{OL} (avg) is the average current in 100ms.
8 : When changing the contents of the most significant bit at address $00F5_{16}$, f(X_{IN}) needs the following range : f(X_{IN})>3f(X_{CIN}).

ELECTRICAL CHARACTERICS (V_{SS}= 0 V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$(Note 9)(Note10)		V_{CC}=5V, I_{OH}=−2mA		3			V
			V_{CC}=3V, I_{OH}=−0.7mA		2			
V_{OH}	"H" output voltage X_{OUT}		V_{CC}=5V, I_{OH}=−1.5mA		3			V
			V_{CC}=3V, I_{OH}=−0.3mA		2			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$(Note10), CNTR		V_{CC}=5V, I_{OL}=10mA				2	V
			V_{CC}=3V, I_{OL}=3mA				1	
V_{OL}	"L" output voltage X_{OUT}		V_{CC}=5V, I_{OL}=1.5mA				2	V
			V_{CC}=3V, I_{OL}=0.3mA				1	
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$, CNTR		V_{CC}=5V		0.25		1	V
			V_{CC}=3V		0.15		0.7	
$V_{T+}-V_{T-}$	Hysteresis $P3_6$		When used as CLK input	V_{CC}=5V		0.5		V
				V_{CC}=3V		0.4		
$V_{T+}-V_{T-}$	Hysteresis $P3_1$		When used as X_{CIN} input	V_{CC}=5V		0.7		V
				V_{CC}=3V		0.5		
$V_{T+}-V_{T-}$	Hysteresis $P2_0$~$P2_7$, $P3_2$		V_{CC}=5V			0.5		V
			V_{CC}=3V			0.4		
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$		V_{CC}=5V			0.5	0.7	V
			V_{CC}=3V			0.35		
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		V_{CC}=5V			0.5		V
			V_{CC}=3V			0.35		
I_{IL}	"L" input current $P4_0$~$P4_7$ (except reset state), {$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR (Note 12)} without pull-up Tr. CNTR (Note 11), $\overline{INT_1}$, $\overline{RESET}$, X_{IN}		V_{CC}=5V, V_I=0V				−5	μA
			V_{CC}=3V, V_I=0V				−4	
I_{IL}	"L" input current {$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR (Note 12)} with pull-up Tr.		V_{CC}=5V, V_I=0V		−30	−70	−140	μA
			V_{CC}=3V, V_I=0V		−6	−25	−45	
I_{IL}	"L" input current $P4_0$~$P4_7$ (at reset state)		V_{CC}=5V, V_{L3}=5V, V_I=0V		−30		−140	μA
			V_{CC}=3V, V_{L3}=3V, V_I=0V		−6		−45	
I_{IH}	"H" input current $P4_0$~$P4_7$ (except reset state), $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}		V_{CC}=5V, V_I=5V				5	μA
			V_{CC}=3V, V_I=3V				4	
I_{IH}	"H" input current $P4_0$~$P4_7$ (at reset state)		V_{CC}=5V, V_{L3}=5V, V_I=5V				5	μA
			V_{CC}=3V, V_{L3}=3V, V_I=3V				4	
R_{COM}	Output impedance COM_0~COM_3		V_{L1}=V_{CC}/3, V_{L2}=2V_{L1}, V_{L3}=V_{CC}, Other COM, SEG pins are opend.	V_{CC}=5V	30	200	2000	Ω
				V_{CC}=3V	70	500	4000	
R_S	Output impedance SEG_0~SEG_{31}			V_{CC}=5V		2		kΩ
				V_{CC}=3V		3		
I_{CC}	Supply current (at operation)	Output pin are opened. $\overline{RESET}$, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, and $P3_0$~$P3_7$ are connected to V_{CC}. Except the above pins are connected to V_{SS}. However, X_{IN} and X_{CIN} are input signal according to the conditions.	f(X_{IN})=4MHz, V_{CC}=5V			3	6	mA
			f(X_{IN})=1MHz, V_{CC}=3V			0.4		
			T_a=25℃, X_{IN}=0V, f(X_{CIN})=32.8kHz at low power mode (LM_6=1)	V_{CC}=5V		45		μA
				V_{CC}=3V		18		
I_{CC}	Supply current (at wait state)		f(X_{IN})=4MHz, V_{CC}=5V			1		mA
			f(X_{IN})=1MHz, V_{CC}=3V			0.2		
			T_a=25℃, X_{IN}=0V, f(X_{CIN})=32.8kHz at low power mode (LM_6=1)	V_{CC}=5V		20	60	μA
				V_{CC}=3V		4	12	
I_{CC}	Supply current		f(X_{IN})=0, f(X_{CIN})=0, V_{CC}=5V	T_a=25℃		0.1	1	μA
				T_a=70℃			10	
V_{RAM}	RAM retention voltage		f(X_{IN})=0, f(X_{CIN})=0		2		5.5	V

Note 9 : Except when the output type of $P3_5$ is N-channel open drain (mask option).
10 : If $P3_0$ is used as X_{COUT}, capability of load driving is lower than the above.
11 : For M50930-XXXFP and M50931-XXXFP
12 : For M50932-XXXFP

TIMING REQUIREMENTS
Memory expanding mode and microprocessor mode (V_{CC}=5V±10%, V_{SS}=0 V, T_a=25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		270			ns
t_{WI}	$\overline{INT_1}$, $\overline{INT_2}$ external clock input pulse width		1			μs
		V_{CC}=2.7V	4			
t_{WR}	$\overline{RESET}$ external clock input pulse width (Note 13)		2			μs
		V_{CC}=2.7V	8			
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		20			ns
t_C	External clock input cycle time (X_{IN} pin)		250			ns
t_W	External clock input pulse width (X_{IN} pin)		75			ns
t_r	External clock rising edge time (X_{IN} pin)				25	ns
t_f	External clock falling edge time (X_{IN} pin)				25	ns
t_{CC}	External clock input cycle time ($P3_1/X_{CIN}$ pin, X_{CIN})		20			μs
t_{WC}	External clock input pulse width ($P3_1/X_{CIN}$ pin, X_{CIN})		5			μs
t_{rc}	External clock rising edge time ($P3_1/X_{CIN}$ pin, X_{CIN})				6.2	μs
t_{fc}	External clock falling edge time ($P3_1/X_{CIN}$ pin, X_{CIN})				6.2	μs

Note 13 : Hold $\overline{RESET}$ to "L" level while eight or more rise pulses are input from X_{IN}.

SWITCHING CHARACTERISTICS
Memory expanding mode and microprocessor mode (V_{CC}=5V±10%, V_{SS}=0 V, T_a=25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 30			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				330	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				tcyc/4 +200	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				250	ns

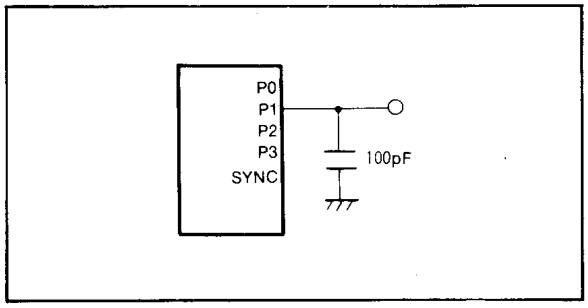
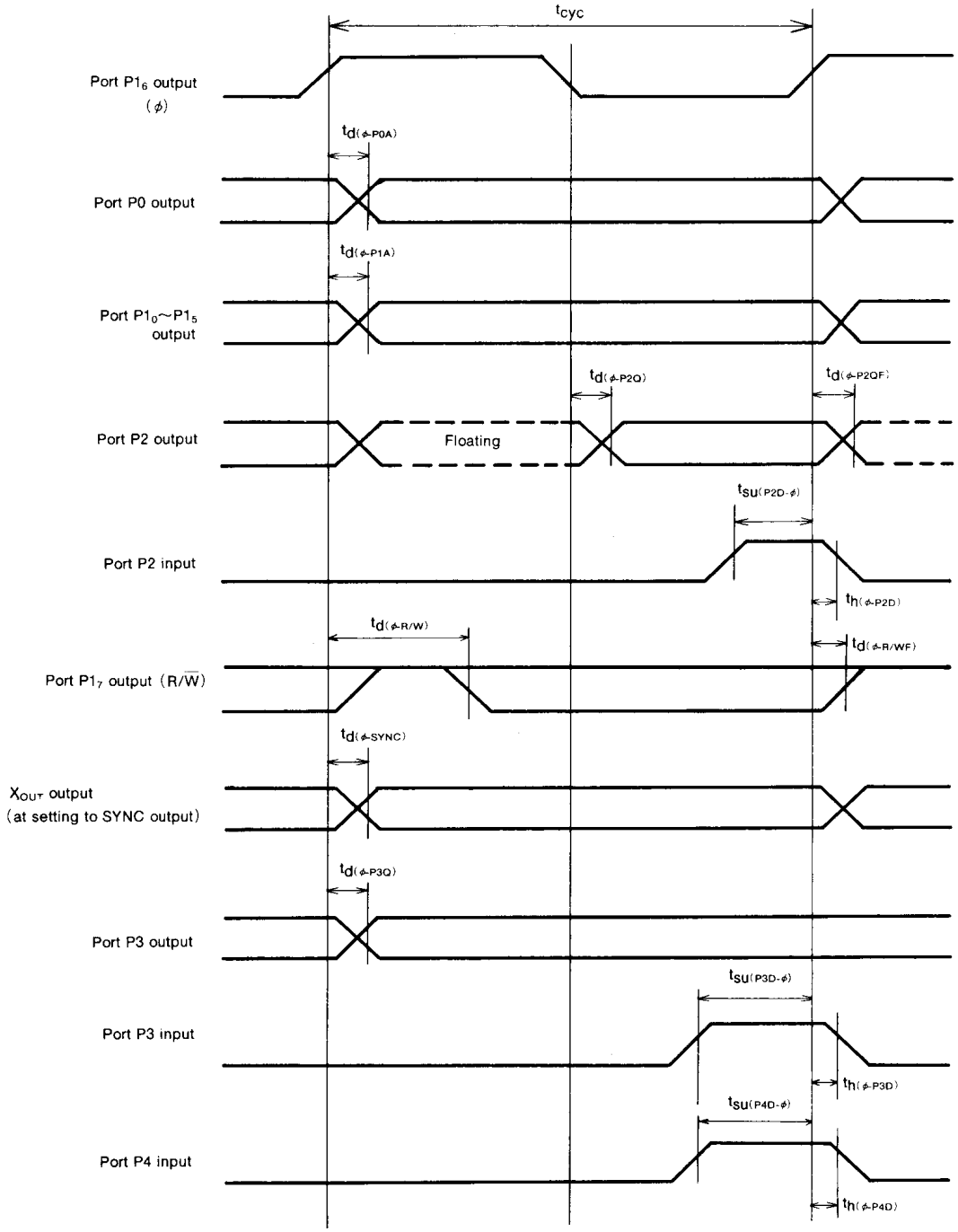
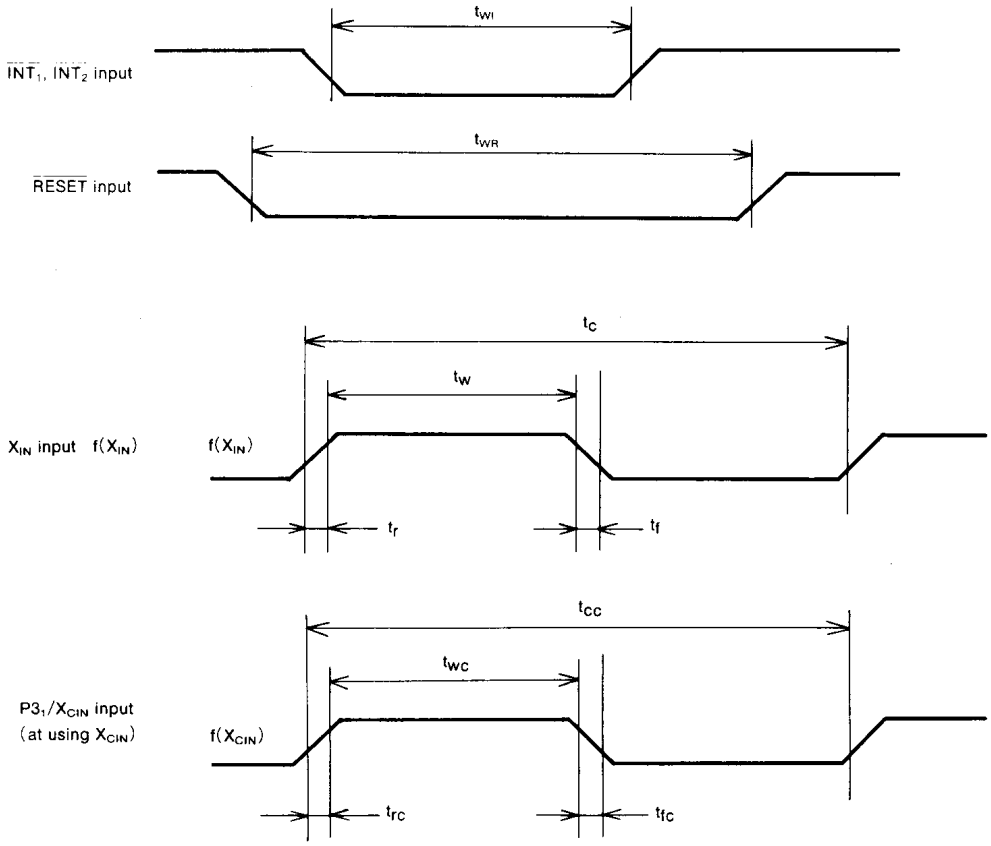


Fig.30 Port P0, P1, P2, P3, SYNC (X_{OUT}) test circuit

TIMING DIAGRAMS

In memory expanding mode and microprocessor mode




t_{WI}
$\overline{INT_1}$, $\overline{INT_2}$ input
t_{WR}
$\overline{RESET}$ input
t_C
t_W
X_{IN} input $f(X_{IN})$
$f(X_{IN})$
t_r
t_f
t_{CC}
t_{WC}
$P3_1/X_{CIN}$ input
(at using X_{CIN})
$f(X_{CIN})$
t_{rc}
t_{fc}