GROUP 16

Coverage Model Report (Project 3)

This report summarizes the instruction coverage achieved during simulation, highlighting the key areas tested.

1. ALU Instructions (ADD, AND, NOT):

- All valid combinations for immediate and register-based ADD, AND, and NOT instructions are covered.

2. Memory Instructions (LD, LDI, LEA, LDR, ST, STI, STR):

- **Load Operations:** Includes coverage of all valid destination registers and address offsets for LD, LDI, and LEA.
- **Store Operations:** Ensures all valid source registers and address offsets for ST, STI, and STR are exercised.

3. Control Instructions (BR, JMP):

- **Branch Instructions:** All valid offsets and NZP combinations for BR are covered.
- **Jump Instructions:** Coverage for all base registers used in JMP instructions.

Summary:

The coverage model fully exercises all major instruction types, including arithmetic, memory, and control flow instructions. This results in 99.13% coverage and meets all the specified testplan goals.
Number of Tests: 12 **Total Simulation Time** : ~8 mins (wall-clock time)

RESULTS:
1. TestPlan Tracker

Testplan Tracker

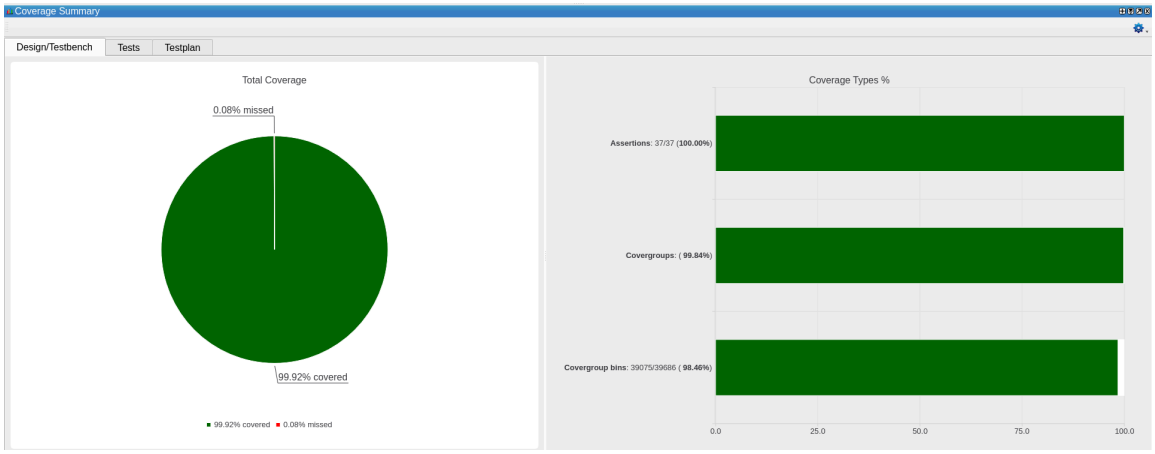
Sec#	Testplan Section/Coverage Link	Type	Status	Coverage%	Goal	% of Goal	Weight	Link Status	Bins	Hits	% Hit
0	testplan	Testplan		99.13%	-	99.13%	1	Clean	37448	36837	98.36%
1	LC3 Instruction Coverages	Testplan		99.13%	100%	99.13%	1	Clean	37448	36837	98.36%
...00001	Add, And immediate ops	Testplan		99.82%	100%	99.82%	1	Clean	4096	4089	99.82%
1.2	Add, And register ops	Testplan		100.00%	100%	100.00%	1	Clean	1024	1024	100.00%
1.3	Not ops	Testplan		100.00%	100%	100.00%	1	Clean	64	64	100.00%
1.4	Ld, Ldi, Lea ops	Testplan		97.81%	100%	97.81%	1	Clean	12288	12020	97.81%
1.5	Ldr ops	Testplan		99.14%	100%	99.14%	1	Clean	4096	4061	99.14%
1.6	St, Sti ops	Testplan		97.14%	100%	97.14%	1	Clean	8192	7958	97.14%
1.7	Str ops	Testplan		98.99%	100%	98.99%	1	Clean	4096	4055	98.99%
1.8	Br ops	Testplan		99.27%	100%	99.27%	1	Clean	3584	3558	99.27%
1.9	Jmp ops	Testplan		100.00%	100%	100.00%	1	Clean	8	8	100.00%

2. Cross Covergroups

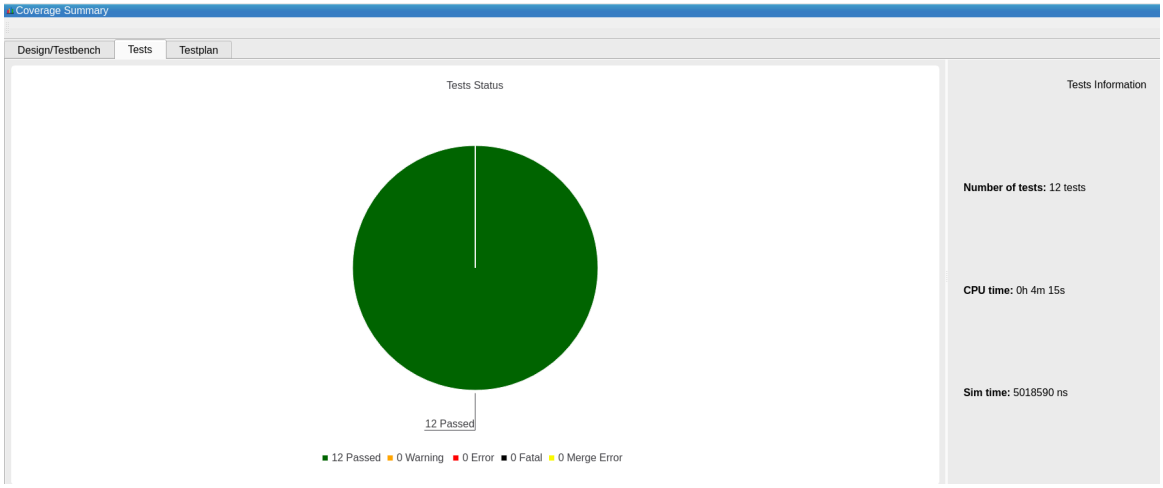
Path	Missing Bins	Total Bins	% Hit	Coverage	Status	Goal
Total Covergroups	611	39686	98.46%	99.84%		
/imem_pkg/imem_transaction_coverage/imem_transaction_cg	0	437	100.00%	100.00%		100%
/imem_pkg/imem_transaction_coverage/add_and_ops_cg	7	5181	99.86%	99.98%		100%
/imem_pkg/imem_transaction_coverage/not_cg	0	82	100.00%	100.00%		100%
/imem_pkg/imem_transaction_coverage/loads_cg	303	16980	98.21%	99.62%		100%
/imem_pkg/imem_transaction_coverage/stores_cg	275	12883	97.86%	99.51%		100%
/imem_pkg/imem_transaction_coverage/control_cg	26	4123	99.36%	99.91%		100%

3. Coverage Summary

3.1 Design/Testbench



3.2 Tests



3.3 Testplan