

دانشگاه صنعتی شاهرود دانشکده مهندسی برق

عنوان:

ساعت ديجيتال

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آزمایشگاه FPGA

1. با استفاده از کد VHDL یک ساعت دیجیتال با تکنیک مالتی پلکس زمانی پیاده سازی کنید.

در این گزارش کد آزمایش قبل که صرفا ثانیه و دقیقه را نشان میداد تکمیل کرده و یک ساعت دیجیتال ۲۴ ساعته با تکنیک مالتی پلکس زمانی نوشته ایم.

● کد نوشته شده به صورت زیر است:

Listing 1: Example VHDL code

```
library IEEE;
  use IEEE.STD_LOGIC_1164.ALL;
  use IEEE.STD_LOGIC_ARITH.ALL;
  use IEEE.STD_LOGIC_UNSIGNED.ALL;
  entity main is
  Port (
          b
               : in std logic;
           clk : in std_logic;
               : out std_logic_vector(5 downto 0);
           dpp : out std_logic;
               : out std_logic_vector(0 to 6);
           rest: in std_logic );
  end main;
  architecture Behavioral of pr is
      signal counter1 : std_logic_vector(3 downto 0) := "0000";
      signal counter2 : std_logic_vector(3 downto 0) := "0000";
18
      signal counter3 : std_logic_vector(3 downto 0) := "0000";
19
      signal counter4 : std_logic_vector(3 downto 0) := "0000";
20
      signal counter5 : std_logic_vector(3 downto 0) := "0000";
      signal counter6 : std_logic_vector(3 downto 0) := "0000";
      signal clk_1s : std_logic := '0';
      function Bcd_7seg( s : std_logic_vector(3 downto 0)) return
24
          std_logic_vector is
      variable y : std_logic_vector(6 downto 0);
  begin
26
      case (s) is
           when "0000" =>
28
               y := "11111110";
29
           when "0001" =>
30
               y := "0110000";
           when "0010" =>
               y := "1101101";
33
           when "0011" =>
34
               y := "1111001";
           when "0100" =>
36
               y := "0110011";
           when "0101" =>
38
               y := "1011011";
39
           when "0110" =>
40
               y := "1011111";
```

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```
when "0111" =>
42
                y := "1110000";
43
            when "1000" =>
44
                y:= "1111111";
45
            when "1001" =>
                y := "1111011";
            when others =>
                y := "0000000";
49
       end case;
50
       return y;
   end Bcd_7seg;
53
54
   begin
       dpp \le b;
55
       process (clk)
56
       variable counter0 : integer range 0 to 1000:= 0;
       begin
58
            if (clk'event and clk = '1') then
                counter0 := counter0 + 1;
60
                if (counter0 < 500) then
61
                     clk 1s <= '0';
                elsif (counter0 >= 500) then
63
                     clk_1s <= '1';
64
                end if;
            end if;
66
       end process;
68
       process (rest, clk_1s)
       begin
70
            if(rest = '0') then
                counter1 <= "0000";
                counter2 <= "0000";
                counter3 <= "0000";
                counter4 <= "0000";
                counter5 <= "0000";
                counter6 <= "0000";</pre>
            else
78
                if (clk_1s'event and clk_1s='1')then
79
                     counter1 <= counter1+1;</pre>
80
                     if (counter1 = "1001") then
                          counter1 <= "0000";
82
                          counter2 <= counter2+1;</pre>
83
                          if (counter2 = "0101") then
84
                              counter2 <= "0000";
85
                              counter3 <= counter3+1;</pre>
86
                              if (counter3 = "1001") then
87
                                   counter3 <= "0000";
88
                                   counter4 <= counter4+1;</pre>
89
                                   if (counter4 = "0101") then
90
                                       counter4 <= "0000";
91
```

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```
counter5 <= counter5+1;</pre>
92
                                          if (counter5 = "1001") then
93
                                               counter5 <= "0000";
94
                                               counter6 <= counter6+1;</pre>
95
                                               if (counter6 = "0010") then
96
                                                   counter6 <= "0000";
97
                                                   counter5 <= "0000";
98
                                                   counter4 <= "0000";
99
                                                   counter3 <= "0000";
100
                                                   counter2 <= "0000";
                                                   counter1 <= "0000";
                                               end if;
103
                                          end if;
104
                                     end if;
105
                                end if;
106
                           end if;
                      end if;
108
                  end if;
109
             end if;
110
        end process;
112
        process(clk)
        variable C: integer range 0 to 5 := 0;
        begin
             if (clk'event and clk='1') then
116
                 C := C + 1;
                 if (C=1) then
                      Q <= "000001";
119
                      Z <= Bcd_7seg(counter1);</pre>
120
                  elsif (C = 2) then
                      Q <= "000010";
                      Z <= Bcd_7seg(counter2);</pre>
                  elsif(c = 3) then
                      Q <= "000100";
125
                      Z <= Bcd_7seg(counter3);</pre>
126
                  elsif(c = 4) then
127
                      Q <= "001000";
128
                      Z <= Bcd_7seg(counter4);</pre>
                  elsif(c = 5) then
130
                      Q \le "010000";
131
                      Z <= Bcd_7seg(counter5);</pre>
                  elsif(c = 6) then
133
                      Q <= "100000";
134
                      Z <= Bcd_7seg(counter6);</pre>
135
                  end if;
136
             end if;
        end process;
138
   end Behavioral;
139
```