1 Example VHDL code

Here's an example of how to include VHDL code in a LaTeXdocument using the `listings` package:

Listing 1: Example VHDL code

```
1
2  library ieee;
3  use ieee.std_logic_1164.all;
4
5  entity example is
6  port (
7  clk : in std_logic;
8  rst : in std_logic;
9  data_in : in std_logic_vector(7 downto 0);
10 data_out : out std_logic_vector(7 downto 0)
11 );
12 end entity;
13
14 architecture rtl of example is
15 begin
16 -- insert your VHDL code here
17 end architecture;
```