In The Name Of God

Department of Electrical Engineering

Electronics (I) Project Reports

Project Title:

“Single Stage Transistor Amplifier Design”

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Contents

Theory analysis

1.1 About of Project:

We want design the single stage transistor amplifier with this parameters:

$$\begin{cases} A_V \geq 100 \\ R_{in} = 50\ \Omega \\ V_{cc} = 5\ V \end{cases}$$

Only use these values in this design: $$\begin{cases} \beta = 100 \\ |V_{BE}| = 0.7 \\ |V_{CE,sat}| = 0.2 \\ V_A = 100\ V \\ Capasitor\ value = 100\ \mu F \\ input\ signal\ frequency = 10\ KHz \end{cases}$$

1.2 Common Emitter Amplifier:

The **Common Emitter Amplifier** is a type of bipolar junction transistor, (BJT) configuration where the emitter terminal of the transistor is a common terminal to both the input and output signals, hence its name *common emitter* (CE).

For the common emitter configuration to operate as an amplifier, the input signal is applied to the base terminal and the output is taken from the collector terminal.

The basic common emitter amplifier configuration is shown below.

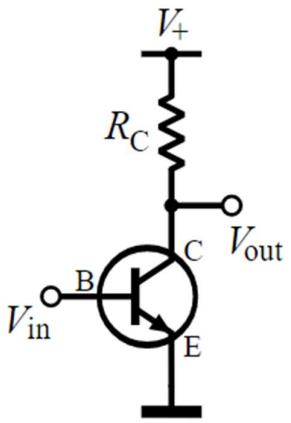


FIGURE 1.1 : Basic NPN common-emitter circuit

Completed Common Emitter Circuit

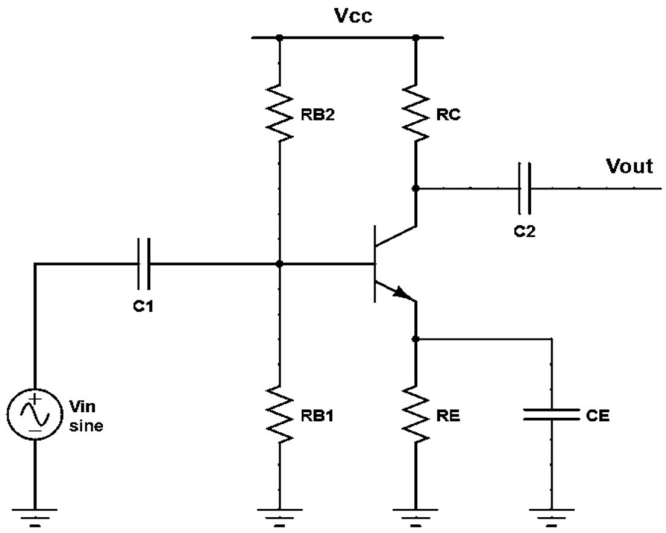


FIGURE 1.2 : Completed common emitter circuit

Amplifier Coupling Capacitors:

In **Common Emitter Amplifier** circuits, capacitors C1 and C2 are used as **Coupling Capacitors** to separate the AC signals from the DC biasing voltage. This ensures that the bias condition set up for the circuit to operate correctly is not affected by any additional amplifier stages, as the capacitors will only pass AC signals and block any DC component.

The output AC signal is then superimposed on the biasing of the following stages. Also a bypass capacitor, C_E is included in the Emitter leg circuit.

This capacitor is effectively an open circuit component for DC biasing conditions, which means that the biasing currents and voltages are not affected by the addition of the capacitor maintaining a good Q-point stability.

However, this parallel connected bypass capacitor effectively becomes a short circuit to the Emitter resistor at high frequency signals due to its reactance. Thus only R_L plus a very small internal resistance acts as the transistors load increasing voltage gain to its maximum. Generally, the value of the bypass capacitor, C_E is chosen to provide a reactance of at most, 1/10th the value of R_E at the lowest operating signal frequency.

Common Emitter Voltage Gain:

The **Voltage Gain** of the common emitter amplifier is equal to the ratio of the change in the input voltage to the change in the amplifiers output voltage.

$$A_V = \frac{V_{out}}{V_{in}} = -g_m(R_c \,||\, R_o)$$

Output resistance:

The resistance seen from output node, is R_{out} and is equal to:

$$R_{Out} = r_O || \, R_C$$

Input resistance:

The resistance seen from input node, is R_{in} and is equal to:

$$R_{in} = R_{B1} || \, R_{B2} || \, r_\pi$$

1.3 Configuration and Amplifier Value Calculation:

In the first step we select the type of amplifier, That we chose a common emitter. Because it has a small input resistance and the high voltage gain.

Assume a current for the collector and then determine g_m, r_π, r_o.

Assume $I_C = 0.5\ mA$

$\rightarrow\ g_m \cong 40 I_C = 20\ \frac{mA}{V}$

$\rightarrow\ r_\pi = \frac{\beta}{g_m} = \frac{100}{20} = 5\ K\Omega$

$\rightarrow\ r_o = \frac{V_A}{I_C} = \frac{100}{0.5} = 200\ K\Omega$

$\rightarrow\ R_{in} = R_{B1} || R_{B2} || r_\pi = 50\ \Omega \xrightarrow{r_\pi \gg 50\ \Omega} R_{in} = R_{B1} || R_{B2} = \boxed{50}$

$\rightarrow \begin{cases} R_{B1} = 100\ \Omega \\ R_{B2} = 100\ \Omega \end{cases}$

$R_{Out} = R_C || r_o \cong R_C$

$A_V = -g_m(R_C || r_o) > 100\ \rightarrow 20(R_C || 200K) > 100 \xrightarrow{r_o = high} 20 \times R_C > 100$

$\rightarrow\ \boxed{R_C > 5\ K\Omega}$

$V_E > 0.1 V_{cc}\ \rightarrow\ V_E > 0.5\ V\ \rightarrow\ \boxed{V_E = 1.85\ V}$

$\rightarrow\ R_E \gg 10 \frac{R_{TH}}{100}\ \rightarrow\ R_E \gg \frac{R_{TH}}{10} \gg \frac{100||100}{10} \gg 5\ \Omega$

$\xrightarrow{I_E = I_C = 0.5\ mA} R_E = \frac{V_E}{I_E} = \boxed{3.7\ K\Omega}$

$\begin{cases} R_{B1} = 100\ \Omega \\ R_{B2} = 100\ \Omega \end{cases} \rightarrow\ V_{TH} = 2.5\ V$

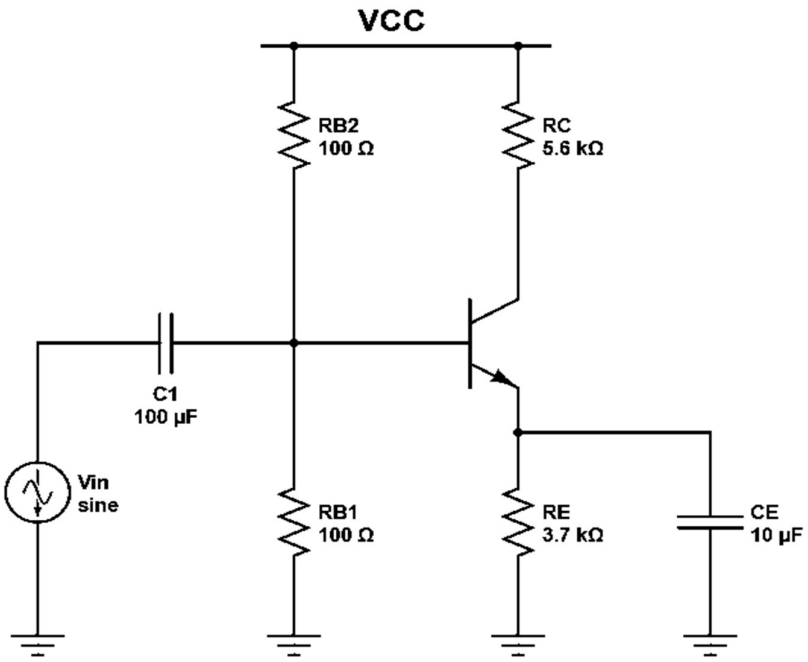
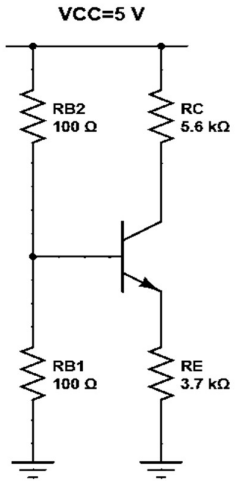


FIGURE 1.3 : Completed schematic layout

Last to first:

DC analysis: → *capacitor is open circuit*



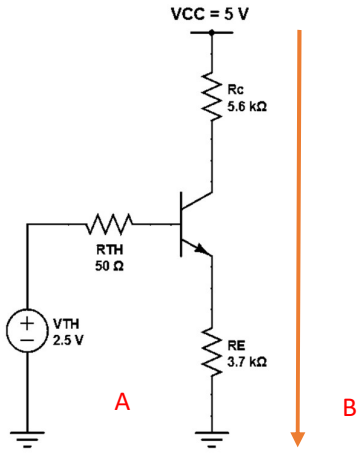


FIGURE 1.4 : Four resistor biasing

FIGURE 1.5 : Four resistor biasing

$$KVL\ @\ A:\ -V_{TH} + 50 \times I_B + V_{BE,on} + 3.7 \times I_E = 0 \xrightarrow{3.7K \gg \frac{50}{100}} I_B \cong 0$$

$$\rightarrow\ -2.5 + 0.7 + 3.7 \times I_E = 0 \quad \rightarrow \quad I_E = \frac{1.8}{3.7} = 0.49\ mA \cong 0.5\ mA \cong I_C$$

$$KVL\ @\ A:\ -5 + 5.6 \times 0.5 + V_{CE} + 3.7 \times 0.5 = 0\ \rightarrow\ V_{CE} = 0.35 > V_{CE,sat}$$

$$\rightarrow transistor\ in\ forward\ active\ region\ (F.A)$$

$$\begin{cases} g_m = 40 \times I_C = 20\ \dfrac{mA}{V} \\ r_\pi = \dfrac{\beta}{g_m} = \dfrac{100}{20} = 5\ K\Omega \\ r_o = \dfrac{V_A}{I_C} = \dfrac{100}{0.5} = 200\ K\Omega \end{cases}$$

$$\rightarrow C.E\ Amplifier \begin{cases} A_V = -g_m(R_C||r_\pi) = -20(5.6) = -112 \\ R_{in} = R_{B1}||\ R_{B2}\ ||r_\pi = 100\Omega\ ||100\Omega = 50\Omega \\ R_{out} = R_c||r_o \cong R_c = 5.6\ K\Omega \end{cases}$$

$$\boldsymbol{Swing_{Vout}}: min\left\{R_{AC}I_{CQ}\ , V_{CE,Q} - V_{CE,sat}\right\}$$

$$R_{AC} = R_E + R_C \quad in\ ac\ mode \xrightarrow{capacitor=shor\ \ circuit} 5.6\ K\Omega + 0 = 5.6\ K\Omega$$

$$\rightarrow \min\{5.6 \times 0.5\ ,0.35 - 0.2\} = \min\{2.8,0.15\}$$

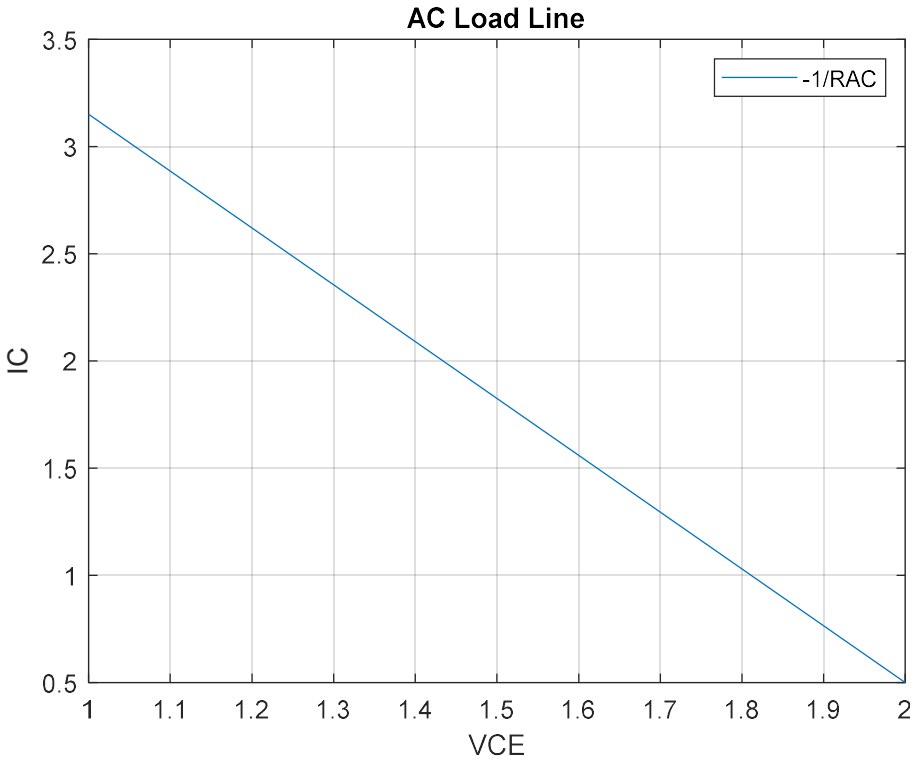


FIGURE 1.6 : AC load line characteristics

Swing limiting factors:

The VCC voltage is one of the limiting factors Because the amplified signal does not exceed its maximum. Emitter and collector resistances also limit swing from top and bottom. And the last factor is $V_{SE,sat}$, Because if the V_{CE} is less than that, the transistor will be saturated and Swing is not defined.

Simulations analysis

2.1 PSpice Simulations:

In the first step run the PSpice Application and created a new project and new simulation profile.

After created a new project, select components need from place part.

Selected BC107 transistor model with simulation. Then edit transistor parameters (Vaf, bf).

Right click on the transistor and select Edit PSpice model and change their value to 100.

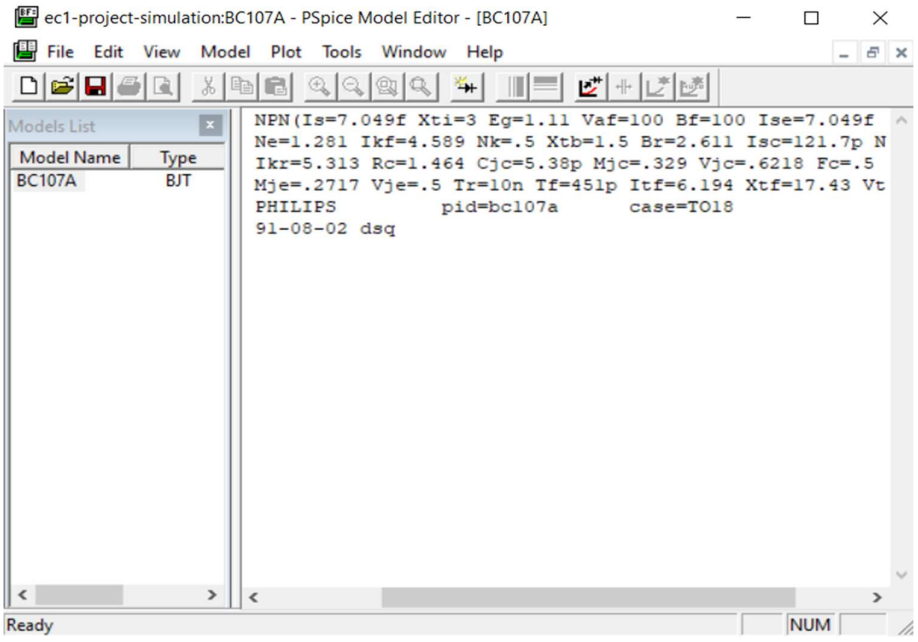


FIGURE 2.1 : Edit PSpice Model

Draw circuit schematics without bias Structure:

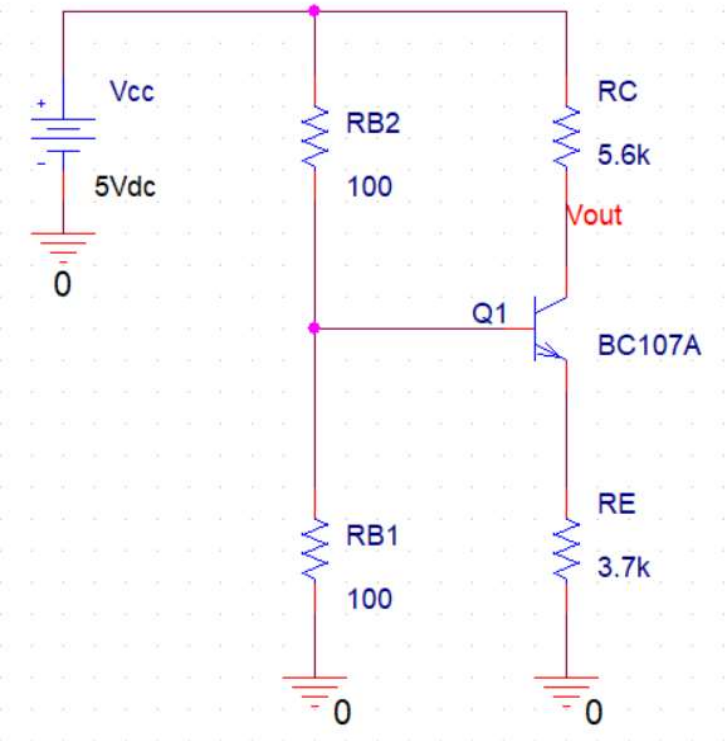


FIGURE 2.2 : circuit schematics without bias configuration

Then in the simulation settings, selected the bias point analysis to obtain operating point current and the collector emitter voltage (V_{CE}).

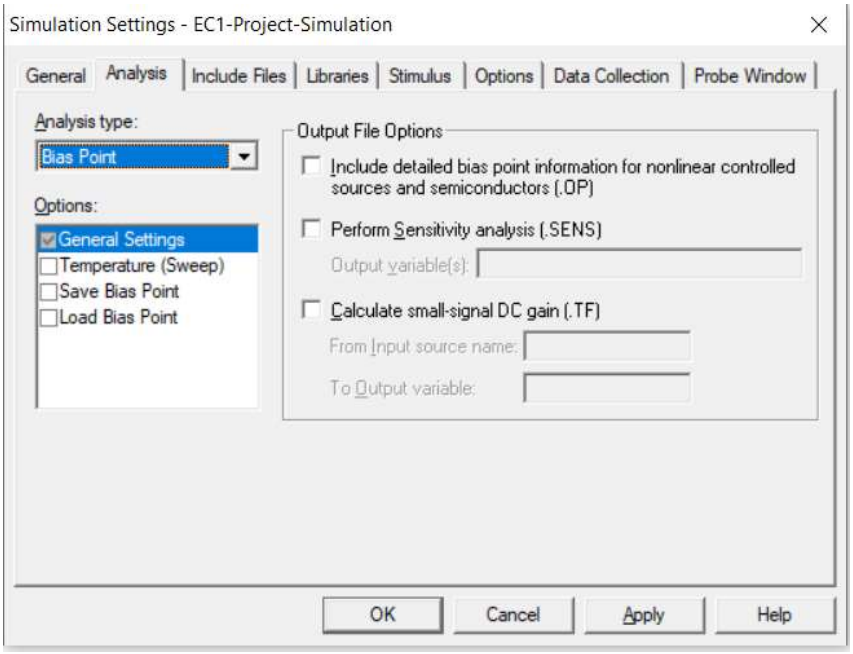


FIGURE 2.3 : Simulation settings

Run the simulation and find operating voltage and current:

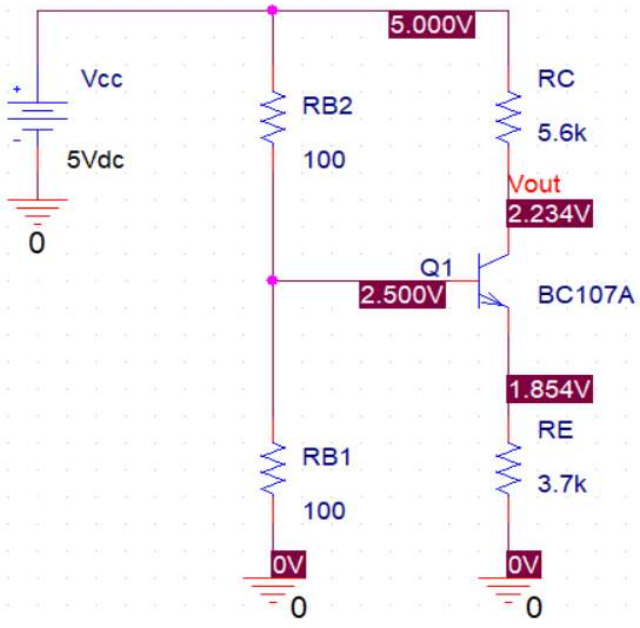


FIGURE 2.4 : branches voltage

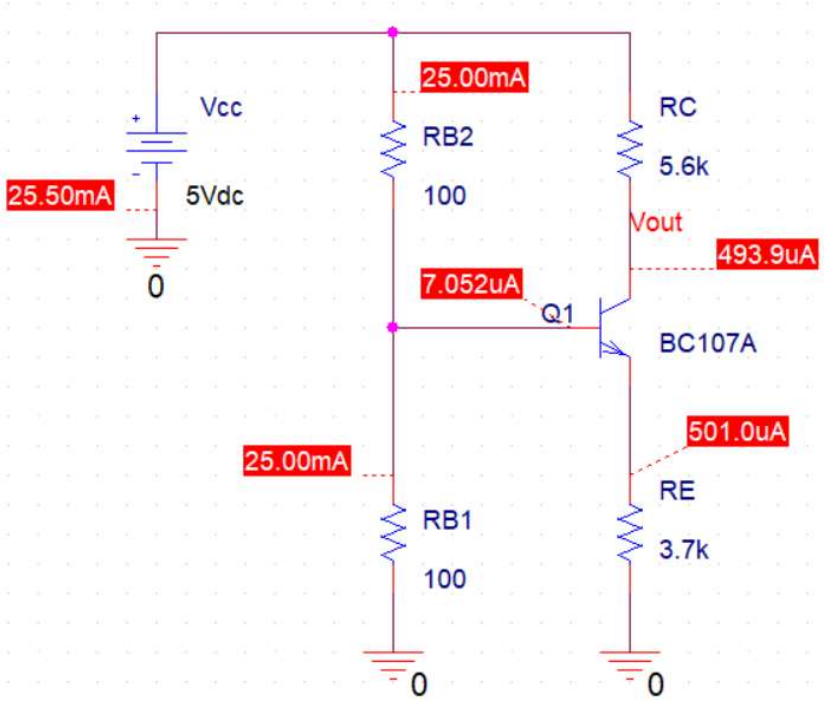


FIGURE 2.5 : nodes current

It can be seen that the current obtained from this section is approximately equal to the assumed current in the theoretical section.

$$\begin{cases} I_{CQ} \cong I_{EQ} \cong 500\ \mu A = 0.5\ mA \\ V_{CE} = 2.234 - 1.854 \cong 0.4 > V_{CE,sat} \end{cases}$$

Find input and output resistance:

To do this, we must draw a complete schematic of the circuit (with bias configuration). Thus, the completed schematic is shown below:

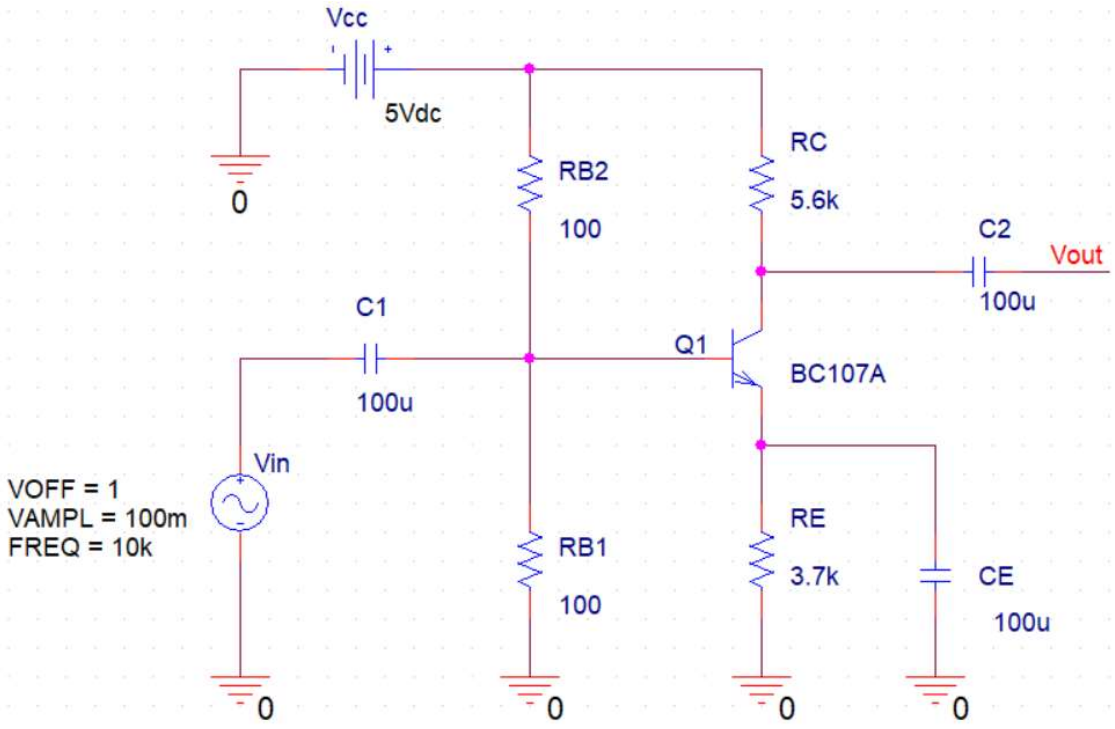


FIGURE 2.6 : completed schematic

For obtain input resistance, analyze the circuit in the small signal field (S.S).

I know that the capacitor, is short circuited in the S.S and the input impedance in this transistor structure (emitter is GND and look at the transistor from base) is equal to r_π. So above schematic is equal to the below circuit.

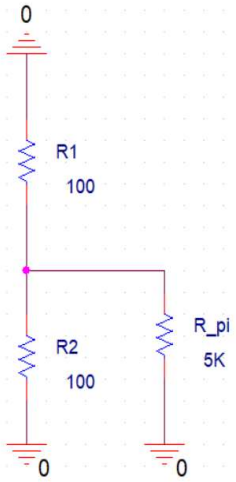


FIGURE 2.7 : input impedance

Then we apply a DC source with the desired value to the input and calculate $\frac{V_T}{I_T}$

- The 10 volt DC source is assumed here

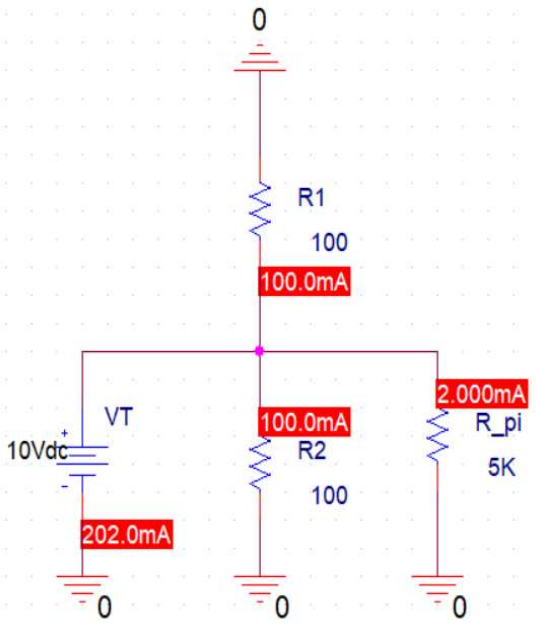


FIGURE 2.8 : input impedance

$$\frac{V_T}{I_T} = R_{in} = \frac{10\ V}{202\ mA} = 0.49\ K\Omega\ \cong 49\ \Omega$$

For obtain output resistance, we can delete $R_{B1}||R_{B2}$, because V_{in} is short circuit is S.S. in this transistor structure (base is GND and look at the transistor from collector) is equal to $R_C||R_O$. So above schematic is equal to the below circuit.

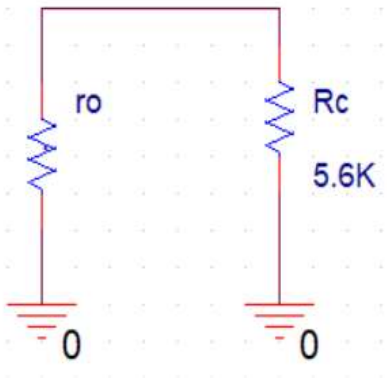


FIGURE 2.9 : output impedance

Output resistance is equal to: $R_{Out} = R_C = 5.6\ K\Omega$

Plot input and output characteristic and calculate voltage gain (A_V):

- Amplitude of input voltage is 100 mV.
- Amplitude of output voltage is 3 V.

$$A_V = \frac{V_{out}}{V_{in}} = 30$$

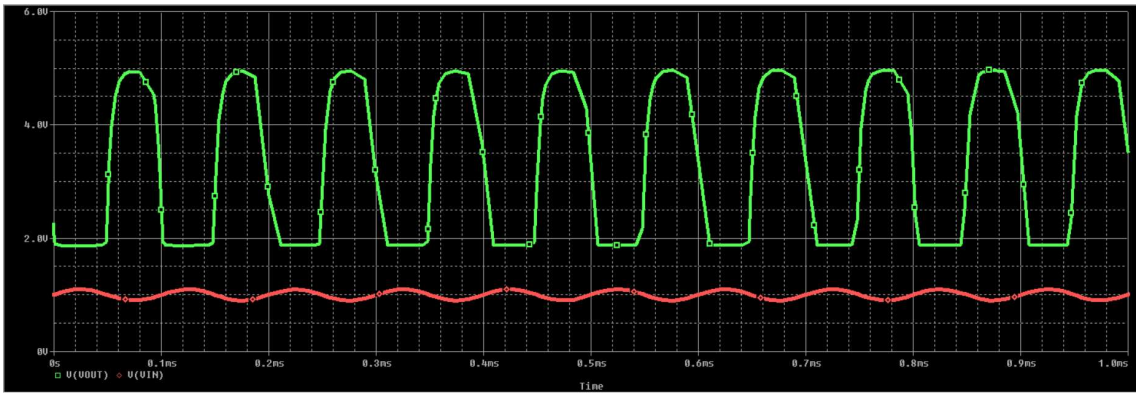


FIGURE 2.10 : input and output characteristic

Output swing:

To determine the output swing of the circuit with characteristics, we place a voltage source with an amplitude of 2.5 and plotting an output characteristic with characteristic of amplified signal.

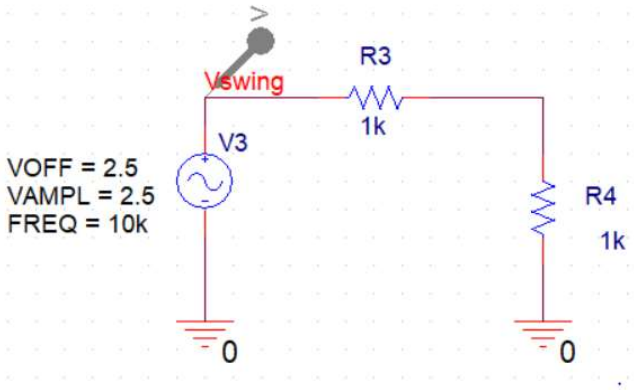


FIGURE 2.11 : circuit to get the swing

The output characteristic is as follows:

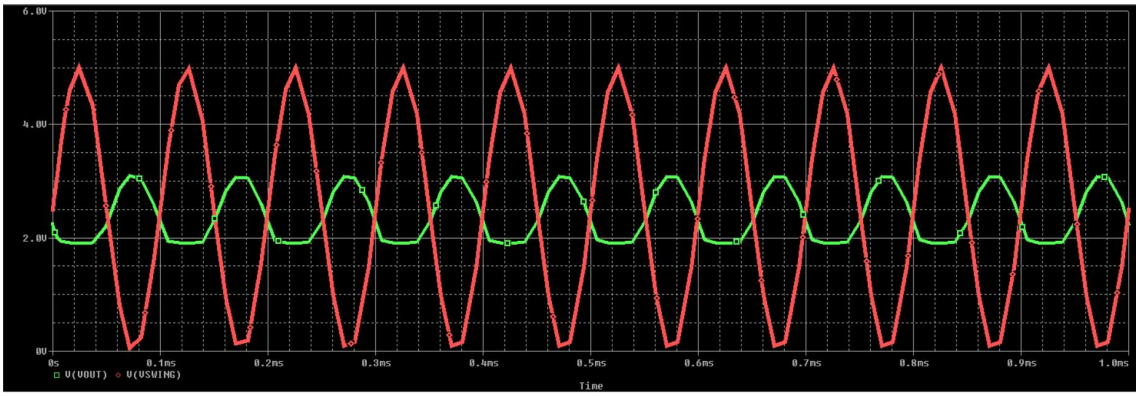


FIGURE 2.12 : output characteristic

One measure of distorion is the "**Total Harmonic Distortion**" (THD) of your output signal. Since you input a pure sine wave, you expect to get a pure sine wave back out, or, put another way, you expect there to be only one component in the spectrum of your signal, represented by one Fourier coefficient. If there are other coefficients, these are distorting your original signal.

THD is calculated as $D = 100\% \times \sqrt{\frac{\sum_{n=1}^{\infty} {F_n}^2}{{F_0}^2}}$, where F_0 is the fundamental frequency, F_1 is the first harmonic, and so on.

PSpice can output the Fourier coefficients. In your Simulation Profile, click on Output File Options and select Perform Fourier Analysis. Center Frequency is the fundamental frequency you are driving your circuit at; Number of Harmonics should be at least 5; and Output Variables should be of the form V(out), where out is your output node. After you run your simulation, the data will be included in the .out file corresponding to your simulation profile. But the easier way is to select Fourier scale from the simulation section.

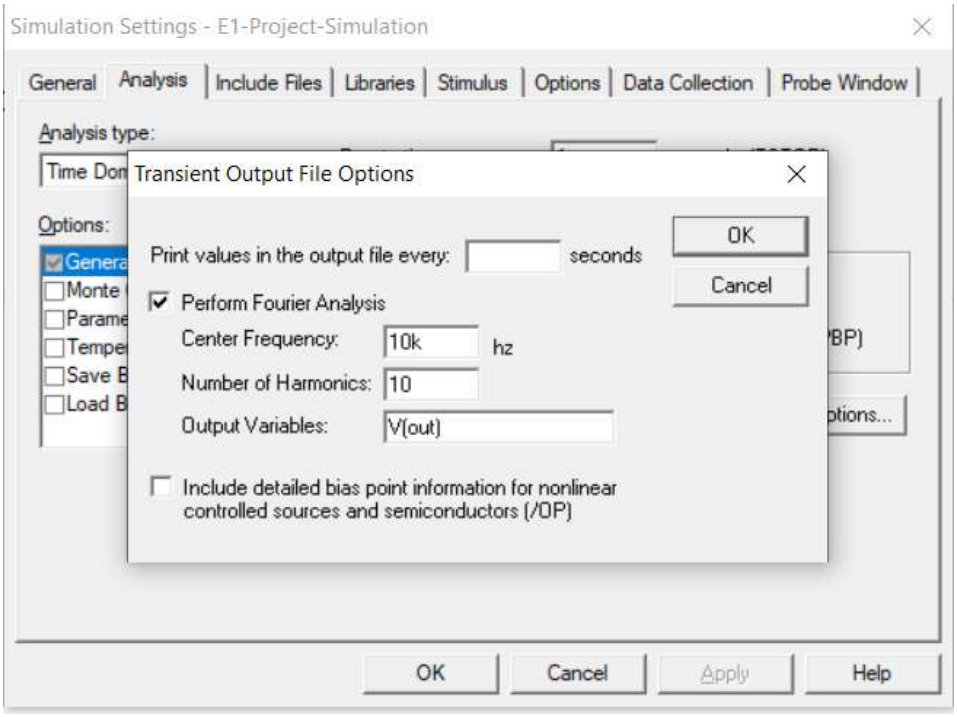


FIGURE 2.13 : Transient output file options

Using PSPICE, calculate the THD of your distorted signal for a 10 KHz, 10 mV amplitude of input wave?

Draw schematics and applied this value and plot the THD characteristic.

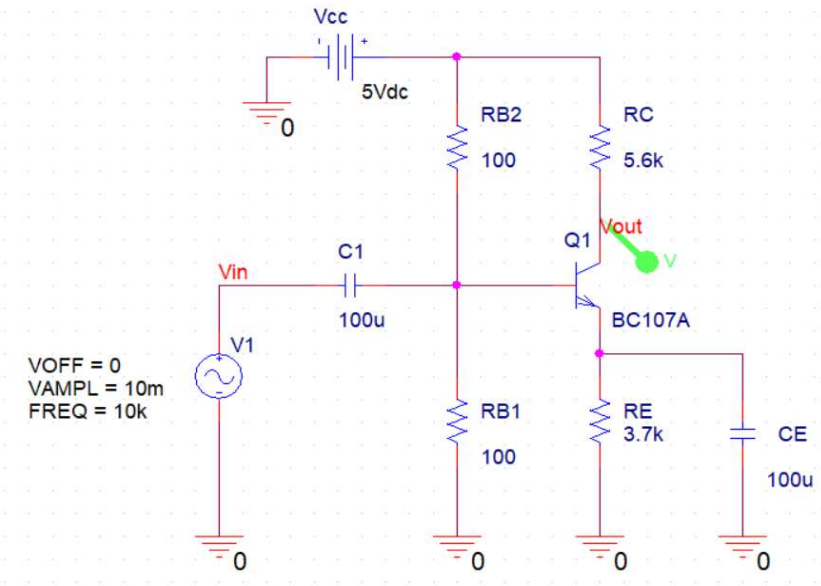


FIGURE 2.14 : circuit schematic

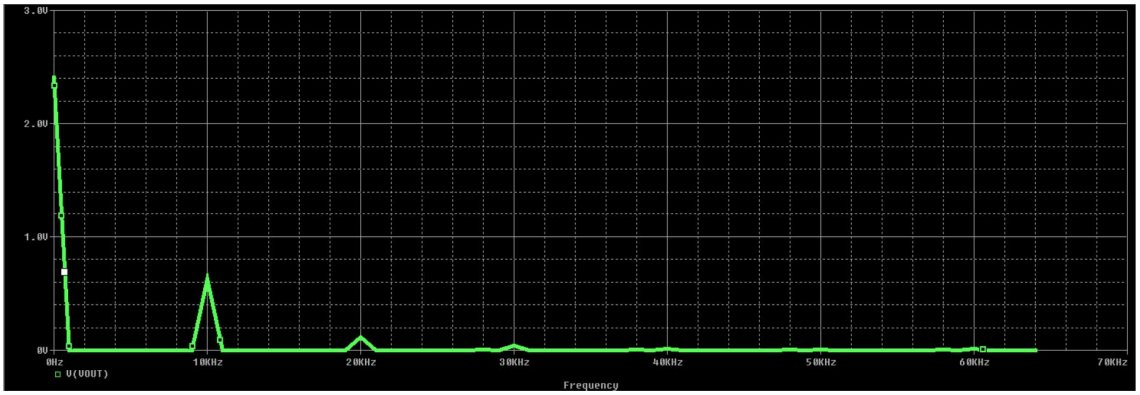


FIGURE 2.15 : THD characteristic

Change the amplitude to 300 mV and repeat the simulation.

The sinusoidal signal is converted to the square pulse almost.

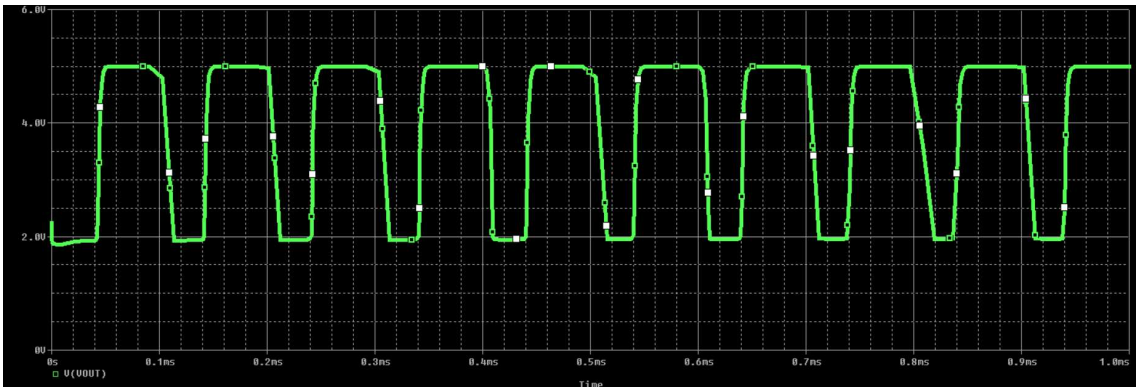


FIGURE 2.16 : output signal

And The THD characteristic is as follows:

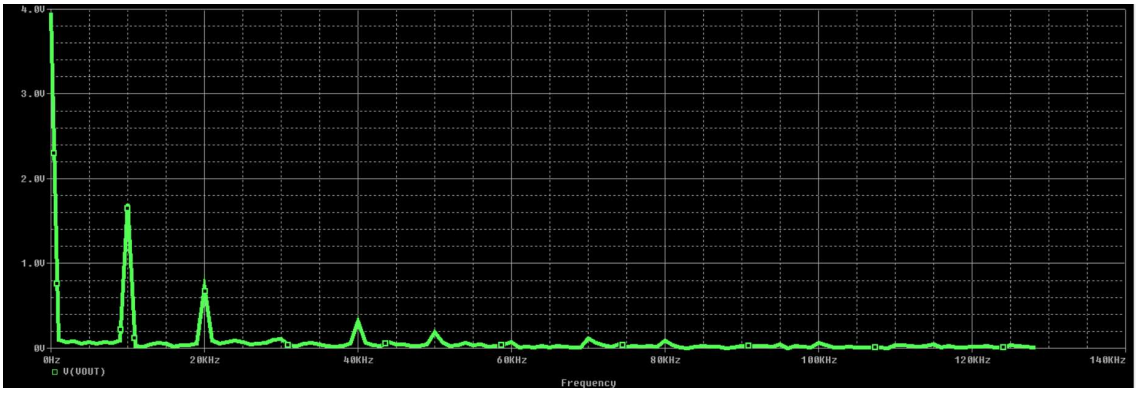


FIGURE 2.17 : output signal

The result is that: the THD increases with increasing amplitude from 10 to 300 mV.

2.2 PCB Design With Altium Designer:

With Altium Designer version 20, design schematic and PCB board

In the first step draw schematic layout:

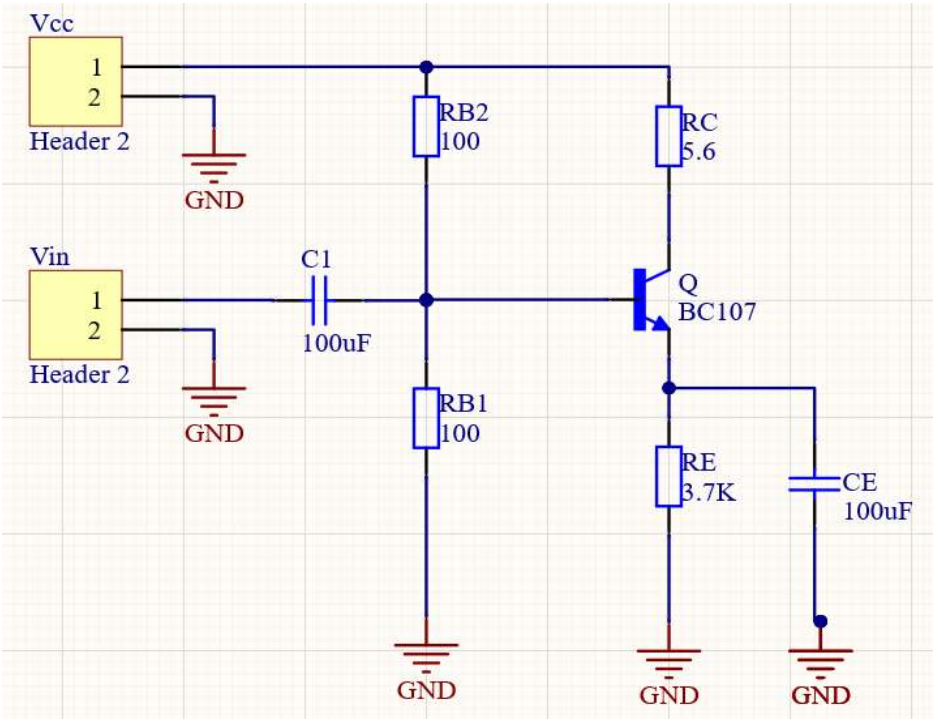


FIGURE 2.18 : schematic layout in Altiume

Then update schematic layout to PCB document and connect all tracks

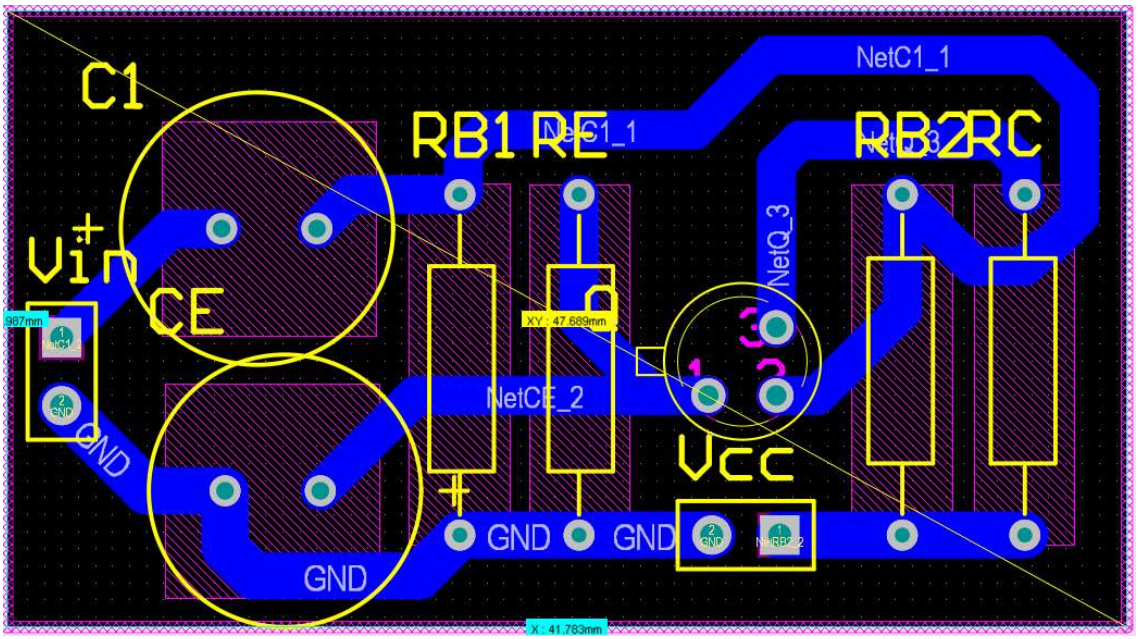


FIGURE 2.19 : 2D PCB layout

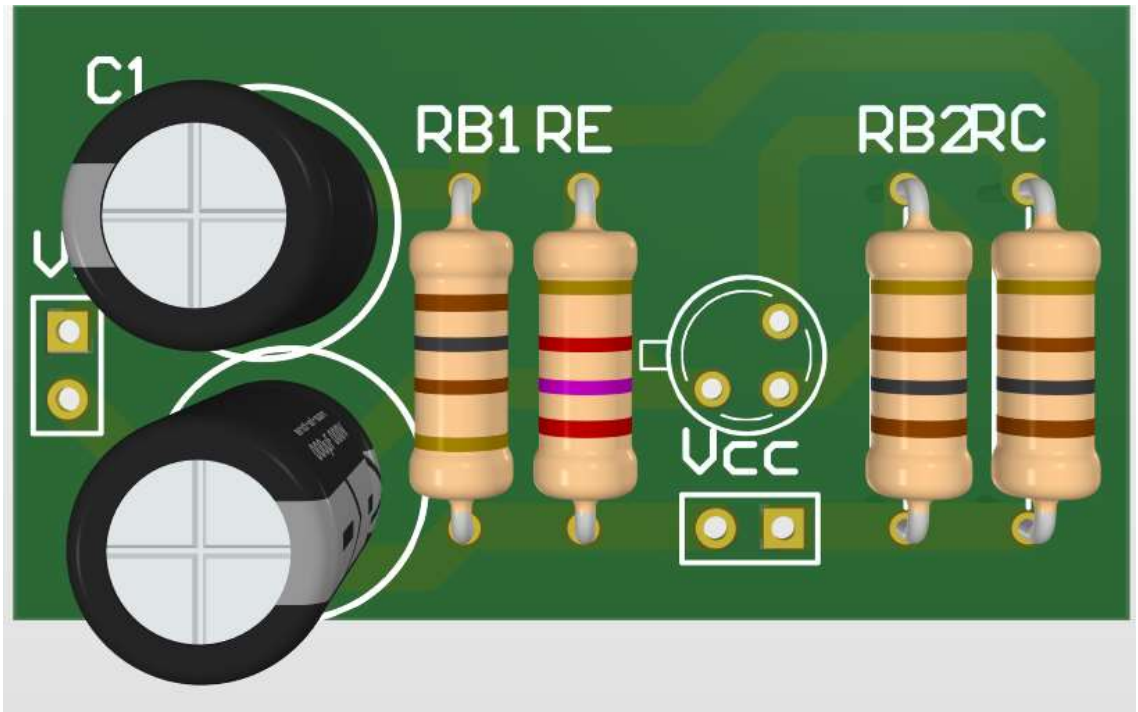


FIGURE 2.20 : 3D PCB layout (front)

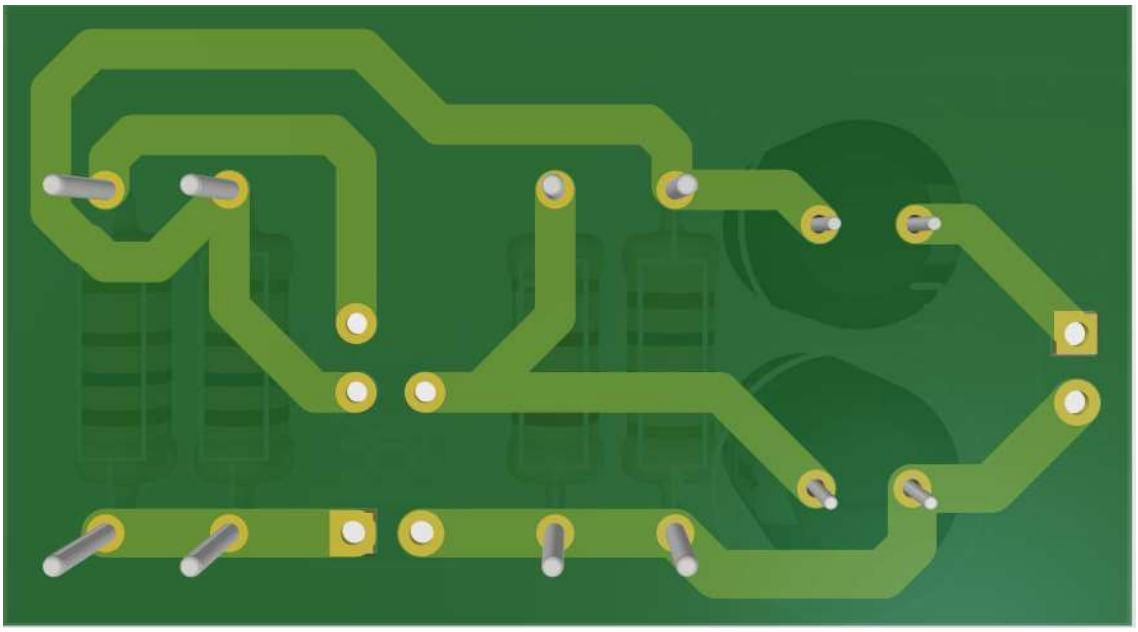


FIGURE 2.21 : 3D PCB layout (back)

Theory analysis, Simulations analysis Compare

3.1 Compare and Conclusions of them:

	THEORY ANALYSIS	SIMULATIONS ANALYSIS
$(I_{C,Q}, V_{CE,Q})$	(0.5 mA, 0.35 V)	(0.494 mA, 0.38 V)
$\|A_V\|$	112	30
R_{in}	50 Ω	49 Ω
R_{out}	5.6 KΩ	5.6 KΩ

Table 3.1 : Compare the values obtained

Source:

- Mohammad Reza Ashraf, *Class Booklet.*
- Behzad Razavi, *Fundamentals of Microelectronics.*
- www.en.wikipedia.org.
- www.electronics-tutorials.ws.
- www.mitmath.github.io.
- www.circuitlab.com.
- ORCAD PSPICE, *9.2 Version.*
- Matlab, *R200a Version.*
- Altium Designer, *2020 Version.*