In the name of god

Reza Adinepour
402131055
HW08

9.35 :
- $F = (A+B)(C+D)$
- max of 30λ
- output load : 500λ

I know, Domino Design
1) Precharge Phase
2) Evaluation Phase
3) static Inverter

1) Phase 1 : use a Precharge NMOS transistor to pull the output node high during the Precharge phase

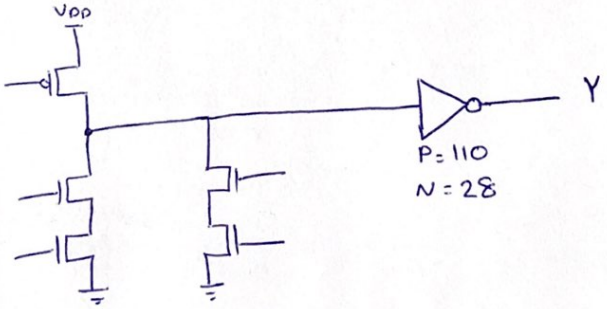
2) Evaluation phase : use PMOS transistor for the pullup network and NMOS for the Pull down

calculate electrical affort : $H = \frac{C_{out}}{C_{in}} = \frac{500}{30} = 16.6$

logical effort : $G = \frac{2}{3} \times \frac{5}{6} = \frac{10}{18}$, Parasitic delay : $P = \frac{5}{3} + \frac{5}{6} = \frac{5}{2}$

$F = GBH = 9.3$ $\quad \hat{f} = F^{\frac{1}{N}} = F^{\frac{1}{2}} = 3$ $\quad \Rightarrow D = 2\hat{f} + P = 8.6\,\tau$

Inverter size : $\frac{500 \times \frac{5}{6}}{3} \simeq 138.8 \simeq 138$

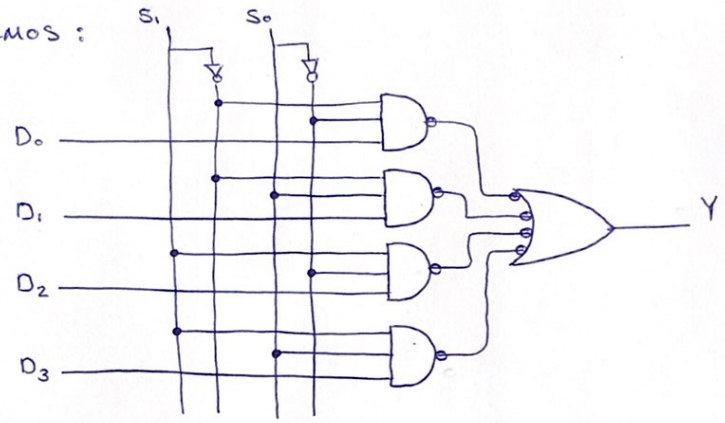


9.38 : How many transistors are used in 4X1 MUX?

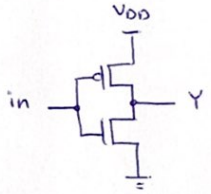
a) Use only static CMOS logic gates.

b) Use a combination of logic gates and transmition gates.

a) use static CMOS :

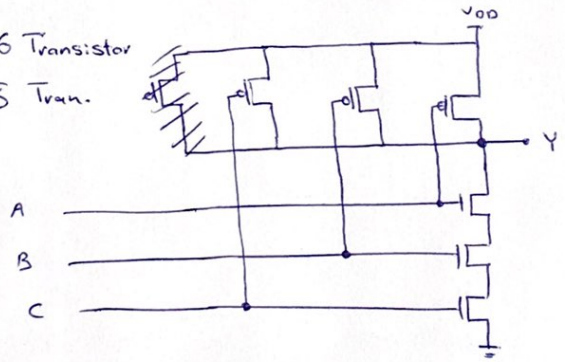


Static CMOS Inverter ⟶ 2 Transistor :



Static CMOS NAND3 ⟶ 6 Transistor

Static CMOS NaND4 ⟶ 8 Tran.

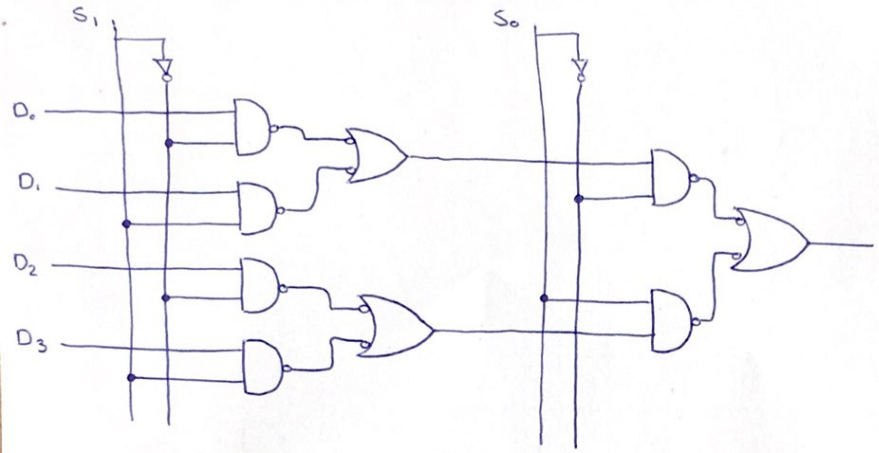


Now
- 4 NAND3 ⟶ 24
- 1 NAND4 ⟶ 8
- 2 Inverter ⟶ 4

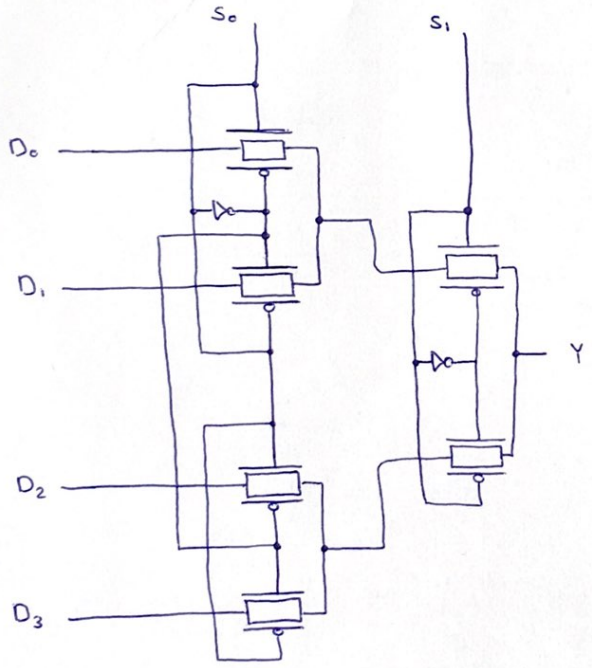
\+ = 36

Total of transistor for 4X1 MUX with static CMOS

b) Now use Combination of logic gates and transmition gates.

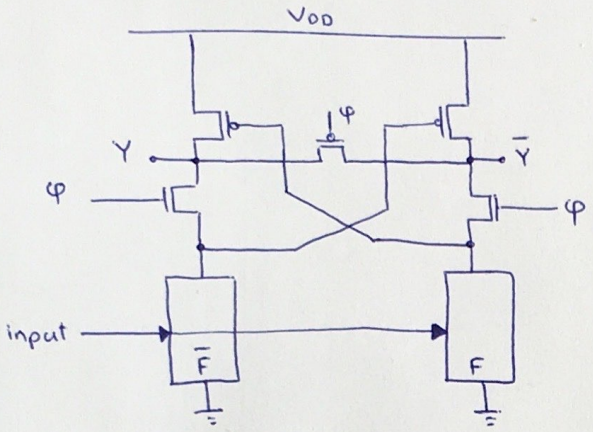


40 Transistor



16 Transistor

9.42 :



SOD structure

when the clk is low, two output is equal at $\frac{V_{DD}}{2}$. when the clock is rised, one side pulls down, fully turning ON the pmos transistor to pull the other side up.

This gate saved precharg power relative to dynamic logic because the Precharge equalizes the two outputs rather than drawing power from the rail.