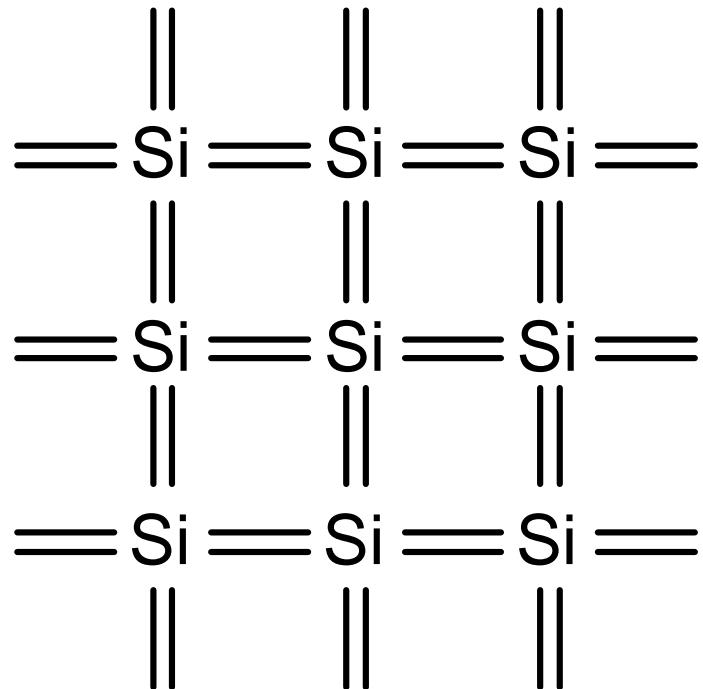


MOSFET Transistors

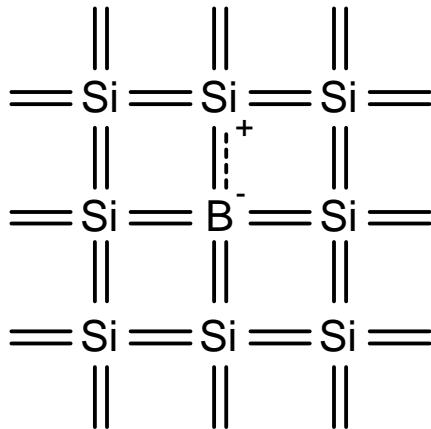
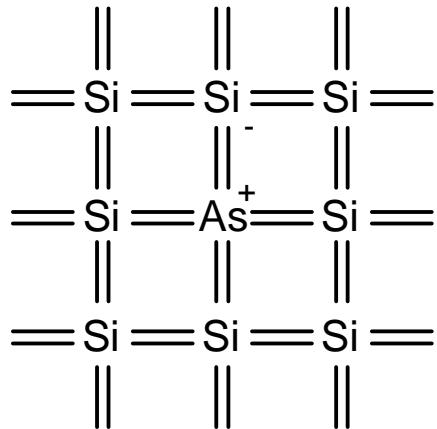
Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors



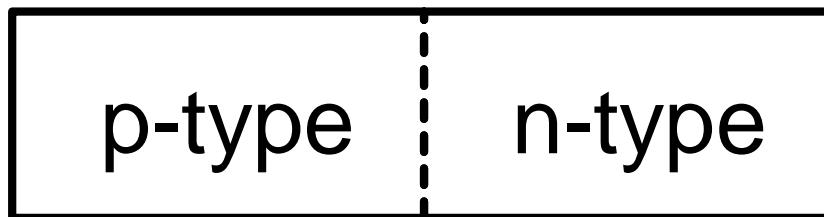
Dopants

- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)

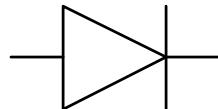


p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction

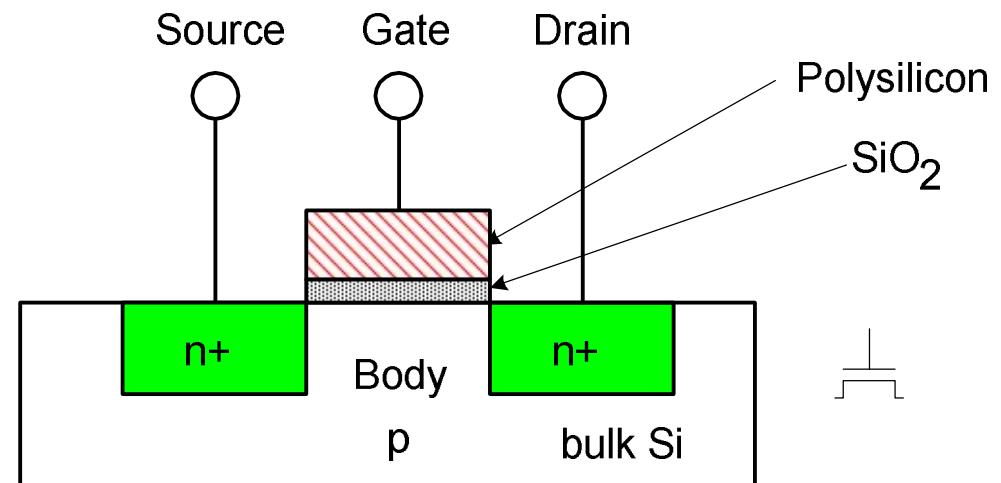


anode cathode



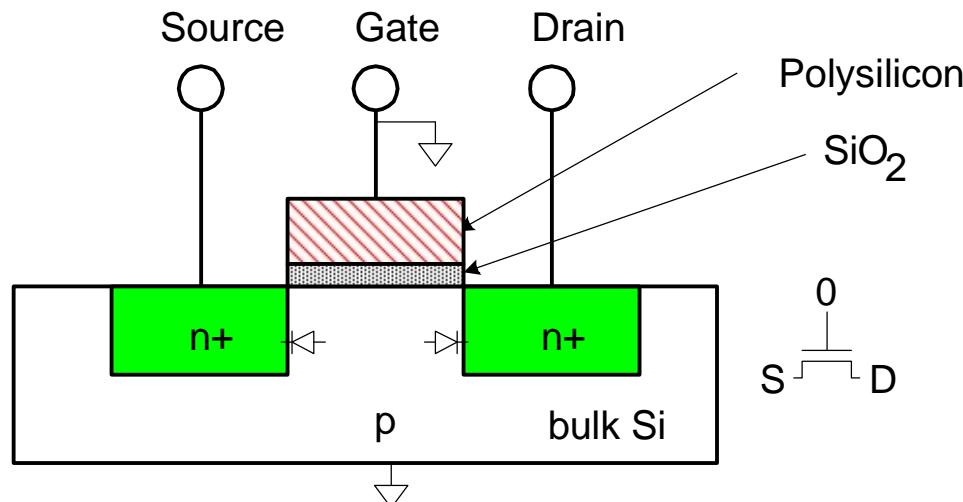
nMOS Transistor

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
 - Gate and body are conductors
 - SiO_2 (oxide) is a very good insulator
 - Called metal – oxide – semiconductor (MOS) capacitor



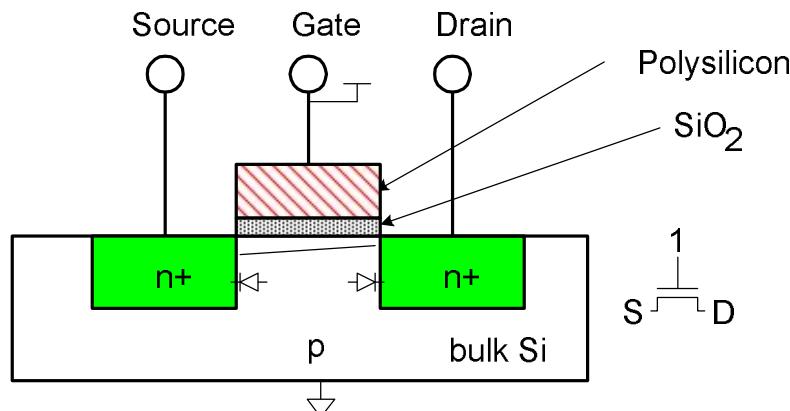
nMOS Operation

- Body is usually tied to ground (0 V)
- When the gate is at a low voltage:
 - P-type body is at low voltage
 - Source-body and drain-body diodes are OFF
 - No current flows, transistor is OFF



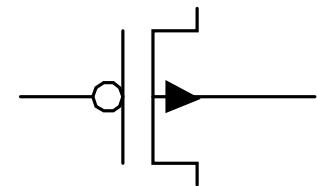
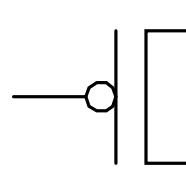
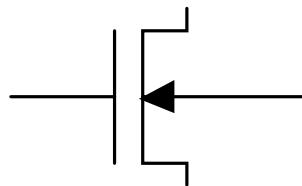
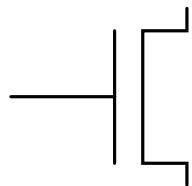
nMOS Operation Cont.

- When the gate is at a high voltage:
 - Positive charge on gate of MOS capacitor
 - Negative charge attracted towards gate
 - Inverts a channel under gate to n-type
 - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



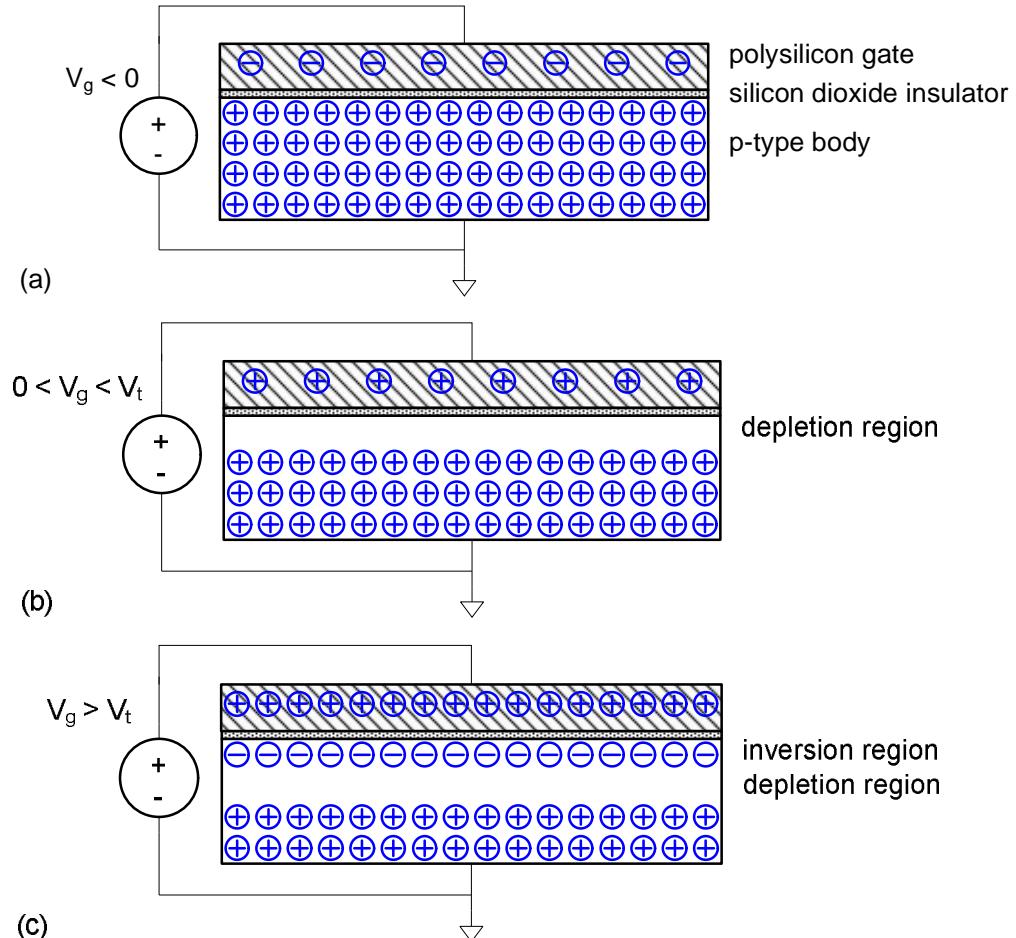
Large Picture

- An ON transistor passes a finite amount of current
 - Depends on terminal voltages
 - Derive current-voltage (I-V) relationships
- Transistor gate, source, drain all have capacitance
 - $I = C (\Delta V / \Delta t) \rightarrow \Delta t = (C/I) \Delta V$
 - Capacitance and current determine speed



MOS Capacitor

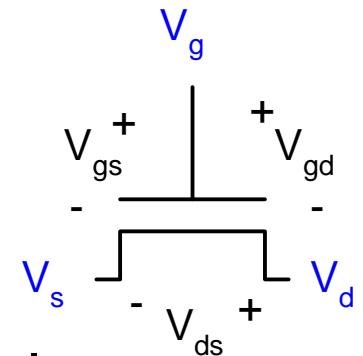
- Gate and body form MOS capacitor
- Operating modes
 - Accumulation
 - Depletion
 - Inversion



Terminal Voltages

- ❑ Mode of operation depends on V_g , V_d , V_s

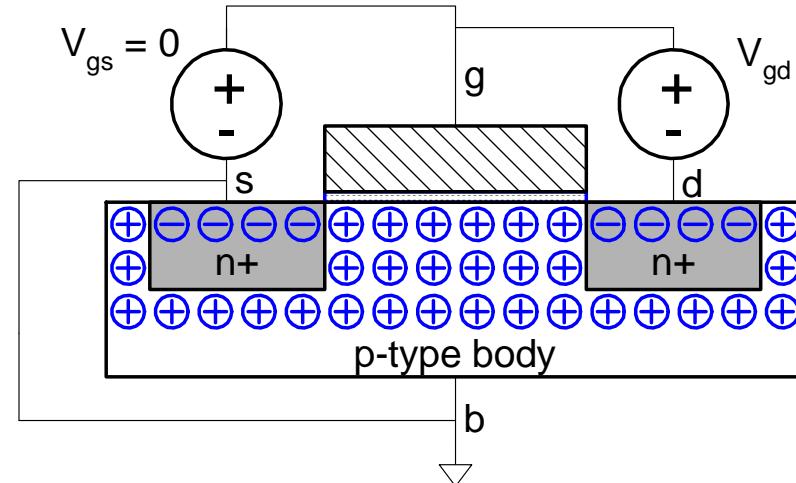
- $V_{gs} = V_g - V_s$
- $V_{gd} = V_g - V_d$
- $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$



- ❑ Source and drain are symmetric diffusion terminals
 - By convention, source is terminal at lower voltage
 - Hence $V_{ds} \geq 0$
- ❑ nMOS body is grounded. First assume source is 0 too.
- ❑ Three regions of operation
 - *Cutoff*
 - *Linear*
 - *Saturation*

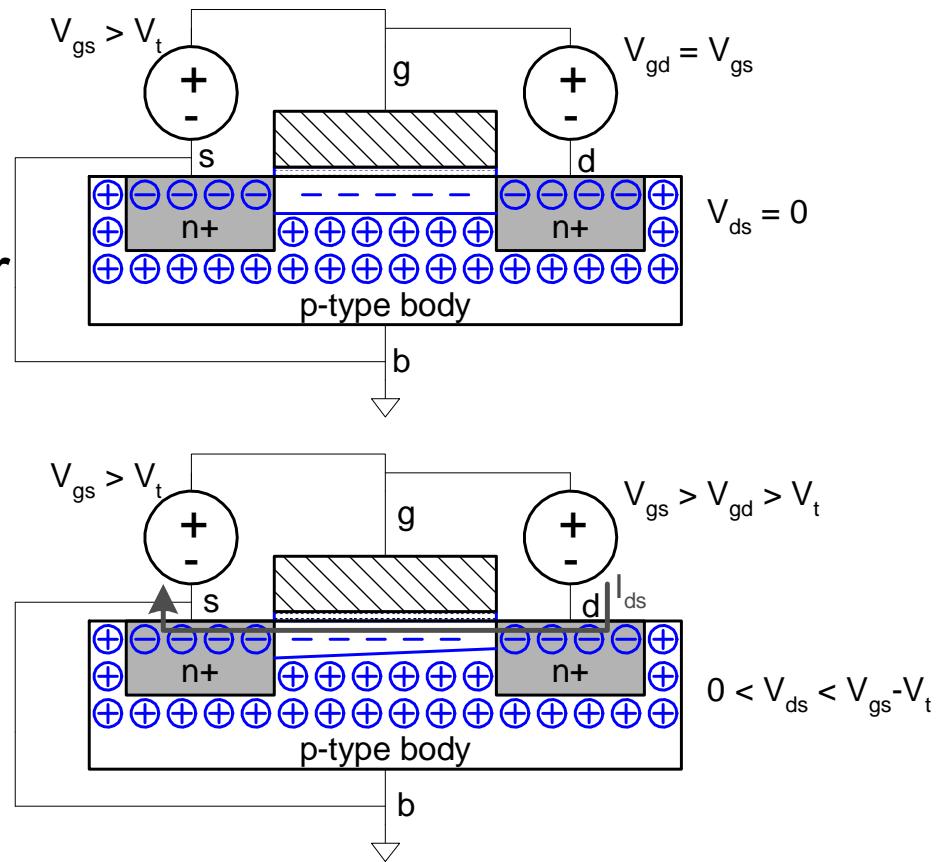
nMOS Cutoff

- ❑ No channel
- ❑ $I_{ds} \approx 0$



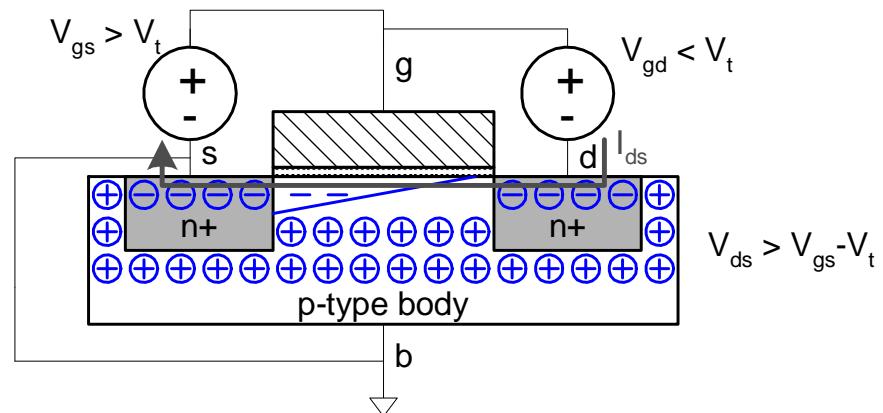
nMOS Linear

- Channel forms
- Current flows from d to s
 - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor



nMOS Saturation

- ❑ Channel pinches off
- ❑ I_{ds} independent of V_{ds}
- ❑ We say current *saturates*
- ❑ Similar to current source



I-V Characteristics

- In Linear region, I_{ds} depends on
 - How much charge is in the channel?
 - How fast is the charge moving?

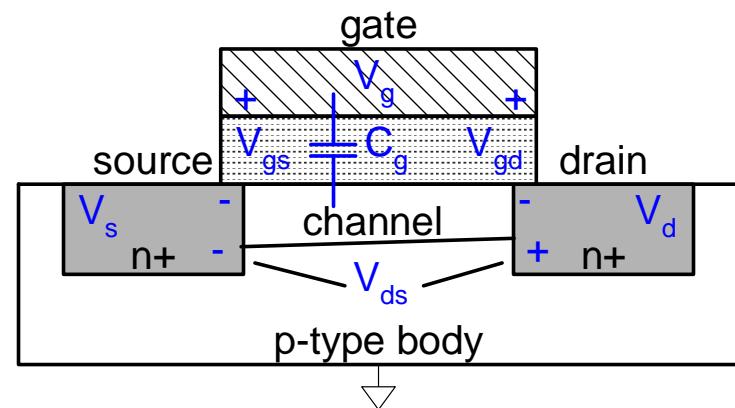
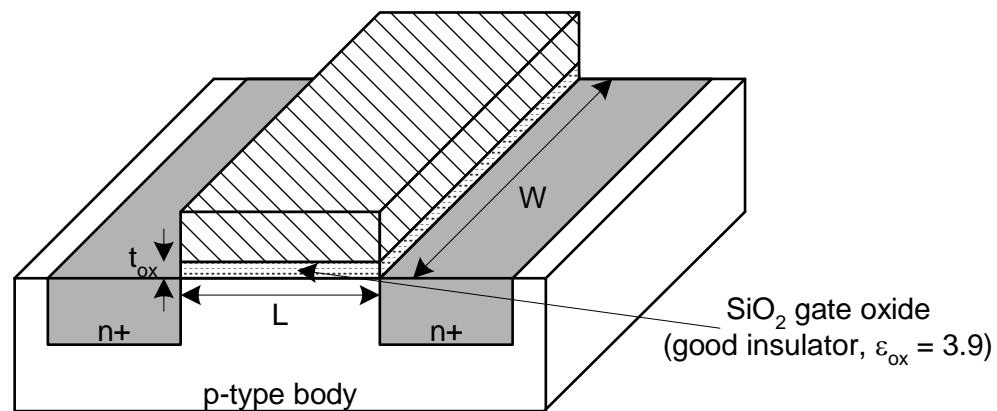
Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversions
 - Gate – oxide – channel

- $Q_{\text{channel}} =$

-

-



Carrier velocity

- Charge is carried by e-
- Electrons are propelled by the lateral electric field between source and drain
 - $E =$
- Carrier velocity v proportional to lateral E-field
 - $v =$
- Time for carrier to cross channel:
 - $t =$

nMOS Linear I-V

- Now we know
 - How much charge Q_{channel} is in the channel
 - How much time t each carrier takes to cross

$$I_{ds} =$$

$$=$$

$$=$$

nMOS Saturation I-V

- ❑ If $V_{gd} < V_t$, channel pinches off near drain
 - When $V_{ds} > V_{dsat} =$
- ❑ Now drain voltage no longer increases current

$$I_{ds} =$$

$$=$$

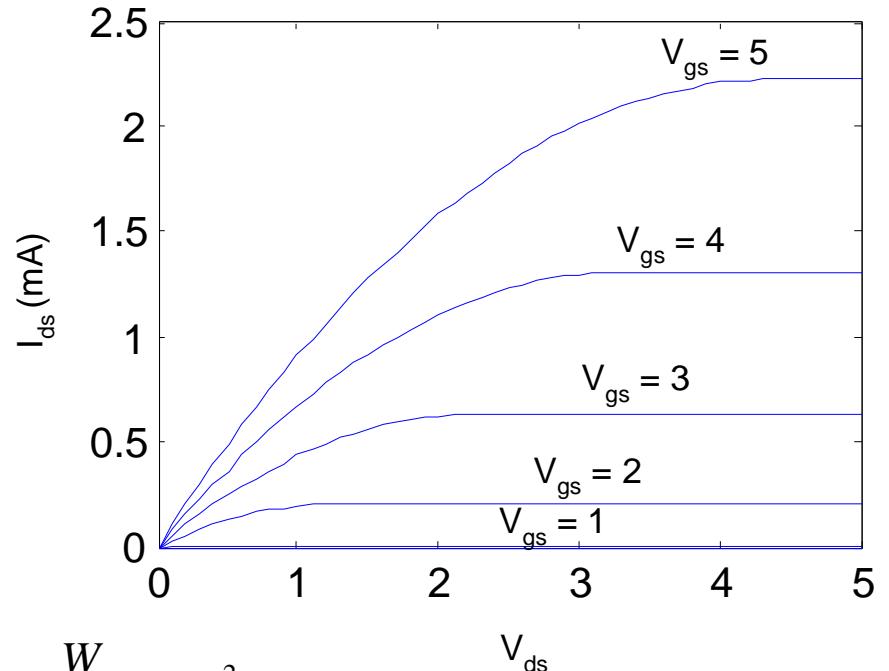
nMOS I-V Summary

- Shockley 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

Example

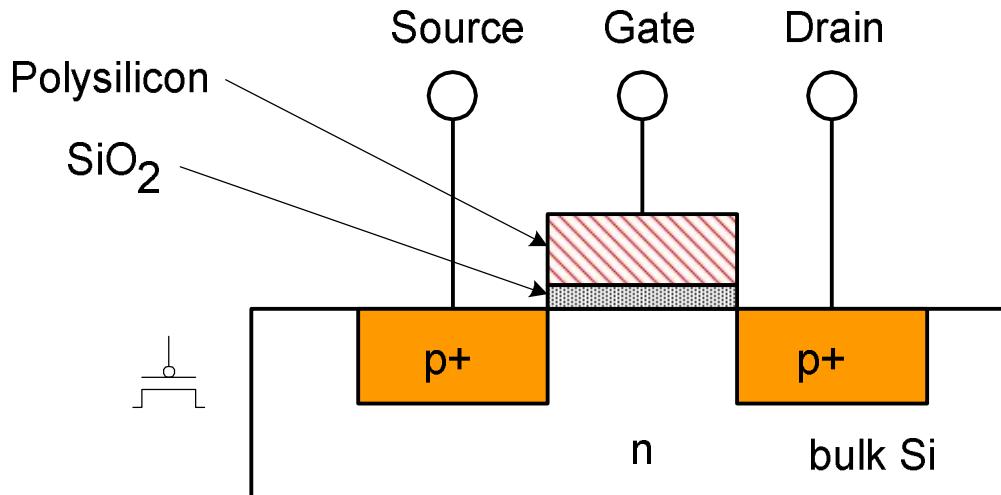
- We will be using a $0.6 \mu\text{m}$ process for your project
 - From AMI Semiconductor
 - $t_{\text{ox}} = 100 \text{ \AA}$
 - $\mu = 350 \text{ cm}^2/\text{V}\cdot\text{s}$
 - $V_t = 0.7 \text{ V}$
- Plot I_{ds} vs. V_{ds}
 - $V_{\text{gs}} = 0, 1, 2, 3, 4, 5$
 - Use $W/L = 4/2 \lambda$



$$\beta = \mu C_{\text{ox}} \frac{W}{L} = (350) \left(\frac{3.9 \times 8.85 \cdot 10^{-14}}{100 \cdot 10^{-8}} \right) \left(\frac{W}{L} \right) = 120 \frac{W}{L} \mu\text{A/V}^2$$

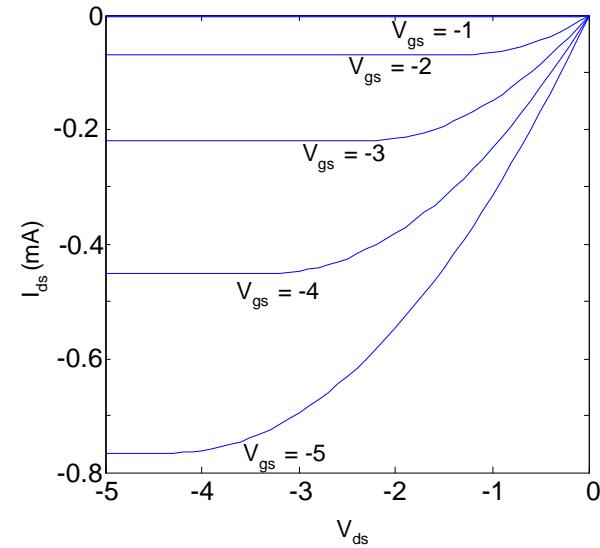
pMOS Transistor

- Similar, but doping and voltages reversed
 - Body tied to high voltage (V_{DD})
 - Gate low: transistor ON
 - Gate high: transistor OFF
 - Bubble indicates inverted behavior



pMOS I-V

- ❑ All dopings and voltages are inverted for pMOS
 - Source is the more positive terminal
- ❑ Mobility μ_p is determined by holes
 - Typically 2-3x lower than that of electrons μ_n
 - $120 \text{ cm}^2/\text{V}\cdot\text{s}$ in AMI 0.6 μm process
- ❑ Thus pMOS must be wider to provide same current
 - In this class, assume $\mu_n / \mu_p = 2$

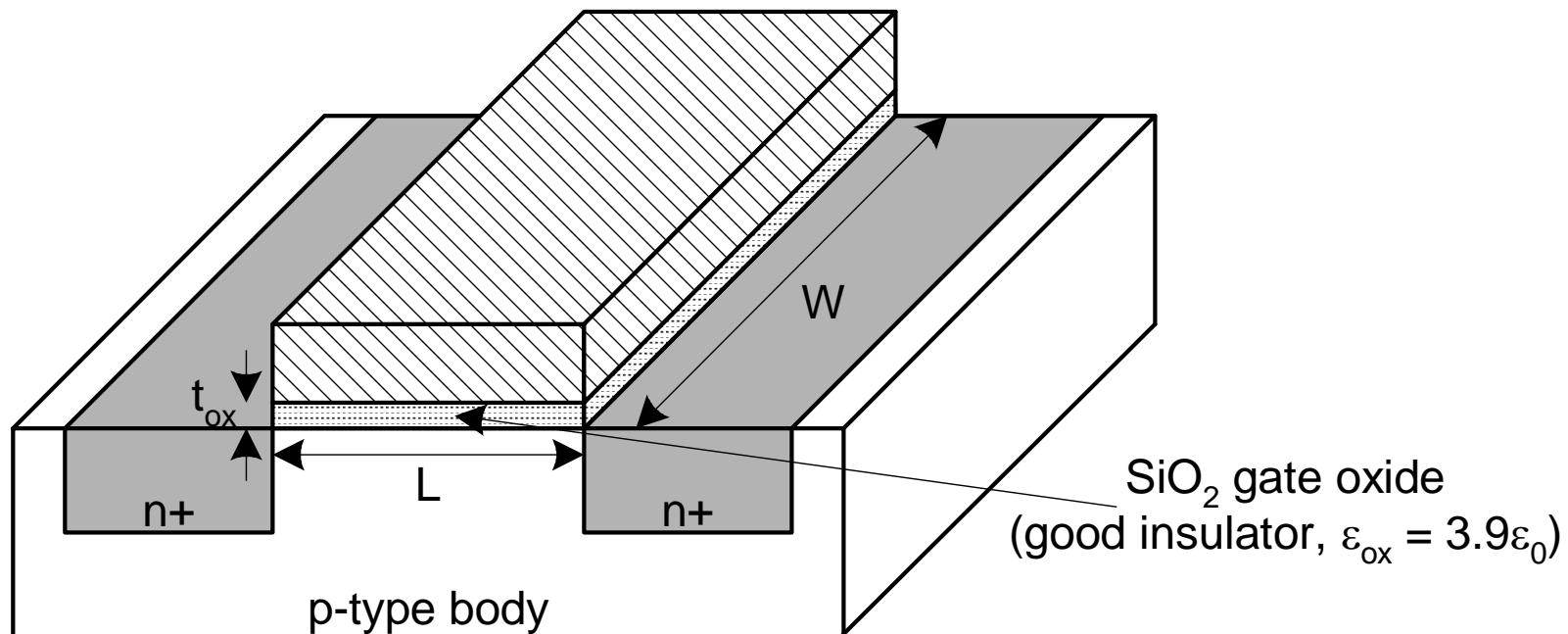


Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
 - Creates channel charge necessary for operation
- Source and drain have capacitance to body
 - Across reverse-biased diodes
 - Called diffusion capacitance because it is associated with source/drain diffusion

Gate Capacitance

- ❑ Approximate channel as connected to source
- ❑ $C_{gs} = \epsilon_{ox} WL/t_{ox} = C_{ox}WL = C_{\text{permicron}}W$
- ❑ $C_{\text{permicron}}$ is typically about $2 \text{ fF}/\mu\text{m}$



Power Supply Voltage

- ❑ GND = 0 V
- ❑ In 1980's, $V_{DD} = 5V$
- ❑ V_{DD} has decreased in modern processes
 - High V_{DD} would damage modern tiny transistors
 - Lower V_{DD} saves power
- ❑ $V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, \dots$