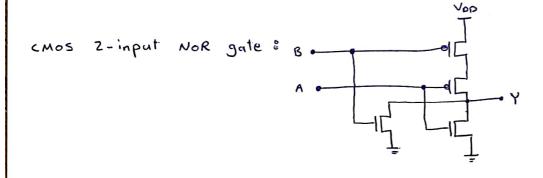
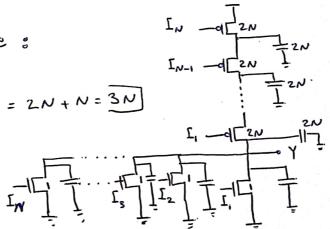
Reza Adinepour HW03 - chapter 4 402 131055

4.4: Find the worst-case Elmore parasitic delay of an n-input NOR gate



cmos n-input NOR gate :

total of c on Y node = 2N+N= 3N



I, - IN-1 all at 0 and IN goes from 0 to 1 worst case for Fall-Time &

$$R_{x} \left[\sum_{i=1}^{N-1} 2NC + 3NC \right]$$

$$= R\left(2N^{2}C + NC\right) = RC\left(2N^{2} + N\right)$$

Worst case for Rise time &

[- In-1 at 0 and In goes from 1 to 0

$$\frac{R}{N}(2NC) + \frac{2n}{N}(2NC) + \dots + \frac{(N-1)R}{N}(2NC) + R(3NC)$$

$$= RC\left(\frac{1+\dots+N-1}{2}\right) + 3NCR$$

$$= RC\left(\frac{(N-1)N}{2}\right) + 3NRC$$

$$= RC\left(\frac{N^2-N}{2}\right) + 3NRC$$

$$= RC\left(\frac{N^2+2N}{2}\right)$$
so fall time is the worst case