

Introduction

About The Slides

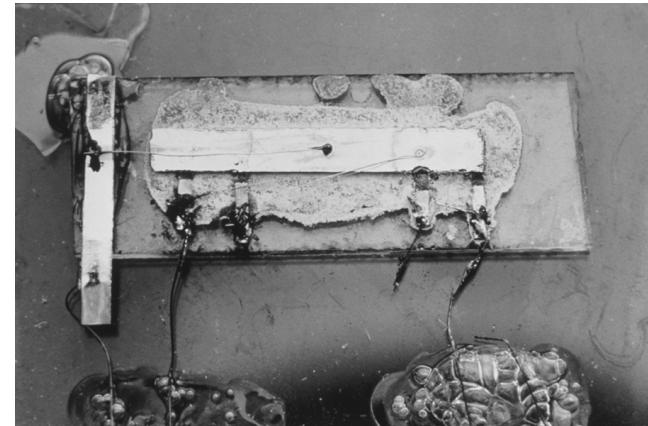
- ❑ Lecture notes ©2011 David Money Harris:
- ❑ These notes may be used and modified for educational and/or non-commercial purposes so long as the source is attributed.
- ❑ This is precisely what I have done (MS)

Outline

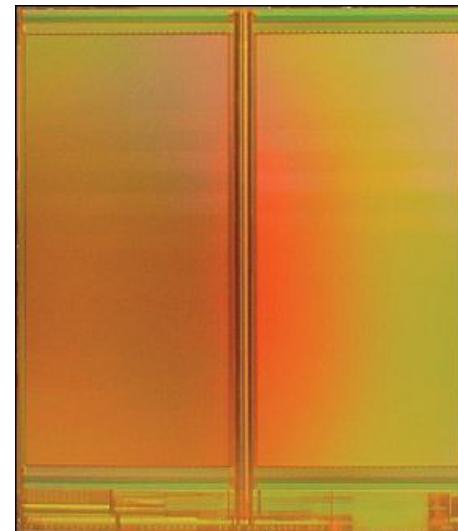
- A Brief History
- Introduction to MOSFETs
- Introduction to CMOS Gates
- Introduction to levels of abstraction

A Brief History

- 1958: First integrated circuit
 - Flip-flop using two transistors
 - Built by Jack Kilby at Texas Instruments
- 2010
 - Intel Core i7 μprocessor
 - 2.3 billion transistors
 - 64 Gb Flash memory
 - > 16 billion transistors



Courtesy Texas Instruments



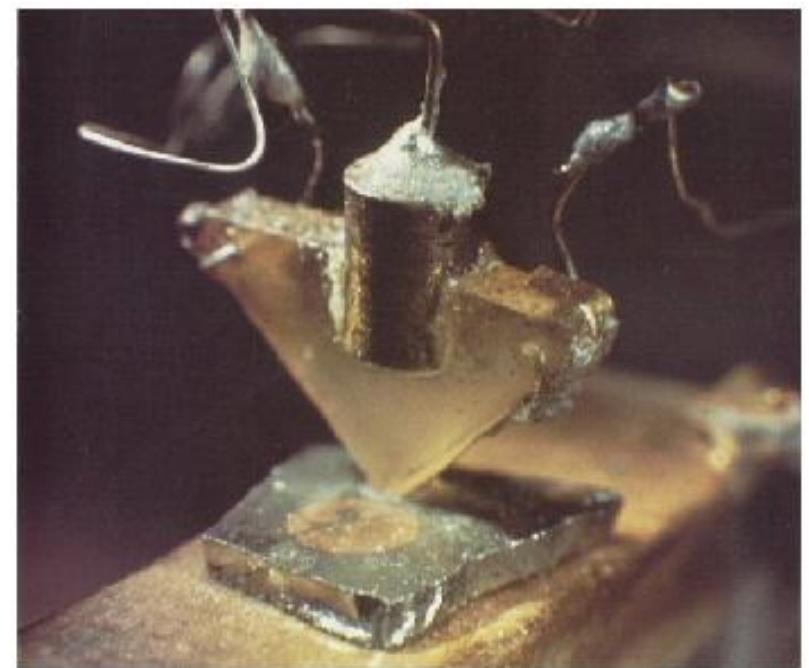
[Trinh09]
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Growth Rate

- 53% compound annual growth rate over 50 years
 - No other technology has grown so fast so long
- Driven by miniaturization of transistors
 - Smaller is cheaper, faster, lower in power (if designed carefully!)
 - Revolutionary effects on society

Invention of the Transistor

- Vacuum tubes ruled in first half of 20th century
Large, expensive, power-hungry, unreliable
- 1947: first point contact transistor
 - John Bardeen and Walter Brattain at Bell Labs
 - See *Crystal Fire*
by Riordan, Hoddeson



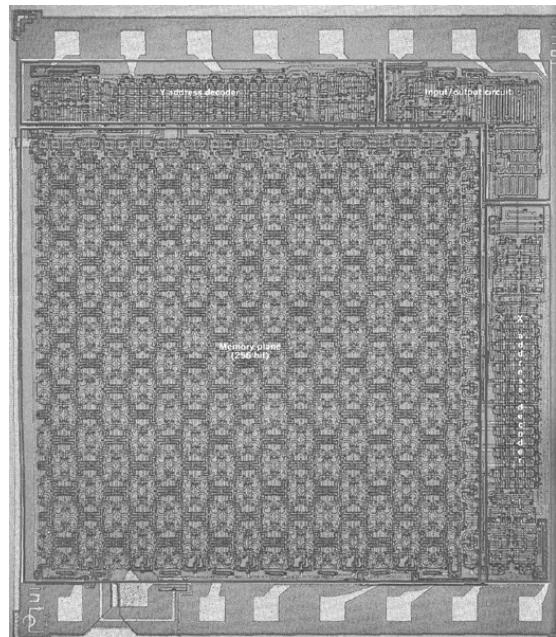
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Transistor Types

- Bipolar transistors
 - npn or pnp silicon structure
 - Small current into very thin base layer controls large currents between emitter and collector
 - Base currents limit integration density
- Metal Oxide Semiconductor Field Effect Transistors
 - nMOS and pMOS
 - Voltage applied to insulated gate controls current between source and drain
 - Low power allows very high integration

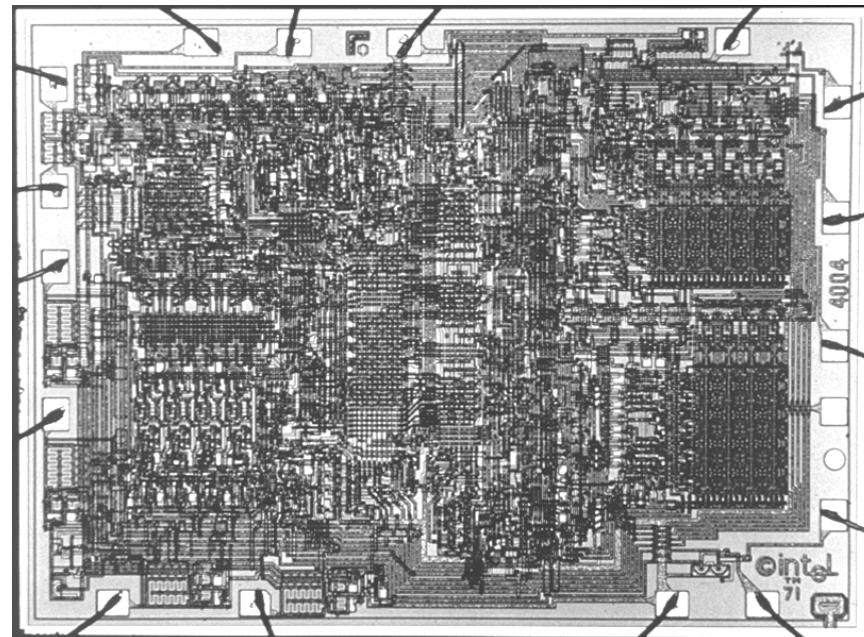
MOS Integrated Circuits

- 1970's processes usually had only nMOS transistors
 - Inexpensive, but consume power while idle



[Vadasz69]
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Intel 1101 256-bit SRAM



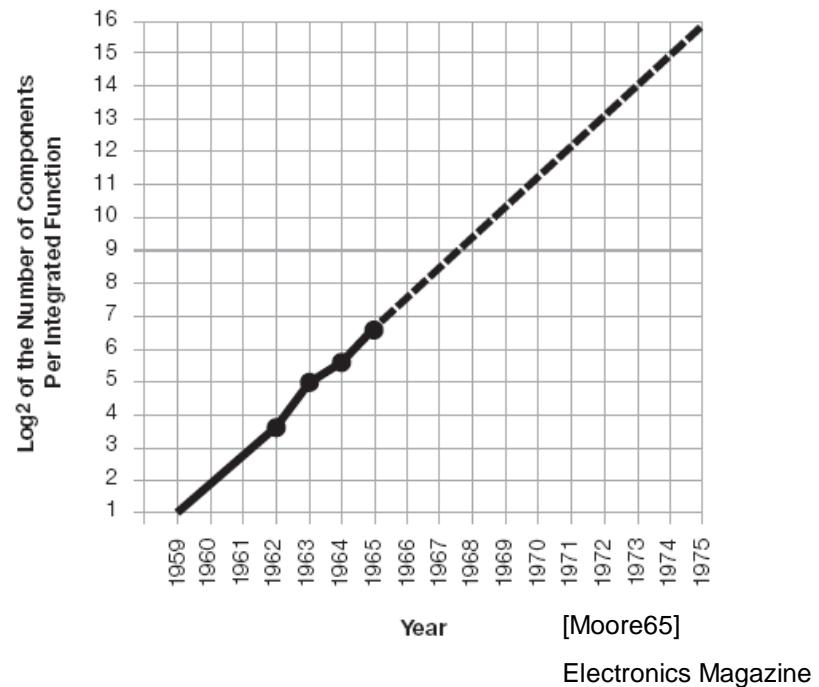
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Intel 4004 4-bit μ Proc

- 1980s-present: CMOS processes for low idle power

Moore's Law: Then

- 1965: Gordon Moore plotted transistor on each chip
 - Fit straight line on semilog scale
 - Transistor counts have doubled every 26 months



Integration Levels

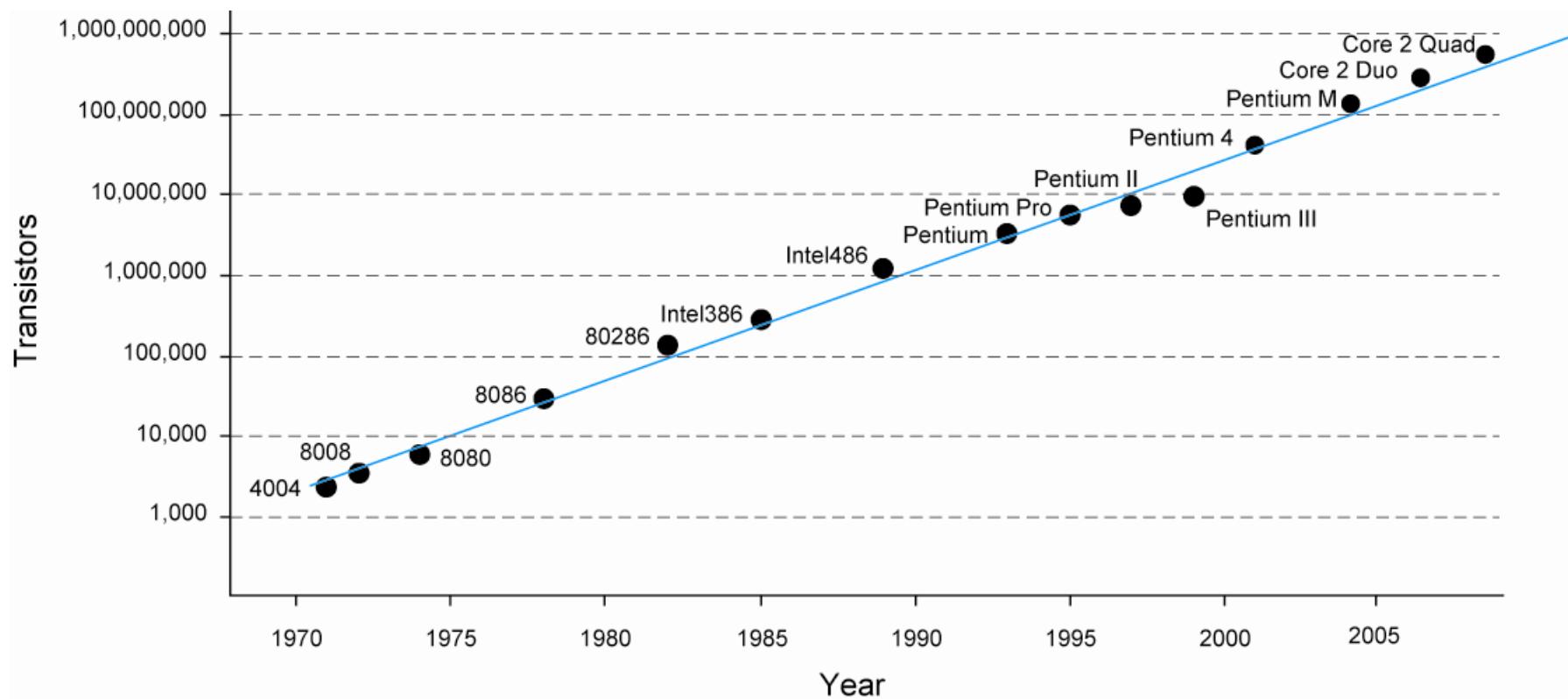
SSI: 10 gates

MSI: 1000 gates

LSI: 10,000 gates

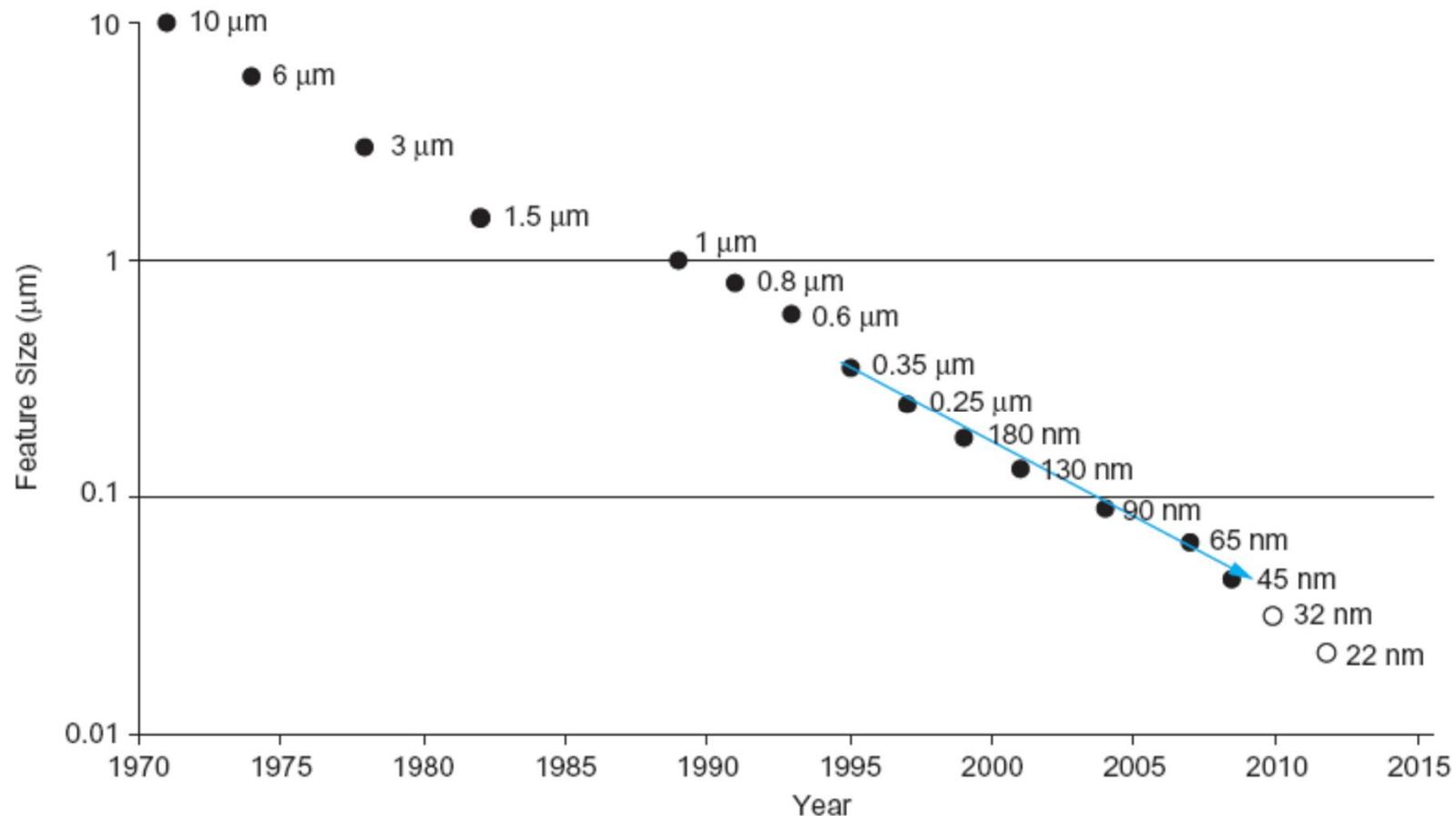
VLSI: > 10k gates

And Now...



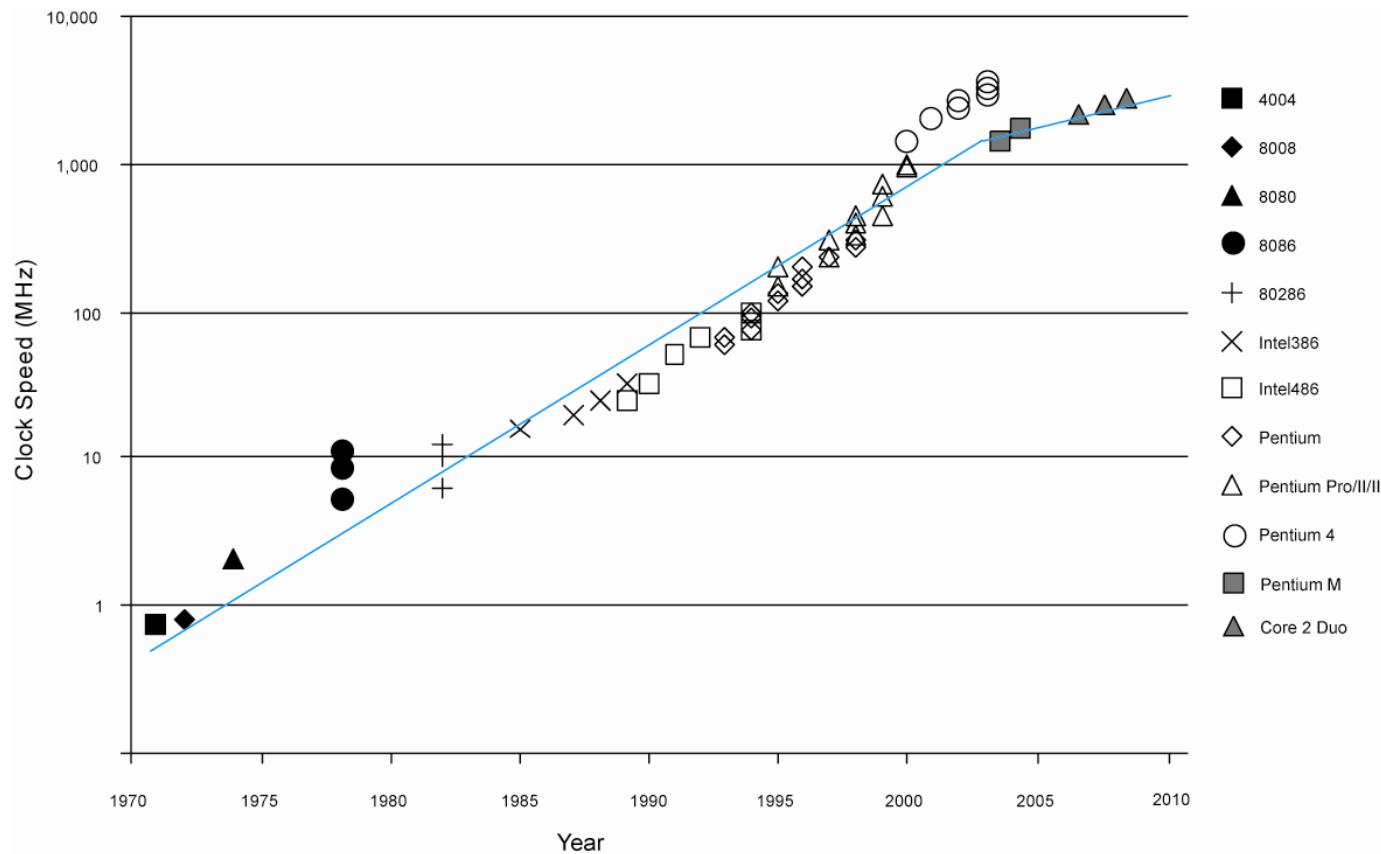
Feature Size

- Minimum feature size shrinking 30% every 2-3 years



Corollaries

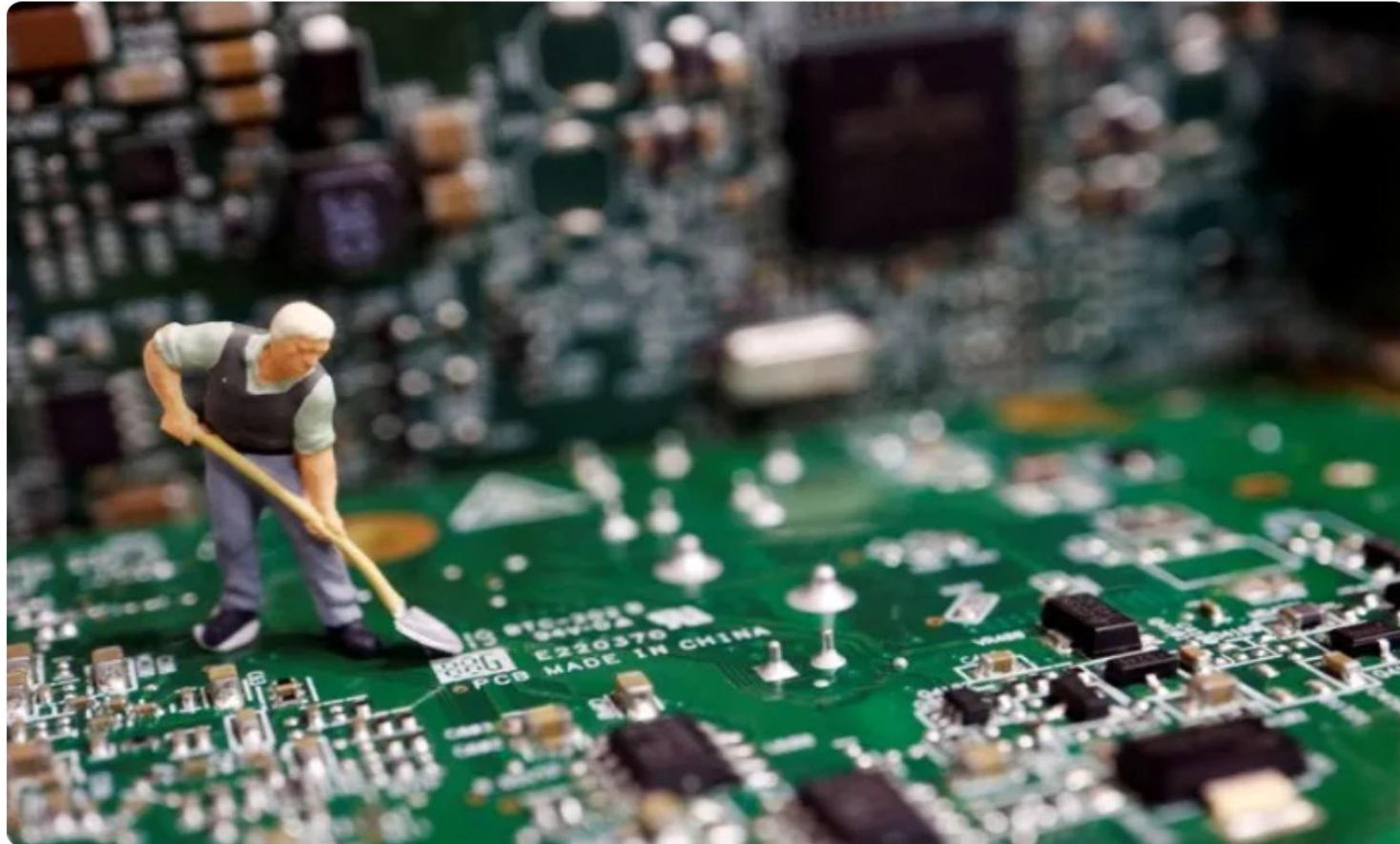
- Many other factors grow exponentially:
 - Clock frequency, processor performance, power



HW vs. SW?

- Integrated circuits: many transistors on one chip.
- *Very Large Scale Integration* (VLSI): Millions of transistors!
- Software technological advances require a hardware platform to execute
- Hence:

U.S. will be short 67,000 chip workers by 2030, industry group says



FILE PHOTO: Illustration picture of semiconductor chips

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Max A. Cherney

Tue, July 25, 2023 at 12:35 PM GMT+3:30 · 2 min read

Coping with Complexity

- How to design System-on-Chip?
 - Many millions (even billions!) of transistors
 - Tens to hundreds of engineers
- Structured design:
 - Levels of abstraction
- Design partitioning
- Hardware Description Languages (HDL's)
- Synthesis tools

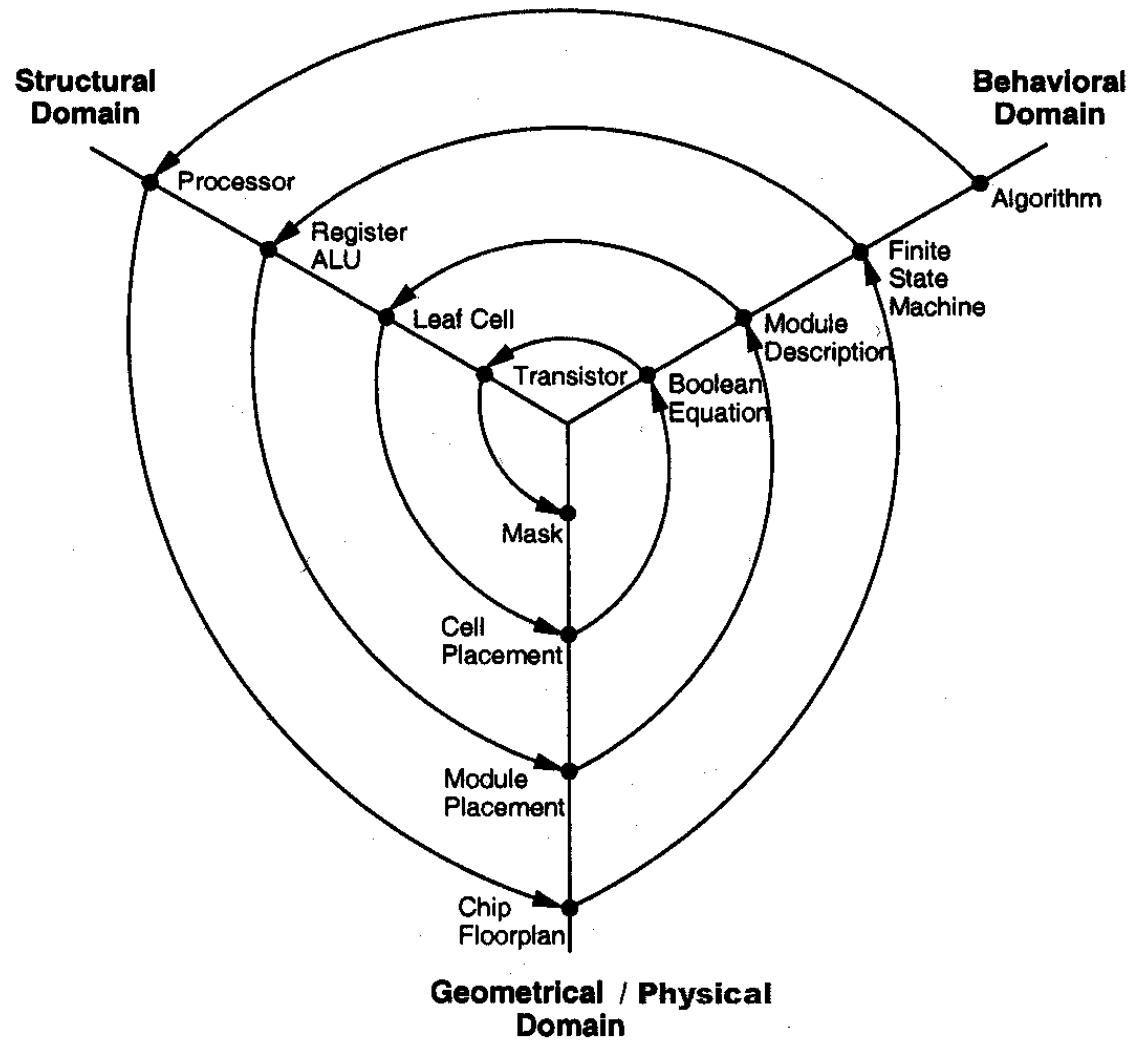
Structured Design

- **Hierarchy:** Divide and Conquer
 - Recursively system into modules
- **Regularity**
 - Reuse modules wherever possible
 - Ex: Standard cell library
- **Modularity:** well-formed interfaces
 - Allows modules to be treated as black boxes
- **Locality**
 - Physical and temporal

Design Partitioning

- **Architecture:** User's perspective, what does it do?
 - Instruction set, registers
 - MIPS, x86, Alpha, PIC, ARM, ...
 - **Microarchitecture**
 - Single cycle, multicycle, pipelined, superscalar?
 - **Logic:** how are functional blocks constructed
 - Ripple carry, carry lookahead, carry select adders
 - **Circuit:** how are transistors used
 - Complementary CMOS, pass transistors, domino
 - **Physical:** chip layout
 - Datapaths, memories, random logic
-

Gajski Y-Chart

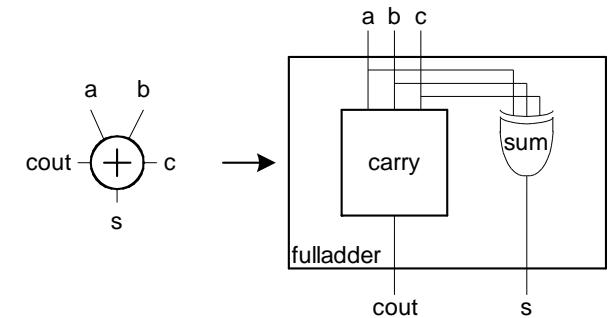


HDLs

- ❑ Hardware Description Languages
 - Widely used in logic design
 - Verilog and VHDL
- ❑ Describe hardware using code
 - Document logic functions
 - Simulate logic before building
 - Synthesize code into gates and layout
 - Requires a library of standard cells

Verilog Example

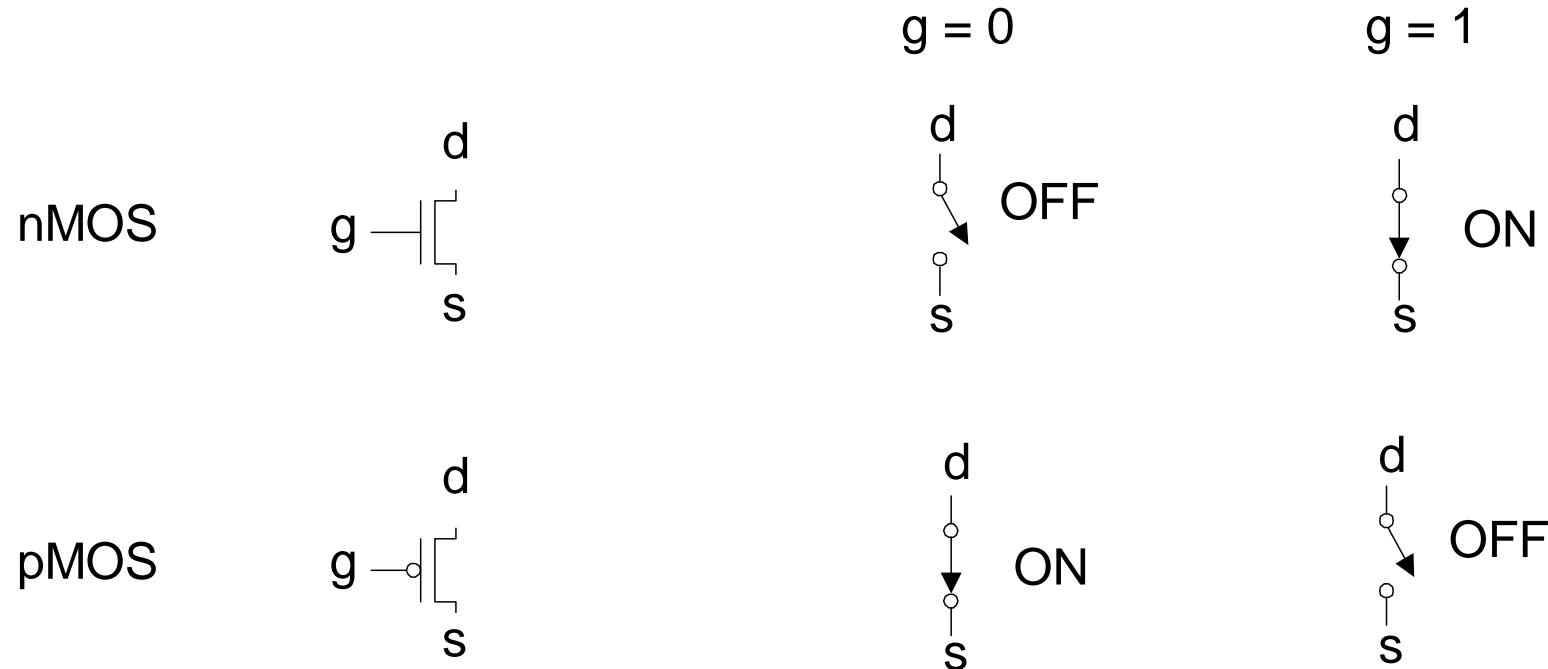
```
module fulladder(input a, b, c,  
                  output s, cout);  
  
    sum      s1(a, b, c, s);  
    carry    c1(a, b, c, cout);  
  
endmodule
```



```
module carry(input a, b, c,  
            output cout)  
  
    assign cout = (a&b) | (a&c) | (b&c);  
  
endmodule
```

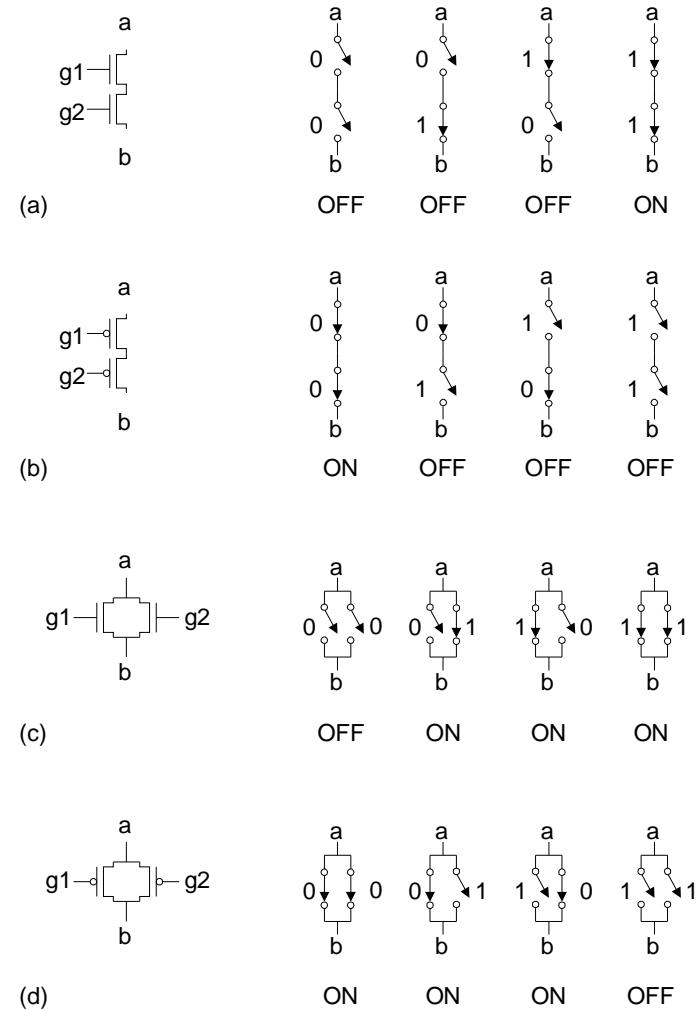
Transistors as Switches

- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



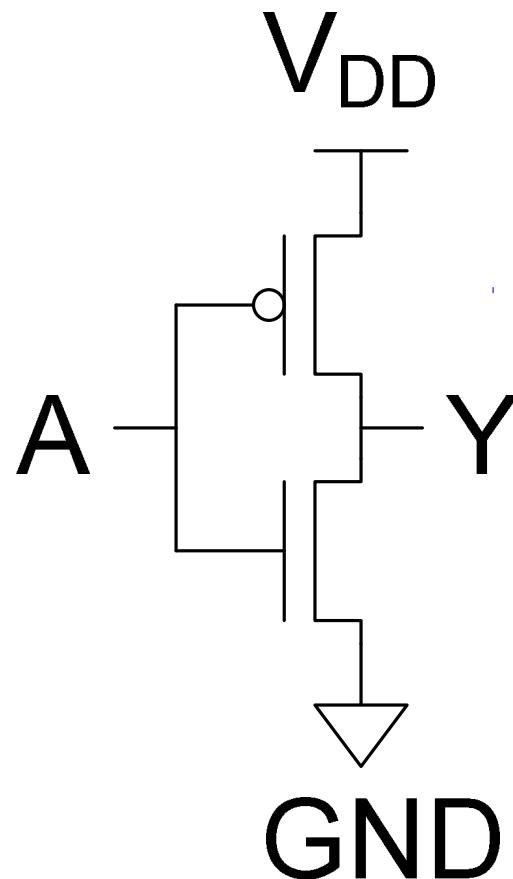
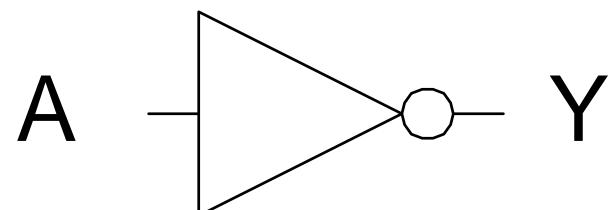
Series and Parallel

- nMOS: 1 = ON
- pMOS: 0 = ON
- Series: both must be ON
- Parallel: either can be ON



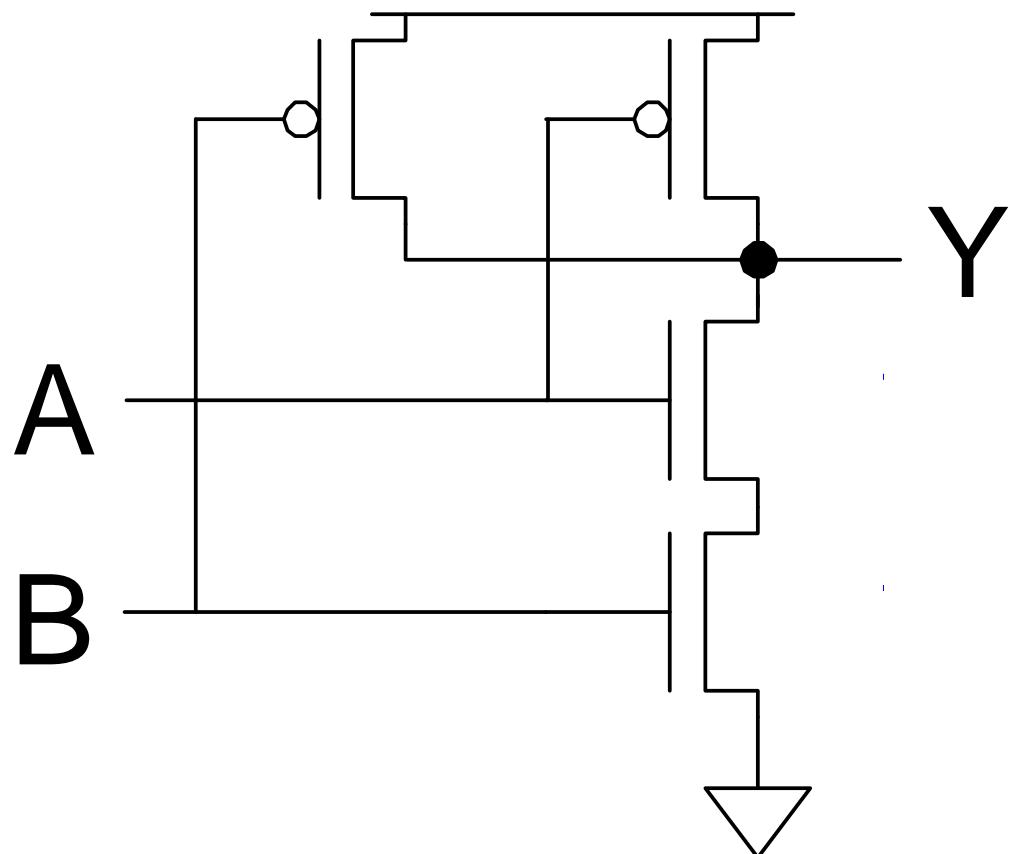
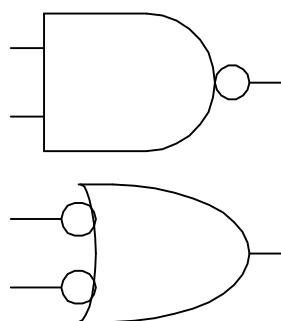
CMOS Inverter

A	Y
0	1
1	0



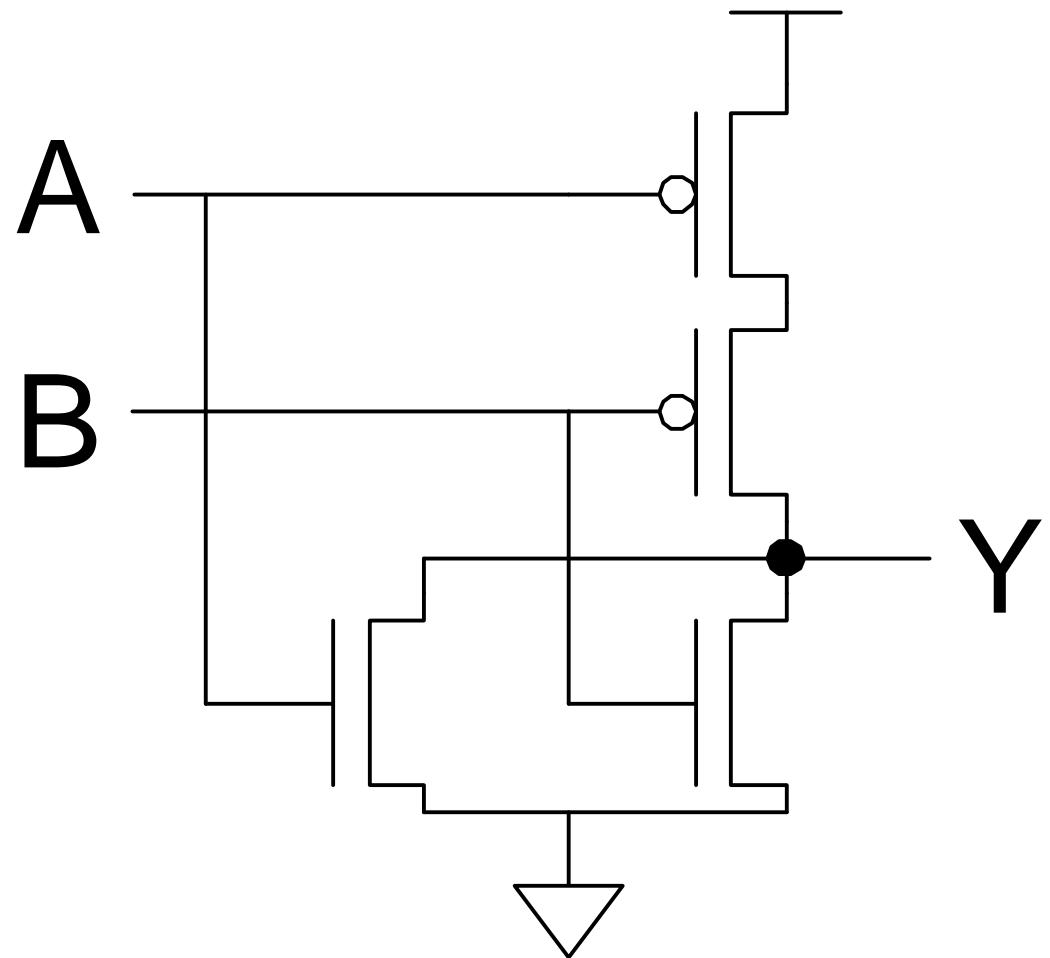
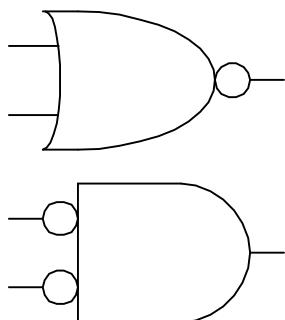
CMOS NAND Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	



CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

Summary

- MOS transistors act as electrically controlled switches
- Build logic gates out of switches
- In reality, MOS transistors are stacks of gate, oxide, silicon
- Next set of slide:
 - Moving from switch level to transistor level