

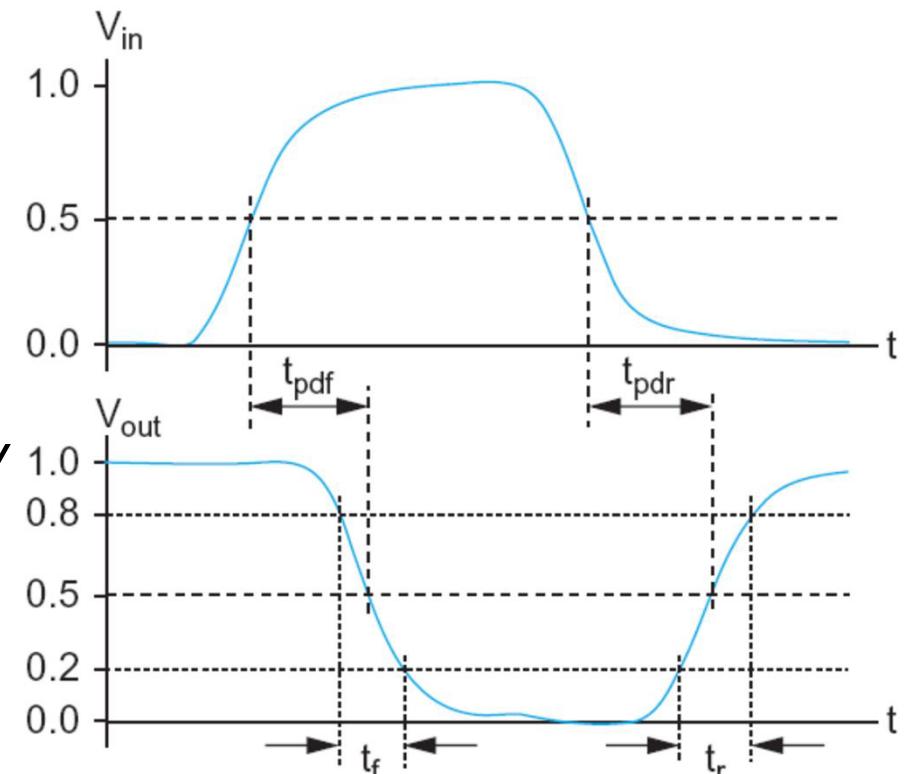
Delay

Outline

- Delay Definition
- Transient Response
- Delay Estimation:
 - RC Delay Model
 - Elmore Delay Model
 - Logical Effort will be discussed later

Delay Definitions

- t_{pdr} : *rising propagation delay*
 - From input to rising output crossing $V_{\text{DD}}/2$
- t_{pdf} : *falling propagation delay*
 - From input to falling output crossing $V_{\text{DD}}/2$
- t_{pd} : *average propagation delay*
 - $t_{\text{pd}} = (t_{\text{pdr}} + t_{\text{pdf}})/2$
- t_r : *rise time*
 - From output crossing 0.2 V_{DD} to 0.8 V_{DD}
- t_f : *fall time*
 - From output crossing 0.8 V_{DD} to 0.2 V_{DD}



Inverter Step Response

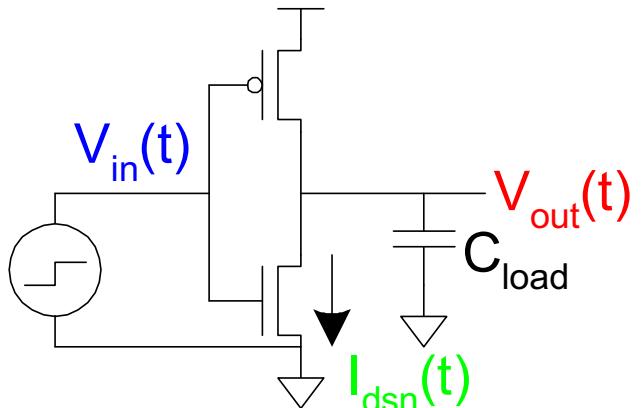
- Ex: find step response of inverter driving load cap

$$V_{in}(t) =$$

$$V_{out}(t < t_0) =$$

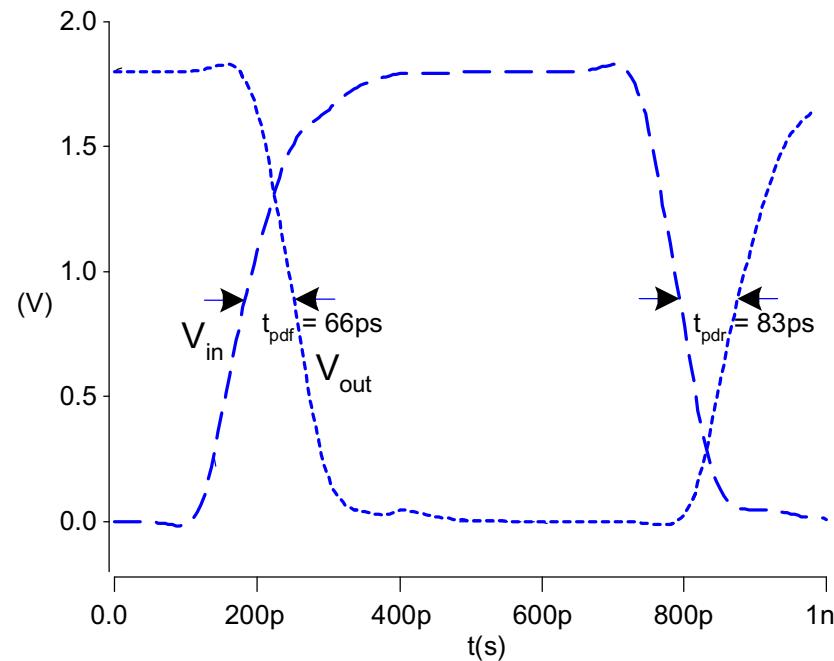
$$\frac{dV_{out}(t)}{dt} =$$

$$I_{dsn}(t) = \begin{cases} & t \leq t_0 \\ & V_{out} > V_{DD} - V_t \\ & V_{out} < V_{DD} - V_t \end{cases}$$



Simulated Inverter Delay

- Solving differential equations by hand is too hard
- SPICE simulator solves the equations numerically
 - Uses more accurate I-V models too!



Delay Estimation

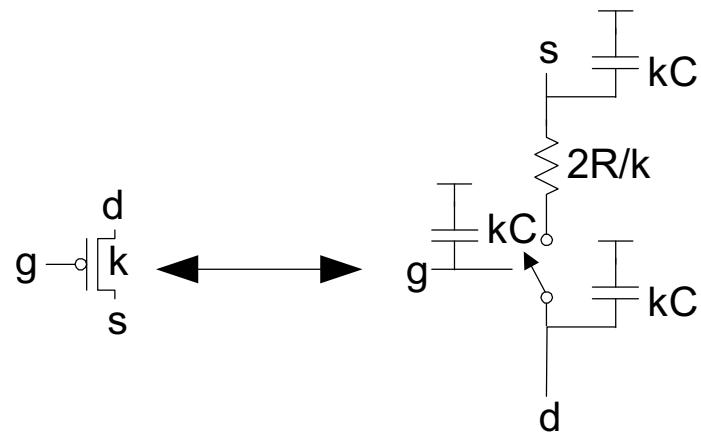
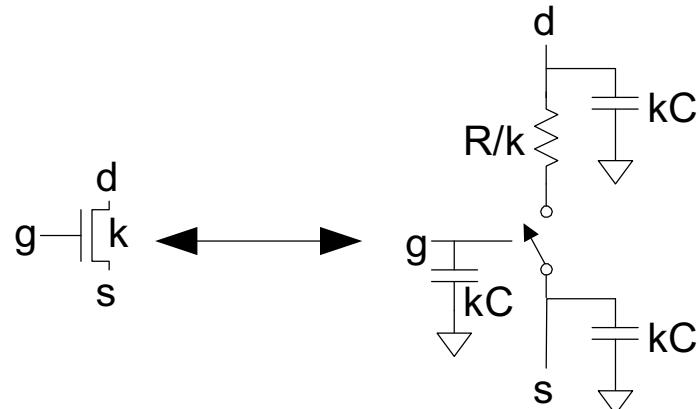
- We would like to be able to easily estimate delay
 - Not as accurate as simulation
 - But easier to ask “What if?”
- The step response usually looks like a 1st order RC response with a decaying exponential.
- Use RC delay models to estimate delay
 - C = total capacitance on output node
 - Use *effective resistance R*
 - So that $t_{pd} = RC$
- Characterize transistors by finding their effective R
 - Depends on average current as gate switches

Effective Resistance

- Shockley models have limited value
 - Not accurate enough for modern transistors
 - Too complicated for much hand analysis
- Simplification: treat transistor as resistor
 - Replace $I_{ds}(V_{ds}, V_{gs})$ with effective resistance R
 - $I_{ds} = V_{ds}/R$
 - R averaged across switching of digital gate
- Too inaccurate to predict current at any given time
 - But good enough to predict RC delay

RC Delay Model

- Use equivalent circuits for MOS transistors
 - Ideal switch + capacitance and ON resistance
 - Unit nMOS has resistance R , capacitance C
 - Unit pMOS has resistance $2R$, capacitance C
- Capacitance proportional to width
- Resistance inversely proportional to width

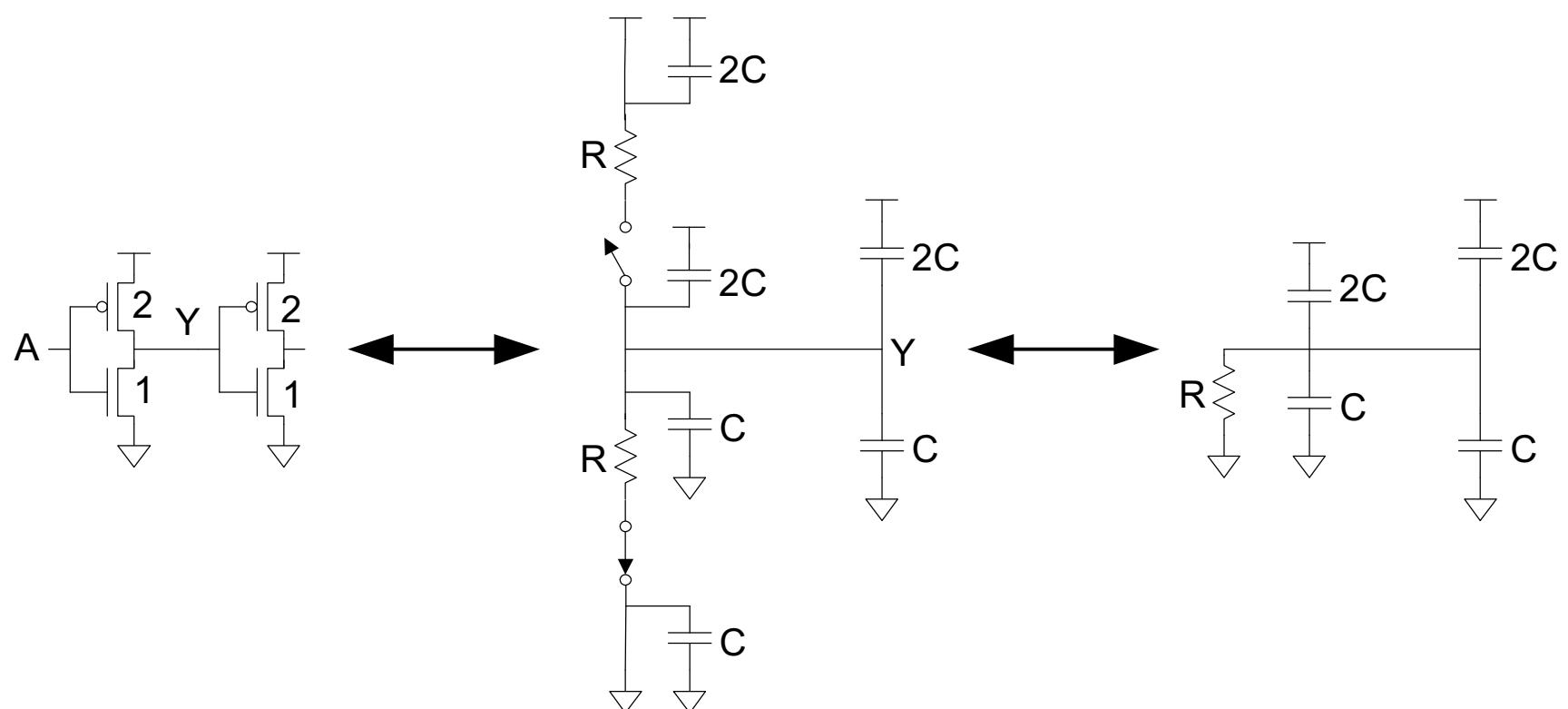


RC Values

- Capacitance
 - $C = C_g = C_s = C_d = 2 \text{ fF}/\mu\text{m}$ of gate width in 0.6 μm
 - Gradually decline to 1 $\text{fF}/\mu\text{m}$ in 65 nm
- Resistance
 - $R \approx 10 \text{ K}\Omega \cdot \mu\text{m}$ in 0.6 μm process
 - Improves with shorter channel lengths
 - 1.25 $\text{K}\Omega \cdot \mu\text{m}$ in 65 nm process
- Unit transistors
 - May refer to $k=1$
 - Doesn't matter as long as you are consistent

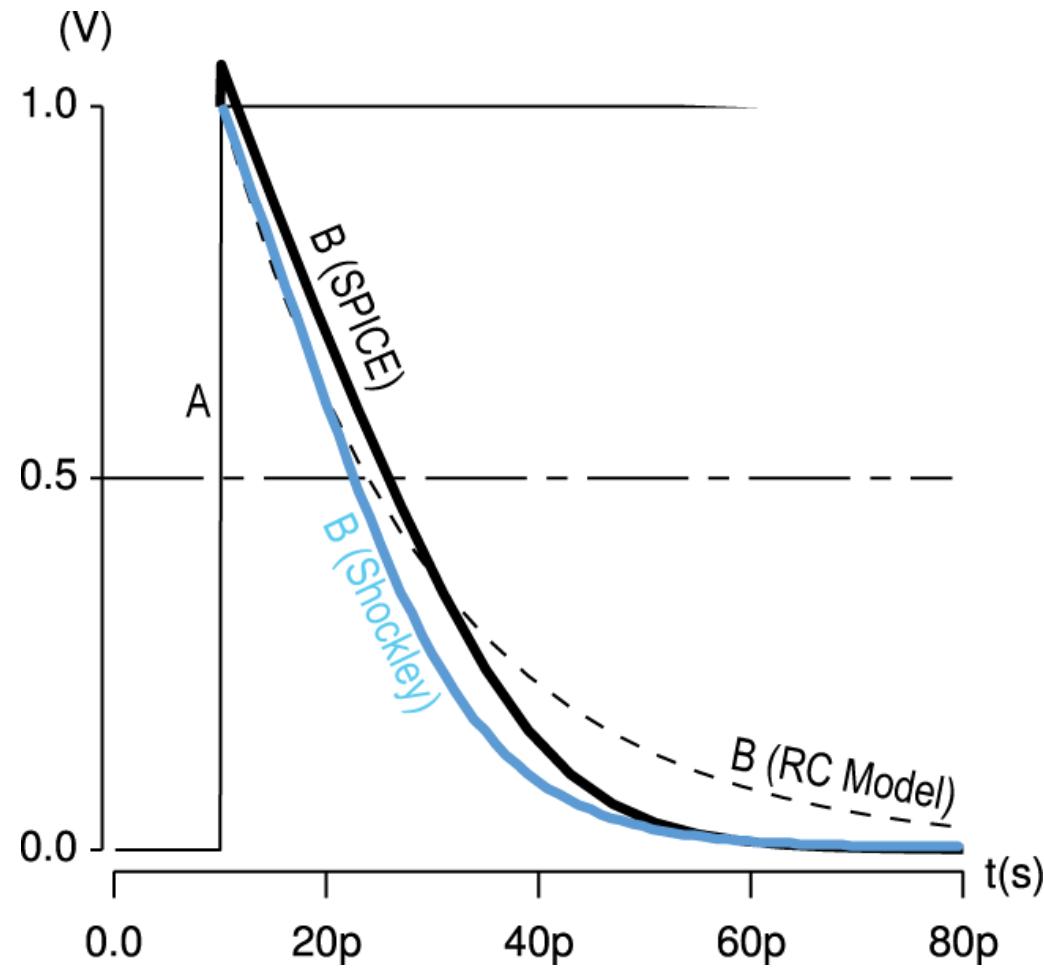
Inverter Delay Estimate

- Estimate the delay of a fanout-of-1 inverter



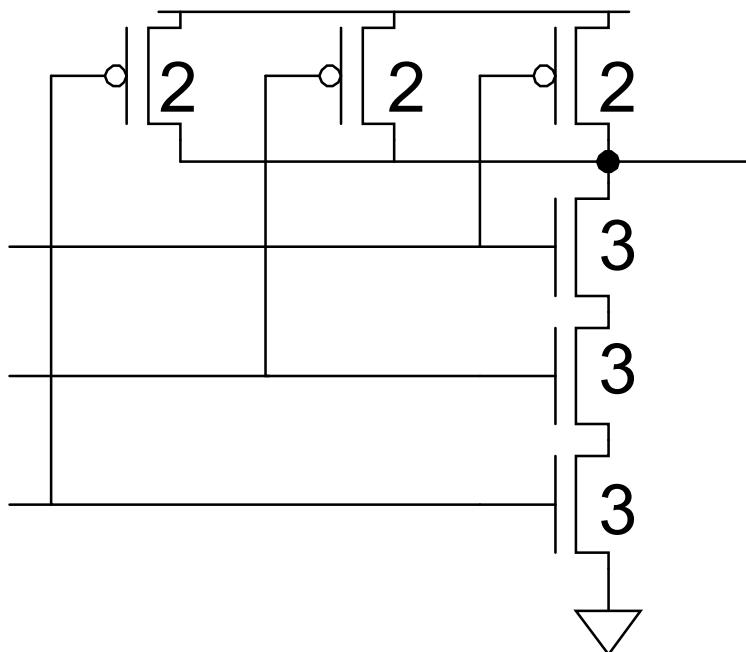
$$d = 6RC$$

Delay Model Comparison



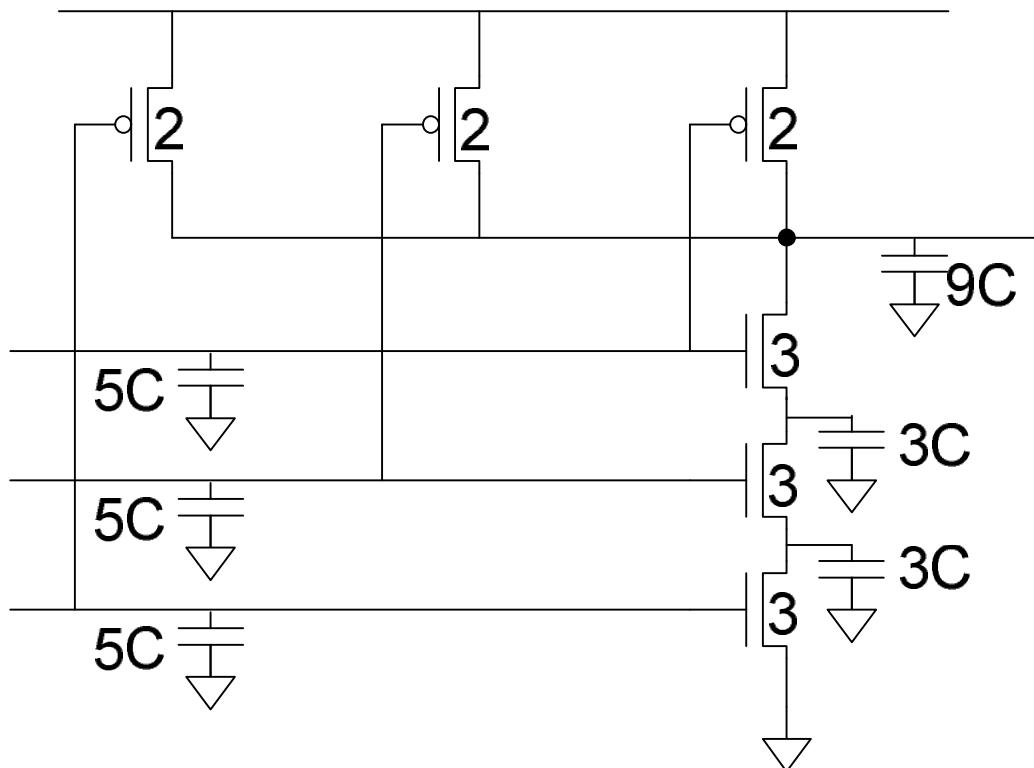
Example: 3-input NAND

- Sketch a 3-input NAND with transistor widths chosen to achieve effective rise and fall resistances equal to a unit inverter (R).



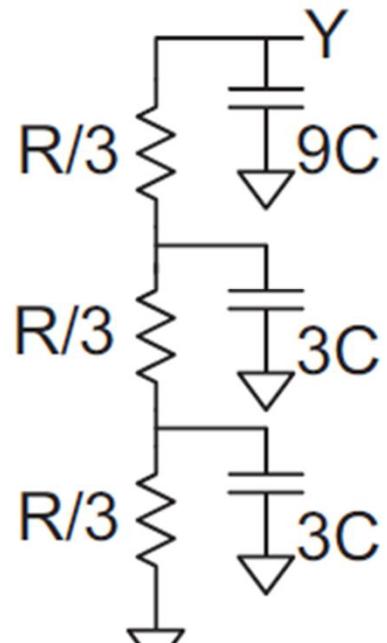
3-input NAND Caps

- Annotate the 3-input NAND gate with gate and diffusion capacitance:

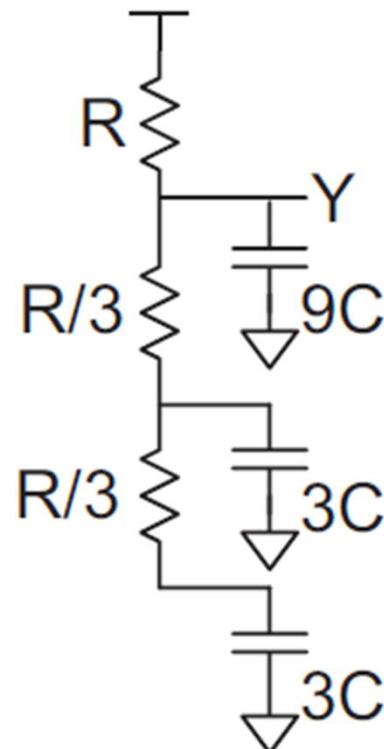


3-input NAND Delays

- Equivalent circuits for falling and rising transitions:



Falling

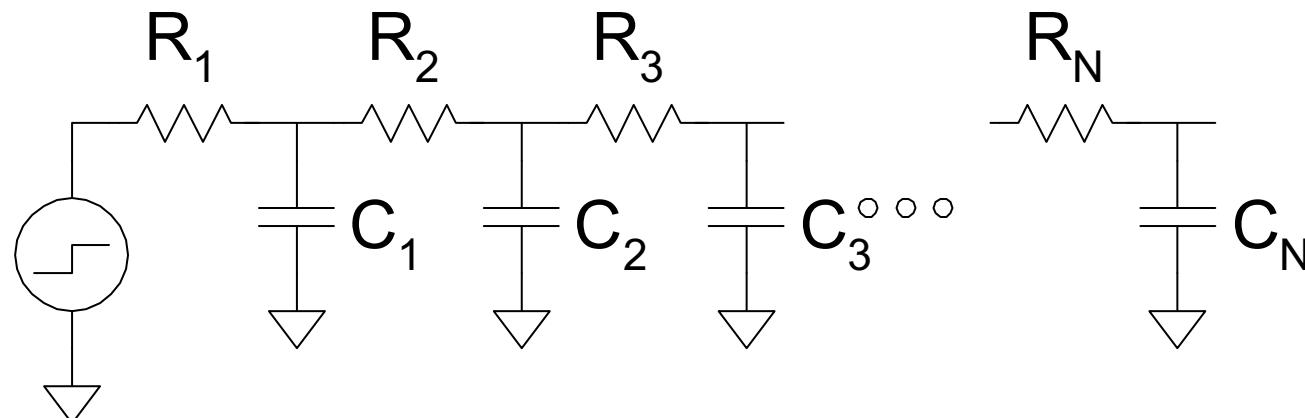


Rising

Elmore Delay

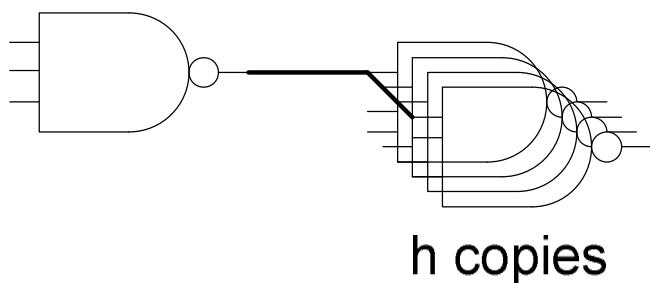
- ON transistors look like resistors
- Pullup or pulldown network modeled as *RC tree*
- Elmore delay of RC tree

$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-\text{to-source}} C_i$$
$$= R_1 C_1 + (R_1 + R_2) C_2 + \dots + (R_1 + R_2 + \dots + R_N) C_N$$

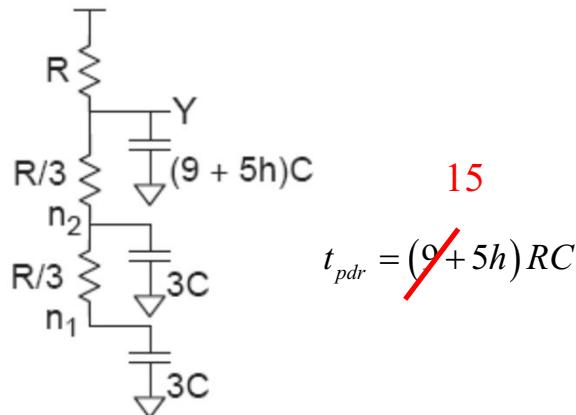
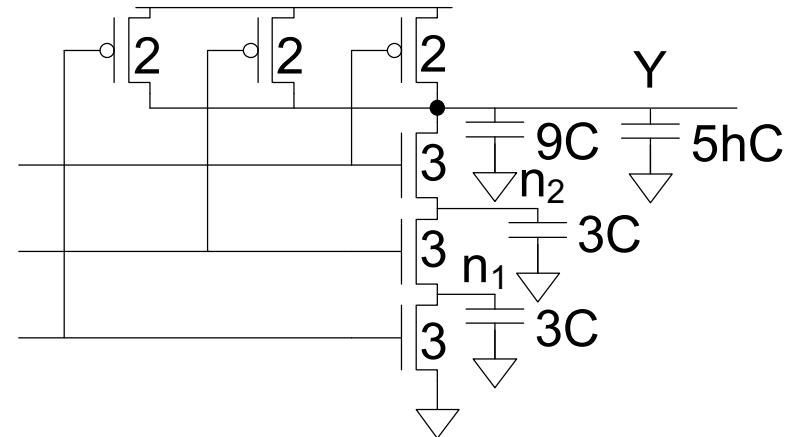


Example: 3-input NAND

- Estimate worst-case rising and falling delay of 3-input NAND driving h identical gates.

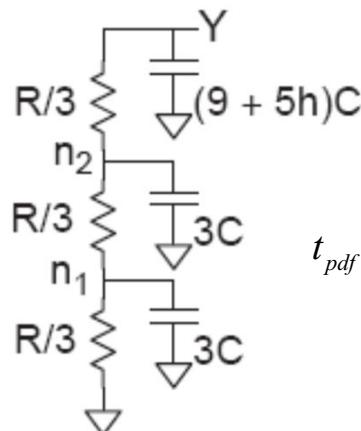


h copies



$$t_{pdr} = \cancel{(9+5h)}RC$$

15



$$\begin{aligned} t_{pdf} &= (3C)\left(\frac{R}{3}\right) + (3C)\left(\frac{R}{3} + \frac{R}{3}\right) + [(9+5h)C]\left(\frac{R}{3} + \frac{R}{3} + \frac{R}{3}\right) \\ &= (12 + 5h)RC \end{aligned}$$

Delay Components

- Delay has two parts
 - *Parasitic delay*
 - 15 or 12 RC
 - Independent of load
 - *Effort delay*
 - 5h RC
 - Proportional to load capacitance

Homeworks

- Chapter 4 exercise: 4.4
- Due date: 1402/9/7