In the name of god

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HW05

5.1 :

$$\begin{cases} \alpha = 0.1 \\ C_{switching} = 450 \ \frac{PF}{mm^2} \\ A = 70 \ mm^2 \ , \ f = 450 \ MHZ \ , \ V_{DD} = 0.9 \ V \end{cases}$$

Estimate the dynamic power consumption?

Because in question, there is nothing data for this part

for estimate $P_{dynamic}$ I know : $P_{dynamic} = P_{switching} + P_{short\ circuit}$

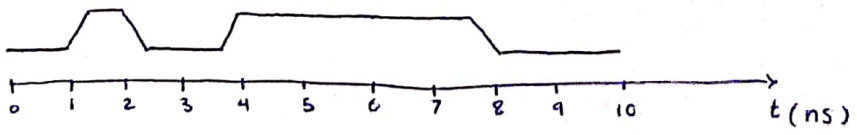
$\Rightarrow P_{dynamic} = P_{sw} = \alpha f C V_{DD}^2$

so first calculate total capacitance : $C_{total} = C_{sw} \times A = 450 \times 70$

$= 31500 \ PF$

$\Rightarrow P_{dynamic} = 0.1 \times 450^{MHZ} \times 31500^{PF} \times (0.9)^2 = 1148175 \ \mu W \simeq 1.15 \ W$

5.4 : for calculat Activity factor in this signal. we first counting the number of transitions in the signal during time Period.



This signal has changed 4 times in 10^{ns} so : $\alpha = \frac{\#\ transition}{Time\ Period \times clock\ rate}$

$$= \frac{4}{10 \times 10^{-9} \times 1 \times 10^{9}} = \frac{4}{10} = 0.4$$

5.7 :

Gate	P_Y
AND2	$P_A P_B$
AND3	$P_A P_B P_C$
OR2	$1 - \bar{P}_A \bar{P}_B$
NAND2	$1 - P_A P_B$
NOR2	$\bar{P}_A \bar{P}_B$
XOR2	$P_A \bar{P}_B + \bar{P}_A P_B$

In generally i know Activity factor is : $\alpha = P_i \bar{P}_i$

1) AND2 : The AND2 gate outputs a logical 1 only when both inputs are 1. therefore The probability of both inputs being 1 which is given by $P_Y = P(A) P(B)$

2) AND3 : Similary to AND2 : $P_Y = P_A P_B P_C$

3) OR2 : OR2 output a logical high when at last one of the inputs is high.
→ $P_Y = 1 - \bar{P}_A \bar{P}_B$

4) NAND2 : NAND2 outputs a logical 1 when at last one of ~~the~~ the inputs is 0 → $P_Y = 1 - P_A P_B$

5) NOR2 : NOR2 outputs a logical high only when both inputs are low → $P_Y = \bar{P}_A \bar{P}_B$

6) XOR2 : XOR2 outputs a logical 1 when the inputs have different Value (one high and one low) → $P_Y = P_A \bar{P}_B + \bar{P}_A P_B$

5.10 :

- PMOS transistor ON resistance = $2.5^{K\Omega} \cdot \mu m$
- Block ON current = 100^{mA}
- Desired increase in delay = 0.02

to calculate the wide of the header transistor, we can use the following equation

$$W = \left(\frac{\text{ON resistance}}{\text{Block ON current} \times \text{Delay Increase}} \right)^2 = \frac{(2.5^{K\Omega} \times 1 \mu m)^2}{(100^{mA} \times 0.02)^2}$$

$$= \frac{(2.5 \times 10^3 \mu m)^2}{(0.1^A \times 0.02)^2} = \boxed{1.25 \times 10^6 \mu m^2}$$