

Process Variations And Reliability

Outline

- Variation
 - Noise Budgets
 - Reliability
-

Variation

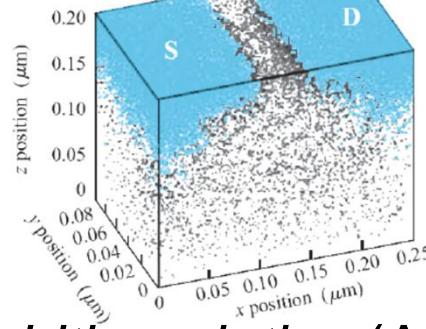
- ❑ Process
 - Threshold
 - Channel length
 - Interconnect dimensions
 - ❑ Environment
 - Voltage
 - Temperature
 - ❑ Aging/Wearout
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Process Variation

□ Threshold Voltage

- Depends on placement of dopants in channel
- Standard deviation inversely proportional to channel area

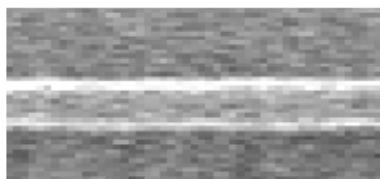
$$\sigma_{V_t} = \frac{t_{\text{ox}}}{\epsilon_{\text{ox}}} \frac{\sqrt[4]{q^3 \epsilon_{\text{si}} \phi_b N_a}}{\sqrt{2LW}} = \frac{A_{V_t}}{\sqrt{LW}}$$



[Bernstein06]

□ Channel Length

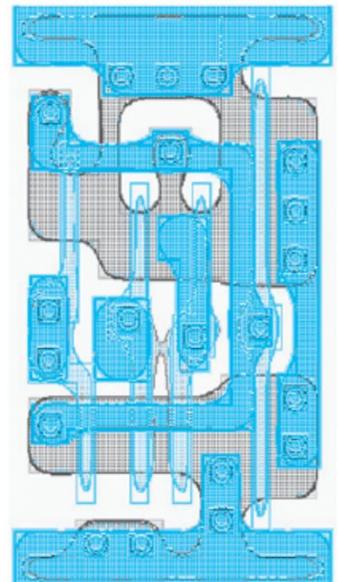
- Systematic *across-chip linewidth variation* (ACLV)
- Random line edge roughness (LER)



Courtesy Texas Instruments

□ Interconnect

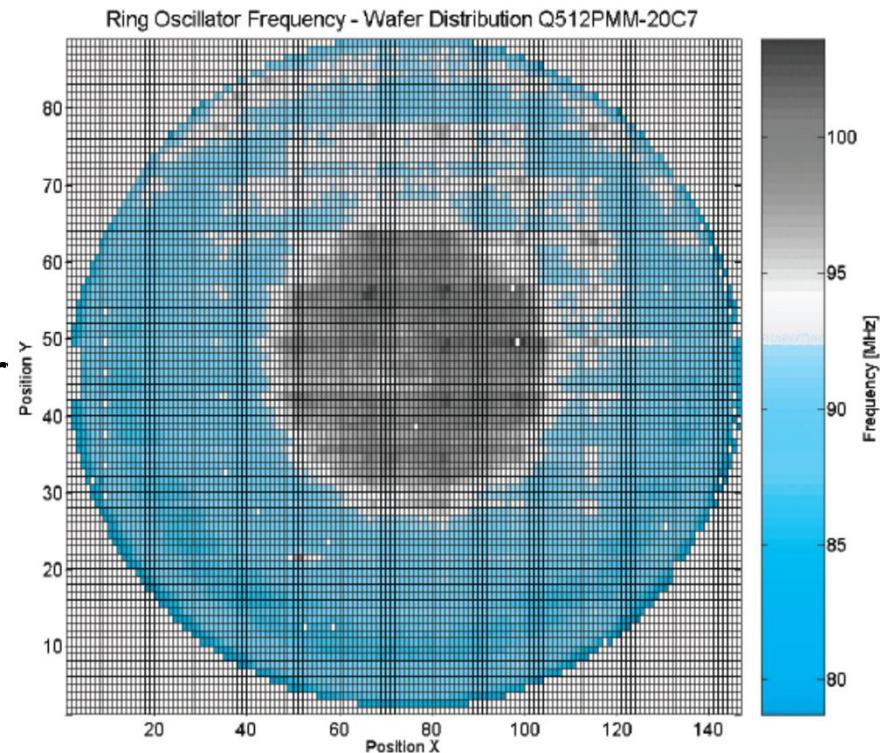
- Etching variations affect w, s, h



Courtesy Larry Pileggi

Spatial Distribution

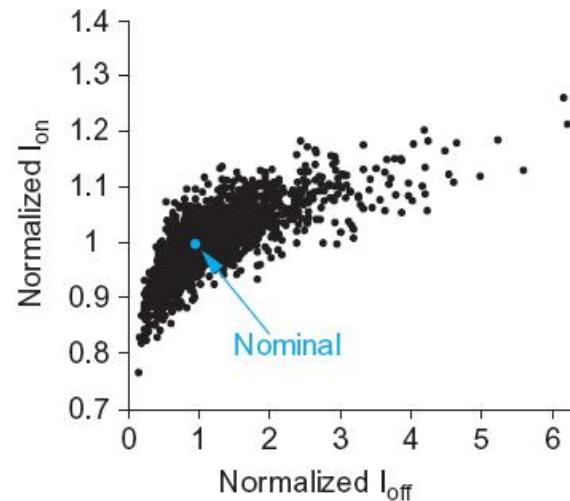
- Variations show spatial correlation
 - *Lot-to-lot* (L2L)
 - *Wafer-to-wafer* (W2W)
 - *Die-to-die* (D2D) / *inter-die*
 - *Within-die* (WID) / *intradie*
- Closer transistors match better



Courtesy M. Pelgrom

Monte Carlo Simulation

- As process variation increases, the worst-case corners become too pessimistic for practical design
- Monte Carlo: repeated simulations with parameters randomly varied each time
- Look at scatter plot of results to predict yield
- Ex: impact of V_t variation
 - ON-current
 - leakage



Noise

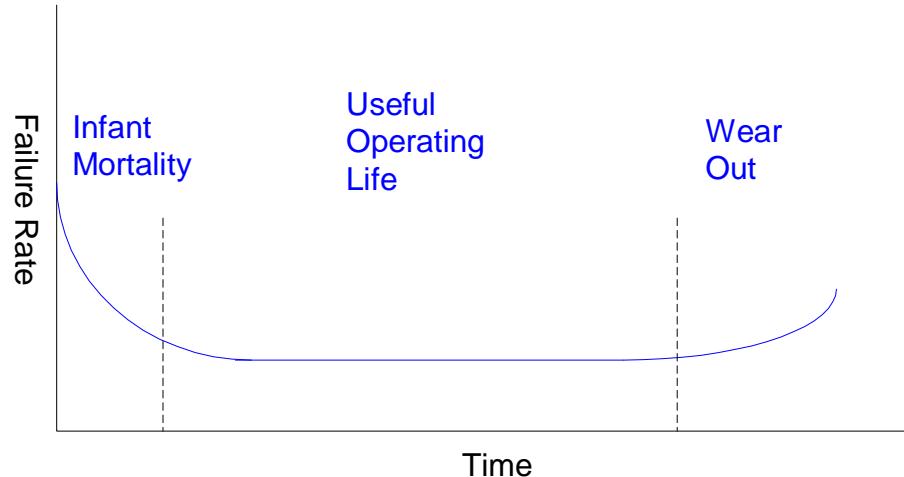
- Sources
 - Power supply noise / ground bounce
 - Capacitive coupling
 - Charge sharing
 - Leakage
 - Noise feedthrough
- Consequences
 - Increased delay (for noise to settle out)
 - Or incorrect computations

Aging

- ❑ Transistors change over time as they wear out
 - Hot carriers
 - Negative bias temperature instability
 - Time-dependent dielectric breakdown
- ❑ Causes threshold voltage changes
- ❑ More on this later ...

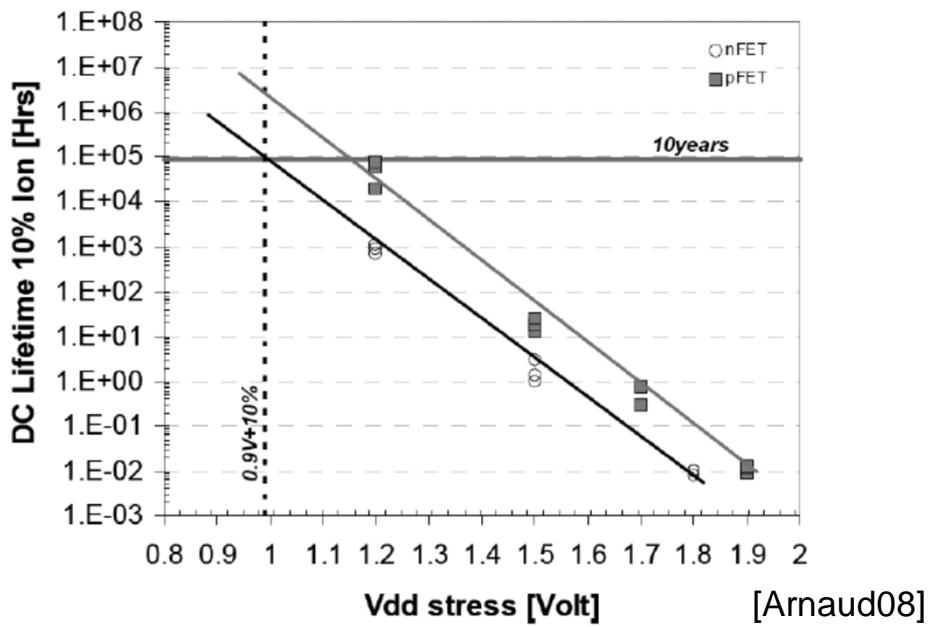
Reliability

- Hard Errors
 - Oxide wearout
 - Interconnect wearout
 - Overvoltage failure
 - Latchup
- Soft Errors
- Characterizing reliability
 - Mean time between failures (MTBF)
 - # of devices × hours of operation / number of failures
 - Failures in time (FIT)
 - # of failures / thousand hours / million devices



Accelerated Lifetime Testing

- ❑ Expected reliability typically exceeds 10 years
- ❑ But products come to market in 1-2 years
- ❑ Accelerated lifetime testing required to predict adequate long-term reliability



Effect of Aging on Oxide Layer

- ❑ Oxide undergoes wearout
- ❑ Three phenomena take place:
 - Hot carriers
 - NBTI
 - TDDB

Hot Carriers

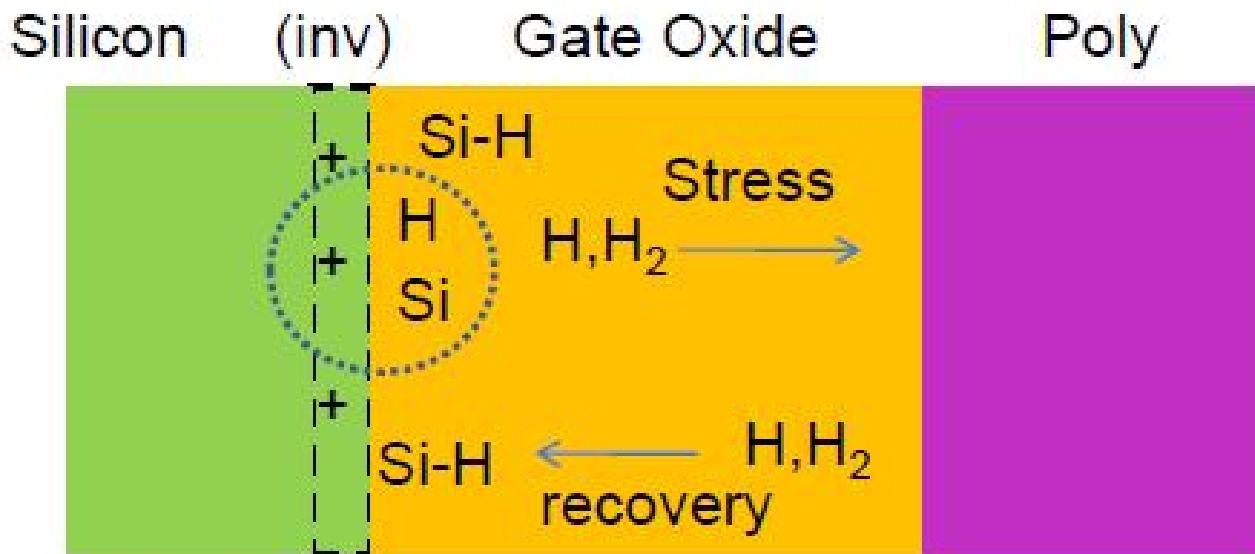
- ❑ Electric fields across channel impart high energies to some carriers (mostly electrons)
 - These “hot” carriers may be blasted into the gate oxide where they become trapped
 - Accumulation of charge in oxide damages it and changes the I-V characteristics over time
 - Eventually damage is too much for devices to operate correctly
 - ❑ Over a long time:
 - In NMOS drain current decreases, in PMOS drain current increases
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Hot Carriers (Cont.)

- ❑ The damage is more when V_{DS} is high (for NMOS)
- ❑ Worst cases when:
 - ❑ V_{DD} too high
 - ❑ gates have fast input rise time and heavy loads
- ❑ To mitigate:
 - ❑ Choose V_{DD} properly to achieve reasonable product lifetime
 - ❑ Set a limit on input rise time

NBTI

- ❑ *Negative Bias Temperature Instability*
- ❑ Electric field applied across oxide forms dangling bonds called traps at Si-SiO₂ interface
- ❑ Accumulation of traps causes V_t to increase



NBTI (Cont'd)

- Most pronounced for pMOS transistors with strong negative bias ($V_g = 0$, $V_s = V_{DD}$) at high temperature
- Most important wearout in deep submicron
- Traditional model:
 - Reaction-Diffusion
- Modern model:
 - Trapping-Detrapping

$$\Delta V_t = k e^{\frac{E_{ox}}{E_0} t^{0.25}} \quad E_{ox} = V_{DD}/t_{ox}$$

PBTI

- ❑ *Positive Bias Temperature Instability*
- ❑ Similar to NBTI but for NMOS

TDDB

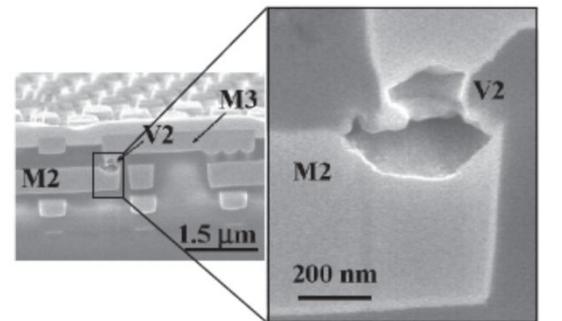
- ❑ *Time-Dependent Dielectric Breakdown*
 - Gradual increase in gate leakage when an electric field is applied across an oxide
 - Extra current called: *SILC (Stress-Induced Leakage Current)*
 - ❑ For 10-year life at 125 C, keep E_{ox} below ~0.7 V/nm
 - ❑ Underlying mechanisms not fully understood
 - ❑ To mitigate:
 - Reduce power supply voltage
 - Reduce power supply noise (fewer overshoots)
 - Use thicker oxides at I/O pads (b/c they experience more ringing and reflection)
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Interconnect Wearout

- Interconnect wearout happens in two forms:
 - Electromigration
 - Self-heating

Electromigration

- “Electron wind” causes movement of metal atoms along wires
- Excessive electromigration leads to open circuits
- Most significant for unidirectional (DC) current
 - Depends on the metal (Cu better than Al)
 - Depends on current density J_{dc} (current / area)
 - Exponential dependence on temperature
 - Black’s Equation: $MTTF \propto \frac{e^{\frac{E_a}{kT}}}{J_{dc}^n}$
 - E_a : activation energy (found experimentally), $n \sim 2$
 - Conservative limit (for Al): $J_{dc} < 1 - 2 \text{ mA} / \mu\text{m}^2$



[Christiansen06]

Self-Heating

- Current through wire resistance generates heat
 - Oxide surrounding wires is a thermal insulator
 - Heat tends to build up in wires
 - Hotter wires are more resistive, slower
- Self-heating limits AC current densities for reliability
- Conservative limit (for Al): $J_{rms} < 15 \text{ mA / } \mu\text{m}^2$

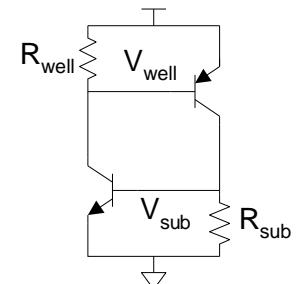
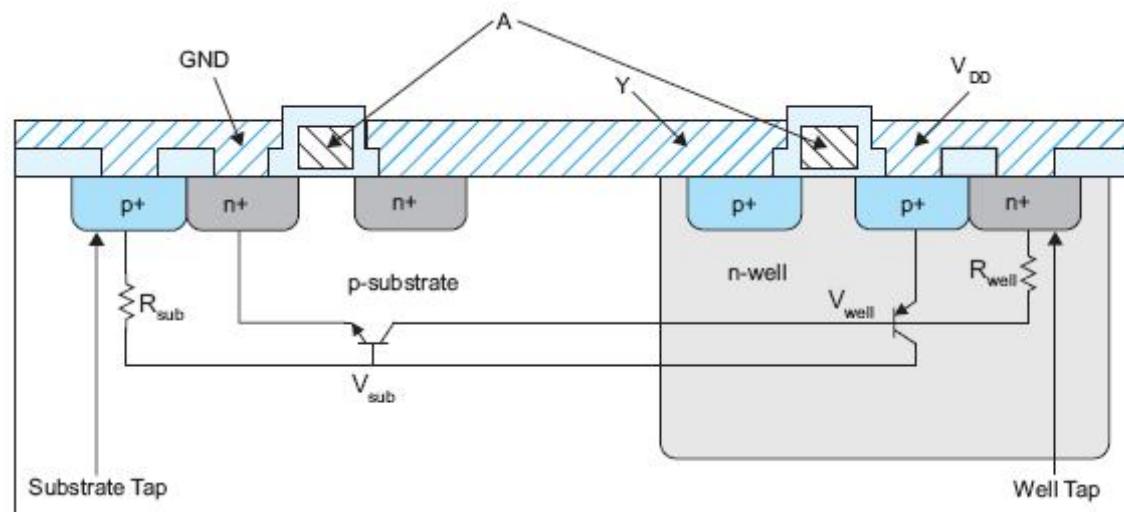
$$I_{rms} = \sqrt{\frac{\int_0^T I(t)^2 dt}{T}}$$

Overvoltage Failure

- High voltages can blow out tiny transistors
 - *Electrostatic discharge* (ESD)
 - kilovolts from static electricity when the package pins are handled
 - *Oxide breakdown*
 - In a 65 nm process, $V_g \approx 3$ V causes *arc*ing through thin gate oxides
 - *Punchthrough*
 - High V_{ds} causes depletion region between source and drain to touch, leading to high current flow and destructive overheating
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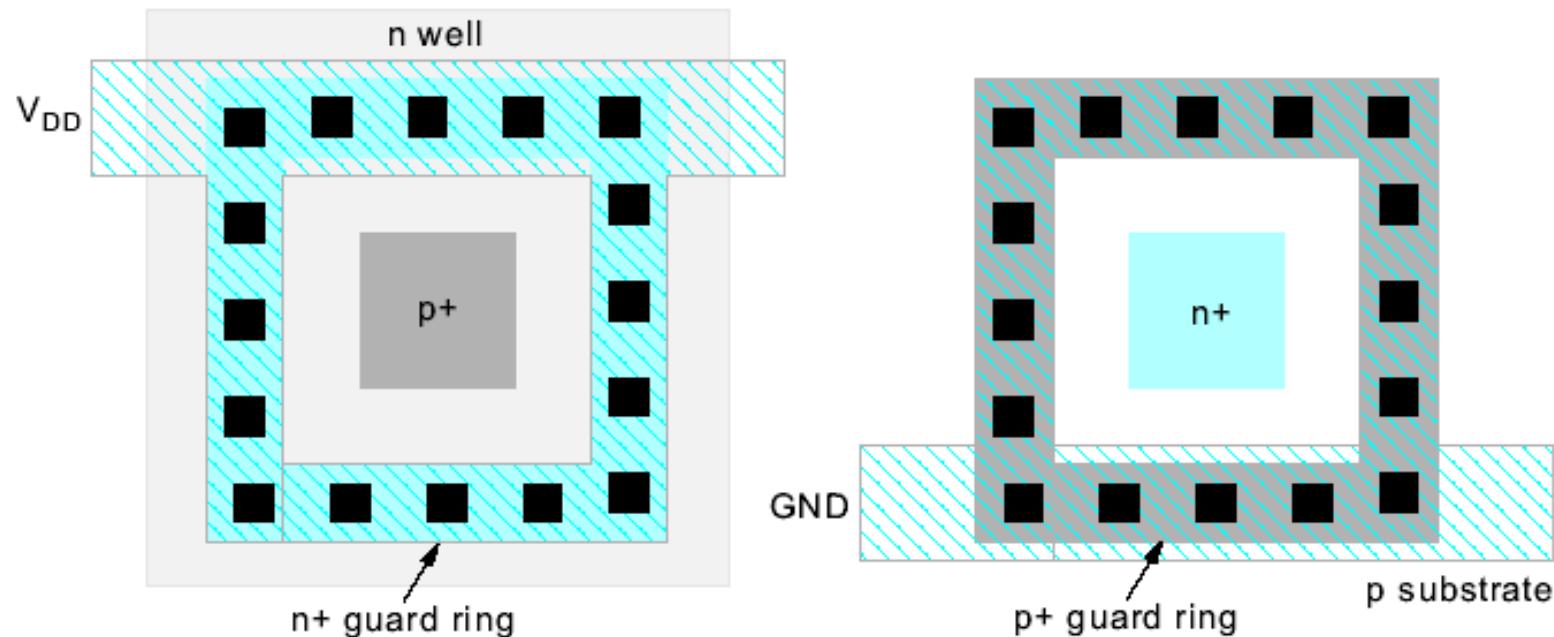
Latchup

- Latchup: positive feedback leading to V_{DD} – GND short
 - Major problem for 1970's CMOS processes before it was well understood
 - Forms a bistable (latch)
- Key factor: amount of R_{well} and R_{sub}



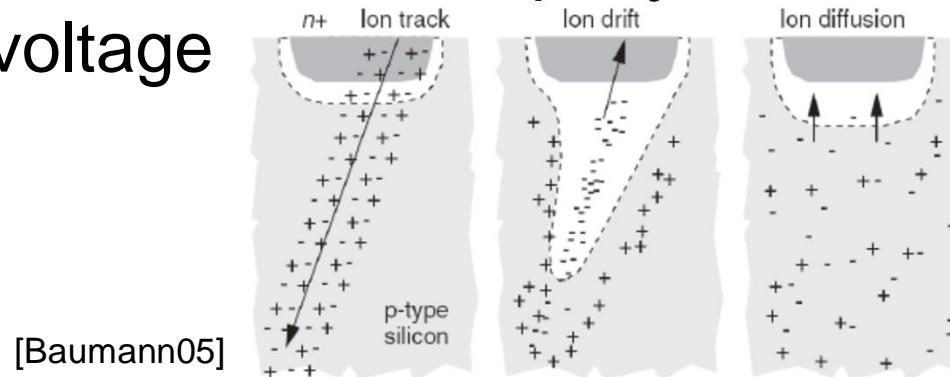
Guard Rings

- ❑ Avoid by minimizing resistance of body to GND / V_{DD}
 - Use plenty of substrate and well taps
- ❑ Surround sensitive regions with guard rings to minimize resistance



Soft Errors

- In 1970's, DRAMs were observed to randomly flip bits
 - Ultimately linked to alpha particles and cosmic ray neutrons
- Collisions with atoms create electron-hole pairs in substrate
 - These carriers are collected on p-n junctions, disturbing the voltage



Summary

- Setting aside the inherent non-ideal characteristics of the MOS transistors, there are still some other elements that create undesirable behavior
- Causes of undesirable behavior:
 - Limitations in the fabrication process makes the resulting chips unpredictable
 - The phenomenon is called “process variation”
 - Even if we start with “perfect” transistors, the device behavior varies over time
 - The phenomenon is called “wearout” or “aging”

Homeworks

- ❑ Chapter 7 problems: 7.2, 7.3, 7.6 for Sunday
(1402/9/28)
- ❑ Preannounced quiz for Sunday (1402/10/3)