

# Reza Adinepour

Department of Computer Engineering,  
Tehran Polytechnic,  
Tehran, Iran

Homepage: <https://rezaadinepour.github.io/>  
E-mails: [adinepour@aut.ac.ir](mailto:adinepour@aut.ac.ir)  
[r3zaadinepour@gmail.com](mailto:r3zaadinepour@gmail.com)

## RESEARCH INTERESTS

- ◇ AI Hardware Accelerators
- ◇ Real-time and Embedded Systems
- ◇ Reconfigurable Computing
- ◇ Neuromorphic Computing
- ◇ Parallel and Distributed Systems
- ◇ Cyber-Physical Systems (CPS)

## EDUCATION

- M.Sc. in Computer Engineering,** Sep. 2023 - Present  
**Amirkabir University of Technology (Tehran Polytechnic),** Tehran, Iran
- Thesis: “*FPGA-Based Hardware Acceleration of Remaining Useful Life Prediction of Rotating Machinery Using Transformer Neural Network*”
  - Advisor: [Prof. Morteza Saheb Zamani](#)
  - GPA: 3.4/4
- B.Sc. in Electrical Engineering,** Sep. 2019 - Jun. 2023  
**Shahrood University of Technology,** Shahrood, Iran
- Thesis: “*Design Real Time Face Recognition Systems Based on LBP Features on ODROID-XU4 Embedded Computer Board*”
  - Advisor: [Prof. Alireza Ahmadyfard](#)
  - GPA: 3.4/4








## PUBLICATIONS

- ◇ **Reza Adinepour**, Shayan Naghizadeh and Morteza Saheb Zamani. “*Edge Deployment of Quantized Transformer Models for Remaining Useful Life Prediction*” The 34th International Conference on Electrical Engineering ([ICEE 2026](#)). IEEE, 2026. (Under-Review)
- ◇ **Reza Adinepour** and Morteza Saheb Zamani. “*Real-Time RUL Prediction via a Persistent-Weight Dual-Kernel Transformer Accelerator on FPGA*” IEEE Transactions on Computers Journals, 2026. IEEE, 2026. (Under-Review)
- ◇ Shayan Naghizadeh, **Reza Adinepour** and Morteza Saheb Zamani. “*Low-Precision POSIT Arithmetic for Spiking Neural Networks with Kahan Summation*” The 11th International Conference on Signal Processing and Intelligent Systems ([ICSPIS 2025](#)). IEEE, 2025.

## RESEARCH COLLABORATIONS

- ◇ **FPGA-Based Hardware Acceleration of Vision Transformer (ViT)** Aug. 2024 - Jun. 2025  
**Research Assistant**, Supervisor: [Prof. Elif Bilge Kavun](#), Department of Computer Engineering, [Dresden University of Technology](#).
  - *Studies and research focused on **Vision Transformer hardware acceleration***  
I was conducting research on the implementation and acceleration of ViT on FPGA with the goal of Deep fake image generation.

## TEACHING EXPERIENCE

- Teaching Assistant**-Amirkabir University of Technology
- **Digital Electronics**  Fall 2025
  - **Embedded Systems Modeling & Design**  Spring 2025
  - **Digital Logic Design**  Fall 2024
- Invited Lecturer**-Amirkabir University of Technology
- **Operating System Lab**  Fall 2025
  - **Computer Architecture Lab**  Spring 2025
  - **Logic Circuits Lab**   Spring 2024 and Fall 2023
- Teaching Assistant**-Shahrood University of Technology
- **Digital Electronics** Spring 2023
  - **Signal and Systems** Spring 2023, Fall 2022, Spring 2022, Fall 2021
  - **Analog Electronic** Fall 2022
  - **Circuit Theory** Fall 2020, Spring 2020

HONORS AND AWARDS	<ul style="list-style-type: none"> <li>◇ <b>Direct Admission</b> of Master's Degree at <b>Amirkabir University of Technology (Tehran Polytechnic)</b></li> <li>◇ <b>Ranked 2<sup>nd</sup> (top 1%)</b> in Department of Electrical Engineering, Shahrood University of Technology, <b>Among More Than 120 Students.</b> 2023</li> </ul>	
NOTABLE PROJECTS	<ul style="list-style-type: none"> <li>◇ <b>High-Level to RTL Conversion Framework for CNN Acceleration</b> (In Progress)</li> <li>◇ <b>Secure and High-Performance Firmware Architecture Customization</b> (In Progress)</li> <li>◇ <b>FPGA Implementation of Logic Locking in Deep Neural Networks</b></li> <li>◇ <b>Research-Oriented SystemC Examples</b></li> <li>◇ <b>Algorithm Acceleration on HBM-PIM Architecture using PIMSimulator</b></li> <li>◇ <b>FPGA-Based Implementation of CNN Using High Level Synthesis (HLS)</b></li> <li>◇ <b>Edge Detector HW/SW Co-design on FPGA</b></li> <li>◇ <b>HLS-Based Implementation of Vision Transformer (ViT)</b></li> <li>◇ <b>FPGA-Based Implementation of Neural Network</b></li> </ul>	
WORK EXPERIENCE	<p><b>Member of Digital System Design Automation Laboratory</b> Aug. 2023 - Present Tehran, Iran <i>Job Description:</i> Research Assistant</p> <p><b>R&amp;D department Member, at D3H-Group</b> Jun. 2023 - Sep. 2023 Al Maryah Island, Abu Dhabi, UAE <i>Job Description:</i> Biomedical Signal Processing Developer</p> <p><b>R&amp;D department Member, at Radan Electronic StartUp</b> May. 2022 - Aug. 2022 Mashhad, Iran <i>Job Description:</i> Embedded Software Developer</p>	
SKILLS	<ul style="list-style-type: none"> <li>◇ <b>Programming Languages:</b> <ul style="list-style-type: none"> <li>◦ <b>Back-end:</b> C, C++, Rust, Java, Python, Matlab,</li> <li>◦ <b>HDLs:</b> VHDL, Verilog, HLS, SystemC, Nvidia CUDA, OpenMP</li> </ul> </li> <li>◇ <b>Machine Learning Tools:</b> PyTorch, TensorFlow, Keras, Scikit-learn, OpenCV, NumPy, Pandas</li> <li>◇ <b>Applications and Scientific Tools:</b> <ul style="list-style-type: none"> <li>◦ <b>FPGA/Embedded Systems Development:</b> Xilinx Vivado, Vitis HLS, Vitis AI, FINN, Xilinx ISE, ModelSim, IAR, Keil, CubeMX, Altium Designer, KiCad, Spice, Arduino IDE</li> <li>◦ <b>Cloud &amp; DevOps Engineering:</b> Git, GitLab, Docker</li> <li>◦ <b>Scientific Computing &amp; Research Tools:</b> MATLAB, Gem5</li> </ul> </li> <li>◇ <b>Operating Systems:</b> Linux, Microsoft Windows</li> <li>◇ <b>Typesetting:</b> T<sub>E</sub>X, L<sub>A</sub>T<sub>E</sub>X, VIM, Microsoft Word, Gnuplot</li> </ul>	
REFERENCES	<p><b>Prof. Morteza Saheb Zamani</b> Professor, Dept. of Computer Engineering Amirkabir University of Technology <b>Email:</b> <a href="mailto:szamani@aut.ac.ir">szamani@aut.ac.ir</a></p> <p><b>Prof. Hamid.R Zarandi</b> Associate Professor, Dept. of Computer Engineering Amirkabir University of Technology <b>Email:</b> <a href="mailto:h_zarandi@aut.ac.ir">h_zarandi@aut.ac.ir</a></p>	<p><b>Prof. Mehdi Sedighi</b> Professor, Dept. of Computer Engineering Amirkabir University of Technology <b>Email:</b> <a href="mailto:msedighi@aut.ac.ir">msedighi@aut.ac.ir</a></p> <p><b>Prof. Hamed Farbeh</b> Assistant Professor, Dept. of Computer Engineering Amirkabir University of Technology <b>Email:</b> <a href="mailto:farbeh@aut.ac.ir">farbeh@aut.ac.ir</a></p>