VETENSKAPSRÅDET
THE SWEDISH RESEARCH COUNCIL

Kansliets noteringar Kod	Dnr
2013-44981-102418-41	2013-5069

2013
Project Grant Junior Researchers

Area of science
Natural and Engineering Sciences
Announced grants
Research grants NT April 11, 2013
Total amount for which applied (kSEK)

2014	2015	2016	2017	2018
506	961	993	1046	531

APPLICANT

Name(Last name, First name)
Myréen, Magnus Oskar

Date of birth
830415-

Gender
Male

Email address
magnus.myreen@cl.cam.ac.uk

Academic title
PhD

Position
UK Royal Society University Research Fellow

Phone
+44 78 17913727

Doctoral degree awarded (yyyy-mm-dd)
2009-07-18

WORKING ADDRESS

University/corresponding, Department, Section/Unit, Address, etc.
University of Cambridge, UK
Computer Laboratory
Automated Reasoning Group
15 JJ Thomson Avenue, Cambridge
CB3 0FD Cambridgeshire, United Kingdom

ADMINISTRATING ORGANISATION

Administrating Organisation
Chalmers tekniska högskola

DESCRIPTIVE DATA

Project title, Swedish (max 200 char)
Verifikation av operativsystem - sista fasen

Project title, English (max 200 char)
Systems Verification - The Last Mile

Abstract (max 1500 char)
At the very base of every software system lies an operating system. In a recent landmark achievement, the L4.verified project from NICTA, demonstrated that it is possibly to prove strong safety and security properties of a general-purpose operating system [SOSP´09]. Like all other systems verification projects, they made a number of simplifying assumptions, e.g. the C compiler is trusted, inlined assembly is assumed to be correct and the boot code is right.

The proposed project will establish new approaches for the construction and verification of reliable systems software, which will allow future systems verification projects to avoid many of the current simplifying assumptions. The plan is to enable this by modelling the actual behaviour of computer hardware and providing proof methods which scale to the point where functional correctness of operating systems can be mathematically proven down to the level of machine code, not just C code. Ultimately, the aim is to have systems where every hardware peripheral has been specified and every single machine instruction is part of the verification.

In order to make sure that all reasoning strictly follows the rules of a formal logic, we will develop this work within the HOL4 theorem prover ? a readily programmable higher-order logic prover; and in order to ensure relevance and impact of this work, I will continue and deepen my collaboration with the high-profile L4.verified project.

VETENSKAPSRÅDET
THE SWEDISH RESEARCH COUNCIL

Kod
2013-44981-102418-41

Name of Applicant
Myréen, Magnus Oskar

Date of birth
830415-

Abstract language
English

Keywords
verifikation, formella metoder, operativsystem, maskinkod,

Research areas
*Nat-Tek generellt

Review panel
NT-2

Classification codes (SCB) in order of priority
10206, 10201,

Aspects
Ethical considerations are described in enclosed appendix A on page: n/a

Application is also submitted to

similar to: **identical to:**

ANIMAL STUDIES

Animal studies
No animal experiments

OTHER CO-WORKER

Name(Last name, First name) **University/corresponding, Department, Section/Unit, Addressetc.**
,

Date of birth **Gender**

Academic title **Doctoral degree awarded (yyyy-mm-dd)**

Name(Last name, First name) **University/corresponding, Department, Section/Unit, Addressetc.**
,

Date of birth **Gender**

Academic title **Doctoral degree awarded (yyyy-mm-dd)**

Name(Last name, First name) **University/corresponding, Department, Section/Unit, Addressetc.**
,

Date of birth **Gender**

Academic title **Doctoral degree awarded (yyyy-mm-dd)**

Name(Last name, First name) **University/corresponding, Department, Section/Unit, Addressetc.**
,

Date of birth **Gender**

Academic title **Doctoral degree awarded (yyyy-mm-dd)**

VETENSKAPSRÅDET
THE SWEDISH RESEARCH COUNCIL

Kod
2013-44981-102418-41

Name of Applicant
Myréen, Magnus Oskar

Date of birth
830415-

ENCLOSED APPENDICES

A, B, C, N, S

APPLIED FUNDING: THIS APPLICATION

Funding period (planned start and end date)
2014-07-01 -- 2018-06-30

Staff/ salaries (kSEK)

Main applicant	**% of full time in the project**	**2014**	**2015**	**2016**	**2017**	**2018**
Magnus Myreen	75	405	838	868	899	466
Other staff						
	Total, salaries (kSEK):	405	838	868	899	466

Other projectrelated costs (kSek)	**2014**	**2015**	**2016**	**2017**	**2018**
Premesis	26	54	55	57	30
Direct IT costs	5	9	10	10	5
Travel costs	30	60	60	60	30
Equipment costs	40			20	
Total, other costs (kSEK):	101	123	125	147	65

Total amount for which applied (kSEK)

2014	2015	2016	2017	2018
506	961	993	1046	531

ALL FUNDING

Other VR-projects (granted and applied) by the applicant and co-workers, if applic. (kSEK)

Funds received by the applicant from other funding sources, incl ALF-grant (kSEK)

POPULAR SCIENCE DESCRIPTION

Popularscience heading and description (max 4500 char)
RUBRIK:

Framtidens datorsystem blir pålitligare tack vare matematiska bevis om binär kod

BESKRIVNING:

Datorer är närvarande i varje aspekt av våra liv. De finns till exempel i kreditkort, mobiltelefoner, radioapparater, tvättmaskiner, medicinsk utrustning och olika delar av bilar, flygplan och byggnader. Dessa datorer kan ibland vara felaktigt programmerade och kanske inte alltid lyckas utföra de saker som de är avsedda att göra. Sådana fel kan orsaka irritation hos användarna och kan leda till förlust av tid, pengar eller data, eller tom. till fysiska skador. Man kan föreställa sig vad som kan hända om en dator som skall styra en insulinpump inte reagerar som förväntat [Reuters, 25/08/2011].

När datorsystem utvecklas skriver programmerare programvara på basis av intuition. De försöker hitta misstag i sina program genom att provköra programvaran på kända exempel. När systemen tas i bruk händer det tyvärr ibland att oväntade ingångsdata påträffas, vilket kan leda till fel.

För att vara säker på att datorsystem alltid fungerar korrekt måste man använda matematiska metoder

för att visa att de alltid ger korrekta resultat. Detta område inom datavetenskapen kallas formella metoder - ett område som har gjort stora framsteg på senaste tiden. Inom olika projekt har man nyligen kunnat visa att komplexa program, som t.ex. operativsystem, är tillförlitliga under lämpliga antaganden.

Formella metoder har hittills så gott som endast använts för att bevisa saker om programtexten som programmerarna skriver. Innan datorer kan köra programtext måste texten översättas till binär kod, dvs ettor och nollor som hårdvaran förstår. Översättningen från text till binär kod utförs av komplexa program som i sig själva kan vara defekta. För att uppnå den fulla potentialen av formella metoder bör bevis användas för binär kod. Min forskning behandlar denna fråga; jag skapar formella metoder som kan användas direkt på binär kod. Jag har visat att dessa tekniker kan användas även för komplicerad kod.

De flesta datorprogram läser data, sedan gör de beräkningar och när beräkningarna är färdiga skriver de ut resultaten. Att tillämpa formella metoder för inläsning och utskrivning av data är ett svårt problem - ett problem som är en viktig del av en "Grand Challenge" utmaning för formella metoder (J S. Moore, University of Texas). Detta problem är fortfarande i stort sett olöst.

Anledningen till denna svårighet ligger både i att utveckla realistiska modeller för hur datorer kommunicerar och praktiska tekniker för att bevisa att sådan binär kod är korrekt. På nivån av binär kod är kommunikationen knepig: data som skall läsas in kan användas sporadiskt och kommunikationen av resultaten kan kräva flera försök. Detta är ett problem som ännu inte har en tillfredsställande lösning för något nära till verklig binär kod.

Projektet har många matematiska och tekniska utmaningar men har potential att förverkliga en ambition: att möjligöra att formella metoder skall kunna tillämpas direkt på verkliga datorsystem vid nivån av binär kod för opertivsystem.

VETENSKAPSRÅDET
THE SWEDISH RESEARCH COUNCIL

Kod
þÿ2013 44981 102418

Name of applicant
Myréen, Magnus Oskar

Date of birth
þÿ830415

Title of research programme
þÿSystems Verification The Last Mile

Appendix A

Research programme

Vetenskapsrådet, Box 1035, SE-101 38 Stockholm, tel. +46 (0)8 546 44 000, vetenskapsradet@vr.se

Attachment A: Research Programme

Systems Verification — The Last Mile

Dr Magnus Myréen, University of Cambridge, UK

1. Purpose and aims

In a recent landmark achievement, the L4.verified project from NICTA, demonstrated that it is possibly to prove strong safety and security properties of a *general-purpose* operating system [SOSP'09]. Like all other systems verification projects, they made a number of simplifying assumptions, e.g. the C compiler is trusted, inlined assembly is assumed to be correct and the boot code is right.

The proposed project will establish new approaches for the construction and verification of reliable systems software, which will allow future systems verification projects to avoid many of the current simplifying assumptions. The plan is to enable this by modelling the actual behaviour of computer hardware and providing proof methods which scale to the point where functional correctness of operating systems can be mathematically proven down to the level of machine code, not just C code. Ultimately, the aim is to have systems where every hardware peripheral has been specified and every single machine instruction is part of the verification.

We aim to push for significant proof automation. For the most part, this automation intends to help with interactive verification. However, at the extreme end, this project will look into how component implementations that are 'correct-by-construction' can be automatically derived from specifications of the desired behaviour and models of the underlying hardware.

In order to make sure that all reasoning strictly follows the rules of a formal logic, we will develop this work within the HOL4 theorem prover — a readily programmable higher-order logic prover; and in order to ensure relevance and impact of this work, I will continue and deepen my collaboration with the high-profile L4.verified project.

2. Motivation

As computer-based systems become embedded in exotic locations — credit cards, phones, radios, washing machines, medical devices, and parts of cars, airplanes and buildings, etc. — we become reliant on them and, therefore, are increasingly in need of rigorous engineering methods that achieve robust computer systems.

At the very base of every software system lies an operating system. This provides the foundation for all other programs. The safety and security features of all software that runs on top of a the operating system are immediately compromised if the operating system is faulty. When operating systems fail, the entire computer becomes vulnerable as process isolation can break down, service can be disrupted, data can be lost, and intruders from outside might be able to hijack control.

As such key pieces of infrastructure, operating systems ought to be developed using proper engineering methods and be rigorously validated. The unfortunate reality is that operating systems and other systems software are developed based on only the intuition of systems programmers. The only validation that is done is testing, i.e. programs are run on sample inputs. Testing may suffice for certain programs, but is very difficult and unreliable to apply to systems software, since these interact very intimately with hardware, e.g. memory management units (MMUs), and certain faults only appear in complex configurations.

An emerging and increasingly relevant approach to gaining higher levels of assurance is the use of mathematical proof. This form of *formal verification* can be used to show that the software has its intended behaviour for all possible inputs, not just a finite set of test inputs. Formal verification and other techniques based on solid logical foundations (boolean algebra, model checking, SAT, BDDs, AIGs etc.) are currently used by all major hardware vendors, since, for them, the cost of a fault in the post silicon phase is so devastatingly high that they invest heavily in finding flaws early. Compared with software, formal verification of hardware is arguably easier to automate.

Formal verification for software has generally been perceived as only being applicable to toy languages and small programs, particularly if the properties to be proven are deep functional specifications. This myth is slowly being dispelled thanks to recent high profile projects that have shown that this is not the case. Most relevant to this proposal is the landmark achievement by the L4.verified project from NICTA [SOSP'09]. They demonstrated that it is possibly to use mathematical proof to show that a C implementation of a *general-purpose* operating system with *decent real-world performance* meets a high-level functional specification, and as a consequence satisfies a number of strong safety and security properties.

As a demonstration of what formal verification can achieve, the work of the L4.verified team is excellent; they successfully opened the eyes of many formal methods skeptics. However, the L4.verified project also did not go far enough. As with many other projects on operating systems verification (see **Survey of the field**), the L4.verified project make a number of simplifying assumptions. Systems verifications to date, with very few exceptions, all fall short of proving the actual binary code correct with respect to well-defined models of real hardware. Nearly all make simplifying assumptions about the underlying hardware, leave gaps in their proofs where hardware interaction occurs, and fail to prove the actual binary code which runs on the hardware.

Nearly all verification so far has targeted the programs as they are expressed in the implementation language, typically C, and thus completely ignore the fact that compilers and linkers can introduce faults. A consequence of sticking to the implementation language, usually C, is that it becomes very hard to give proper semantics to inlined assembly in the presence of the source language semantics and a compiler. No current operating systems verification assigns anything close to a proper semantics to the unavoidable inlined assembly.

Going below the level of C code necessitates actually modelling hardware and dealing with machine code, which is much more detailed than C code, requiring proof tools and modelling to scale much further.

The purpose of this project is to

- provide reusable, detailed and trustworthy specifications of common hardware peripherals, such as MMUs, timers, UARTs and non-volatile RAM,
- establish proof methods that can make reasoning about such hardware specifications manageable and scale well even in the presence of all the detail one encounters when reasoning about machine code, and
- complete a number of increasingly complex case studies that will be used to showcase the research advances made in the two points above.

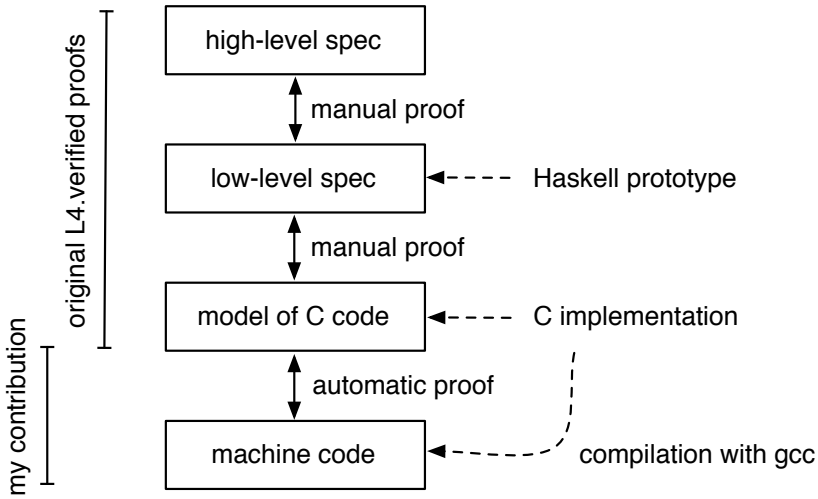
3. Preliminary results

The two most significant simplifying assumptions that project on systems verification make are that (i) the C compiler is correct w.r.t. the semantics used for verification, and (ii) the inlined assembly achieves the low-level state change (e.g. cache flush, MMU reconfiguration) that it is supposed to accomplish. It is very difficult, if not impossible, to give a proper semantics for inlined assembly as part of a C semantics. As a result, a prerequisite for tackling these assumptions is to move reasoning down to the machine code, where proofs target the generated machine code, not the source code.

Much of my previous work, including my on-going collaboration with the L4.verified project, centres around verification of machine-code programs. For this project I intend to use and extend my previously developed verification technology.

My work has so far targeted ARM, Intel x86 and IBM PowerPC processors. In particular, I have a proof-producing decompiler [FMCAD'08, PhD'09, FMCAD'12], which given some machine code for any of the processors mentioned above will automatically, via proof, derive a functional program from the machine code. This functional program is a record of the state change the machine code can perform. The beauty of this tool is that, for each decompilation, it produces a certificate theorem which allows all subsequent reasoning to be performed over the functional program, since the certificate theorem states that the generated functional program is an accurate record of all behaviours of the original machine code w.r.t. a formal semantics of the underlying machine language.

This tool has been successfully used in a number of case studies. The most relevant case study to this project is its use within the L4.verified project. During visits to the L4.verified team at NICTA, I have successfully applied my decompiler to the machine code that the latest version of the GNU C compiler (gcc -O2) produces for their verified operating system. Their original verification proof bottomed out at the level of a C implementation. With the aid of my decompiler, Thomas Sewell (of NICTA) and I managed to extend their entire proof down to the level of concrete ARM machine code and thus remove the assumption that the C compiler correctly compiles their kernel [PLDI'13]. The new structure of the L4.verified proofs is shown in the figure below.



Note that this extension of the L4.verified project's proofs did not discharge their assumption regarding inlined assembly. The inlined assembly has not yet been verified (at any of the levels), since they do not have a specification of a semantics for the hardware peripherals that these inlined assembly sections interact with. The proposed project will produce such semantics and can thus facilitate a further extension which would *complete* the bottom end of the L4.verified proofs.

The decompiler is a good tool for post hoc verification of existing machine code. However, often it is more desirable, if possible, to generate code that is correct by construction. For this purpose, I have also constructed system-building tools that can synthesise correct-by-construction machine code from high-level specifications [CC'09, ICFP'12]. These tools have enabled me to successfully produce functionally correct implementations of sizeable applications, such as implementation of functional programming languages [TPHOLs'09, ITP'11] and just-in-time compilers [POPL'10]. The two approaches, post hoc verification and synthesis, can be combined to provide local optimisations for code fragments whose execution speed is critical, e.g. in fast paths, inside the synthesised code.

4. Project description

Although my research has made significant contributions to verification of machine code, many challenges remain before full systems verification can be achieved. Being able to prove machine code is not in itself enough to tackle the detailed interaction between hardware and software that operating systems require, e.g. boot code which initializes the state, interrupt handlers which react to concurrent events, and code which processes I/O and deals with memory management via the hardware.

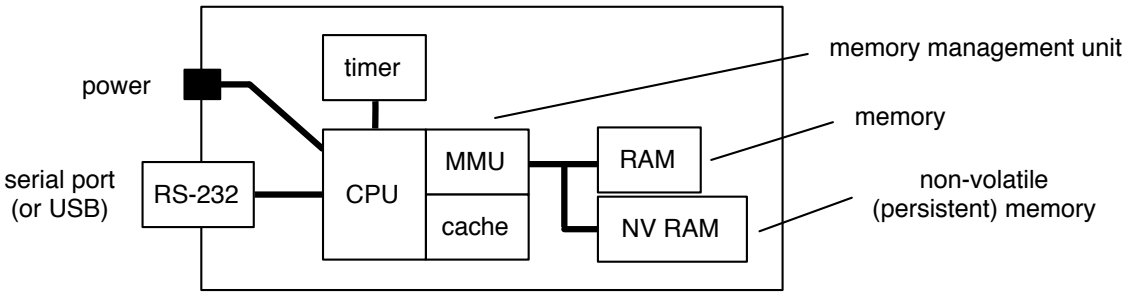
Full systems verification requires giving a semantics to the hardware components (interrupts, memory, MMUs, I/O devices) that such code communicates with. These new models will pose new challenges for proofs. New proof methods and automation will need to be devised that fits these more precise underlying hardware semantics.

The bulk of the effort is thus production of formal specifications for common hardware components and development of related proof methods. The research challenges will be

tackled in a step-by-step manner through a series of increasingly complex case studies. The case studies are designed to keep the project on track and also showcase its results.

4.1. Target case study

The final target case study is to run on hardware where all of the modelled hardware components exist. The following diagram sketches such a configuration.



This hardware diagram consists of all the basic components of a simple but complete system: the RS-232 port provides I/O, the CPU performs the computation, the timer can notify the CPU when time has come to perform a potential task switch, the MMU provides memory protection (helps isolate processes), the RAM together with the cache are the non-persistent memory and finally there is persistent memory that survives power off. The power component is included here in order to emphasise that this project will consider the possibility of sudden, potentially malicious, power cuts. Can such power cuts leave the persistent memory in a confused or vulnerable state?

This hardware configuration is an only slightly simplified version of real development boards such as the Raspberry Pi, the PandaBoard or the BeagleBoard. All of these are cheap ARM-based test boards that the author has experience in using.

The target is to model all of these hardware components and then to write and verify a small operating system that sits on top of such a hardware configuration. The example system that is being considered is to implement a cryptographic token, i.e. a device which holds a secret key and provides a cryptographic signature service: given some data to sign, it outputs a *hash* that is computed from both the input data and the secret key. For such systems we want to be able to prove that, if the verified machine code is installed, then the entire device exhibits only behaviours that respect a clean high-level functional specification of its allowed behaviours, even in the presence of erratic power on/off events that aim to confuse the state of the NV RAM.

This case study allows for gradual development: one can start with a nearly stateless version which just echos input over to output; such an echo device can then be extended to echo an encrypted version of the input; and the next version can make use of the persistent store and so forth. The most complex configuration allows user programs to run on the CPU and issue encryption requests to the operating system, which would protect the secret using memory protection provided by the MMU.

4.2. Approach

There are a number of challenges in completing the target case study. Here is my strategy for tackling these challenges:

Managing the details

Without care, the sheer volume of details in any formal proof of realistically modelled hardware is easily overwhelming. To make sure that no detail is dropped or overlooked, all reasoning will be carried out inside an interactive theorem prover [TPHOLs'08]. This ensures that all proofs follow from the primitive inferences of a formal logic. This project will use the HOL4 theorem prover as its higher-order logic provides convenient means of abstraction and its system is easily programmable.

Modelling the hardware

For the hardware modelling, the intention is to start from Fox's formalisation of the ARM instruction set architecture (ISA) and treat that as a model of the ARM CPU. Fox's latest model lives within a domain specific specification language, called L3 [ITP'12], which he is currently developing. By using L3 to model the hardware components, these can essentially be made into parts of the ARM inside L3. The benefits of using L3 are that it has a neat syntax which was designed to be able to look very similar to the data sheets found in hardware manuals; L3 also has a very good back-end for HOL4. It generates corresponding HOL4 definitions from L3 files and at the same time also sets up some basic automation that helps perform fast 'evaluation' of the models by logical inference in the prover.

A further challenge is to keep the hardware models generic enough. For example, each hardware board has its own version of an RS-232 port and each such port is conceptually near identical, but different in the names of pins, detail of protocols etc. To counter this, there will be generic specifications and instantiations of the generic specifications.

Dealing with concurrency

Efficient I/O, among other things, is typically done through interrupts. Interrupts introduce single-processor concurrency. My previous work on machine-code verification does not deal with concurrency. Fortunately, the concurrency found here is very asymmetric in nature. Interrupts jump (non-deterministically) into the system's interrupt handler and the handler *usually* turns off interrupts, deals with the interrupt and then returns while switching interrupt on again.

Such interrupts pose a challenge for code verification. The plan is to address this challenge by first verifying the interrupt handlers (assuming no interrupts happen since these are usually turned off) and then using a trick I call *folding in the verified specification into the hardware model*. The idea is that the user-mode code is to be verified in the presence of the hardware and the interrupt handler. Since the interrupt handler is verified, we know it has a specific behaviour and can treat its actions as just

executing its verified specification. In other words, the model which is used to for user-mode code assumes a hardware model consisting of the original hardware model with the specification of the interrupt handler superimposed. From the point of view of the user-mode code, interrupt do not happen, instead the extended hardware has a richer set of actions it can perform.

A worry here is the specification of spurious interrupts. Verification proofs must show that the system is resilient against some kinds of spurious interrupts.

Retaining proof automation

The previously developed proof automation, mentioned in Section 3, needs to carry over to the hardware-enhanced semantics of machine code. Conceptually there are two challenges to overcome here: concurrency from interrupts and non-determinism from the hardware. However, the addition of concurrency can be handled if the approach for folding the verified interrupt handling into the hardware model is followed. The real question is how genuine non-determinism is to be handled. My original approach to decompilation produces deterministic functions describing deterministic machine code. Such functions will not immediately suffice to describe all behaviours of non-deterministic machine code. One possible standard solution is to pass around an ‘oracle function’. Another solution is to modify the decompiler to produce relations instead of functions. The best alternative will become clear in the case studies.

Synthesis of special code

Having detailed models of the hardware opens up the possibility of synthesising efficient component implementations from models and behavioural requirements. This will be based on the synthesis tools described in Section 3. Examples that will be considered are synthesis of boot code that initializes the hardware into an appropriate state and simple interrupt handling routines that correctly identify the type of interrupt and act accordingly, e.g. just jump to the appropriate routine or perform some basic update to the global state and then return.

4.3. Time management

This is a four-year project where the work will be organised as follows. The focus of the first year will be modelling the interrupt-driven UART and NV RAM and developing solid proof technology to fit with these models. The second year is devoted to the MMU model and making the methods from the first year scale. The third and fourth years of the project will concentrate on completing the most advanced form of the target case study. Starting from year two onwards there will be a parallel thread of activity experimenting with the use of synthesis of code from specifications.

5. Survey of the field

The desire to have systems verification has been present since Goldstein and von Neumann [Neu'61]. However, the first significant systems verification project was the `CLI short stack' [JAR'89], an ambitious project which constructed a verified CPU,

verified compiler, verified systems software — i.e. a full verified stack. All artifacts were built to be verified and I/O was never satisfactorily addressed. Boyer and Yu [JAR'96] showed that it is possible to verify machine code of a real commercial processor w.r.t. a detailed formal semantics. They verified object code for the Motorola MC68020. Proof-carrying code (PCC) by Necula [POPL'97] and typed assembly language (TAL) by Morrisett et al. [POPL'98] renewed interest in verification of low-level code and new advances in dealing with low-level pointer reasoning have also been made [LICS'02].

All of these advances made it clear that the time is ripe for systems verification. A number of project on systems verification emerged, most notably, the aforementioned L4.verified project and the Verisoft and Verisoft XT projects [VSTTE'10]. The Verisoft projects have been a diverse mix of research on verified special-purpose operating systems and a hypervisor, all verified at the level of source code and without I/O. Like TAL and PCC, there have also been systems verifications that focus on safety properties, most notably, Yang and Hawblitzel's type safe operating system [PLDI'10]. New supporting technology such as programming logics for systems like code have been developed, e.g. by Shao's group at the University of Yale [PLDI'08]. Systems verification has yet to be based on detailed models of hardware and I/O devices.

6. Significance

As mentioned above, practically all projects on systems verification to date have made simplifying assumptions about the underlying hardware, leave gaps in their proofs where hardware interaction occurs, and fail to prove the actual binary code which runs on the hardware. My previous work on machine-code verification — which I have already demonstrated to be very effective in systems verification as part of the L4.verified project — promises to provide a very good basis for tackling these shortcomings.

There is a strong desire in current systems verification projects to do better, to have better hardware specifications and to fill the current gaps in their formal arguments. As such, the project proposed here is timely and has the potential to have an immediate impact with its outputs, i.e. the open source models and proof methods, finding use by others very quickly. The work described in this proposal is likely to be published at venues such as PLDI, POPL, ITP, CAV and FMCAD.

The core value of this project is that it is designed to make progress towards a long-standing ambition of the computer science community: to make formal methods applicable directly to real operating systems, running on real hardware as real machine code.

7. International and national collaboration

The NICTA collaboration will be continued and deepened in order to ensure relevance and impact of this work. Many people follow the high-profile verification group at NICTA. If that group picks up and start using the technology developed for this grant, then widespread dissemination is practically guaranteed.

Other international collaborations include a close working relationship with Dr Anthony Fox from the University of Cambridge. He is the author of the extensively validated Cambridge ARM model and the L3 toolchain which will be used as part of this project. Other work at Cambridge may also turn out to be relevant, e.g. that by Prof Mike Gordon on secure devices and Prof Peter Sewell's group on lightweight rigorous methods. Another international collaboration that is expected to have an impact on this project is my work with Dr Jared Davis of Centaur Technologies Inc and University of Texas Austin on implementation of the next generation of theorem provers.

On the national level, I am keen to establishing links with the functional programming group at Chalmers University. Their expertise in design and use of domain-specific languages may turn out to be a very useful in developing both extensions of the L3 specification language and a source language for use for synthesis of systems software. Another group which I intend to keep a close connection with is Prof Mads Dam and his PROSPER (Provably Secure Execution Platforms for Embedded Systems) project, which is developing a verified hypervisor in HOL4 using the Cambridge ARM model.

8. Other grants

I currently hold a Royal Society University Research Fellowship (UK). This research fellowship can unfortunately not be used outside of the UK and will be suspended if this VR grant is funded. I will move to Sweden, if this VR grant is funded.

9. References

PLDI'13: Thomas Sewell, Magnus O. Myreen and Gerwin Klein. Translation validation for a verified OS kernel. To appear in Cormac Flanagan, editor, Programming Language Design and Implementation (PLDI), ACM, 2013.

FMCAD'12: Magnus O. Myreen, Konrad Slind and Michael J. C. Gordon. Decompilation into Logic — Improved. In Gianpiero Cabodi, Satnam Singh, editors, Formal Methods in Computer-Aided Design (FMCAD), IEEE, 2012.

ICFP'12: Magnus O. Myreen and Scott Owens. Proof-producing synthesis of ML from higher-order logic. In Peter Thiemann, Robby Bruce Findler, editors, International Conference on Functional Programming (ICFP), ACM, 2012.

ITP'12: Anthony Fox. Directions in ISA specification. In Lennart Beringer, Amy P. Felty, editors, Interactive Theorem Proving (ITP), Springer, 2012.

ITP'11: Magnus O. Myreen and Jared Davis. A verified runtime for a verified theorem prover. In Marko C. J. D. van Eekelen, Herman Geuvers, Julien Schmaltz, Freek Wiedijk, editors, Interactive Theorem Proving (ITP), Springer, 2011.

POPL'10: Magnus O. Myreen. Verified just-in-time compiler on x86. In Manuel V. Hermenegildo, Jens Palsberg, editors, Principles of Programming Languages (POPL), ACM, 2010.

PLDI'10: Jean Yang and Chris Hawblitzel. Safe to the last instruction: automated verification of a type-safe operating system. In Benjamin G. Zorn and Alexander Aiken, editors, Programming Language Design and Implementation (PLDI), ACM, 2010.

VSTTE'10: Eyad Alkassar and Mark A. Hillebrand and Wolfgang J. Paul and Elena Petrova. Automated Verification of a Small Hypervisor. In Gary T. Leavens, Peter W. O'Hearn and Sriram K. Rajamani, editors, Verified Software: Theories, Tools, Experiments (VSTTE), Springer, 2010.

SOSP'09: Gerwin Klein, Kevin Elphinstone, Gernot Heiser, June,ronick, David Cock, Philip Derrin, Dhammika Elkaduwe, Kai Engelhardt, Rafal Kolanski, Michael Norrish, Thomas Sewell, Harvey Tuch and Simon Winwood. seL4: formal verification of an OS kernel. In Jeanna Neefe Matthews and Thomas E. Anderson, editors, Symposium on Operating Systems Principles (SOSP), ACM, 2009.

PhD'09: Magnus O. Myreen. Formal verification of machine-code programs. PhD dissertation, University of Cambridge, 2008.

CC'09: Magnus O. Myreen, Konrad Slind and Michael J. C. Gordon. Extensible proof-producing compilation. In Oege de Moor, Michael I. Schwartzbach, editors, Compiler Construction (CC), Springer, 2009.

TPHOLs'09: Magnus O. Myreen and Michael J. C. Gordon. Verified LISP implementations on ARM, x86 and PowerPC. In Stefan Berghofer, Tobias Nipkow, Christian Urban, Makarius Wenzel, editors, Theorem Proving in Higher-Order Logics (TPHOLs), Springer, 2009.

FMCAD'08: Magnus O. Myreen, Konrad Slind and Michael J. C. Gordon. Machine-code verification for multiple architectures – An application of decompilation into logic. In Alessandro Cimatti, Robert B. Jones, editors, Formal Methods in Computer-Aided Design (FMCAD), IEEE, 2008.

TPHOLs'08: Konrad Slind and Michael Norrish. A Brief Overview of HOL4. In Otmane Aat Mohamed, Cesar Munoz and Sofiene Tahar, editors, Theorem Proving in Higher Order Logics (TPHOLs), Springer, 2008.

PLDI'08: Xinyu Feng, Zhong Shao, Yuan Dong and Yu Guo. Certifying Low-Level Programs with Hardware Interrupts and Preemptive Threads. In Rajiv Gupta and Saman P. Amarasinghe, editors, Programming Language Design and Implementation (PLDI), ACM, 2008.

LICS'02: John Reynolds. Separation logic: A logic for shared mutable data structures. In Logic in Computer Science (LICS). IEEE Computer Society, 2002.

POPL'98: George C. Necula. From System F to Typed Assembly Language. In J. Gregory Morrisett, David Walker, Karl Crary and Neal Glew, editors, Principles of Programming Languages (POPL), ACM, 1998.

POPL'97: George C. Necula. Proof-Carrying Code. In Peter Lee, Fritz Henglein and Neil D. Jones, editors, Principles of Programming Languages (POPL), ACM, 1997.

JAR'96: Robert S. Boyer and Yuan Yu. Automated Proofs of Object Code for a Widely Used Microprocessor, 43(1), Springer, 1996.

JAR'89: W. R. Bevier, W. A. Hunt, J S. Moore, and W. D. Young. Special Issue on System Verification. Journal of Automated Reasoning 5(4), Springer, 1989.

Neu'61: Herman H. Goldstine and John von Neumann. Planning and coding problems for an electronic computing instrument. In John von Neumann, Collected Works, volume V. Pergamon Press, Oxford, 1961.

VETENSKAPSRÅDET
THE SWEDISH RESEARCH COUNCIL

Kod
2013-44981-102418-41

Name of applicant
Myréen, Magnus Oskar

Date of birth
830415-

Title of research programme
Systems Verification - The Last Mile

Appendix B

Curriculum vitae

Vetenskapsrådet, Box 1035, SE-101 38 Stockholm, tel. +46 (0)8 546 44 000, vetenskapsradet@vr.se

CV

Dr Magnus Myréen, University of Cambridge, UK
email: magnus.myreen@cl.cam.ac.uk web: http://www.cl.cam.ac.uk/~mom22/

1. Higher education degree

B.A. (Computer Science) – University of Oxford, UK — Oct 2002 – June 2005

- First-class Honours

2. Doctoral degree

PhD (Computer Science) – University of Cambridge, UK — Oct 2005 – July 2009

- Title: Formal verification of machine-code programs
- Awarded the British Computer Society's *Distinguished Dissertation Award 2010*
- The British Computer Society published my dissertation as a book in their *Distinguished Dissertation Award Series* (ISBN: 978-1906124816)

3. Postdoctoral positions

University of Cambridge, UK (Computer Laboratory) — Oct 2008 – Sep 2012

4. Docent level

5. Present position

UK Royal Society University Research Fellow — Oct 2012 – now
University of Cambridge, UK (Computer Laboratory)

- One of 36 fellowships awarded across all sciences for all UK universities (two fellowships awarded to computer scientists in 2012).

6. Previous positions and periods of appointment

University of Cambridge, UK (Computer Laboratory) — Oct 2008 – Sep 2012
Postdoctoral research associate

Åbo Akademi University, Finland — July – Sept in 2005 and 2004
Research assistant (Turku Centre for Computer Science)

7. Supervision

8. Deductible time

9. Additional information

9.1. International academic collaborations

National ICT of Australia (NICTA) — Jan – Feb 2011, Oct – Dec 2011, Dec 2012 – Feb 2013

- Visiting academic to work with the NICTA team on the L4.verified OS verification project where I successfully applied my methods to the code of their verified OS.
- Industry connection: the operating system produced by the L4.verified team is sold and distributed by Open Kernel Labs, Australia and USA.

9.2. Grants

UK Royal Society University Research Fellowship — Oct 2012 – Sep 2017

Ministry of Defence, UK — Apr 2012 – Sep 2012

- Constructing Verified Emulators Using HOL4

UK Engineering and Physical Sciences Research Council (EPSRC) — Oct 2008 – Mar 2012

- Trustworthy programming for multiple instruction sets
- I wrote the proposal and was Research Co-Investigator

9.3. Teaching

Lectures, University of Cambridge, UK

- *Functional Programming: Implementation, Specification and Verification (2013)*
  I'm currently preparing a new MPhil course for starting in Oct 2013. The course is partly based on my research on verified implementations of Lisp and ML.
- *Hoare Logic (2012)*
  When Prof. Mike Gordon was on sabbatical in the academic year 2012-2013, I lectured, set and marked exam papers for this final-year undergraduates course.
- *Foundations of Computer Science (2010)*
  When Prof. Larry Paulson was on sabbatical in the academic year 2010-2011, I lectured, set and marked exam papers for this first-year course on the theoretical concept of CS.

Classes, University of Cambridge, UK (Oct – Nov 2007)

- Gave two-hour classes for final-year undergraduates for *Specification and Verification I.*

Supervisions, University of Cambridge, UK (Jan 2007 – present)

- Supervised, in small groups, final-year undergraduates for *Optimising Compilers, Temporal Logic, Discrete Maths* and *Hoare Logic.*
- Have so far given more than 60 one-hour supervisions to more than 30 students.

9.4. Contact with industry

Department of Defense (DoD), USA, and Certicom, Canada

- The DoD has taken an interest in my work for a long time. They have funded some of my travel and invited me to present at their annual meeting, High Confidence Software Systems, in 2009, 2011 and 2012.
- In Nov 2007, the DoD funded a visit by me (accompanied by one of their staff scientists) to Ceritcom, a Canadian company specializing in cryptography, for them to assess how well my techniques apply in industry. Even back then my techniques were directly applicable to small hand written assembly programs that they produce.

Rockwell Collins, USA Dec 2008 – present

- Rockwell Collins develops high-assurance software for the defence and avionics industry.
- Since engineers from Rockwell Collins saw a presentation of mine at FMCAD'08, I have been in regular email contact on how they can best exploit my findings in their own verification processes.
- From 2011, engineers at Rockwell Collins have been working on an internal project based on techniques that I have developed during my PhD.

Broadcom, UK April 2010

- A subdivision of Broadcom, formerly known as Element 14, contacted me to find out whether my verification techniques could be used to automatically validate hand-optimised assembly code, which they produce. Initial experiments suggested that this was possible, but unfortunately we were unable to pursue this collaboration further due to disagreement over IP rights between the University of Cambridge and Broadcom.

9.5. Conferences and international profile

I have been contributing to more than 20 international conferences and meetings where I present my research, review papers, chair conference sessions and am active on programme committees. I have 24 publications, including papers at the prestigious POPL and PLDI conferences.

VETENSKAPSRÅDET
THE SWEDISH RESEARCH COUNCIL

Kod
þÿ 2 0 1 3 4 4 9 8 1 1 0 2 4 1 8

Name of applicant
Myréen, Magnus Oskar

Date of birth
þÿ 8 3 0 4 1 5

Title of research programme
þÿ S y s t e m s V e r i f i c a t i o n T h e L a s t M i l e

Appendix C

List of publications

Vetenskapsrådet, Box 1035, SE-101 38 Stockholm, tel. +46 (0)8 546 44 000, vetenskapsradet@vr.se

Publications

Dr Magnus Myréen, University of Cambridge, UK

In computer science, top-tier conferences are the primary outlet for research results and are considered more competitive than journals.

Publications most relevant to the proposed project are marked with an asterisk *.

1. Peer-reviewed articles (2 total)

Magnus O. Myreen and Michael J. C. Gordon. Function Extraction. In **Science of Computer Programming**, 77(4), Elsevier, 2010.

Peter Sewell, Susmit Sarkar, Scott Owens, Francesco Zappa Nardelli and **Magnus O. Myreen**. x86-TSO: A Rigorous and Usable Programmer's Model for x86 Multiprocessors. In **Comm. ACM**, 53(7), ACM, July 2010.

2. Peer-reviewed conference contributions (20 total)

* Thomas Sewell, **Magnus O. Myreen** and Gerwin Klein. Translation validation for a verified OS kernel. To appear in Cormac Flanagan, editor, Programming Language Design and Implementation (**PLDI**), ACM, 2013.

Magnus O. Myreen, Scott Owens and Ramana Kumar. Steps towards verified implementations of HOL Light. To appear in Sandrine Blazy, Christine Paulin-Mohring and David Pichardie, editors, Interactive Theorem Proving (**ITP**), Springer, 2013.

Magnus O. Myreen and Scott Owens. Proof-producing synthesis of ML from higher-order logic. In Peter Thiemann, Robby Bruce Findler, editors, International Conference on Functional Programming (**ICFP**), ACM, 2012.

* **Magnus O. Myreen**, Konrad Slind and Michael J. C. Gordon. Decompilation into Logic — Improved. In Gianpiero Cabodi, Satnam Singh, editors, Formal Methods in Computer-Aided Design (**FMCAD**), IEEE, 2012.

Magnus O. Myreen. Functional programs: conversions between deep and shallow embeddings. In Lennart Beringer, Amy P. Felty, editors, Interactive Theorem Proving (**ITP**), Springer, 2012.

* **Magnus O. Myreen** and Jared Davis. A verified runtime for a verified theorem prover. In Marko C. J. D. van Eekelen, Herman Geuvers, Julien Schmaltz, Freek Wiedijk, editors, Interactive Theorem Proving (**ITP**), Springer, 2011.

Magnus O. Myreen. Reusable verification of a copying collector. In Rajeev Joshi, Peter Müller, Andreas Podelski, editors, Verified Software: Theories, Tools and Experiments (**VSTTE**), Springer, 2010.

* Anthony Fox and **Magnus O. Myreen**. A Trustworthy Monadic Formalization of the ARMv7 Instruction Set Architecture. In Matt Kaufmann, Lawrence C. Paulson, editors, Interactive Theorem Proving (**ITP**), Springer, 2010.

Magnus O. Myreen. Separation logic adapted for proofs by rewriting. In Matt Kaufmann, Lawrence C. Paulson, editors, Interactive Theorem Proving (**ITP**), Springer, 2010.

* **Magnus O. Myreen**. Verified just-in-time compiler on x86. In Manuel V. Hermenegildo, Jens Palsberg, editors, Principles of Programming Languages (**POPL**), ACM, 2010.

Magnus O. Myreen and Michael J. C. Gordon. Verified LISP implementations on ARM, x86 and PowerPC. In Stefan Berghofer, Tobias Nipkow, Christian Urban, Makarius Wenzel, editors, Theorem Proving in Higher-Order Logics (**TPHOLs**), Springer, 2009.

Magnus O. Myreen, Konrad Slind and Michael J. C. Gordon. Extensible proof-producing compilation. In Oege de Moor, Michael I. Schwartzbach, editors, Compiler Construction (**CC**), Springer, 2009.

Susmit Sarkar, Peter Sewell, Francesco Zappa Nardelli, Scott Owens, Tom Ridge, Thomas Braibant, **Magnus O. Myreen**, Jade Alglave. The Semantics of x86-CC Multiprocessor Machine Code. In Zhong Shao, Benjamin C. Pierce, editors, Principles of Programming Languages (**POPL**), ACM, 2009.

Jade Alglave, Anthony C. J. Fox, Samin Ishtiaq, **Magnus O. Myreen**, Susmit Sarkar, Peter Sewell, Francesco Zappa Nardelli. The semantics of Power and ARM multiprocessor machine code. In Leaf Petersen, Manuel M. T. Chakravarty, editors, Declarative aspects of multicore programming (**DAMP**), ACM, 2009.

Magnus O. Myreen, Konrad Slind and Michael J. C. Gordon. Machine-code verification for multiple architectures – An application of decompilation into logic. In Alessandro Cimatti, Robert B. Jones, editors, Formal Methods in Computer-Aided Design (**FMCAD**), IEEE, 2008.

Magnus O. Myreen and Michael J. C. Gordon. Transforming Programs into Recursive Functions. In Patricia Machado, editors, the Brazilian Symposium on Formal Methods (**SBMF**), Springer, 2008.

Magnus O. Myreen and Michael J. C. Gordon. Hoare Logic for Realistically Modelled Machine Code. In Orna Grumberg, Michael Huth, editors, Tools and Algorithms for the Construction and Analysis of Systems (**TACAS**), Springer, 2007.

Magnus O. Myreen, Anthony C. J. Fox and Michael J. C. Gordon. Hoare Logic for ARM Machine Code. In Farhad Arbab, Marjan Sirjani, editors, Fundamentals of Software Engineering (**FSEN**), Springer, 2007.

Ralph-Johan Back, Johannes Eriksson and **Magnus Myreen**. Testing and Verifying Invariant Based Programs in the SOCOS Environment. In Yuri Gurevich, Bertrand Meyer, editors, Tests And Proofs (**TAP**), Springer, 2007.

Ralph-Johan Back and **Magnus Myreen**. Tool Support for Invariant Based Programming. In Jonathan Lee, Pankaj Jalote and William Cheng-Chung Chu, editors, Asia-Pacific Software Engineering Conference (**APSEC**), Springer, 2005.

3. Review articles, book chapters, books (2 total)

Magnus O. Myreen. Formal verification of machine-code programs, 2010. ISBN: 978-1906124816. This book was published by the **British Computer Society** (BCS) in their Distinguished Dissertation Award Series as a result of my PhD dissertation winning the BCS Distinguished Dissertation Award 2010.

Anthony C. J. Fox, Michael J. C. Gordon, and **Magnus O. Myreen**. Specification and verification of ARM hardware and software. A chapter in David S. Hardin, editor, **Design and Verification of Microprocessor Systems for High-Assurance Applications**, Springer, 2010.

4. Patents

None

5. Open access computer programs that you have developed

Since 2005, I have been an active developer of the HOL4 interactive theorem prover. This software is key to my research. HOL4 is a long-running open source project with a BSD-style licence. Its code is hosted on http://hol.sourceforge.net/ and https://github.com/mn200/HOL/.

6. Popular science articles/presentations

I contributed a **Don's diary** piece to Issue XXV of **The Journal of The Cambridge Computer Lab Ring**, Cambridge, September 2010. My piece describes what life is like as a researcher at an international conference, in this case the Federated Logic Conference (FLoC) 2010.

VETENSKAPSRÅDET
THE SWEDISH RESEARCH COUNCIL

Kod
þÿ 2 0 1 3 4 4 9 8 1 1 0 2 4 1 8

Name of applicant
Myréen, Magnus Oskar

Date of birth
þÿ 8 3 0 4 1 5

Title of research programme

Appendix N

Budget and research resources

Vetenskapsrådet, Box 1035, SE-101 38 Stockholm, tel. +46 (0)8 546 44 000, vetenskapsradet@vr.se

Justification of budget and research resources

Dr Magnus Myréen, University of Cambridge, UK

Salary

This grant is to pay 75 % of my salary (approximately 40k SEK per month). I am not currently employed by Chalmers University of Technology. However, if this grant is funded, then the Computer Science and Engineering Department of Chalmers University of Technology will employ me and pay the 25 % that remains.

Travel

I intend to publish in top-tier conferences and make other research visits. I therefore budget for three trips per year within Europe (two for conferences and one to collaborators in Cambridge UK) and one trip per year to North America. Target conferences such as PLDI, POPL, ITP, FMCAD and CAV are frequently held in North America.

Equipment

The research I propose will make extensive use of computer programs which mechanise theorem proving. These theorem proving programs will be applied to very large problems, i.e. computationally very intense tasks that require computer equipment with fast processors and unusually large RAM memory (at least 16 GB of RAM memory).

My research will create special-purpose operating systems for embedded computer-based systems. In order to test and validate these, I will require off-the-shelf hardware development boards, such as development boards by Olimex and Atmel.

Keeping in touch with the other researchers in my field and related fields is a high priority. I plan to attend international conferences and make other research visits. For this purpose, I need a laptop which is powerful enough for me to demonstrate my research software and from which I can give presentations.

Other costs

Financial administrators at Chalmers University of Technology provided me with the figures for their mandatory fees for use of premises and IT infrastructure.

Other grants

I currently hold a Royal Society University Research Fellowship (UK). This research fellowship can unfortunately not be used outside of the UK and will be suspended if this VR grant is funded.

VETENSKAPSRÅDET
THE SWEDISH RESEARCH COUNCIL

Kod
2013-44981-102418-41

Dnr
2013 -

Name of applicant
Myréen, Magnus Oskar

Date of birth
830415-

Reg date
2013-04-11 13:12:52

Project title
Systems Verification - The Last Mile

NT

Research grants NT April 11, 2013
Project Grant Junior Researchers
*Nat-Tek generellt
Chalmers tekniska högskola

NT-2

Appendix S

Signatures

2014	2015	2016	2017	2018	
506	961	993	1046	531	2014-07-01 -- 2018-06-30

Applicant | **Date**

Head of department at host University | **Clarifi cation of signature** | **Telephone**

A signature on the application is required not only from the applicant but also from the authorised representative of the administrating organisation/institution or equivalent (normally the head of the department or establishment where the research is to be conducted). The signature confirms that the department can accommodate the proposed research, position or equipment; that the costing in the application is approved for the department's part, that any proposed experimentation on human or animal subjects has been reported, and that the applicant has reported any secondary occupations and commercial ties (s)he may have, and nothing inconsistent with good research practice has thereby emerged. The applicant must have discussed these conditions with the representative of the administrating organisation/institution or equivalent before the latter approves and signs the application.

NOTE the exceptions!
Please note that a different procedure applies for the following types of grants:

- Infrastructure- Operation Grants
- Infrastructure- Grants for Expensive Equipment
- Infrastructure- Grants for Large Databases
- Framework Grant SIMSAM

For these types of grants the vice-chancellor, instead of the head of department, must sign Appendix S. Thereby (s)he confirms the commitments of the administrative organization. The details are specified in the Call for Proposals, published at www.vr.se.

Vetenskapsrådets noteringar
Kod

2013-44981-102418-41

Vetenskapsrådet, Box 1035, SE-101 38 Stockholm, tel. +46 (0)8 546 44 000, vetenskapsradet@vr.se