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THE SWEDISH RESEARCH COUNCIL

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2015	2016	2017	2018	2019
1210	1288	1408	1503	

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DESCRIPTIVE DATA

Project title, Swedish (max 200 char)
Förutsägbar QoS-/effektsamförvaltning i heterogena flerkärniga plattformar

Project title, English (max 200 char)
PQCOM: Predictive QoS-Power Co-Management in Heterogeneous Multicore Platforms

Abstract (max 1500 char)
Multicore chips are building blocks of embedded, mobile and data center systems. On these chips, multiple or many applications run simultaneously and share platform resources such as network-on-chip and memory bandwidth. Despite interferences resulting from sharing the resources among co-running applications, the multicore chip has to ensure a certain level of Quality-of-Service (QoS) for each application.

Current QoS frameworks suffer from two major drawbacks. One is lack of predictability. The performance isolation property can only be obtained a posterior after experiments. This invalidates these solutions for embedded real-time systems that require predictable performance certainty under any conditions. The other is lack of consideration of energy efficiency, even though energy efficiency has been the primary barrier for further advancing multicore performance.

Overcoming the drawbacks of the state-of-the-art, the PQCOM project aims at predictive QoS-power co-management in heterogeneous multicore platforms. It designs a novel QoS framework where resource and power budget are jointly allocated and controlled using a run-time characterized traffic model. With this model, performance and power/energy consumption can be mathematically analyzed to obtain foresight rather than experiment-based hindsight. Through collaborative resource-power allocation, it achieves multiple objectives in performance isolation, system throughput, energy efficiency and thermal balance.

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Aspects

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Application concerns: New grant
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ANIMAL STUDIES

Animal studies
No animal experiments

ENCLOSED APPENDICES

A, B, C, N, S

APPLIED FUNDING: THIS APPLICATION

Funding period (planned start and end date)
2015-01-01 -- 2018-12-31

Staff/ salaries (kSEK)

Main applicant	% of full time in the project	2015	2016	2017	2018	2019
Zhonghai Lu	30	284	296	308	320	
Other staff						
One PhD student	80	384	420	481	528	
Total, salaries (kSEK):		668	716	789	848	

Other project related costs (kSEK)	2015	2016	2017	2018	2019
Equipment and tool (computer and software)	60	60	60	60	
Conference and publication	50	50	50	50	
Premises	110	118	129	138	
Indirect cost	322	344	380	407	
Total, other costs (kSEK):	542	572	619	655	

Total amount for which applied (kSEK)

2015	2016	2017	2018	2019
1210	1288	1408	1503	

ALL FUNDING

Other VR-projects (granted and applied) by the applicant and co-workers, if applic. (kSEK)

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Funding source	Total	Proj.period	Applied 2015
Intel Corporation (Portland, USA)	168	2011-2013	

Project title
Formal QoS Analysis and Control for Network-on-Chip Communication

Applicant
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POPULAR SCIENCE DESCRIPTION

Popularscience heading and description (max 4500 char)

Flerkärniga chip är byggstenar för inbyggda, mobila och datacentriska datorsystem. På dessa chip, kör flera eller många applikationer samtidigt, som delar plattformresurser såsom network-on-chip och minnesbandbredd. Trots störningar till följd av att dela resurser mellan applikationer som kör samtidigt, måste det flerkärniga chippet garantera en viss kvalitetsnivå på Quality-of-Service (QoS) för varje applikation.

De aktuella QoS-ramarverken lider av två stora nackdelar. Den ena är bristen på förutsägbarhet. Egenskapen av prestandaisolering kan endast erhållas i efterhand genom experimentell utvärdering. Detta gör ogiltiga alla de lösningar för inbyggda realtidssystem som kräver förutsägbar prestandasäkerhet under alla förhållanden. Den andra är bristen på hänsyn till energieffektivitet, även om energieffektiviteten har varit det främsta hindret för att göra ytterligare framsteg i flerkärniga chips prestanda.

PRIME-projektet övervinner nackdelarna med de state-of-the-art lösningarna, genom att syfta på en förutsägbar resurseffekthantering i heterogena flerkärniga plattformar. Det utvecklar ett nytt QoS-ramverk där resurser och effektbudget gemensamt allokeras och styrs med hjälp av en run-time-karakteriserad trafikmodell. Med denna modell, kan prestanda och effekt-/energiförbrukningen matematiskt analyseras för att få ett förutseende snarare än experimentbaserad efterkloket. Genom samverkande resurs-effektallokering, uppnår det flera mål i prestandaisolering, systemthroughput, energieffektivitet och termisk balans.

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Title of research programme
PQCOM: Predictive QoS-Power Co-Management in Heterogeneous Multicore Platforms

Appendix A

Research programme

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Appendix A: Research Programme

PQCOM: Predictive QoS-Power Co-Management in Heterogeneous Multicore Platforms

Zhonghai Lu

KTH Royal Institute of Technology

1 Purpose and Aims

Energy efficiency has been recognized as a primary cross-cutting challenge in all embedded, mobile, and data center computing systems where the power constraints appear either in battery capacity, energy cost, or cooling limitation [1][2]. In response to the power roof challenge, multicore chips, the fundamental building block of these systems, are becoming increasingly parallel and radically heterogenous in core type, interconnect and on-chip memory. As a result, multicore computers enjoy consistently performance enhancement with a growing number of cores, and more and more applications can run simultaneously on them. This rapid development presents an urgent requirement in *application-level performance isolation* because it is obligatory to offer a certain level of Quality-of-Service (QoS) to each and every application.

While the type and number of cores assigned to each application can be controlled [3], the key challenge in performance isolation lies in managing platform resources such as network-on-chip (NoC) and main memory channels (bandwidth) shared across multiple or many applications. Current QoS frameworks have identified that the basic principle of providing performance isolation lies in allocating sufficient amount of resources to each application [3][4][5][6][7]. On top of this principle, dynamic re-allocation of excessive resources [4] and application differentiation techniques [8][9] are necessary to raise system throughput together with application-wise QoS assurance. However, the dynamic performance isolation quality and resource allocation efficiency of the state-of-the-art can only be obtained *a posterior* through *experimental* evaluation. Apparently the lack of predictable dynamic timing guarantees and countable resource utilization efficiency cannot satisfy requirements of embedded realtime applications. More unfortunately, current multicore QoS frameworks have not addressed energy efficiency, albeit its critical importance. As projected in [10], NoC power can reach the order of 64W with technology scaling on a 64-tile multicore chip. The combination of resource-power co-allocation is essential because, for example, a continuous heavy allocation of a particular network region may help to optimize QoS but result in gradually overheated hot spots.

The overall purpose of the PQCOM project is to develop a predictive QoS-power co-management framework in heterogenous multicore platforms. The framework has two salient characteristics: (1) *Predictive*, because it utilizes a predictive model that establishes a fundamental relation between performance requirement and resource/power requirement. With this model, the resource and power allocations become not only predictably accurate but also can be *mathematically* analyzed *a prior*. (2) *QoS-Power co-management*, because it combines resource allocation with power allocation in a coherent and collaborative way. As such, our framework overcomes the fundamental drawbacks of the state-of-the-art and achieves both performance predictive and energy smart.

PQCOM has specific aims from framework to analysis to evaluation. (1) Design a predictive QoS-power co-management framework for shared platform resources (NoC and main memory bandwidth) which allows to jointly optimize not only application QoS and system throughput but also energy and thermal efficiency; (2) Develop mathematical analysis techniques for performance and power to understand the application-level performance and theoretical potentials in power/energy efficiency under QoS constraints and targets for a set of co-running applications;

(3) Implement and evaluate the framework to investigate how much the theoretical limits can be approached under practical conditions with associated overheads.

2 Survey of the Field

2.1 The Application-Level Multicore QoS Problem

Quality-of-Service (QoS) is a term from the telephony and computer network, referring to the overall performance of a network, particulary, the performance seen by the users of the network. Because it concerns application-level performance and user experience, it was recently borrowed to express the performance isolation property of multi-core or many-core chips which run multiple or many applications at the same time. While the number and type of cores assigned to each workload or application can be controlled [3], the problem is centered on shared resource management because the performance of a particular application is no longer only a function of its own behavior but also co-running applications as a result of competing for accessing shared resources such as shared caches/scratch pads, NoC, and main memory bandwidth etc.

The requirement on performance isolation advances quickly in both application-specific and general-purpose computing domains. It is common that today's MPSoCs run multiple applications. For example, TI details portable consumer devices that usually contain image, video, audio processing capabilities [11]. These possibly co-running applications require often realtime performance guarantees to satisfy acceptable quality with stringent power and cost budgets. The trend is that a growing number of heterogenous applications will have to run on the same die with the growing number of heterogenous cores. For CMPs, as noted by HP Labs, the current trend in enterprise IT highlights a diversity of workloads and usage patterns in the emerging large consolidated data centers and virtualized computing clouds [12]. The service-oriented and utility computing infrastructure has to emphasize service-level agreement driven performance tuning.

2.2 Digest of State-of-the-Art Multicore QoS Provision

One fundamental principle in offering application-level QoS is *resource demand-supply matching*, i.e., provide each application an appropriate amount or portion of the shared resources according to each application's demand. Because there are multiple applications, the shared resources need to be divided into physical or logical *partitions* which are then assigned to the applications. In this way, each application executes as if running on its own virtual machine with exclusive resources, and thus its performance can be promised. The concept of partitioning applies to all computing and communicating resources such as cores, caches, NoC, and main memory bandwidth. For example, in [3], the multi-core system is partitioned as virtual private machines, each of which includes partitioned core(s), a slice of cache space and a portion of main memory bandwidth. Not only spatial partitioning, shared resources can be temporally partitioned and allocated on time slot basis. For instance, in [5], the guaranteed-service NoC hosts globally synchronized time frames to accept a limited quota of traffic at each frame. In Æthereal NoC, channel bandwidth and main memory (through DRAM controller) can be statically co-reserved end-to-end along the packet communication path in a contention-free TDM fashion [7]. Furthermore, because applications may be of different granularity, resource partitioning can be hierarchical and recursive.

Although the principle of resource demand-supply matching is conceptually simple to function, it often requires *dynamic resource re-allocation* mechanisms to deal with practical resource over-provisioning and under-provisioning situations. Because an application has usually dynamic execution phases, its demand on resources may vary over time. Such dynamic demand creates two situations: *under-load* state and *over-load* state. While the former results in allocated resources under-utilized, the latter leads to allocated resources temporally insufficient to guarantee the performance. In [4], the excessive resources can be stolen (re-allocated) by other jobs to optimize system throughput, while an admission control was incorporated to accept jobs only when their QoS targets can be met. Such dynamic adjustments are meaningful because different applications' QoS requirements may differ in strictness and thus such QoS requirement elasticity can be exploited. In networks, rate-proportional channel bandwidth allocation techniques can achieve logically isolated bandwidth partitions while allowing dynamic re-allocation of un-used bandwidth

[13]. Recently a preemptive virtual clock technique, a variant of virtual clock [13] using preemption to avoid starvation, was proposed to ensure performance isolation in NoCs [6].

QoS provisioning cannot be satisfactory in both per-application QoS target and system-wide performance goals if *application heterogeneity* is not exploited to offer heterogenous treatment to heterogenous applications. Application heterogeneity comes in various forms, not only in QoS target elasticity but also in detailed access patterns and frequencies to shared resources (e.g. compute-bound or memory-bound). For example, some applications may incur non-proportional load/store memory accesses where load instructions are generally more critical to performance. Some applications generating less memory transactions can be more sensitive to memory access stall times than those generating more memory transactions [9]. As a result, the shared NoC should not treat all packets with equal priority. Rather *service specialization* and *prioritization mechanisms* [8] need to be incorporated to opportunistically explore the heterogeneity in raising system throughput without compromising per-application QoS. By priority, shared resources are accessed via run-time arbitration rather than reservation, archiving higher resource utilization and suiting for excessive resource (unallocated or allocated but not used) allocation.

2.3 Our Vision on the Multicore QoS Research

As described above, we can see that the general demand-supply matching principle for allocating shared resources is established to satisfy QoS requirements of multiple co-running applications, and sophisticated resource re-allocation and service differentiation techniques have further been developed to enhance system utilization. While the achievements are high, we consider the current *dynamic* QoS frameworks somewhat *ad hoc* because of lacking formal QoS analysis, e.g., analyze network performance guarantees in backlog, delay and throughput under any conditions without or prior to experiments. Consequently their performance evaluations have to rely on empirical results which are only obtained *a posterior*. The TDM NoC [7] can *statically* ensure predictable per-application QoS but it cannot satisfy the system-level goal in utilization efficiency under dynamic scenarios, and it is therefore very limited in applicability. Apparently embedded multicore systems are hard to embrace such methods because satisfying hard/firm/soft realtime constraints must be predictably satisfied (rather than empirically satisfied) with cost efficiency.

More severely, existing multicore QoS frameworks have not integrated energy efficiency as their first-level concern. Consequently they may result in good QoS certainty but bad in power consumption, eventually hurting on-chip thermal and temperature constraints. For example, when a gather traffic pattern (like all-to-one traffic to a shared memory) creates a hot spot region in the network, the routers in the region can adaptively switch to a turbo mode, increasing frequency to accelerate sinking packets for QoS assurance, according to the frequency tuning technique in [14]. However, increasing frequency increases power, which directly translates into heat, leading to possibly overheated chip area. If this automatic frequency tuning continues, the ”hot” region may even burn the chip. Note that power management for NoC-based multicores have been studied *separately* for *single applications* (without the QoS notion) [14][15]. In [14], the NoC allows per-router Voltage/Frequency (V/F) adaption to enable fine-grain power and congestion comanagement. It uses a distributed V/F control scheme by monitoring and passing per-router buffer utilization to upstream routers which adjust V/F scales according to empirical thresholds. In [15], the entire NoC is treated as a single V/F island to offer simpler coarse-grain power management. A centralized PID controller is used to dynamically adjust the V/F scale according to injected network traffic so as to minimize energy consumption under application performance (e.g. completion time) constraints.

The reason for lacking formal analysis originates from missing a proper predictive traffic model which can map application performance requirement to resource/power requirement accurately and continuously at runtime. Such a model should ideally also enable to analyze performance guarantees using mathematical analysis. Furthermore, it is essential to combine resource management with power management in a collaborative way to achieve efficiency in multiple goals (not only two goals): performance isolation and system utilization plus system power/energy consumption and thermal/temperature management. These constitute strong motivations for PQCOM.

3 Project Description

3.1 Foundation and Overview of PQCOM

PQCOM studies two shared platform resources: NoC (buffers in routers and physical channels) and main memory channels (bandwidth). The resource allocation is performed at the *flow* level, where flow refers to a unicast packet stream sent from a source to a destination. It can be either memory request/reply between a core and a main memory or coherency request/reply traffic among shared last level caches. Let T be a time interval called *epoch*, flow has a four-parameter model $(I,A(T),b(T),r(T))$ where I represents a fixed flow identifier (ID), $A(T)$ a flow criticality level, $b(T)$ burst tolerance in bits, and $r(T)$ average rate in bits/second. The four parameters are used by a conceptual Resource Manager (RM) to allocate shared network and memory bandwidth resources and Power Manager (PM) to configure V/F islands of the network. The first two parameters can be used to provide differentiated services by the network and memory controller to flows, similarly to [4][9][8]. The key benefits come from the last two parameters, (b,r), which enable to nicely achieve PQCOM's objectives.

- The (b,r) model maps flow's performance requirement to required exact channel/memory bandwidth, which is equal to r, and minimum buffer size b. Any reserved bandwidth greater than r less than capacity would be valid.
- The (b,r) model maps flow's performance requirement r to required exact dynamic power consumption P_r of hardware circuits and channel wires. Based on the transistor speed-power (F-P_F) equation, the formula can be written by replacing F with rate r ($r \leq F$) as follows:

$$P_r = \alpha \cdot r \cdot C \cdot V(r)^2. \tag{1}$$

  where α represents switching probability, C switched capacitance, and $V(r)$ rate-sensitive power supply voltage. This formula establishes a fundamental relation between logic/channel operating rate and consumed dynamic power. It directly gives the permissible V/F adjustment range $[r,F]$ and possible dynamic power savings $\Delta P = P_F - P_r$.
- The (b,r) model is indeed the traffic linear arrival model of *Network Calculus* [16][17][18], which makes worst-case delay, backlog and throughput bounds mathematically analyzable by applying the theory (See Section 3.3 Phase 2).

With the above formal foundation established, PQCOM is proposed for four years with three *overlapping phases*. Phase 1 designs a predictive QoS-power co-management framework, focusing on key scientific innovations. Phase 2 conducts performance and energy analysis, tackling fundamental questions. Phase 3 implements and evaluates the co-management framework. Considering the workloads of the tasks and their inter-dependency, we plan Phase 1 from Month 1 to Month 36 (36 months), Phase 2 from Month 13 to Month 48 (36 months), and Phase 3 from M1 to M48 (48 months). In the following, we elaborate the three phases in sequence.

3.2 Phase 1: Predictive QoS-Power Co-Management Framework

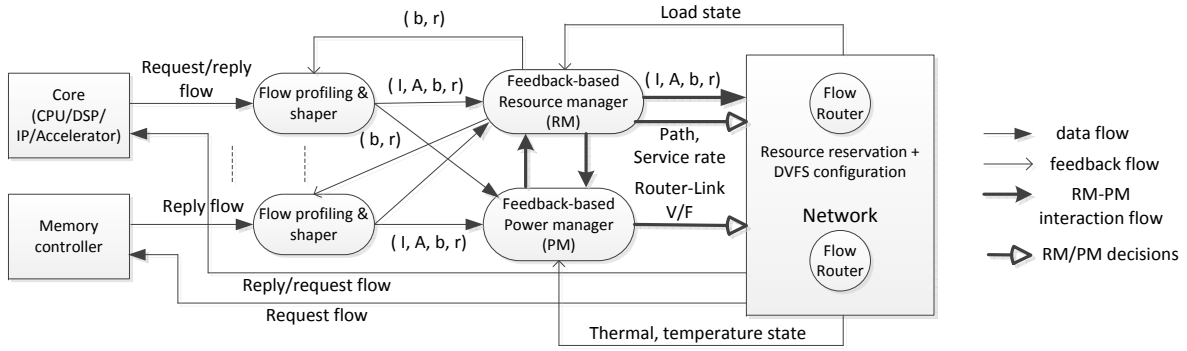

Figure 1: The PQCOM framework

Figure 1 sketches the framework comprising four major components: (1) Input flow profiling and shaping; (2) Network resource reservation and DVFS configuration; (3) Feedback-based resource manager (RM); (4) Feedback-based power manger (PM). While (1) produces characterized traffic in the predictive form (I,A,b,r) to the network, (2) implements the resource allocation and power management decisions made by (3) and (4), respectively. Note that RM and PM may be implemented in a centralized or distributed way (See implementation discussions in Section 3.4 Phase 3).

The flow shaper regulates online traffic injection based on the input traffic profile and the network load state (through RM). While the input traffic characteristics can be arbitrary, the output flow of the shaper always conforms to the (b,r) model using the leaky-bucket control, as done in [19]. Incorporating the active network state in adjusting $(b(T),r(T))$ acts as a proactive admission control to manage network congestion. Depending on if the input traffic is request or reply, we can have two different types of shapers: one based on prediction and the other on casuality. In the past, we have studied the *prediction-based shaper* [19], which applies to the request-type traffic such as master or peer initiated memory or coherency request. Though the request-type traffic has a varying nature, we can perform a sliding window (T) based online $(b(T),r(T))$ characterization, and then use a Mealy state machine type of predictor to project its $(b(T),r(T))$ for the next epoch. In PQCOM, we focus on *causality-based shaper* for reply or response traffic, which is a casual traffic in the sense that the characteristics of a reply can be derived from its corresponding request. For example, a main-memory write request (evicting a whole cache line) results in only one write acknowledgement back.

The resource allocation assigns needed amount of buffers and bandwidth for each flow along its route according to decisions from RM. A basic principle, which shows good performance guarantee with good utilization, is the family of rate proportional service disciplines including weighted fair queuing (WFQ), weighted round-robin (WRR), virtual clock, service-curve fair queueing (SCFQ) etc. [13]. PQCOM intends to re-visit these formally-grounded techniques, study their energy efficiency and make adjustments if necessary. Note that these disciplines are not only used in macro-networks, they are also proposed for NoCs in MPSoCs and CMPs for QoS provisioning [8][6]. The DVFS configuration adjusts the operating speeds of routing units and physical channels to closet V/F scales according to decisions from PM. This link-level heterogeneity [20] opens even larger room than the router-level heterogeneity [14] to minimize power. The resource reservation and DVFS configuration are updated epoch by epoch so as to adapt to application's execution phases, flexible QoS requirements and targets.

Based on the predictive input traffic (I,A,b,r) characteristics (either projected or derived) and the network load or thermal status, the RM and PM make resource allocation decisions in routers and DVFS configuration decisions for partitioned V/F islands, respectively. The basic principle is to reserve bandwidth and power budget according to r for each flow over a deterministic path from source to destination. The reservation does not have to be exactly r, though. To accommodate design space exploration, the valid reservation falls into range $[r,F]$. While a feedback-based performance or power tuning framework is a versed approach [15][21], our key innovations in PQCOM include:

(1) Inspired by task migration, we introduce a new concept of *flow migration* or *flow re-routing* to exploit the path diversity to balance workload and thermal distribution by re-allocating a perhaps non-minimal path at runtime. Data locality will be imposed by scheduling flows in local regions to minimize data movement over the network. The RM is responsible for scheduling flows, and makes flow routing and migration decisions.

(2) Besides the spatial exploration via flow migration, we also want to temporally explore the *permissible allocation range* $[r,F]$ to investigate application-level performance/power tradeoffs empirically and analytically, in conjunction with Phase 2 and 3. A larger resource allocation can speed up flow delivery but consumes more power. A smaller resource allocation is less performing but burns less power. We intend to apply the well-known *Pareto analysis* [22] to model and analyze the tradeoffs. Among a set of factors influencing a given objective, Pareto analysis can help to identify the most critical one. This information can be exploited by RM-PM to optimize decisions

towards specific objectives.

(3) We investigate the interactions between RM and PM to develop *collaborative mechanisms* to optimize performance, power and thermal distribution. While (1) and (2) are orthogonal, (3) relies on (1) and (2) to achieve. For example, when PM notices an overheated region due to a heavily used routing path, it will inform RM to re-route related traffic (flow migration) or reduce resource allocation on the path. When RM has to transfer urgent high-criticality traffic, it may advise PM to raise related router/channel frequencies to temporally form an express channel.

The outcome of Phase 1 is the framework design, partly based on our previous works (See Section 5). The milestones include the causality-based shaper, flow migration methods for load and thermal balancing, Pareto analysis of application-level performance-power tradeoffs, and resource-power co-allocation mechanisms for optimized performance, power and thermal distribution.

3.3 Phase 2: Per-Application Performance and Power/Energy Analysis

After designing the framework, PQCOM attempts to rigorously investigate the energy-aware performance isolation property. We intend to answer the following questions: For performance isolation, how can *per-application* communication throughput, delay and backlog bounds be mathematically derived? For power/energy efficiency, given a set of co-running applications on the co-management platform, what is the *ideal (minimum) power/energy consumption* without compromising QoS guarantees?

The performance analysis is based on *network calculus* [16][17][18], a queuing theory for analyzing worst-case network performance. The research was initiated from Computer Networks in the 90's [16], and has ever since been a powerful foundation for QoS provisioning in Internet and ATM [18]. Here we briefly introduce its fundamental concepts and basic results. Network calculus developed two fundamental abstractions. One is *arrival curve* to upper-bound the cumulative behavior of a traffic flow and the other *service curve* to lower-bound the cumulative service behavior of a network element (a router or channel). The simple yet elegant arrival curve has a linear form $\alpha(t) = b + rt$ [16], where b stands for burst tolerance and r sustainable rate. The simple yet powerful service curve is the latency-rate server in the form $\beta_{R,T} = R(t-T)^+$, where R is the minimum service rate and T the maximum processing latency of the network element [17]. Notation $x^+ = x$ if $x > 0$; $x^+ = 0$, otherwise. When a flow constrained by a linear arrival curve is served by a latency-rate server, the delay bound $\bar{D}$ and backlog bound $\bar{B}$ of the flow can be calculated by $\bar{D} = T + \frac{b}{R}$ and $\bar{B} = b + r \cdot T$, respectively. Since service rate $R \in [r, F]$ is valid, R can be flexibly set to explore meaningful resource-performance tradeoffs. The backlog bound $\bar{D}$ is useful for sizing and reserving buffers in routers. Even if the buffer size may have already been determined, this bound can be used to "turn off" un-used buffers to save power.

Over the last five years, we have gained substantial knowledge and experience in the network calculus based *per-flow* performance analysis for NoCs (See Section 5). In PQCOM, we leverage our per-flow analysis to *per-application* analysis. While per-flow concerns a single flow over a single path, per-application results in multiple flows (from core to memory, from core to core) over multiple paths. Through the per-application analysis, we will further gain insights on application's critical performance path, which is often cumbersome to conclude from simulations. For example, whether application's QoS property is more sensitive to memory access flows or cache coherency flows. This pathological information can be used to speed up program execution without increasing power budget by, for example, re-routing the critical flows to less-congested or express channels. Per-application analysis will use our previous per-flow analysis techniques but it is not a mere iteration of per-flow analysis for multiple flows because these flows from the same application are not independent but often dependent. We need to build a proper task graph model where flow dependency and concurrency can be expressed. Based on such a model, per-application performance analysis can be carried out to compute required buffer sizes, end-to-end delay and throughput bounds.

The power/energy analysis focuses on finding the theoretical limits of power/energy consumption without QoS distortion, given a set of applications executing on the shared NoC platform

simultaneously. We gradually approach the goal from low to high level step by step.

(1) We first investigate the power/energy implications of the QoS-capable rate-proportional service disciplines [13]. These disciplines (WFQ, WRR, Virtual Clock, SCFQ, etc.) can be modeled by a latency-rate server to reason about multiplexing flows' throughput, delay and backlog bounds. However, their impact on power/energy consumption and resulting energy-delay products have not been studied. Although they all can provide guaranteed bandwidth reservation, their exact packet delivery order and packet timing behavior are different [13]. They also largely differ in their arbitration circuits, circuit and buffering behaviors affecting switching probabilities and switched capacitances, implying a diverse impact on power and energy. We will add capacitance models for these arbiter components in ORION [23], and run cycle-accurate simulation to trigger switching activities so as to accurately calculate router and network power. The leakage power will be included.

(2) Then we look into *contention power*, a new concept that we introduce to capture additional power due to resource contention. Our particular interest is how much additional power/energy is needed in the NoC when an application runs together with other applications, compared to standalone execution? Upon network resource sharing, the performance of an individual application is no longer solely dependent on its own behavior. So is the power of the application. The reason is that contending for shared resources creates not only delay but also re-arbitration and waiting (in buffer) related power consumption. Together with the power study of the QoS disciplines, we will quantify the contention-resulted additional dynamic and leakage power.

(3) Based on (1) and (2), we finally attempt to find the lower bounds in power/energy consumption in the NoC. From (2), we know that more contention would consume more power. If we minimize the contention, the contention power will be minimized. This is in turn associated with our system goals in balancing load and thermal distribution under QoS constraints. By investigating the ideal load/thermal balancing, we should be able to analyze the minimum power/energy consumption. To enable quick exploration, we need a high-level formal analysis method, which can embed the cycle-accurate power estimates of the QoS policies and contentions. To this end, since the QoS disciplines reserve channel bandwidth, the concept of using link utilization as the unit of abstraction [24] can be naturally employed and adapted for our high-level network power estimation. The effects of resource allocation aware DVFS configurations due to flow migration and exploration of $[r, F]$ allocation flexibility are to be considered.

The milestones of Phase 2 include network calculus based per-application performance analysis methodology, power/energy analysis for rate-proportional service polices, contention power analysis, and analysis of theoretical potentials in power/energy efficiency.

3.4 Phase 3: Implementation and Evaluation of the Framework

Besides pursuing rigorous performance-power analysis, PQCOM has a relatively heavy experimental setting. The primary need for implementation is to realize a *reference design* of the framework in a full-system context in order to conduct system-wide evaluation. The evaluation objectives are to (1) evaluate per-application performance isolation property in a full-system simulation environment; (2) evaluate power/energy consumption of applications over the shared NoC resources. In particular, how the theoretical potentials in power/energy efficiency (from results of Phase 2) can be approached in practical non-ideal conditions? (3) evaluate overheads in performance, cost and energy of the additional modules.

According to the framework in Phase 1, we will make a complete reference design. We will implement the causality-based shaper, deriving casual response flows' characteristics from that of request flows. The RM and PM are feedback based closed-loop decision makers. For example, the RM monitors the actual network load status and uses this information to coordinate the behavior of the flow shapers. When a network region is overloaded, related traffic injection may need to be slowed down; when a network region is under-loaded and thus excessive services are available, related traffic injection can be opportunistically speed up. Among a variety of control theories, we have exercised the *fuzzy control* theory, which relies on fuzzy logic to pursue precise control. Our latest study [21] shows that this theory is particulary suitable and promising because of the

nature of the control problem. First, network states cannot and need not to be precisely described. Approximate judgement such as lightly loaded, medium loaded, heavily loaded is good enough. Second, the control loop has latency and the network state change is relatively latent due to buffering effect. This means that immediate reaction to the network state change is not necessary. A fuzzy mechanism gives comfortable tolerance to latent control and network state transitions. As a result, it can promise both control optimality and stability.

The RM and PM may be implemented either in a centralized or distributed fashion. Since our focus is not on specific implementations but fundamentals, we will start with centralized RM and PM implementations for simplicity and global optimization before going for distributed ones. This also allows us to concentrate on developing their collaborative mechanisms. Already in modern multicore processors, Intel's Nehalem architecture uses a small processor as a centralized power control unit for chip power management [25]. To overcome the scalability limitation of a centralized RM/PM, we will take a *divide-and-conquer* approach to manage large scale systems. The network is partitioned into clusters, and each cluster owns a RM/PM making local cluster decisions. The cluster RMs/PMs may be either networked with each other to exchange cluster load/thermal information (peer-to-peer RM/PM) or connected to a global RM/PM (hierarchical RM/PM) who receives cluster-wide load/thermal information and makes global resource allocation and DVFS configuration decisions.

In the NoC, the key innovation is to develop a new *application-aware flow router* to conduct flow-wise rate-proportional bandwidth and power allocations. The router maintains and updates per-application state (through flow ID) epoch by epoch. Packets from the same application will be treated in the same way, and packets from different applications may be treated with differentiation. The router owns non-uniform link Vs/Fs and widths. Similarly to [20], it provides adaptive data rates (closest to the V/F levels) for different output links. We will also incorporate known good ideas to explore heterogeneity at the network level. The network is hierarchical with *bandwidth tapering* where higher bandwidth per operation is provided at the lowest level of hierarchy to support data locality and overall lower bandwidth per operation at higher levels to save energy [10]. The network has a GALS communication style where clock domain interfaces will be realized using a dual-clock buffer interface, as with [14].

Two orthogonal aspects for the evaluation are on *sensitivity* and *scalability*. Sensitivity refers to how per-application performance is sensitive to a parameter in the design space of the framework. For example, one crucial parameter is the length of epoch, which defines the time granularity of resource reservation and DVFS. A smaller epoch ensures fast adaptivity to varying workloads while a larger epoch ensures stability for more invariant workloads. Fast adjustment of DVFS can theoretically be more optimal but if associated higher overhead is taken into account, it may not even break even. Such evaluation will need a thorough evaluation on the overheads from V/F domain interfaces, configuration and controller overheads. Scalability refers to how the properties of the framework in performance isolation and energy efficiency be maintained when the system size enlarges. This is important to understand its applicability to large systems.

To make the evaluation results convincing, PQCOM shall use well accepted system simulators and benchmarks. The plan is to design, implement and integrate the framework in the full-system simulator GEM5 [26], in which the build-in network GARNET will be innovated with the application-aware flow router and the GALS hierarchical network. ORION 3.0 (3.0 is the latest version) provides the NoC power-performance estimates for different technologies [23]. PARSEC [27] (for emerging RMS (Recognition-Mining-Synthesis) applications and large scale multi-threaded programs) and EEMBC (for embedded applications http://www.eembc.org/) will be the benchmarks.

The outcome of Phase 3 comprises a fully functioning co-management framework together with an evaluation methodology, experiments and results followed by well-grounded conclusions.

4 Significance

PQCOM addresses a timely important problem with future vision in mind. The QoS issue is raised recently in all kinds of multicore systems running multiple applications simultaneously. As the rapidly growing number of cores and the rapidly increasing number of co-running applications,

the problem becomes extremely urgent. While offering a certain level of application-level performance isolation, current multicore QoS research has not jointly addressed energy. Apparently the power-unconscious QoS approach must be leveraged due to the universal concern in energy efficiency and the particular role of multicore chips as building blocks in enterprise, embedded and mobile computing systems. Moreover, the concept of co-managing resource and power for QoS assurance enables to achieve performance isolation with energy efficiency, load balancing with thermal balancing. With "one shot multiple targets", the proposed framework likely influences how next-generation highly efficient heterogenous computers will be built.

The PQCOM approach has a non-incremental compelling nature. It is grounded on the fundamental relation between required resource and required power consumption (Equation 1). The (b, r) model borrowed from the Communication Networks discipline establishes a proper foundation for resource/power allocation and analyzable performance guarantees. As embedded systems transit from single core to NoC-based multicores, WCET (worst-case execution time) and WCRT (worst-case response time) analysis for timing-critical applications becomes much more complicated due to sharing network resources. The performance-power analysis techniques of PQCOM target the bottleneck problem. Through mathematical analysis, PQCOM provides deep insights to performance isolation, energy minimization and their relationship, which cannot be obtained through simulation. As such, it may further inspire new ways to build predictable real-time embedded computer architectures, following well-grounded mathematical formalisms.

5 Preliminary Results

The project proposer has strong background in QoS analysis and control in NoCs. As PI, his project "Formal QoS Analysis and Control for NoC Communication" was granted research gift from year 2011 to 2013 by Intel Corporation through the "Future of On-Die Communication Fabrics" academic research program. This program contains only six projects from six top universities worldwide.

For the formal QoS analysis of NoCs, he has been a pioneer adopter of network calculus. He published the first paper on employing network calculus for worst-case performance analysis of packet-switching NoCs in TCAD [28]. This paper proposes a step-by-step procedure to derive per-flow delay bound based on a contention tree model capturing arbitrary flow interferences. In his Intel project, he developed a QoS analysis methodology using network calculus based on Intel's formal communication modeling framework [29] (Best paper candidate of NOCS'2013). By formulating the analysis accuracy into an optimization problem, his recent research shows that the network calculus based analytic delay bounds are very tight (97%) when compared against simulated results [30]. For the formal QoS control of NoCs, he has developed an online (b, r) traffic characterization method and a prediction-based open-loop shaper to perform proactive admission control [19]. Furthermore, he recently proposed a fuzzy-logic based feedback controller to improve both worst-case and average-case network performance [21]. These models, implementations and experimental platforms (GEMS, predecessor of GEM5) are to be used or adapted in construction of the reference design and experiments.

As network calculus is an essential knowledge for PQCOM, his track record in deploying network calculus for QoS analysis and control on chip places him in an excellent position to exercise the project tasks, produce quality results and eventually generate high impact.

References

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Appendix B

Curriculum vitae

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Appendix B
Curriculum Vitae of Zhonghai Lu

1 Higher education qualifications

- June 1989, BSc. in Radio & Electronics, Beijing Normal University, China.
- June 2002, MSc. in System-on-Chip Design, KTH Royal Institute of Technology.
- October 2012, MBA in Innovation and Growth, University of Turku, Finland.

2 Degree of Doctor

March 2007, Ph.D. in Electronic and Computer System Design, KTH.
Thesis: *Design and Analysis of On-Chip Communication for Network-on-Chip Platforms*.
Supervisor: Axel Jantsch

3 Postdoctoral work

April 2007 - March 2010: Postdoc
Dept. of Electronics, Computer and Software Systems, KTH.

4 Decent

Granted in November 2011, KTH.

5 Present position

From May 2011, Associate Professor (Universitetslektor), School of ICT, KTH.

6 Previous employment

- April 2010 - April 2011. Researcher (Tillsvidareanställning) at KTH.
- Jan. 2002 - March 2007. Research and teaching assistants at KTH.
- June 2000 - Aug. 2000. Engineer, Beijing Office, Axis Communications of Sweden.
- Sept. 1989 - May 2000. Electronic Engineer, China Electronic Equipment System Engineering Company.

7 Interruptions in research

No interruption.

8 PhD/Postdoc supervision as the main supervisor

8.1 Graduated PhD

- Huimin She, Graduated in September 2012.
  PhD Thesis: Performance Analysis and Deployment Techniques for Wireless Sensor Networks

8.2 Current Postdoc supervision

- Yang Chen, joining my research group as postdoc from Nagoya University, Japan.
  March 2013 - February 2015

9 Deductible time

None.

10 Other relevant information

10.1 Research Grant as PI

- Sponsor: Intel Corporation, Portland, USA
  Project: Formal QoS Analysis and Control for Network-on-Chip Communication
  Program: Future of On-Die Communication Fabrics
  Period: Year 2011 - 2013

10.2 Awards and recognition

- Best paper candidate at NOCS'2013. (Seventh ACM/IEEE International Symposium on Networks-on-Chip), Tempe Arizona, USA, April 2013.
- Best paper candidate at ICCAD'2009 (IEEE/ACM 2009 International Conference on Computer-Aided Design), San Jose, USA.
- Best paper selection at FDL'2005 (2005 Forum on Design Languages), Lausanne, Switzerland.
- Best paper nominee at DATE'2003 (2003 Design, Automation and Test in Europe Conference), Munich, Germany.

10.3 International Research Visits

- August 2013: Norwegian University of Science and Technology (NTNU), Trondheim, Norway.
- Nov. 2009 - Jan. 2010: Swiss Federal Institute of Technology, Zürich (ETHz), Switzerland.
- Oct. - Nov. 2008: National Institute of Informatics (NII), Tokyo, Japan.
- June - August 2005: Samsung Electronics, Seoul, Korea.
- June 2004: Tempere University of Technology, Finland.

10.4 Review for Transaction/Journal papers

- IEEE Transactions: TVLSI, TCAD, TC, TII.
- ACM Transactions: TECS, TODAES,
- Other journals: JSA, JDEDS, JPDA, MicPro, IET-CDT, IJCA, Microelectronics Journal, VLSI Design, DAEM, IJE, AJSE.

10.5 Conference/Workshop TPCs and Chairs

- TPC members: NoCS, NoC-Arc, SoCC, NPC, APPT, ASICon.
- Organization chair, APPT, in Stockholm, Sweden, August 2013
- Tutorial chair + Session chair, NOCS, in Arizona, USA, April 2013
- Session chair, CODES+ISSS, in Tampere, Finland, October 2012
- Organization chair, WSN workshop at The IOT Industry Development (Shanghai) Forum, Nov. 2011
- TPC chair, NoCArc, in Atlanta, USA, December 2010,
- Session chair, CODES+ISSS, in Grenoble, France, October 2009

10.6 Assignments as public examiner

- PhD thesis evaluation for Bo Yang, University of Turku, Finland, October 2013
  Thesis title: Towards Optimal Application Mapping for Energy-Efficient Many-Core Platforms
- PhD thesis evaluation for Ville Rantala, University of Turku, Finland, October 2012
  Thesis title: On Dynamic Monitoring Methods for Networks-on-Chip
- PhD defense committee for Yi Guo, Universitat Autonoma de Barcelona (UAB) Spain, Dec. 2011
  Thesis title: Parallel Post-Processing Solution for GNSS-R Instrument

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Appendix C

List of publications

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Publication List (Year 2007 - 2014) of Dr. Zhonghai Lu

KTH Royal Institute of Technology, Stockholm
Email: zhonghai@kth.se

April 2014

Notes:

- The list contains publications for the last eight years, from 2007 to 2014.
- The five publications most important for the project are indicated with an asterisk (*).
- The citation data below are from Google Scholar.

Table 1: **Citation Statistics**

	All	**Since 2009**
Citations	1267	1081
H-index	19	17
i10-index	37	31

1 Peer-reviewed original articles

1. Shaoteng Liu, Axel Jantsch and **Zhonghai Lu**. "A Fair and Maximal Allocator for Single-Cycle On-Chip Homogeneous Resource Allocation". IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Accepted for publication in September 2013 (E-version online).

2. Zhi Zhang, **Zhonghai Lu**, Vardan Saakian, Xing Qin, Qiang Chen, and Li-Rong Zheng. "Item-level indoor localization with passive UHF RFID based on tag interaction analysis". IEEE Transactions on Industrial Electronics, 61(4):2122-2135, April 2014.

3. Chaochao Feng, **Zhonghai Lu**, Axel Jantsch, Minxuan Zhang, Zuocheng Xing. "Addressing Transient and Permanent Faults in NoC with Efficient Fault-tolerant Deflection Router". IEEE Transaction on Very Large Scale Integration Systems (TVLSI), 21(6):1053-1066, June 2013.

4. Abdul Naeem, Axel Jantsch and **Zhonghai Lu**. "Scalability Analysis of Memory Consistency Models in NoC based Distributed Shared Memory SoCs". IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 32(5):760-773, May 2013.

5. Xiaowen Chen, **Zhonghai Lu**, Axel Jantsch, Shuming Chen, Shenggang Chen and Huitao Gu. "Reducing Virtual-to-Physical address translation overhead in Distributed Shared Memory based multi-core Network-on-Chips according to data property", ELSEVIER Computers & Electrical Engineering, 39(2):596-612, February, 2013.

6. Abbas Eslami Kiasari, **Zhonghai Lu**, and Axel Jantsch. "An Analytical Latency Model for Networks-on-Chip". IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 21(1):113-123, January 2013.

7. (*) Meikang Qiu, Zhong Ming, Jaiyin Li, Shaobo Liu, Bin Wang and **Zhonghai Lu**. "Three-Phase Time-Aware Energy Minimization with DVFS and Unrolling for Chip Multiprocessors". Journal of Systems Architecture (JSA) - Embedded Systems Design 58(10): 439-445, 2012.

8. Ming Liu, **Zhonghai Lu**, Wolfgang Kuehn and Axel Jantsch. ”A Survey of FPGA Dynamic Reconfiguration Design Methodology and Applications”. International Journal of Embedded and Real-Time Communication Systems (IJERTCS) 3(2): 23-39, 2012.

9. Chaochao Feng, **Zhonghai Lu**, Axel Jantsch and Minxuan Zhang. ”A 1-cycle 1.25 GHz Bufferless Router for 3D Network-on-Chip”. IEICE Transactions on Information and Systems. 95-D(5): 1519-1522, 2012.

10. Chaochao Feng, **Zhonghai Lu**, Axel Jantsch, Minxuan Zhang and Xianju Yang. ”Support Efficient and Fault-tolerant Multicast in Bufferless Network-on-Chip”. IEICE Transactions on Information and Systems. 95-D(4):1052-1061, 2012.

11. Wenmin Hu, Hengzhu Liu, **Zhonghai Lu**, Axel Jantsch, G Hu. ”Self-selection pseudo-circuit: a clever crossbar pre-allocation”, IEICE Electronics Express, 9(6):558-564, 2012.

12. Wenmin Hu, **Zhonghai Lu**, Hengzhu Liu, Axel Jantsch. ”TPSS: A Flexible Hardware Support for Unicast and Multicast on Networks-on-Chip”. Journal of Computers. 7(7):1743-1752, 2012.

13. Zhi Zhang, **Zhonghai Lu**, Qiang Chen, Xiaolang Yan and Li-Rong Zheng. ”CDMA-PPM UWB RFID for Internet of Things: Concept and Analysis”, International Journal of Communication Systems, 25(9): 1103-1121, 2012.

14. Yancang Chen, **Zhonghai Lu**, Lunguo Xie, Jinwen Li, Minxuan Zhang. ”A single-cycle output buffered router with layered switching for Networks-on-Chips”. ELSEVIER Computers & Electrical Engineering 38(4):906-916, 2012.

15. Huimin She, **Zhonghai Lu**, Axel Jantsch, Dian Zhou and Li-Rong Zheng. ”Performance Analysis of Flow Based Traffic Splitting Strategy on Cluster-Mesh Sensor Networks”. International Journal of Distributed Sensor Networks. 2012.

16. Zhi Zhang, **Zhonghai Lu**, Qiang Chen and Xiaolang Yan, ”Design and Optimization of a CDMA-based Multi-Reader Passive UHF RFID System for Dense Scenarios,” IEICE Transactions on Communications, E95-B(01):206-216, Jan. 2012.

17. Xiaowen Chen, Shuming Chen, **Zhonghai Lu**, Axel Jantsch: ”Hybrid Distributed Shared Memory Space in Multi-core Processors”. Journal of Software (JSW) 6(12): 2369-2378, Dec. 2011.

18. Xiaowen Chen, **Zhonghai Lu**, Axel Jantsch, Shuming Chen and Hai Liu, ”Cooperative Communication Based Barrier Synchronization in On-Chip Mesh Architectures”, IEICE Electronics Express, Vol.8, No.22, 1856 - 1862, November 2011.

19. Ming Liu, **Zhonghai Lu**, Wolfgang Kuehn and Axel Jantsch. FPGA-based Particle Recognition in the HADES Experiment. IEEE Design & Test of Computers, 28(4):48-57, July/August 2011.

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21. Ming Liu, Wolfgang Kuehn, Soeren Lange, Shuo Yang, Johannes Roskoss, **Zhonghai Lu**, Axel Jantsch, Qiang Wang, Hao Xu, Dapeng Jin, Zhen'an Liu. *A High-end Reconfigurable Computation Platform for Nuclear and Particle Physics Experiments*, IEEE Computing in Science and Engineering (CiSE). 13(2):52 - 63, March/April 2011.

22. Ning Ma, **Zhonghai Lu**, and Lirong Zheng. *System Design of Full HD MVC Decoding on Mesh-based Multicore NoCs*. Microprocessors and Microsystems: Embedded Hardware Design (MICPRO). 35(2):217 - 229, March 2011.

23. Fahimeh Jafari, **Zhonghai Lu**, Axel Jantsch, and Mohammad Hossein Yaghmaee. *Buffer Optimization in Network-on-Chip Through Flow Regulation*. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 29(12):1973 - 1986, December 2010.

24. (*) Yue Qian, **Zhonghai Lu** and Wenhua Dou. *Analysis of Worst-Case Delay Bounds for On-Chip Packet-Switching Networks*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 29(5):802-815, 2010.

25. Yue Qian, **Zhonghai Lu** and Wenhua Dou. *Worst-Case Flit and Packet Delay Bounds in Wormhole Networks on Chip*, IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, Special Section on "VLSI Design and CAD Algorithms", 92-A(12): 3211-3220, December 2009.

26. Yue Qian, **Zhonghai Lu**, Wenhua Dou and Qian Dou. *Analyzing Credit-Based Router-to-Router Flow Control for On-Chip Networks*. IEICE Transactions on Electronics, Special Section on "Hardware and Software Technologies on Advanced Microprocessors", 92-C(10): 1276-1283, October 2009.

27. **Zhonghai Lu** and Axel Jantsch. *Time-Division-Multiplexing (TDM) Virtual-Circuit Configuration for Network-on-Chip*. IEEE Transactions on Very Large Scale Integration Systems (TVLSI) 16(8):1021-1034, 2008.

28. Huimin She, **Zhonghai Lu**, Axel Jantsch, Li-Rong Zheng and Dian Zhou. *Analysis of Traffic Splitting Mechanisms for 2D Mesh Sensor Networks*, International Journal of Software Engineering and Its Applications (IJSEIA), Vol.2 No.3, July 2008.

29. **Zhonghai Lu** and Axel Jantsch. *Admitting and Ejecting Flits in Wormhole-switched Networks on Chip*. IET Computers & Digital Techniques, 1(5):546-556, September 2007.

2 Peer-reviewed conference contributions

Year 2014

30. Yanchen Long, **Zhonghai Lu** and Xiaolang Yan. "Analysis and Evaluation of Per-Flow Delay Bound for Multiplexing Models". In Proceedings of Design, Automation and Test in Europe Conference (DATE'14), Dresden, Germany, March 2014.

31. Xueqian Zhao and **Zhonghai Lu**. "Empowering Study of Delay Bound Tightness with Simulated Annealing". In Proceedings of Design, Automation and Test in Europe Conference (DATE'14), Dresden, Germany, March 2014.

32. Shaoteng Liu, Axel Jantsch, and **Zhonghai Lu**. "Parallel Probe Based Dynamic Connection Setup in TDM NoCs". In Proceedings of Design, Automation and Test in Europe Conference (DATE'14), Dresden, Germany, March 2014.

33. (*) Yuan Yao and **Zhonghai Lu**. "Fuzzy Flow Regulation for Network-on-Chip Based Chip Multiprocessors Systems". In Proceedings of 19th Asia and South Pacific Design Automation Conference (ASP-DAC'14), pages 343-348, Singapore, January 2014.

Year 2013

34. Shaoteng Liu, Axel Jantsch, and **Zhonghai Lu**. "Analysis and Evaluation of Circuit Switched NoC and Packet Switched NoC". Proc. of Euromicro Conference on Digital Systems Design (DSD'13), 2013.

35. (*) Xueqian Zhao and **Zhonghai Lu**. "Per-Flow Delay Bound Analysis Based On a Formalized Micro-architectural Model", In Proceedings of the Seventh ACM/IEEE International Symposium on Networks-on-Chip (NoCS'2013), Tempe Arizona, USA, April 2013. (**Best Paper Candidate**)

Year 2012

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VETENSKAPSRÅDET
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2014-28050-116041-34

Name of applicant
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Date of birth
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Title of research programme

Appendix N

Budget and research resources

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Appendix N
Project Budget

Zhonghai Lu

1 Budget

The project is proposed for four years for the project leader and one full-time PhD student (to be employed through open announcement), working 30% and 80% for the project, respectively. At KTH, a full-time employed PhD student needs to spend 20% of time as teaching assistant.

Table 1: **Project Budget Table** (K SEK)

Year	**2015**	**2016**	**2017**	**2018**	**Sum**
Salary for Zhonghai Lu (30%)	284	296	308	320	1 208
Salary for one PhD student (80%)	384	420	481	528	1 813
Equipment and tool (Computer and software)	60	60	60	60	240
Conference and publication	50	50	50	50	200
Premises	110	118	129	138	495
Direct cost (Sum of the above)	888	944	1 028	1 096	3 956
Indirect cost	322	344	380	407	1 453
Total Cost (Direct + Indirect Cost)	**1 210**	**1 288**	**1 408**	**1 503**	**5 409**
Co-funds by KTH (20%)	242	258	280	301	1 081
Requested funds from VR (80%)	**968**	**1 030**	**1 128**	**1 202**	**4 328**

Table 1 shows the project budget. It includes both direct and indirect costs, which have been verified by the financier at the department.

The total project budget is 5,409 KSEK. KTH co-funds 20%, and we request 80%, i.e., 4,328 KSEK from VR.

2 Motivation

In the following, the costs are motivated one by one:

- Salary cost for the project leader: This is computed on the base of the project leader's current salary (48K SEK per month) and 30% workload on the project. Following KTH's standard, it takes into account anticipated salary growth.
- Salary cost for a PhD student: This is computed on the base of a new PhD student and 80% workload on the project. Currently the starting salary for a new PhD student at KTH is 26.4K SEK per month. Following KTH's standard, it takes into account anticipated salary growth for Ph.D. students.
- Equipment and tool: This covers the cost of one computer for the PhD student, hardware modeling, simulation, synthesis and software design tools, licences fees etc.
- Conference and publication: We plan to participate in two conferences a year. This will cover conference registration, hotel, travelling costs, and publication fees etc.
- Premises: This is computed as 17.3% of salary cost by related KTH standard.
- Indirect cost: This covers overhead costs at the three levels, i.e., KTH university, ICT school and the department. The amount is calculated according to related KTH standard.

VETENSKAPSRÅDET
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Kod
2014-28050-116041-34

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2014 -

Name of applicant
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Date of birth
681207-1279

Reg date
2014-04-09 23:13:00

Project title
PQCOM: Predictive QoS-Power Co-Management in Heterogeneous Multicore Platforms

NT

Research grants NT April 9, 2014
Project Grant Junior Researchers
*Övrigt generellt
Kungl Tekniska Högskolan

Appendix S

Signatures

NT-2

2015	2016	2017	2018	2019
1210	1288	1408	1503	

2015-01-01 -- 2018-12-31

Applicant

Date

Head of department at host University

Clarifi cation of signature

Telephone

A signature on the application is required not only from the applicant but also from the authorised representative of the administrating organisation/institution or equivalent (normally the head of the department or establishment where the research is to be conducted). The signature confirms that the department can accommodate the proposed research, position or equipment; that the costing in the application is approved for the department's part, that any proposed experimentation on human or animal subjects has been reported, and that the applicant has reported any secondary occupations and commercial ties (s)he may have, and nothing inconsistent with good research practice has thereby emerged. The applicant must have discussed these conditions with the representative of the administrating organisation/institution or equivalent before the latter approves and signs the application.

NOTE the exceptions!
Please note that a different procedure applies for the following types of grants:

- Infrastructure- Operation Grants
- Infrastructure- Grants for Expensive Equipment
- Infrastructure- Grants for Large Databases
- Framework Grant SIMSAM
- International Recruitment

For these types of grants the vice-chancellor, instead of the head of department, must sign Appendix S. Thereby (s)he confirms the commitments of the administrative organization. The details are specified in the Call for Proposals, published at www.vr.se.

Vetenskapsrådets noteringar
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