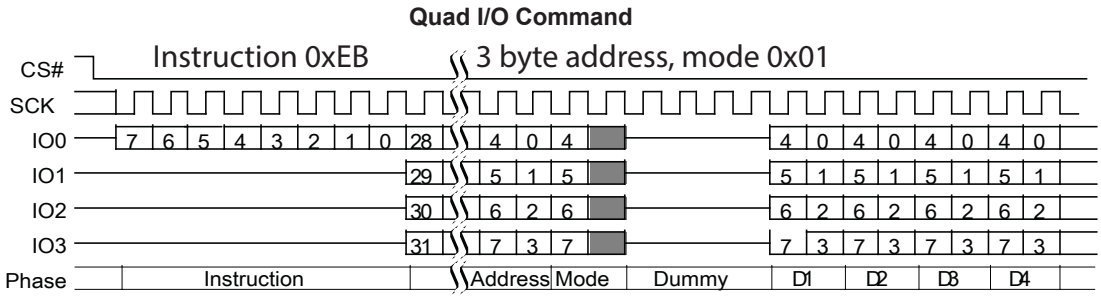
MEA1K interface emulator for Cypress speed testing and debugging



8 clk + 8 clk + 0 clk = 16 clk

IO lines should be in high impedance with CS# high and during 16 clocks before data output, but if needed any arbitrary number of Dummy clocks can be added

SPI mode 0,
i.e. CPOL=0, CPHA=0,
means CLK is low in waiting
and data read at Rising edge.
This also means that the first
bit should be set just after CS.
No DDR supported,
CLK max 80 MHz.

The format of this command is taken from description of Flash chip S25FL512S soldered at Cypress evaluation board.
However, this chip needs 4 Dummy clk cycles.
It would be nice to have for testing two similar interfaces with FPGA. One is exactly as shown in the picture above, but interpretation of instruction and address csan be omitted in FPGA. The second cionterface can have similar number clocks with high impredance output lines (16 clks), but should use 8 data lines instead of 4. Switrching between two modes can be done, for instance, by checking the state of one of the lines that are conected to the switch SW2 at the Lattice brerakout board, excepthe line IOT_37a, that is coinnected to the first switch. This line, when the switch is up, it blocks FPGA run for some unknown reason.
Switches 2-4irst of the switch SW2 that are lionked with the lines IOT_36b, IOT_44b and IOT_49a can be freely used.
Lower position of the switch connects the switch pads, making level of the corresponding line low,. Lifting of the switch will lift the level of the line to logical “1”.
For instance, switch number 4 with the line IOT_49a can be used.
High level of the line IOT_49a can be associatred with 8-line octal SPI interface.

The transmitted data can be repeatedly incrementing values from 0 to 0xFF. Data can be repeated until CS# is rised.