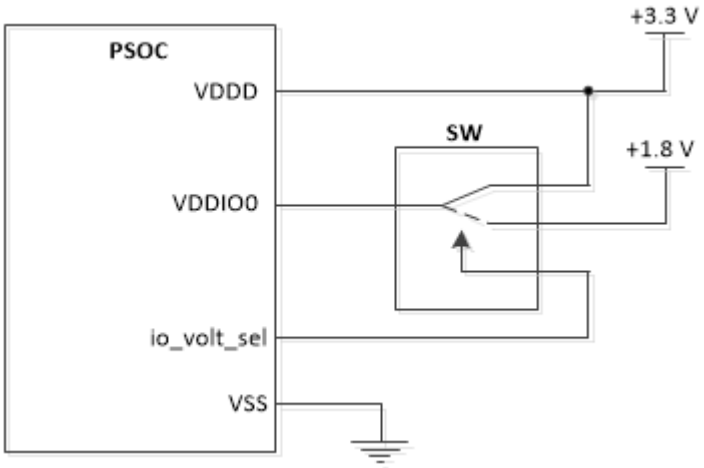
Modifications in Cypress CY8CPROTO-062-4343W PSoC 6 evaluation board

SD card IO voltage switching 3.3V -> 1.8V

Hi-speed communication modes of SD card SDR25 and SDR50 (25 MBps and 50 MBps respectively) require switching of the bus IO voltage from 3.3V to 1.8V after their initialization. The test has shown that the cards can work successfully in these modes even with 3.3V IO level, but to follow specification and to decrease current consumption it was decided to realize switching of the IO voltage on the board.

When the parameter lowVoltageSignaling in the configuration of SD host is true,, the SD Host driver sets UHS-I mode during the card initialization. The SD Host driver always starts talking to the card at 3.3V and then later switches to 1.8V. There is no internal regulator in the PSoC 6 to change SD signals from 3.3V to 1.8V. Thus, an external regulator ADG779 for the VDDIO of the PSoC device to provide the ability to go from 3.3V to 1.8V has been placed. The io_volot_sel was associated with the pin **P9_6** (white wire). The user function that is called by SD Host driver sets the io_volt_sel pin to **high when 1.8V level is needed**.



To isolate VDDIO0 pin from the bus with the same name resistor R54 was removed. And switch ADG779 switched voltage at processor VDDIO0 pin from 3.3V that was at VDDIO0line on the board and a pad of R84 absent resistor that has 1.8V voltage level. To indicate status of P9_6 line orange LED APHHS1005SECK was connecting this line to the ground though 1K 0603 resistor. Thus, orange LED is ON when IO level is 1.8V (high-speed mode).

Input voltage VDDIO0 sets voltage level for ports 11, 12, 13 to which SDIO1 with SD card is connected.

Table 21-1. I/O Banks

Ports	I/O Supply Source
Port 0	V_{BACKUP}/V_{SSIO_B}
Port 1	V_{DDD}/V_{SSIO_B}

Port 2, Port 3, Port 4	V_{DDIO_R}/V_{SSIO_R}
Port 5, Port 6, Port 7, Port 8	V_{DDIO_1}/V_{SSIO_1}
Port 9, Port 10	V_{DDIO_A}/V_{SSIO_A}
Port 11, Port 12, Port 13	V_{DDIO_0}/V_{SSIO_0}

Thus, setting this voltage also changes voltage level at QSPI communication port used for communication with FPGA controlling MEA1K neuro chip. Thus, voltage levels will be changed there as well. Thus, switched 1.8V level also should be routed to FPGA. This evaluation board also has another SDIO0 communication port that is associated with voltage level controlled by VDDIO_R that control ports 2, 3, 4. However, there SDIO WiFi adapter is attached. One could swap SD memory card with SDIO WiFi in theory, but there is another limitation. Maximal data rate that this WiFi is supported is 50 MHz. And the PSoC 6 provides o0ne single clock shared between SDIO1 and QSPI. Thus, placing WiFi at SDIO1 would limit speed maximal speed of QSPI 80 MHz by 50 MHz. This is not good. Thus, it was decided that it is better to limit SD card speed by 80 MHz (from maximal 100 MHz) and have maximal QSPI rate.

Switching OFF power of SD card (and QSPI flash on the same panel)

It has been found that pressing Reset button resets the processor, but puts micro SD card into a strange state. When SD initialization starts with SD inn this state, the driver does not determine that SD card support low levels of IO voltage. It initiates with a desired communication rate but at 3.3V level. To force the card start properly after each reset an additional 3.3V voltage regulator NCP177AMX330TCG was placed at the board. Its Enable pin was connected to **P6_2**. **High voltage level provided power** to micro SD and soldered on the panel QSPI flash. Regulator was powered from 3.6V source on the board and had two 1uF capacitors at input and output. Normal VDDIO was disconnected from this panel by cutting a track at main Cypress panel. Note that NCP177A has a discharge circuitry for fast discharging of capacitors at micro SD power line. When Enable is low, the output is shortened to the ground by 60R resistor internally in the voltage regulator.

18.75 MHz CLK output for FPGA PLL

18.75 MHz CLK output for FPGA PLL is associated with pin **P0_5**.

SD card communication pins

Other pins used for SD card communication are default:
CMD – **P12_4**, CLK – **P12_5**, #0 – **P13_0**, #1 – **P13_1**, #2 – **P13_2**, #3 – **P13_3**, Card detect (mechanical switch) – **P13_5**. When **SD card is inserted**, voltage level at P13_5 is **low**.

Interface with Lattice iCE40 Ultra Plus Breakout Board (UP5K FPGA, QFN48)

The following lines are routed to FPGA (Cypress pad to **Lattice pad**):

GND to **GND** (20-pin #19)
3.3V from the main regulator of Cypress board (not additional for micro SD/soldered Flash) to **+3.3V** (20-pin #1)
P0_5 (18.75MHz, always 3.3V level, separate 2-conductor cable, black) to **IOT_46b_G0** (ICE_CLK, pin closer to the center of Lattice PCB)
VDDIO0 (IO voltage 3.3 or 1.8V, separate 2-conductor cable, red) to **VCCIO_1** and **VCCIO_2,** pin close to the edge of Lattice PCB)
P11_1 (CS1, chip select for FPGA) to **IOB_8a** (20-pin #3)
P11_7 (CLK for FPGA) to **IOB_25b_G3** (20-pin #8)
P11_6 (#0) to **IOB_24a** (20-pin #6)
P11_5 (#1) to **IOB_4a** (20-pin #7)
P11_4 (#2) to **IOB_29b** (20-pin #10)
P11_3 (#3) to **IOB_5b** (20-pin #9)
P12_0 (#4) to **IOB_9b** (20-pin #5)
P12_1 (#5) to **IOB_23b** (20-pin #4)
P12_2 (#6) to **IOB_22a** (20-pin #2)
P12_3 (#7) to **IOB_2a** (20-pin #11)

Modifications in Lattice iCE40 UltraPlus Breakout Board

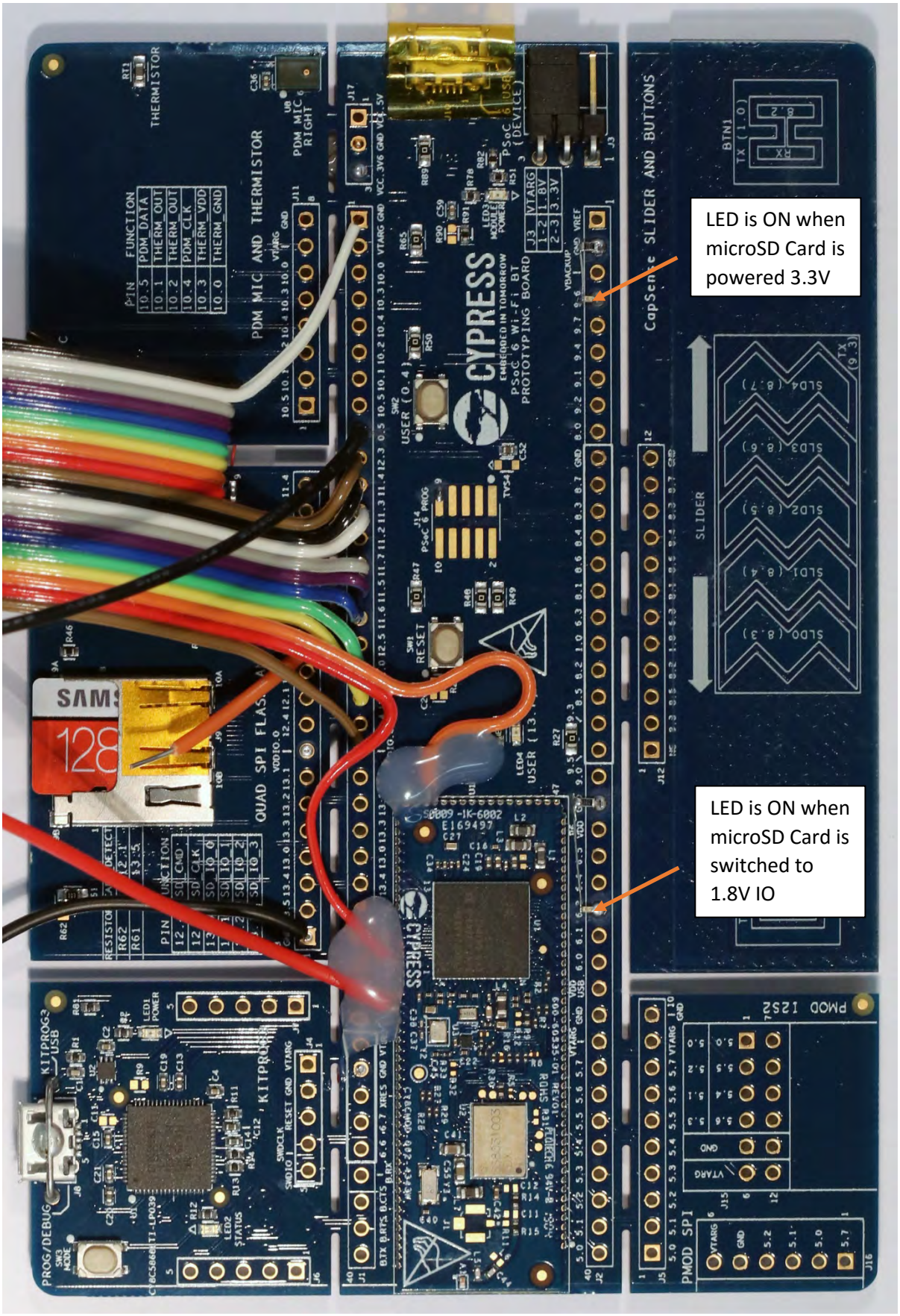
To make voltage at banks 1 and 2 switchable resistors R74 and R75 1R were disconnected from one side from +3.3V and connected with 3.3/1.8V source from Cypress board (the closest pin to the board edge from two) by red wire. If no Cypress board is connected and Lattice board is powered from its USB connector, the first pin +3.3V should be shortened with the mentioned above closest to the edge pin to provide 3.3V voltage to the banks 1 and 2. See photo below.

To make possibility to route 18.75 MHz clock to ICE_CLK a jumper has been placed at Lattice board. Originally 12 MHz clock was routed to FPGA from FTDI chip through jumper J51. To take the clock from Cypress this jumper should be removed, and new jumper (two closest to FTDI new pins) should be bridged. Yellow wire is used for routing of new 18.75 MHz clock.

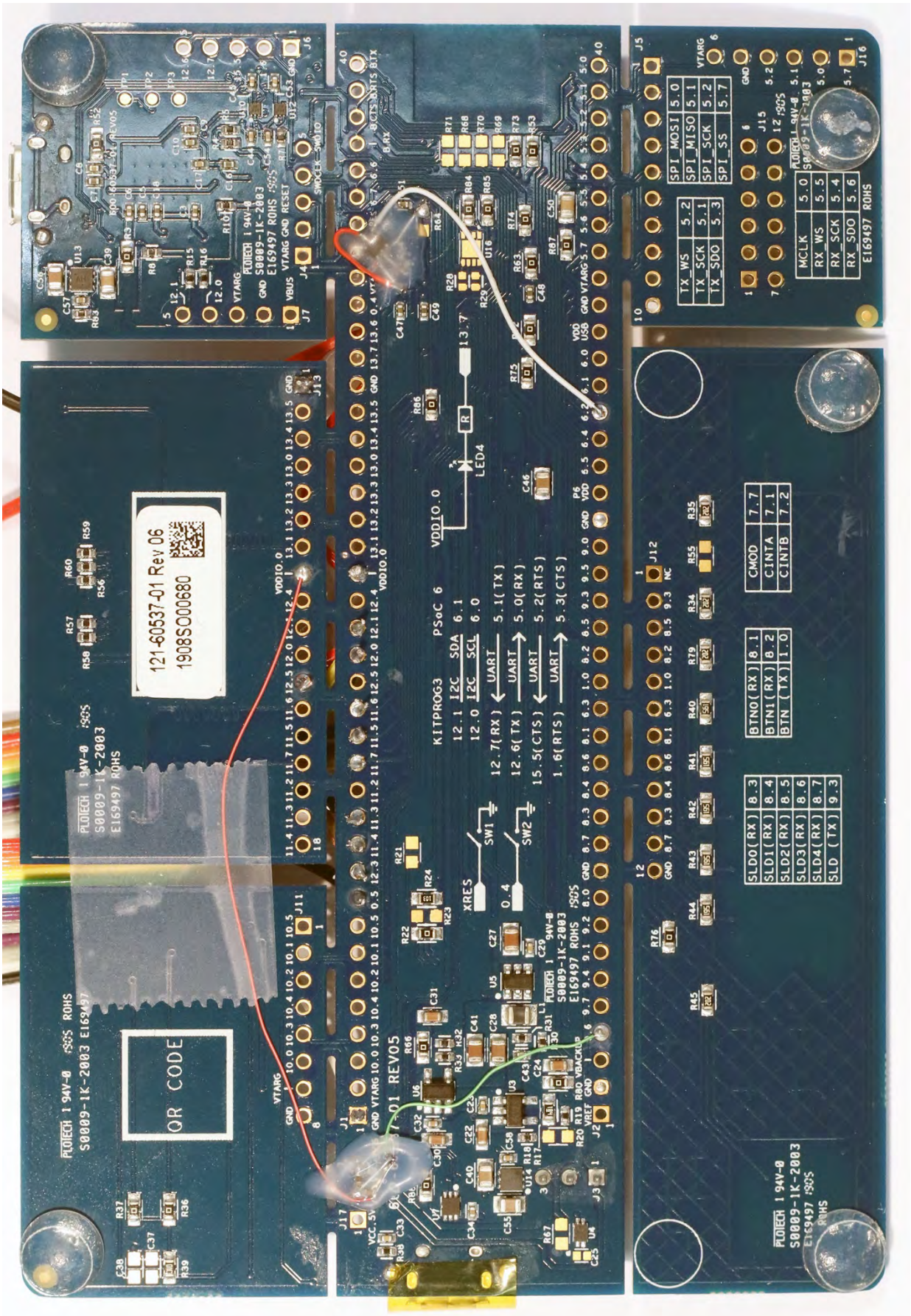
It has been found that even if 3.3V is given to Lattice board from Cypress board, the FPGA did not start because 1.2V FPGA core voltage is absent. It was received from 5V USB voltage through U7 dual output voltage regulator. To provide 1.2V core voltage 5V bus was powered from 3.3V bus from Schottky diode. The diode was soldered to TP1 +3.3V by one side and another side was connected with the distant from USB connector terminal of the coil L4.

Photos of changes in Cypress and Lattice boards

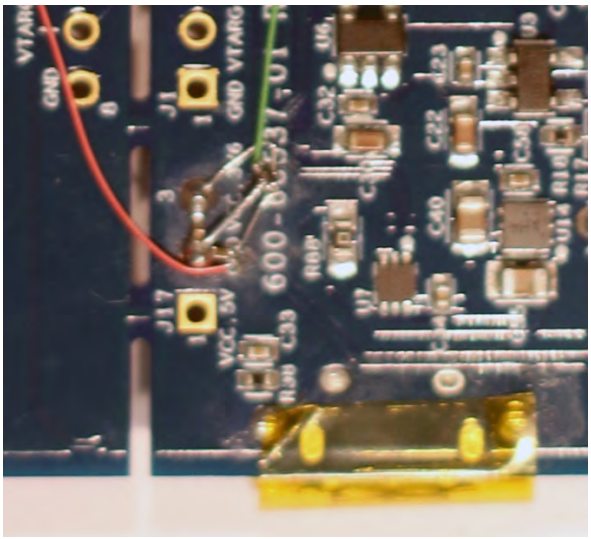
Cypress board frontal side

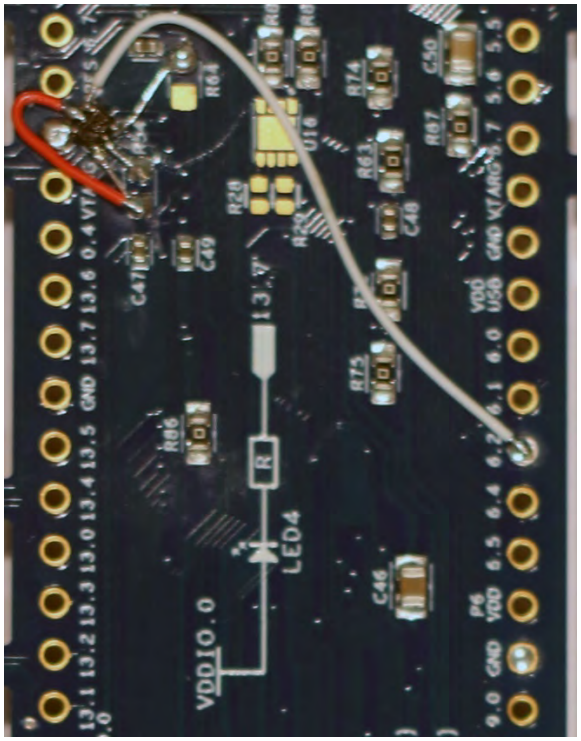


Cypress board rare side with covered analog switch and voltage regulator

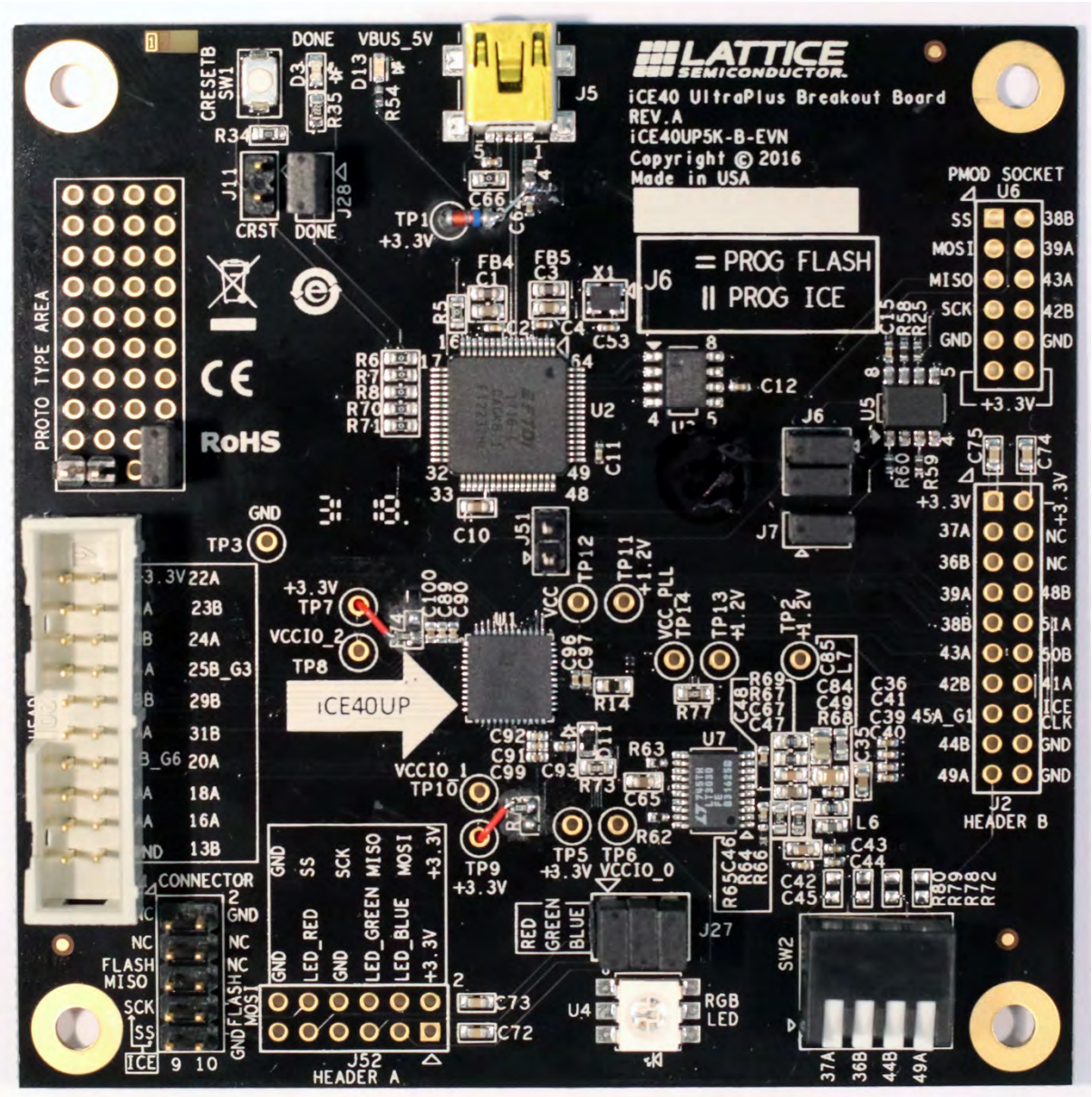


Cypress board rare side with uncovered 3.3V voltage regulator (on the left side) and analog switch (on the right side)

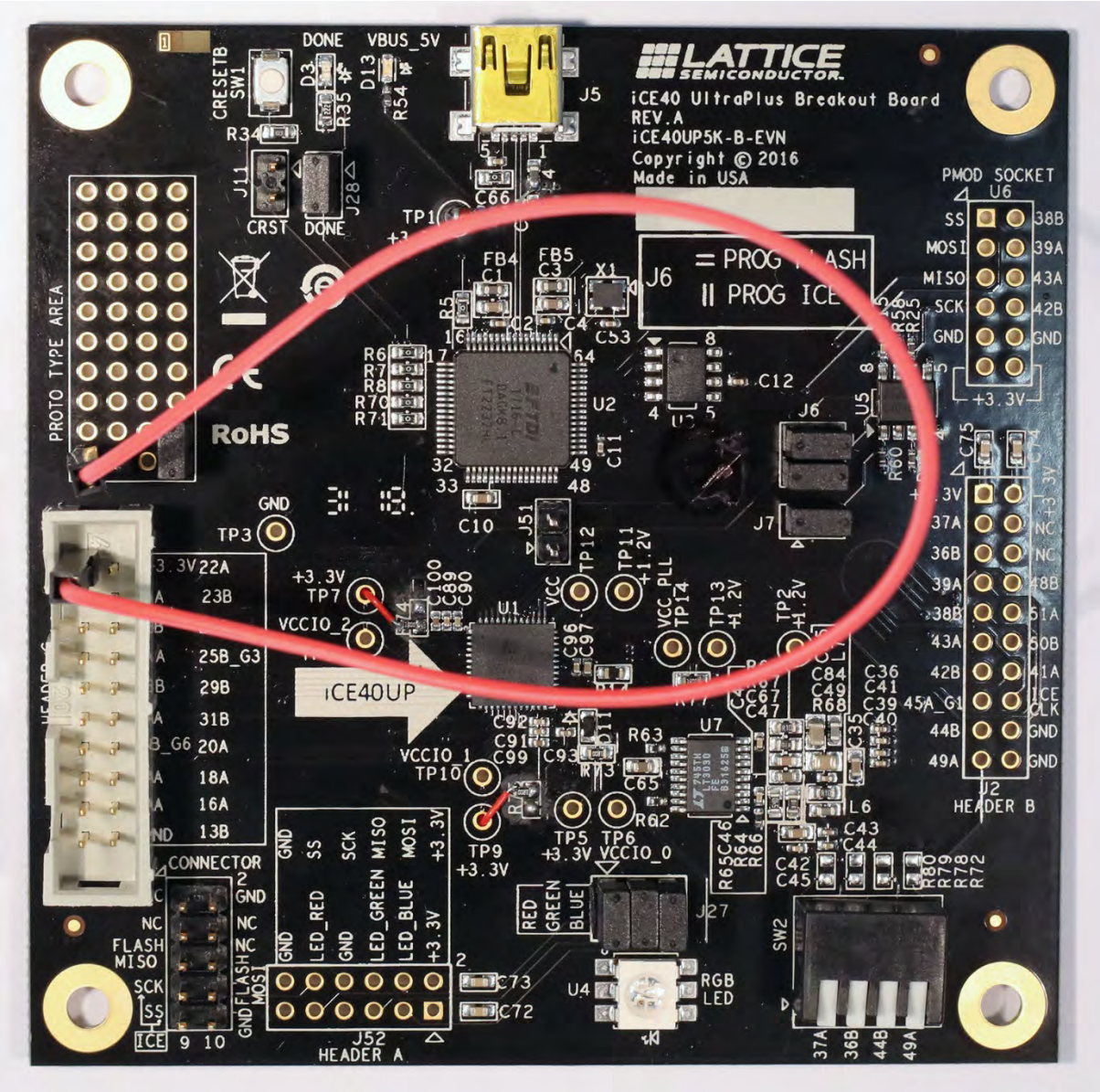




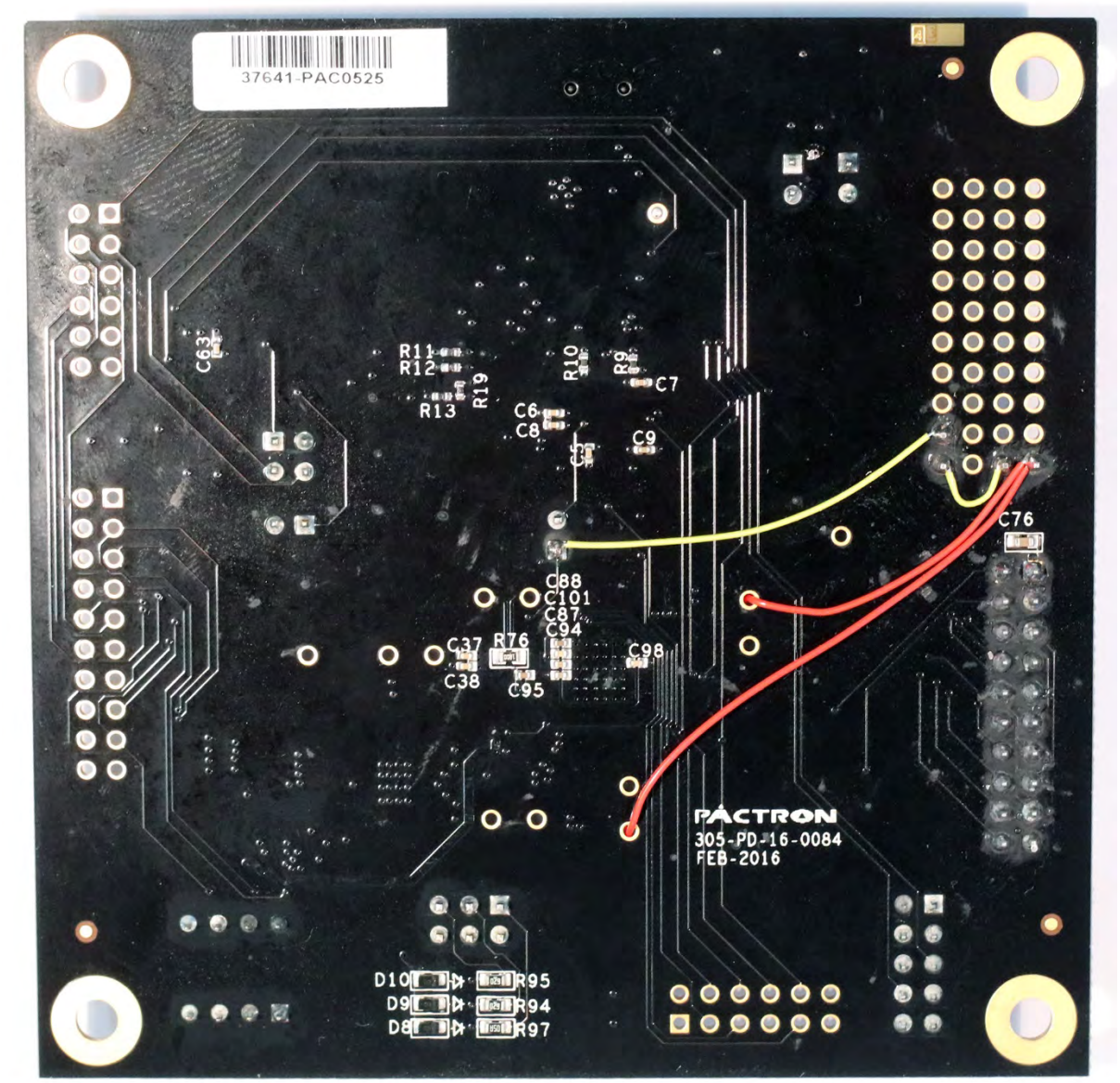
Lattice board frontal side



Lattice board frontal side with the bridged first pin of 20-pin connector (+3.3V) with 1.8/3.3V input for FPGA banks 1 and 2



Lattice board rare side



Cypress board and Lattice board connected together