Product family: zynq
Target device: xc7z020clg484-1

The result from Vivado HLS C synthesizer when using serial method:

Performance Estimates

- **Timing (ns)**
  - **Summary**

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.510	1.25

- **Latency (clock cycles)**
  - **Summary**

Latency		Interval		Type
min	max	min	max	
41	41	41	41	none

Utilization Estimates

- **Summary**

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	3	0	81
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	-	-	-	-
Multiplexer	-	-	-	51
Register	-	-	141	-
Total	0	3	141	132
Available	280	220	106400	53200
Utilization (%)	0	1	~0	~0

When the UNROLL hint use inside the loop the C synthesizer try to execute the loop in the parallel mode, as result the number of clocks which need to finish the task will decreases.

Performance Estimates

- **Timing (ns)**
  - **Summary**

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.742	1.25

- **Latency (clock cycles)**
  - **Summary**

Latency		Interval		Type
min	max	min	max	
8	8	8	8	none

Utilization Estimates

- **Summary**

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	6	0	335
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	-	-	-	-
Multiplexer	-	-	-	179
Register	-	-	393	-
Total	0	6	393	514
Available	280	220	106400	53200
Utilization (%)	0	2	~0	~0

In conclusion we can see by using the unroll hint, the number of clocks which need for solve the task decreases dramatically from 41 to 8 (it finishes the task almost 5 times faster), but the hardware resources which need is almost increases two times.