**Title**: Designing a Half Adder using CMOS.

**Abstract:**

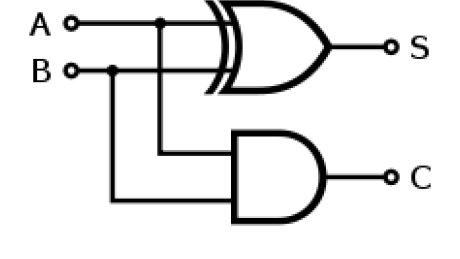
Adders and subtractors are the most basic and most important part of digital electronics. The main objective of the experiment is:

* Designing a Half Adder using CMOS.

**Introduction:**

**ADDER:**

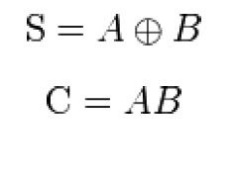
In electronics, an **adder** or **summer** is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations.

Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder– subtractor. Other signed number representations require a more complex adder.

**Fig-1:** Half adder logic diagram [1].

The **half adder** adds two single binary digits *A* and *B*. It has two outputs, sum (*S*) and carry (*C*). The carry signal represents an overflow into the next digit of a multi-digit addition. The value of the sum is 2*C* + *S*. The simplest half-adder design, pictured above, incorporates an XOR gate for *S* and an AND gate for *C*. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder.

The half-adder adds two input bits and generate carry and sum which are the two outputs of half-adder. The input variables of a Half adder are called the Augend and addend bits. The output variables are the Sum and Carry. The Truth table and equations for the Half adder are: [1]



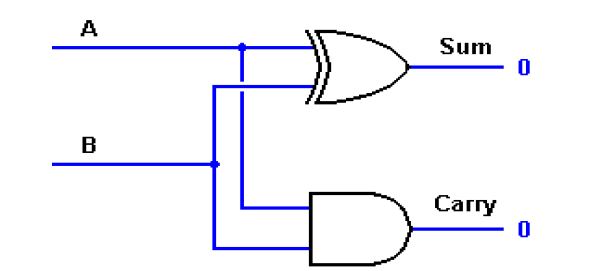
**Table-1:** Half Adder [1].

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | S | C |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**Theory and Methodology:**

To design any logic circuit first the truth table is needed to be established using different combinations of logic ‘0’ and ‘1’ to get the desired output. After that the gate level design is found from which transistor level design is done using desired transistors. Here CMOS is used for the transistor level design of the Half Adder. The whole process is given step wise below:

**Half Adder:**

Gate Level Design:

**Fig-2:** Logic diagram of a Half Adder [1].

Equation of Sum = A (XOR) B

=AB’+A’B

This equation can be written as=((AB’+A’B)’)’

Equation of Carry= AB

**Answer to the Pre-Lab Homework:**

1. **Develop the Truth table for a half adder.**

Ans: see the table-1 of half adder.

1. **Develop the truth table for a full adder.**

Ans:

**Table-2: Full Adder**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **Cin** | **S** | **C** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Apparatus:**

1. PMOS,
2. NMOS,
3. IC 7404(Inverter).
4. Connecting wires.
5. Trainer Board

**Experimental Procedure:**

1. Set the circuit for half adder as shown in Fig-2.
2. For each input combination, find the output and place them in a Truth Table. The Truth Table should have two sets of outputs- one ideal and one experimental.

**Experimental Results:**

**Table:**

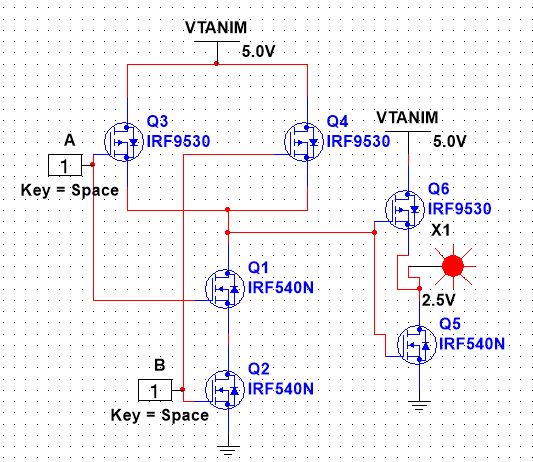
|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Cout** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1(6.2V) |

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Sum** |
| 0 | 0 | 0 |
| 0 | 1 | 1(6.2V) |
| 1 | 0 | 1(6.2V) |
| 1 | 1 | 0 |

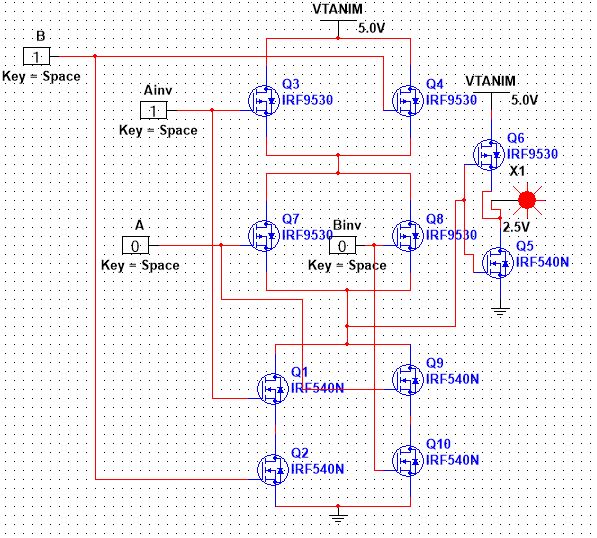
**Table-3:** Half adder carry out table(left) & Half adder Sum table(right).

**Simulation Results:**

**Circuit Diagram:**

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**Fig-3:** Half adder carry out circuit using MULTISIM**.**



**Fig-4:** Half adder sum circuit using MULTISIM.

**Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Cout** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **Sum** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Table-4:** Half adder carry out table(left) & Half adder Sum table(right) using multisim.

**Answer to Report Question:**

* **Document the data acquired from the hardware, from simulation as well as the expected values for the CarryOut and Sum of the Half Adder**

**Ans:** All the documents are attached in above.

**Discussion & conclusion:**

All the apparatus was checked before start of the experiment. All the components were placed according to the circuit figure. That’s why the was done so quickly. The expected result come so quickly. The theoretical and experimental result is same. Learn half adder circuit function in different way.

**References:**

**[1] Lab Manual**