

## Features

- Pin- and function-compatible with CY7C1049B
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 90 \text{ mA}$  at 10 ns
- Low CMOS Standby power
  - $I_{SB2} = 10 \text{ mA}$
- 2.0 V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Pb-free 36-Pin (400-Mil) Molded SOJ package

## Functional Description<sup>[1]</sup>

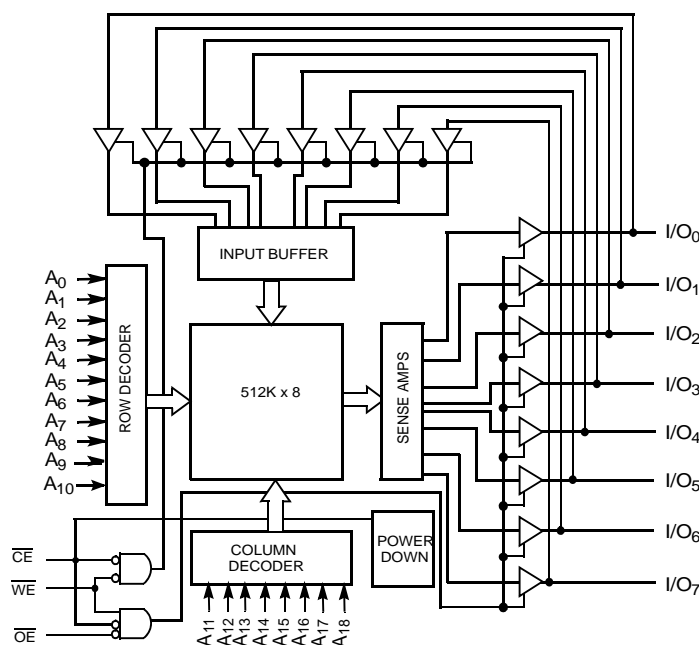
The CY7C1049D is a high-performance CMOS static RAM organized as 512K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1049D is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.

## Logic Block Diagram



## Selection Guide

|                              | -10 | Unit |
|------------------------------|-----|------|
| Maximum access time          | 10  | ns   |
| Maximum operating current    | 90  | mA   |
| Maximum CMOS standby current | 10  | mA   |

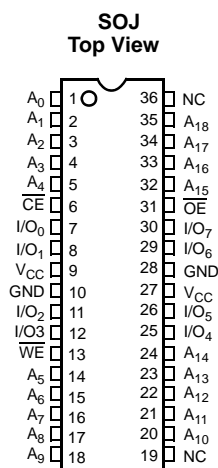
### Note

1. For guidelines on SRAM system design, refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

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## Pin Configuration



## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with

Power Applied ..... –55°C to +125°C

Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[2]</sup> ... –0.5 V to +6.0 V

DC Voltage Applied to Outputs

in High Z State<sup>[2]</sup> ..... –0.5 V to V<sub>CC</sub> + 0.5 V

DC Input Voltage<sup>[2]</sup> ..... –0.5 V to V<sub>CC</sub> + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001 V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

| Range      | Ambient Temperature | V <sub>CC</sub> |
|------------|---------------------|-----------------|
| Industrial | –40°C to +85°C      | 4.5 V–5.5 V     |

## Electrical Characteristics Over the Operating Range

| Parameter                      | Description                                  | Test Conditions  |         | –10  |                       | Unit |
|--------------------------------|--|--|---------|------|-----------------------|------|
|                                |  |  |         | Min. | Max.                  |      |
| V <sub>OH</sub>                | Output HIGH Voltage                          | V <sub>CC</sub> = Min., I <sub>OH</sub> = –4.0 mA  |         | 2.4  | –                     | V    |
| V <sub>OL</sub>                | Output LOW Voltage                           | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA   |         | –    | 0.4                   | V    |
| V <sub>IH</sub> <sup>[2]</sup> | Input HIGH Voltage                           |  |         | 2.0  | V <sub>CC</sub> + 0.5 | V    |
| V <sub>IL</sub> <sup>[2]</sup> | Input LOW Voltage <sup>[2]</sup>             |  |         | –0.5 | 0.8                   | V    |
| I <sub>IX</sub>                | Input Leakage Current                        | GND < V <sub>I</sub> < V <sub>CC</sub>   |         | –1   | +1                    | μA   |
| I <sub>OZ</sub>                | Output Leakage Current                       | GND < V <sub>OUT</sub> < V <sub>CC</sub> ,<br>Output Disabled  |         | –1   | +1                    | μA   |
| I <sub>CC</sub>                | VCC Operating Supply Current                 | V <sub>CC</sub> = Max.,<br>f = f <sub>MAX</sub> = 1/t <sub>RC</sub>  | 100 MHz | –    | 90                    | mA   |
|                                |  |  |         | –    |                       |      |
|                                |  |  | 83 MHz  | –    | 80                    | mA   |
|                                |  |  |         | –    |                       |      |
|                                |  |  | 66 MHz  | –    | 70                    | mA   |
|                                |  |  |         | –    |                       |      |
| 40 MHz                         | –  | 60   | mA      |      |                       |      |
|                                | –  |  |         |      |                       |      |
| I <sub>SB1</sub>               | Automatic CE Power-Down Current —TTL Inputs  | Max. V <sub>CC</sub> , CE > V <sub>IH</sub> , V <sub>IN</sub> > V <sub>IH</sub> or<br>V <sub>IN</sub> < V <sub>IL</sub> , f = f <sub>MAX</sub> |         | –    | 20                    | mA   |
| I <sub>SB2</sub>               | Automatic CE Power-Down Current —CMOS Inputs | Max. V <sub>CC</sub> , CE > V <sub>CC</sub> – 0.3 V,<br>V <sub>IN</sub> > V <sub>CC</sub> – 0.3 V, or V <sub>IN</sub> < 0.3 V, f = 0           |         | –    | 10                    | mA   |

## Capacitance<sup>[3]</sup>

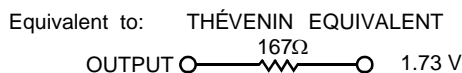
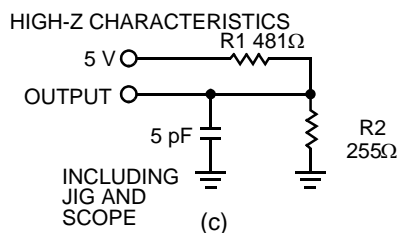
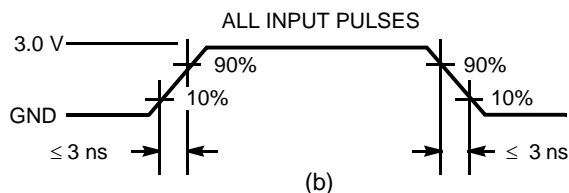
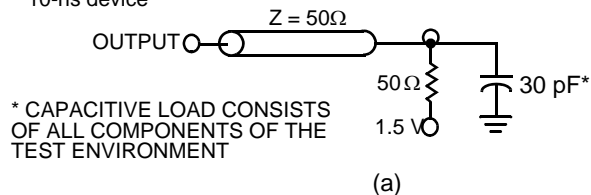
| Parameter | Description       | Test Conditions  | Max. | Unit |
|-----------|-------------------|--|------|------|
| $C_{IN}$  | Input capacitance | $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ ,<br>$V_{CC} = 5.0\text{ V}$ | 8    | pF   |
| $C_{OUT}$ | I/O capacitance   |  | 8    | pF   |

## Thermal Resistance<sup>[3]</sup>

| Parameter     | Description  | Test Conditions  | SOJ Package | Unit               |
|---------------|--|--|-------------|--------------------|
| $\Theta_{JA}$ | Thermal resistance<br>(Junction to Ambient) <sup>[3]</sup> | Still Air, soldered on a 3 × 4.5 inch,<br>four-layer printed circuit board | 57.91       | $^\circ\text{C/W}$ |
| $\Theta_{JC}$ | Thermal resistance<br>(Junction to Case) <sup>[3]</sup>    |  | 36.73       | $^\circ\text{C/W}$ |

## AC Test Loads and Waveforms<sup>[4]</sup>

10-ns device



### Notes

- Minimum voltage is  $-2.0\text{ V}$  and  $V_{IH}(\text{max}) = V_{CC} + 2\text{ V}$  for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

**Switching Characteristics<sup>[5]</sup>** Over the Operating Range

| Parameter                      | Description  | -10  |      | Unit |
|--------------------------------|--|------|------|------|
|                                |  | Min. | Max. |      |
| Read Cycle                     |  |      |      |      |
| t <sub>power</sub>             | V <sub>CC</sub> (typical) to the First Access <sup>[6]</sup> | 100  | –    | μs   |
| t <sub>RC</sub>                | Read Cycle Time  | 10   | –    | ns   |
| t <sub>AA</sub>                | Address to Data Valid  | –    | 10   | ns   |
| t <sub>OHA</sub>               | Data Hold from Address Change                                | 3    | –    | ns   |
| t <sub>ACE</sub>               | CE LOW to Data Valid   | –    | 10   | ns   |
| t <sub>DOE</sub>               | OE LOW to Data Valid   | –    | 5    | ns   |
| t <sub>LZOE</sub>              | OE LOW to Low Z <sup>[8]</sup>                               | 0    | –    | ns   |
| t <sub>HZOE</sub>              | OE HIGH to High Z <sup>[7, 8]</sup>                          | –    | 5    | ns   |
| t <sub>LZCE</sub>              | CE LOW to Low Z <sup>[8]</sup>                               | 3    | –    | ns   |
| t <sub>HZCE</sub>              | CE HIGH to High Z <sup>[7, 8]</sup>                          | –    | 5    | ns   |
| t <sub>PU</sub>                | CE LOW to Power-Up   | 0    | –    | ns   |
| t <sub>PD</sub>                | CE HIGH to Power-Down  | –    | 10   | ns   |
| Write Cycle <sup>[9, 10]</sup> |  |      |      |      |
| t <sub>WC</sub>                | Write Cycle Time   | 10   | –    | ns   |
| t <sub>SCE</sub>               | CE LOW to Write End  | 7    | –    | ns   |
| t <sub>AW</sub>                | Address Set-Up to Write End                                  | 7    | –    | ns   |
| t <sub>HA</sub>                | Address Hold from Write End                                  | 0    | –    | ns   |
| t <sub>SA</sub>                | Address Set-Up to Write Start                                | 0    | –    | ns   |
| t <sub>PWE</sub>               | WE Pulse Width   | 7    | –    | ns   |
| t <sub>SD</sub>                | Data Set-Up to Write End                                     | 6    | –    | ns   |
| t <sub>HD</sub>                | Data Hold from Write End                                     | 0    | –    | ns   |
| t <sub>LZWE</sub>              | WE HIGH to Low Z <sup>[8]</sup>                              | 3    | –    | ns   |
| t <sub>HZWE</sub>              | WE LOW to High Z <sup>[7, 8]</sup>                           | –    | 5    | ns   |

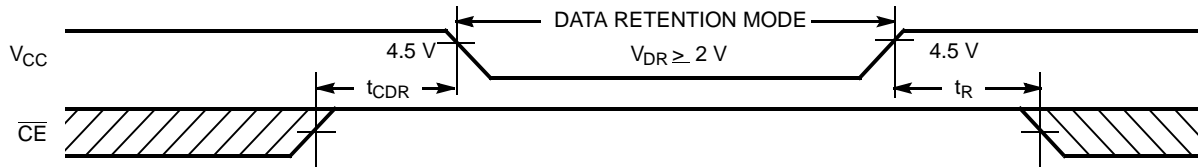
**Data Retention Characteristics** Over the Operating Range

| Parameter              | Description                          | Conditions <sup>[12]</sup>  | Min.            | Max | Unit |
|------------------------|--------------------------------------|---|-----------------|-----|------|
| $V_{\text{DR}}$        | $V_{\text{CC}}$ for Data Retention   |   | 2.0             | –   | V    |
| $I_{\text{CCDR}}$      | Data Retention Current               | $V_{\text{CC}} = V_{\text{DR}} = 2.0 \text{ V}$ ,<br>$\text{CE} \geq V_{\text{CC}} - 0.3 \text{ V}$ | –               | 10  | mA   |
| $t_{\text{CDR}}^{[3]}$ | Chip Deselect to Data Retention Time | $V_{\text{IN}} \geq V_{\text{CC}} - 0.3 \text{ V}$ or $V_{\text{IN}} \leq 0.3 \text{ V}$            | 0               | –   | ns   |
| $t_{\text{R}}^{[11]}$  | Operation Recovery Time              |   | $t_{\text{RC}}$ | –   | ns   |

**Notes**

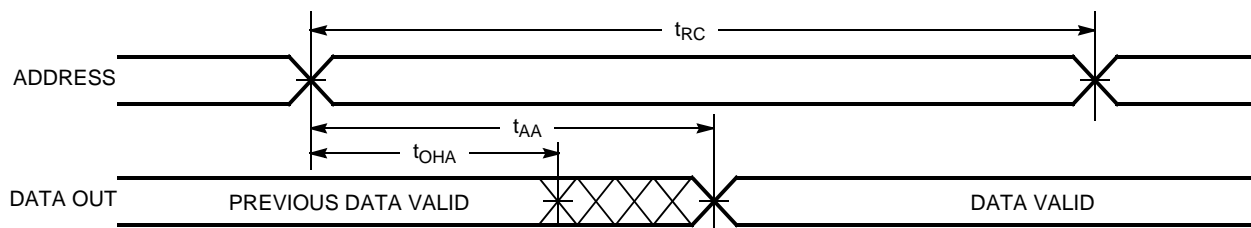
- AC characteristics (except High-Z) for 10-ns parts are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c)
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{\text{OL}}/I_{\text{OH}}$  and 30-pF load capacitance.
- $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at typical  $V_{\text{CC}}$  values until the first memory access can be performed.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
- At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle no. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

## Data Retention Waveform



## Switching Waveforms

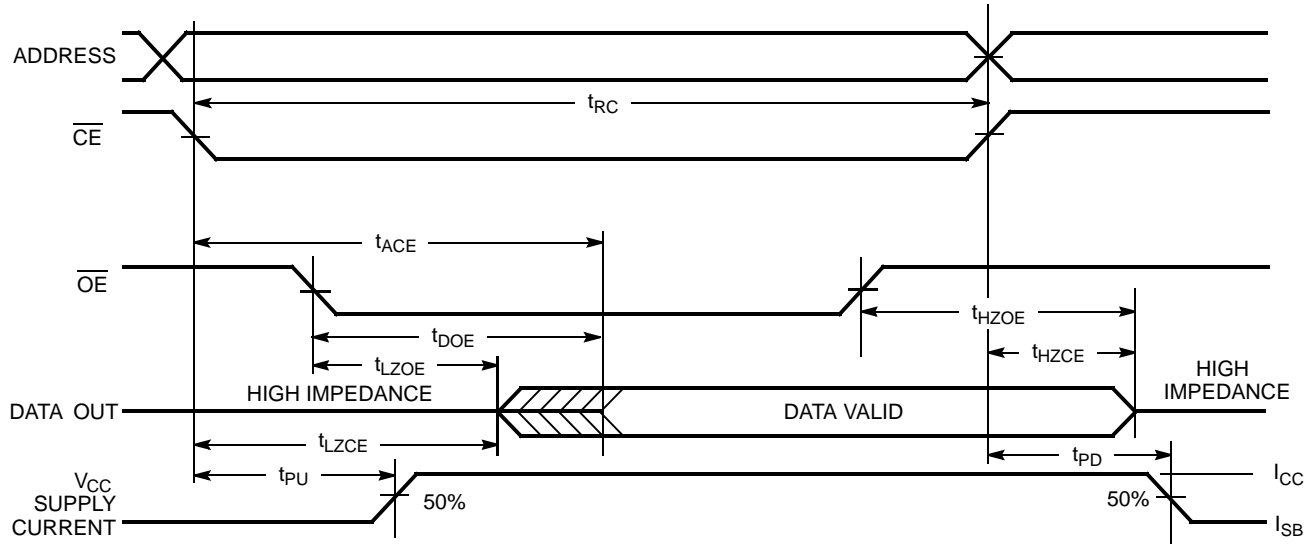
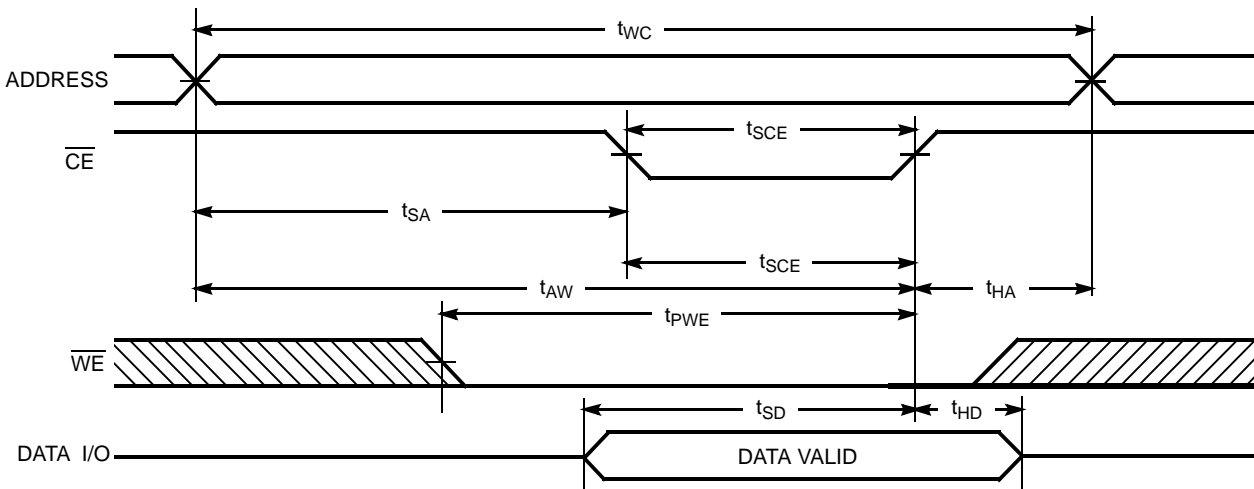
Figure 1. Read Cycle No. 1<sup>[13, 14]</sup>



### Notes

11. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50 \mu s$  or stable at  $V_{CC(min.)} \geq 50 \mu s$
12. No input may exceed  $V_{CC} + 0.5$  V.
13. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
14. WE is HIGH for read cycle.

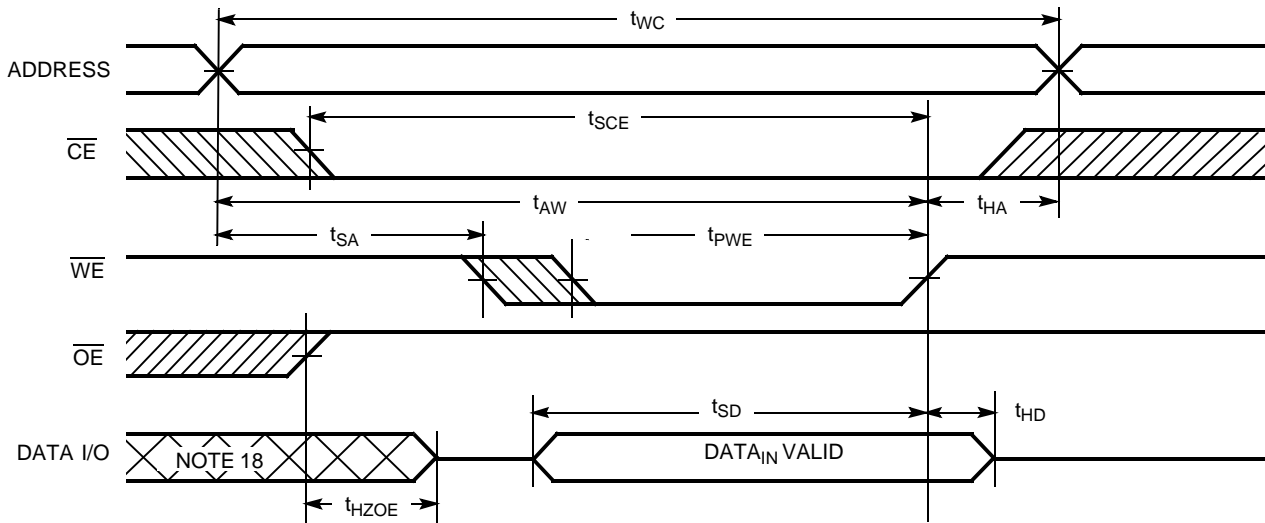
**Switching Waveforms**(continued)

**Figure 2. Read Cycle No. 2 ( $\overline{OE}$  Controlled)**<sup>[14, 15]</sup>

**Figure 3. Write Cycle No. 1 ( $\overline{CE}$  Controlled)**<sup>[16, 17]</sup>

**Notes**

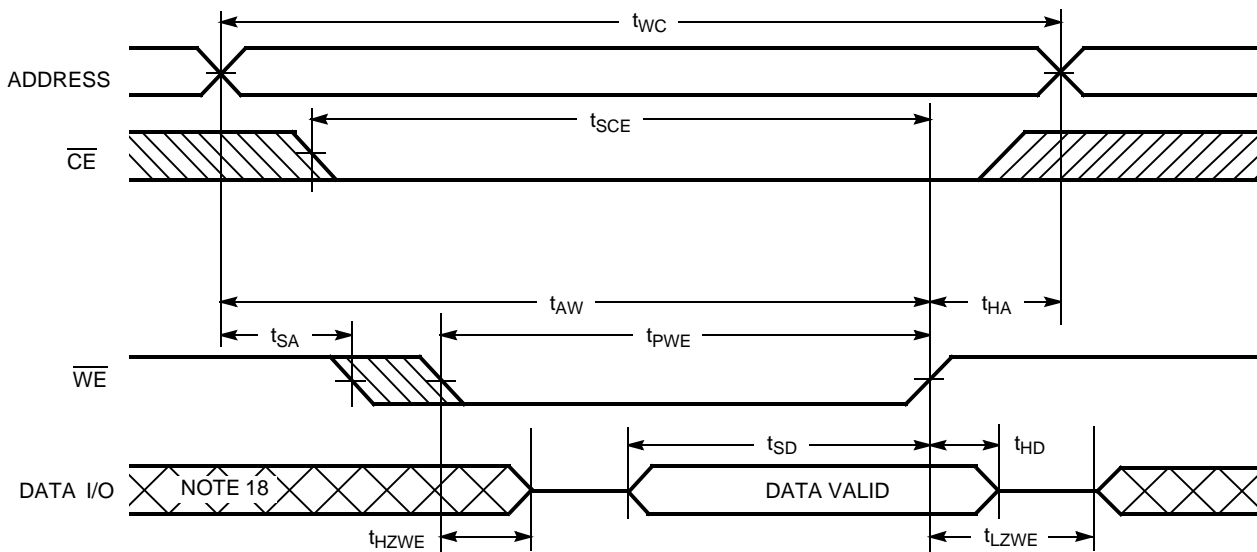
15. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
16. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
17. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

## Switching Waveforms(continued)

**Figure 4. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[16, 17]</sup>**



**Figure 5. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[17]</sup>**





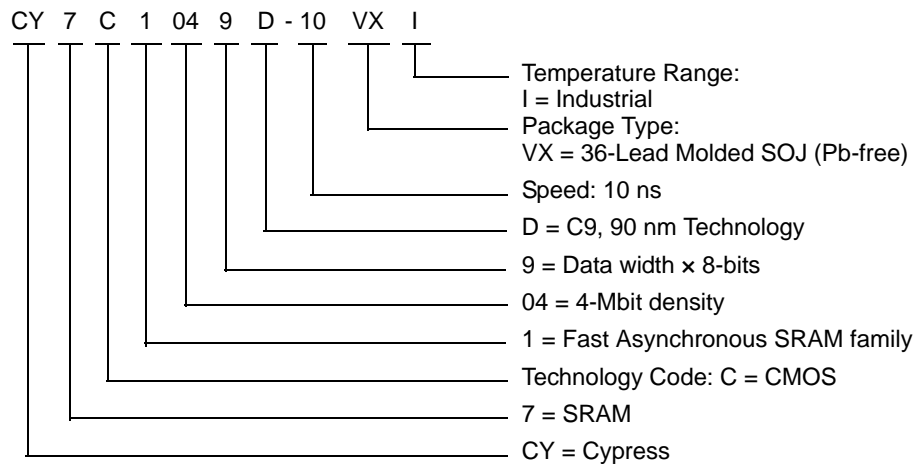
## Truth Table

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | I/O <sub>0</sub> –I/O <sub>7</sub> | Mode                       | Power                |
|-----------------|-----------------|-----------------|------------------------------------|----------------------------|----------------------|
| H               | X               | X               | High-Z                             | Power-down                 | Standby ( $I_{SB}$ ) |
| L               | L               | H               | Data Out                           | Read                       | Active ( $I_{CC}$ )  |
| L               | X               | L               | Data In                            | Write                      | Active ( $I_{CC}$ )  |
| L               | H               | H               | High-Z                             | Selected, Outputs Disabled | Active ( $I_{CC}$ )  |

## Ordering Information

| Speed (ns) | Ordering Code   | Package Diagram | Package Type                           | Operating Range |
|------------|-----------------|-----------------|--|-----------------|
| 10         | CY7C1049D-10VXI | 51-85090        | 36-Lead (400-Mil) Molded SOJ (Pb-free) | Industrial      |

## Ordering Code Definitions



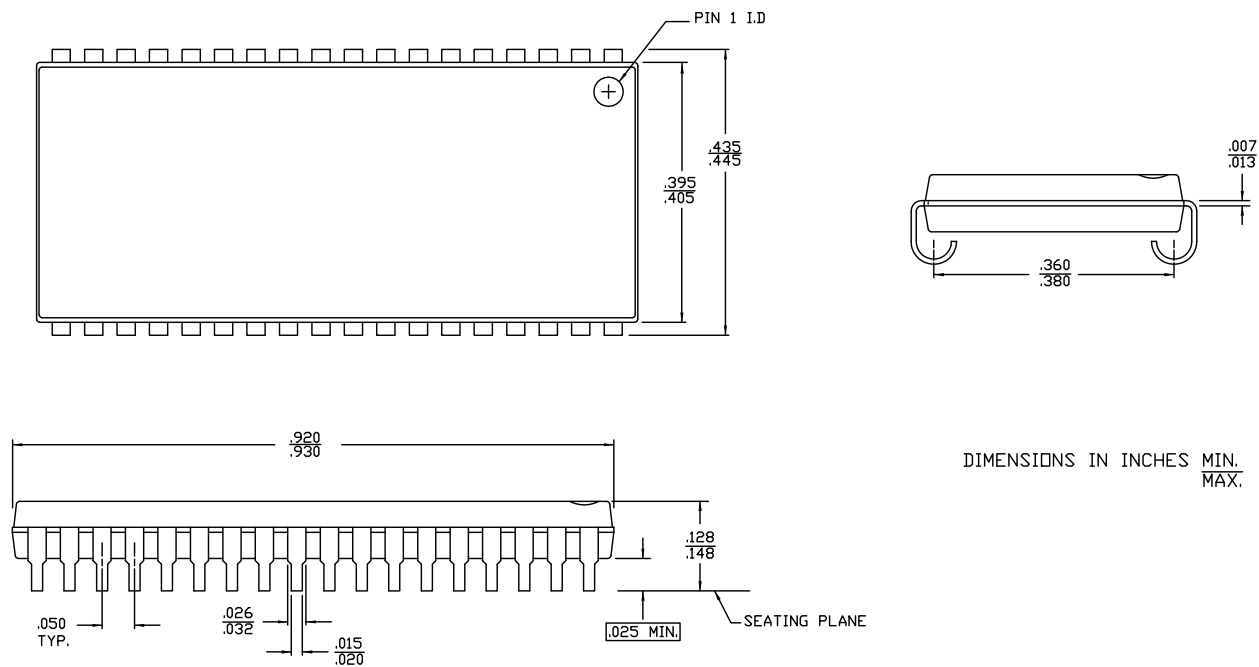
Please contact your local Cypress sales representative for availability of these parts.

### Note

18. During this period the I/Os are in the output state and input signals should not be applied.

## Package Diagram

**Figure 6. 36-Pin (400-Mil) Molded SOJ (51-85090)**



51-85090 \*E

## Acronyms

| Acronym | Description                             |
|---------|---|
| CE      | chip enable                             |
| CMOS    | Complementary metal oxide semiconductor |
| I/O     | Input/output                            |
| OE      | output enable                           |
| SRAM    | Static random access memory             |
| SOJ     | Small Outline J-Lead                    |
| TSOP    | Thin Small Outline Package              |
| VFBGA   | Very Fine-Pitch Ball Grid Array         |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| ns     | nano seconds    |
| V      | Volts           |
| μA     | micro Amperes   |
| mA     | milli Amperes   |
| mV     | milli Volts     |
| mW     | milli Watts     |
| MHz    | Mega Hertz      |
| pF     | pico Farad      |
| °C     | degree Celcius  |
| W      | Watts           |

## Document History Page

| Document Title: CY7C1049D 4-Mbit (512K x 8) Static RAM<br>Document Number: 38-05474 |         |                 |                 |   |
|---|---------|-----------------|-----------------|---|
| Revision  | ECN     | Orig. of Change | Submission Date | Description of Change   |
| **  | 201560  | SWI             | See ECN         | Advance Datasheet for C9 IPP  |
| *A  | 233729  | RKF             | See ECN         | 1.AC, DC parameters are modified as per EROS(Spec # 01-2165)<br>2.Pb-free offering in the 'ordering information'  |
| *B  | 351096  | PCI             | See ECN         | Changed from Advance to Preliminary<br>Removed 17, 20 ns Speed bin<br>Added footnote # 4<br>Redefined I <sub>CC</sub> values for Com'I and Ind'I temperature ranges<br>I <sub>CC</sub> (Com'I): Changed from 67 and 54 mA to 75 and 70 mA for 12 and 15 ns speed bins respectively<br>I <sub>CC</sub> (Ind'I): Changed from 80, 67 and 54 mA to 90, 85 and 80 mA for 10, 12 and 15 ns speed bins respectively<br>Added V <sub>IH(max)</sub> spec in Note# 2<br>Modified Note# 10 on t <sub>R</sub><br>Changed t <sub>SCE</sub> from 8 to 7 ns for 10 ns speed bin<br>Changed reference voltage level for measurement of Hi-Z parameters from ±500 mV to ±200 mV<br>Added Truth Table on page# 6<br>Removed L-Version<br>Added 10 ns parts in the Ordering Information Table<br>Added Lead-Free Product Information<br>Shaded Ordering Information Table |
| *C  | 446328  | NXR             | See ECN         | Converted from Preliminary to Final<br>Removed -12 and -15 speed bins<br>Removed Commercial Operating Range product information<br>Changed Maximum Rating for supply voltage from 7 V to 6 V<br>Updated Thermal Resistance table<br>Changed t <sub>HZWE</sub> from 6 ns to 5 ns<br>Updated footnote #7 on High-Z parameter measurement<br>Replaced Package Name column with Package Diagram in the Ordering Information table   |
| *D  | 3109184 | AJU             | 12/13/2010      | Added <a href="#">Ordering Code Definitions</a> .<br>Updated <a href="#">Package Diagram</a> .  |
| *E  | 3235742 | PRAS            | 04/20/2011      | Updated template.<br>Added Acronyms and Units of measure.   |

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| PSoC                     | <a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>   |
| Touch Sensing            | <a href="http://cypress.com/go/touch">cypress.com/go/touch</a>   |
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### PSoC Solutions

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PSoC 1 | PSoC 3 | PSoC 5

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