SRAM Controller for Intel DE-Series Boards

For Quartus Prime 16.1

1 Core Overview

The SRAM Controller communicates with the 1M × 16 asynchronous CMOS static RAM (SRAM) chip on Intel's DE2-115 Board. It provides a convenient byte-addressable interface for using the SRAM chip on the DE2-115 board.

2 Functional Description

By mapping Avalon® Switch Fabric signals to the SRAM chip, the SRAM Controller enables users to read or write the SRAM from a master device (such as the Nios® II processor) as a normal memory operation. The Avalon Switch Fabric handles addressing automatically and 8, 16 and 32-bit read/write transfers are supported.

Because the data inside the SRAM Controller are registered, for 8-bit or 16-bit data, there will be two clock cycles of latency for a read operation and one clock cycle of latency for a write operation. For 32-bit data, the Avalon Switch Fabric automatically breaks the data into two 16-bit words and transfers them one by one. As a result, there will be a delay of five clock cycles for reading 32-bit data and a delay of two clock cycles for writing 32-bit data to the SRAM.

Below shows two example timing diagrams for reading and writing 32-bit data. Figure 1 shows writing 0xAAAABBBB and 0xCCCCDDDD to SRAM address 0x00000000 and 0x00000004, and Figure 2 shows how 0xAAAABBBB is read from the SRAM.

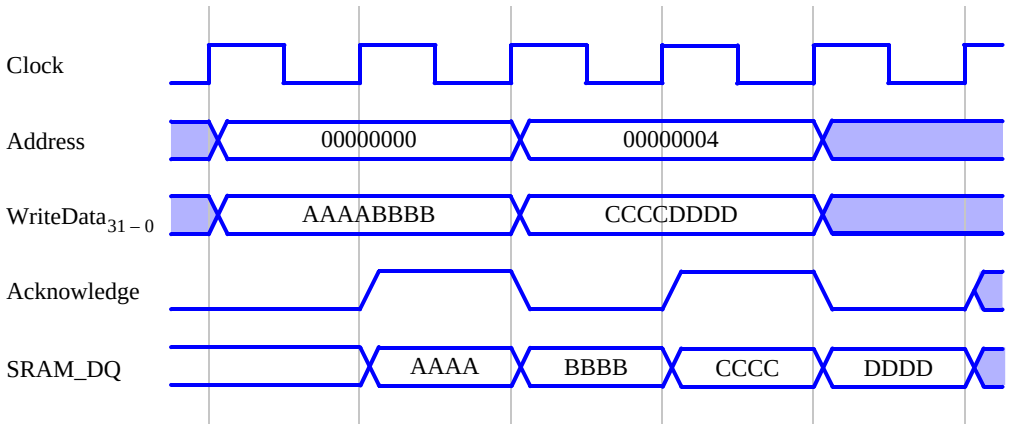

Figure 1. Timing diagram of writing 32-bit data to the SRAM

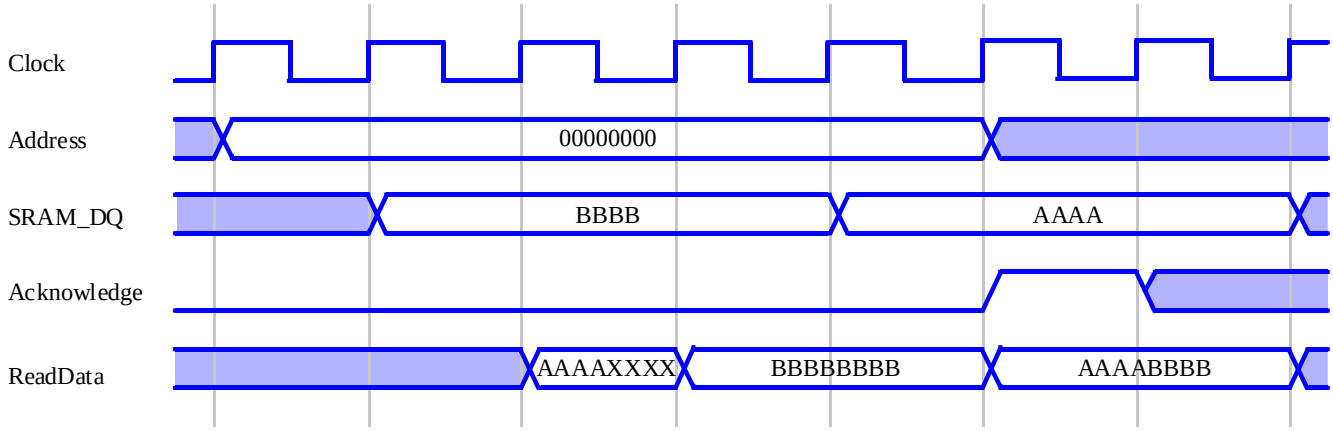

Figure 2. Timing diagram of reading 32-bit data from the SRAM

The SRAM Controller supports a clock frequency of 50 MHz, which is readily available on the DE2-115 Board.

3 Instantiating the Core

The SRAM Controller can be instantiated in a system using Qsys or as a standalone component from the IP Catalog within the Quartus II software. There is no need to configure the controller. Once instantiated the user can use the SRAM in the same way as using an On-Chip Memory. Any read or write operation to an address within SRAM Controller's address range will be read or written to the SRAM on the DE2-115 boards. Note that the SRAM Controller has a longer read/write latency than the On-Chip Memory and needs two transfers for 32-bit data, hence it is not recommended for designs that require fast memory response.

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