Neil Thanawala

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EDUCATION

University of California, Irvine
Masters of Science in Computer Engineering Sep '19 – Dec'20
Relevant Coursework: Computer Architecture, Design and Analysis of Algorithms, High Performance Architecture

Birla Institute of Technology and Science Pilani, Goa
Bachelor of Engineering in Electronics and Instrumentation (GPA: 7.95/10) Aug'15 – May'19
Relevant Coursework: Computer Architecture, Digital Design, Microprocessors, Analog and Digital VLSI Design, Neural Networks, Software for Embedded Systems, Mobile Telecommunication Networks, C Programming

TECHNICAL PROFICIENCY

Languages: C++, Verilog, Python, SystemVerilog, Assembly Level Programming
Scripting: Python, Perl, Shell, Tcl
Methodology: UVM
Applications and Tools: Xilinx Vivado, ModelSim, GitHub, Spyglass, Synopsys VCS, QTSpim, Linux

COMPUTER ENGINEERING EXPERIENCE

Infinera India *- ASIC Design Intern* Jul '18 – Dec'18

Digital Design of InfnScope

- Designed the RTL of a four-stage pipelined digital logic to probe signals from other on-chip modules and view their waveform on screen and implemented the same in Verilog.
- Created a customizable API for processor interface to read inputs from the user in C++.
- Majorly impacted debugging of faulty chips by recognizing the erroneous modules.

Verification of the i2c Bus protocol

- Built a UVM testbench from scratch to verify the communication of two microcontrollers on the i2c bus and wrote test cases for functional coverage.
- Executed the logic of sequencer, driver, monitor using SystemVerilog and created a UVM interface. This project was essential to learn the fundamentals of verification using UVM.

G.U.I.D.E – GUI Debug Environment – Infinera Hackathon 2018

- Developed a GUI based application using Python to perform register read, register write commands on FPGA.
- Saved company 10% time on company projects as it gave ASIC engineers direct access to conduct tests on FPGA bypassing Validation tests.

RELEVANT PROJECTS

Pipelined Processor Mar'19 – May'19

- Implemented a four-stage pipelined processor in Verilog that supports data transfer (mov), addition (add) and Unconditional Jump (J) instructions.
- The processor implements forwarding to resolve data hazards.

Implementation of Processor Datapath Mar'19 – May'19

- Designed and implemented (in Verilog) datapath and control unit for a single cycle MIPS like processor (including instruction memory) which has two classes of instructions - Immediate type (I Type) and Register Type (R Type).

Floating Point Adder in a RISC Processor Feb'19 – Apr'19

- Developed the architecture of 32-bit floating point addition in a RISC Processor using Verilog. Simulated the design in ModelSim software to verify the design.

Image de-raining using Deep Residual Learning Sep'17 – Dec'17

- Rain is treated as Gaussian noise. The aim of the project was to remove this noise using convolutional neural networks using a custom dataset in Python.
- Used deep residual networks and obtained 76% accuracy.