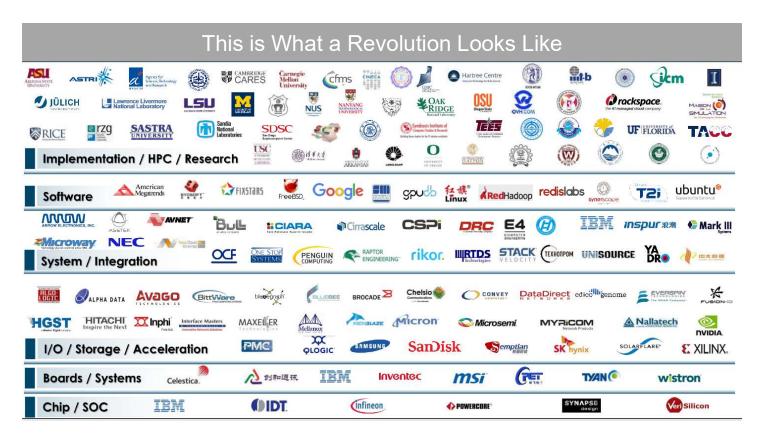


IBM POWER Linux

IBM OpenPOWER – Over 260 Members



Linux Applications on POWER

HPC

CHARMM miniDFT **GROMACS** CTH **BLAST** NAMD **AMBER Bowtie BWA** RTM **FASTA GAMESS** WRF **HMMER HYCOM GATK** SOAP3 HOMME LES STAC-A2 SHOC MiniGhost Graph500 AMG2013 OpenFOAM llog







100,000+ Packages in Linux Distributions on Power







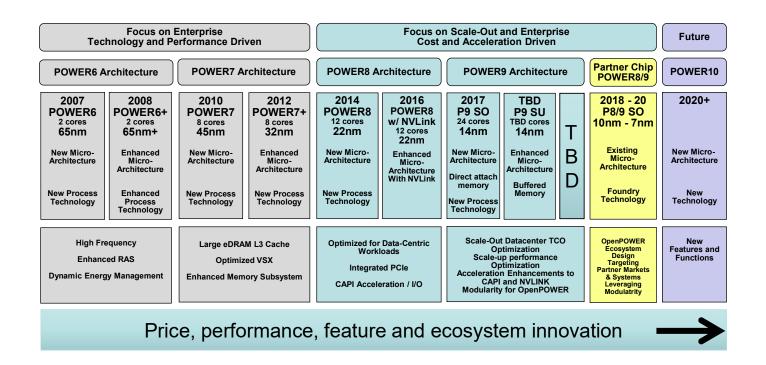
Major Linux Distros







Power Processor Roadmap



Source: http://openpowerfoundation.org/presentations/brad-mccredie-board-advisor-ibm/

Memory Bandwidth? IO? Cores? Flops?

What does it Mean? Better Application Performance

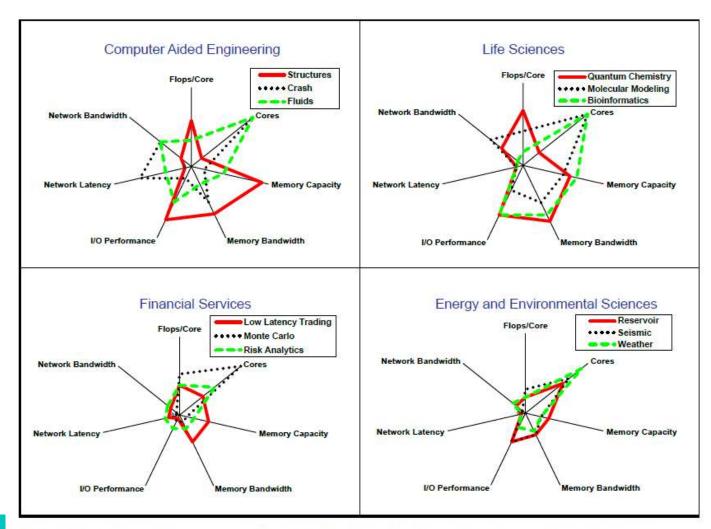


Figure 4: Application Performance Characteristics Mapped to Seven Key Cluster System Features



POWER9 – Premier Acceleration Platform

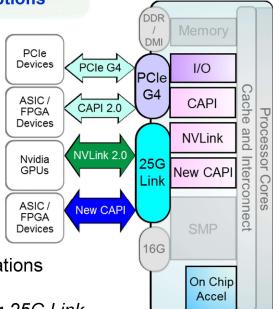
Extreme Processor / Accelerator Bandwidth and Reduced Latency
Coherent Memory and Virtual Addressing Capability for all Accelerators
OpenPOWER Community Enablement – Robust Accelerated Compute Options

State of the Art I/O and Acceleration Attachment Signaling

- PCIe Gen 4 x 48 lanes 192 GB/s duplex bandwidth
- 25G Link x 48 lanes 300 GB/s duplex bandwidth

Robust Accelerated Compute Options with OPEN standards

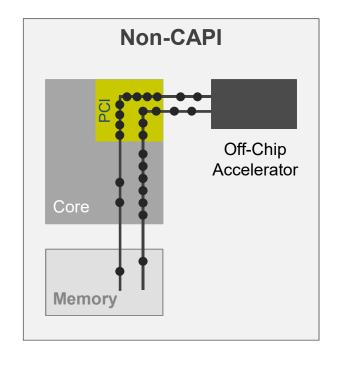
- On-Chip Acceleration Gzip x1, 842 Compression x2, AES/SHA x2
- CAPI 2.0 4x bandwidth of POWER8 using PCle Gen 4
- NVLink 2.0 Next generation of GPU/CPU interconnect
 - Up to 2x bandwidth of NVLink1.0
 - Easier programming model for complex analytic & cognitive applications
 - Coherency, virtual addressing, low overhead communication
- OpenCAPI 3.0 High bandwidth, low latency and open interface using 25G Link

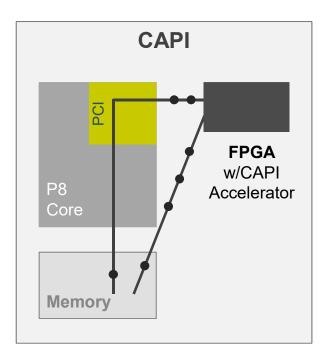


POWER9

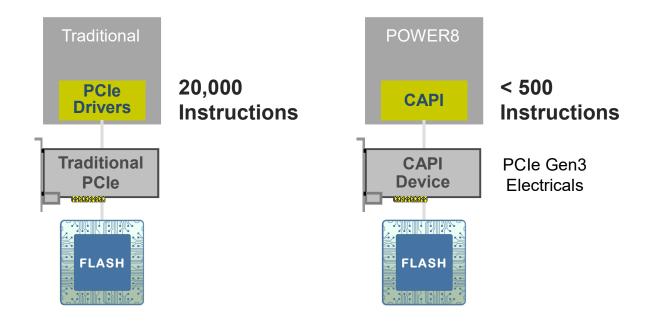
PowerAccel

Coherent Accelerator Processor Interface





CAPI Lowers Flash Latency



IBM CAPI Roadmap

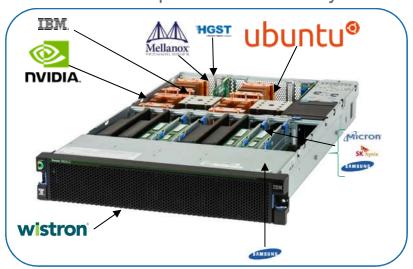
Feature	CAPI	CAPI 2.0	OpenCAPI 3.0	OpenCAPI 4.0
CPU Generation	POWER8	POWER9	POWER9	Post-POWER9
PSL Location	FPGA/ASIC	FPGA/ASIC	Processor	Processor
Native DMA	No	Yes	Yes	Yes
Native Atomic Ops	No	Yes	Yes	Yes
Interface	PCIe (8 Gbps)	PCle (16 Gbps)	25 Gbps	32 Gbps
# Lanes per port	x8	x16	x 8*	x4, x8, x16, x32
BW per port	8+8 GB/s	32+32 GB/s	25+25 GB/s	Up to 128+128 GB/s
POWER Systems	All P8 models	All P9 models	Most P9 models	TBD

^{*}Note: ports may be bonded to multiply bandwidth

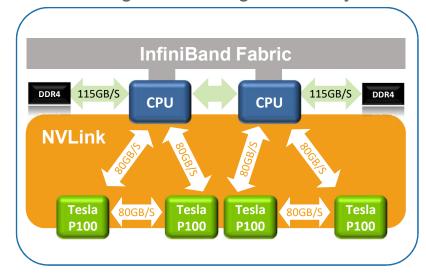
10GbE		HP Dual Port 10GbE SFP+ HP Dual Port 10GbE SR	EC38 / EL53 EC2N / EL54		Connect X:3
	Sec. Sec.	LP Dual Port 10GbE SFP+ LP Dual Port 10GbE SR	EC37 / EL3X EC2M / EL40	- x8	
10/ 25 GbE		LP Dual Port 10/25GbE SFP+	EKAU	x8	Connect X 4 Lx
40GbE	HP Dual Port 40GbE QSFP EC3B			Connect X:3	
	To the last	LP Dual Port 40GbE QSFP	ЕСЗА	x8	Connect A J
100GbE	LP Single Port 100GbE QSFP28 EKAM				
		LP Dual Port 100GbE QSFP28 HP Dual Port 100GbE QSFP28	EC3L EC3M	x16	Connect X:4
100GbE / EDR	HE	LP Dual Port 100GbE / EDR QSFP28	EKAL]	
FDR	THE SHOP N	HP Dual Port FDR QSFP	EC33 / EL50	×16	Connect·IB
	THE	LP Dual Port FDR QSFP	EC32 / EL3D		
EDR		HP Single Port EDR QSFP28 HP Dual Port EDR QSFP28	EC3U EC3F	- x16	Connect X:4
		LP Single Port EDR QSFP28 LP Dual Port EDR QSFP28	EC3T EC3E		

GPU & POWER

Infused with OpenPOWER Ecosystem

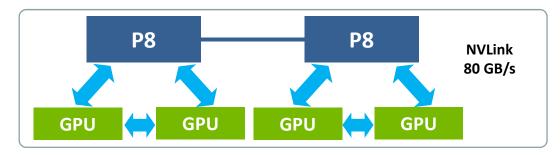


Designed for Programmabilty



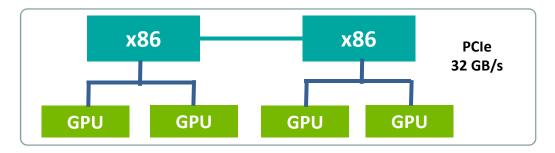
- 2.5X the CPU:GPU Interface Bandwidth
- Tight coupling: strong CPU: strong GPU performance
- Equalizing access to memory for all kinds of programming
- Closer programming to the CPU paradigm

POWER8 NVLink Server



No NVLink between CPU & GPU

for x86 Servers: PCIe Bottleneck





IBM.