DEPT. of Computer **Science Engineering**

SRM IST, Kattankulathur – 603 203

Sub Code & Name: 18CSS201J - ANALOG AND DIGITAL ELECTRONICS

Experiment No	**07**
Title of Experiment	**Design and implementation of 2 bit comparator**
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Date of Experiment	04/10/2020

Mark Split Up

S.No	Description	Maximum Mark	Mark Obtained
1	Oral Viva / Online Quiz	5	
2	Circuit Connection and Execution	10	
3	Verification of truth table	5	
	Total	**20**	

Staff Signature with date

7. Design and implementation of Magnitude Comparator Combinational circuits using simulation package

Aim

To Design a magnitude comparator using Multisim software and to verify its truth table.

Apparatus / Software Required:

MULTISIM SOFTWARE

Theory:

A magnitude digital comparator is a combinational circuit that compares two digital or binary numbers in order to find out whether one binary number is equal, less than or greater than the other binary number. We logically design a circuit for which we will have two inputs one for A and other for B and have three output terminals, one for A > B condition, one for A = B condition and one for A < B condition.

Figure-1: Block Diagram of Comparator

2-Bit Magnitude Comparator:

A comparator used to compare two binary numbers each of two bits is called a 2-bit magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to and greater than between two binary numbers.

Truth Table:

The truth table for a 2-bit comparator is given below:

INPUT				OUTPUT		
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Figure-2: Truth Table of 2-Bit Comparator

The logical expressions for each output can be expressed as follows:

$A > B : A_1B_1' + A_0B_1'B_0' + A_1A_0B_0'$

$A = B : A_1'A_0'B_1'B_0' + A_1'A_0B_1'B_0 + A_1A_0B_1B_0 + A_1A_0'B_1B_0'$

$: A_1'B_1' (A_0'B_0' + A_0B_0) + A_1B_1 (A_0B_0 + A_0'B_0')$

$: (A_0B_0 + A_0'B_0') (A_1B_1 + A_1'B_1')$

$: (A_0 \text{ Ex-Nor } B_0) (A_1 \text{ Ex-Nor } B_1)$

$A < B : A_1'B_1 + A_0'B_1B_0 + A_1'A0'B0$

Logical Diagram:

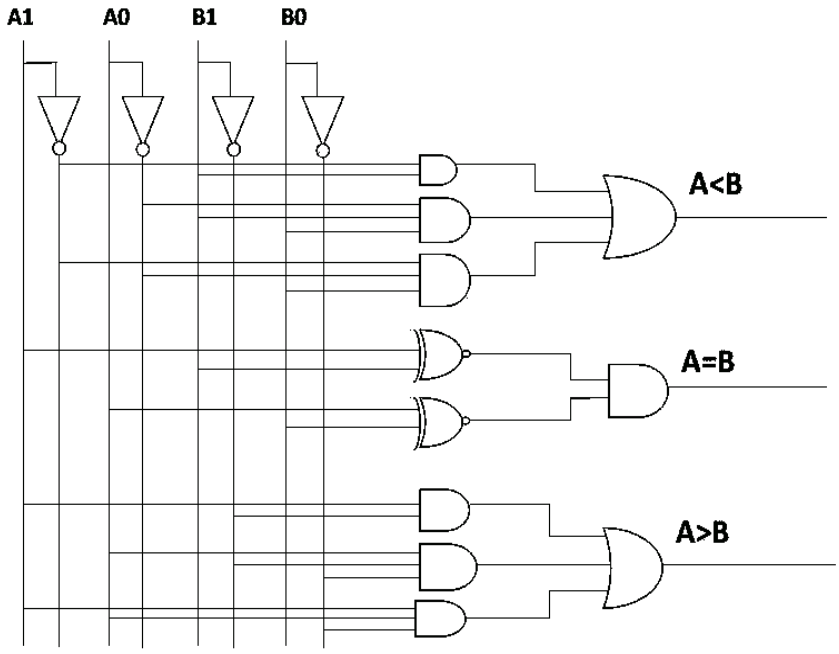


Figure-3: Logic Circuit of 2-Bit Magnitude Comparator

Multisim Diagram:

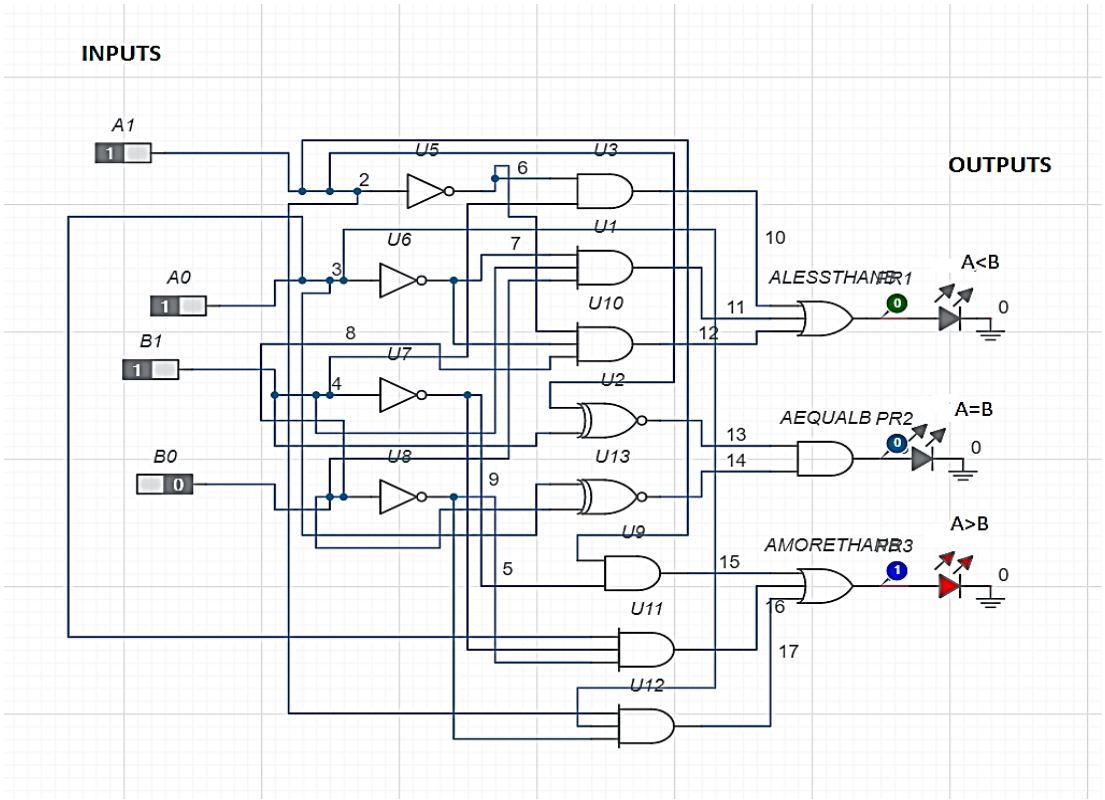
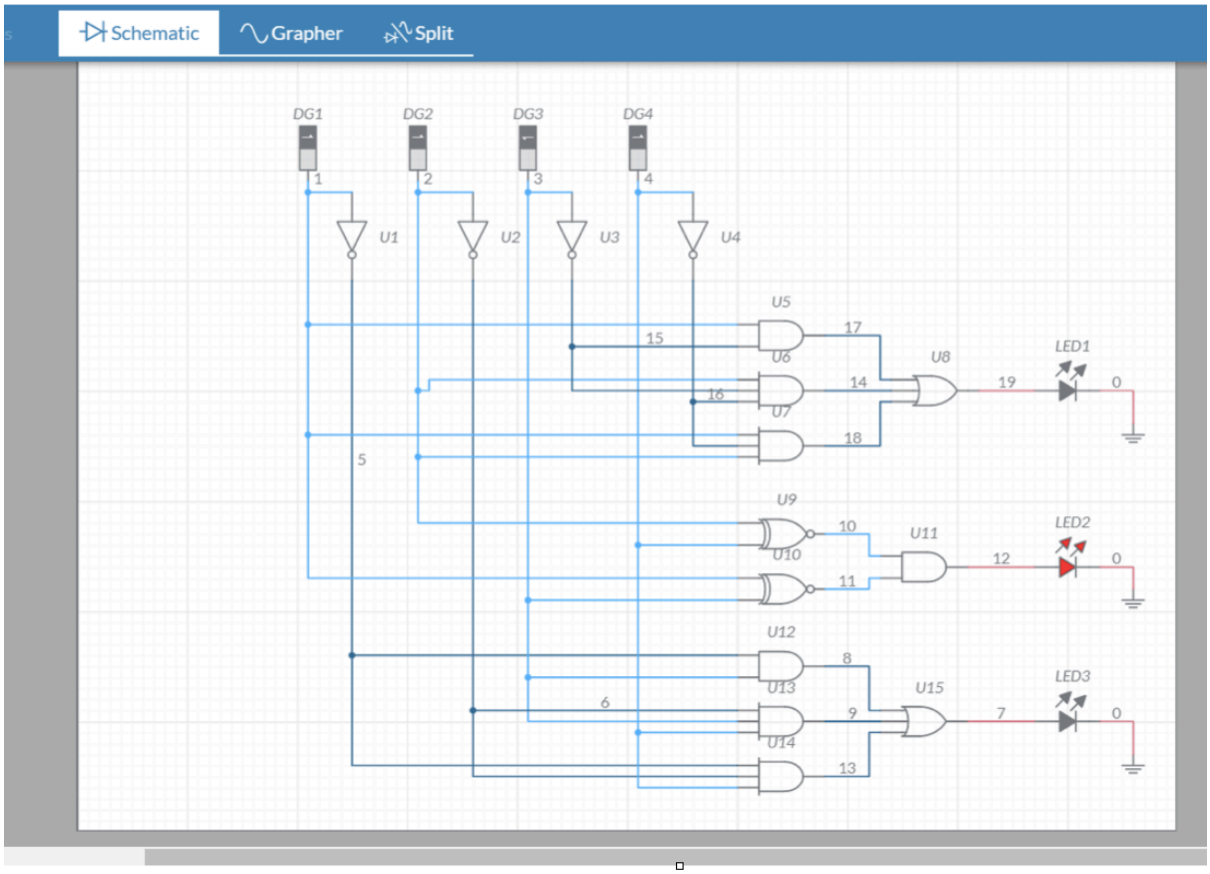


Figure-4: Multisim Circuit of 2-Bit Magnitude Comparator

Simulation diagram:



Input:

A0 : on

A1 : on

B0 : on

B1 : on

Output:

A=B

Result:

Thus the 2 bit magnitude comparator was designed and verified with the truth table using Multisim software.