



Department of

Computer Science

Engineering

SRMIST, Kattankulathur - 603 203

Sub Code & Name: 18CSS201J - ANALOG AND DIGITAL ELECTRONICS

Experiment No	09
Title of Experiment	Implementation of SISO, SIPO, PISO and PIPO shift registers using Flip Flops
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Register Number	RA19110030010094
Date of Experiment	17/10/2020

Mark Split Up

S.No	Description	Maximum Mark	Mark Obtained
1	Oral Viva / Online Quiz	5	
2	Execution	10	
3	Model Calculation / Result Analysis	5	
Total		20	

Staff Signature with date

Experiment No: 9

Date:

Implementation of SISO, SIPO, PISO and PIPO shift registers using Flip Flop

AIM:

To Implement SISO, SIPO, PISO and PIPO shift registers using Flip Flop.

APPARATUS REQUIRED

S.N o	Apparatus	Type	Range	Quantity
1)	D Flip Flop			4
2)	LED			4
3)	Switch			4
4)	DC Power Source			1
5)	Digital Clock			1

Software Required:

<https://www.multisim.com/>

THEORY

A D-type flip-flop is a clocked flip-flop which has two stable states. A D-type flip-flop operates with a delay in input by one clock cycle. Thus, by cascading many D-type flip-flops delay circuits can be created, which are used in many applications such as in digital television systems.

A D-type flip-flop is also known as a D flip-flop or delay flip-flop. A D-type flip-flop consists of four inputs:

- Data input
- Clock input
- Set input
- Reset input

It also has two outputs, with one being logically inverse of other. The data input is either logic 0 or 1, meaning low or high voltage. The clock input helps in synchronizing the circuit to an external signal. The set input and reset input are mostly held low. A D-type flip-flop can have two possible values. When input $D = 0$, the flip-flop undergoes a reset, which means the output would be set to 0. When input $D = 1$, the flip-flop does a set, which makes the output 1. There are several applications in which a D-type flip-flop is used, such as in frequency dividers and data latches.

Serial-in to Serial-out (SISO) Shift Register

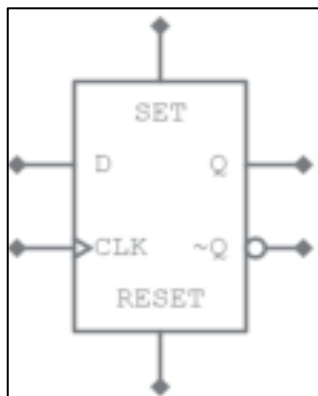
This **shift register** is very similar to the SIPO above, except were before the data was read directly in a parallel form from the outputs Q_A to Q_D , this time the data is allowed to flow straight through the register and out of the other end. Since there is only one output, the DATA leaves the shift register one bit at a time in a serial pattern, hence the name **Serial-in to Serial-Out Shift Register** or **SISO**.

The SISO shift register is one of the simplest of the four configurations as it has only three connections, the serial input (SI) which determines what enters the left hand flip-flop, the serial output (SO) which is taken from the output of the right hand flip-flop and the sequencing clock signal (Clk). The logic circuit diagram below shows a generalized serial-in serial-out shift register.

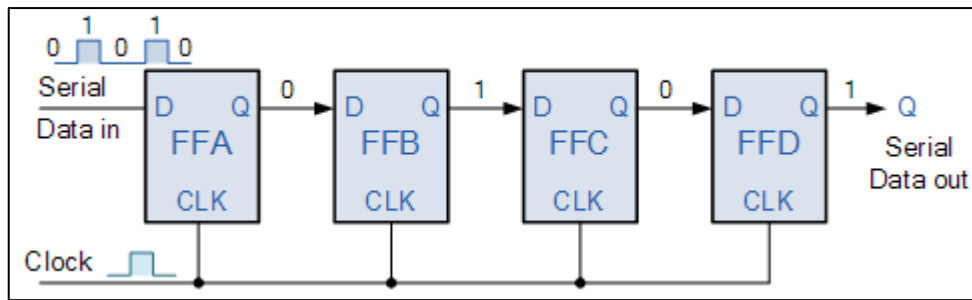
SISO PROCEDURE

1. Log in Multisim Live Online Circuit Simulator.
2. Built-in D Flip Flop is available in the below link.
<https://www.multisim.com/content/TU4wEJ8VgRsRNyxeecQ3Wd/d-flip-flop/open/>
3. Connect four D flip flops in cascaded form.
4. Connect LED at the output 'Q' terminal of fourth flip flop.
5. Connect common ground for the 'Reset' pin for four D flip flops and leave the 'set' pin of all four D flip flops floating.
6. Give input to first flip flop using Digital Switch (Select Digital Switch Digital components list) , For Clock signal generation use digital switch itself for all four flip flops.
7. Observe the movement of input from one flip flop to another by Switching on and off the clock digital switch, if input is set as '1', after four clock pulses you can observe LED at the fourth flip flop will be 'ON' this shows the movement of logic '1' from first flip flop to fourth flip flop.
8. Save the file by clicking the file navigation menu at the left top and save with a file name.
9. Run the simulation change the value of the switches to verify the truth table.

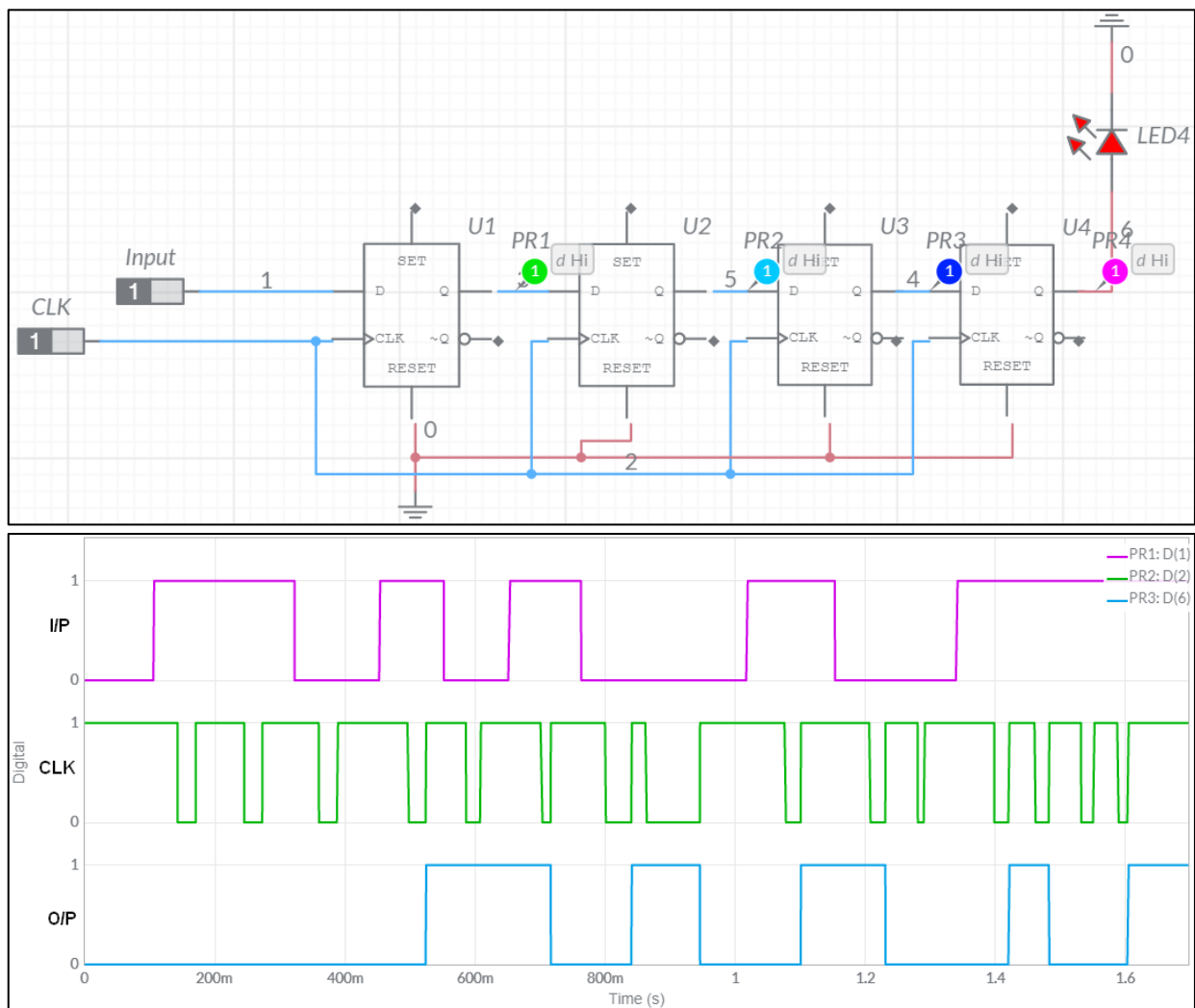
PIN DIAGRAM:



4-bit Serial-in to Serial-out Shift Register

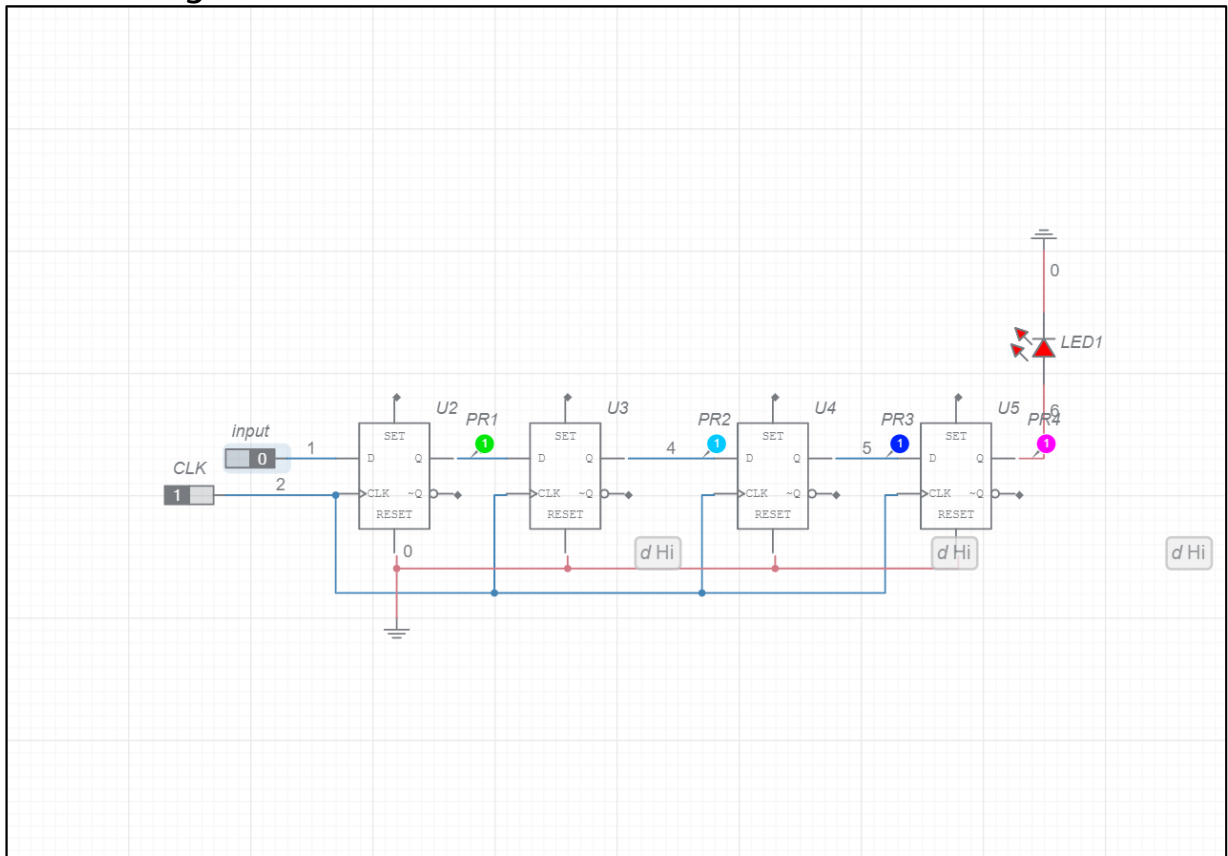


SISO CIRCUIT DIAGRAM in Multisim:

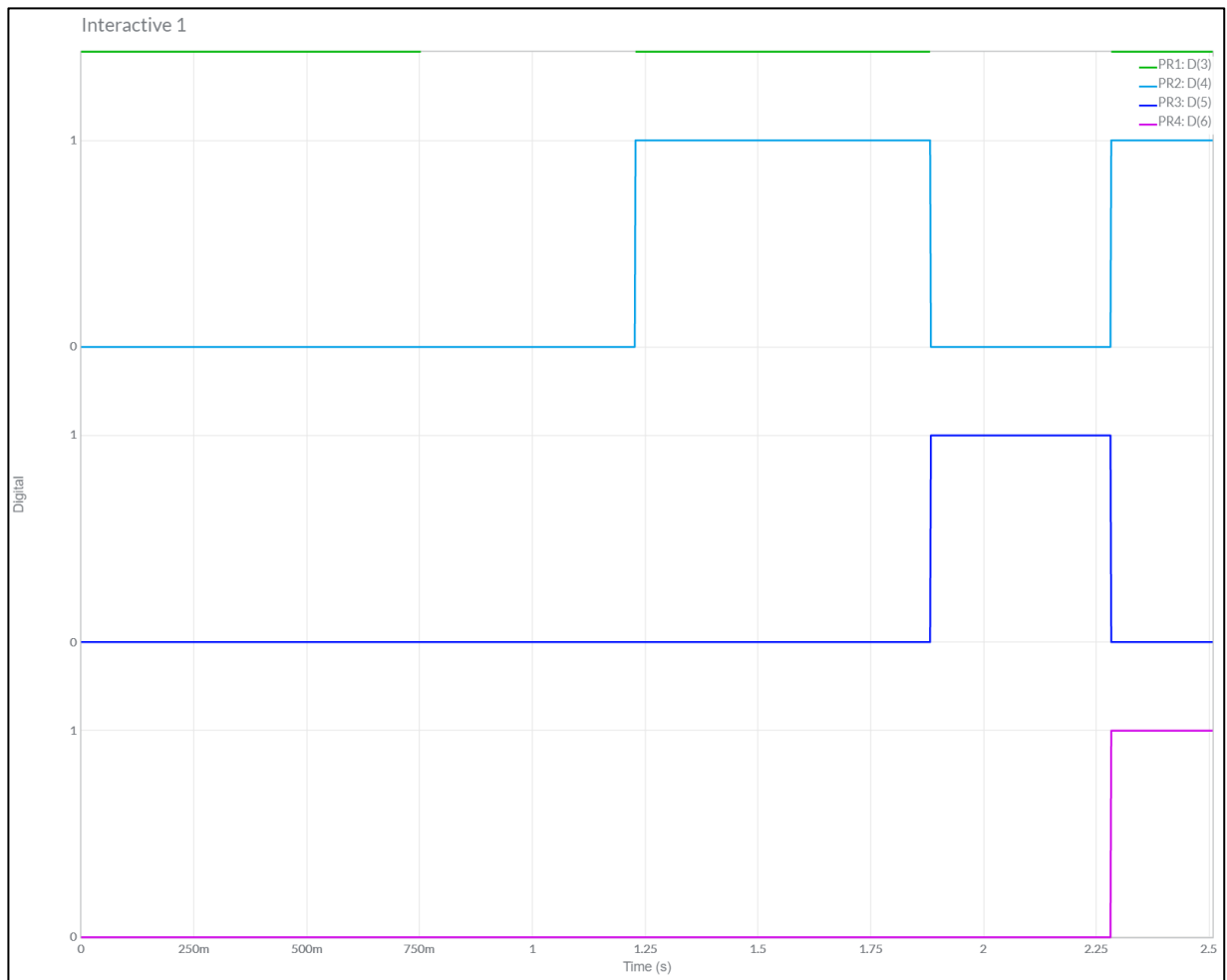


SIMULATION RESULTS

Circuit Diagram

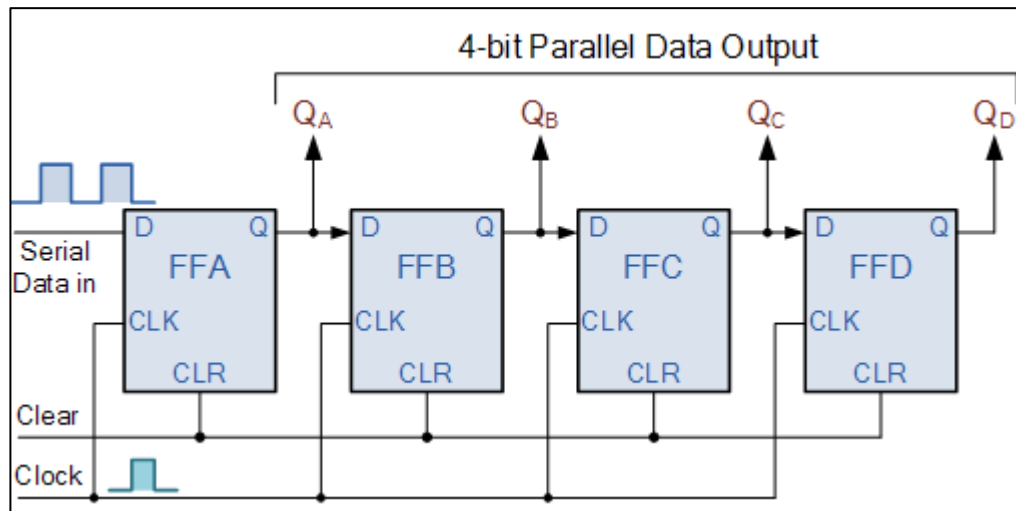


Timing Diagram



Serial-in to Parallel-out (SIPO) Shift Register

4-bit Serial-in to Parallel-out Shift Register



Theory:

The operation is as follows. Lets assume that all the flip-flops (FFA to FFD) have just been RESET (CLEAR input) and that all the outputs QA to QD are at logic level “0” ie, no parallel data output.

If a logic “1” is connected to the DATA input pin of FFA then on the first clock pulse the output of FFA and therefore the resulting QA will be set HIGH to logic “1” with all the other outputs still remaining LOW at logic “0”. Assume now that the DATA input pin of FFA has returned LOW again to logic “0” giving us one data pulse or 0-1-0.

The second clock pulse will change the output of FFA to logic “0” and the output of FFB and QB HIGH to logic “1” as its input D has the logic “1” level on it from QA. The logic “1” has now moved or been “shifted” one place along the register to the right as it is now at QA.

When the third clock pulse arrives this logic “1” value moves to the output of FFC (QC) and so on until the arrival of the fifth clock pulse which sets all the outputs QA to QD back again to logic level “0” because the input to FFA has remained constant at logic level “0”.

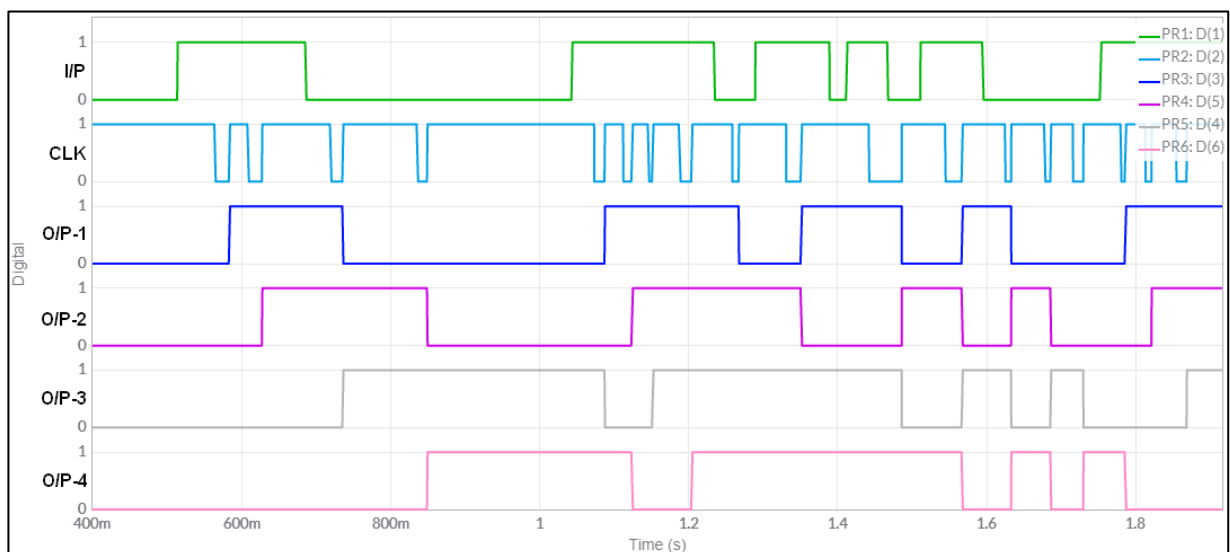
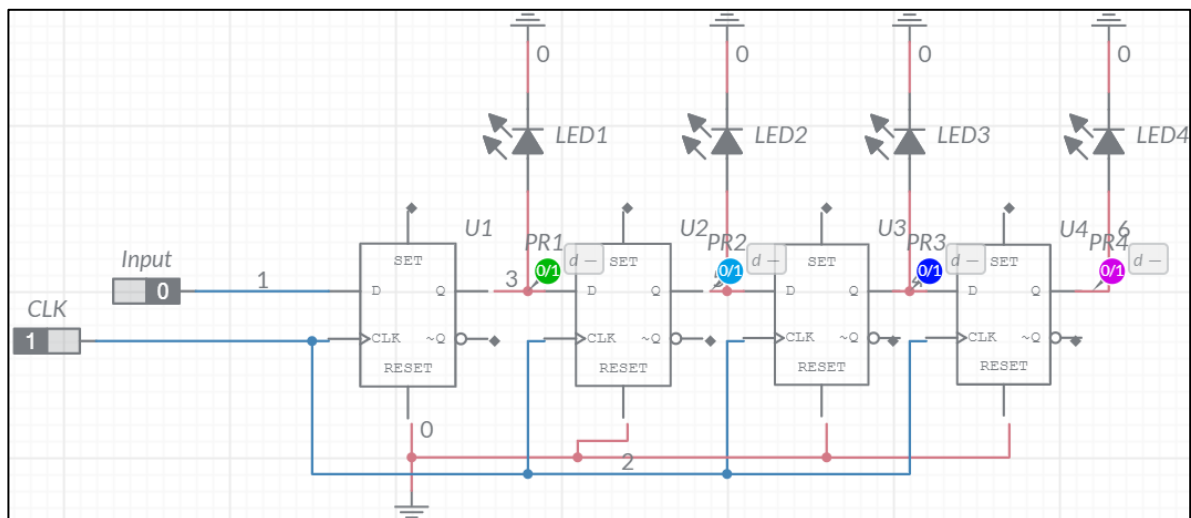
The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of QA to QD.

Then the data has been converted from a serial data input signal to a parallel data output. The truth table and following waveforms show the propagation of the logic “1” through the register from left to right as follows.

Data Movement

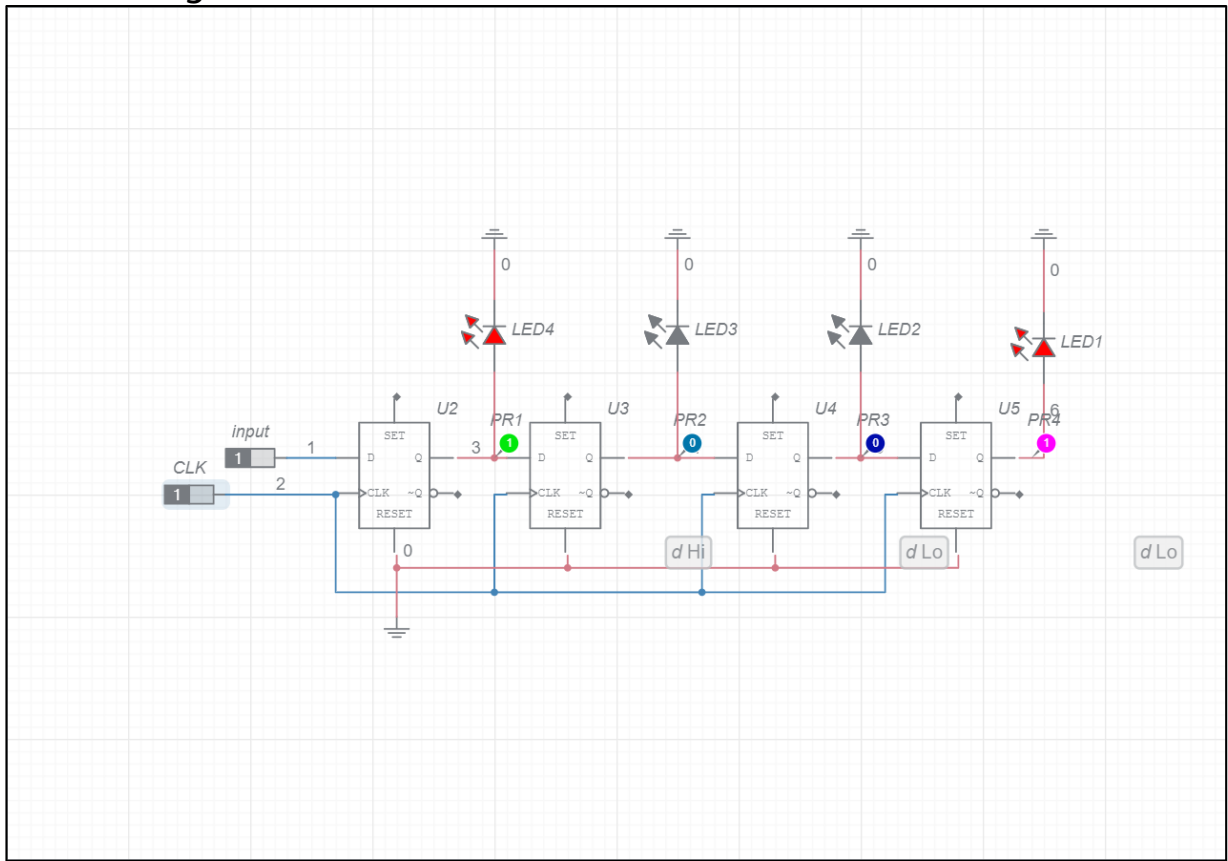


SIPO CIRCUIT DIAGRAM in Multisim:

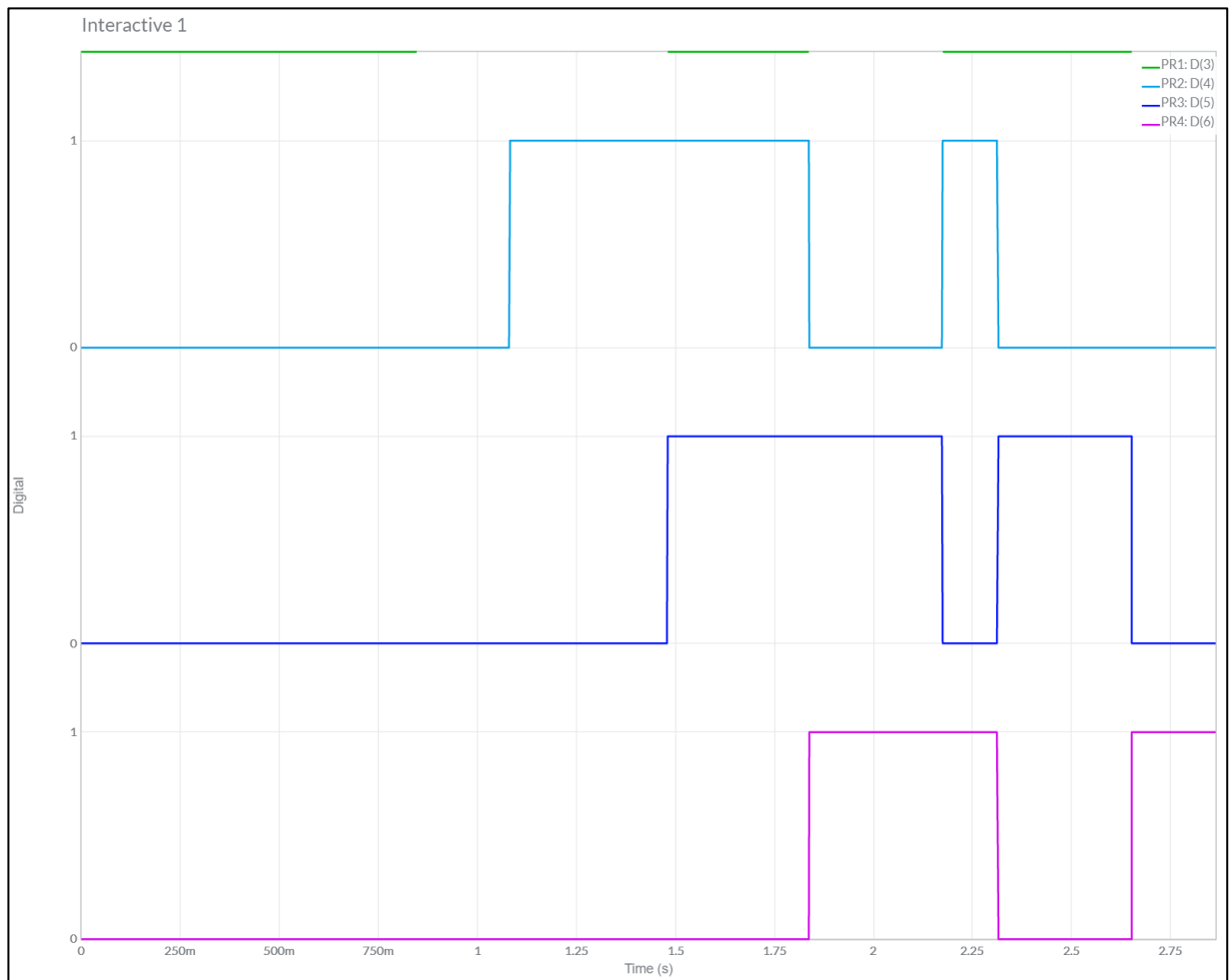


SIMULATION RESULTS

Circuit Diagram



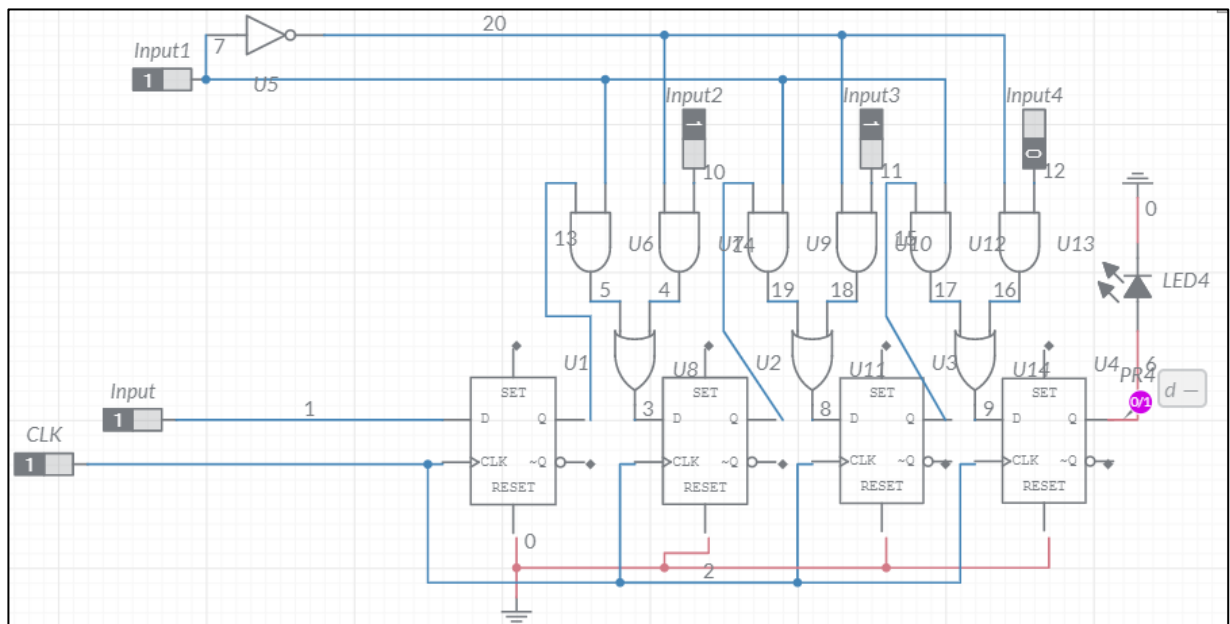
Timing Diagram

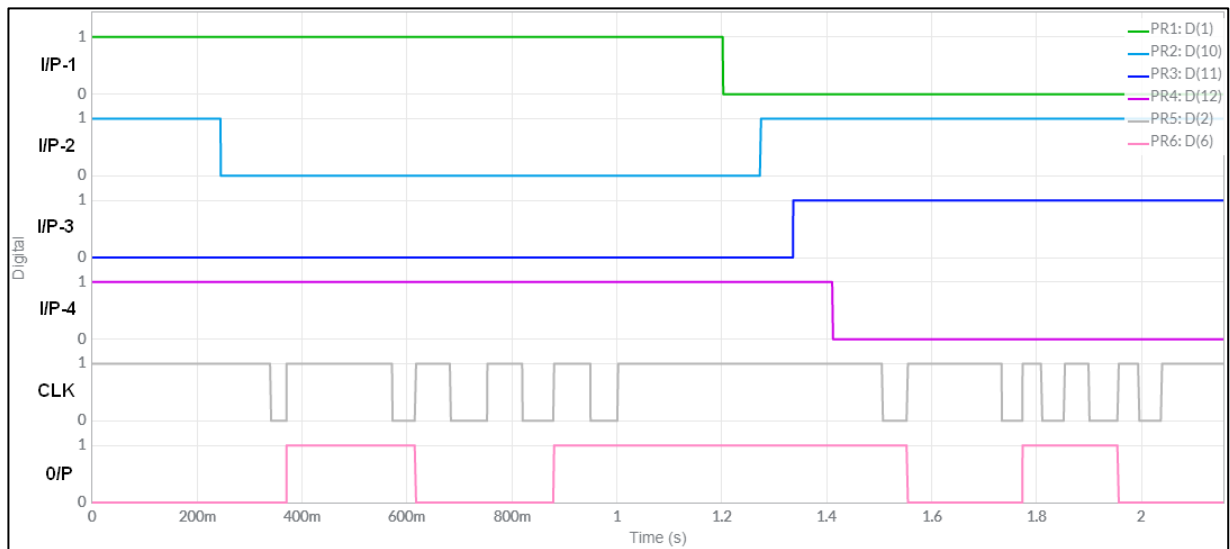


Parallel-in to Serial-out (PISO) Shift Register

The Parallel-in to Serial-out shift register acts in the opposite way to the serial-in to parallel-out one above. The data is loaded into the register in a parallel format in which all the data bits enter their inputs simultaneously, to the parallel input pins P_A to P_D of the register. The data is then read out sequentially in the normal shift-right mode from the register at Q representing the data present at P_A to P_D .

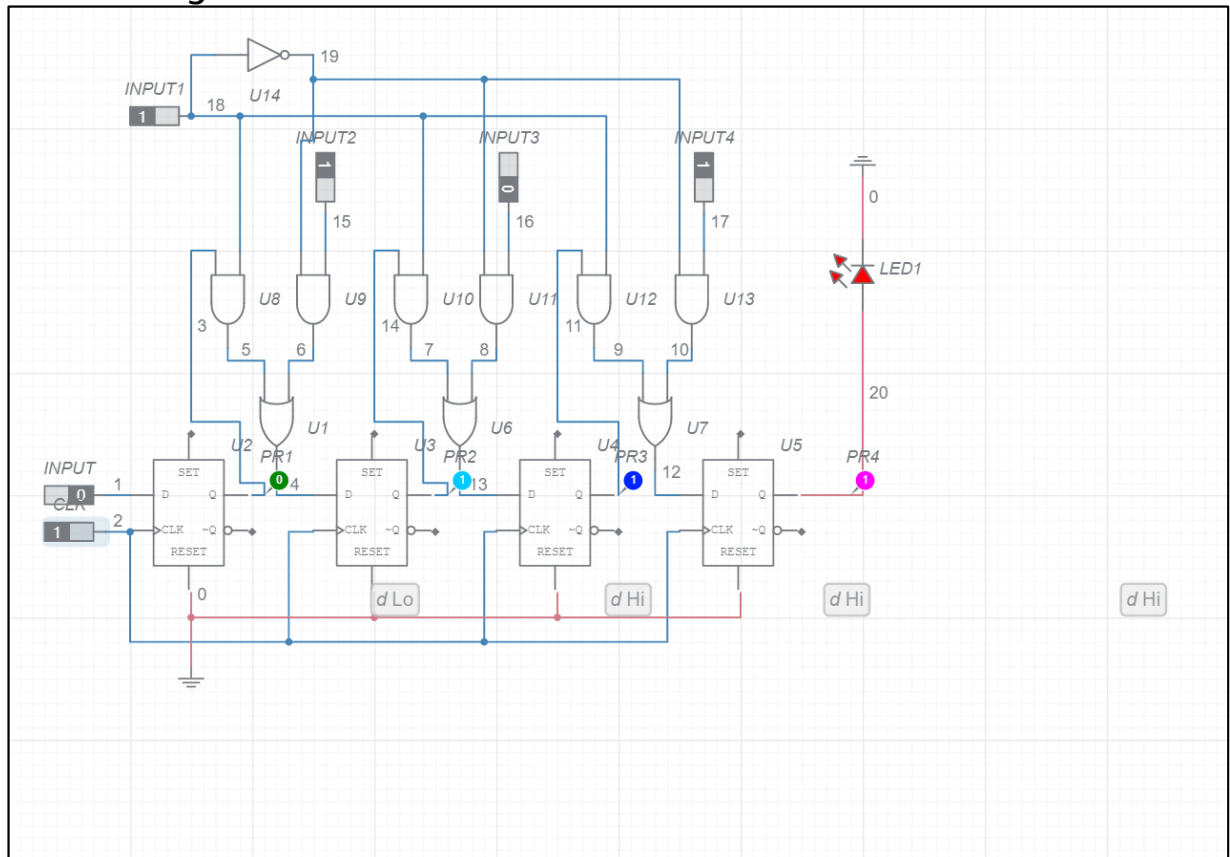
4-bit Parallel-in to Serial-out Shift Register



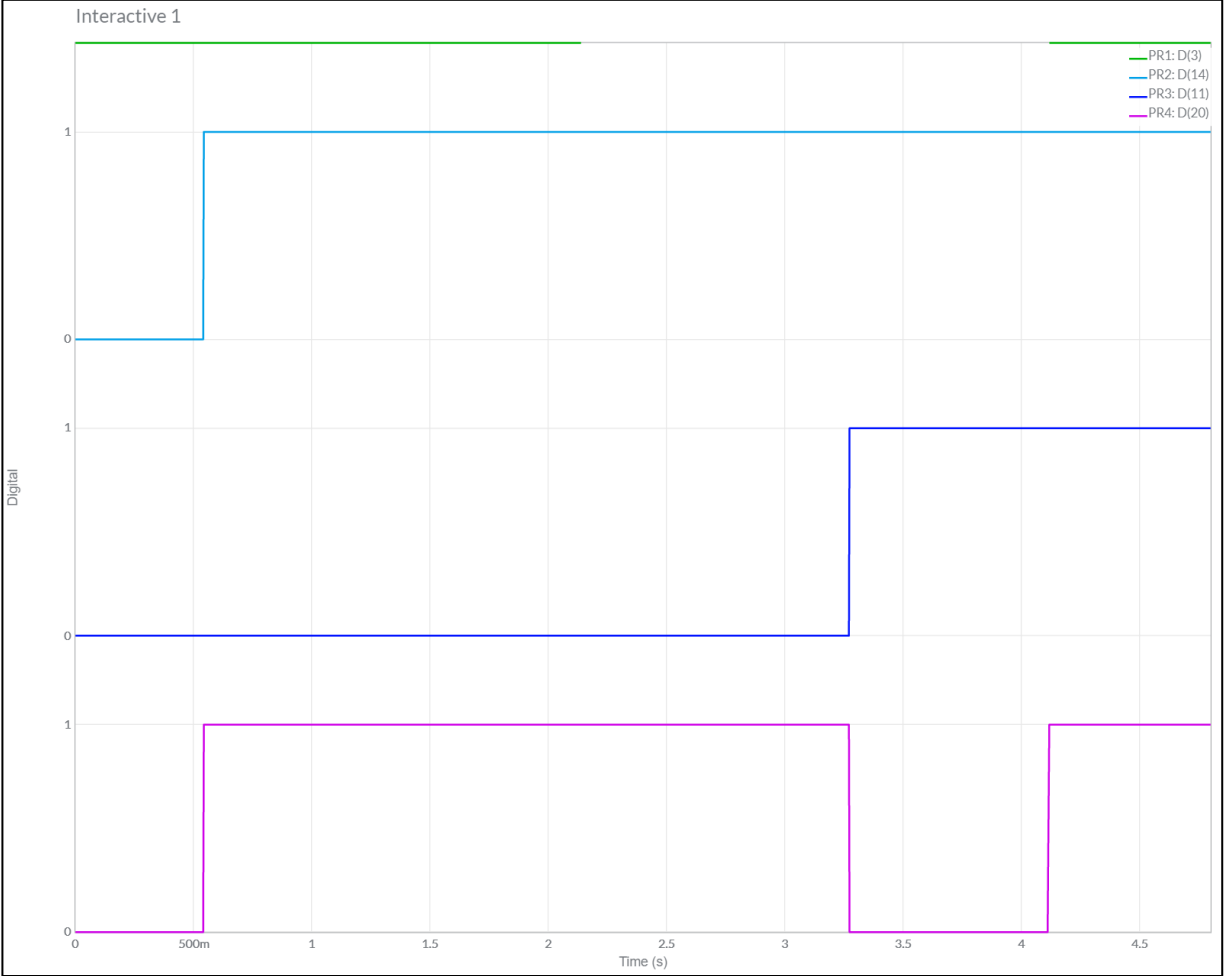


SIMULATION RESULTS

Circuit Diagram



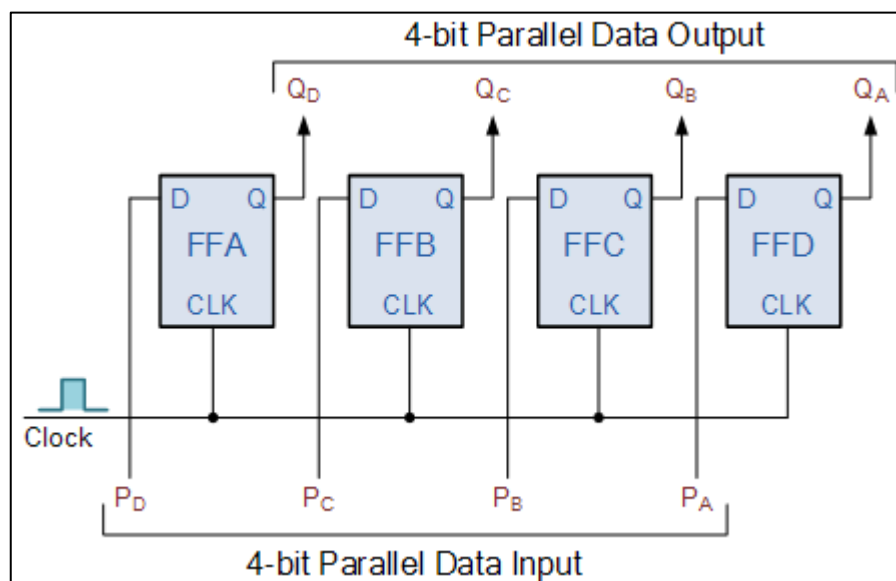
Timing Diagram



Parallel-in to Parallel-out (PIPO) Shift Register

The final mode of operation is the Parallel-in to Parallel-out Shift Register. This type of shift register also acts as a temporary storage device or as a time delay device similar to the SISO configuration above. The data is presented in a parallel format to the parallel input pins P_A to P_D and then transferred together directly to their respective output pins Q_A to Q_D by the same clock pulse. Then one clock pulse loads and unloads the register. This arrangement for parallel loading and unloading is shown below.

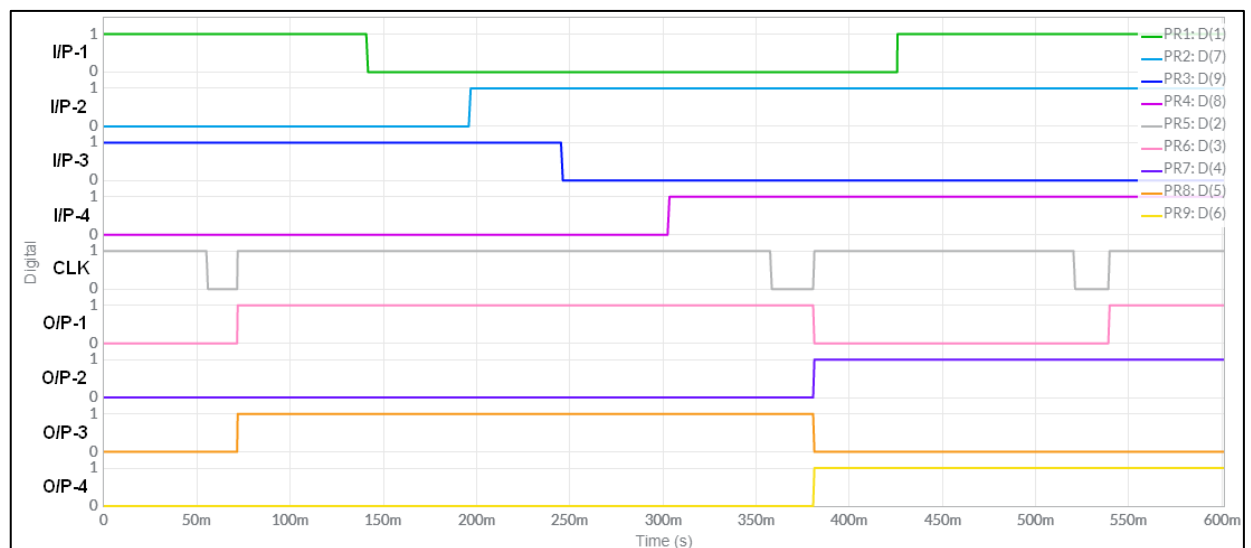
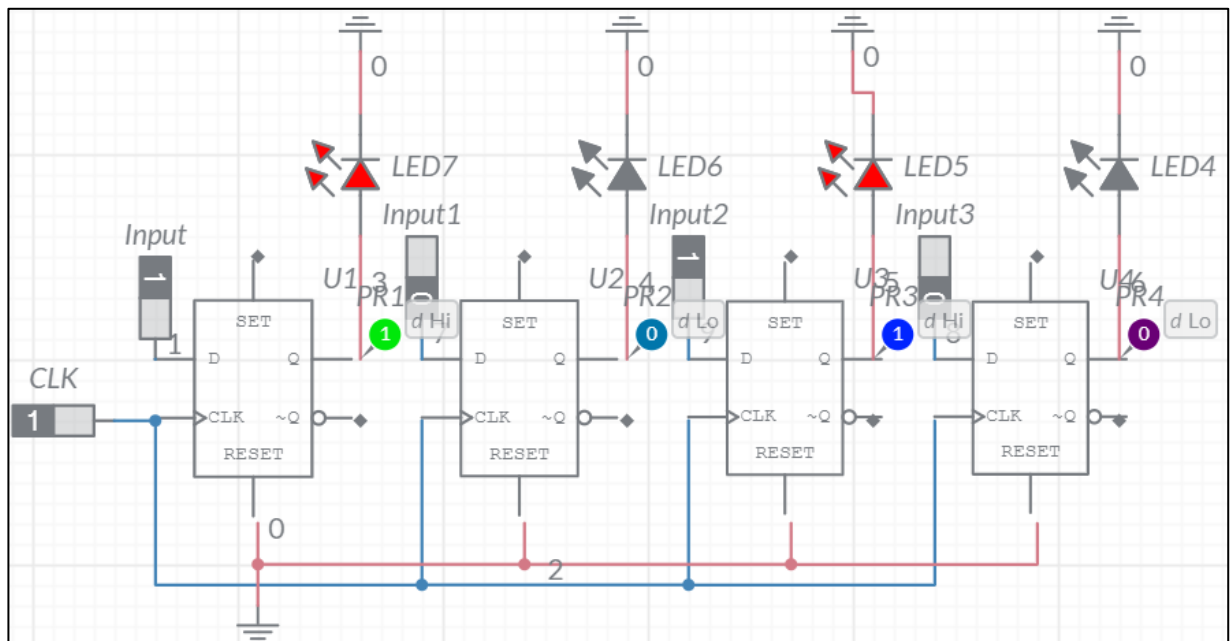
4-bit Parallel-in to Parallel-out Shift Register



The PIPO shift register is the simplest of the four configurations as it has only three connections, the parallel input (PI) which determines what enters the flip-flop, the parallel output (PO) and the sequencing clock signal (Clk).

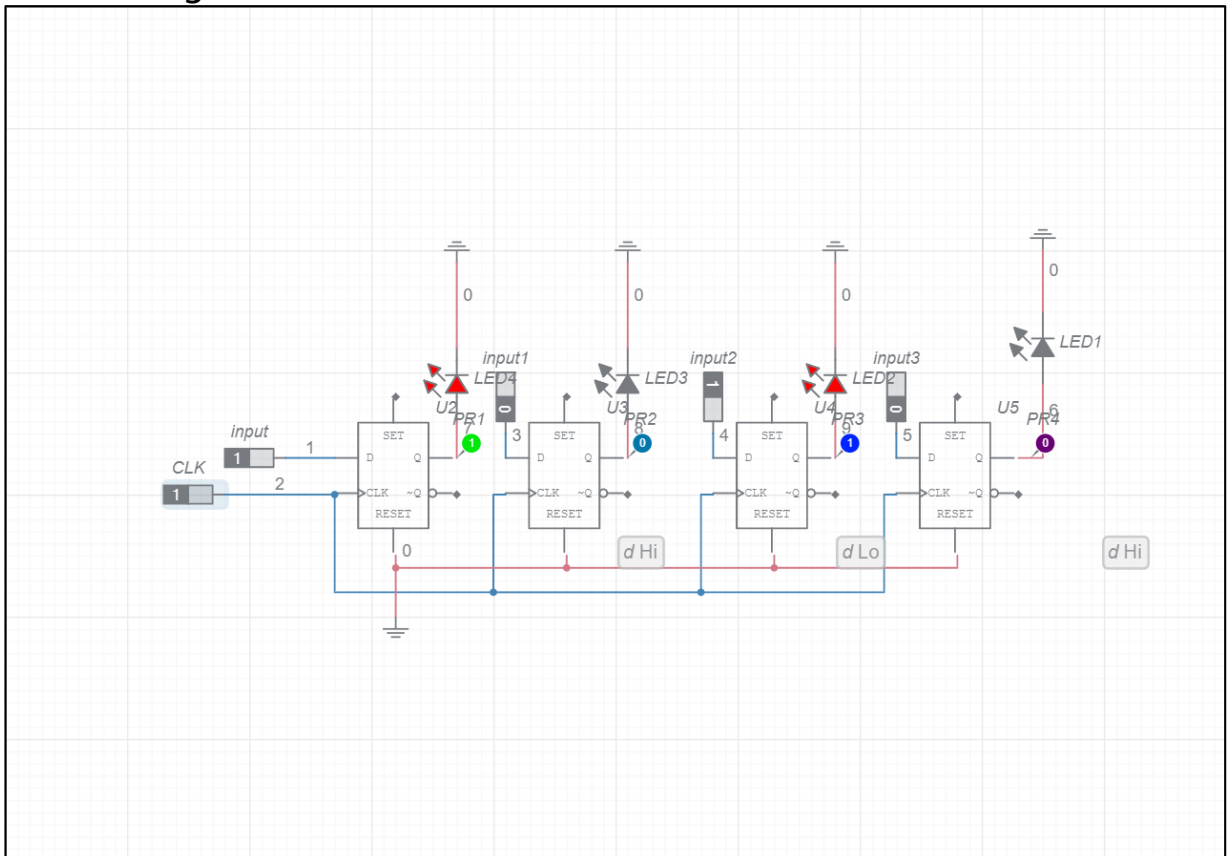
Similar to the Serial-in to Serial-out shift register, this type of register also acts as a temporary storage device or as a time delay device, with the amount of time delay being varied by the frequency of the clock pulses. Also, in this type of register there are no interconnections between the individual flip-flop since no serial shifting of the data is required.

PIPO CIRCUIT DIAGRAM in Multisim:

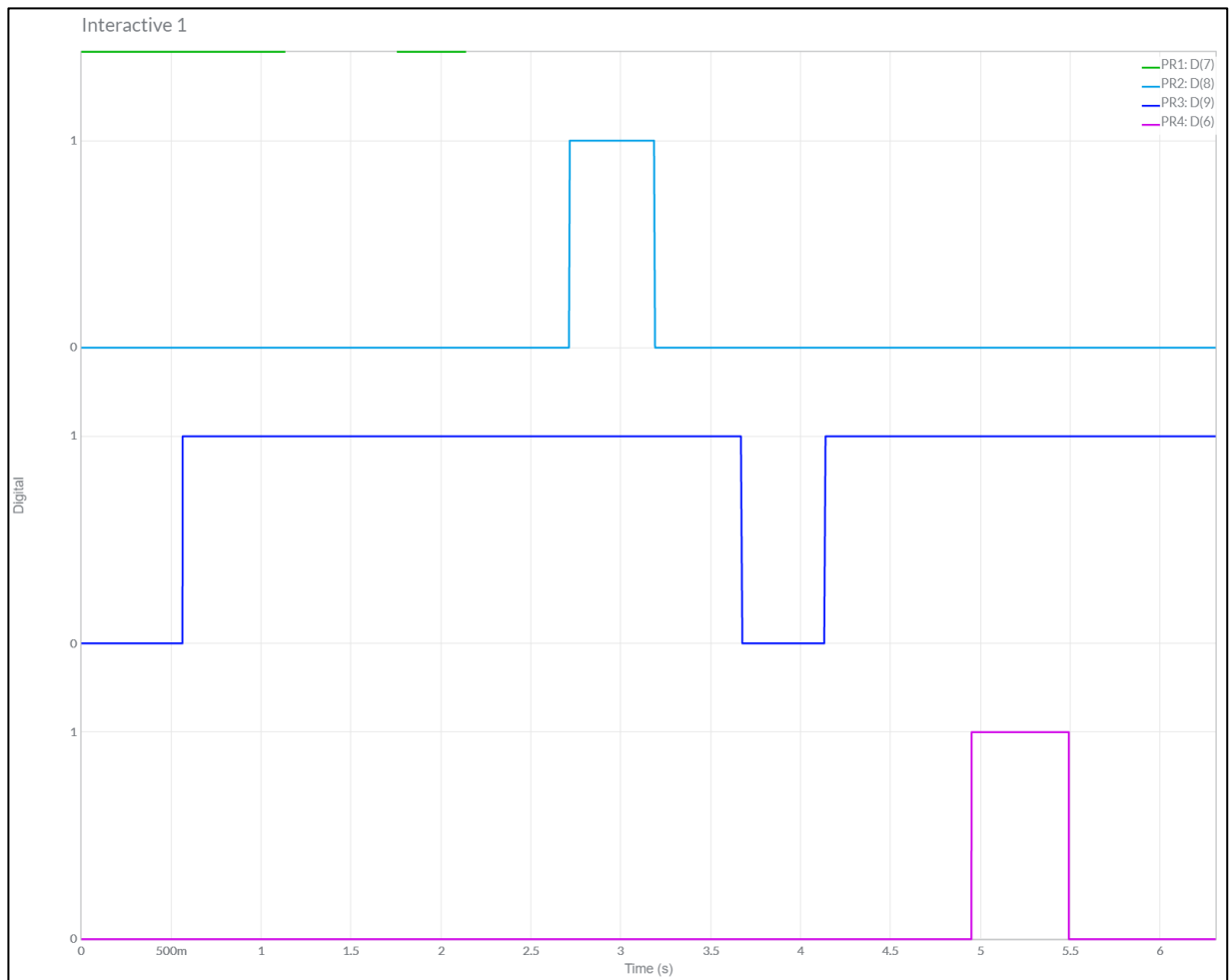


SIMULATION RESULTS

Circuit Diagram



Timing Diagram



Reference for Theory: https://www.electronics-tutorials.ws/sequential/seq_5.html

<https://www.electronicengineering.nbcafe.in/parallel-in-serial-out-shift-register-piso/>

RESULT

Thus, the implementation of D flip flop using Multisim is verified