SRM INSTITUTE OF SCIENCE & TECHNOLOGY
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DEPT. Of Computer Science Engineering

SRM IST, Kattankulathur – 603 203

Sub Code & Name: 18CSS201J - ANALOG AND DIGITAL ELECTRONICS

Experiment No	05
Title of Experiment	Design CMOS Inverter and measure its propagation delay using Multisim Live Online Circuit Simulator.
Name of the candidate	RAHUL GOEL
Register Number	RA1911030010094
Date of Experiment	20/09/20

Mark Split Up

S.No	Description	Maximum Mark	Mark Obtained
1	Oral Viva / Online Quiz	5	
2	Execution	10	
3	Model Calculation / Result Analysis	5	
	Total	**20**	

Staff Signature with date

Aim

To Design CMOS Inverter and measure its propagation delay.

Apparatus Required:

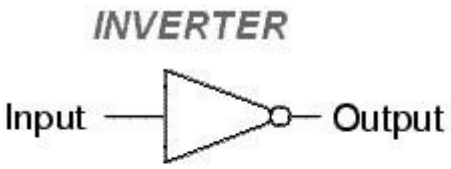
S.No	Apparatus	Type	Range
1	Transistor	Pmos4T	
2	Transistor	Nmos4T	
3	Clock Voltage		
4	Capacitor		500fF

Software Required:

https://www.multisim.com/

THEORY

The inverter is universally accepted as the most basic logic gate doing a Boolean operation on a single input variable. Fig.1 depicts the symbol, truth table and a general structure of a CMOS inverter. As shown, the simple structure consists of a combination of an pMOS transistor at the top and a nMOS transistor at the bottom.



Input	Output
1	0
0	1

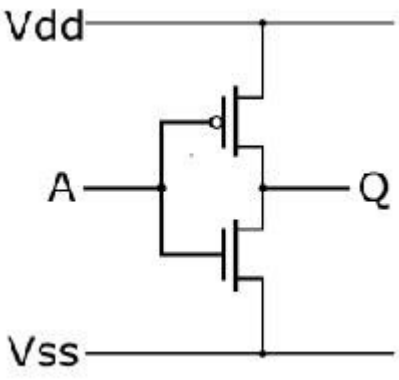


Fig.1: Symbol, circuit structure and truth table of a CMOS inverter

CMOS is also sometimes referred to as complementary-symmetry metal–oxide– semiconductor. The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn while the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic, which uses all n-channel devices without p-channel devices. Fig. 2 shows the propogation delay graph.

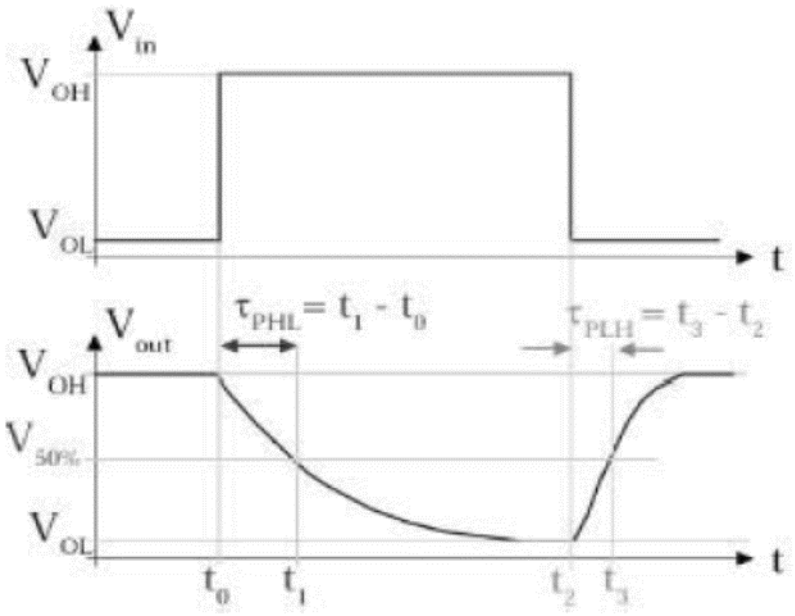


Fig.2 Propogation delay graph

The propagation delay t_p of a gate defines how quickly it responds to a change at its inputs. It express the delay experienced by a signal when passing through a gate. It is measured between the 50% transition points of the input and output waveforms. The τ_{pLH} defines the response time of the gate for a low to high output transition. The τ_{pHL} defines the response time of the gate for a high to low output transition. The propagation delay t_p is the average of the two.

Formula:

$$\tau_p = \left(\frac{\tau_{pHL} + \tau_{pLH}}{2} \right)$$

Procedure:

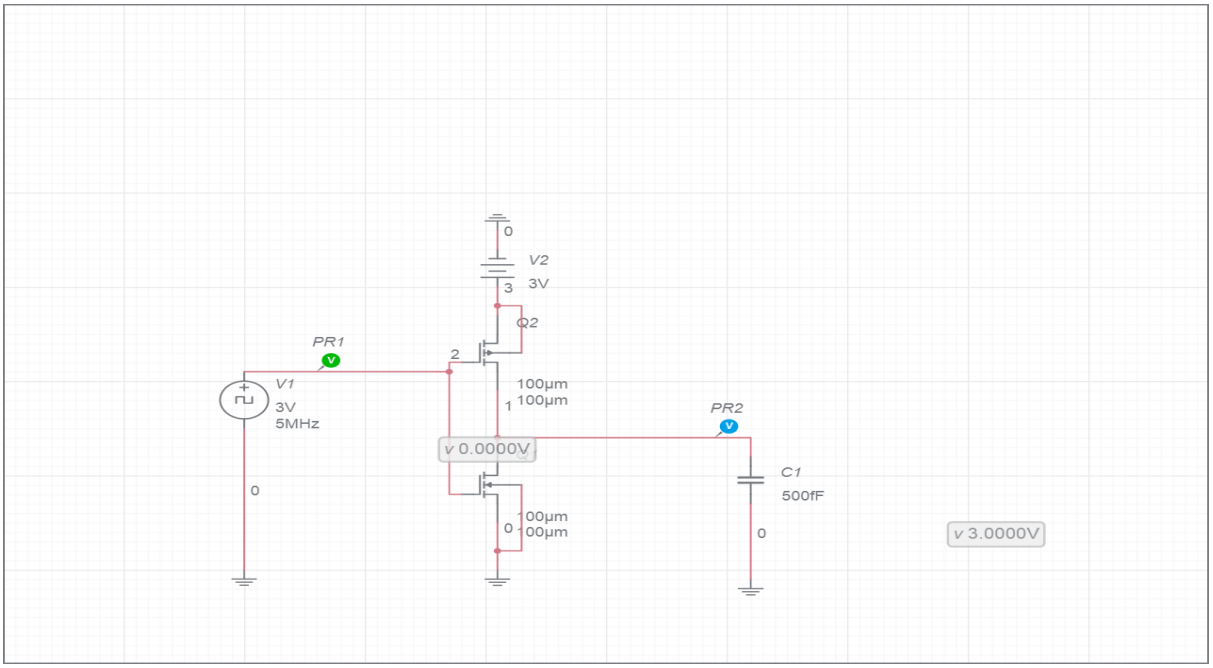
I. Give the connections as per the circuit diagram.

II. Give 3 V, 5MHz Input to the circuit.

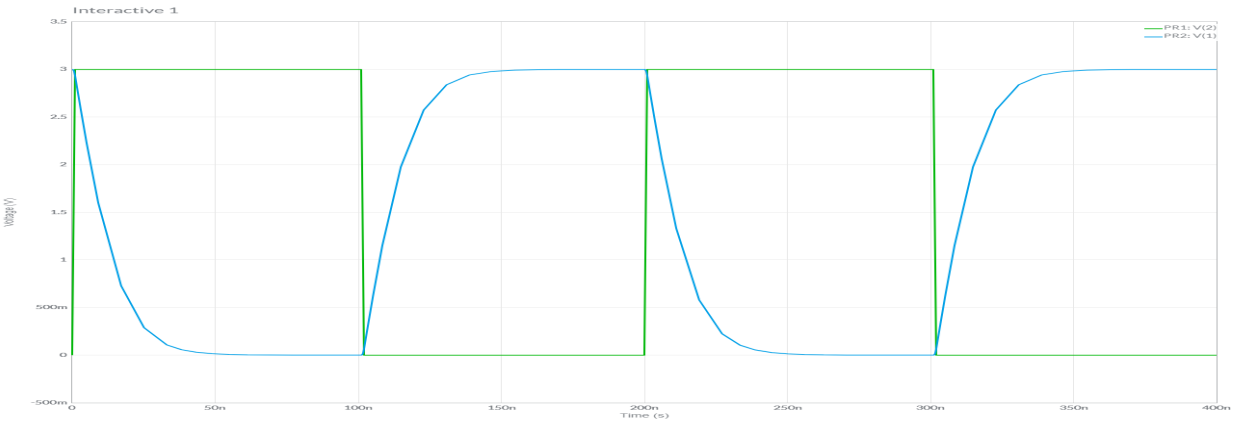
III. Measure the inverter output across the capacitor and input voltage.

IV. Plot its performance graph and measure the propagation delay from the output waveform.

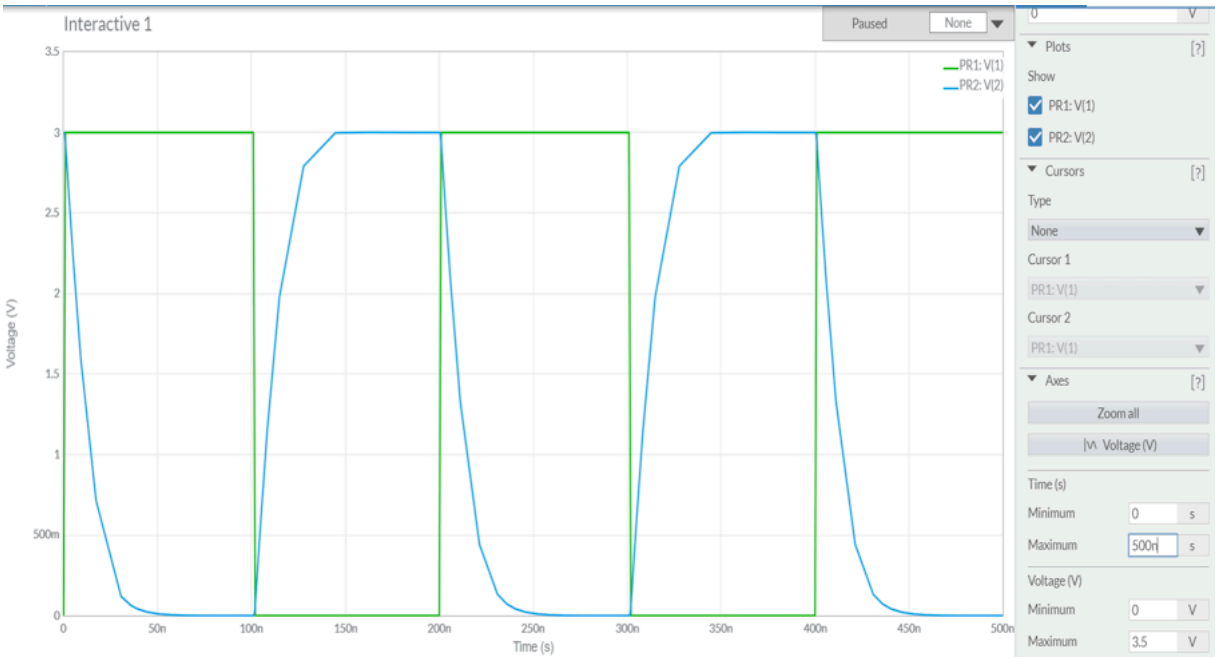
Circuit Diagram:



Model graph:



Simulation waveform for the inverter:



Model Calculation:

$\tau_{pLH} = 252.2 - 200.0 =$ **52.2**

$\tau_{pHL} = 144.6 - 101.0 =$ **43.6**

$\tau_p = (\tau_{pLH} + \tau_{pHL})/2 = (52.2 + 43.6)/2 = 95.8/2 =$ **47.9**

Result:

Thus, the CMOS Inverter is simulated and the propagation delay is measured.