



DEPT. of Computer Science Engineering

SRM IST, Kattankulathur – 603 203

Sub Code & Name: 18CSS201J - ANALOG AND DIGITAL ELECTRONICS

Experiment No	10
Title of Experiment	Design and simulation of 3-bit Synchronous up and down counter using multisim
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Register Number	RA1911030010094
Date of Experiment	8/10/20

Mark Split Up

S.No	Description	Maximum Mark	Mark Obtained
1	Oral Viva / Online Quiz	5	
2	Circuit Connection and Execution	10	
3	Verification of Results	5	
Total		20	

Staff Signature with date

10. Design and simulation of 3-bit Synchronous up and down counter using multisim

AIM:

To design and simulation 3-bit synchronous up and down counter using multisim software.

APPARATUS REQUIRED

S.No	Apparatus	Type	Quantity
1)	JK - Flipflop	Link attached	3
2)	Multisim online		

THEORY: COUNTER

Counter is the most useful and versatile subsystem of digital branch. Counter is going to count number of clock pulses applied to it. Maximum count that binary counter can count is $2^n - 1$. Clock pulses occur at regular time interval, so that counter can be used to measure time or frequency. Digital counters are integrated circuits (ICs) that count events in computers and other digital systems. Because they must remember past states, digital counters include memory. Generally, digital counters consist of bistable devices or bistable multi vibrators called flip-flops. The number of flip-flops and the way in which they are connected determines the number of states and the sequence of states that digital counters complete in each full cycle.

Counters can be subdivided into 2 groups:

1. Asynchronous Counters
2. Synchronous Counters

The way in which devices are clocked determines whether digital counters are

categorized as synchronous or asynchronous. In synchronous devices (such as synchronous BCD counters and synchronous decade counters), one clock triggers all of the flip-flops simultaneously.

With asynchronous devices, often called asynchronous ripple counters an external clock pulse triggers only the first flip-flop. Each successive flip-flop is then clocked by one of the outputs (Q or Q') of the previous flip-flop.

Digital counters are configured as UP (counting in increasing sequence), DOWN (counting in decreasing sequence) or Bidirectional (UP / DOWN).

Synchronous / Asynchronous counter can be subdivided into following subgroups:

- Sequential Counters: States of counter are sequential.
- Non-sequential Counters: Sequence or states of counter are sequential but irregular.
- Regular Counters: In this counters, FFs are used. There is direct relation between number of states and number of FFs used i.e. $N=2^m$.
- Decade counter – counts through ten states per stage.
- Up down counter – counts both up and down, under command of a control input

Some of the commercial ICs used for design of Counters:

- ✓ IC 7490-Decade Counter
- ✓ IC 7492 Divide by 10 Counter
- ✓ IC 7493 4 - bit binary Counter
- ✓ IC 74190 Up -Down Decade Counter
- ✓ IC74191 Binary Up-down Counter

a. 3-BIT SYNCHRONOUS UP COUNTER

The 3 bit up counter shown in below diagram is designed by using JK flip flop. External clock pulse is connected to all the flip flops in parallel. For designing the counters JK flip flop is preferred.

The significance of using JK flip flop is that it can toggle its state if both the inputs are high, depending on the clock pulse. The inputs of first flip flop are connected to HIGH (logic 1), which makes the flip flop to toggle, for every clock pulse entered into it. So the synchronous counter will work with single clock signal and changes its state with each pulse.

Truth Table:

Clk	Present State			Next state			Flipflop Inputs					
	Qc	Qb	Qa	Q _{c+1}	Q _{b+1}	Q _{a+1}	Jc	Kc	Jb	Kb	Ja	Ka
1	0	0	0	0	0	1	0	X	0	X	1	X
2	0	0	1	0	1	0	0	X	1	X	X	1
3	0	1	0	0	1	1	0	X	X	0	1	X
4	0	1	1	1	0	0	1	X	X	1	X	1
5	1	0	0	1	0	1	X	0	0	X	1	X
6	1	0	1	1	1	0	X	0	1	X	X	1
7	1	1	0	1	1	1	X	0	X	0	1	X
8	1	1	1	0	0	0	X	1	X	1	X	1

K-Map Simplification:

Jc

QcQb \ Qa	0	1
00	0	0
01	0	1
11	X	X
10	X	X

Jb

QcQb \ Qa	0	1
00	0	1
01	X	X
11	X	X
10	0	1

Ja

QcQb \ Qa	0	1
00	1	X
01	1	X
11	1	X
10	1	X

Kc

QcQb \ Qa	0	1
00	X	X
01	X	X
11	0	1
10	0	0

Kb

QcQb \ Qa	0	1
00	X	X
01	0	1
11	0	1
10	X	X

Ka

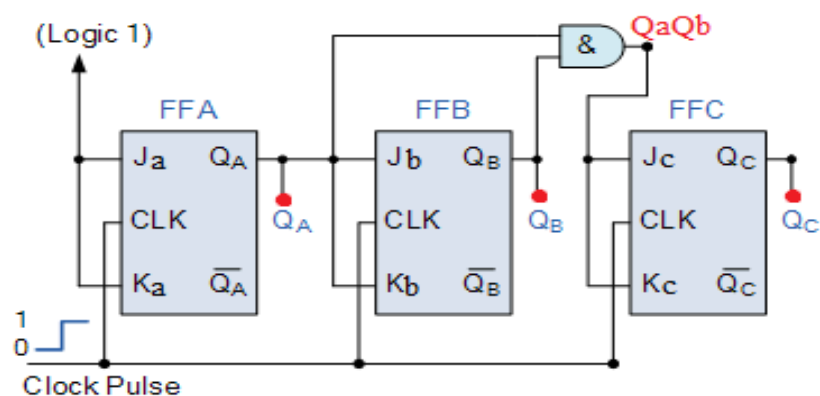
QcQb \ Qa	0	1
00	X	1
01	X	1
11	X	1
10	X	1

Ja = 1; Ka = 1

Jb = Qa; Kb = Qa

Jc = Qa Qb; Kc = Qa Qb

Logic Diagram:



b. 3-BIT SYNCHRONOUS DOWN COUNTER

Truth Table:

Clk	Present State			Next state			Flipflop Inputs					
	Qc	Qb	Qa	Q _{c+1}	Q _{b+1}	Q _{a+1}	Jc	Kc	Jb	Kb	Ja	Ka
1	1	1	1	1	1	0	X	0	X	0	X	1
2	1	1	0	1	0	1	X	0	X	1	1	X
3	1	0	1	1	0	0	X	0	0	X	X	1
4	1	0	0	0	1	1	X	1	1	X	1	X
5	0	1	1	0	1	0	0	X	X	0	X	1
6	0	1	0	0	0	1	0	X	X	1	1	X
7	0	0	1	0	0	0	0	X	0	X	X	1
8	0	0	0	1	1	1	1	X	1	X	1	X

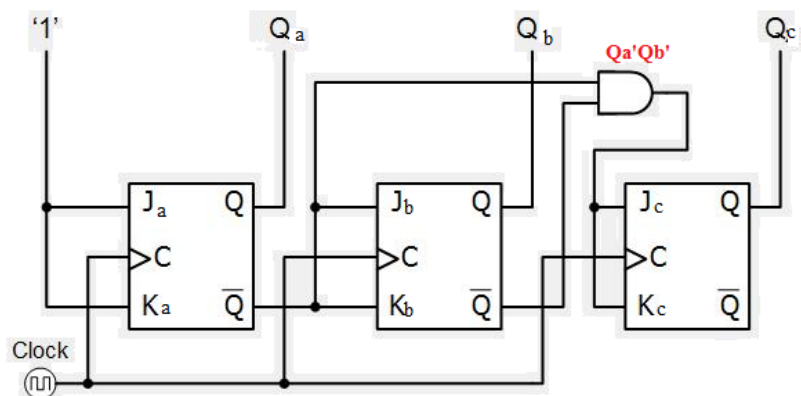
K-Map Simplification:

$$J_a = 1; K_a = 1$$

$$J_b = Q_a'; K_b = Q_a'$$

$$J_c = Q_a' Q_b'; K_c = Q_a' Q_b'$$

Logic Diagram:

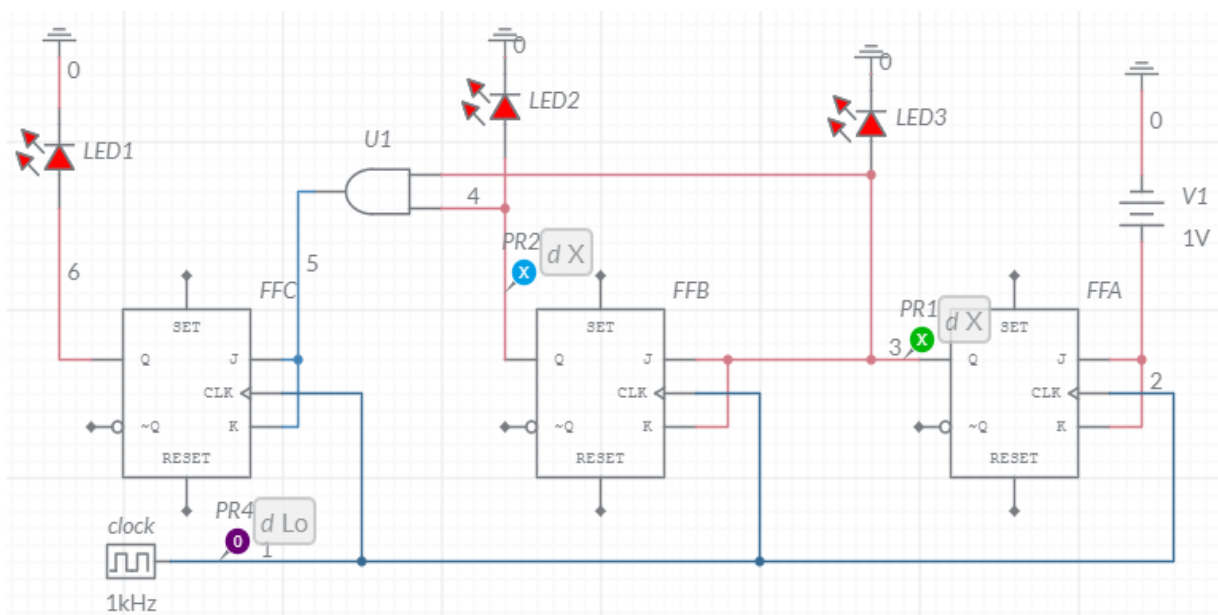


PROCEDURE:

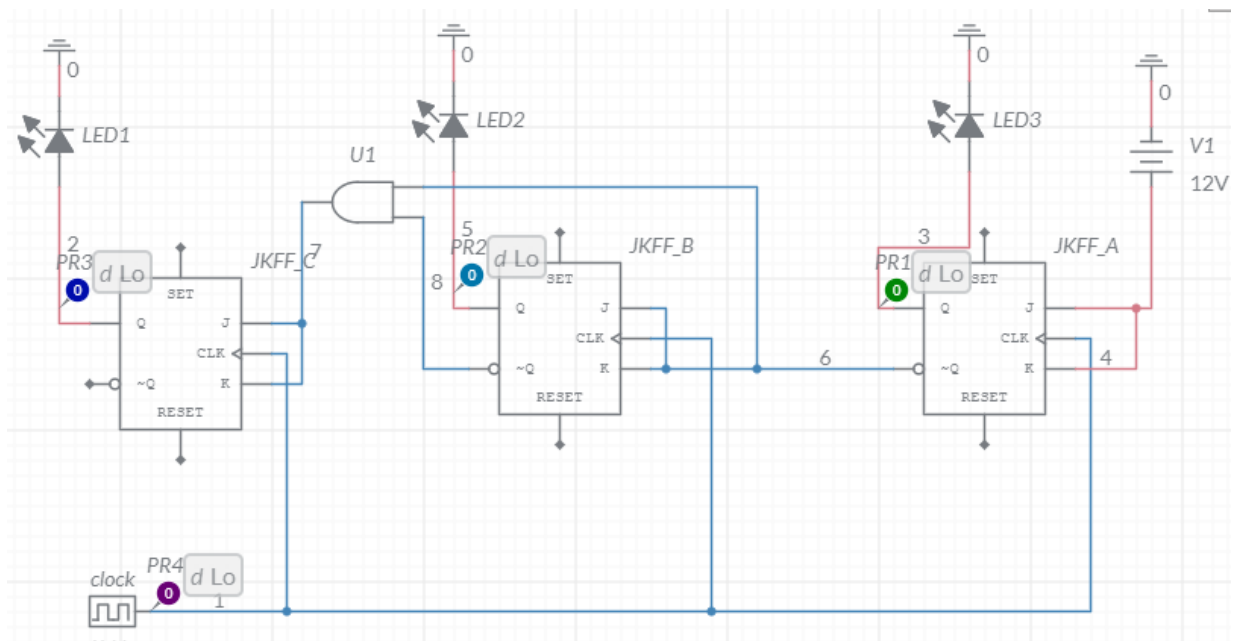
1. Open online Multisim software and create a new circuit
2. Use the following link to add JK- flipflop and Clock Pulse (it's not available in online multisim)
<https://www.multisim.com/content/R47jgTRSmr4SeacynyyJ26/jk-ff-clock/open/>
3. Connect the circuit as per given logic diagram.
4. Apply the Clock Pulse parameters as Duty=50%, Frequency =1kHz.
5. Verify results of 3-bit synchronous up and down counter.

SIMULATION DIAGRAM:

3-BIT SYNCHRONOUS UP COUNTER

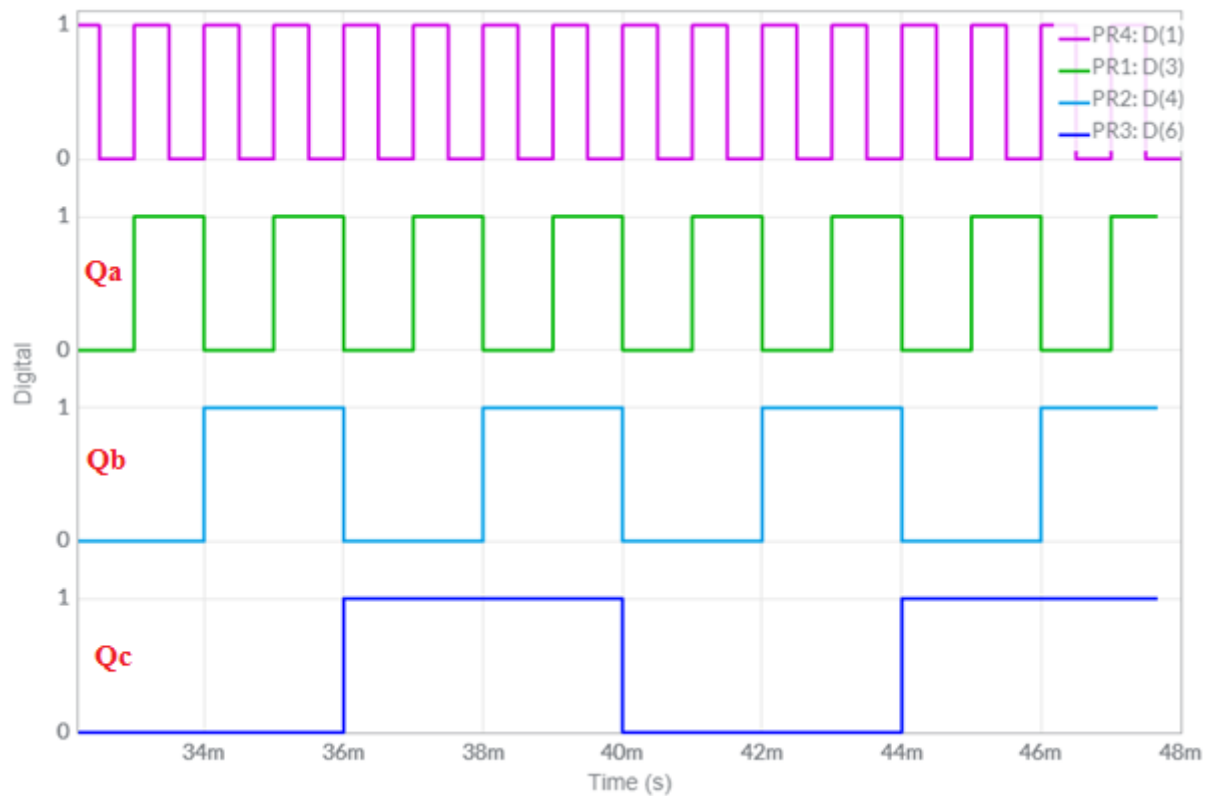


3-BIT SYNCHRONOUS DOWN COUNTER

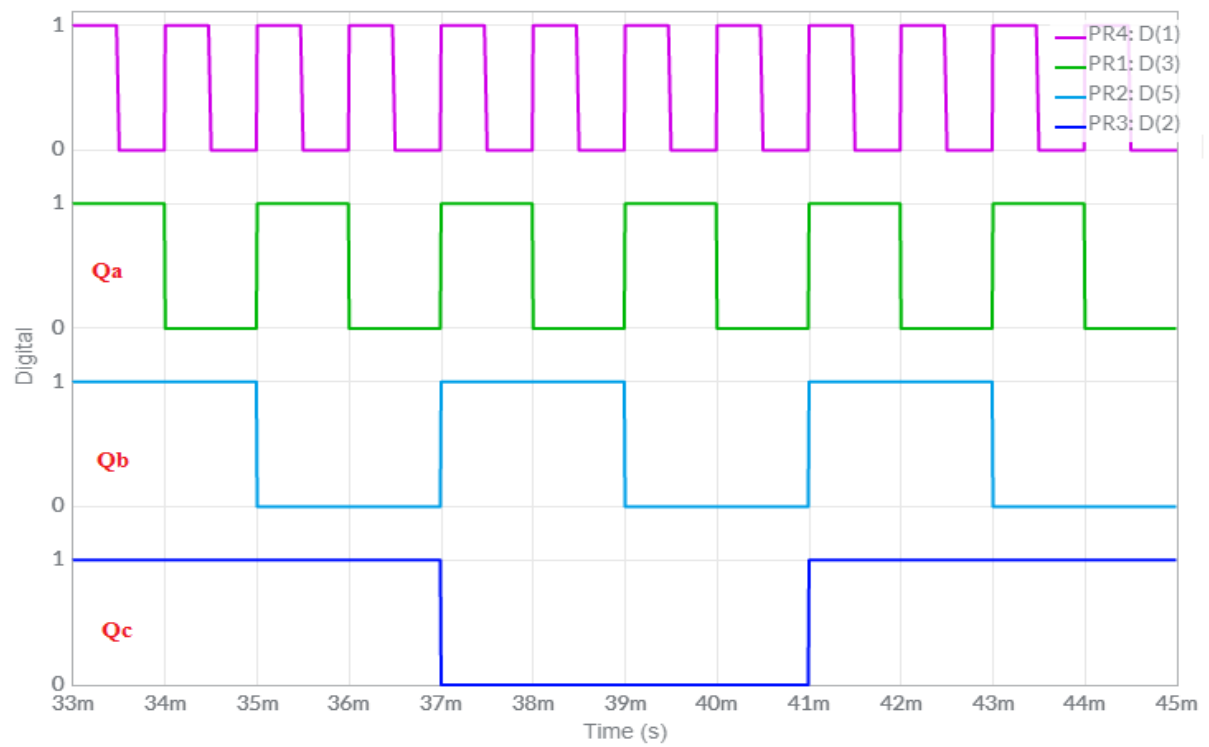


SIMULATION RESULT:

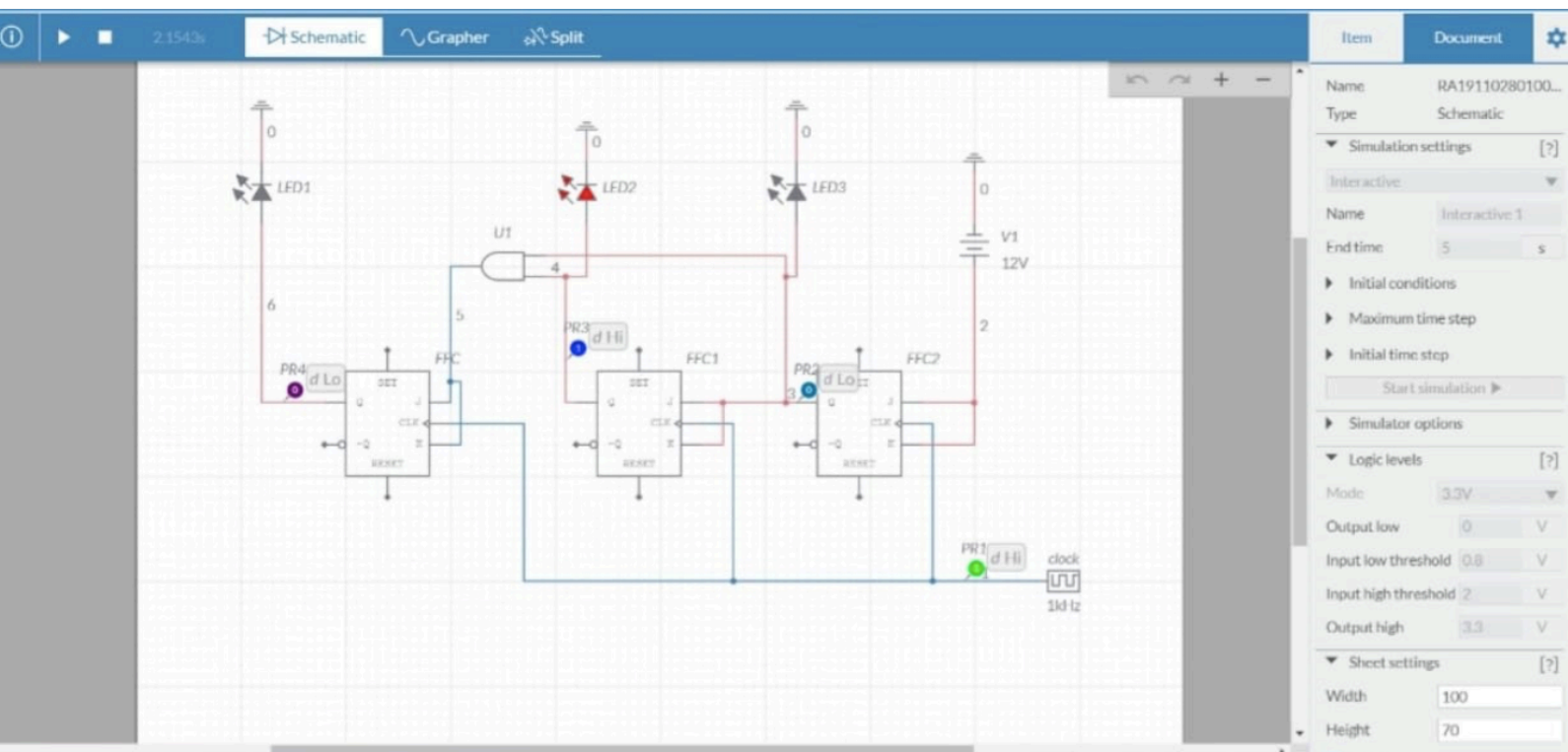
3-BIT SYNCHRONOUS UP COUNTER



3-BIT SYNCHRONOUS DOWN COUNTER



3-BIT SYNCHRONOUS UP COUNTER





RESULT

Thus, the design and simulation of simulation 3-bit synchronous up and down counter using multisim software.