NAME : RAHUL GOEL
REG NO: RA1911030010094
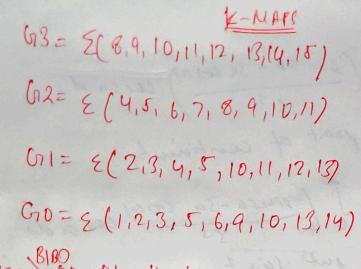
Batch: O2-TP304
Year: 2nd
Semester: 3rd
Subject Code: 18CSS201J

TITLE: Design the code converter to convert Binary data into Gray code data using Multisim
software. Draw the truth table and show the simplification using K Map.
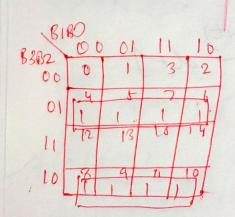
Aim	2	
Circuit diagram / Logic diagram, Tabulation, Formula / K map simplification, Procedure, Timing diagram, & Document submission	10	
Execution & Result	8	
Viva	5	
TOTAL	25	

Binary   Gray Code

B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	0
0	1	1	0	0	1	1	1
0	1	1	1	0	1	1	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	1
1	0	1	1	1	0	1	0
1	1	0	0	1	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	0

K-MAPS

$$G3 = \Sigma(8,9,10,11,12,13,14,15)$$

$$G2 = \Sigma(4,5,6,7,8,9,10,11)$$

$$G1 = \Sigma(2,3,4,5,10,11,12,13)$$

$$G0 = \Sigma(1,2,3,5,6,9,10,13,14)$$

B3B2 \ B1B0	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12 [1]	13 [1]	15 [1]	14 [1]
10	8 [1]	9 [1]	11 [1]	10 [1]

$$G3 = B3$$

B3B2 \ B1B0	00	01	11	10
00	0	1	3	2
01	4 [1]	5 [1]	7 [1]	6 [1]
11	12	13	15	14
10	8 [1]	9 [1]	11 [1]	10 [1]

$$G2 = \overline{B3}\,B2 + B3\overline{B2}$$

$$G2 = B3 \oplus B2$$

Karnaugh map 1:

B3B2 \ B1B0	00	01	11	10
00	0	1	1 (3)	2
01	1 (4)	1 (5)	7	6
11	1 (12)	1 (13)	15	14
10	8	9	1 (11)	1 (10)

$$G1 = B2\overline{B1} + \overline{B2}B1$$

$$G1 = B1 \oplus B2$$

Karnaugh map 2:

B3B2 \ B1B0	00	01	11	10
00	0	1 (1)	3	1 (2)
01	4	1 (5)	7	1 (6)
11	12	1 (13)	15	1 (14)
10	8	1 (9)	11	1 (10)

$$G0 = \overline{B1}B0 + B1\overline{B0}$$

$$G0 = B1 \oplus B0$$

$$G3 = B3$$

$$G2 = \overline{B3}B2 + B3\overline{B2}$$

$$G2 = B3 \oplus B2$$

$$G1 = B2\overline{B1} + \overline{B2}B1$$

$$G1 = B1 \oplus B2$$

$$G0 = \overline{B1}B0 + B1\overline{B0}$$

$$G0 = B1 \oplus B0 .$$

Schematic   Grapher   Split   210.23ms

Item   Document

ID   DG1
Type   Digital Constan

▼ Description

Interactive digital constant. See Digi
constant for more information.

▼ Model

Digital_Source

State

Toggle output state

Rise time   0
Time it takes for signal to transition
from low to high.

Fall time   0
Time it takes for signal to transition
from high to low.

▼ Logic levels

☑ Use document settings
Use logic levels settings from
Document tab.

Mode   3.3V
Threshold voltage levels.

Output low   0
Output low voltage.

Output high   3.3
Output high voltage.

▶ Symbol

▶ Details

VIVA QUESTIONS:

1. 6 selection lines

2. AB'

3. Because its two basic functions are data storage and data movement. Each flip-flop in a shift register represents one bit of storage capacity.

4. Q(next)= S+R'Q   SR = 0