EXPERIMENT – 12

NAME :Rahul Goel

Reg no:RA1911030010094

Aim:

Software used: Logic Gate Simulator

Truth Table:

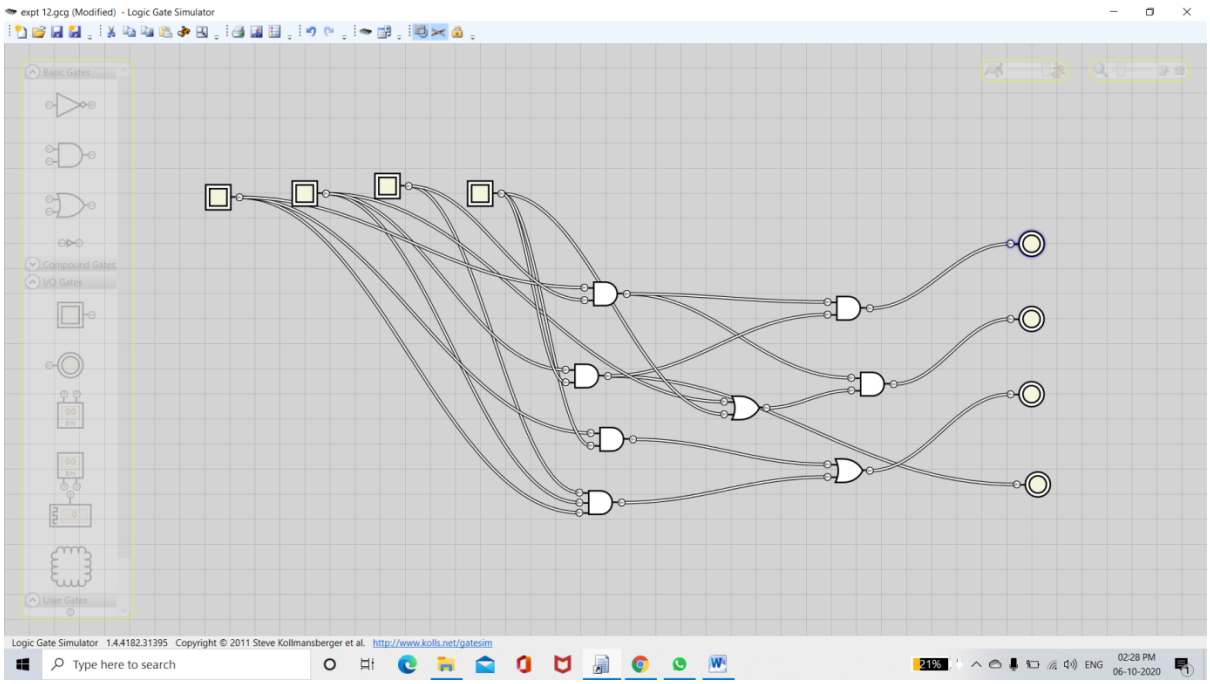
A		B		Y			
A1	A0	B1	B0	Y3	Y2	Y1	Y0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1

1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

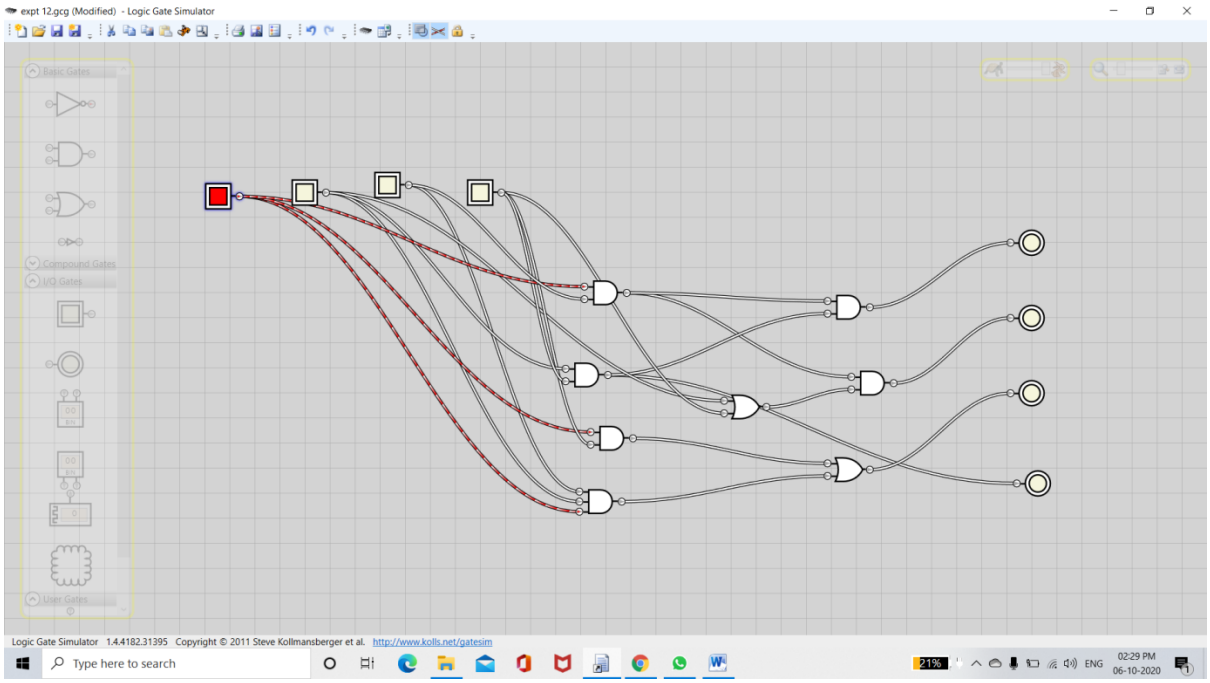
Y3=A1A0B1B0

Y2=A1

Circuit Diagram:



OUTPUT:


expt 12.gcg (Modified) - Logic Gate Simulator
Basic Gates
Compound Gates
I/O Gates
User Gates
Logic Gate Simulator 1.4.4182.31395 Copyright © 2011 Steve Kollmansberger et al. http://www.kolls.net/gatesim
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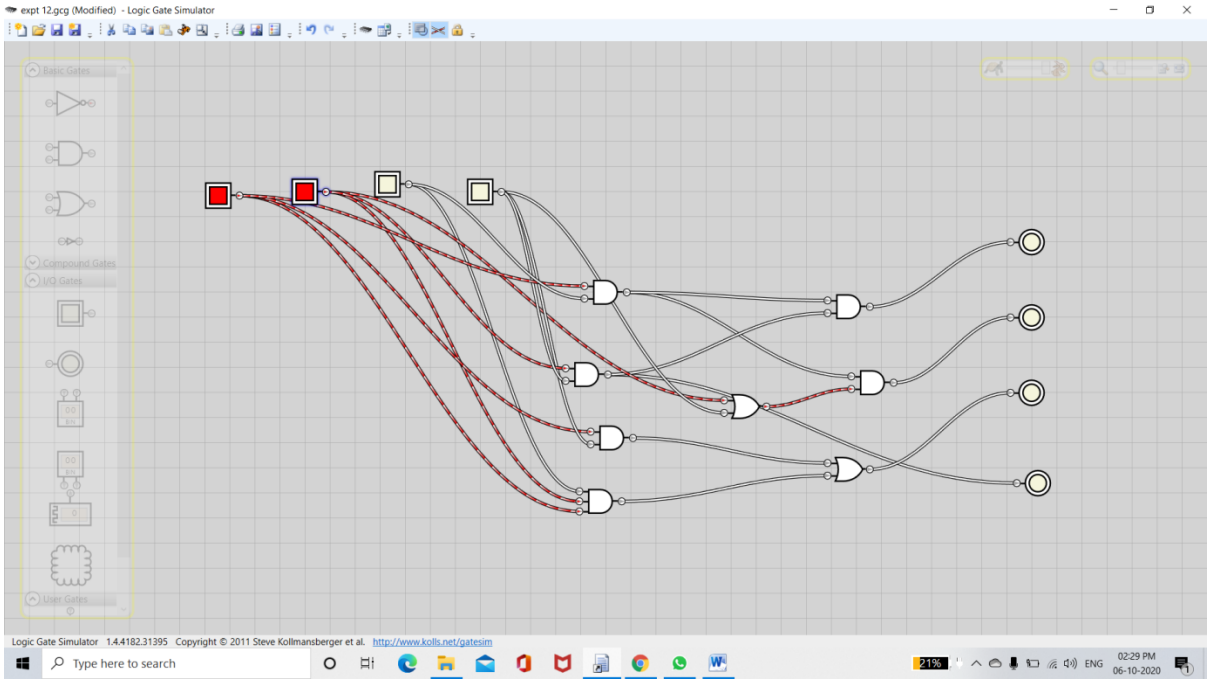
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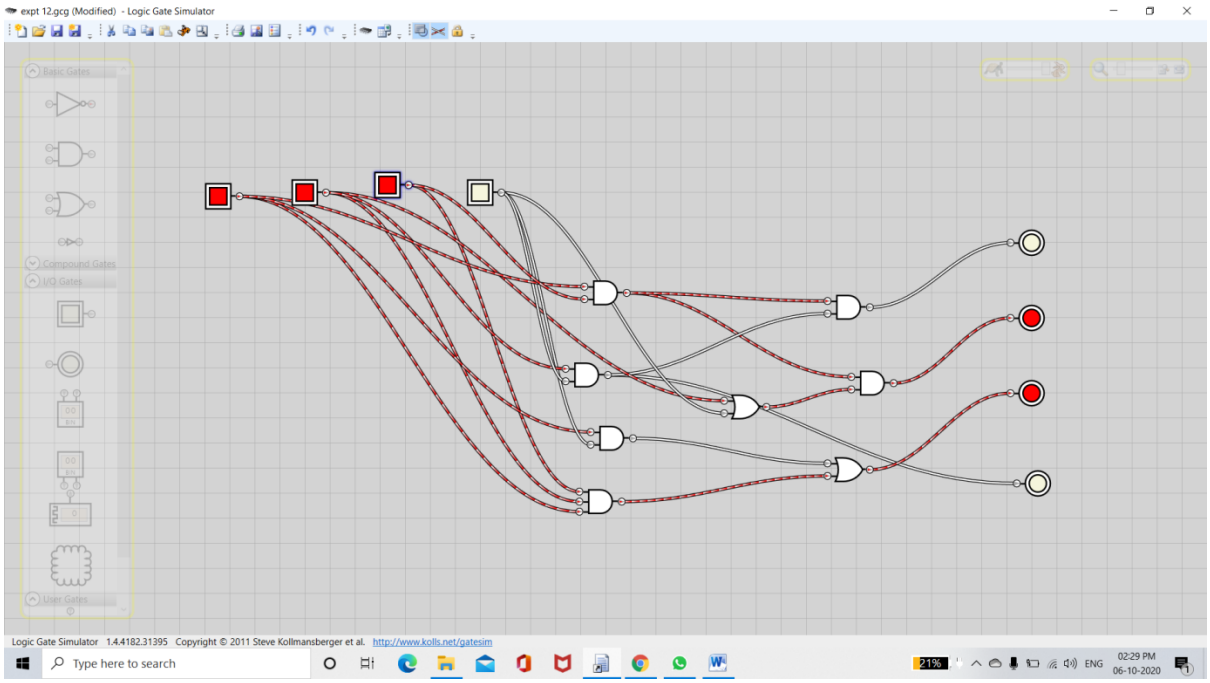
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