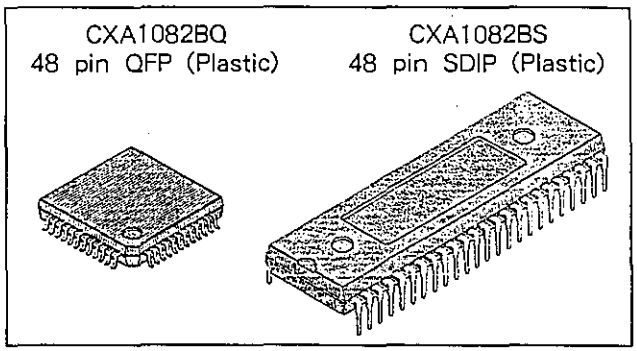
SONY®

CXA1082BQ/BS

Servo Signal Processor for CD Player

Description

CXA1082BQ/BS is a bipolar IC designed for the servo control of the compact disc player. The only difference from CXA1082AQ/AS is the FZC threshold.



Features

- Single power supply, 5 V
- Dual power supply, ±5 V
- Low power consumption (165 mW Typ.: ±5 V, 100 mW, 5 V)
- Servo functions same as the CX20108 (focus, tracking, and sled servo)
- Built-in auto sequencer
- Built-in LPF for spindle servo
- Built-in loop filter and VCO for EFM clock reproduction PLL
- Fewer external parts
- Built-in circuit for preventing sled runaway
- Built-in circuit for disc defects
- Built-in anti-shock circuit
- High-speed access using a linear motor
- Sharing of the serial data bus of the microcomputer with the CX23035 or CXD1135Q
- Compatible in the upword with the CX20108 for microcomputer software
- The peaks of focus search, track jump, and sled kick pulse can be set with external resistors.

Functions

- Focus servo control
- Tracking servo control
- Sled servo control
- Spindle servo
  LPF, drive amplifier
- EFM clock reproduction PLL
  Loop filter, 8.64 MHz VCO
- Auto sequencer
  Built-in RAM

Structure

Bipolar silicon monolithic IC

E90777B78

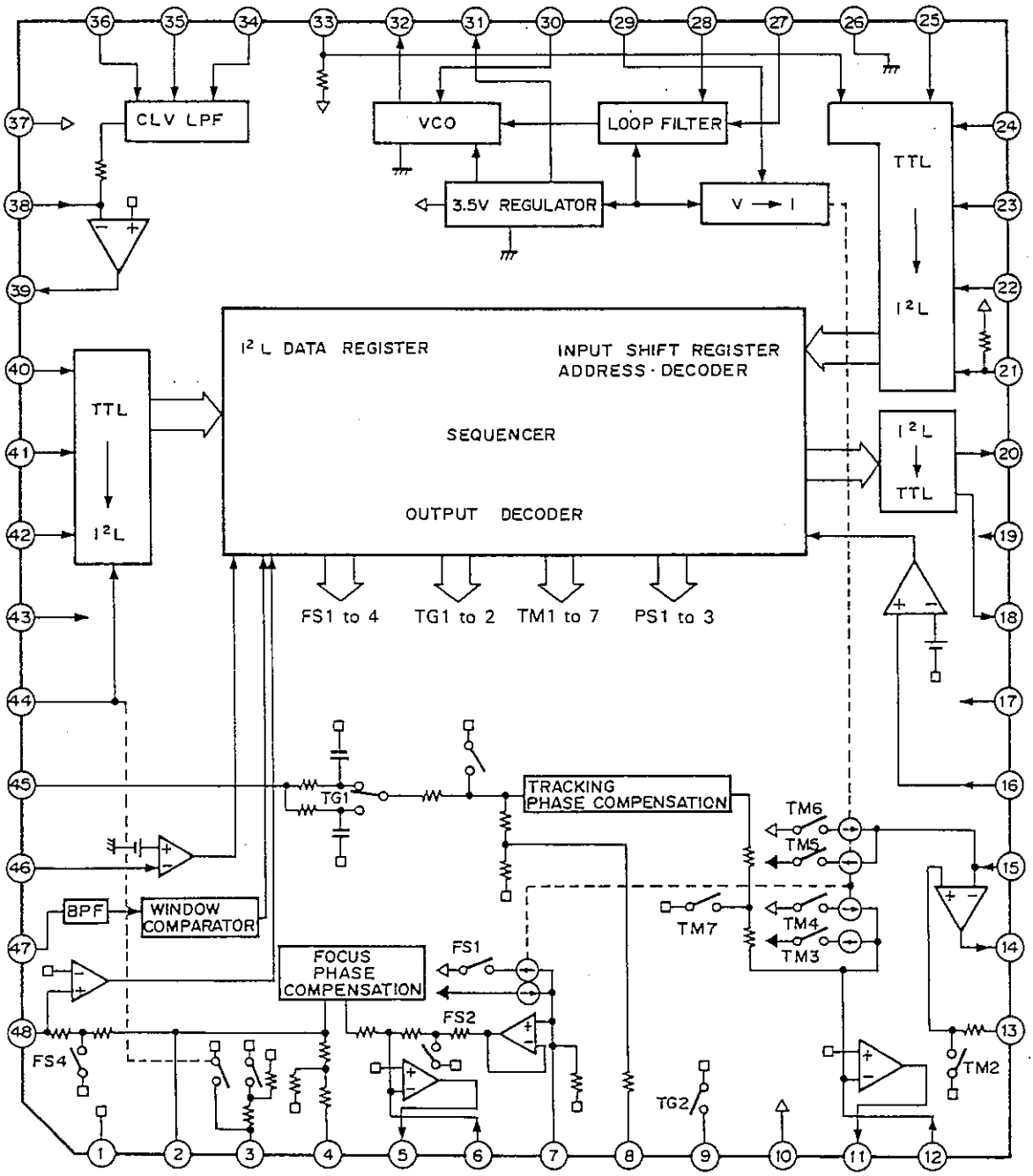
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc — VEE		12	V
• Operating temperature	Topr		−20 to +75	°C
• Storage temperature	Tstg		−55 to +150	°C
• Allowable power dissipation	PD	CXA1082BQ	833	mW
		CXA1082BS	1330	mW

Recommended Operating Conditions

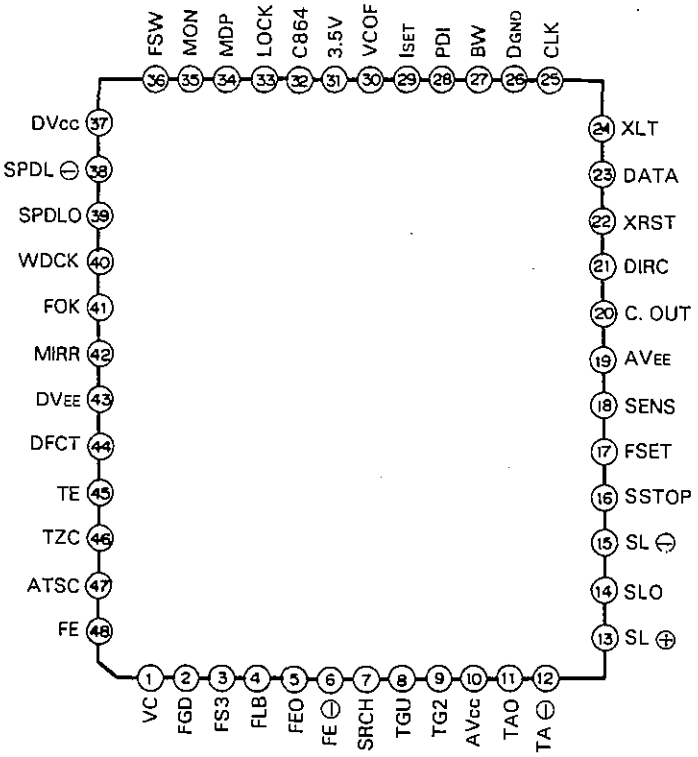
• Supply voltage	Vcc — VEE	4 to 11	V
	Vcc — DGND	4 to 5.5	V

Block Diagram

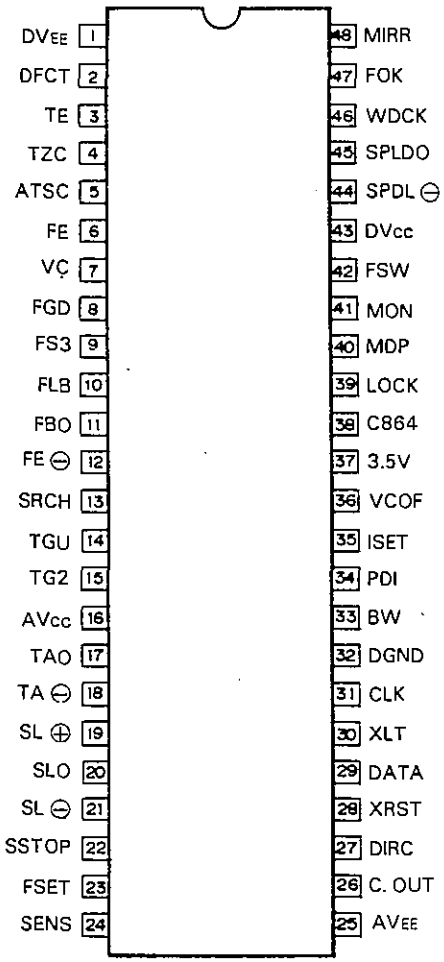


Pin Configuration

CXA1082BQ

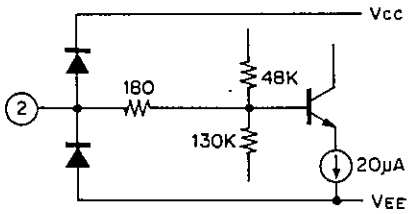
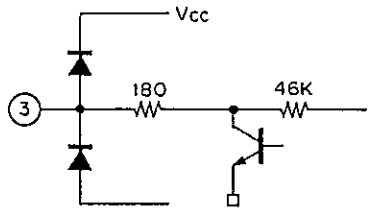


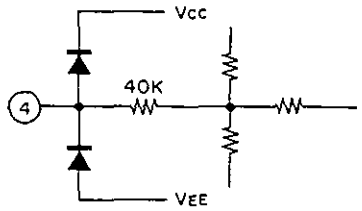
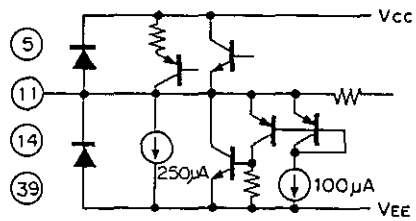
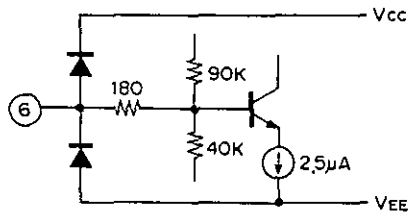
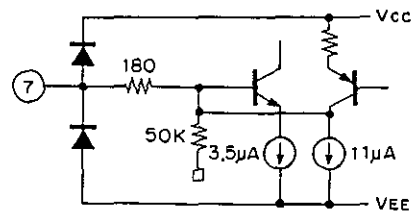
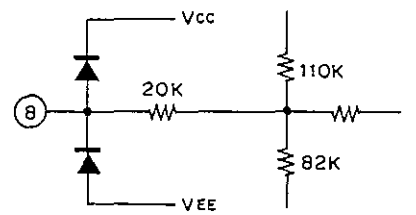
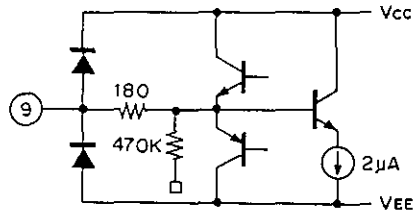
CXA1082BS

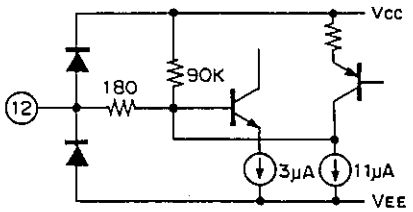
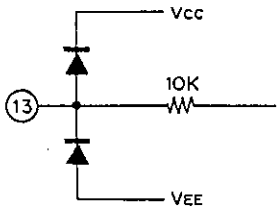
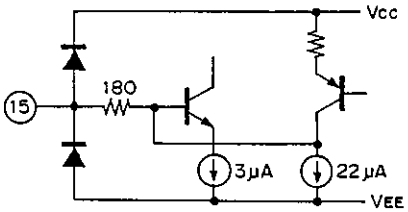
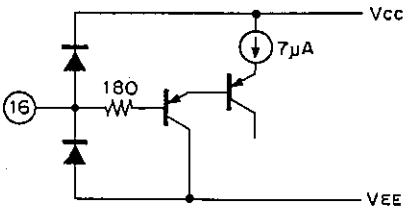
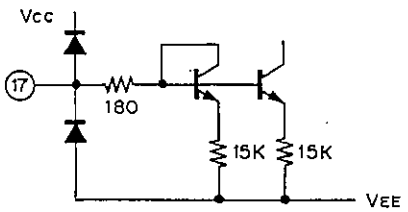
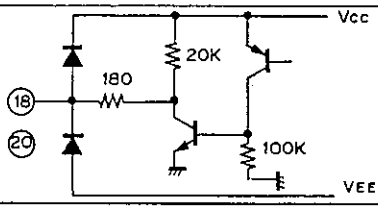


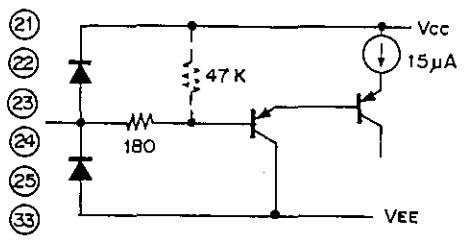
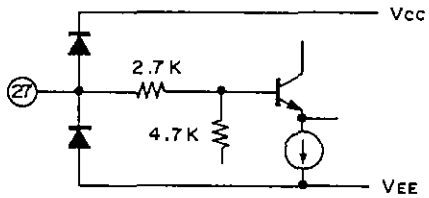
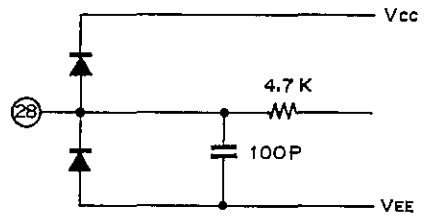
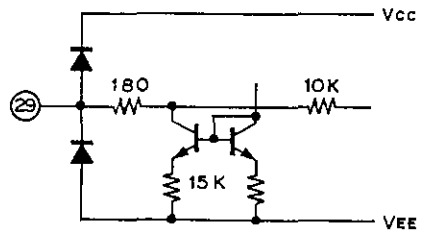
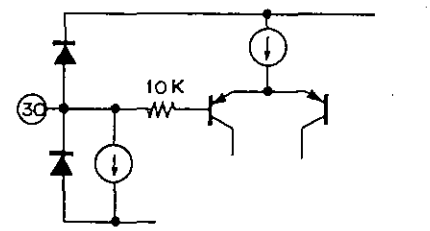
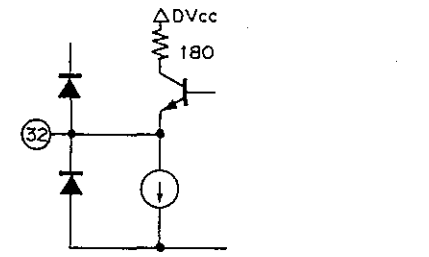
Pin Description

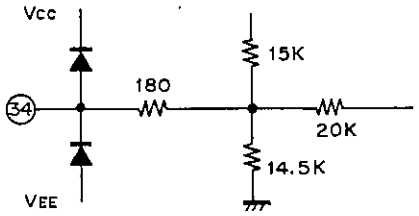
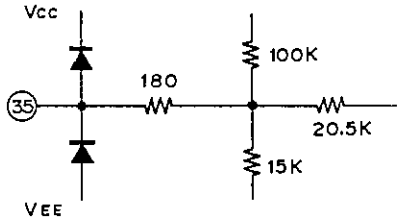
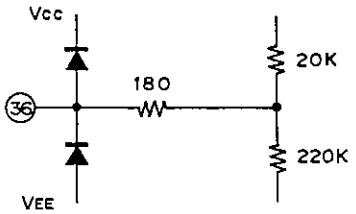
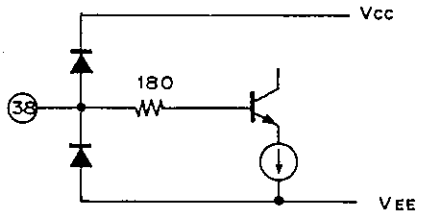
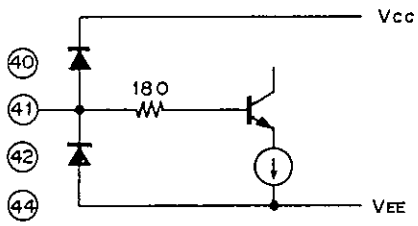
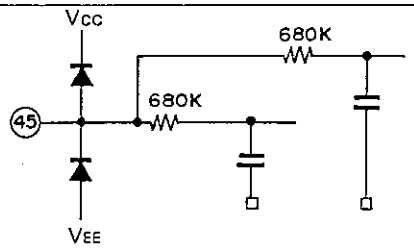
Numbers in ( ) show CXA1082BS

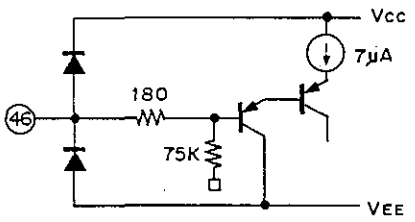
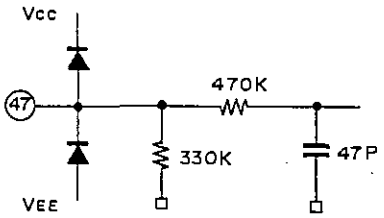
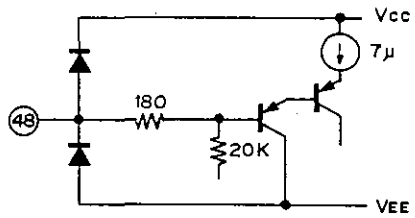
No.	Symbol	Equivalent Circuit	Description
2 (8)	FGD		Connect a capacitor between this pin and pin 3 (9) to reduce the high-frequency gain.
3 (9)	FS3		The high-frequency gain of the focus servo can be changed by switching FS3 ON or OFF.

No.	Symbol	Equivalent Circuit	Description
4 (10)	FLB		Time constant external pin for rising low band-width of the focus servo.
5 (11)	FEO		Focus drive output
11 (19)	TAO		Tracking drive output
14 (20)	SLO		Sled drive output
39 (45)	SPDLO		Spindle drive output
6 (12)	FE –		Inverse input pin for the focus amplifier.
7 (13)	SRCH		Pin for providing a time constant to generate the focus search waveform.
8 (14)	TGU		Pin for providing a time constant to switch the tracking gain of high-frequency.
9 (15)	TG2		Pin for providing a time constant to change the high-frequency tracking gain.

No.	Symbol	Equivalent Circuit	Description
12 (18)	TA –		Inverse input pin for the tracking amplifier.
13 (19)	SL +		Non-inverse input pin for the sled amplifier.
15 (21)	SL –		Inverse input pin for the sled amplifier.
16 (22)	SSTOP		Pin for detecting a signal for the ON/OFF limit switch of the innermost part of the disc.
17 (23)	FSET		Pin for setting the peak frequency of the focus, tracking phase compensation and f0 of the CLV LPF.
18 (24)	SENS		Pin to output FZC, AS, TZC, SSTOP and $\overline{\text{BUSY}}$ by command from CPU.
20 (26)	C. OUT		Track number count signal output

No.	Symbol	Equivalent Circuit	Description
21 (27)	DIRC		Pin for one-track jump Contains a 47 kΩ pull-up resistor.
22 (28)	XRST		Reset input pin, reset at "L"
23 (29)	DATA		Serial data input from CPU
24 (30)	XLT		Latch input from CPU
25 (31)	CLK		Serial data transfer clock input from CPU
33 (39)	LOCK		Pin for the operation of the sled runaway prevention circuit at "L" Contains a 47 kΩ pull-up resistor.
27 (33)	BW		Pin for providing a time constant for the loop filter.
28 (34)	PDI		Input pin for the CX23035/CXD1135 phase comparator output PDO.
29 (35)	ISET		Current is input, determining the peaks of focus search, track jump, and sled kick.
30 (36)	VCOF		The free-running frequency of VCO is almost proportional to the resistance value between this pin and pin 31 (37).
32 (38)	C864		Output pin of 8.64 MHz VCO.

No.	Symbol	Equivalent Circuit	Description
34 (40)	MDP		Pin for connecting the CX23035/CXD1135 MDP pin.
35 (41)	MON		Pin for connecting the CX23035/CXD1135 MON pin.
36 (42)	FSW		Pin for providing an external LPF time constant of the CLV servo error signal.
38 (44)	SPDL —		Inverse input pin for the spindle drive amplifier.
40 (46) 41 (47) 42 (48) 44 (2)	WDCK FOK MIRR DFCT		Clock input for auto sequence, usually 88.2 kHz is input FOK signal input pin Mirror signal input pin Defect signal input pin for the operation of the defect countermeasure circuit at "H"
45 (3)	TE		Input pin for tracking error signals.

No.	Symbol	Equivalent Circuit	Description
46 (4)	TZC		Input pin for the zero-cross tracking comparator.
47 (5)	ATSC		Input pin of the window comparator for ATSC detection.
48 (6)	FE		Input pin for focus error signals.

Electrical Characteristics

Ta = 25°C AV_{CC}, DV_{CC} = 2.5V AV_{EE}, DV_{EE} = −2.5V DGND = −2.5V

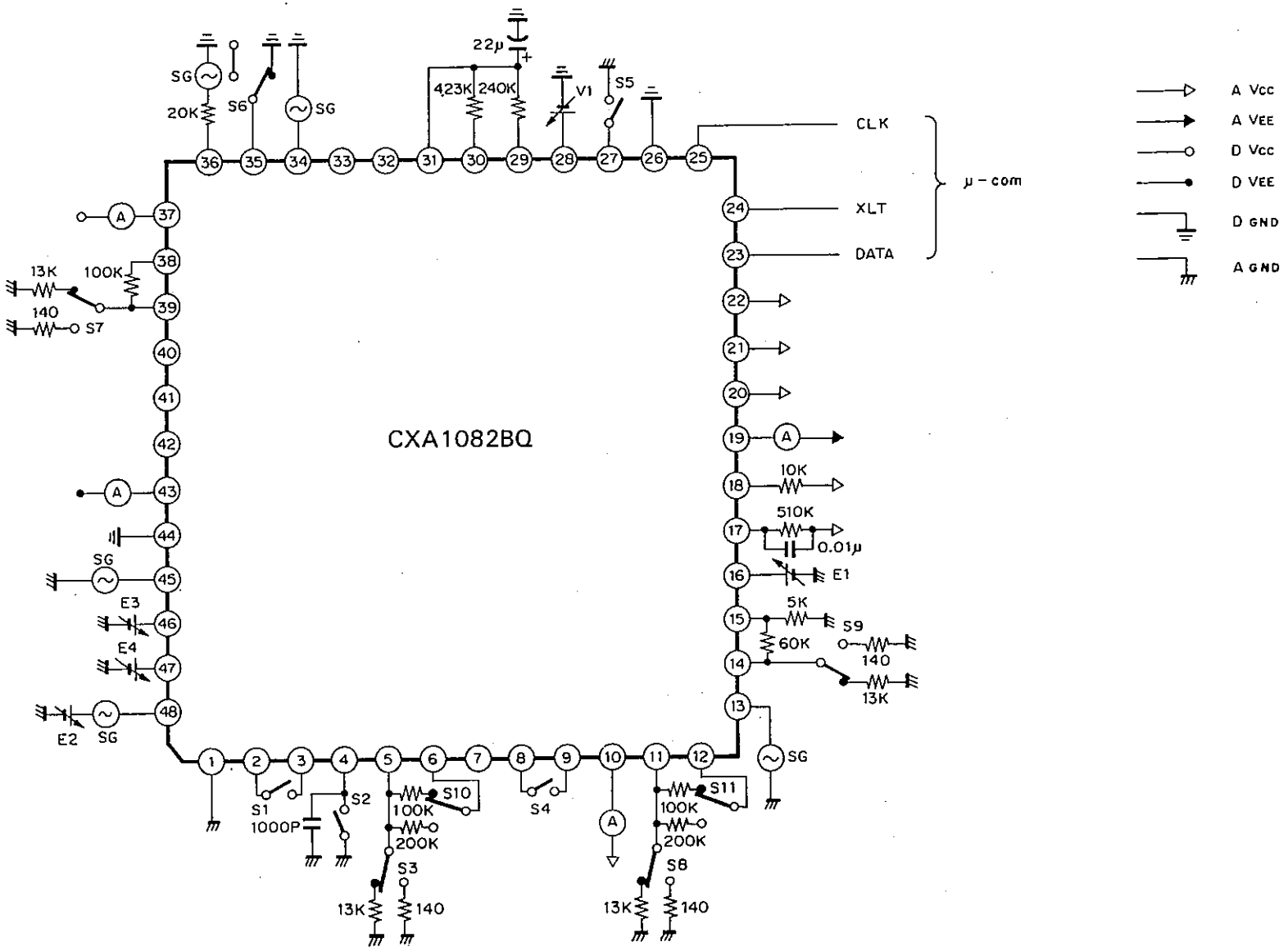
Test No.	Test items		Symbol	SW conditions											* SD	Bias conditions				Input point	Test point	Description of output waveform and test method	Min.	Typ.	Max.	Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11		E1	E2	E3	E4							
1	Supply current 1		AICC												00	0	0	0	0		10	Measure after resetting	2.8	5.5	8.2	mA
2	Supply current 2		DICC																		37		10.8	15.0	19.2	mA
3	Supply current 3		A, DIEE																		19 43		9.8	13.0	16.2	mA
4	Supply current 4		IDGND																		26		4.8	7.5	10.2	mA
5	Focus servo	DC voltage gain	GFEO												08					48	5	SG = 10Hz, 200mVp-p	18.0	21.0	24.0	dB
6		Feedthrough	VFEOF	O	O																	SG = 10kHz, 40mVp-p, Gain difference between 08 and 00 of SD			-35	dB
7		Max. output voltage 1	VFEO1										O		08							SG = 0.5VDC	1.98			V
8		Max. output voltage 2	VFEO2										O		08							SG = −0.5VDC			-1.98	V
9		Max. output voltage 3	VFEO3			O							O		08							SG = 0.5VDC	1.18			V
10		Max. output voltage 4	VFEO4			O							O		08							SG = −0.5VDC			-1.18	V
11		Search output voltage 1	VSRCH1												02								-0.64	-0.55	-0.36	V
12		Search output voltage 2	VSRCH2												03								0.36	0.55	0.64	V
13	Tracking servo	DC voltage gain	GTEO				O								25					45	11	SG = 10Hz, 500mVp-p	11.6	14.6	17.6	dB
14		Feedthrough	VTEOF				O								13							SG = 10kHz, 100mVp-p, Gain difference between 25 and 20 of SD			-39	dB
15		Max. output voltage 1	VTEP1											O	25							SG = −1.5VDC	1.98			V
16		Max. output voltage 2	VTEP2											O	25							SG = 1.5VDC			-1.98	V
17		Max. output voltage 3	VTEP3								O			O	25							SG = −1.5VDC	1.18			V
18		Max. output voltage 4	VTEP4								O			O	25							SG = 1.5VDC			-1.18	V
19		Jump output voltage 1	VJUMP1												2C								-0.64	-0.55	-0.36	V
20		Jump output voltage 2	VJUMP2												28								0.36	0.55	0.64	V
21	Sled servo	DC voltage gain	GSLO												25					13	14	SG = 10Hz Openloop gain	50	56	62	dB
22		Max. output voltage 1	VSLP1												25							SG = 0.4VDC	1.98			V
23		Max. output voltage 2	VSLP2												25							SG = −0.4VDC			-1.98	V
24		Max. output voltage 3	VSLP3									O			25							SG = 0.4VDC	1.18			V

*Serial data (hex)

Test No.	Test items		Symbol	SW conditions											* SD	Bias conditions				Input point	Test point	Description of output waveform and test method	Min.	Typ.	Max.	Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11		E1	E2	E3	E4							
25	Sled servo	Max. output voltage 4	VSLP4									O			25	0	0	0	0	13	14	SG = −0.4VDC			-1.18	V
26		Feed through	VSLOF																			SG=10kHz,200mVp-p,Gain difference between 25 and 20 of SD			-34	dB
27		Kick output voltage 1	VKICK1												22								-0.75	-0.6	-0.45	V
28		Kick output voltage 2	VKICK2												23								0.45	0.6	0.75	V
29	Spindle servo	Spindle servo gain	GSPO						O											34	39	SG = 10Hz, 200mVp-p	14	16.5	19	dB
30		Max. output voltage 1	VSPP1						O													SG = 1.0VDC	1.78			V
31		Max. output voltage 2	VSPP2						O													SG = −1.0VDC			-1.78	V
32		Max. output voltage 3	VSPP3						O	O												SG = 1.0VDC	1.13			V
33		Max. output voltage 4	VSPP4						O	O												SG = −1.0VDC			-1.13	V
34	PLL	PLL Reg. output voltage	Vreg																		31	DC voltage	3.3	3.5	3.85	V
35		Self-running frequency	FVCO														0				32	V_I = 0mV	7.4	8.6	9.7	MHz
36		Frequency deviation 1	ΔF_1																			Frequency deviation from FVCO, V_I = 148mV	7	11	15	%
37		Frequency deviation 2	ΔF_2																			V_I = −148mV	-15	-11	-7	%
38	SENS low level		VSENS																		18				-1.98	V
39	COUT low level		VCOUT																		20				-1.98	V
40	FZC threshold value		VTZC												00		*			48	18		39	50	61	mV
41	ATSC threshold value		VATSC1												10		0		*	47		* Value of E when SENS becomes High (=1.1V) by E1 to E4 varying	-45	-26	-7	mV
42	ATSC threshold value		VATSC2												10				*	47			7	26	45	mV
43	TZC threshold value		VTZC												20			*	0	46		SG = 0V	-20	0	20	mV
44	SSTOP threshold value		VSSTOP												30	*		0		16			-65	-50	-35	mV

Electrical Characteristics Test Circuit

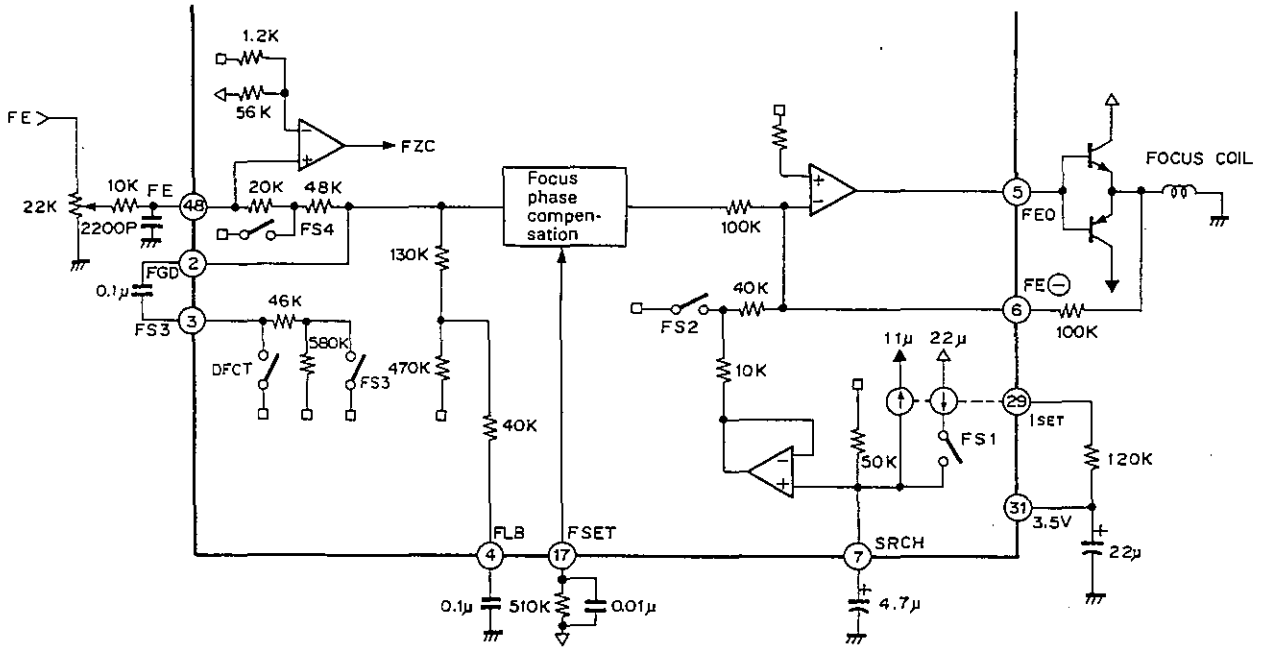
(See the Pin Configuration for CXA1082BS)



Description of Functions

Focus servo system

(See the Pin Configuration for CXA1082BS)



The above is a block diagram of the focus servo system.

When FS3 is switched on, the high frequency gain can be reduced by forming a low frequency time constant through a capacitor connected across pins 2 and 3 and the internal resistor.

The capacitor across the pin 4 and GND has a time constant to raise the low frequency usually playback condition.

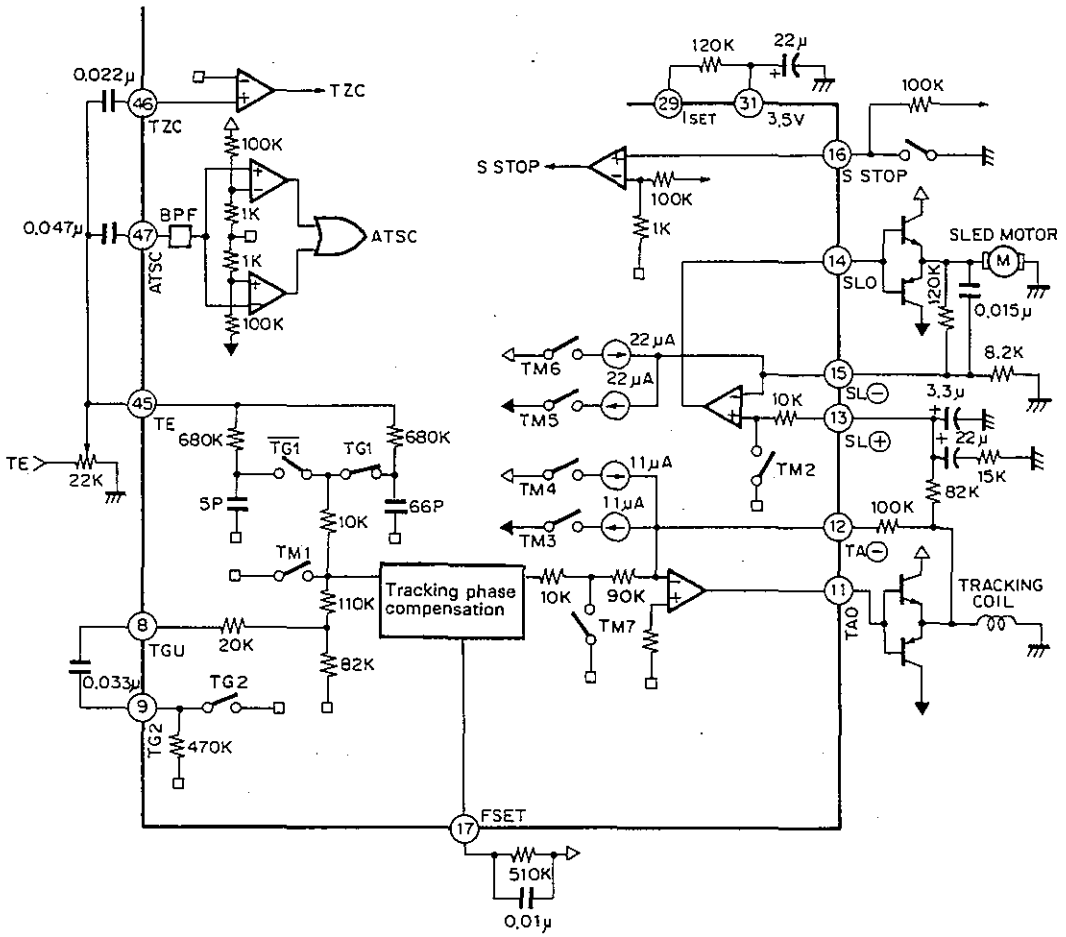
The peak frequency of the focus phase compensation is inversely proportional to the resistor connected to pin 17 (about 1.2 kHz when the resistor is 510 kΩ).

The focus search peak becomes about ± 1.1 Vp-p with the above constant. The peak is inversely proportional to the resistor connected across the pins 29 and 30. However, when this resistor is varied, the peaks of track jump and sled kick also vary.

The FZC comparator invert input is set to 2% of the difference between the reference voltage Vcc and VC (pin 1): 2% × (Vcc − VC).

Note) A resistor of 510 kΩ is recommended for pin 17.

Tracking sled servo system



The above is a block diagram of the tracking sled servo system.
The capacitor across pins 8 and 9 has a time constant to lower the high frequency when TG2 is switched off. The tracking phase compensation peak frequency is inversely proportional to the resistor connected to pin 17 (about 1.2 kHz when the resistor is 510 kΩ).

For a tracking jump in the FWD or REV direction, TM3 or TM4 are set to ON. At this time, the peak voltage fed to the tracking coil is determined by the TM3 and TM4 current values and the feedback resistor from pin 12. That is:

Track jump peak voltage = TM3 (TM4) current value x feedback resistor value

The FWD or REV sled kick is done by setting TM5 or TM6 to ON. At this time, the peak voltage added to the sled motor is determined by the TM5 or TM6 current value and the feedback resistor from pin 15.

Sled jump peak voltage = TM5 (TM6) current value x feedback resistor value

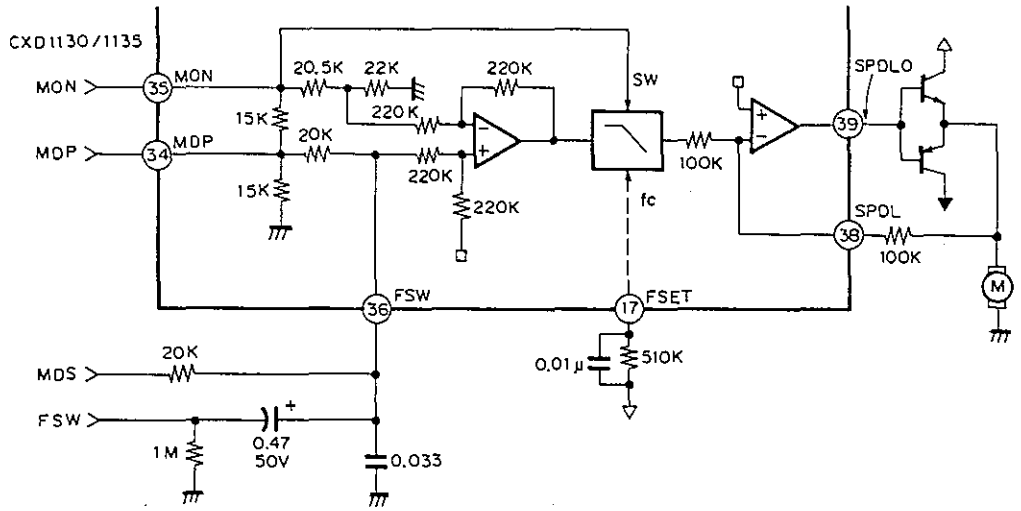
Each SW current value is determined by the resistor connected to pins 29 and 31.
When the resistor is at about 120 kΩ,

TM3 or TM4 is ±11 μA and TM5 or TM6 is ±22 μA.

This current value is almost inversely proportional to the resistor, variable within a range of about 5 to 40 μA for TM3.

S STOP is the ON/OFF detection signal for the limit SW of the sled motor's innermost circumference.

Spindle servo and LPF

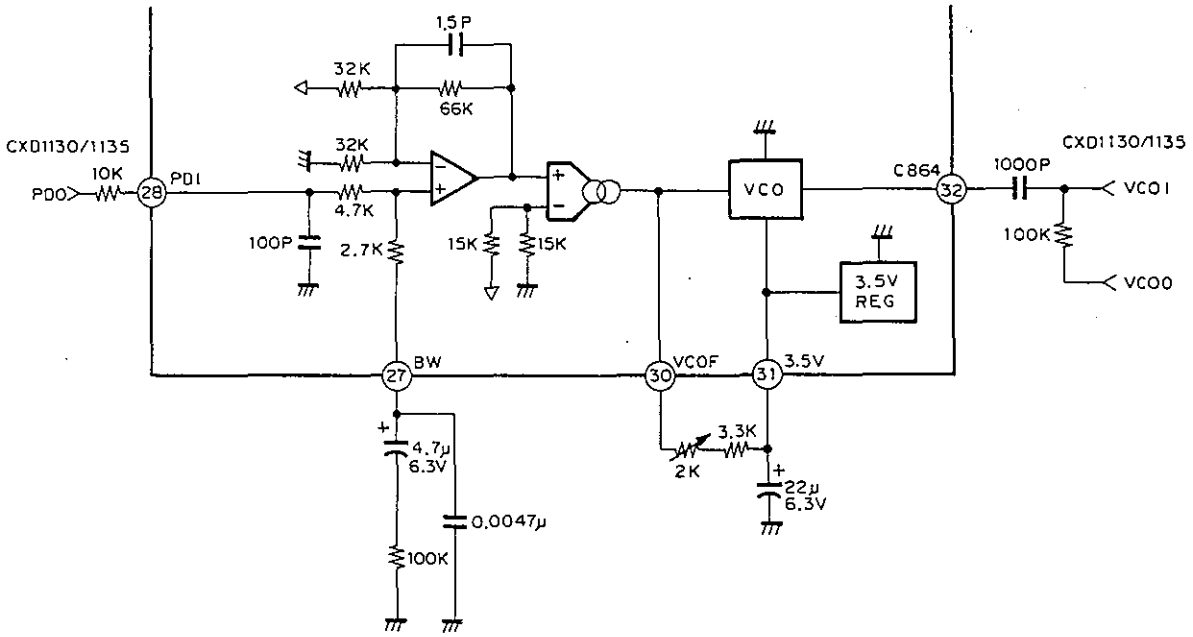


The 200 Hz LPF is formed with 0.033 μF and 20 kΩ connected to pin 36 and the secondary LPF is formed with the built-in LPF (fc up to 200 Hz with 510 kΩ for pin 17), and the carrier component of the CLV servo error signals MDS and MDP is eliminated.

In the CLV-S mode, FSW becomes L and the pin 36 LPF fc lowers, strengthening the filter further. With the pin 17 resistor connected to Vcc, fc does not vary with power supply voltage fluctuations.

Note) Use the phase compensation instead of MDS when the CX23035 is used.

VCO loop filter and 8.64 MHz VCO



The phase compensation output PDO input from pin 28 has its PWM carrier component removed in the loop filter. Then, the V-I conversion is made and the free-running frequency setting current from pin 30 is added to control the VCO frequency. The VCO self-running frequency is almost inversely proportional to the resistor across pins 30 and 31. This resistor is set so that the PLL capture range center matches the 4.3218 MHz at pin 70 of the CXD1135/1130.

Commands

The input data to activate this IC consists of 8-bits. It shall be represented as $XX in two hexadecimal digits. (X denotes 0 to F). Instructions for the CXA1082BQ are classified into 8 types — $0X to 7X.

1. $0X [SENSE Pin 18 is "FZC"]

This instruction is related to the focus servo control.

The bit configuration is as follows:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	FS4	FS3	FS2	FS1

The four switches FS1 to FS4 are related to focusing, and correspond to D0 to D3.

$00 At FS1 = 0, Pin 7 is charged to (22μA − 11μA) × 50 kΩ = 0.55 V).
If FS2 = 0, this voltage is not output and the output of Pin 5 remains 0 V.

$02 From the above state, FS2 only becomes 1 and a negative output is output to Pin 5. This voltage level is stipulated as follows:

$$(22\ \mu A - 11\ \mu A) \times 50\ k\Omega \times \frac{\text{Resistance value between Pin 5 and Pin 6}}{50\ k\Omega} \quad \cdots\cdots (1)$$

$03 From the above state, FS1 becomes 1 and the current supply of +22 μA is separated. Then, the CR charge/discharge circuit is formed and Pin 7 voltage decreases as time passes, as shown in Fig. 1.

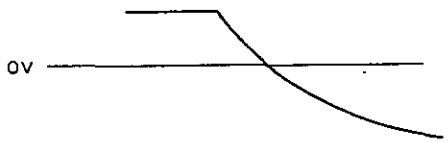


Fig. 1 Voltage of pin 7 as FS1 changes from 0 to 1

The time constant is formed by 50 kΩ and an external capacitor.

By giving instructions $02 and $03 alternately, the focus search voltage is produced (Fig. 2).

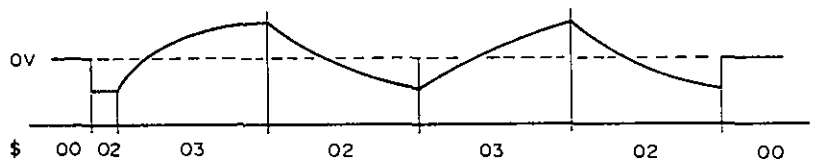


Fig. 2 Production of search voltage by $02 and $03
(Voltage of Pin 5)

1) Description of FS4

This switch is placed between the focus error input 48 and the focus phase compensation, serving to switch on and off the focus servo.

$00	→	$08
Focus off	←	Focus on

2) Focusing procedure

Assume the polarity as follows:

a) The lens moves away or toward the disc in searching.

b) At this time, the output voltage of Pin 5 varies from negative to positive.

c) Further, the focus S-curve changes as follows:

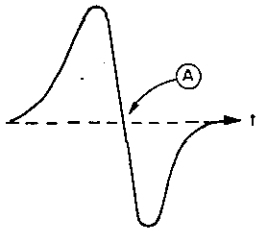


Fig. 3 S-curve

The focus servo is activated at the operating point of Ⓐ as shown in Fig. 3. Generally, a logical product (AND) with the Focus-OK signal is used to switch on the focus servo in focus searching and to prevent a malfunction while passing the Ⓐ point in Fig. 3.
This IC is designed so FZC (Focus Zero Cross) is output from the Sense Pin 18 as the Ⓐ point passing signal.
The Focus-OK indicates a signal is in focus (focus is enabled in this case). In summary, the following time chart shows how to obtain the focus.

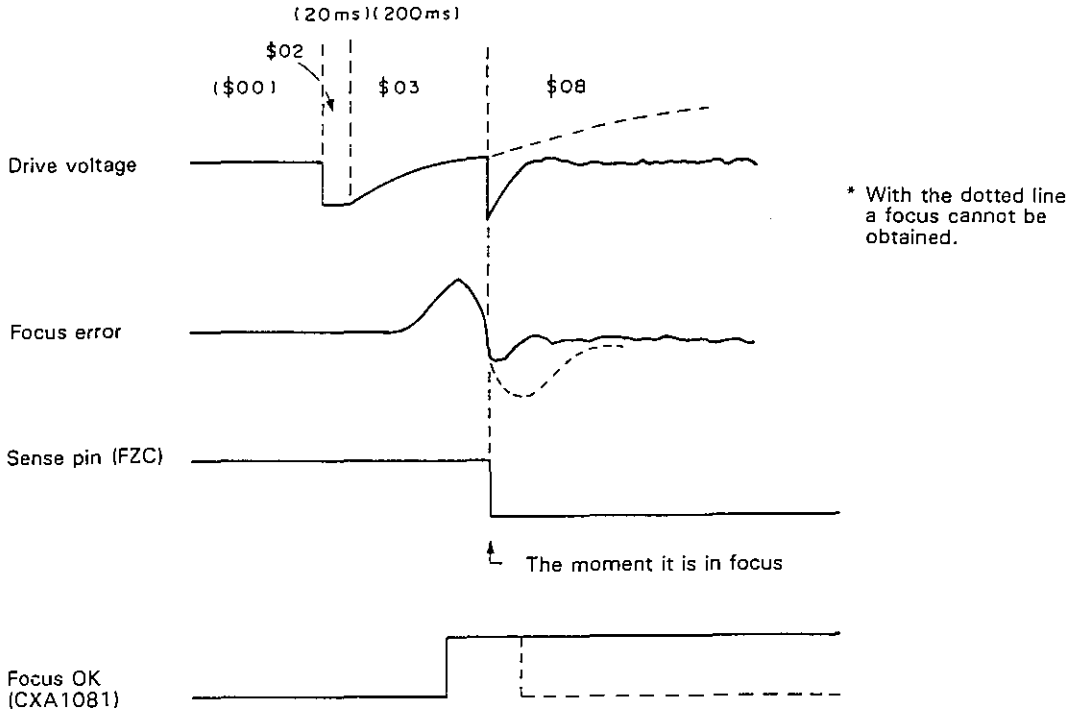


Fig. 4 Timing Chart of In-Focus

Care should be taken here that $08 is instructed in the shortest time after FZC changes from H to L.
For this purpose, the (b) sequence required for software is better than (a).

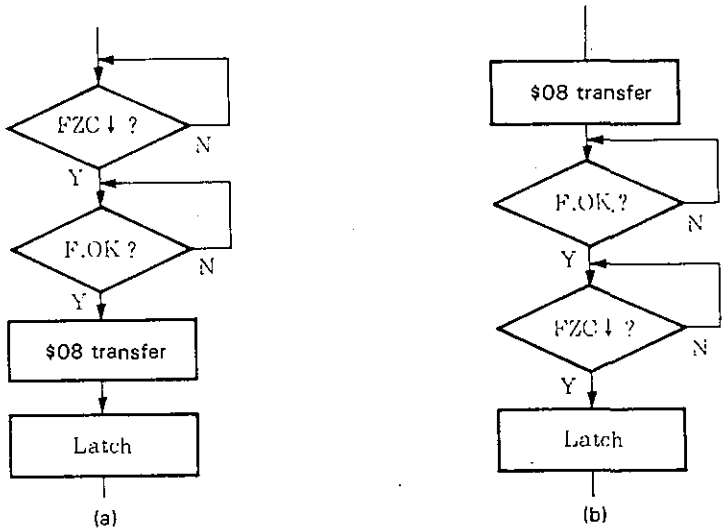


Fig. 5 Bad Sequence and Good Sequence

3) On the Sense Pin 18

What is output to the Sense Pin depends on input data as follows:

FZC is output with $0X.
AS is output with $1X.
TZC is output with $2X.
SSTOP is output with $3X.
$\overline{\text{BUSY}}$ is output with $4X.
HIGH-Z is output with $5X to 7X.

Higher instructions than $7X are codes for the CXD1135 and several outputs are obtained by connecting to the CXD1135 "SENS" pin.

2. $1X (SENS Pin 18 is "AS")

This instruction refers to ON/OFF of TG1, TG2 and the break circuit.
The bit configuration is as follows:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	ANTI SHOCK ON/OFF	Break Circuit ON/OFF	TG2	TG1

TG1, TG2

The purpose of these switches is to switch on or off Up/Normal of the tracking servo gain. The break circuit refers to a mechanism which prevents a volatile actuator servo circuit. After jumps of 100 tracks or 10 tracks, the servo circuit is out of the linear range and the actuator often sets tracks wrong. Using a feature that the RF envelope and the tracking error are out of phase by 180° when the actuator crosses the tracks outwardly and vice versa, unwanted tracking errors are cut to break this undesirable jumping.

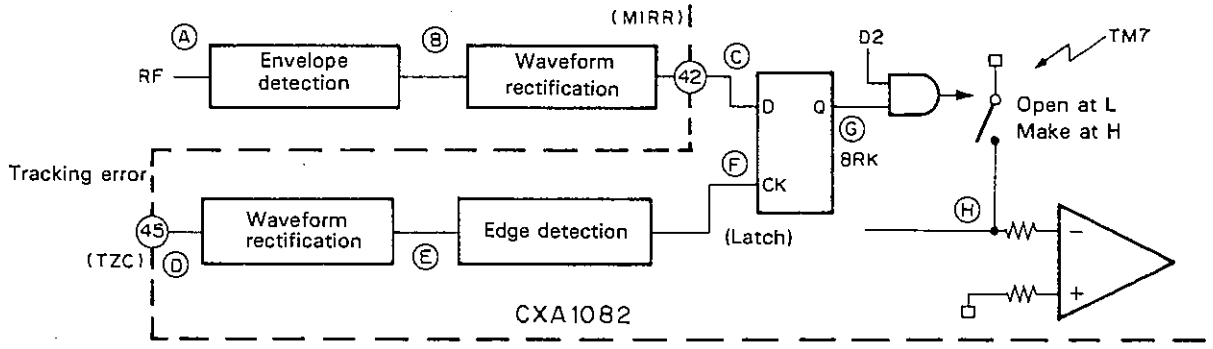


Fig. 6 TM7 Movement (Break Circuit)

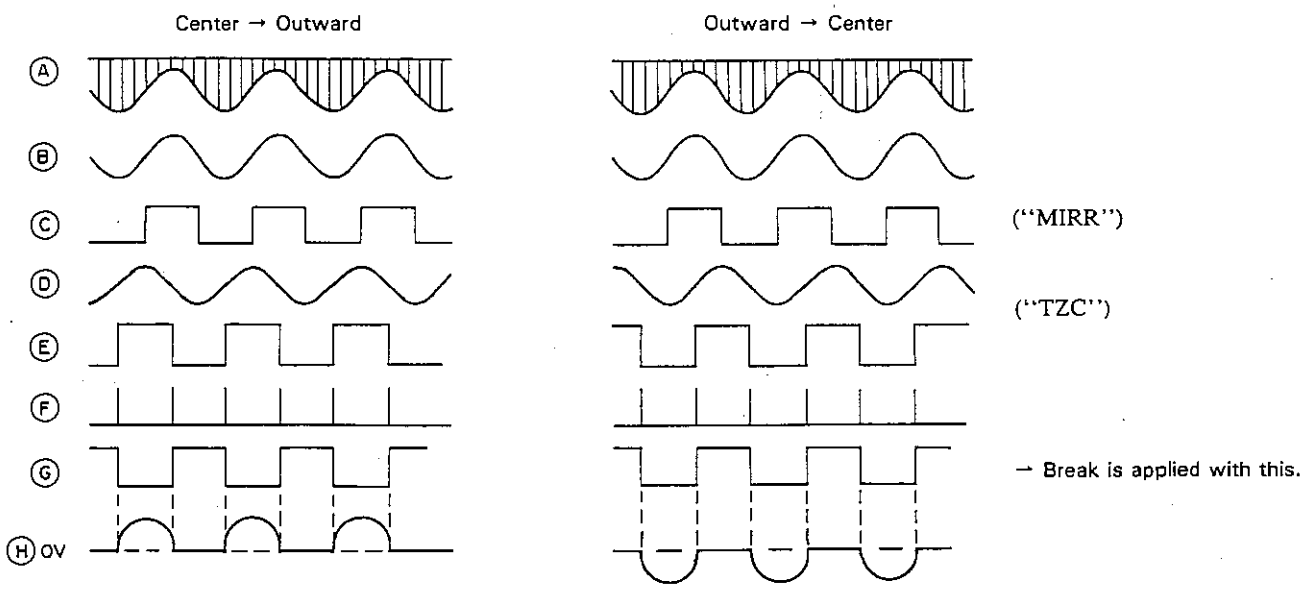


Fig. 7 External Waveform

3. $2X (SENS Pin 18 is "TZC")

This instruction refers to ON/OFF of the tracking servo and thread servo as well as generation of the jump pulse and speed feeding pulse in accessing.

D7	D6	D5	D4	D3 D2	D1 D0
0	0	1	0	Tracking control	Sled control
				00 off	00 off
				01 Servo ON	01 Servo ON
				10 F-JUMP	10 F-speed feed
				11 R-JUMP	11 R-speed feed
				⇩	⇩
				TM1,TM3,TM4	TM2,TM5,TM6

DIRC Pin 21 and 1 Track Jump

Generally, for a 1-track jump, an acceleration pulse is added and a deceleration pulse is given for a specified time from the moment a tracking error passes the 0 point; then the tracking servo is switched on again. For the 100-track jump to be explained in the next item, as long as the number of tracks is about 100 there is no problem, but the 1-track jump must be exactly, requiring the above complicated procedure. For a 1-track jump of a CD player, both the acceleration and deceleration take about 300 to 400 μs. When software is used to execute this operation, it will be as in the flow chart of Fig. 9, but practically it takes time to transfer data.

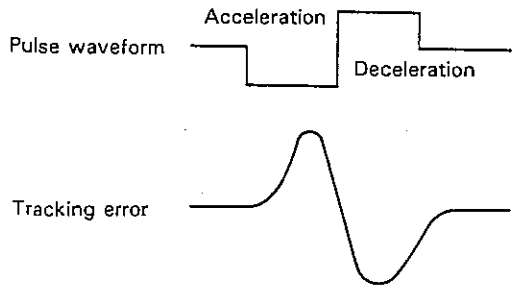


Fig. 8 Pulse Waveform and Tracking Error of 1-Track Jump

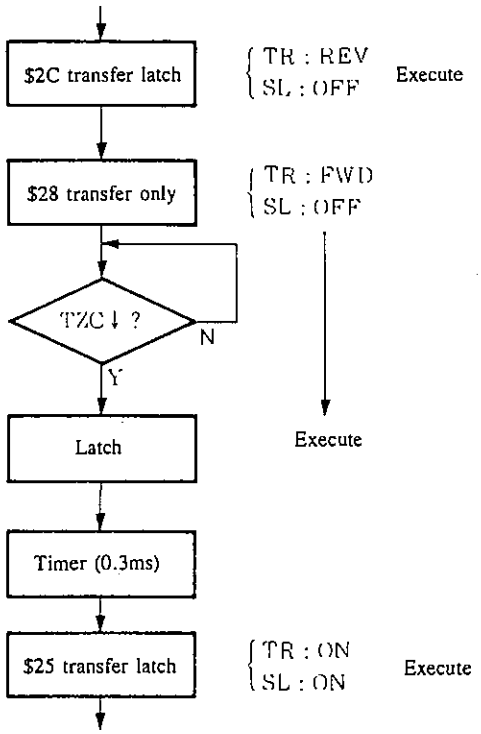


Fig. 9 1-Track Jump without DIRC 21

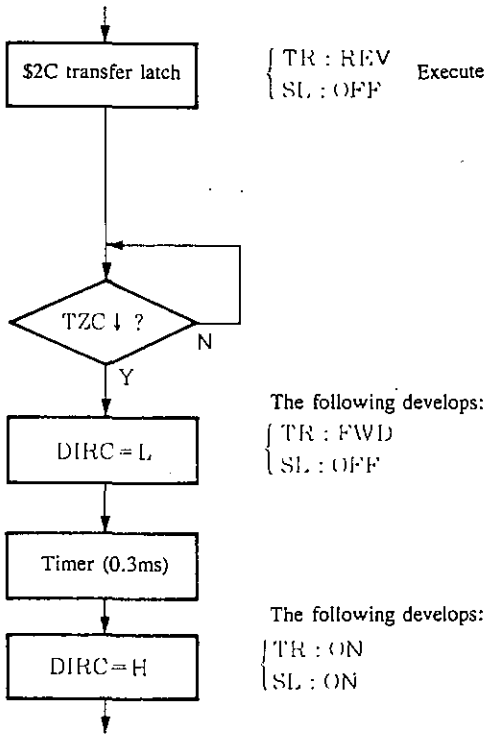


Fig. 10 1-Track Jump with DIRC 21

For this IC, the "DIRC" (Direct Control) Pin is provided for simple 1-track jumping.
For 1-track jump using DIRC, the following is undertaken (DIRC = normal H).

(a) Acceleration pulse is output. ($2C for REV or $28 for FWD).

(b) With TZC ↓ (or TZC ↑), set DIRC to L. (SENS Pin 18 is "TZC"). As the jump pulse polarity is inverted, deceleration is applied.

(c) Set DIRC to H for a specific time.
Both the tracking servo and sled servo are switched on automatically.
As a result, the track jump will be as shown in the flow chart of Fig. 10 and two serial data transfers are saved.

4. $3X

This command is for switching the Focus search and Sled kick peak value.

D0, D1 ..... Sled, NORMAL feed, high-speed feed

D2, D3 ..... Focus search peak switching

D7	D6	D5	D4	Focus search peak		Sled kick peak		Relative value
				D3 (PS3)	D2 (PS2)	D1 (PS1)	D0 (PS0)	
0	0	1	1	0	0	0	0	± 1
				0	1	0	1	± 2
				1	0	1	0	± 3
				1	1	1	1	± 4

5. $4X to $7X

$4X to $7X are for the auto sequencer commands. Refer to the table and timing chart for the auto sequencer.

The auto sequencer automates the troublesome routines of focus pull-in and track jump, eliminating any timing control of the microcomputer that is less than 10 ms and combining with the Q register of the CXD1135, CXD1125, CXD1130 and CX23035.

- Auto focus

When a focus is pull-in during the $\overline{\text{BUSY}}$ shifts H → L → H, the $08 is automatically set in the register. Even when it is out of focus, no auto pull-in is done requiring FOK to be monitored.

- Track jump

When the $\overline{\text{BUSY}}$ shifts H → L → H and the track jump is completed, the $25 is automatically set in the register.

Sequencer malfunctions can be relieved with the $40 anytime.

Others

1. Connection of the power supply pin

	V_{CC}	V_{EE}	VC
±5 V dual power supply	+5V	−5V	0V
5 V single power supply	+5V	0V	VC*

* CXA1081

2. FSET pin

The FSET pin determines the characteristic of the high frequency phase compensation of Focus, Tracking servo, and cut-off frequency (fc) of CLV LPF.

3. ISET pin

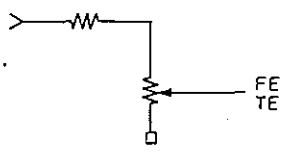
ISET current = 1.27 V/R
= Focus search current ($30)
= Tracking kick current
= 1/2 sled kick current ($30)

4. In the tracking amplifier, input is clamped at 1 V_{BE} to prevent over input.

5. How to change the FE and TE gains

(1) To increase: Pins ⑤ and ⑥ , pins ⑪ and ⑫ to more than 100 kΩ.

(2) To decrease: Divide the FE and TE resistor of input.

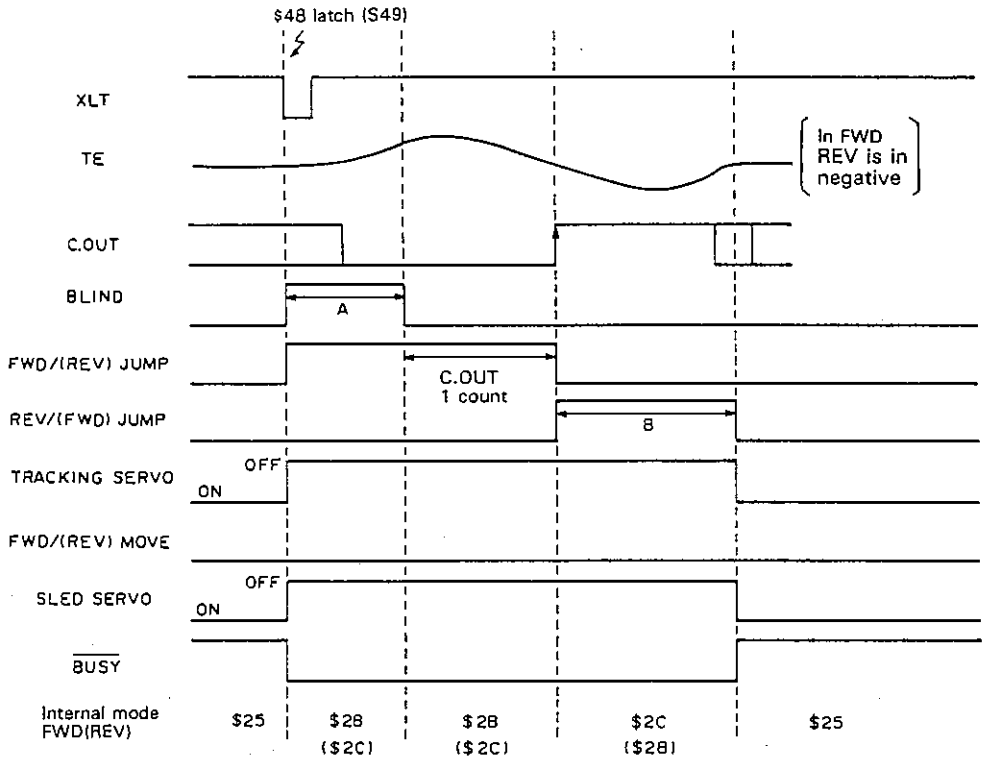


6. Tracking servo phase

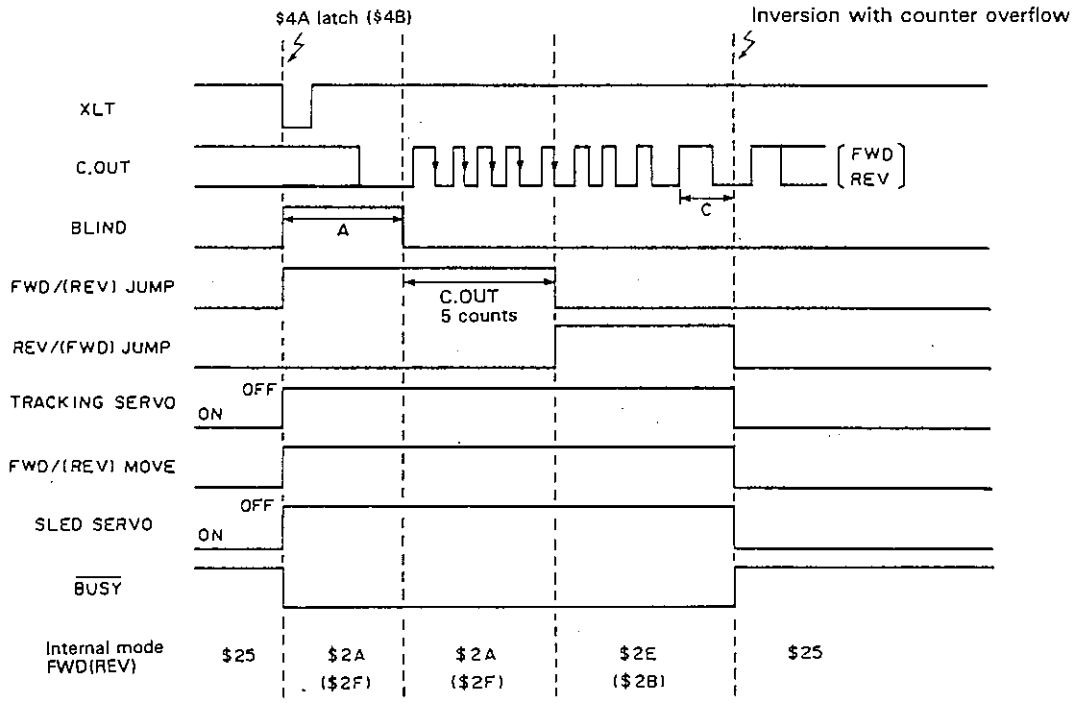
From TE to TAO the phase is negative. (CXA20108 has a positive phase.)

Auto Sequencer Timing Chart

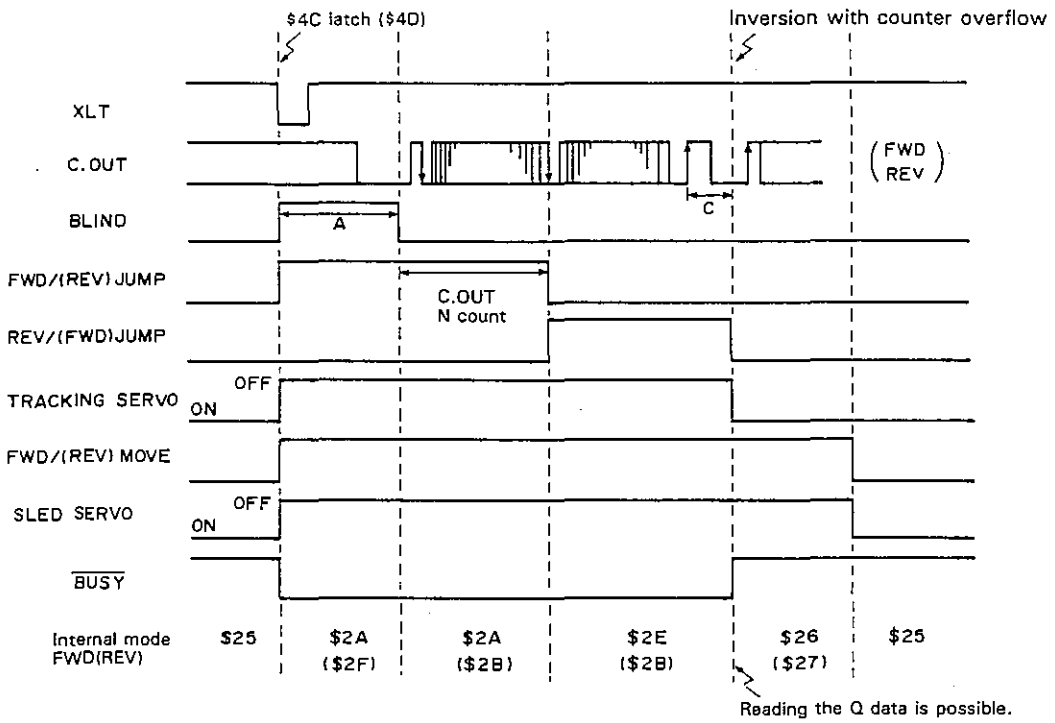
1. 1 track jump



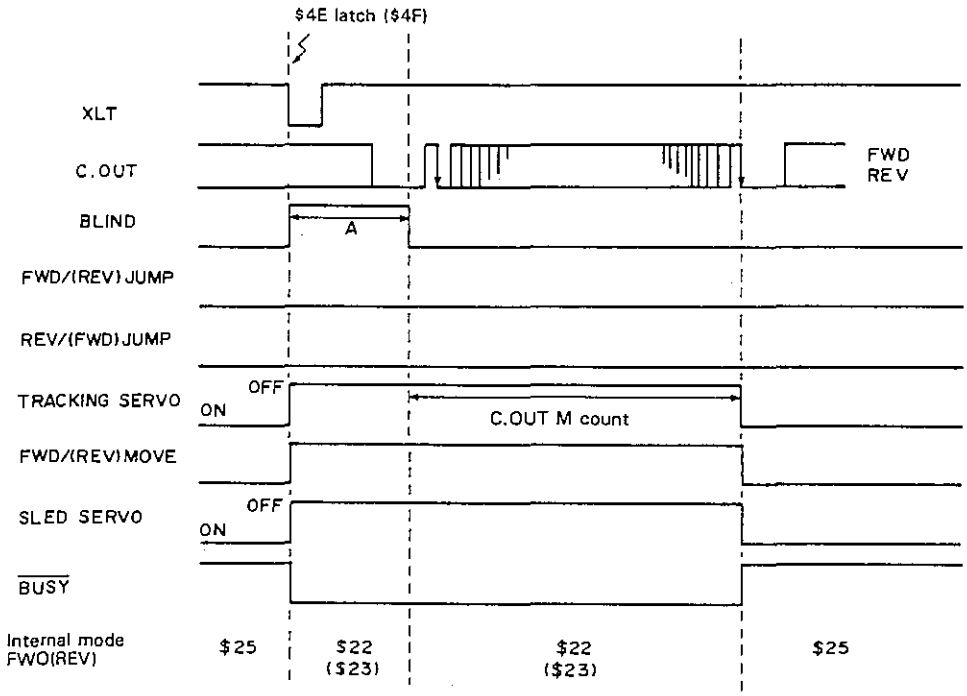
2. 10 track jump



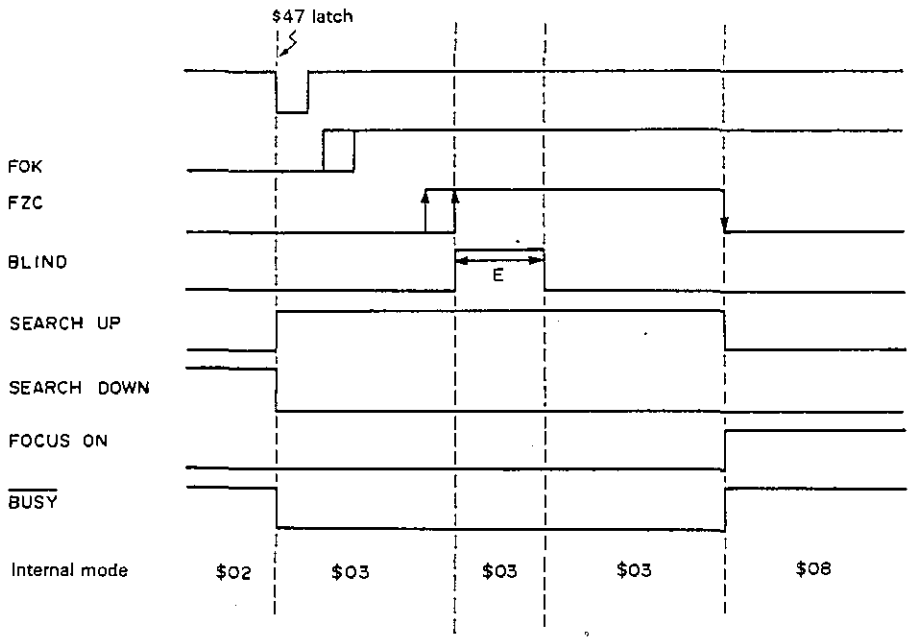
3. 2N track jump



4. M track movement



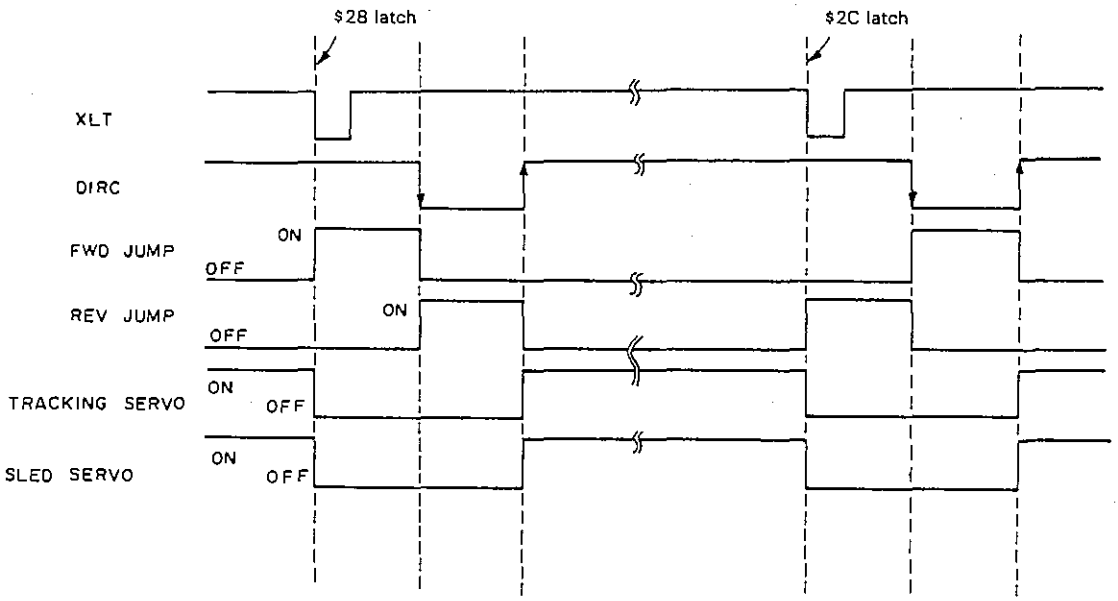
5. Auto focus



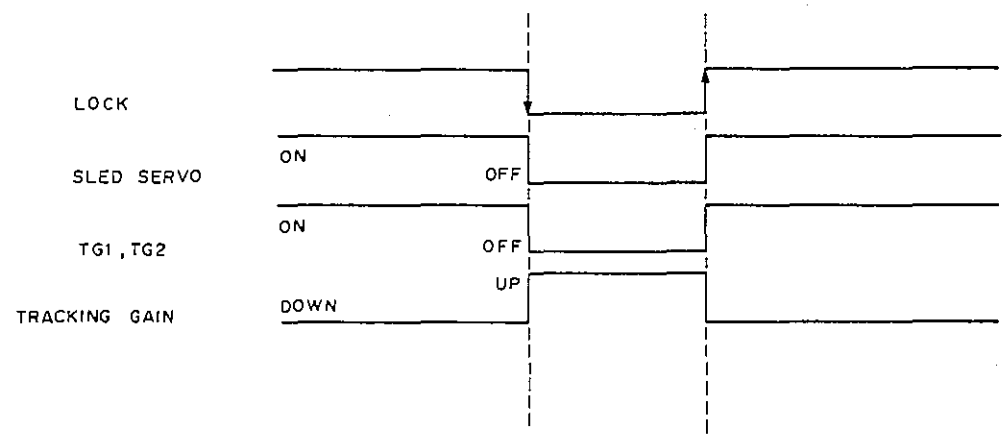
6. Notes on use of the auto sequence
   1) The horizontal axis of the timing chart is not always proportional to the actual time.
   2) Use the auto focus only while the search is down.
      Use the track jump while the focus, tracking, and sled servo are switched on.
   3) The auto sequencer does not cover tracking gain up, brake, anti-shock, and focus gain down. Separate commands are required.
   4) BUSY does not tell the full status of the player. Monitor FOK and GFS, etc. using the microcomputer.
   5) When the sequencer hangs up, detect BUSY's max. excess time using the microcomputer and send $40 (CANCEL) to reset to the preceding status.
   6) In all modes the auto sequence starts from the first WDCK falling edge right after XLT falls.

Parallel Direct Interface

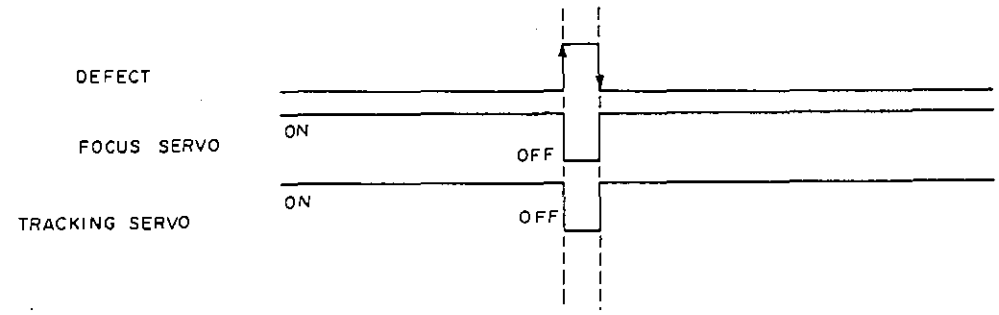
1. DIRC



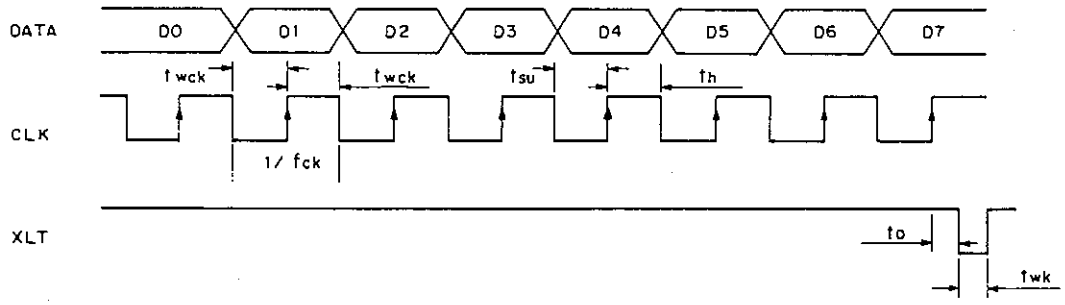
2. LOCK (Sled runaway prevention circuit)



3. DEFECT (Disc defect countermeasure circuit)



CPU Serial Interface Timing Chart



DVcc – DGND = 4.5 to 5.5V

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{ck}			1	MHz
Clock pulse width	f_{wck}	500			ns
Hold time	t_{su}	500			ns
Setup time	t_h	500			ns
Delay time	t_D	500			ns
Latch pulse width	t_{WL}	1000			ns

System Control

Item		ADDRESS	DATA				SENS Output
		D7D6D5D4	D3	D2	D1	D0	
Focus Control		0 0 0 0	FS4 Focus ON	FS3 Gain Down	FS2 Search ON	FS1 Search Up	FZC
Tracking Control		0 0 0 1	Anti Shock	Brake ON	TG2 Gain Set *1	TG1	A.S
Tracking Mode		0 0 1 0	Tracking Mode *2		Sled Mode *3		TZC
Select		0 0 1 1	PS4 Focus Search+2	PS3 Focus Search+1	PS2 Sled Kick+2	PS1 Sled Kick+1	SSTOP
Auto Sequence *4		0 1 0 0	AS3	AS2	AS1	AS0	$\overline{BUSY}$
*5 RAM SET	Blind (A, E)/Overflow (C)	0 1 0 1	0.18ms	0.09ms	0.045ms	0.022ms	Hi-Z
	Brake (B)		0.36ms	0.18ms	0.09ms	0.045ms	
	Kick (D)	0 1 1 0	11.6ms	5.8ms	2.9ms	1.45ms	
	Track Jump (N)	0 1 1 1	64	32	16	8	
	Track Move (M)		128	64	32	16	

Note)*1. GAIN SET
It is possible to set TG1 and TG2 independently.
When the anti-shock is 1 (00011xxx), invert both TG1 and TG2 when the internal anti-shock is H.

* 2 TRACKING MODE

	D3	D2
OFF	0	0
ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

* 3 SLED MODE

	D1	D0
OFF	0	0
ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

* 4 AUTO SEQUENCE

	AS3	AS2	AS1	AS0
CANCEL	0	0	0	0
FOCUS ON	0	1	1	1
1 TRACK JUMP	1	0	0	X
10 TRACK JUMP	1	0	1	X
2N TRACK JUMP	1	1	0	X
M TRACK MOVE	1	1	1	X

X = 0 FORWARD
X = 1 REVERSE

- When CANCEL $40 is sent, the status immediately preceding the auto sequence mode (just before $4X is sent) is reset.
- The auto sequence mode starts with the first falling of the pin 40 input pulse (WDCK) after the $4X transfer and the falling of latch pulse.

*5 RAM·SET

- Values $1 to $E (not $0, $F) can be set.
- The above set values are ones when WDCK (88.2 kHz) is input to pin 40.
- The RAM is preset when the power is switched on and the internal initial set values are as follows:

ADDRESS	DATA
0 1 0 1	0 1 0 1
0 1 1 0	0 1 1 1
0 1 1 1	1 1 1 0

- The actual count values are slightly different from the set values.

A	set value + 4 to 5	WDCK
B, D, E	set value + 3	WDCK
C	set value + 5	WDCK
N, M	set value + 3	Count out

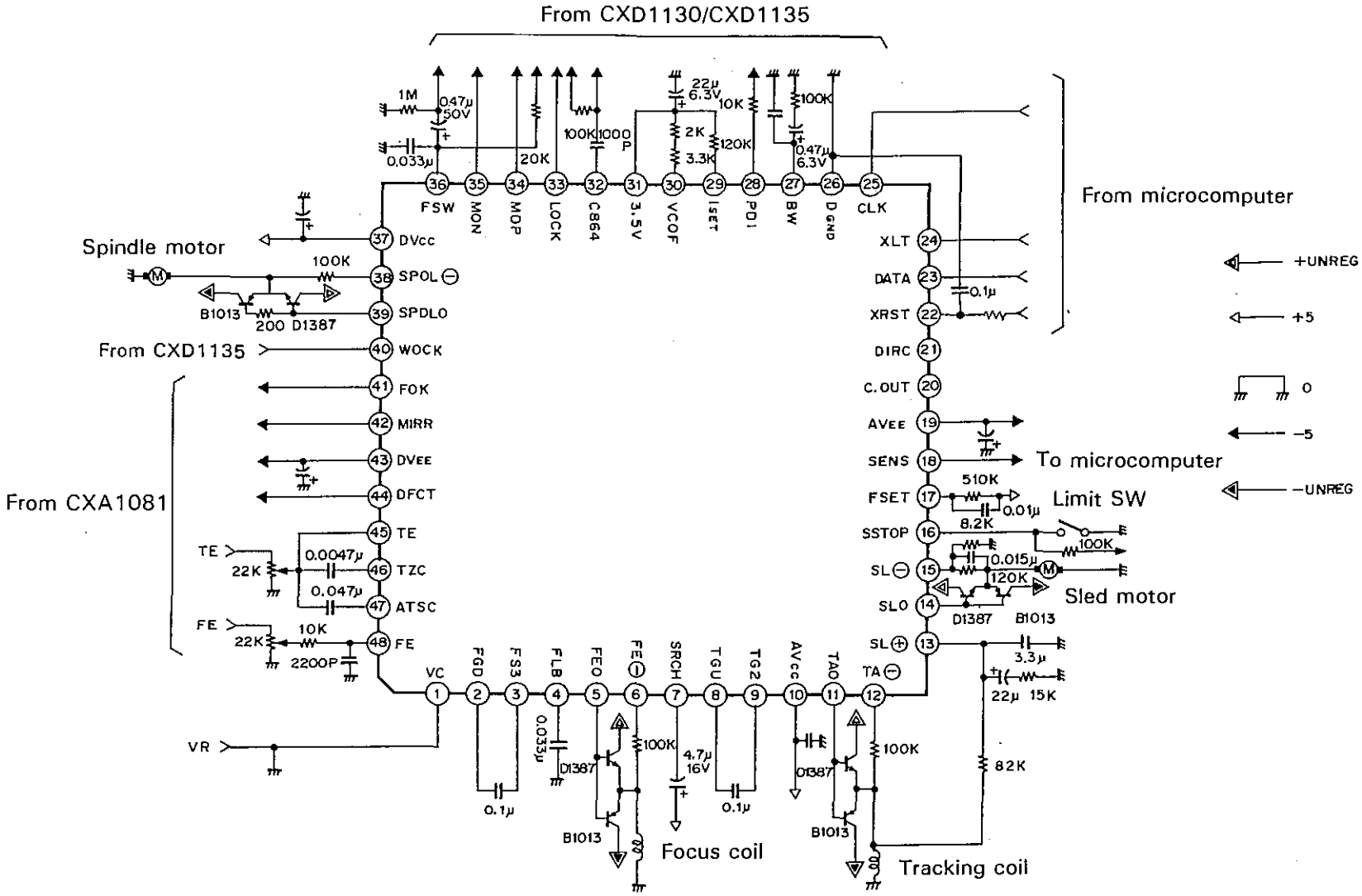
Serial Data Truth Table

Serial data	Hexa.	Function					
FOCUS CONTROL		FS = 4321					
0 0 0 0 0 0 0 0	$00	0 0 0 0					
0 0 0 0 0 0 0 1	$01	0 0 0 1					
0 0 0 0 0 0 1 0	$02	0 0 1 0					
0 0 0 0 0 0 1 1	$03	0 0 1 1					
0 0 0 0 0 1 0 0	$04	0 1 0 0					
0 0 0 0 0 1 0 1	$05	0 1 0 1					
0 0 0 0 0 1 1 0	$06	0 1 1 0					
0 0 0 0 0 1 1 1	$07	0 1 1 1					
0 0 0 0 1 0 0 0	$08	1 0 0 0					
0 0 0 0 1 0 0 1	$09	1 0 0 1					
0 0 0 0 1 0 1 0	$0A	1 0 1 0					
0 0 0 0 1 0 1 1	$0B	1 0 1 1					
0 0 0 0 1 1 0 0	$0C	1 1 0 0					
0 0 0 0 1 1 0 1	$0D	1 1 0 1					
0 0 0 0 1 1 1 0	$0E	1 1 1 0					
0 0 0 0 1 1 1 1	$0F	1 1 1 1					
TRACKING CONTROL		AS = 0			AS = 1		
		TG =	2	1	TG =	2	1
0 0 0 1 0 0 0 0	$10		0	0		0	0
0 0 0 1 0 0 0 1	$11		0	1		0	1
0 0 0 1 0 0 1 0	$12		1	0		1	0
0 0 0 1 0 0 1 1	$13		1	1		1	1
0 0 0 1 0 1 0 0	$14		0	0		0	0
0 0 0 1 0 1 0 1	$15		0	1		0	1
0 0 0 1 0 1 1 0	$16		1	0		1	0
0 0 0 1 0 1 1 1	$17		1	1		1	1
0 0 0 1 1 0 0 0	$18		0	0		1	1
0 0 0 1 1 0 0 1	$19		0	1		1	0
0 0 0 1 1 0 1 0	$1A		1	0		0	1
0 0 0 1 1 0 1 1	$1B		1	1		0	0
0 0 0 1 1 1 0 0	$1C		0	0		1	1
0 0 0 1 1 1 0 1	$1D		0	1		1	0
0 0 0 1 1 1 1 0	$1E		1	0		0	1
0 0 0 1 1 1 1 1	$1F		1	1		0	0

Serial data	Hexa.	Function		
TRACKING MODE		DIRC=1 TM= 654321	DIRC=0 654321	DIRC=1 654321
0 0 1 0 0 0 0 0	$20	000000	001000	000011
0 0 1 0 0 0 0 1	$21	000010	001010	000011
0 0 1 0 0 0 1 0	$22	010000	011000	100001
0 0 1 0 0 0 1 1	$23	100000	101000	100001
0 0 1 0 0 1 0 0	$24	000001	000100	000011
0 0 1 0 0 1 0 1	$25	000011	000110	000011
0 0 1 0 0 1 1 0	$26	010001	010100	100001
0 0 1 0 0 1 1 1	$27	100001	100100	100001
0 0 1 0 1 0 0 0	$28	000100	001000	000011
0 0 1 0 1 0 0 1	$29	000110	001010	000011
0 0 1 0 1 0 1 0	$2A	010100	011000	100001
0 0 1 0 1 0 1 1	$2B	100100	101000	100001
0 0 1 0 1 1 0 0	$2C	001000	000100	000011
0 0 1 0 1 1 0 1	$2D	001010	000110	000011
0 0 1 0 1 1 1 0	$2E	011000	010100	100001
0 0 1 0 1 1 1 1	$2F	101000	100100	100001

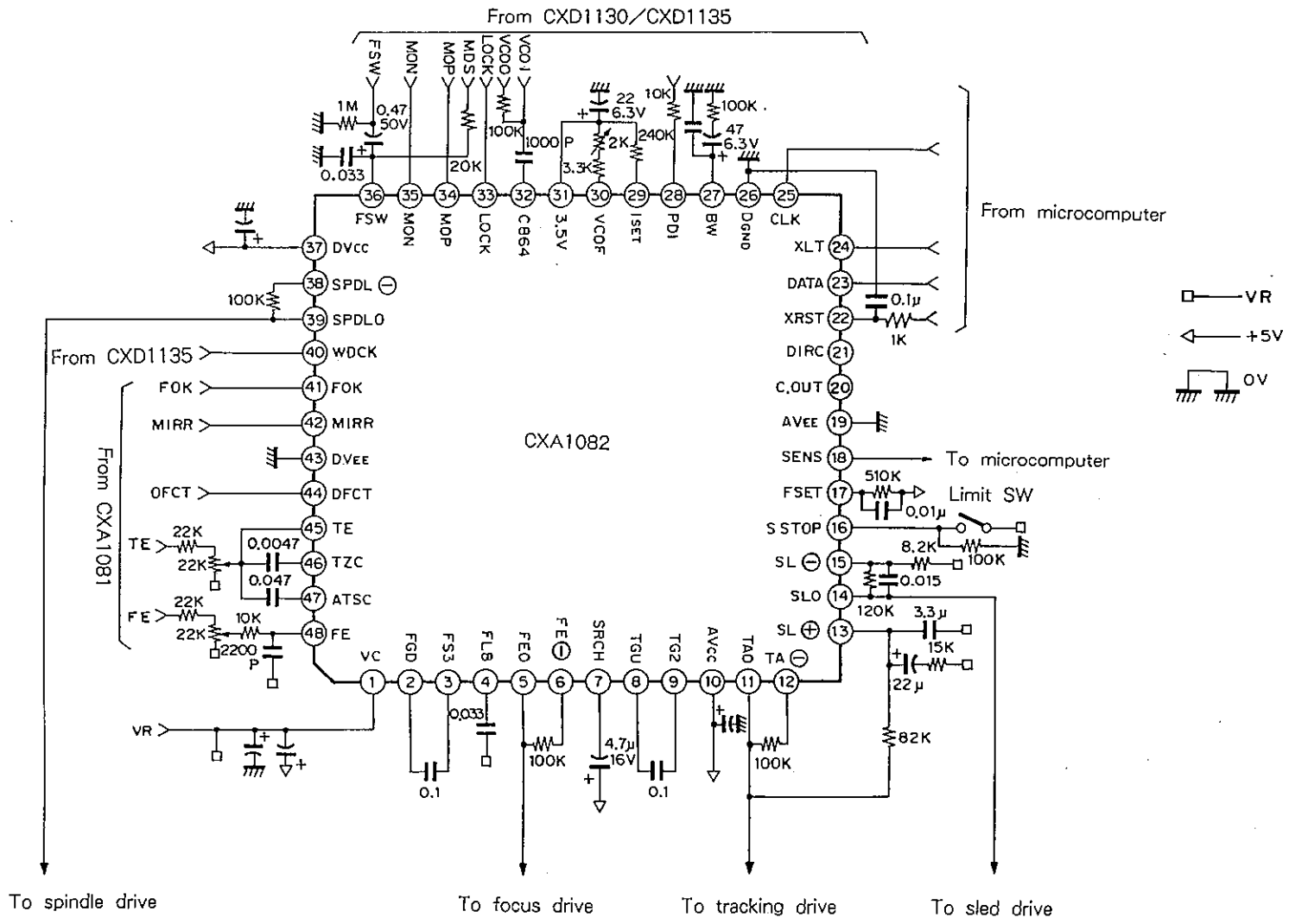
Application Circuit

1. ±5 V dual power supply for CXA1082BQ (48 pin QFP)
   (See the Pin Configuration for CXA1082BS)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

2. +5 V single power supply for CXA1082BQ (See the Pin Configuration for CXA1082BS)

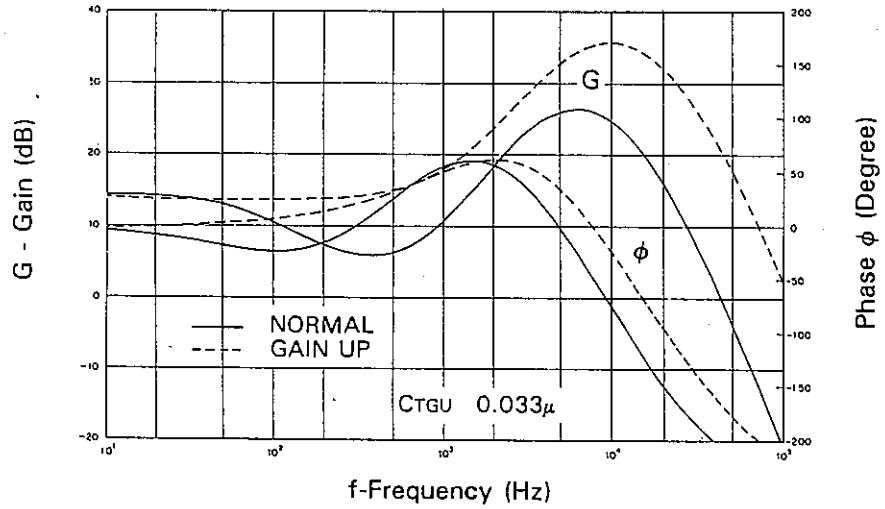


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

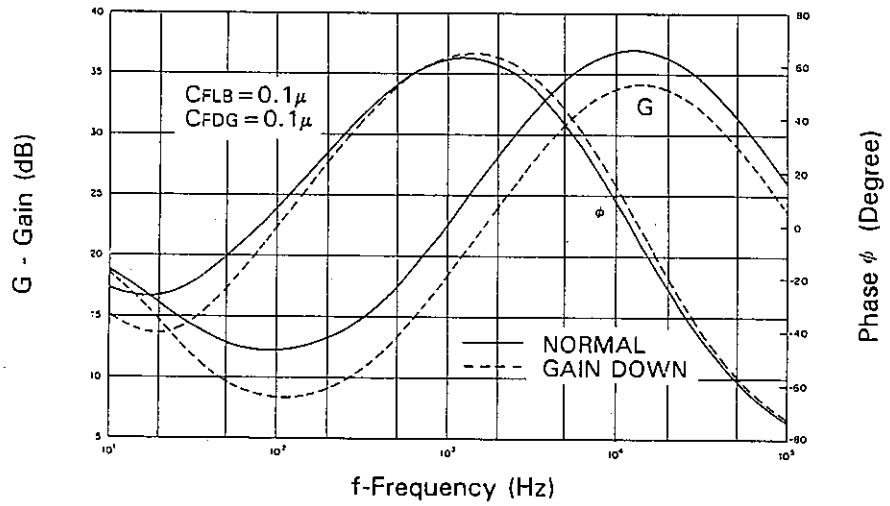
Internal Phase Compensation Standard Circuit Design Data

Mode	Item	Symbol	SW conditions									SD	Bias conditions				Input point	Test point	Output waveform and description of test methods	Min.	Typ.	Max.	Unit
			S1	S2	S3	S4	S5	S6	S7	S8	S9												
Focus	1. 2 kHz gain		O	O								08					48	5			21.5		dB
	1. 2 kHz phase		O	O								08									63		deg
	1. 2 kHz gain		O	O								0C									16		dB
	1. 2 kHz phase		O	O								0C									63		deg
Tracking	1. 2 kHz gain					O						25					45	11			13		dB
	1. 2 kHz phase					O						25									-125		deg
	2. 7 kHz gain					O						25									26.5		dB
	2. 7 kHz phase					O						25									-130		deg
Spindle	100 Hz phase																34	39			-30		deg
	2 kHz gain																				-3.5		dB

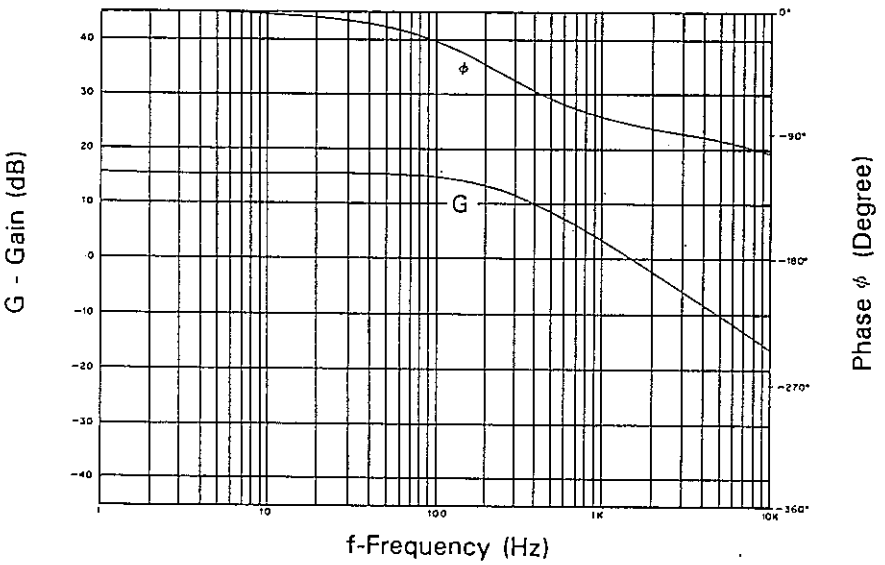
Tracking frequency characteristics



FOCUS frequency characteristics

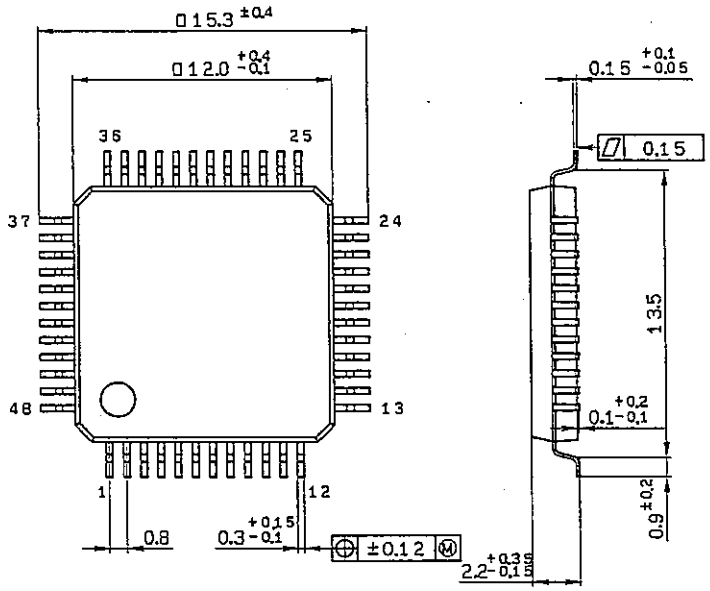


CLV frequency characteristics



Package Outline Unit : mm

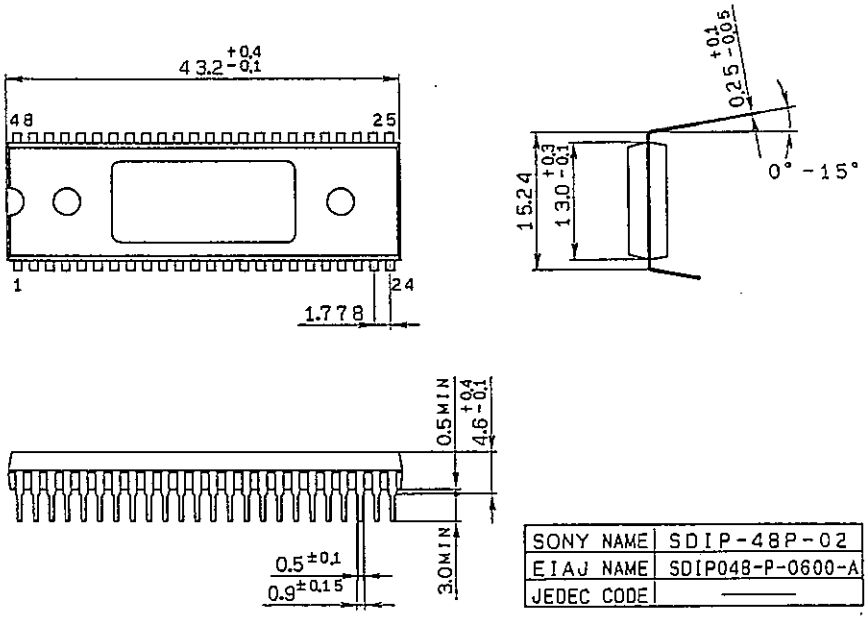
CXA1082BQ 48pin QFP (Plastic) 0.7g



SONY NAME	QFP-48P-L04
EIAJ NAME	*QFP048-P-1212-B
JEDEC CODE	

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).

CXA1082BS 48pin SDIP (Plastic) 600mil 5.1g



SONY NAME	SDIP-48P-02
EIAJ NAME	SDIP048-P-0600-A
JEDEC CODE	

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).