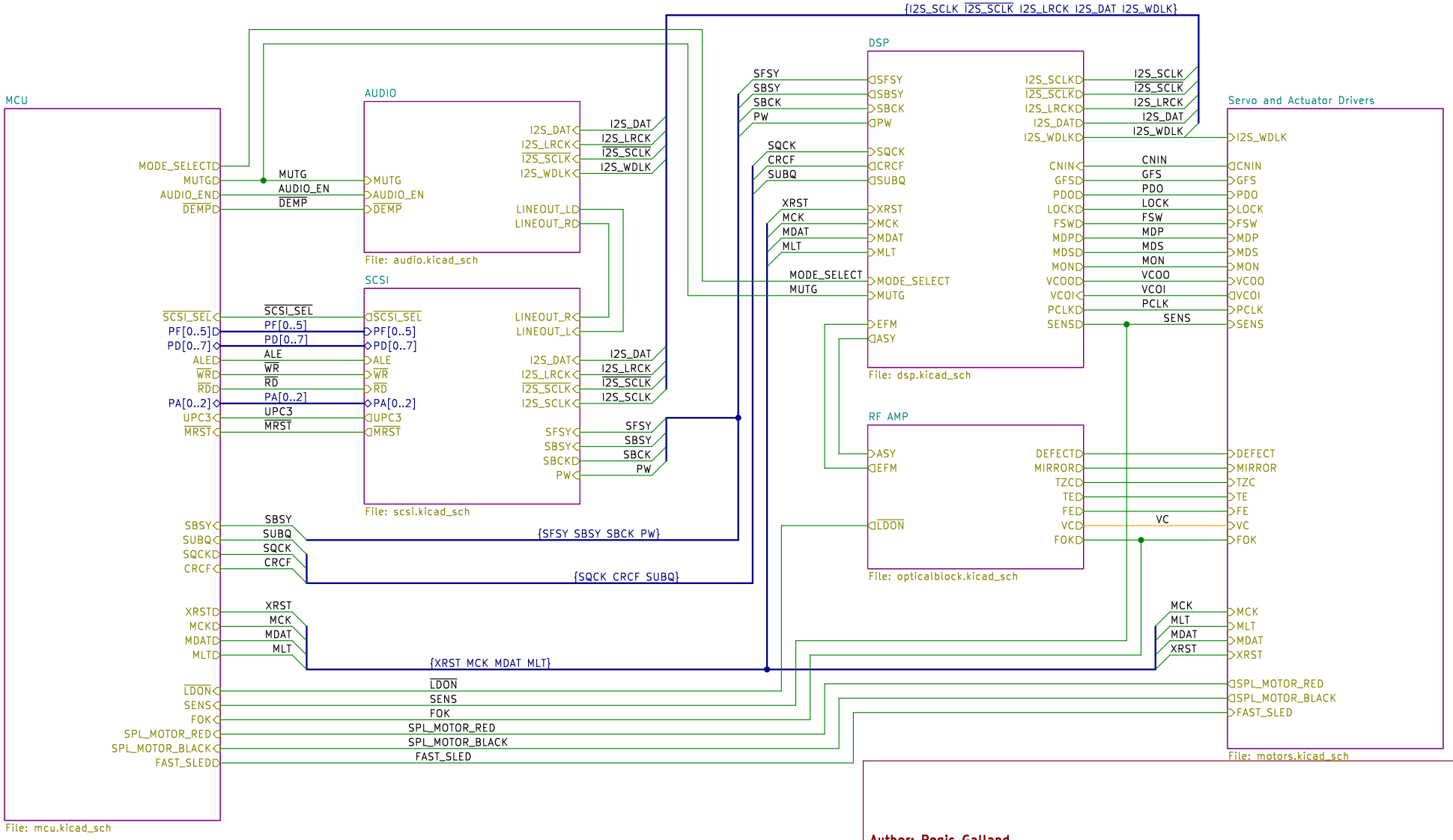
SOT23 Transistor with AAR22 Marking = NPN BEC
SOT23 Transistor with BR22 Marking = NPN BEC

Mentions some differences between the CDR-30A and the older CDR-30 revision.

PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR
Top Level



Author: Regis Galland		
Sheet: /		
File: MAIN_PWR.kicad_sch		
Title: PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR		
Size: A4	Date: 2024-07-19	**Rev: 0.2**
KiCad E.D.A. 8.0.6		Id: 1/7

RF AMP

Notes:
- R198 is relerenced as R135 and R199 does not exist on the CDR-30 revision
- LDON, FOK connected to micro
- EFM connected to DSP
- FOK, MIRROR and DEFECT connected to servo signal processor
- VC comes from VR pin which has an op amp configured as a follower with VCC/2
- CRD-30 revision uses KSM-162 instead of KSM-220

D101 is protection diode?

Test connector for viewing the RF signal and shorting ASY for adjusting VCO
Looks like provision for LDON was made next to pin 1 as the silkscreen seems to indicate but not populated

Pitch is 1.2mm

KSM-220 or KSM-162 Optical Pick-Up Block (1/2)

VR101 TRACKING BALANCE

VR102 FOCUS BIAS

VR104 FOCUS GAIN

VR103 TRACKING GAIN

VC voltage actually comes from VR pin which has a op amp configured as a follower with VCC/2

Author: Regis Galland	
Sheet: /RF AMP/	
File: opticalblock.kicad_sch	
Title: PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR	
Size: A4	Date: 2024-07-19
KiCad E.D.A. 8.0.6	Id: 2/7
	Rev: 0.2

SERVO SIGNAL PROCESSOR

Notes:
- MDP, MON, MDS, FSW, WDLK, CNIN, SENS, LOCK, VCOO and VCOI connected to DSP
- SENS, MLT, MCK and MDAT conencted to micro
- SPDLO, SLO, FEO, TAO connected to motor drivers
- FOK, MIRROR and DEFECT connected to RF amp

VR105 VCO (PLL)

KSM-220 or KSM-162 Optical Pick-Up Block (2/2)

IC104 BA6290A
IC105 BA6290A
IC102 CXA1082BQ
IC103A RC4558
IC103B RC4558
IC103C RC4558

SPL_MOTOR_RED
SPL_MOTOR_BLACK
To spindle motor
P106 Conn_01x02 Pink Blue
To SLED motor

Tracking and Focus
CN101
Conn_01x04_Socket
FOCUS COIL
TRACKING COIL

P104
Conn_01x06_Pin

Author: Regis Galland
Sheet: /Servo and Actuator Drivers/
File: motors.kicad_sch

Title: PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR

Size: A3	Date: 2024-07-19	**Rev: 0.2**
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CDR-30 (older revision used D9309GF instead but seemed to be the same)

8KB RAM

L101 used to filter 5V to IC107, IC209 and all components around

SCSI ASIC

IC109
D6378GF

IC107
D4364G

JK104A
30P_ELCO_5061

C159
47uF

C153
100nF

L103
L

D106
D_Dual_CommonCathode_AAK

DTA114E
Q106

No writing to RAM when $\overline{MSG}$ = '0'!

Possible open collector outputs:
P21-P35
P54-P57

CF102
Crystal

Q104
2SC2412K

C151
?

C150
?

C152
?

R534
0
No R534 on CDR-30 Rev

JK104D
30P_ELCO_5061

JK104C
30P_ELCO_5061

In the CDR-30 Rev all of the series resistos, R511-R527, are not there.

MRST

IC302
1951A

C155
C

Alternative 9V power input

JK103
Barrel_Jack_Switch

D301
D

IC301
L7805

C301
470uF

C300
470uF

C302
100uF

PWR_FLAG

Author: Regis Galland
Sheet: /SCSI/
File: scsi.kicad_sch

Title: PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR

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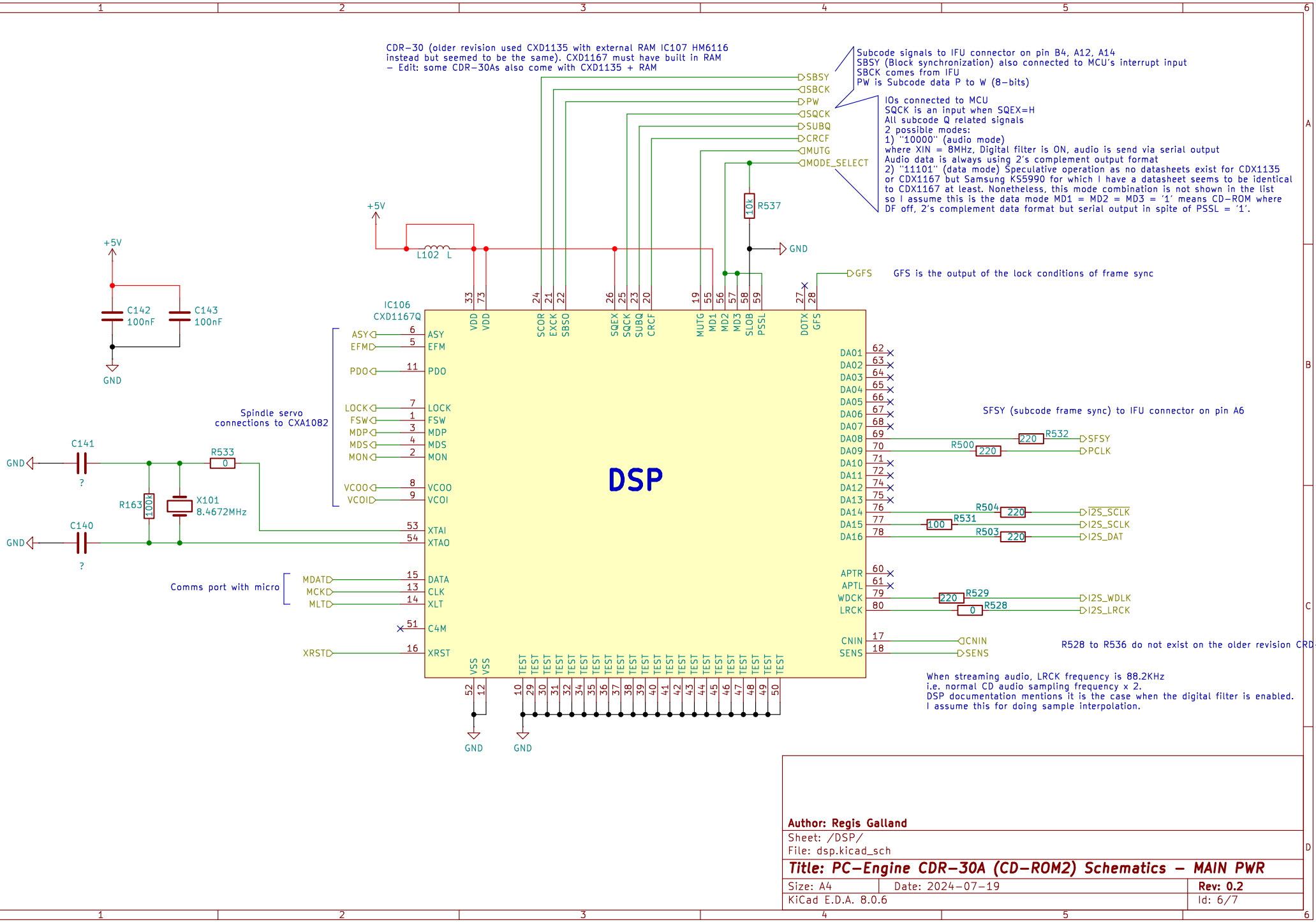
IC201 takes in signed 16 bit data on a 24 bit frame. IF = H means that MSB is sent first.
Effectively, bits 23 down to 16 are a sign extension (i.e. what ever bit 15 is)
since data is coded on 16 bit. Data is right-justified. If IF had been low,
data would have been left-justified instead.

Exact values for C207-210 and aplicable to most SMT capacitors would require for them to be desoldered to be precisely measured.

Dual pot with one common end to GND.
With other components, resistance between 4-6 and 1-3
varies from 140 to 17.5k Ohms

In the CDR-30 Rev, these components are placed the corner of the board instead by the headphone connector

Author: Regis Galland	
Sheet: /AUDIO/	
File: audio.kicad_sch	
Title: PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR	
Size: A3	Date: 2024-07-19
KiCad E.D.A. 8.0.6	Id: 5/7
	Rev: 0.2


CDR-30 (older revision used CXD1135 with external RAM IC107 HM6116
instead but seemed to be the same). CXD1167 must have built in RAM
- Edit: some CDR-30As also come with CXD1135 + RAM
Subcode signals to IFU connector on pin B4, A12, A14
SBSY (Block synchronization) also connected to MCU's interrupt input
SBCK comes from IFU
PW is Subcode data P to W (8-bits)
IOs connected to MCU
SQCK is an input when SQEX=H
All subcode Q related signals
2 possible modes:
1) "10000" (audio mode)
where XIN = 8MHz, Digital filter is ON, audio is send via serial output
Audio data is always using 2's complement output format
2) "11101" (data mode) Speculative operation as no datasheets exist for CDX1135
or CDX1167 but Samsung KS5990 for which I have a datasheet seems to be identical
to CDX1167 at least. Nonetheless, this mode combination is not shown in the list
so I assume this is the data mode MD1 = MD2 = MD3 = '1' means CD-ROM where
DF off, 2's complement data format but serial output in spite of PSSL = '1'.
SBSY
SBCK
PW
SQCK
SUBQ
CRCF
MUTG
MODE_SELECT
R537
10k
GND
+5V
L102 L
GFS
GFS is the output of the lock conditions of frame sync
IC106
CXD1167Q
DSP
VDD
SCOR
EXCK
SBSO
SQEX
SQCK
SUBQ
CRCF
MUTG
MD1
MD2
MD3
SLOB
PSSL
DOUT
GFS
ASY
EFM
PDO
LOCK
FSW
MDP
MDS
MON
VCOO
VCOI
XTAI
XTAO
DATA
CLK
XLT
C4M
XRST
VSS
TEST
DA01
DA02
DA03
DA04
DA05
DA06
DA07
DA08
DA09
DA10
DA11
DA12
DA13
DA14
DA15
DA16
APTR
APTL
WDCK
LRCK
CNIN
SENS
Spindle servo
connections to CXA1082
Comms port with micro
C142
100nF
C143
100nF
C141
?
C140
?
R533
0
R163
100k
X101
8.4672MHz
SFSY (subcode frame sync) to IFU connector on pin A6
R532
220
SFSY
R500
220
PCLK
R504
220
I2S_SCLK
R531
100
I2S_SCLK
R503
220
I2S_DAT
R529
220
I2S_WDLK
R528
0
I2S_LRCK
R528 to R536 do not exist on the older revision CRD-30
When streaming audio, LRCK frequency is 88.2KHz
i.e. normal CD audio sampling frequency x 2.
DSP documentation mentions it is the case when the digital filter is enabled.
I assume this for doing sample interpolation.
Author: Regis Galland
Sheet: /DSP/
File: dsp.kicad_sch
Title: PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR
Size: A4
Date: 2024-07-19
Rev: 0.2
KiCad E.D.A. 8.0.6
Id: 6/7

Only $\overline{SCSI\_SEL}$ is connected to this cjip so other IOs must be used to inform whether we are in a command or data stage. Equally, the micro needs to know when req is asserted to read data and then ack. This might be done with PC3 as it can be configured as an interrupt.
Perhaps the 8KRAM also stores the command bytes.

ALE latches address to PD0–7 when high and presents data when low. PD0–7 and PF0–5 are connected to SCSI chip but PF5 is also connected to the display update signal though a diode. Since writing to display requires both $\overline{WR}$ and PF5 to be low because of the logical 'OR' with diodes, it might then mean that addresses from 0000h to 1FFFh are ignored by the SCSI IC (i.e. PF5 is a chip select pin) but adresses from 2000h to 3FFFh will be seen as read or write operations to the 8KB RAM (0000h–1FFFh)

P101 Data bus is used to send 7 SEG Display data

P102 connector carries mainly signals coming button signal fron the front PCB

DIGIT1_EN, DIGIT2_EN are PWM signals that can't be activated at the same time as they each drive a digit but these digits share the same data bus.
DIGIT1_EN also allows to read the state of all buttons except RS as this one is active when RS_EN is on.
However, it seems possible for RS_EN and DIGIT2_EN to be on at the same time.
Buttons connected to analogue inputs and PWM signals used to trickle charge the internal capacitors (my assumption).

Lid switch. Contact is closed when lid is down
Named P106 on some CDR-30 Rev

To update the display, both PF5 and WR must be low.
When PF5 is high, it acts as a chip select signal to access SCSI chip SRAM.
The MCU external address map would be:
0000h–1FFFh: Display address range where PF0–PF4 can be any value
2000h–3FFFh: SCSI chip SRAM access (8K)

Author: Regis Galland
Sheet: /MCU/
File: mcu.kicad_sch

Title: PC–Engine CDR–30A (CD–ROM2) Schematics – MAIN PWR

Size: A4	Date: 2024-07-19	**Rev: 0.2**
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