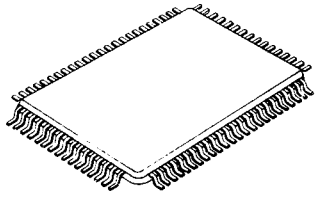
DIGITAL SIGNAL PROCESSOR

The KS5990 is a CMOS integrated circuit designed for compact disc player applications. It consists of 16KSRAM, digital filter, and digital signal processing circuits.

80 Q FP



FEATURES

- All digital signals for regeneration are processed using one chip.
- Internal aperture compensation digital filter
- EFM-PLL circuit for bit clock regeneration
- EFM data demodulation
- Frame synchronous signal detection, protection
- Compensation using mean value and prior value retention
- Subcode signal demodulation subcode Q detection
- CLV servo for spindle motor
- 8-bit tracking counter
- CPU interface with serial bus
- Subcode Q register
- Built-in 17th digital filter
- Built-in 16KSRAM
- 80 Quad flat package type

ORDERING INFORMATION

Device	Package	Operating Temperature
KS5990	80 QFP	−20°C ~ +75°C

BLOCK DIAGRAM

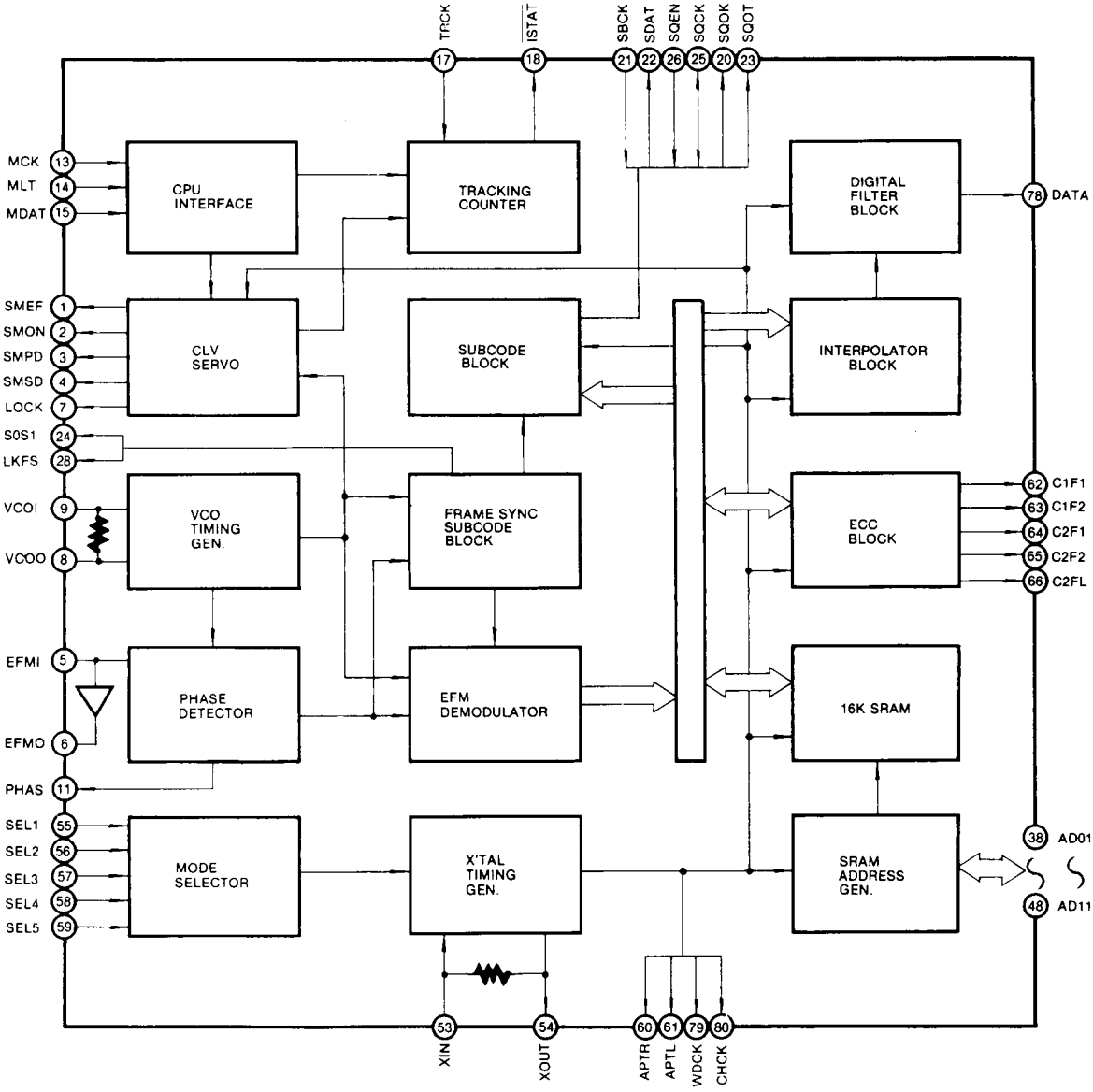


Fig. 1

PIN CONFIGURATION

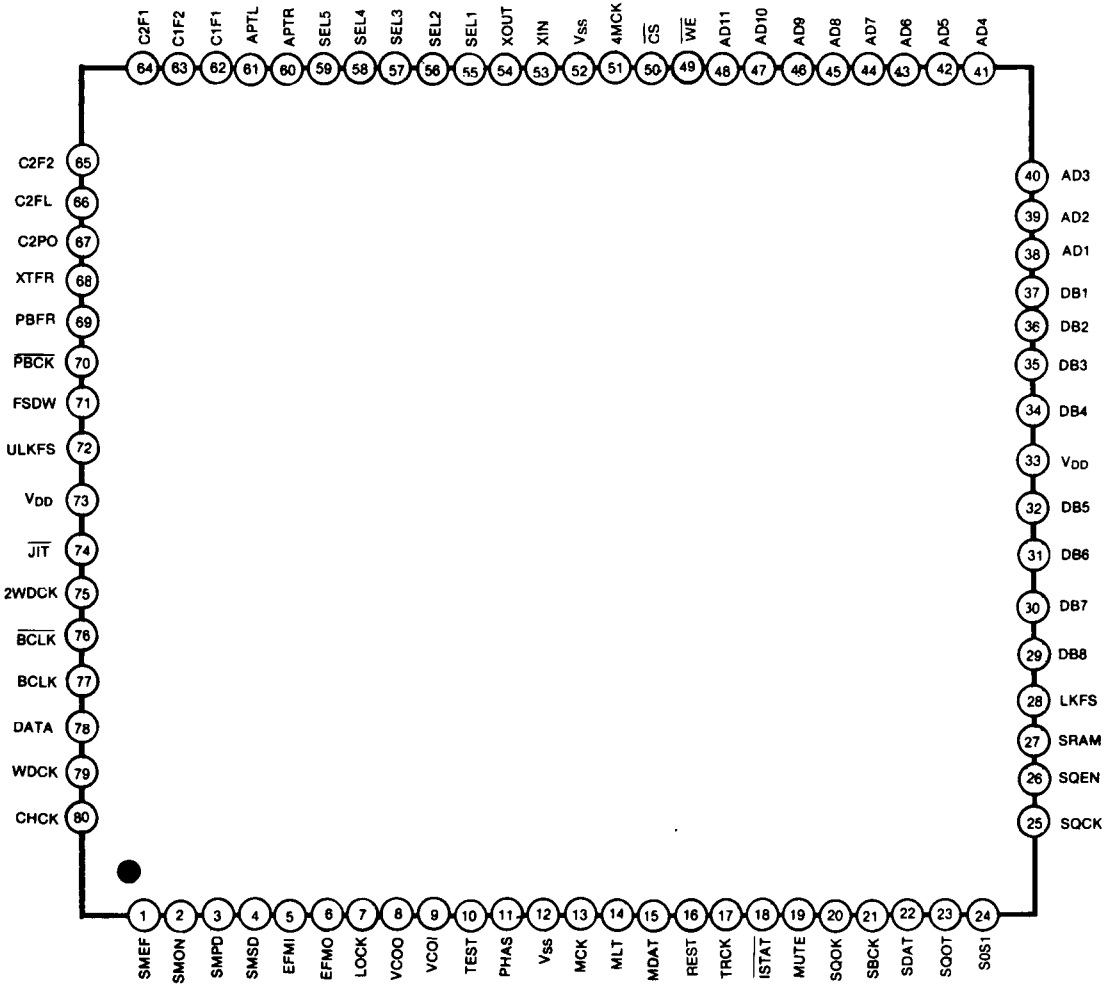


Fig. 2

PIN DESCRIPTION

Pin No	Symbol	I/O	Description
1	SMEF	O	Pin 1 output is switched constant when output filter of the spindle motor is energized.
2	SMON	O	ON/OFF control for spindle motor.
3	SMPD	O	Spindle motor drive. Provides rough control during CLV-S mode and phase control during CLV-P mode.
4	SMSD	O	Spindle motor drive. Controls speed during CLV-P mode.
5	EFMZ	I	EFM signal from RF amplifier.
6	EFMO	O	Controls slice level of the EFM signal.
7	LOCK	O	The output of pin 7 reflects the status of the GFS signal which is sampled at PBFR/16. When the GFS signals is "H", but, when the signal has remained "L" for at least 8 samples, the output of pin 7 is "L".
8	VCOO	O	VCO output. The frequency is f = 8.6436MHz, when locked by the DBFR signal.
9	VCOI	I	VCO input.
10	TEST	I	(0V).
11	PHAS	O	The output of Pin 11 provides phase comparison of EFM signal and VCO/2.
12	V_{SS}	—	GND (0V).
13	MCK	I	Pin 13 provides serial transmission clock from the CPU. Data is latched on the leading edge of the clock.
14	MLT	I	Pin 14 provides latch input from the CPU. 8-bit shift register data (serial data received from the CPU) is latched in each of the registers.
15	MDAT	I	Serial data from the CPU.
16	REST	I	System reset ("L").
17	TRCK	I	Tracking pulse input.
18	ISTAT	O	Output reflecting internal condition as designated by address.
19	MUTE	I	Muting input. MUTE is "L" when ATTM of internal register A is "L" (normal condition). MUTE is "H" when meting condition is set.
20	SQOK	O	Output the results CRC check of subcode Q.
21	SBCK	I	Clock input for subcode serial output.
22	SDAT	O	Serial output of subcode.
23	SQDT	O	Output of subcode Q.
24	S0S1	O	Output of subcode sync S0 + S1.
25	SQCK	I/O	Clock for reading subcode Q.
26	SQEN	I	Input for selecting SQCK (L; SQCK is output, H; SQCK is input)
27	SRAM	I	SRAM is "H" in Nomal, SRAM is "L" when system is testing.
28	LKFS	O	Display output for frame sync lock status.

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
29	DB8	I/O	Data pin for external RAM. DATA8 (MSB) in test mode. Hi-Z in normal
30	DB7	I/O	Data pin for external RAM. DATA7 in test mode. Hi-Z in normal
31	DB6	I/O	Data pin for external RAM. DATA6 in test mode. Hi-Z in normal
32	DB5	I/O	Data pin for external RAM. DATA5 in test mode. Hi-Z in normal
33	V_{DD}	—	Power supply (+5V).
34	DB4	I/O	Data pin for external RAM. DATA4 in test mode. Hi-Z in normal
35	DB3	I/O	Data pin for external RAM. DATA3 in test mode. Hi-Z in normal
36	DB2	I/O	Data pin for external RAM. DATA2 in test mode. Hi-Z in normal
37	DB1	I/O	Data pin for external RAM. DATA1 (LSB) in test mode. Hi-Z in normal
38	AD01	O	(LSB)
39	AD02	O	In normal mode (TEST = 'L', SRAM = 'H'), these pins are High impedance (Hi-Z) In test mode (TEST = 'H', SRAM = 'L'), these pins are Output address of external RAM
40	AD03	O	
41	AD04	O	
42	AD05	O	
43	AD06	O	
44	AD07	O	
45	AD08	O	
46	AD09	O	
47	AD10	O	
48	AD11	O	(MSB)
49	$\overline{WE}$	I/O	In normal mode, this is WE output. In test mode, write enable input.
50	$\overline{CE}$	I/O	In normal mode, this is CE output. In test mode, chip enable input.
51	4MCK	O	Divider output for crystal. f = 4.2336MHz
52	V_{SS}	—	GND (0V)
53	XIN	I	Input to crystal oscillator circuit. Depending on the mode, the frequency is either f = 8.4672 r 16.9344MHz.
54	XOUT	O	Output from crystal oscillator circuit. Depending on the mode, the frequency is either f = 8.4672 or 16.9344MHz.
55	SEL1	I	Mode selection input 1.
56	SEL2	I	Mode selection input 2.
57	SEL3	I	Mode selection input 3.
58	SEL4	I	Mode selection input 4. Code switch input for audio data output. 2's complement output when "L", and offset binary output when "H"
59	SEL5	I	Mode selection input 5. Code switch input for audio data output. Serial output when "L", parallel output when "H".

PIN DESCRIPTION (Continued)

Pin No	Symbol	I/O	Description
60	APTR	O	Output for aperture compensation. "H" when R-ch.
61	APTL	O	Output for aperture compensation. "H" when L-ch.
62	C1F1	O	Monitor output reporting status of error correction for C1 decoder. When SEL5 = 'L', DA01 (LSB of parallel audio data) is output when SEL5 = 'H'.
63	C1F2	O	Monitor output reporting status of error correction for C1 decoder when SEL5 = 'L', DA02 is output when SEL5 = 'H'.
64	C2F1	O	Monitor output reporting status of error correction for C2 decoder when SEL5 = 'L', DA03 is output when SEL5 = 'H'.
65	C2F2	O	Monitor output reporting status of error correction for C2 decoder when SEL5 = 'L', DA04 is output when SEL5 = 'H'.
66	C2FL	O	Output of status condition when SEL5 = 'L'. C2FL is set 'H' when the C2 sequence, being corrected becomes impossible to correct. DA05 is output when SEL5 = 'H'.
67	C2PO	O	Display output of the C2 pointer when SEL5 = 'L'. DA06 is output when SEL5 = 'H'.
68	XTFR	O	When SEL5 = 'L', output of read frame dock, which is 7.35KHz of the crystal system. DA07 is output when SEL5 = 'H'.
69	PBFR	O	When SEL5 = 'I', output of write frame clock, which is 7.35KHz when locked by the crystal system. DA08 is output when SEL5 = 'H'.
70	$\overline{\text{PBCK}}$	O	When SEL5 = 'L', output of VCO/2 (f = 4.3218MHz when locked by the EFM signal). DA09 is output when SEL5 = 'H'.
71	FSDW	O	When SEL5 = 'L', output for unprotected frame sync patterns. DA10 is output when SEL5 = 'H'.
72	ULKFS	O	Output for display of status of frame sync protection when SEL5 = 'L', DA11 is ouput when SEL5 = 'H'.
73	V_{DD}	—	Power supply (+5V).
74	$\overline{\text{JIT}}$	O	When SEL5 = 'L'. output for display of either RAM overflow or underflow for +4 frame jitter absorption. DA12 is output when SEL5 = 'H'.
75	ZWDCK	O	When SEL5 = 'L', output for strobe signal (352.8KHz when DF is ON, 176.4KHz when DF is OFF). DA13 is output when SEL5 = 'H'.
76	$\overline{\text{BLCK}}$	O	When SEL5 = 'L', inverse output of BLCK. DA14 is output when SEL5 = 'H'.
77	BLCK	O	When SEL5 = 'L', bit clock output (4.2336MHz when DF is ON, 2.1168MHz when DF is OFF) DA15 is output when SEL5 = 'H'.
78	DATA	O	Serial data output of audio signal when SEL5 = 'L'. DA16 is output when SEL5 = 'H'.
79	WDCK	O	Strobe signal output. Output is 176.4KHz when DF is on. Output is 88.2KHz when DF is off.
80	CHCK	O	Strobe signal output. Output is 88.2KHz when DF is on. Output is 44.1KHz when DF is off.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ +7	V
Input Voltage	V_I	−0.3 ~ +7	V
Output Voltage	V_O	−0.3 ~ +7	V
Operating Temperature	T_{OPR}	−20 ~ +75	°C
Storage Temperature	T_{STG}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH1}	Note 1	0.7 V_{DD}		V_{DD}	V
Input Low Voltage	V_{IL1}	Note 1			0.3 V_{DD}	V
Input High Voltage	V_{IH2}	Note 2	0.8 V_{DD}			V
Input Low Voltage	V_{IL2}	Note 2			0.2 V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = −1mA	V_{DD} − 0.5		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 1mA	0		0.4	V
Input Leakage Current	I_{LKG}	V_{IN} = 0 ~ 5.5V	−5		+5	μA
Three-State Pin Output Leakage Current	I_{LKG}	V_{OUT} = 0 ~ 5.5V	−5		+5	μA
SRAM Input Leakage Current	I_{LKG}	V_{IN} = 0 ~ 5.5V	−5		+200	μA

Note 1. Related pins—EFMI, RESET, TEST, MUTE, SEL 2 ~ 5, MLT, MDAT, SQEN, SQCK.
Note 2. Related pins—TRCK, MCK, SRAM.

2. AC Characteristics

A. XIN Pin, VCOI Pin

(1) When pulse applied to XIN and VCO, V_{DD} = 5V ± 10%, V_{SS} = 0V, and Ta = 25°C, unless otherwise specified.

Characteristic	Symbol	Min	Typ	Max	Unit
"H" Level Pulse Width	t_{WHX}	20			ns
"L" Level Pulse Width	t_{WLX}	20			ns
Pulse Frequency	t_{CK}	55			ns
Input "H" Level	V_{IH}	V_{DD} − 1.0			V
Input "L" Level	V_{IL}			0.8	V
Rising Time Breaking Time	t_R			15	ns

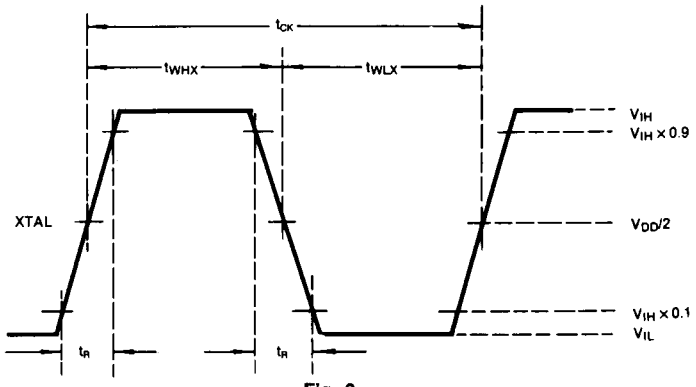


Fig. 3

B. Pins MCK, DATA, MLT, TRCK, SQCK

($V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $T_{OPR} = -20 \sim +75°C$)

Characteristic	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{CK}			1	MHz
Clock Pulse Width	t_{WCK}	300			ns
Setup Time	t_{SU}	300			ns
Hold Time	t_H	300			ns
Delay Time	t_D	300			ns
Latch Pulse Width	t_W	300			ns
CNIN SQCK Frequency	f_{CK2}			1	MHz
CNIN SQCK Pulse Width	t_{WCK2}	300			ns

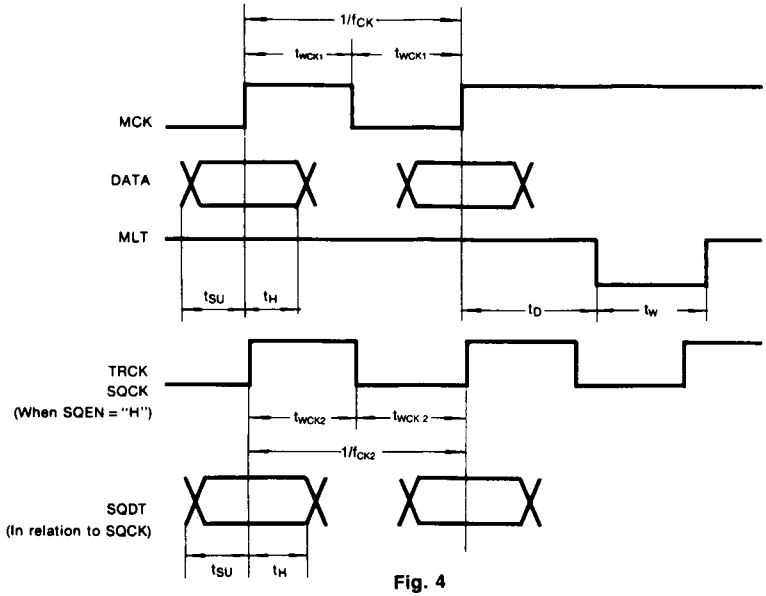


Fig. 4

C. DAC Interface ($V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_{OPR} = -20 \sim +75°C$, $C_L = 50pF$)

Item	Symbol	DF is OFF			When DF ON			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock Pulse Width	t_{WCK}		236			118		ns
Clock Skew (Fast)	t_{FCK}			40			40	ns
Data Skew (Fast)	$t_{F\,(SK)}$			0			0	ns
Data Skew (Delay)	$t_{D\,(SK)}$			80			80	ns

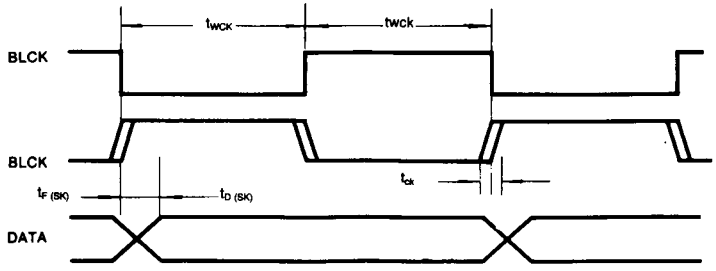


Fig. 5

*Note: CHCK, WDCK, APTR, APTL
DA01 through DA16 during parallel DA conversion or C1F1, C1F2, C2F1, C2F2, C2FL, C2PO, XTFR, 2WDCK, DATA during serial conversion.

APPLICATION INFORMATION
FUNCTION DESCRIPTION

MODE SELECTOR

To control several blocks in KS5991, there are 5 selecting pin signals. Table 1. shows selected mode by these signals.

Input Pins					Function*				
SEL1	SEL2	SEL3	SEL4	SEL5	XIN	DF	P/S	OB/2'S	CD ROM/Audio
0	1	0	0	0	16M	ON	S	2'S	Audio
0	1	0	1	1	16M	ON	P	OB	Audio
0	1	1	0	0	16M	OFF	S	2'S	Audio
0	1	1	1	1	16M	OFF	P	OB	Audio
1	0	0	0	0	8M	ON	S	2'S	Audio
1	0	0	1	1	8M	ON	P	OB	Audio
1	0	1	0	0	8M	OFF	S	2'S	Audio
1	0	1	1	1	8M	OFF	P	OB	Audio
1	1	1	1	0	8M	OFF	S	2'S	CD ROM

Table 1. Mode Selection

* Note: • 8M/16M: Selection of either the XIN or XOUT clocks will provide either a 8.4672MHz or 16.9344MHz signals.
  • DF: Digital Filter
  • P/S: Parallel mode/serial mode
  • OB/2'S: Offset

- Clock selection
  Selectioin of an 16.9344MHz or 8.4672MHz oscillator clock is possible at pins XIN and XOUT. However only 16.9344MHz clocks are provided for digital out usage.

- Digital filter selection
  When the digital filter function is switched to ON, all signals on the DAC interface are handled at twice the normal speed.

- Parallel/Serial output selection
  When the output is parallel, 16-bit parallel data is output from pins DA01 through DA16.
  When the output is serial, the following signals are output at pin DA01 through DA16.

DATA (DA16)	Serial data output (MSB or LSB first output)
BLCK (DA15)	Internal system clock (with DF ON 4.2336MHz and with DF OFF 2.1168MHz)
$\overline{\text{BLCK}}$ (DA14)	Bit clock (BLCK inversion signal)
2WDCK (DA13)	4X multiplied CHLK signal
$\overline{\text{JIT}}$ (DA12)	Jitter Margin Overflow/Underflow signal
ULKFS (DA11)	Display output of frame sync protection status
FSDW (DA10)	Unguarded (unprotected) frame sync signal
PBCK (DA09)	Signal at 1/2 V_{CO} pin cycle times. When locked 4.3218MHz
PBFR (DA08)	Write Frame Clock signal. When locked 7.35KHz.
XTFR (DA07)	Read Frame Clock signal. Crystal system 7.35KHz.
C2PO (DA06)	C2 Pointer signal
C2FL (DA05)	Correction mode output, C2FL = C2F1, C2F2
C2F2 (DA04) C2F1 (DA03)	Monitor Output of Error Correction Mode for C2 Decode
C1F2 (DA02) C1F1 (DA01)	Monitor Output of Error Correction Mode for C1 Decode

- OFFSET Binary/2's Complement Selection
  When pin SEL4 is at "H" output occurs at OFFSET BINARY; when it is at "L" output occurs at 2's complement.
- CD-ROM/AUDIO Selection
  When SEL1 = SEL2 = SEL3 = "H",CD-ROM is selected. Then the C2 pointer is output with each byte (8 bits) and neither the mean value interpolation nor the preceding value hold are exercised. That is, if an error occurs in the upper 8 bits of a 16-bit data, only the C2 pointer related to those upper 8 bits switches to "H" while the lower 8 bits are handled as correct data.

Microcomputer Interface

Data from the microcomputer are inputed through MDAT pins by MCK which is the clock signal of the microcomputer and the pulse signal through MLT pin is for inputed data load one of 6 kinds of control registers.

Fig. 6 Shows the timing diagram of data input from microcomputer.

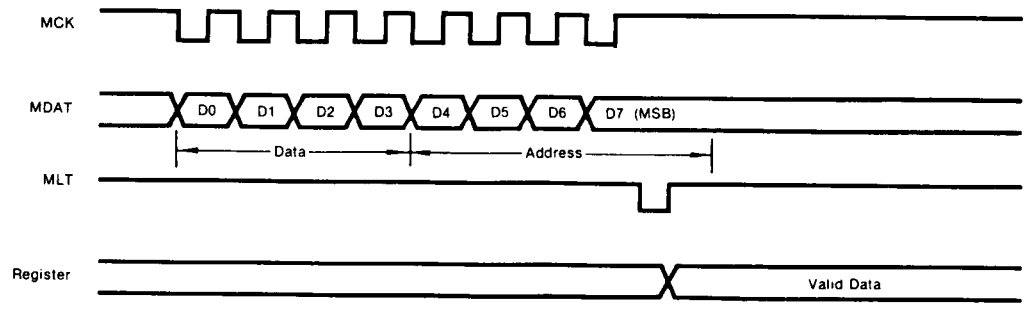


Fig. 6 Data Input Timing Diagram

According to the address of MDAT, control register is selected as below table 2.

Control Register	Comment	Address D7 ~ D4	Data				$\overline{\text{ISTAT}}$ Pin
			D3	D2	D1	D0	
CNTL-Z	Data Control	1 0 0 1	ZCMT	HIPD	NCLV	CRCD	Hi-Z
CNTL-S	Frame Sync Protection Attenuation Control	1 0 1 0	FSEM	FSEL	WSEL	ATTM	Hi-Z
CNTL-L	Tracking Counter Lower 4 Bit	1 0 1 1	TRC3	TRC2	TRC1	TRC0	$\overline{\text{Complete}}$
CNTL-U	Tracking Counter Upper 4 Bit	1 1 0 0	TRC7	TRC6	TRC5	TRC4	$\overline{\text{COUNT}}$
CNTL-W	CLV Control	1 1 0 1	COM	WB	WP	GAIN	Hi-Z
CNTL-C	CLV Mode	1 1 1 0	CLV Mode				$\overline{\text{PW}\geq 64}$

Table 2. Data of Selected Control Register

According to D0 through D1 DAA,
The function of each control register is described below.

1) CNTL-Z Register

This is a control register for the zero cross mute of audio data, PHAS, the control signal of phase servo and CRCF data.

		Data = 0	Data = 1
ZCMT	D3	Zero cross mute "OFF"	Zero cross mute "ON"
HIPD	D2	Phase normally active	Phase convert "L" to "Hi-Z" by LKFS
NCLV	D1	Phase servo driven by frame sync	Phase servo is controlled by base counter
CRCQ	D0	SQDT output without SQOK	SQDT = CRCF during the rising time of S0S1

2) CNTL-S Control Register

This is a control register for the frame sync. Protection and attenuation.

FSEM	FSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTE	dB
0	0	0
0	1	–
1	0	– 12
1	1	– 12

3) CNTL-L, U Control Register

When the numbers of tract to be counted are inputed from a microcomputer, data load these registers.
(See tracking counter)

4) CNTL-W Control Register

This is a control register for CLV-Servo.

		Data = 0	Data = 1	Comments
COM	D3	XTFR/4 & PBFR/4	XTFR/4 & PBFR/4	Phase comparative frequency during PHASE-mode
WB	D2	XTFR/32	XTFR/16	Bottom hold period during SPEED and HSPEED-mode
WP	D1	XTFR/4	XTFR/2	Peak hold period during SPEED-mode
GAIN	D0	– 12dB	0dB	SMPD gain during SPEED & HSPEED-mode

5) CNTL-C Control Register

This is a control register for CLV-Servo.

Mode	D7 ~ D4	D3 ~ D0	SMDP	SMSD	SMEF	SMON
Forward	1 1 1 0	1 0 0 0	H	Hi-Z	L	H
Reverse		1 0 1 0	L	Hi-Z	L	H
SPEED		1 1 1 0	SPEED mode	Hi-Z	L	H
HSPEED		1 1 0 0	HSPEED mode	Hi-Z	L	H
PHASE		1 1 1 1	PHASE mode	PHASE mode	Hi-Z	H
XPHSP		0 1 1 0	SPEED, PHASE mode	Hi-Z or PHASE mode	L or Hi-Z	H
VPHSP		0 1 0 1	SPEED PHASE mode	Hi-Z or PHASE mode	L or Hi-Z	H
STOP		0 0 0 0	L	Hi-Z	L	L

TRACKING COUNTER

This counter is used to improve track-jumping characteristics. The number of tracks that are to be jumped are loaded into either register CNTL-L or CNTL-U. After either register CNTL-L or CNTL-U have been loaded and at the rising edge of the next MLT, TRCK pulse count begins. If register CNTL-L = register = CNTL-U = 0, then n = 256n is loaded into the register, and when the address is set in CNTL-L, the signal ($\overline{\text{COMPLETE}}$) is output from pin SENS at high level until the "n"th pulse and then at low level for succeeding pulses. When the address is set in CNTL-U, the signal ($\overline{\text{COUNT}}$) TRCK/2n is output. Fig. 7 shows the timing of the tracking counter.

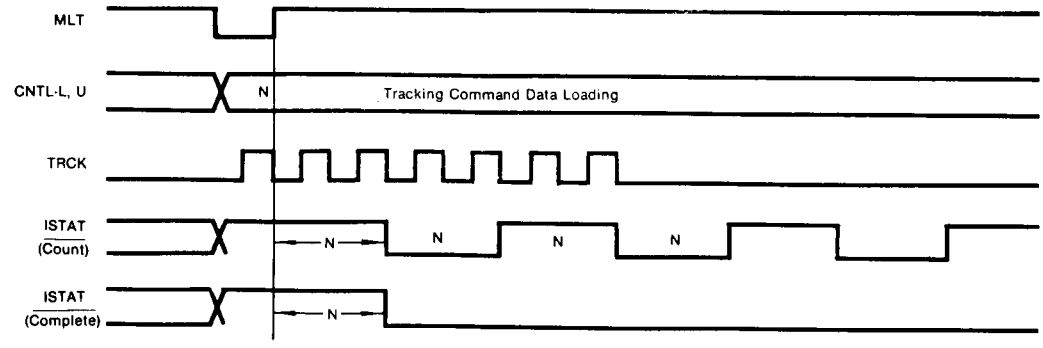


Fig. 7 Tracking Count Timing Chart

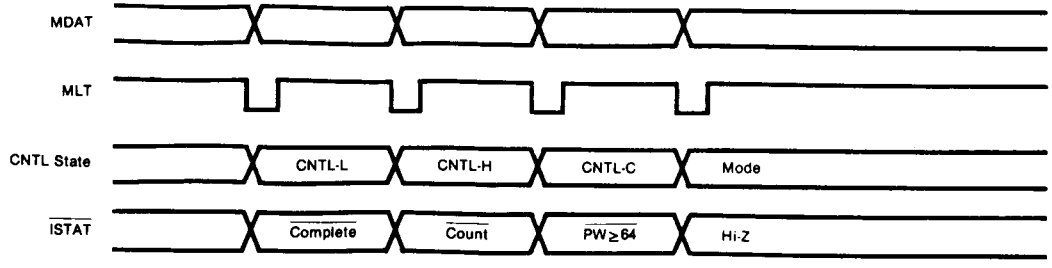
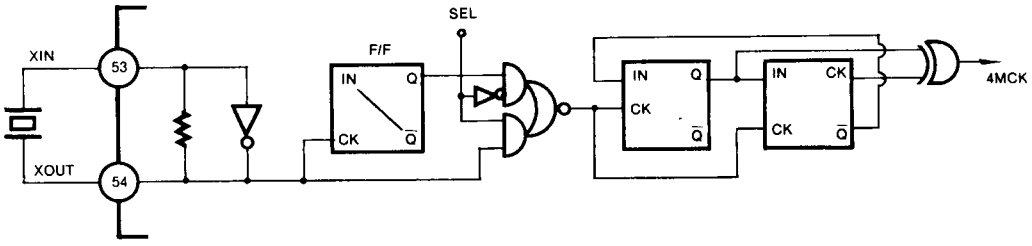


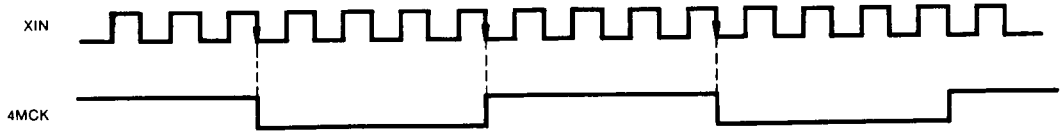
Fig. 8 $\overline{\text{ISTAT}}$ Output Signal by CNTL Register

X'TAL OSCILLATION

1) Block Diagram



2) Timing Chart (SEL = 0) in Use f = 16.9344MHz X'tal OSC.



3) Timing Chart (SEL = 1) in use f = 8.4672MHz X'tal OSC.

Fig. 9

DIGITAL FILTER

KS5990 is built-in 17th FIR Digital Filter.
The digital filter consists of RAM, multiplier, serial to parallel and parallel to serial converter and controller.

1) Block Diagram

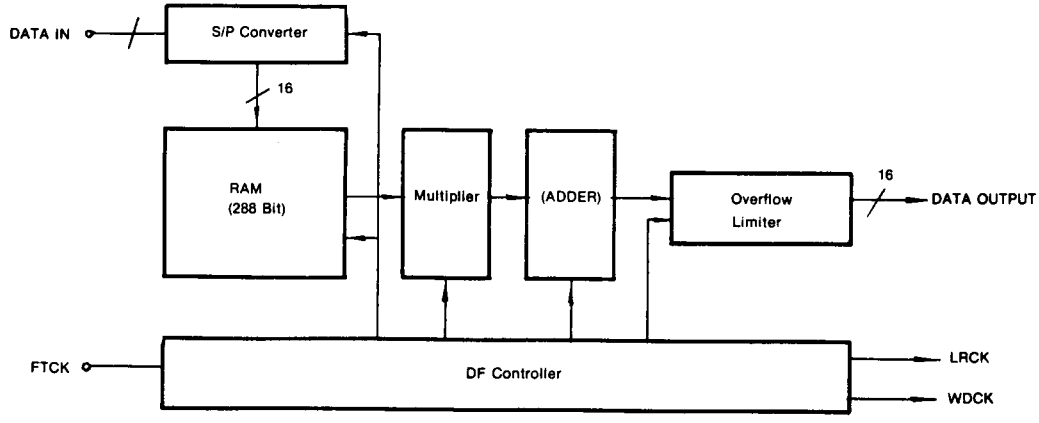


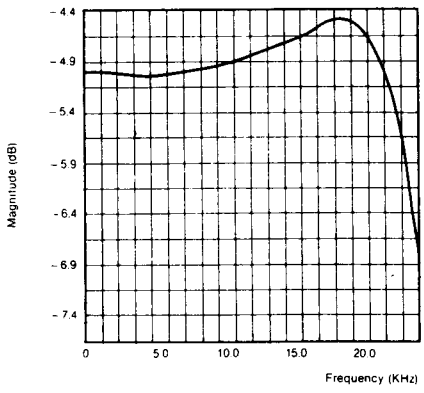
Fig. 10

2) Specification

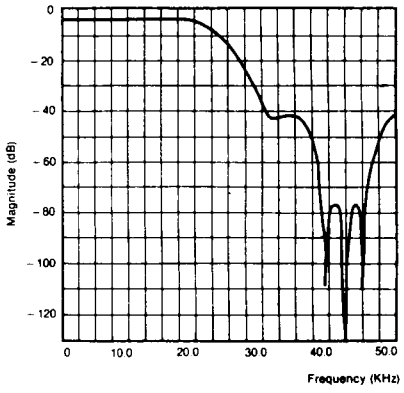
	DC through 18KHz ripple 20KHz of attenuation against 1KHz	±0.07dB max 0.65dB max
	44.1 ± 1KHz attenuation against 1KHz 44.1 ± 5KHz attenuation against 1KHz 44.1 ± 10KHz attenuation against 1KHz 44.1 ± 20KHz attenuation against 1KHz −30dB frequency range against 1KHz −60dB frequency range against 1KHz	87dB min 58dB min 44dB min 10dB min 44.1 ± 14KHz 44.1 ± 4KHz

3) Frequency Characteristic

A. Ripple Characteristic Graph



B. Low Pass Filter Frequency Characteristic Graph



4

EFM BLOCK

The EFM Block is made up of an EFM Demodulator which demodulates the EFM data inputted from a recorded disc, EFM Phase Detector, Frame Sync Detector/Protector/Inserter, Subcode Sync Detector, and Controller for the EFM Block.

1) EFM Phase Detector

As the EFM signal inputted from the disc contains a 2.16 MHz component, a 4.32 MHz bit clock is generated to detec the phase of the signal. The PBCK outputs the result to the PHAS terminal after detecting the phase on the edge of the EFM signal. The relationship between the EFM signal and the PBCK is explained in the following Timing Chart.

A. In normal operation

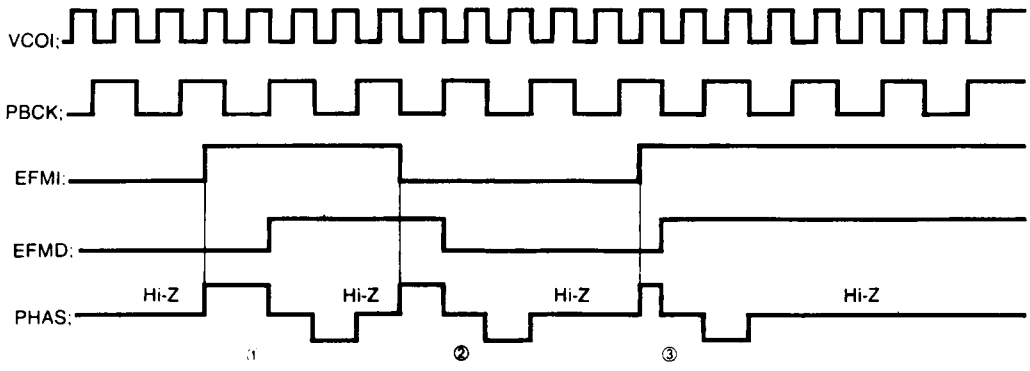


Fig. 11 EFM Phase Detection Timing Chart

Case ①: When the EFM signal is slower than the VCO
Case ②: When the EFM signal is locked up the VCO
Case ③: When the EFM signal is faster than the VCO

B. In abnormal operation

When the HIPD of CNTL-Z is chosen as 'L' from M-COM, the detector of the EFM phase operates as in Fig. 11 When the HIPD is 'H' and the time 'L' of LKFS is below 3.5T, against a PBFS period T, it outpputs Hi-Z to the PHAS terminal as long as "L". When it is above 3.5T, it outputs Hi-Z as long as 3.5T.

2) EFM (Eight to Fourteen) Demodulator

The modulated 14 bit Data is inputted from a disc, then it is inputted into a NRZ-I circuit. As the EFM Data passes by the NRZ-I circuit which converts 14 bit data into 8 bit data, it gets demodulated as 8 bit data. There are two kinds of demodulated data: subcode and PCM data. The subcode data is inputted into the subcode Block, and the PCM Data is written into 16KSRAM by, with both CE and WE signals.

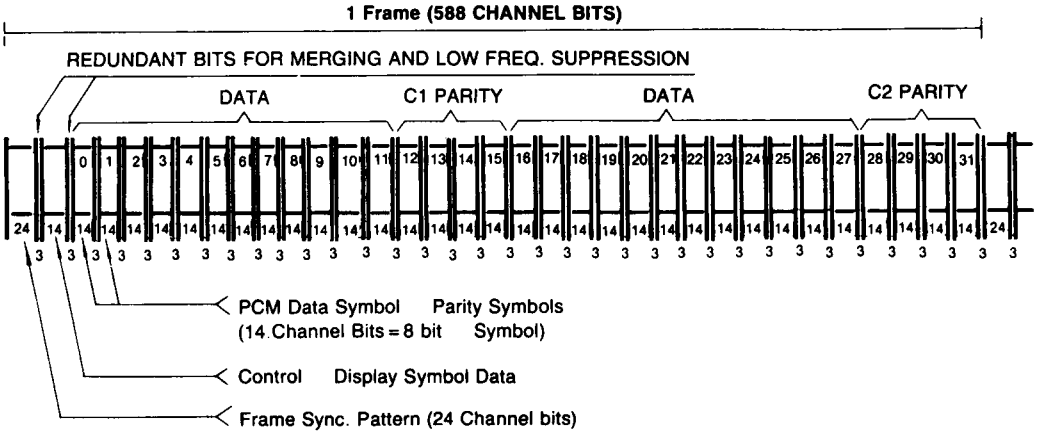
3) Frame Sync Detector/Inserter/Protector

A. Frame Sync Detector

CDP data are composed of units of a frame. A frame is made up of Frame Sync, Subcode Data, PCM Data, and Redundancy Data. A Frame sync is detected per frame against this format.

B. Frame Sync Protector/Inserter

There are cases in which the Frame Sync is left out or detected from the data beside the frame sync because of the effects of an error on the disk or Jitter. In this case the frame sync needs to be protected and inserted. To protect the frame sync, a window is made by the use of a WSEL signal of CNTL-S Reg. The frame sync which comes into the window is true data, and the frame sync deviating from the window is disregarded.



(Frame Format)

The width of the window is determined by the WSEL signal from the CNTL-S Reg. (cf. CNTL-S) being inserted in the frame When the frame sync reaches the number of a frame designated by the FSEM and FSEL, using the CNTL-S Reg, ULKFS becomes 'L' and the frame sync protection window is disregarded. In this case, an outputted frame sync is unconditionally accepted. After the frame sync is received, the ULKFS signal becomes 'H' and accepts a frame sync detected inside the window.

LKFS	ULKFS	Explanation
I	I	When a play back frame sync coincides with a generated frame sync.
O	I	① When a PBFR sync is detected in the window chosen by WSEL even if a play back frame sync does not coincide with a generated frame sync ② In the case of sync insertion, when PBFR sync does not coincide with a XTER sync and a frame sync within the window chosen by WSEL is not detected.
O	O	①After inserting a sync as many as times the number of frames decided by the FSEM and FSEL by the CNTL-S Reg., because Frame Sync is not detected within a window. ② When PBFR sync is not continuously detected after situation ① happens.

SUBCODE BLOCK

The 14 bit subcode sync signal S0, S1 is outputted to the Subcode Sync Block. In a frame delay after the output of S0, S1 is outputted. In this case, the signal of S0 + S1 is outputted through the S0S1 terminal, and the signal of S0·S1 is outputted through the SDAT terminal, when the signal S0S1 becomes 'H'. After the 14 bit Subcode Data inputted to the EFMI terminal has the EFM demodulated, an 8-bit P, Q, R, S, T, U, V, W subcode datum is outputted to SDAT by SBCK clock after it syncronizes with the signal PBFR. Only Q data are chosen among the 8 subcode data, and it is loaded on to 80 shift registers. The CRC-checked results of the loaded data is synchronized with the S0S1 rising edge, and is outputted to the SQCK terminal.
If the result of CRC checking is an error, 'L' is outputted to the SQCK terminal. If it is true, 'H' is outputted to the SQOK terminal. If the CRCD of CNTL-Z mode is 'H', the result of CRC checking is outputted to the SQDT terminal from the S0S1 section 'H' to the period of the SQCK falling edge.
The timing chart of a subcode block is as follows:

1) In SQEN = 'L': SDAT, SQDT, S0S1, SQOK, VCOI Timing Relation

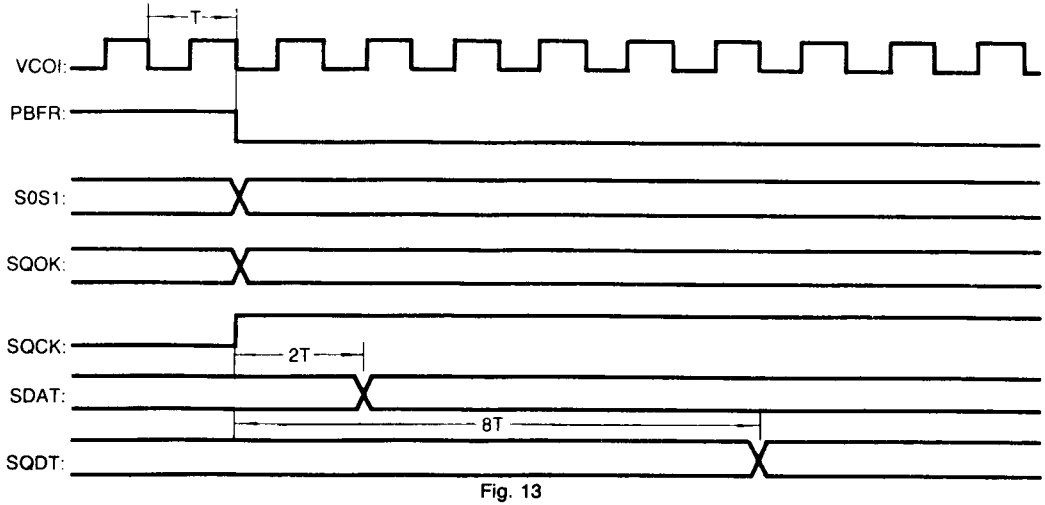


Fig. 13

2) In SQEN = 'L': SQOK, SQDT, S0S1, Timing Chart

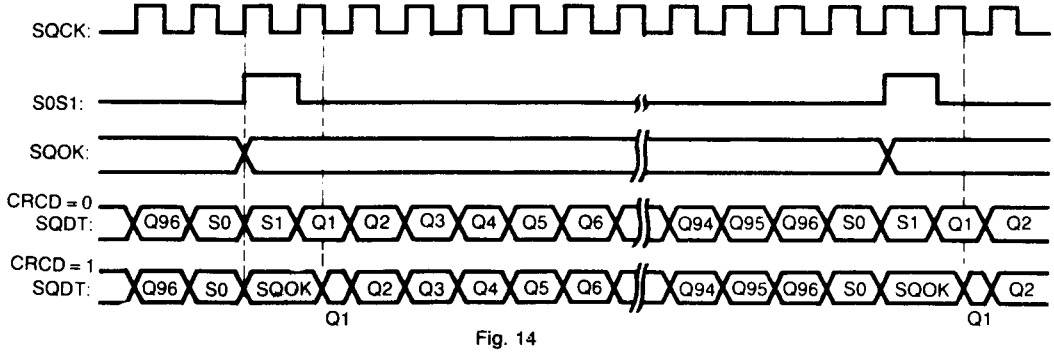
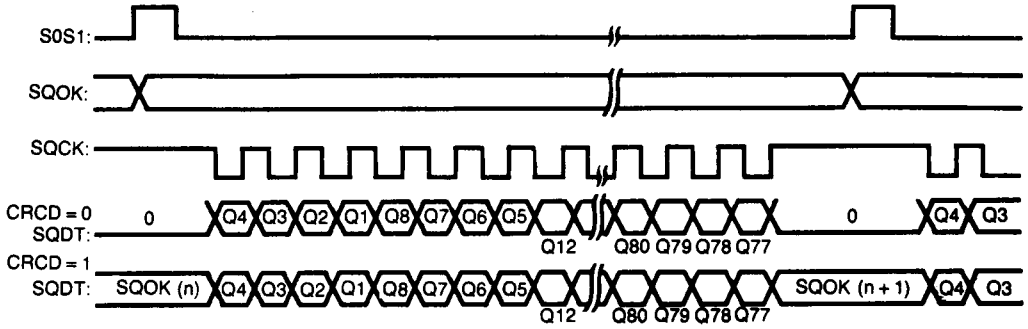


Fig. 14

3) In SQEN = 'H': SQOK, SQDT, S0S1, SQCK Timing Chart



Comment: When a SQOK of subcode Q Data is 'H', subcode data is outputted to SQDT according to SQCK. When SQOK is 'L', 'L' is outputted to the SQDT terminal.

Fig. 15

4) VCO1, SDAT, SBCK Timing Chart

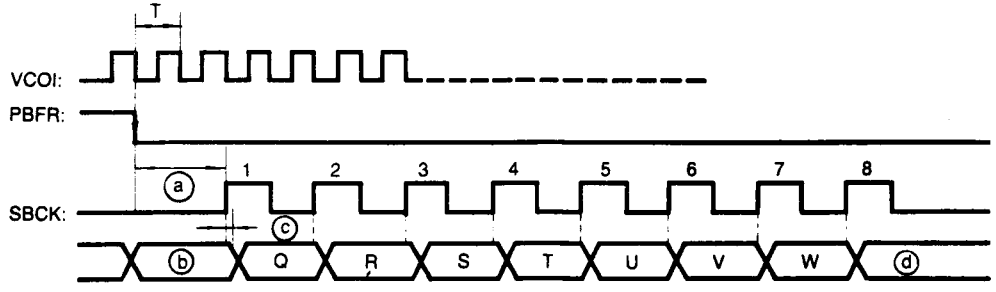


Fig. 16

ⓐ : SBCK is set to "L" for about 10μS after PBFR becomes a falling edge.

ⓑ : When S0S1 is 'L', a subcode P is outputted. When S0S1 is 'H', S0S1 is outputted.

ⓒ : When a cycle of VCO1 is 'T', the width of ⓒ is 4T ~ 6T.

ⓓ : When the pulse inputted to the SBCK terminal is above 7, subcode data P, Q, R, S, T, U, V, W data are repeated.

ECC (Error-Correction Code) Block

The function of ECC Block is to recover damaged data to some extent when data on a disk is damaged. By using CIRC (Crossed-Interleave Reed-Solomon Code), C1 (32, 28) and C2 (28, 24) errors are corrected. ECC is performed with an 8-bit as a symbol unit. In correcting C1, a C1 Pointer is generated, and in correcting C2, a C2 pointer is generated. C1, C2 Pointers send error information or the data to which ECC is given. After correcting C2, against uncorrectable data, Error Data is sent by outputing a C2 Flag.
The signal C2FL is AND signal of C2F1 and C2F2. By using this information, Data is treated in the interpolator block.

C1F1	C1F2	C1, C2 Error	C2F1	C2F2	C2FL
0	0	No Error	0	0	0
0	1	Single Error	0	1	0
1	0	Double Error	1	0	0
1	1	Irretrievable Error	1	1	1

Fig. 17

C1F1, C1F2 — Output the state of an error correction by C1 Decoder

C2F1, C2F2 — Output the state of an error correction by C2 Decoder

C2FL — Becomes 'L' when an error correction by C2 Decoder is possible and an 'H' error correction is impossible.

16K SRAM BLOCK

After EFM demodulation of EFM modulated data inputted from disc, when the data is written into RAM is outputted to Read/Write and D/A Converters in ECC Processing for reading a SRAM Address Generator and a 16K SRAM is installed. SRAM terminal must be 'H' in a 16K SRAM application.

1) Address Generation Priority Control

Writing in EFM demodulation, reading the data with R/W, and a D/A Converter in the ECC process are sometimes required at the same time.
When 3 signals are demanded at the same time, priority of the data process needs to be controlled. Priority is D/A Converter Read demand > EFM Write demand > ECC R/W demand.

2) EFM Demodulation Data Write Demand

EFM demodulated data must be written to SRAM. Priority is controlled when the write demand signal is transmitted to the SRAM Address Generator, and the Enable signal is transmitted to the EFM Block. The generated address is transmitted to the SRAM Interface circuit.
A generated address is data in which deinterleave is considered, and a frame 32 address is generated.

A. In the use of 16K SRAM (in EFM & ECC Write): SRAM terminal 'H'

DB1 ~ DB8 and AD1 ~ AD11 terminals are in a state of Hi-Z. $\overline{CE}$ and $\overline{WE}$ are 'Don't Care.'

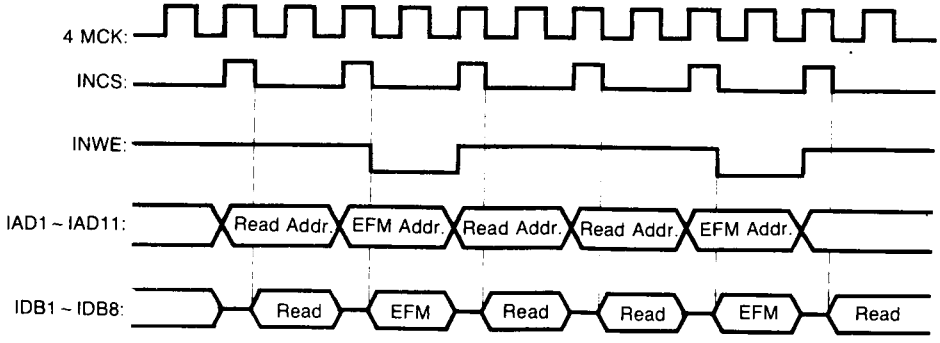
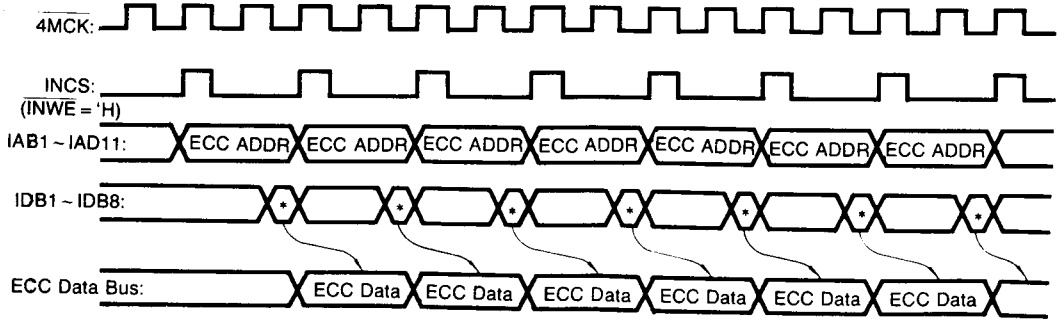


Fig. 18

3) R/W Demand of ECC Data

For C1 and C2, ECC treatment is 129 times of the Address demand signals generated, due to an R/W operation, and must be given to 64 PCM data and 65 Pointers during a frame.
The write of FCC processing is the same as 2) an EFM Write operation.
In reading, it is as follows:

A. In the use of 16K SRAM Reading Timing (SRAM: H)



*: Valid ECC Data

Fig. 19

4) D/A Converter Read Demand

Since each 6 sampling data on the left and right channel and 12 C2 Pointer data must be read for a frame, 36 read enable demand signals are caused. The timing chart for a D/A Converter Read is the same as the R/W demand block of ECC data. As a result, the number of the maximum R/W operation action demanded for a frame is 179.

5) Address Generated Block

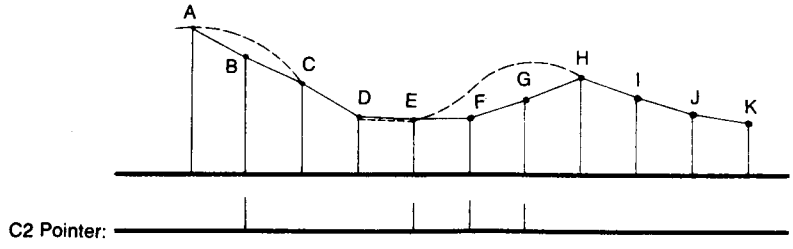
The interleaving data in encoding is deinterleaved in decoding. The data of 108 frames is needed to get 8 frames of PCM data in a CDP format. To get data suitable for a CDP format, 2 counters are needed. A write base counter is used to write. EFM demodulation data are hindered in storing data in SRAM due to disk shaking, the instability of a servo system, etc.

6) Jitter Margin

EFM demodulation data are hindered in storing data in SRAM due to disk shaking, the instability of a servo system, etc. Now that the data that must be kept is limited by the size of SRAM in view of time, data is destroyed if the value of the read/write base counter has a difference above ± 5 frames. Loading into the value of the write base counter with enforcement, the value of read the base counter has a jitter margin below ± 4 frames when there is a difference of over ± 5 frames in the read/write base counter value.
A read base counter value is loaded into a write base counter with enforcement when data on the left and right channels are all muting, or when NCLV is 'H' and CLV-Servo is stop, forward or reverse. When the difference between the read/write base counter is above ± 4 frame, a 'H' signal is outputted to the JIT terminal for a period.

INTERLEAVE, MUTE BLOCK

When a burst error occurs on a disk, sometimes the data can't be corrected even if a ECC process is conducted. An interpolator block revises data by using a C2 Pointer outputted through the ECC Block. PCM data inputted to a data bus are inputted to the left and right channels, respectively, in the order of 8-bit C2 Pointer, Lower 8-bit, and Upper 8-bit. A pre-hold method is taken when a DA Flag is 'H' continuously. In case of the occurrence of a single error, a mean value interploating method is carried out with the range of the PCM Data before and after an error happens. When a check against a checked cycle is 'L', R-CH Data is outputted. L-CH Data is outputted when the check is 'H'. For the timing chart of an interpolator block see figure 6.



$B = \frac{A+C}{2}$: Mean value interpolation

F = E = D : Pre-hold interpolation

G = F + H : Mean value interpolation

Fig. 20

2) Mute and Attenuation

By using a Mute terminal and the ATTM signal of the CNTL-S Reg., AUDIO data is muted or reduced. There are two kinds of mute: zero-cross muting and muting.

A. Zero-Cross Muting
Audio data is muted when a mute terminal is 'H' and when 6 bits in a high position of Audio Data are all 'H' or 'L'.

B. Muting
Audio data is muting when ZCMT of the CNTL-Z Reg. is 'L' and when a mute terminal is 'H'.

C. Attenuation
By means of the ATTM signal of the CNTL-S Reg. and the signal of the Mute terminal, an audio signal attenuation occurs as the following.

ATTM	MUTE	Degree of Attenuation
0	0	0 dB
0	1	– ∞ dB
1	0	– 12 dB
1	1	– 12 dB

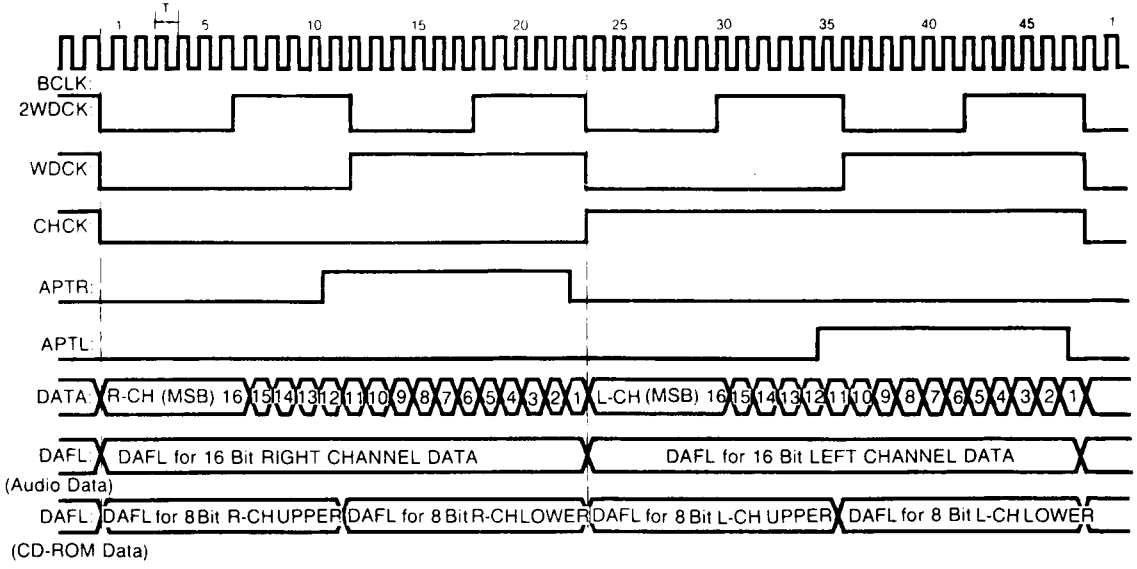


Fig. 21. When Sel. 5 is 'L', and DF is off, the Timing Chart of PCM Data

CLV SERVO

CNTL-C Reg. is selected to control CLV Servo by the Data inputted from μ-COM. In CNTL-C Reg, the data from μ-com appoints CLV servo action mode and controls the spindle motor.

1) Forward

The states of output terminal, related to the mode that rotates a spindle motor forward, are SMDP = 'H', SMSD = Hi-Z, SMEF = 'L' and SMON = 'H', respectively.

2) Reverse

The modes to rotate a spindle motor reversly are SMDP = 'L', SMSD = 'Hi-Z', SMEF = 'L', and SMOD = 'H'.

3) SPEED-Mode

The SPEED-Mode is the mode for the rough control of a spindle motor when a track is jumps or a EFM phase is unlocked. If a cycle of VCO is 'T', the pulse width of a frame sync is '22T'. Sometimes an EFM signal is above 22T, due to noises on a disc, etc. A correct frame sync cannot be detected when the signal is not removed. In this case, the pulse width of an EFM signal is detected at a cycle of XTFR/2 or XTFR/4, which are peak hold clocks. The pulse width an of EFM signal is detected at a cycle of XTFR/16 or XTFR/32, which are bottom hold clocks. The value detected is used for a frame synchronization signal. When the frame synchronization signal is smaller than 21T, the SMPD terminal outputs 'L'. When it is 22T, Hi-Z is outputted. 'H' is outputted when it is above 23T.
When the GAIN signal of CNTL-W Reg. is 'L', the SMDP terminal is outputted after being attenuated at – 12dB. When the signal is 'H', the terminal is outputted without any attenuation. <cf. figure 22>
In SMSD, SMEF, and SMON terminals Hi-Z, 'L', and 'H' are outputted.

4) HSPEED-Mode

The rough servo mode, which moves 20,000 tracks in high speed, acts between the inside of the CD and the outside of the CD. In the domain of a mirror of the track without, a pit EFM and the signal of 20KHz overlap. In this case, since in a speed-mode the peak range of a longer mirror signal than the original frame sync is detected, a servo operation becomes unstable. In HSPEED-mode, a peak hold uses a 8.4672/256 MHz signal, and a bottom hold removes a mirror component and stabilizes the high speed servo operation by using an XTFR/16 or XTFR/32 period signal.
In SMSD, SMEF, and SMON terminals, Hi-Z, 'L', and 'H' are outputted.

5) PHASE-Mode

A PHASE Mode is the mode that control an EFM Phase. When NCLV of CNTL-Z is 'L', it detects a phase difference between PBFR/4 and XTFR/4, and when NCLV is 'H', it detects the phase difference between Read base Counter/4, and write base Counter/4, and then outputs to the SMPD terminal. See figure 8.
If the VCO/2 signal cycle is put as 'T' and the PBFR, during a 'H' period, as a V_{pb}, it outputs 'H' to a SMSD terminal from the falling edge of PBFR for $(W_{pb}\text{-}278T) \times 32$, and later outputs 'L' to the falling edge of PBFR. Refer to figure 24

6) XPHSP-Mode

A XPHSP mode is the mode used in normal operation. It samples a LKFS signal made in the frame sync block at a cycle of PBFR/16. After sampling 'H', DHASE mode is carried out. When 'L' is sampled continuously 8 times, it goes over to speed-mode. CNTL-W Reg. decides the choice of the peak hold of the speed-mode, the bottom hold cycle of SPEED-and HSPEED-Mode, and the choice of a gain.

7) VPHSP-Mode

A VPHSP-Mode is the mode used for rough servo control. It uses VCO instead of X'tal in the EFM pattern test. When the range of VCO center changes, VCO is easily loaded because the rotation of a spindle motor changes in the same direction.

8) STOP

Stop is the mode used to stop a spindle motor.
SMDP = 'L', SMSD = Hi-Z, SMEF = 'L', SMON = 'L'

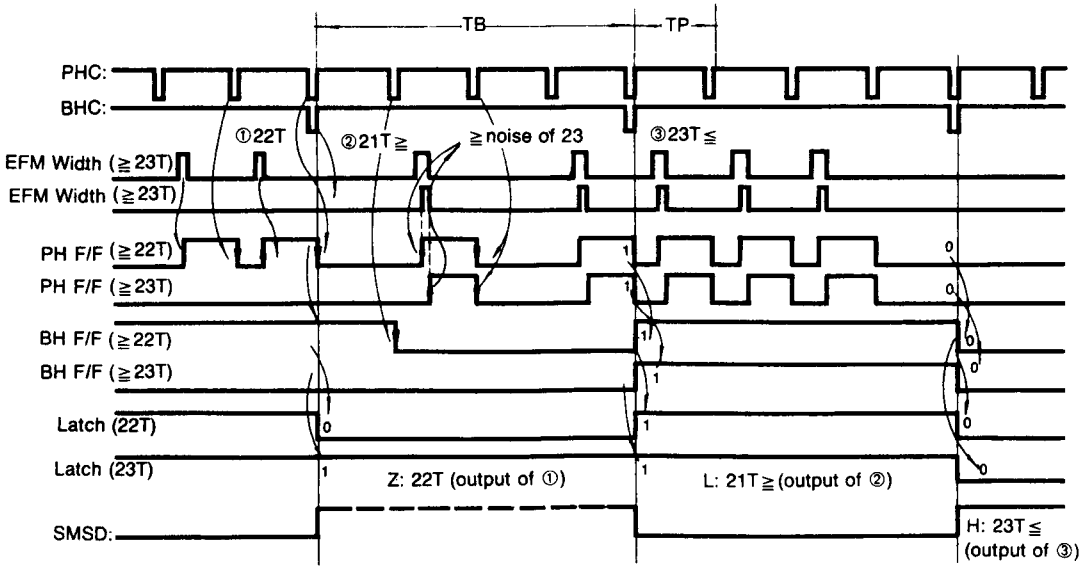


Fig. 22 When gain is 'H' in a speed-mode Timing Chart of SMSD output

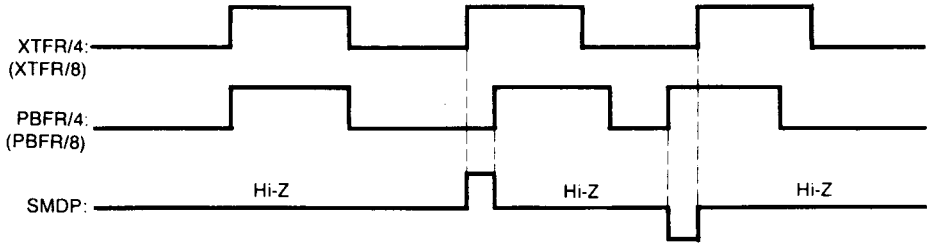
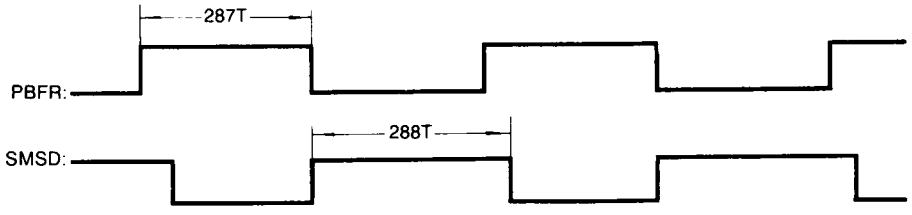
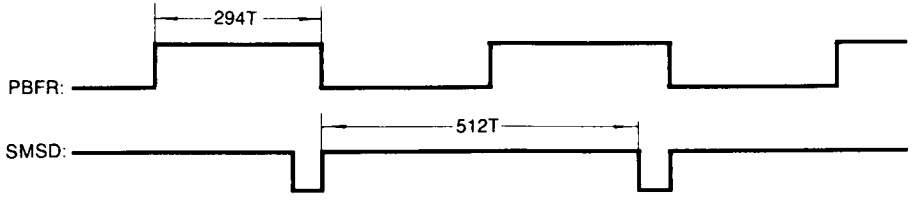


Fig. 23 Output Timing Chart of a SMDP terminal



(a) When PBFR is 287T, Timing Chart of SMSD output



(b) When PBFR is 294T, Timing Chart of SMSD output

Fig. 24 In a PHASE Mode Timing Chart of SMSD output (T: VCO/2)