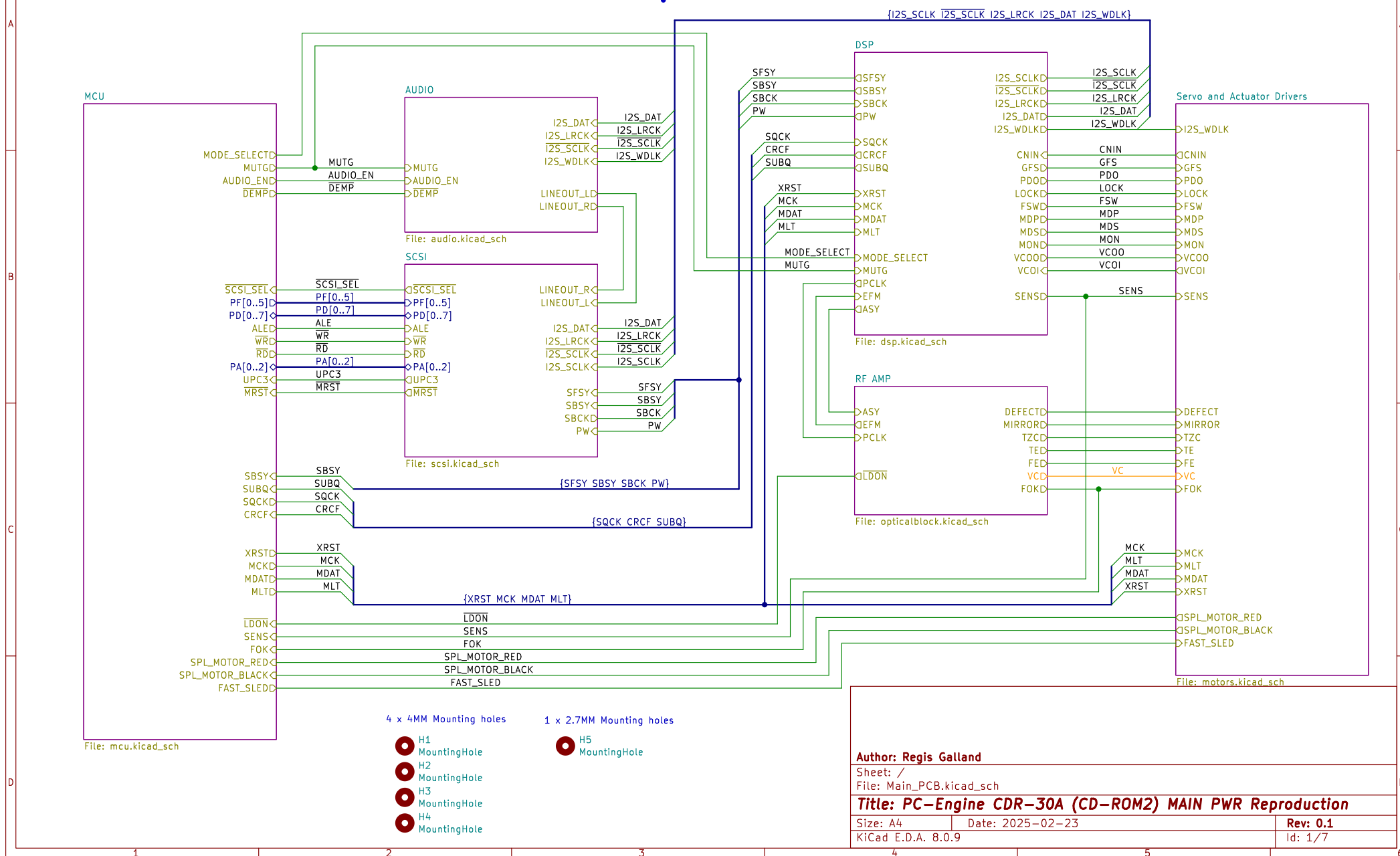


MAIN PWR Reproduction Schematics

Top Level



Author: Regis Galland

Sheet: /

File: Main_PCB.kicad_sch

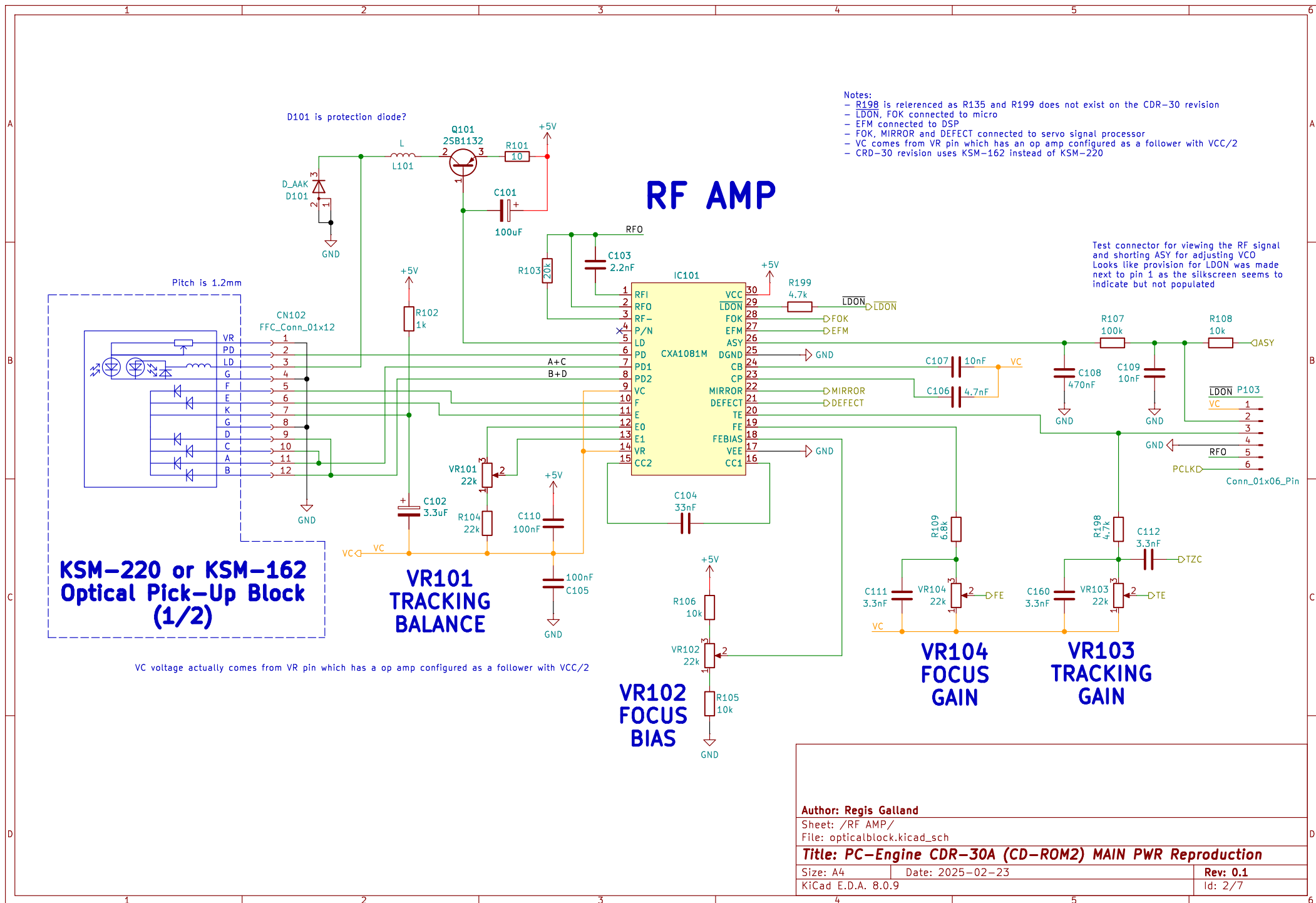
Title: PC-Engine CDR-30A (CD-ROM2) MAIN PWR Reproduction

Size: A4 Date: 2025-02-23

Rev: 0.1

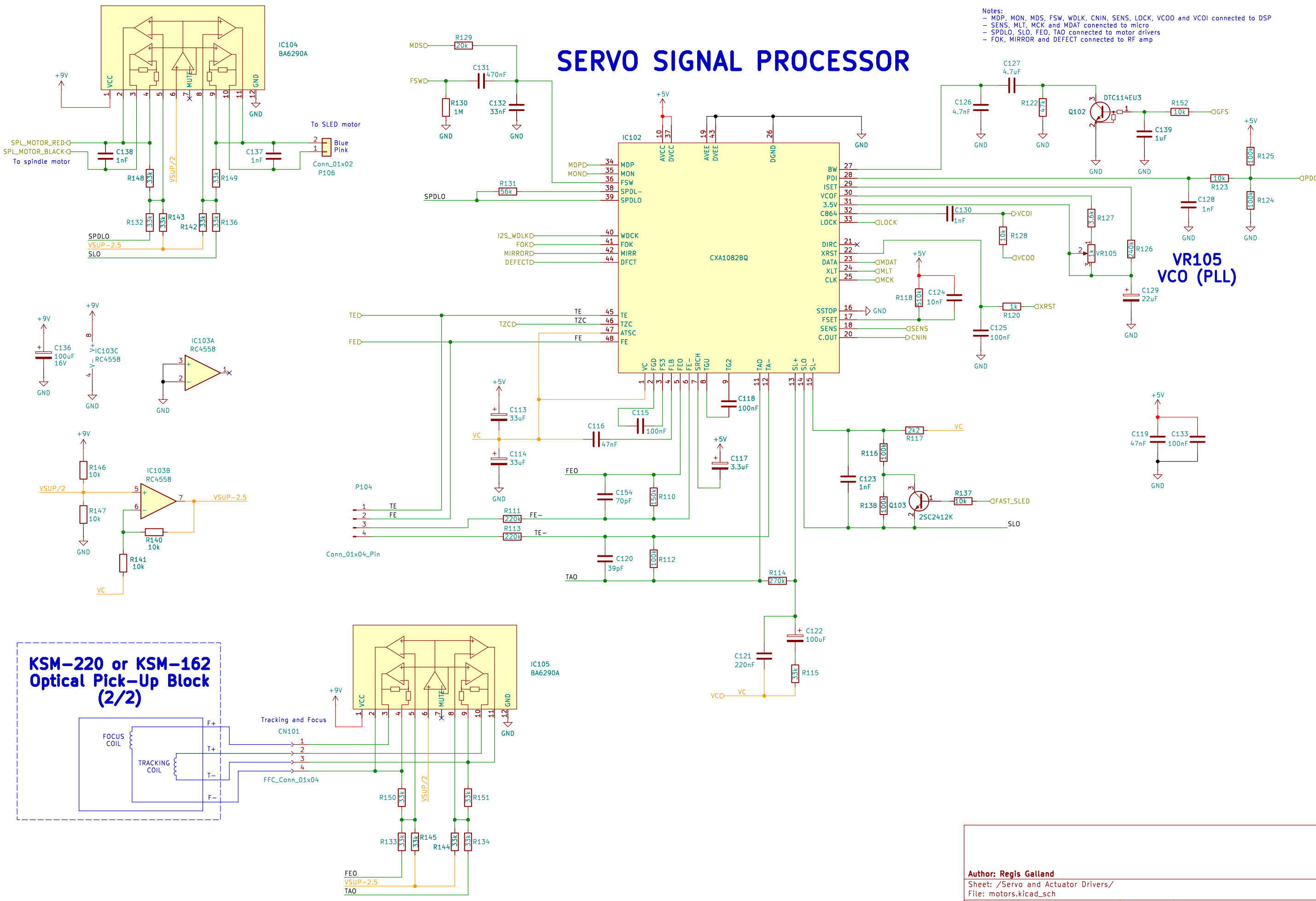
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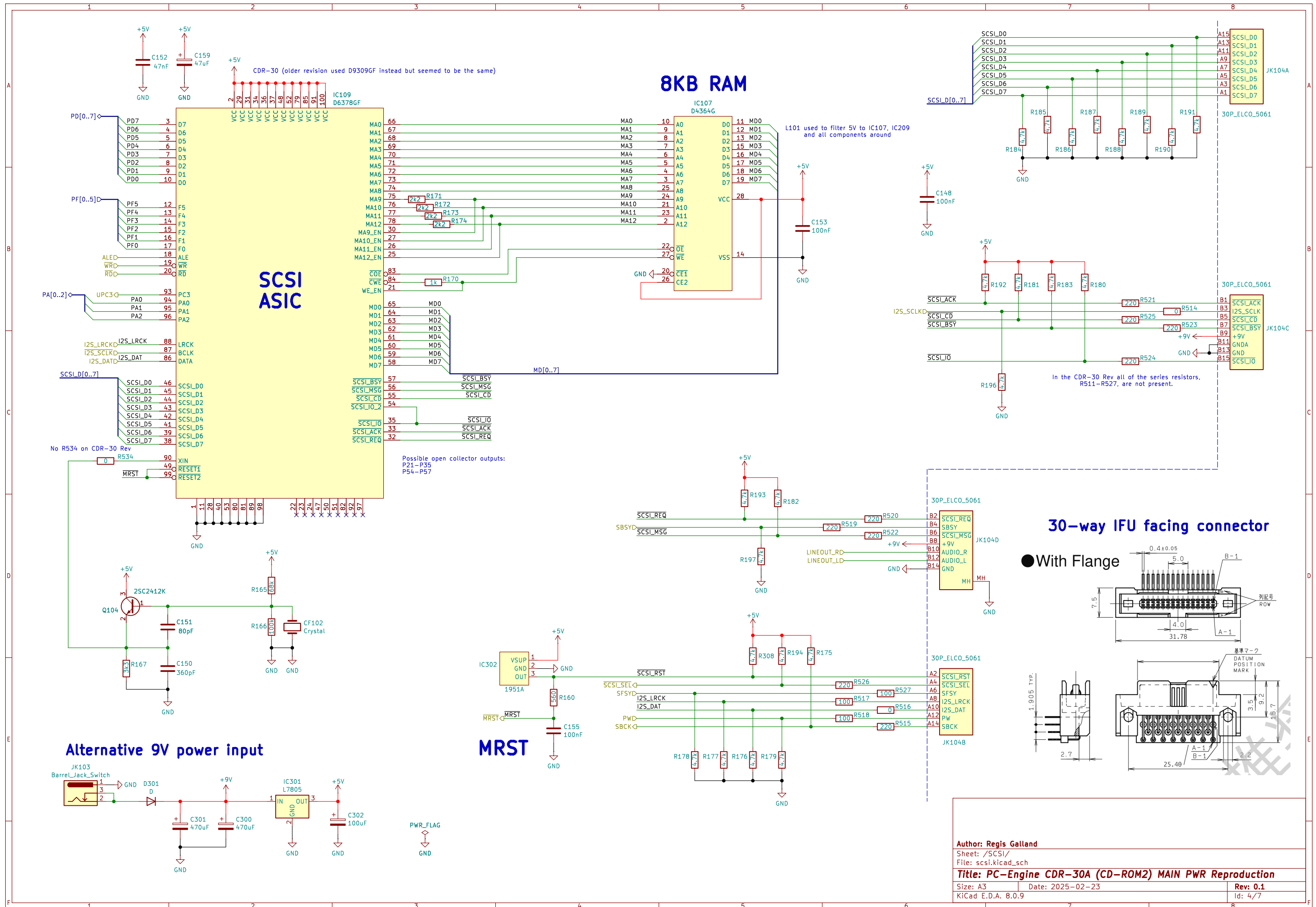
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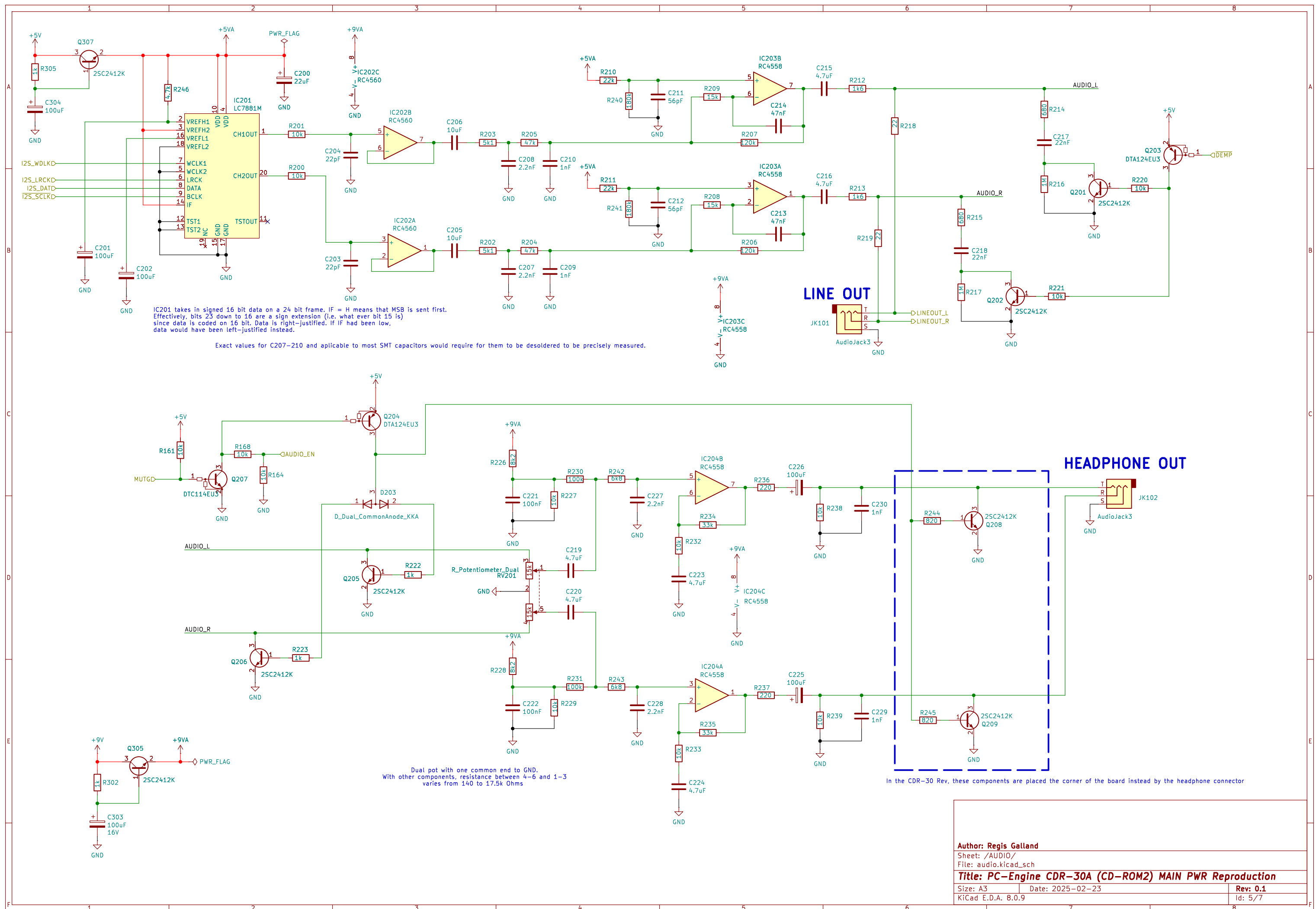


SERVO SIGNAL PROCESSOR

- Notes:
- MDP, MON, MDS, FSW, WDLK, CNIN, SENS, LOCK, VCO0 and VCOI connected to DSP
 - SENS, MLT, MCK and MDAT conencted to micro
 - SPDLO, SLO, FEO, TAO connected to motor drivers
 - FOK, MIRROR and DEFECT connected to RF amp







CDR-30 (older revision used CXD1135 with external RAM IC107 HM6116 instead but seemed to be the same). CXD1167 must have built in RAM
 - Edit: some CDR-30As also come with CXD1135 + RAM

Subcode signals to IFU connector on pin B4, A12, A14
 SBSY (Block synchronization) also connected to MCU's interrupt input
 SBCK comes from IFU
 PW is Subcode data P to W (8-bits)

IOs connected to MCU
 SQCK is an input when SQEX=H
 All subcode Q related signals
 2 possible modes:
 1) "10000" (audio mode)
 where XIN = 8MHz, Digital filter is ON, audio is send via serial output
 Audio data is always using 2's complement output format
 2) "11101" (data mode) Speculative operation as no datasheets exist for CXD1135 or CXD1167 but Samsung K55990 for which I have a datasheet seems to be identical to CXD1167 at least. Nonetheless, this mode combination is not shown in the list so I assume this is the data mode MD1 = MD2 = MD3 = '1' means CD-ROM where DF off, 2's complement data format but serial output in spite of PSSL = '1'.

GFS is the output of the lock conditions of frame sync

SFSY (subcode frame sync) to IFU connector on pin A6

R528 to R536 do not exist on the older revision CDR-30

When streaming audio, LRCK frequency is 88.2KHz
 i.e. normal CD audio sampling frequency x 2.
 DSP documentation mentions it is the case when the digital filter is enabled.
 I assume this for doing sample interpolation.

DSP

Author: Regis Galland

Sheet: /DSP/
 File: dsp.kicad_sch

Title: PC-Engine CDR-30A (CD-ROM2) MAIN PWR Reproduction

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Rev: 0.1

Id: 6/7

ALE latches addresses to PD0-7 when high and presents data when low. PD0-7 and PF0-5 are connected to SCS1 chip but PF5 is also connected to the display update signal through a diode. Since writing to display requires both WR and PF5 to be low because of the logical 'OR' with diodes, it might then mean that addresses from 0000h to 1FFFh are ignored by the SCS1 IC (i.e. PF5 is a chip select pin) but addresses from 2000h to 3FFFh will be seen as read or write operations to the 8KB RAM (0000h-1FFFh).

