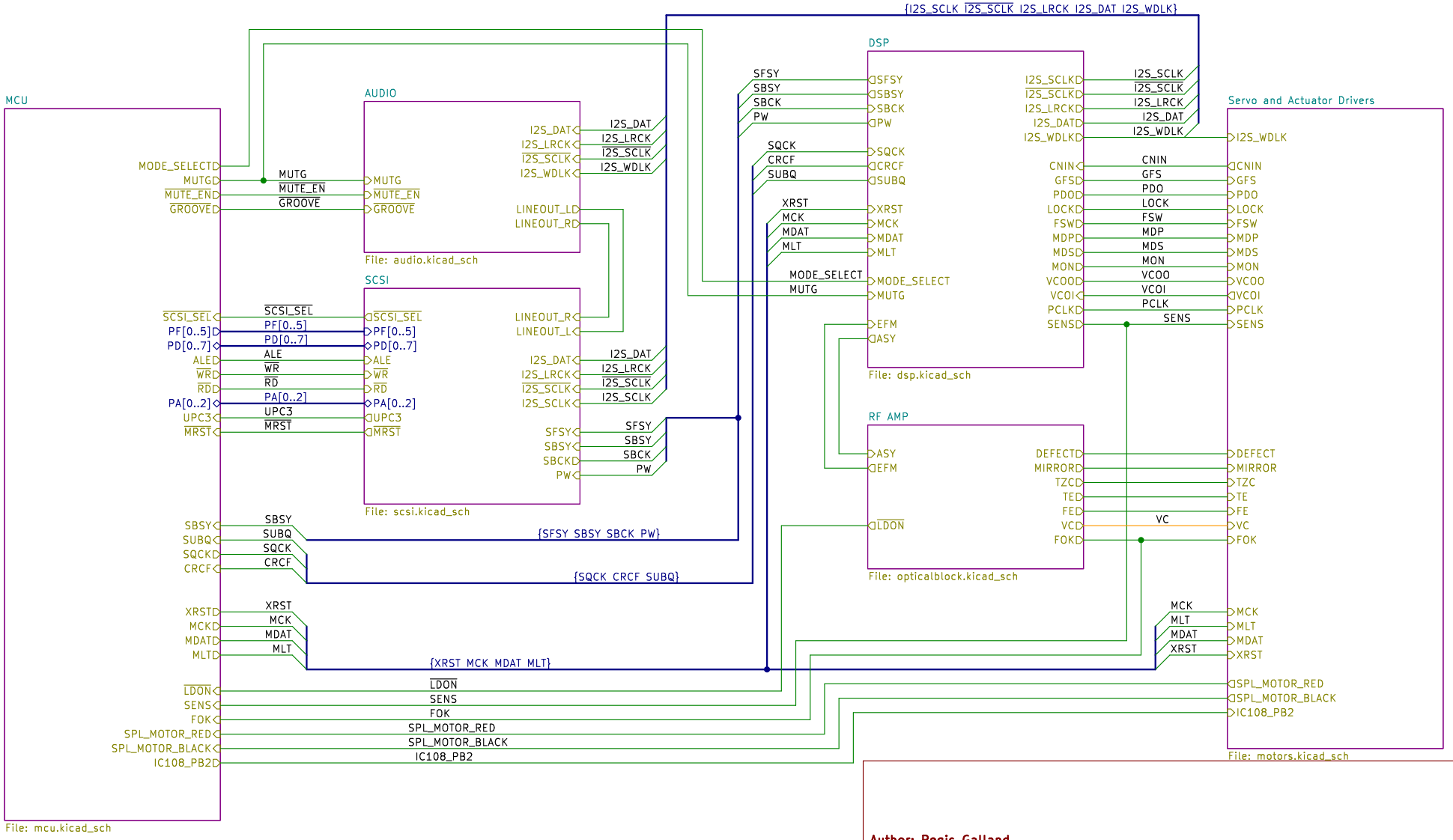
SOT23 Transistor with AAR22 Marking = NPN BEC
SOT23 Transistor with BR22 Marking = NPN BEC

Mentions some differences between the CDR-30A and the older CDR-30 revision.

PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR
Top Level



Author: Regis Galland		
Sheet: /		
File: MAIN_PWR.kicad_sch		
Title: PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR		
Size: A4	Date: 2024-05-03	**Rev: 0.1**
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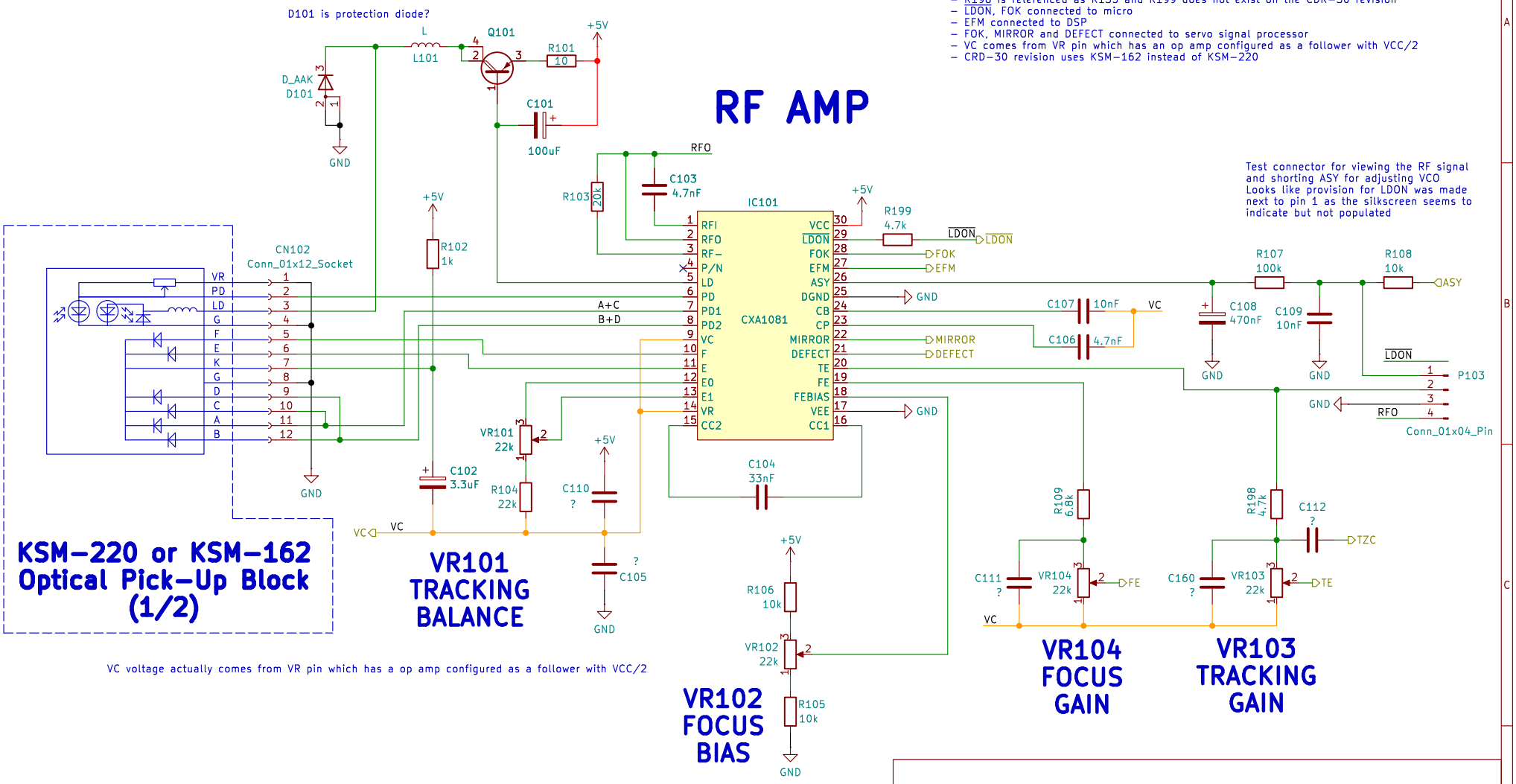
RF AMP

Notes:
- R198 is relerenced as R135 and R199 does not exist on the CDR-30 revision
- LDON, FOK connected to micro
- EFM connected to DSP
- FOK, MIRROR and DEFECT connected to servo signal processor
- VC comes from VR pin which has an op amp configured as a follower with VCC/2
- CRD-30 revision uses KSM-162 instead of KSM-220

D101 is protection diode?

Test connector for viewing the RF signal and shorting ASY for adjusting VCO
Looks like provision for LDON was made next to pin 1 as the silkscreen seems to indicate but not populated



KSM-220 or KSM-162 Optical Pick-Up Block (1/2)

VR101 TRACKING BALANCE

VR102 FOCUS BIAS

VR104 FOCUS GAIN

VR103 TRACKING GAIN

VC voltage actually comes from VR pin which has a op amp configured as a follower with VCC/2

Author: Regis Galland		
Sheet: /RF AMP/		
File: opticalblock.kicad_sch		
Title: PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR		
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SERVO SIGNAL PROCESSOR

Notes:
- MDP, MON, MDS, FSW, WDLK, CNIN, SENS, LOCK, VCOO and VCOI connected to DSP
- SENS, MLT, MCK and MDAT conencted to micro
- SPDLO, SLO, FEO, TAO connected to motor drivers
- FOK, MIRROR and DEFECT connected to RF amp

VR105 VCO (PLL)

KSM-220 or KSM-162 Optical Pick-Up Block (2/2)

IC104 BA6290A
IC105 BA6290A
IC102 CXA1082BQ
IC103A RC4558
IC103B RC4558
IC103C RC4558

SPL_MOTOR_RED
SPL_MOTOR_BLACK
To spindle motor
To SLED motor
P106 Conn_01x02_Pin
P104 Conn_01x06_Pin
CN101 Conn_01x04_Socket
Tracking and Focus
FOCUS COIL
TRACKING COIL
F+ F- T+ T-

MDS FSW SPDLO VSUP-2.5 SLO VSUP/2 VC VCC
I2S_WDLK FOK MIRROR DEFECT
TE TZC FE FEO TAO
MDP MON FSW SPDL- SPDLO
BW PDI ISET VCOF 3.5V C864 LOCK
DIRC XRST DATA XLT CLK
SSTOP FSET SENS C.OUT
WDCK FOK MIRR DFCT
VC FGD FS3 FLB FEO FE- SRCH TGU TG2 TAO TA- SL+ SLO SL-
PDO GFS VCOI VCOO MDAT MLT MCK SENS CNIN XRST LOCK
PCLK FE TE VC

Author: Regis Galland
Sheet: /Servo and Actuator Drivers/
File: motors.kicad_sch

Title: PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR

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L101 used to distribute 5V to IC107, IC209 all around components around

CDR-30 (older revision used D9309GF instead but seemed to be the same)

8KB RAM

SCSI ASIC

MRST

Alternative 9V power input

In the CDR-30 Rev all of the series resistos, R511-R527, are not there.

Author: Regis Galland	
Sheet: /SCSI/	
File: scsi.kicad_sch	
Title: PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR	
Size: A3	Date: 2024-05-03
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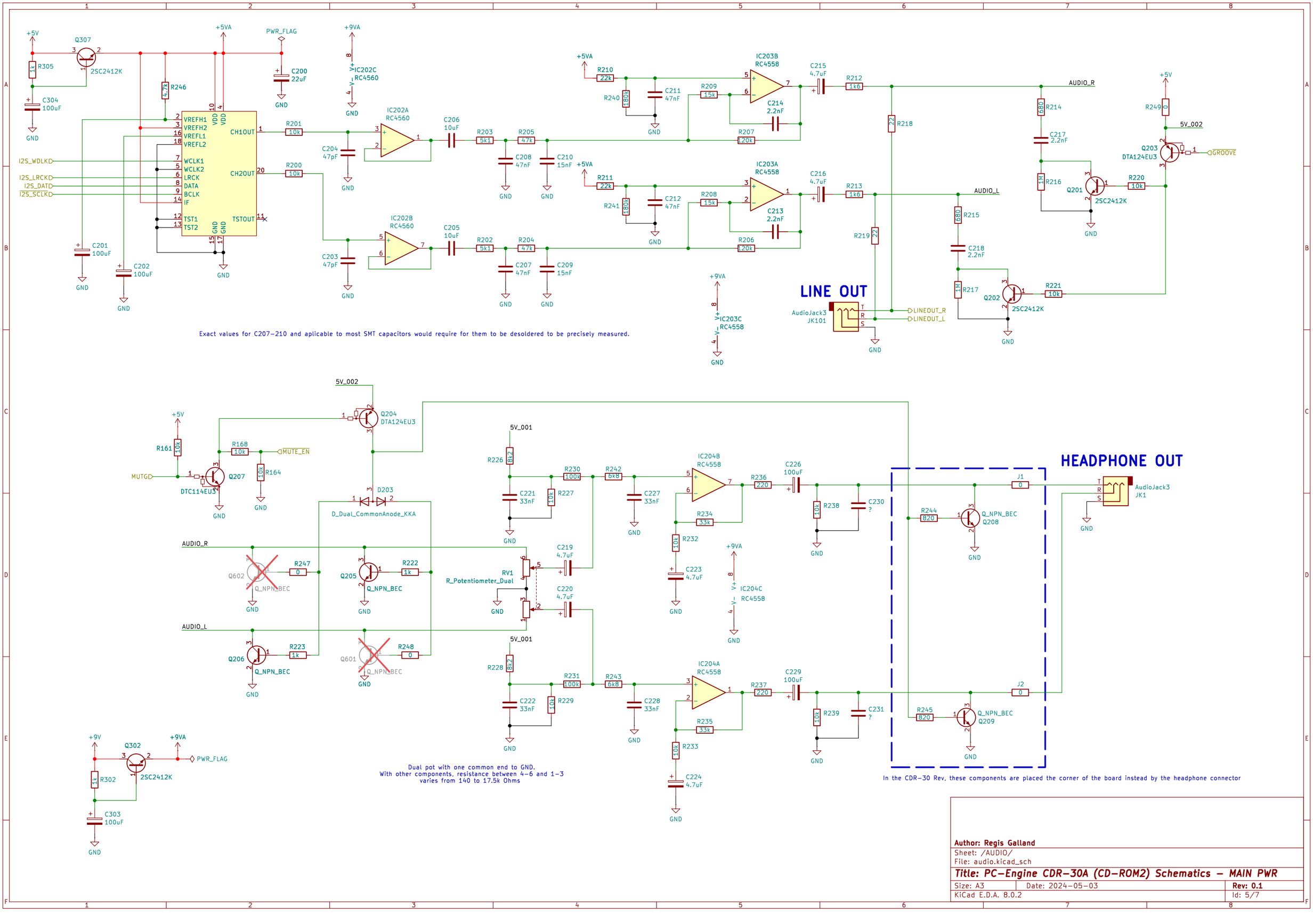
+5V
Q307
2SC2412K
R305
1k
C304
100uF
GND
+5VA
PWR_FLAG
C200
22uF
+9VA
IC202C
RC4560
R246
4.7k
VREFH1
VREFH2
VREFL1
VREFL2
WCLK1
WCLK2
LRCK
DATA
BCLK
IF
TST1
TST2
CH1OUT
CH2OUT
TSTOUT
VDD
GND
I2S_WDLK
I2S_LRCK
I2S_DAT
I2S_SCLK
C201
100uF
C202
100uF
R201
10k
R200
10k
IC202A
RC4560
IC202B
RC4560
C204
47pF
C203
47pF
C206
10uF
C205
10uF
R203
5k1
R202
5k1
R205
47k
R204
47k
C208
47nF
C207
47nF
C210
15nF
C209
15nF
IC203B
RC4558
IC203A
RC4558
IC203C
RC4558
R210
22k
R211
22k
R240
180k
R241
180k
C211
47nF
C212
47nF
R209
15k
R208
15k
C214
2.2nF
C213
2.2nF
R207
120k
R206
120k
C215
4.7uF
C216
4.7uF
R212
1k6
R213
1k6
R218
22
R219
22
AUDIO_R
AUDIO_L
R214
680
R215
680
C217
2.2nF
C218
2.2nF
R216
1M
R217
1M
Q201
2SC2412K
Q202
2SC2412K
R220
10k
R221
10k
R249
0
5V_002
Q203
DTA124EU3
GROOVE
LINE OUT
AudioJack3
JK101
T
R
S
LINEOUT_R
LINEOUT_L
Exact values for C207–210 and aplicable to most SMT capacitors would require for them to be desoldered to be precisely measured.
5V_002
Q204
DTA124EU3
+5V
R161
10k
MUTG
Q207
DTC114EU3
R168
10k
MUTE_EN
R164
10k
D203
D_Dual_CommonAnode_KKA
5V_001
R226
8k2
R228
8k2
R230
100k
R231
100k
R242
6k8
R243
6k8
C221
33nF
C222
33nF
R227
10k
R229
10k
C227
33nF
C228
33nF
IC204B
RC4558
IC204A
RC4558
IC204C
RC4558
R234
33k
R235
33k
R232
10k
R233
10k
C223
4.7uF
C224
4.7uF
C219
4.7uF
C220
4.7uF
RV1
R_Potentiometer_Dual
R236
220
R237
220
C226
100uF
C229
100uF
R238
10k
R239
10k
C230
?
C231
?
AUDIO_R
AUDIO_L
Q602
Q_NPN_BEC
R247
0
Q205
Q_NPN_BEC
R222
1k
Q206
Q_NPN_BEC
R223
1k
Q601
Q_NPN_BEC
R248
0
HEADPHONE OUT
J1
J2
0
R244
820
R245
820
Q208
Q_NPN_BEC
Q209
Q_NPN_BEC
AudioJack3
JK1
Dual pot with one common end to GND.
With other components, resistance between 4–6 and 1–3
varies from 140 to 17.5k Ohms
In the CDR–30 Rev, these components are placed the corner of the board instead by the headphone connector
+9V
Q302
2SC2412K
+9VA
PWR_FLAG
R302
1k
C303
100uF
Author: Regis Galland
Sheet: /AUDIO/
File: audio.kicad_sch
Title: PC–Engine CDR–30A (CD–ROM2) Schematics – MAIN PWR
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Rev: 0.1
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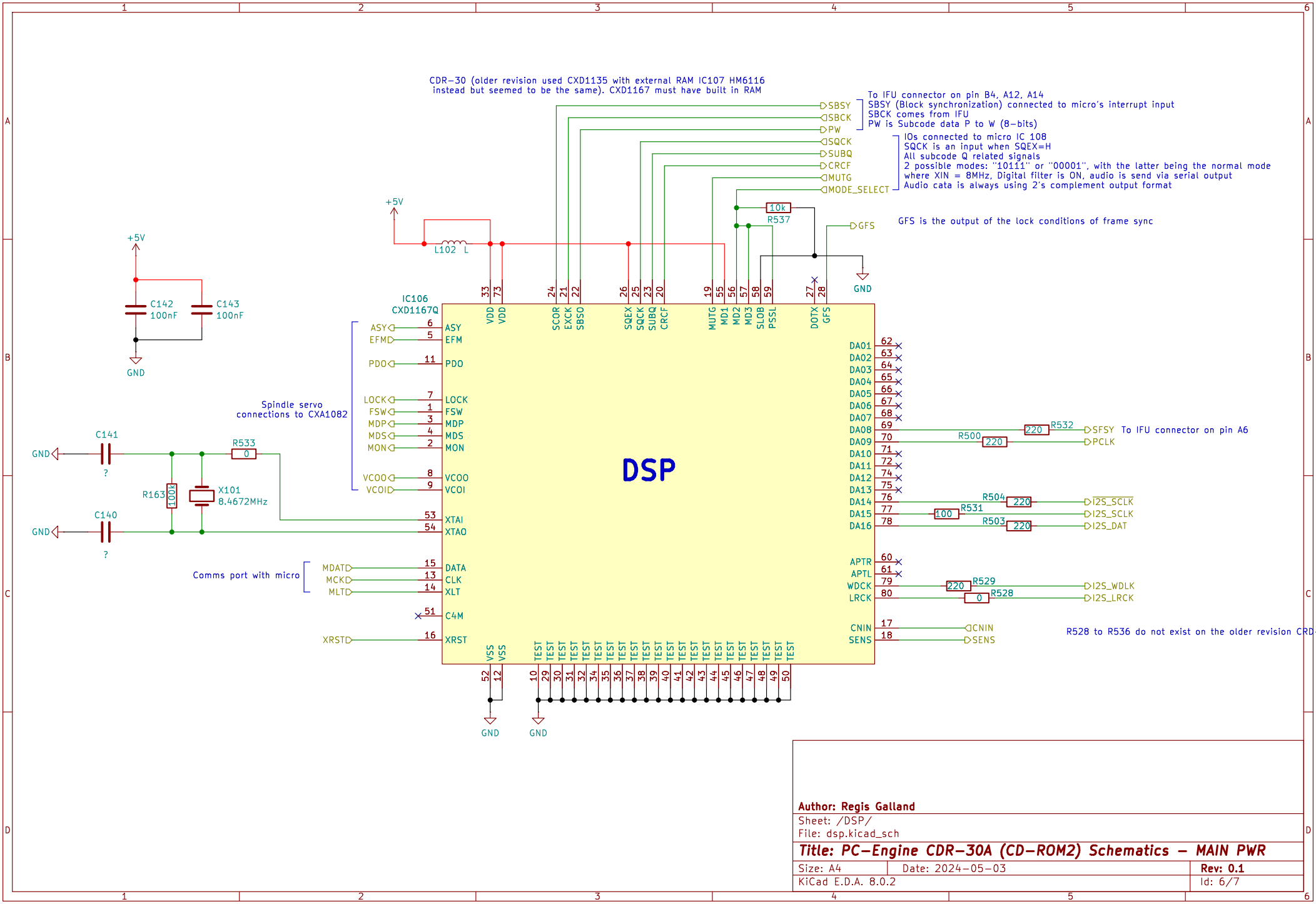

Author: Regis Galland	
Sheet: /DSP/	
File: dsp.kicad_sch	
Title: PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR	
Size: A4	Date: 2024-05-03
KiCad E.D.A. 8.0.2	Id: 6/7
	Rev: 0.1

Only SCSI_SEL is connected to this cjip so other IOs must be used to inform whether we are in a command or data stage. Equally, the micro needs to know when req is asserted to read data and then ack. This might be done with PC3 as it can be configured as an interrupt.
Perhaps the 8KRAM also stores the command bytes.

ALE latches address to PD0-7 when high and presents data when low. PD0-7 and PF0-5 are connected to SCSI chip but PF5 is also connected to the display update signal though a diode. Since writing to display requires both WR and PF5 to be low because of the logical 'OR' with diodes, it might then mean that addresses from 0000h to 1FFFh are ignored by the SCSI IC (i.e. PF5 is a chip select pin) but adresses from 2000h to 3FFFh will be seen as read or write operations to the 8KB RAM (0000h-1FFFh)

P101 Data bus is used to send 7 SEG Display data

P102 connector carries mainly signals coming button signal fron the front PCB

DIGIT1_EN, DIGIT2_EN can't be activated to PWM the Dual seg display. DIGIT1_EN also allows to read the state of all buttons except RS as this one is active when RS_EN is on. However, it seems possible for RS_EN and DIGIT2_EN to be on at the same time. AN inputs can be configured as falling edge interrupt inputs but I doubt that's how it works as the signals are pulled down

P107 is the CD lid switch. Contact is closed when lid is down Named P106 on CDR-30 Rev

P107 is the connection to the sled end stop switch

IC108 D78C14GF

8-bit Micro

Author: Regis Galland
Sheet: /MCU/
File: mcu.kicad_sch

Title: PC-Engine CDR-30A (CD-ROM2) Schematics - MAIN PWR

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