

Author: Regis Galland
Sheet: /
File: S-CPU.kicad_sch

End 8

100

26

CBTU

Title: Reverse Engineering

-02-1

12

1

1

Size: A2 Date: 2024-05-01

.10~u

buntu

22.0

4.1

KiCad E.D.A. kicad 7.0.10-7.0

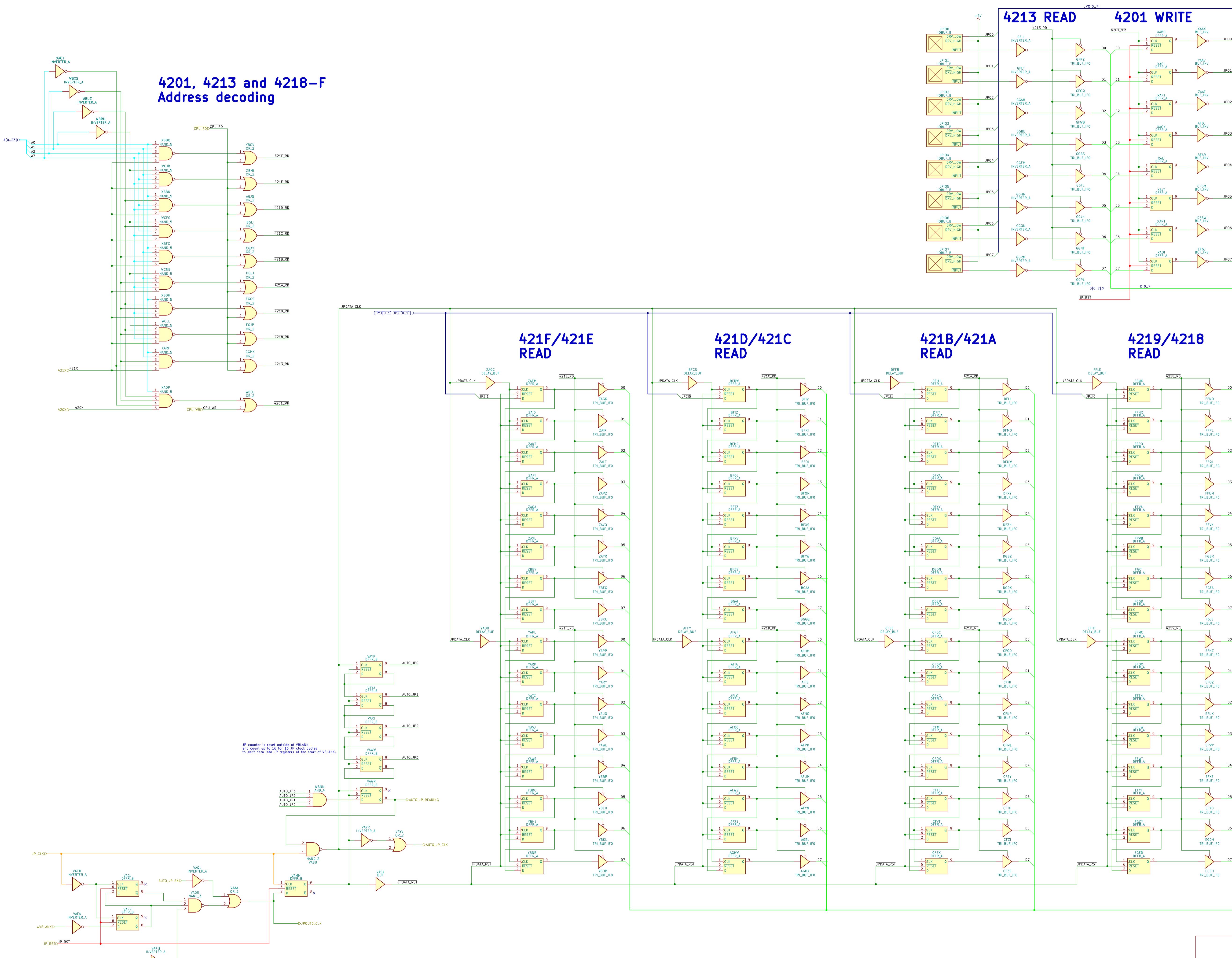
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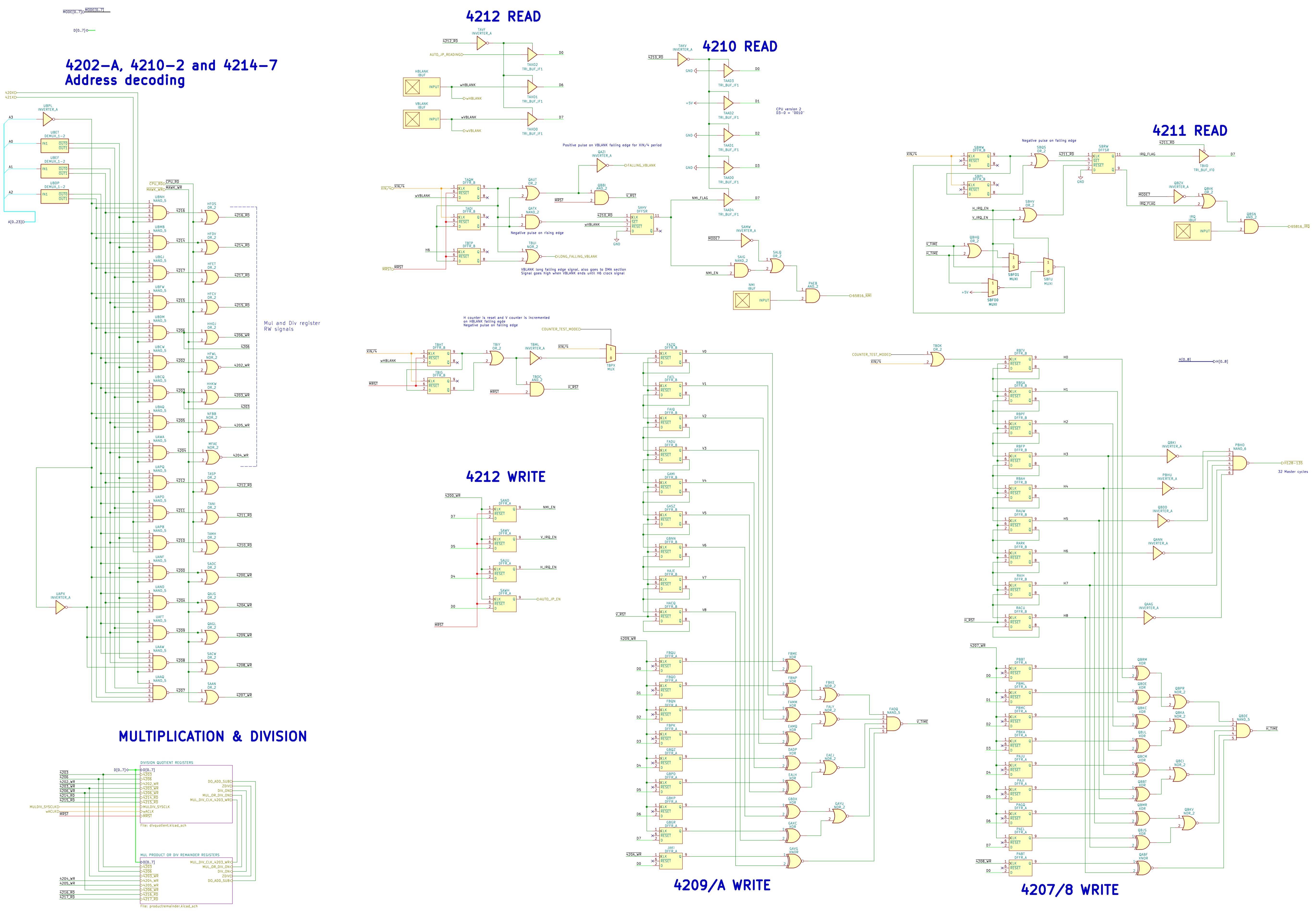
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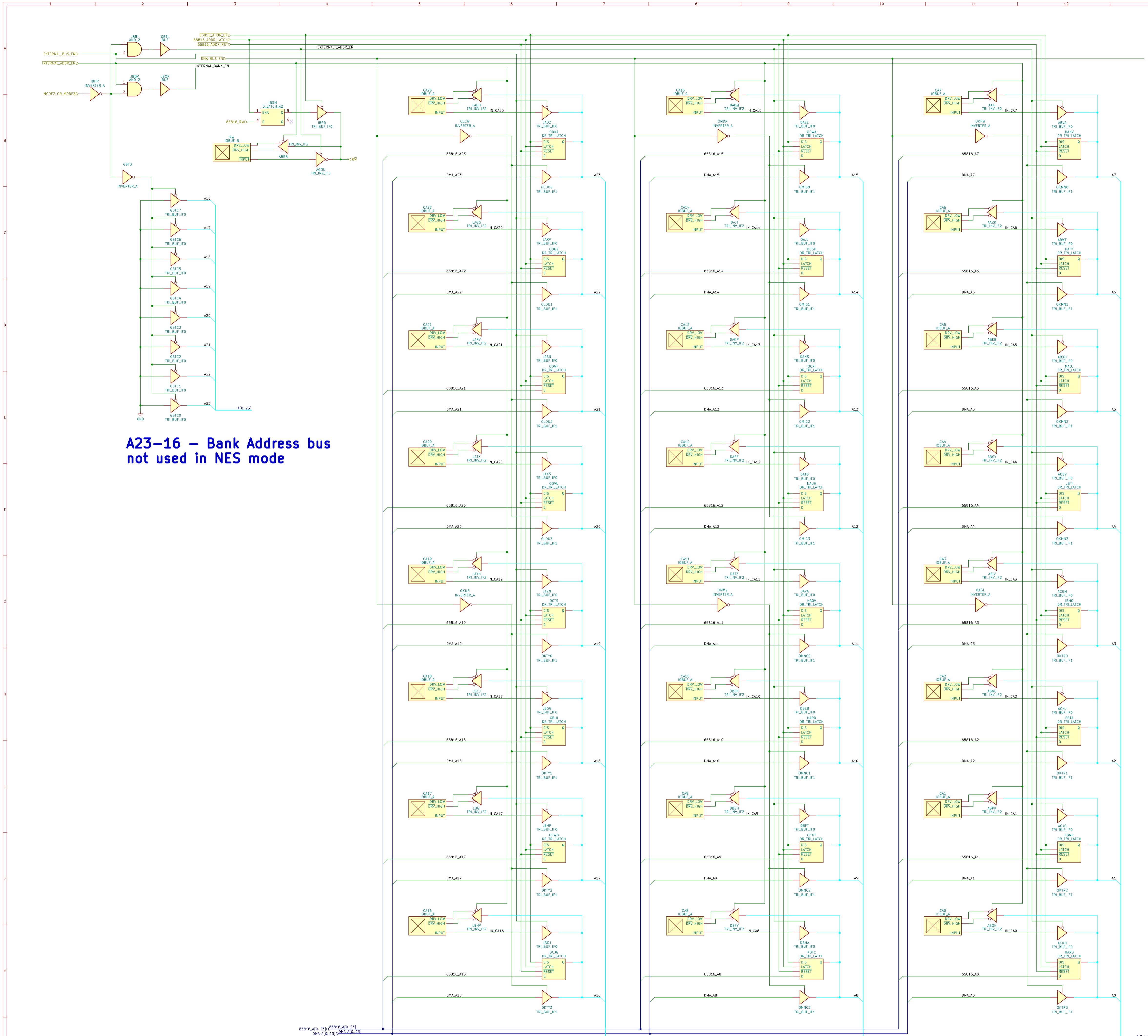
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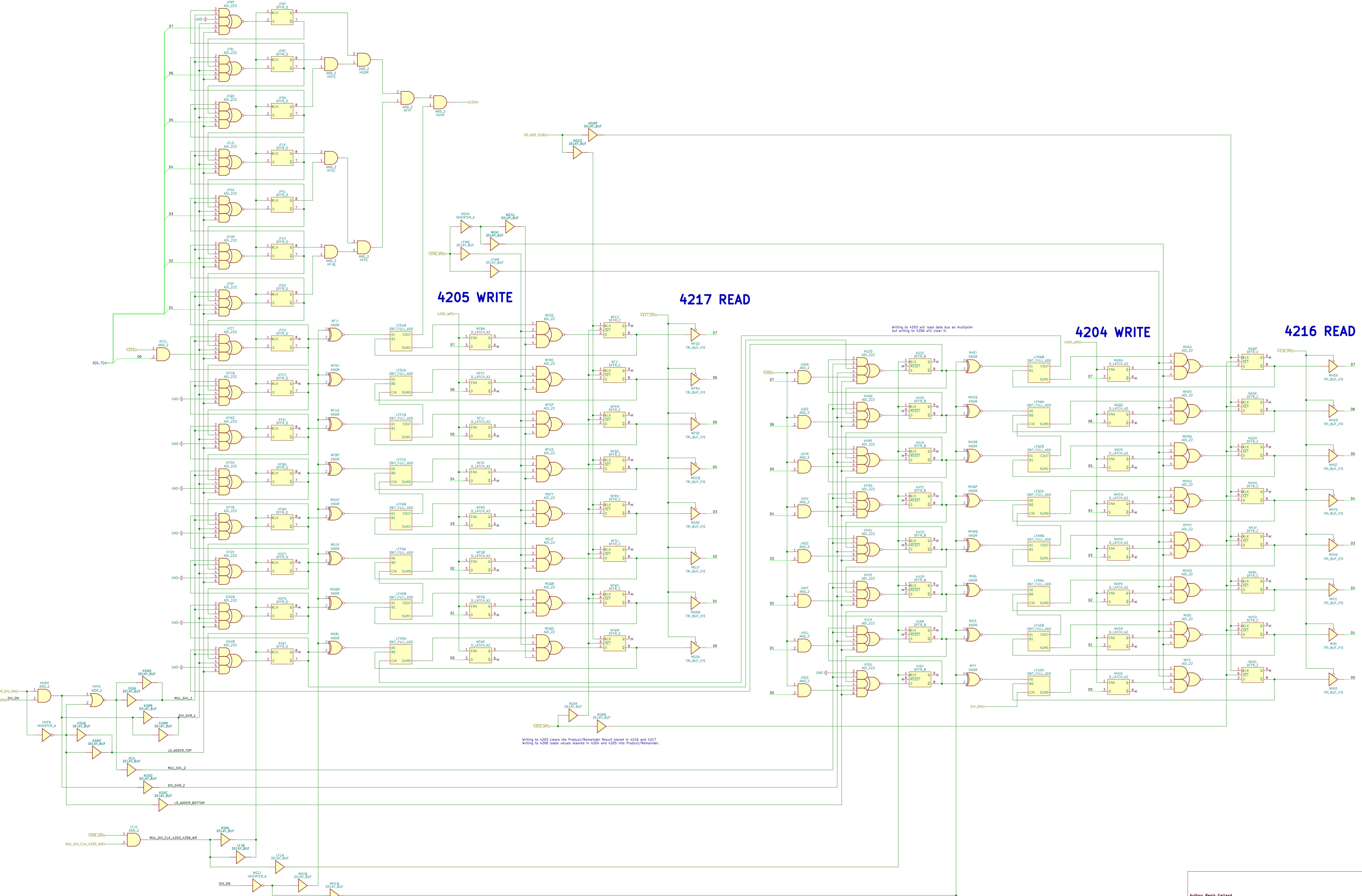


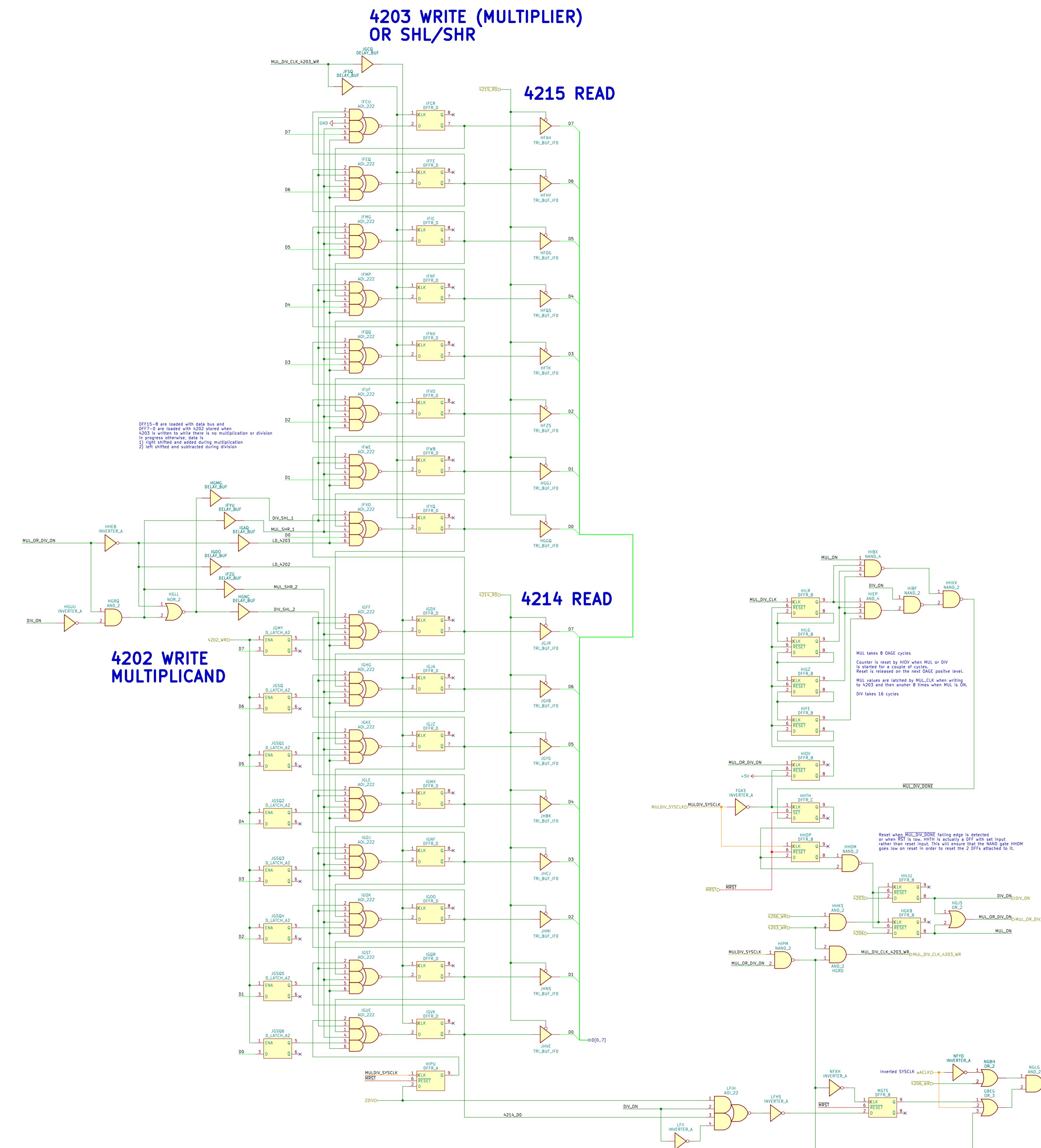


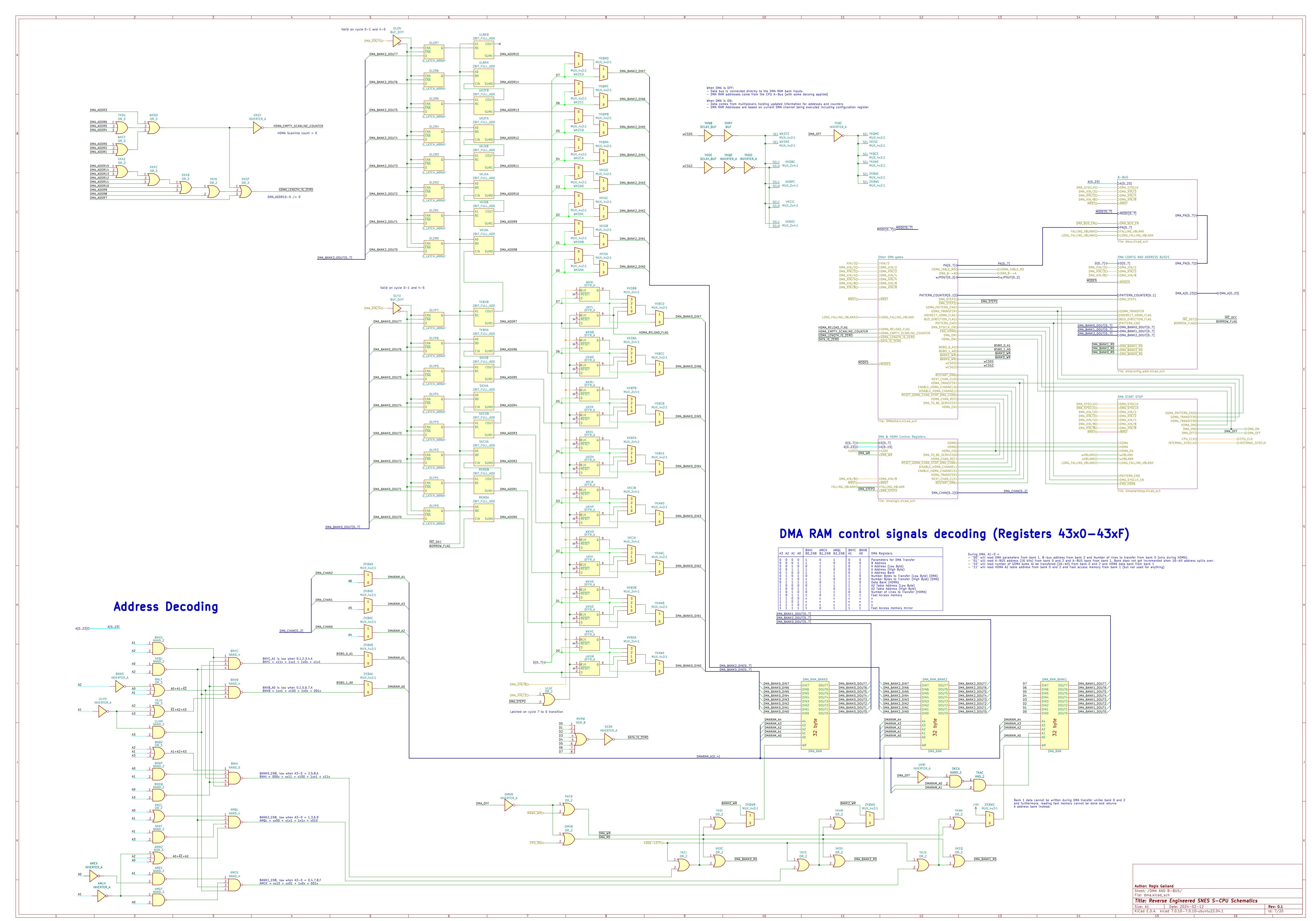


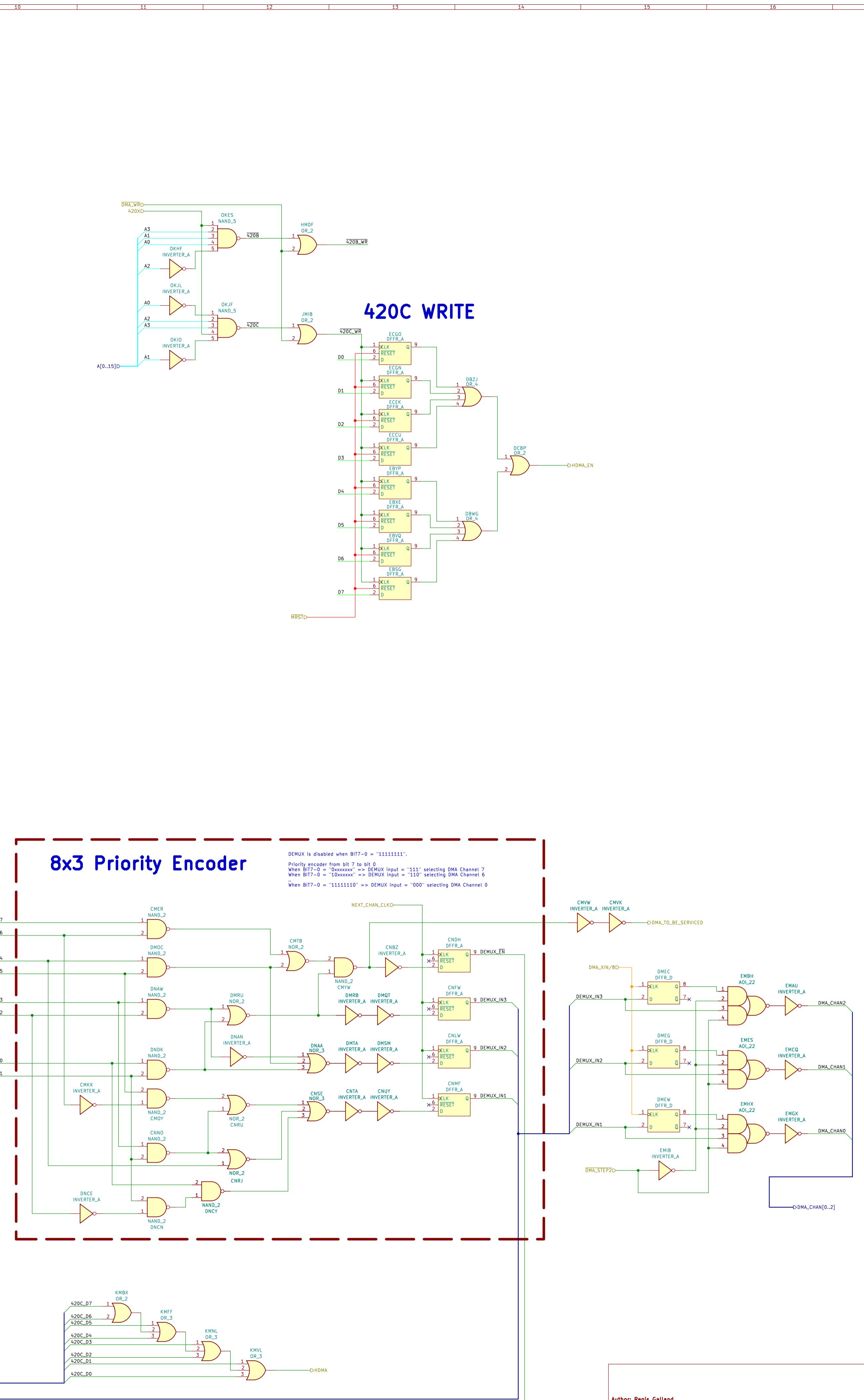
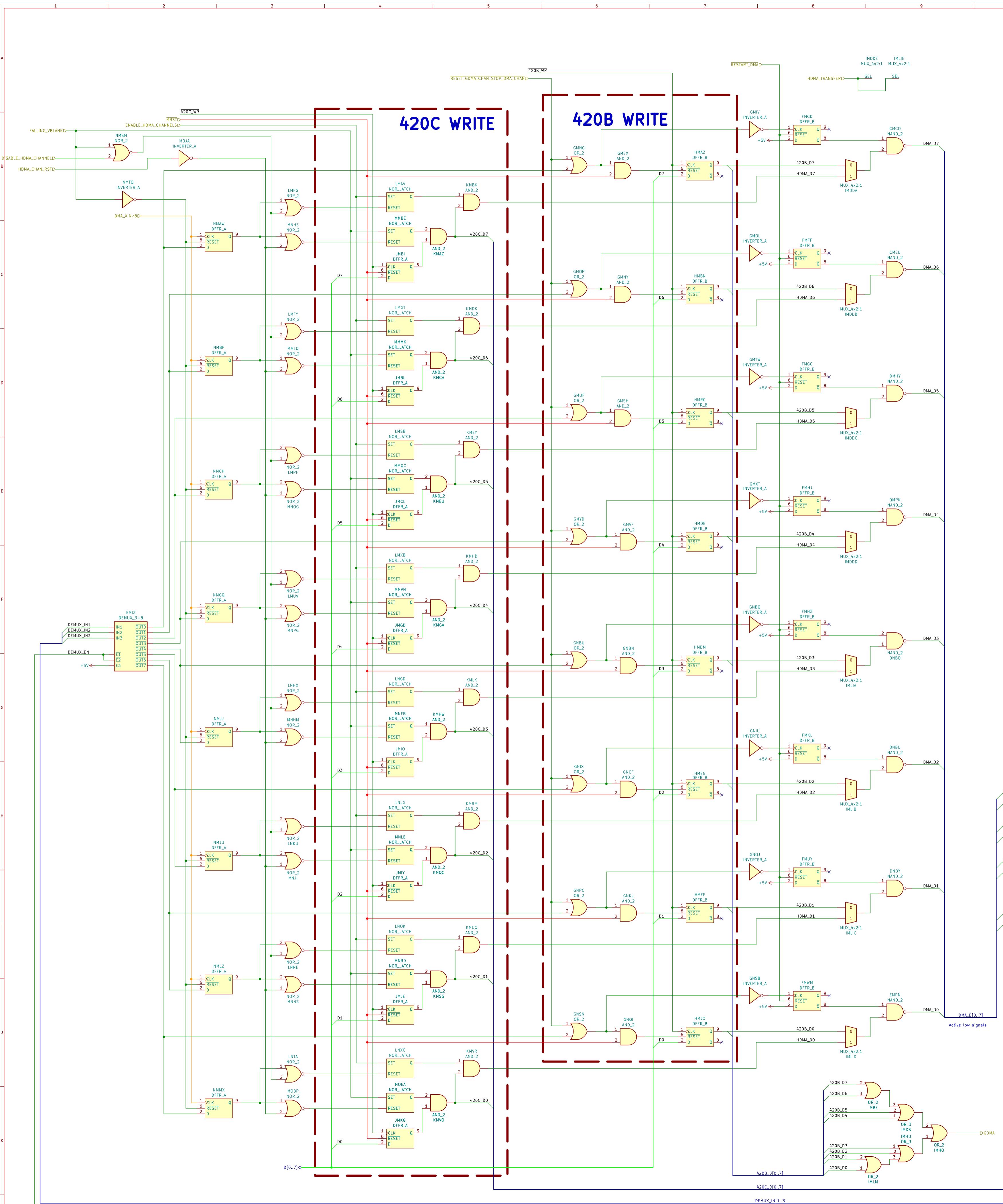
A-BUS

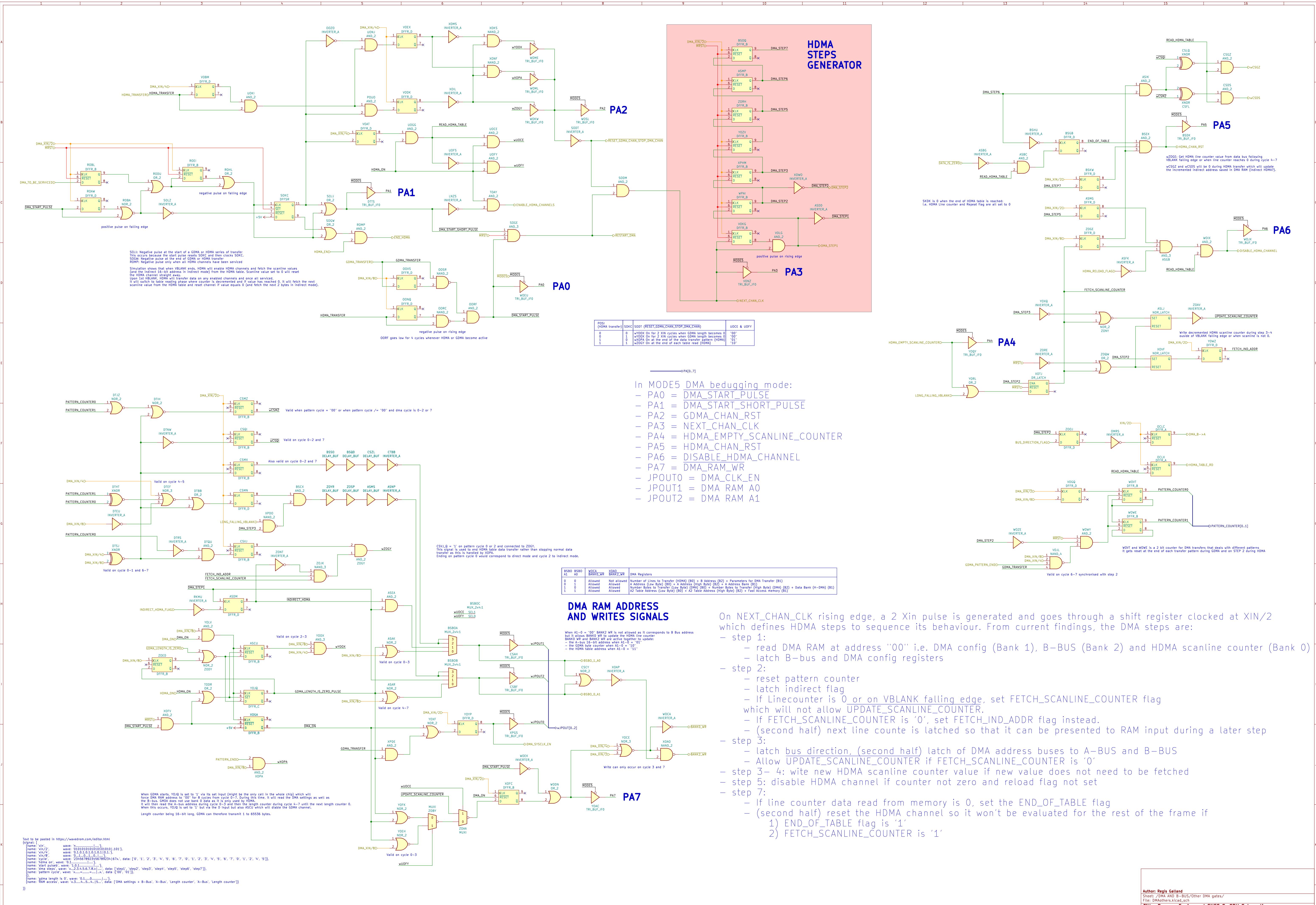
**4203 WRITE (MULTIPLIER) OR 4206 WRITE
OR SHL/SHR**

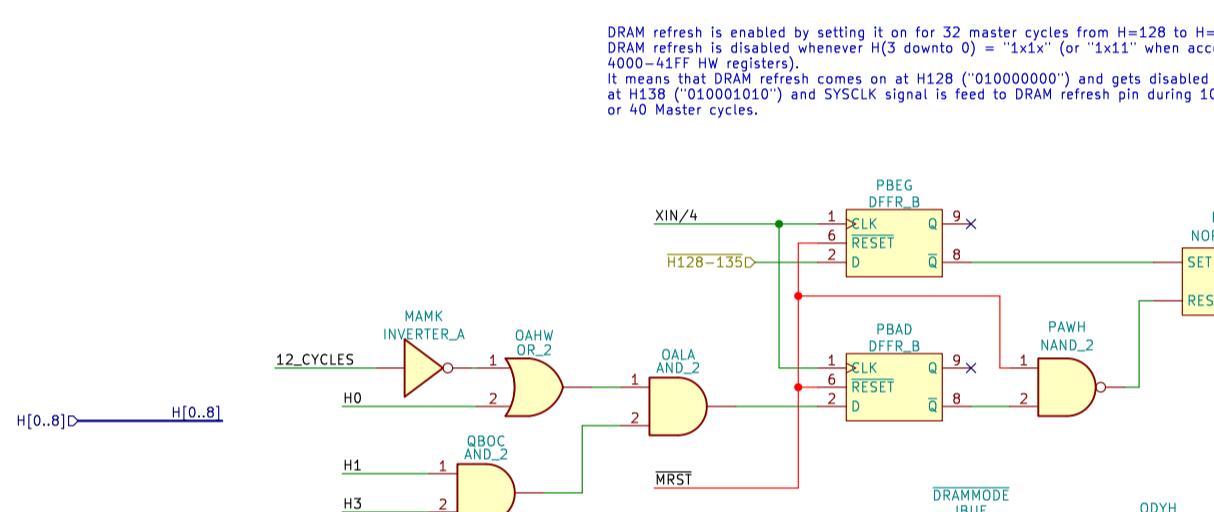
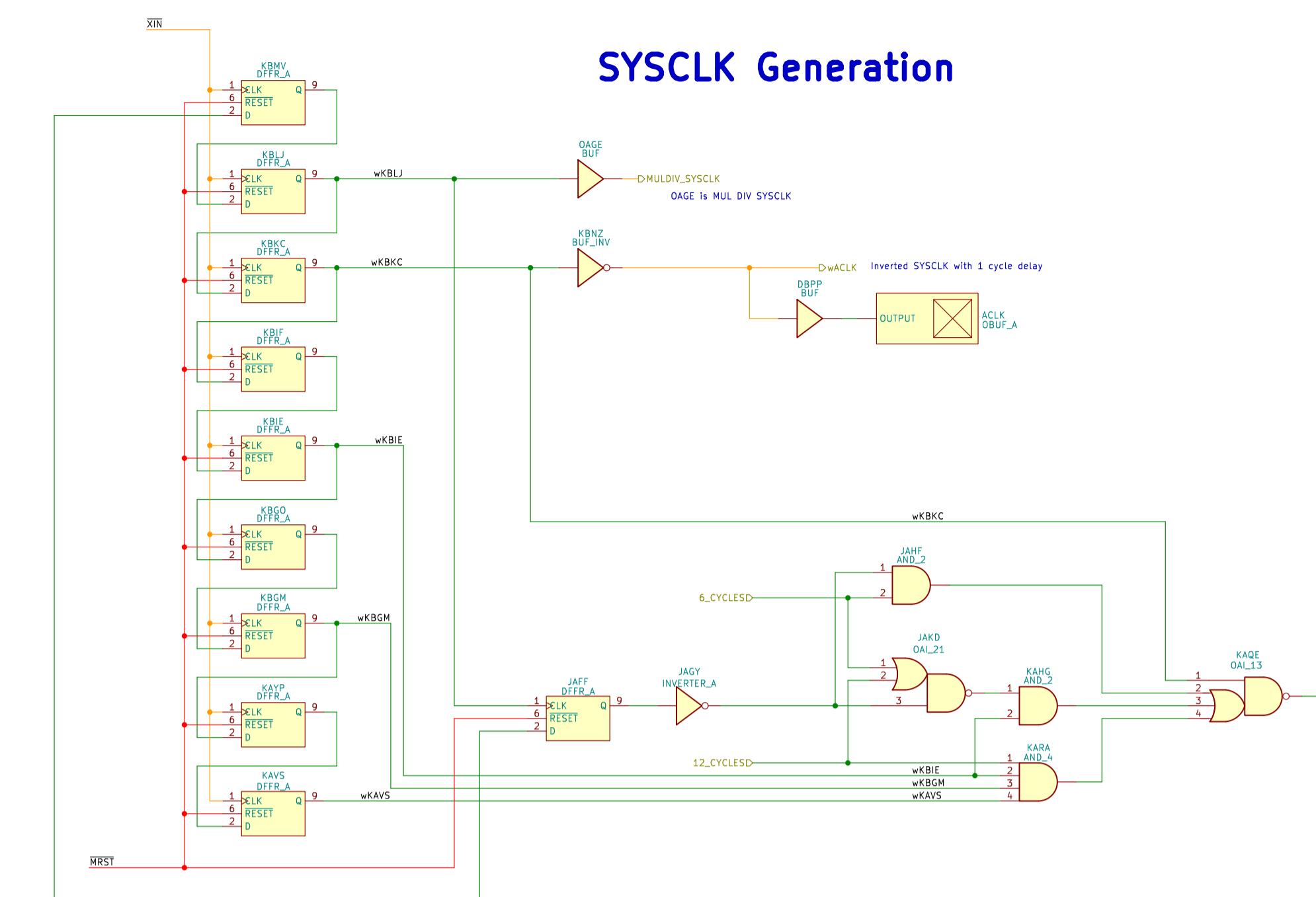




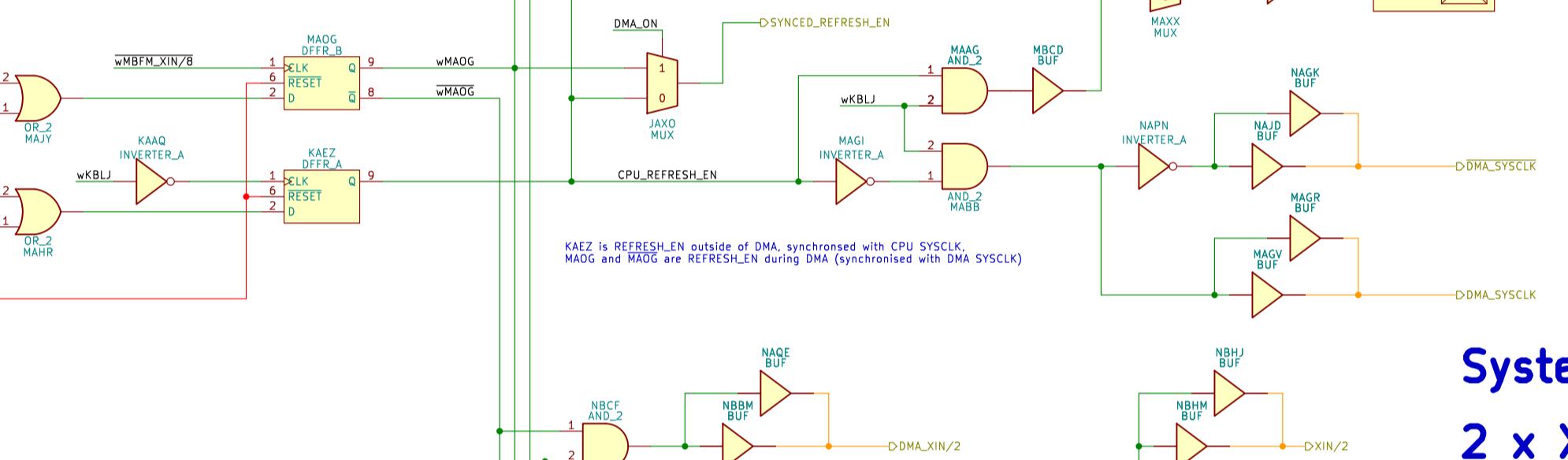




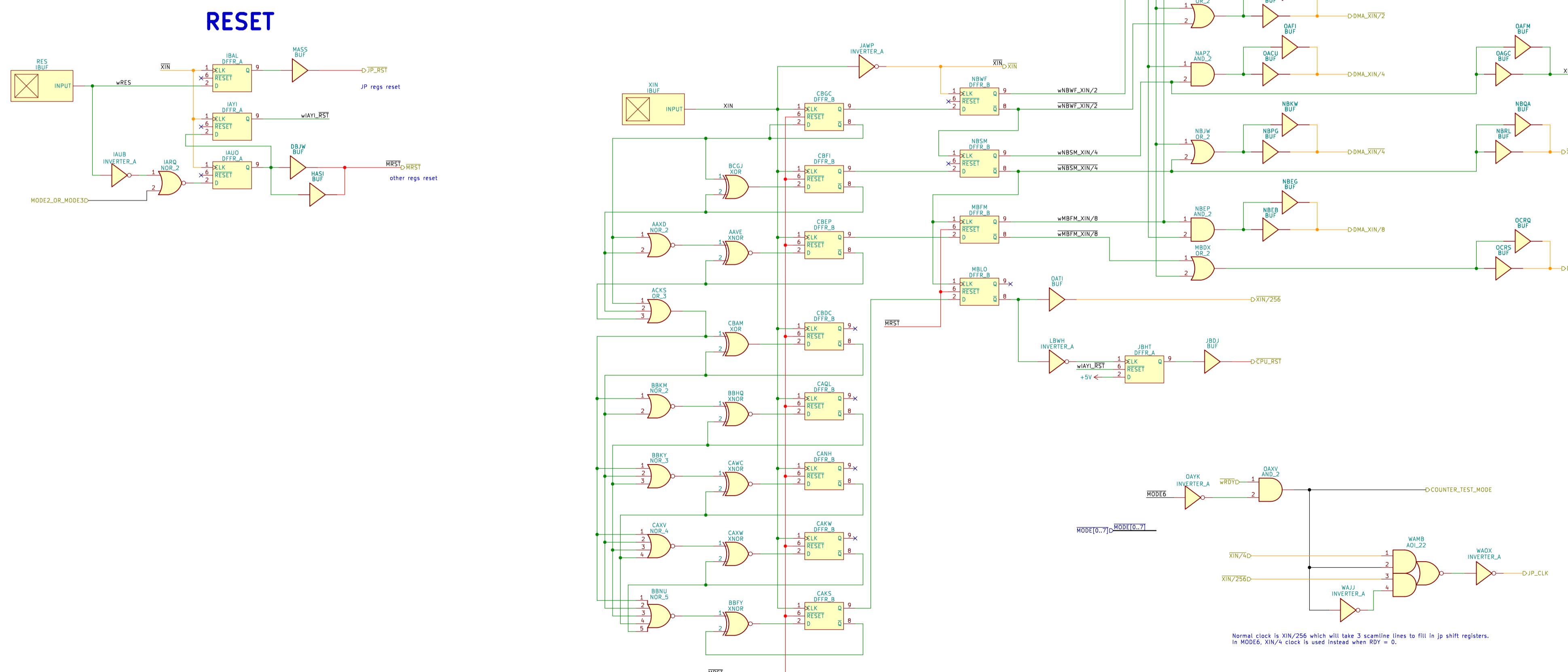




DRAM Refresh



SYSCLK and SYSCLK signals used in the DMA region



System clocks
 $2 \times XIN/2$

$1 \times XIN/2$

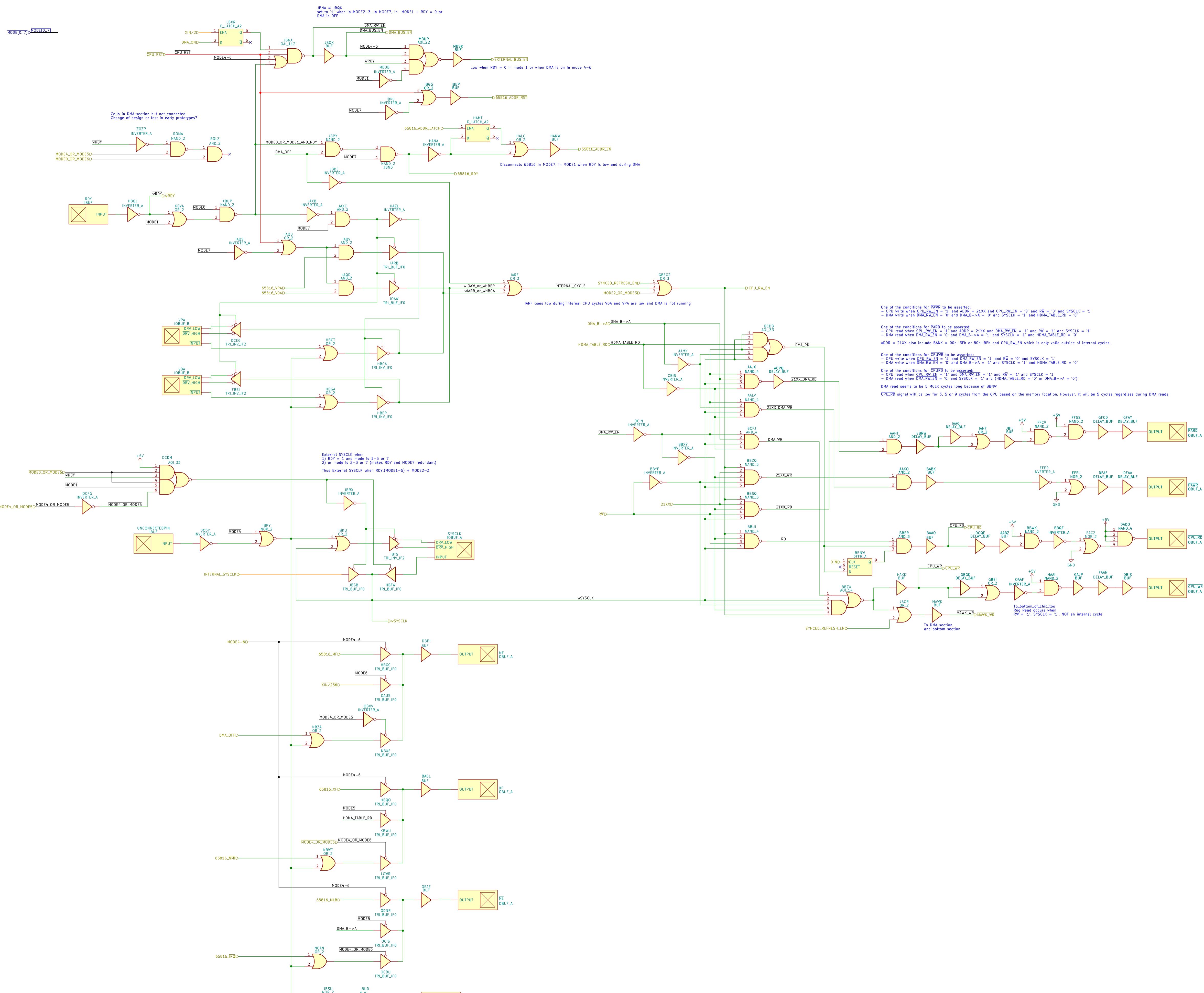
$2 \times XIN/4$

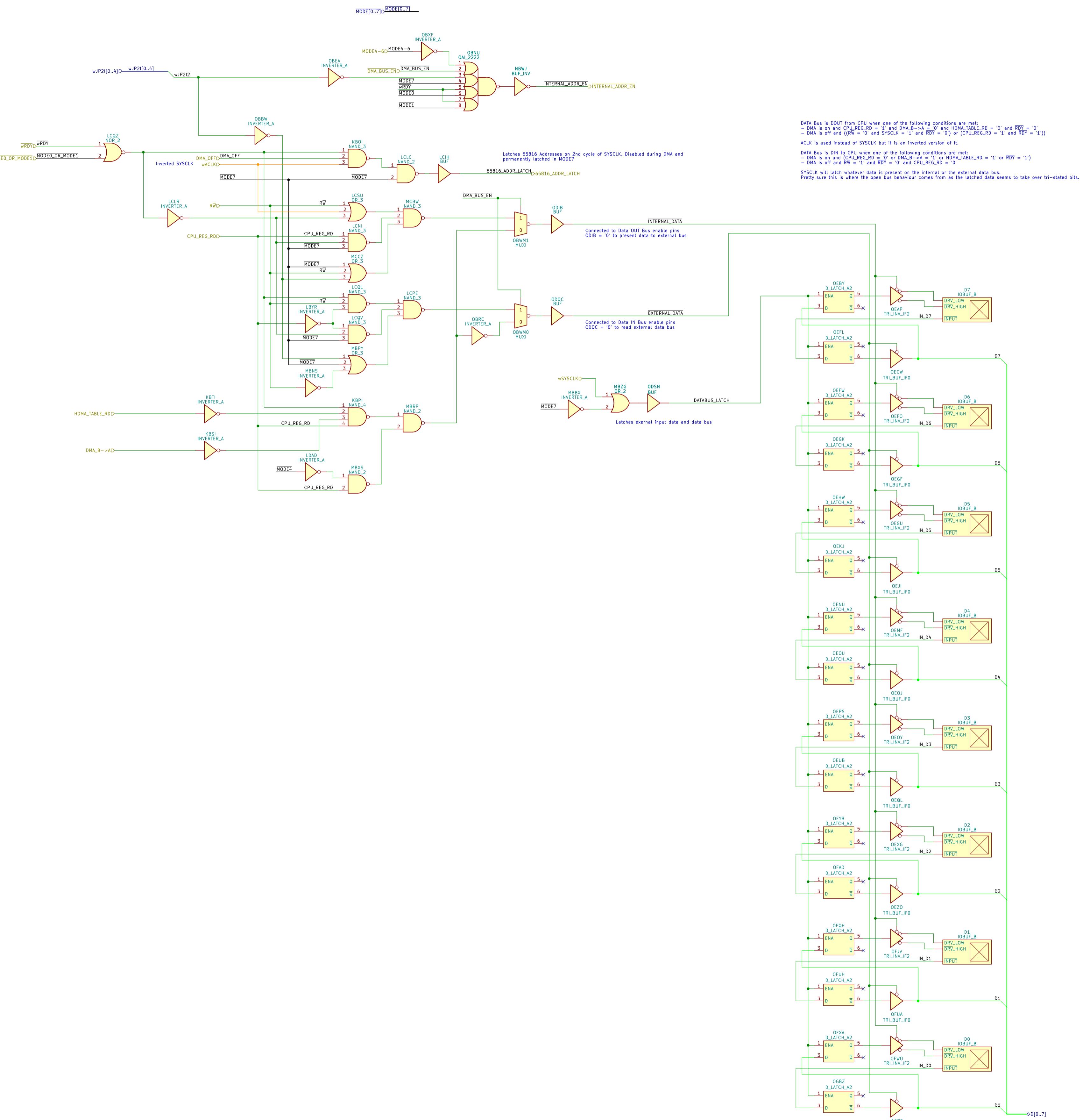
$2 \times XIN/4$

$1 \times XIN/8$

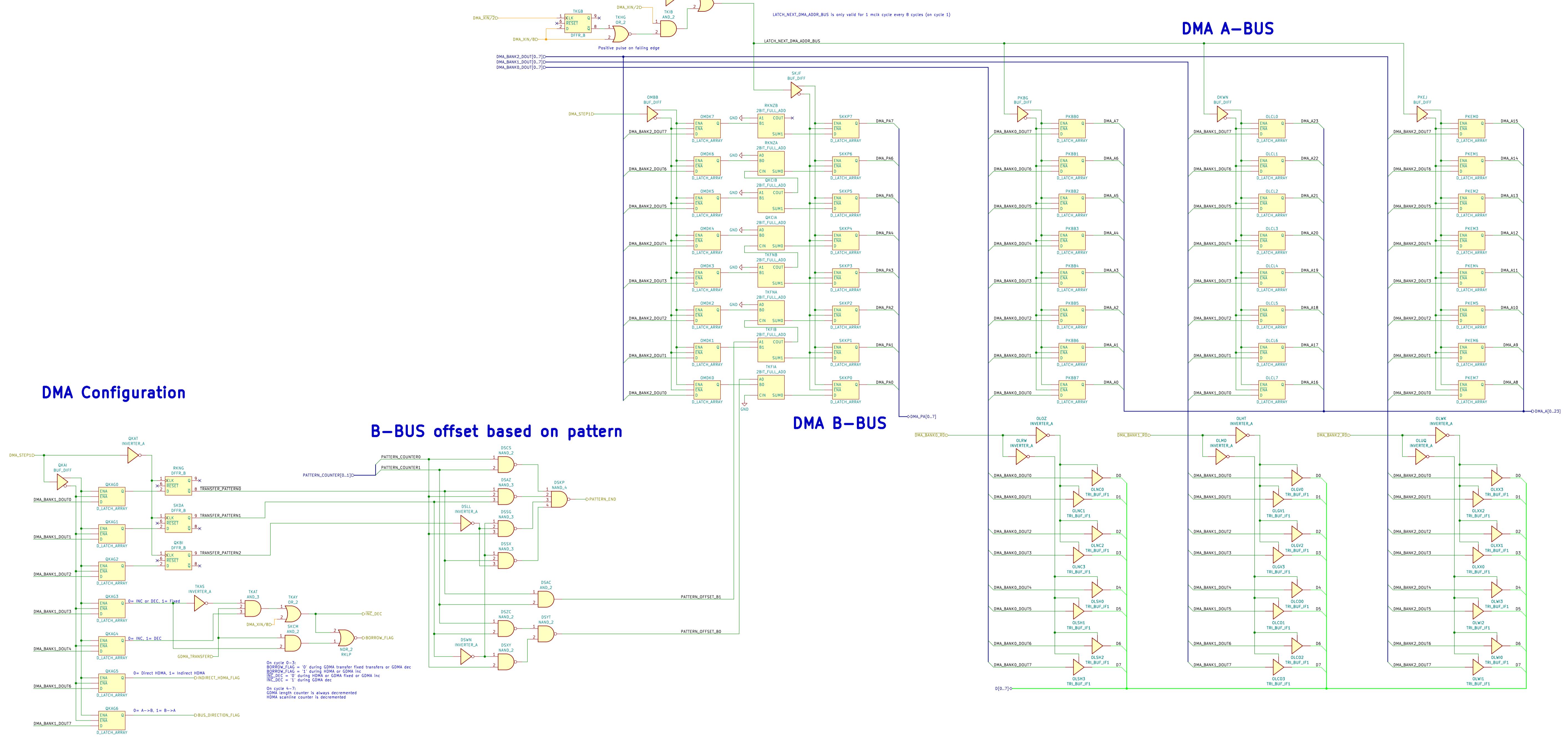
$1 \times XIN/8$

$1 \times XIN/256$

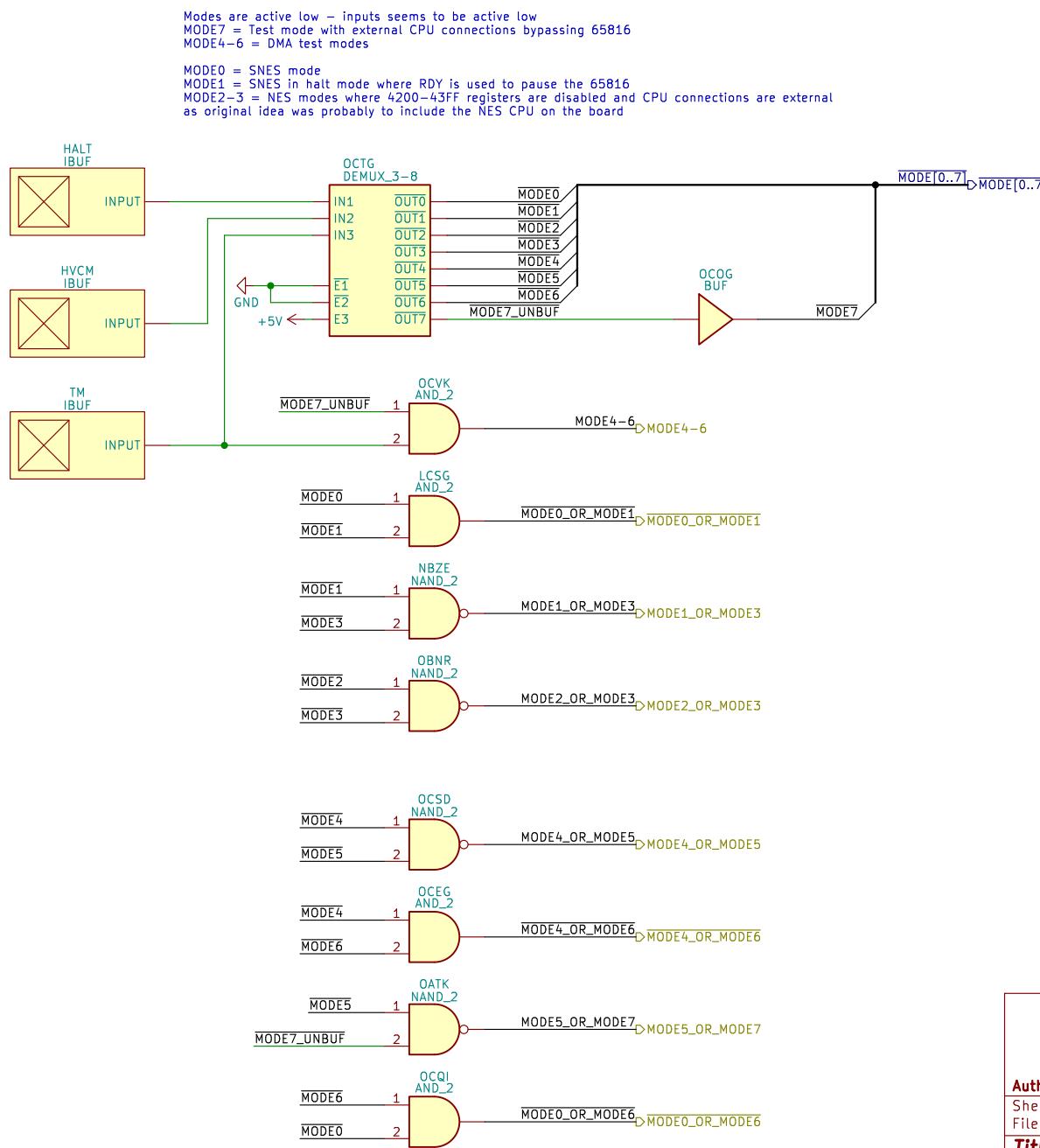




DMA Configuration



DMA A-BUS



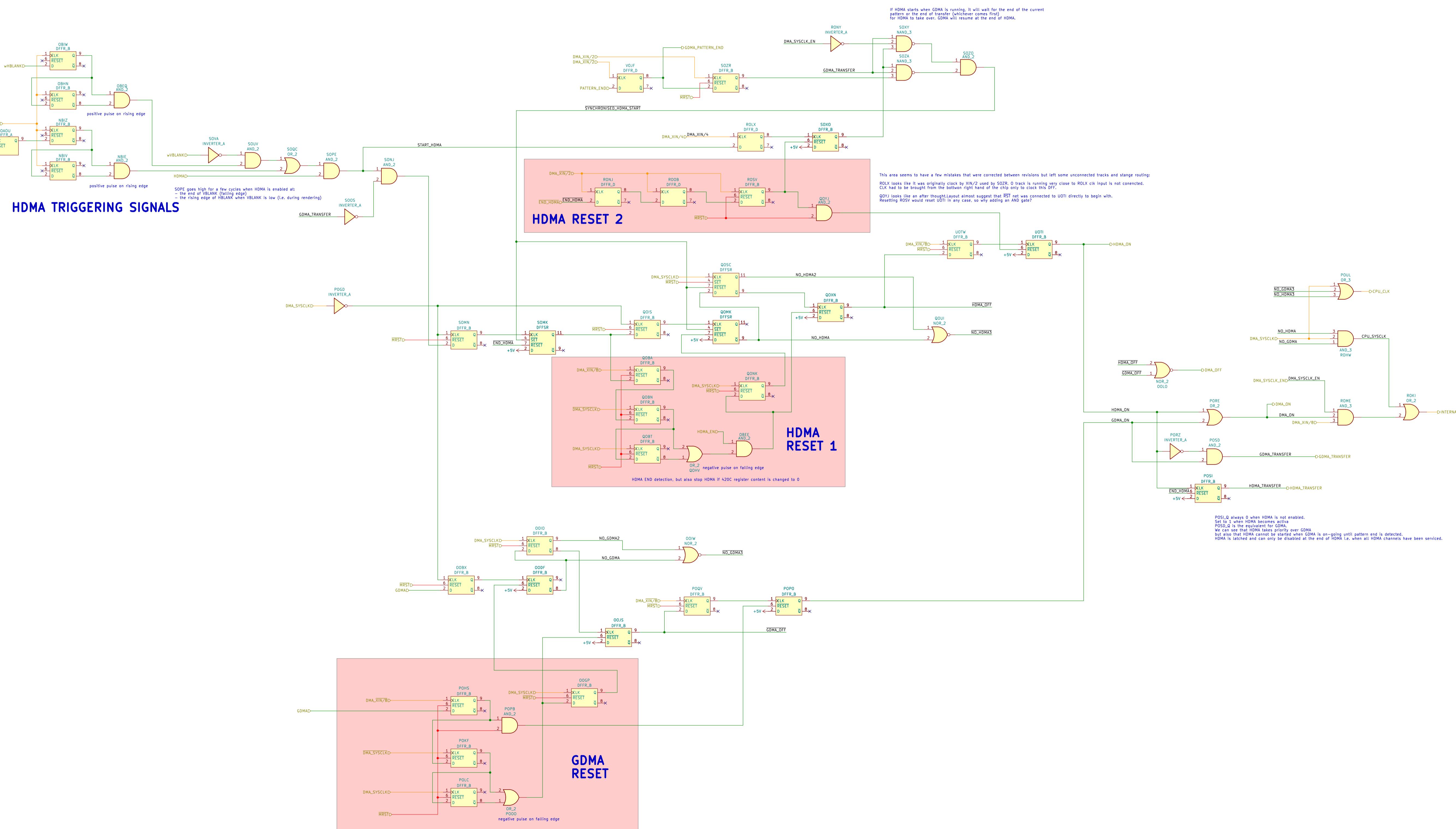
Author: Renis Galland

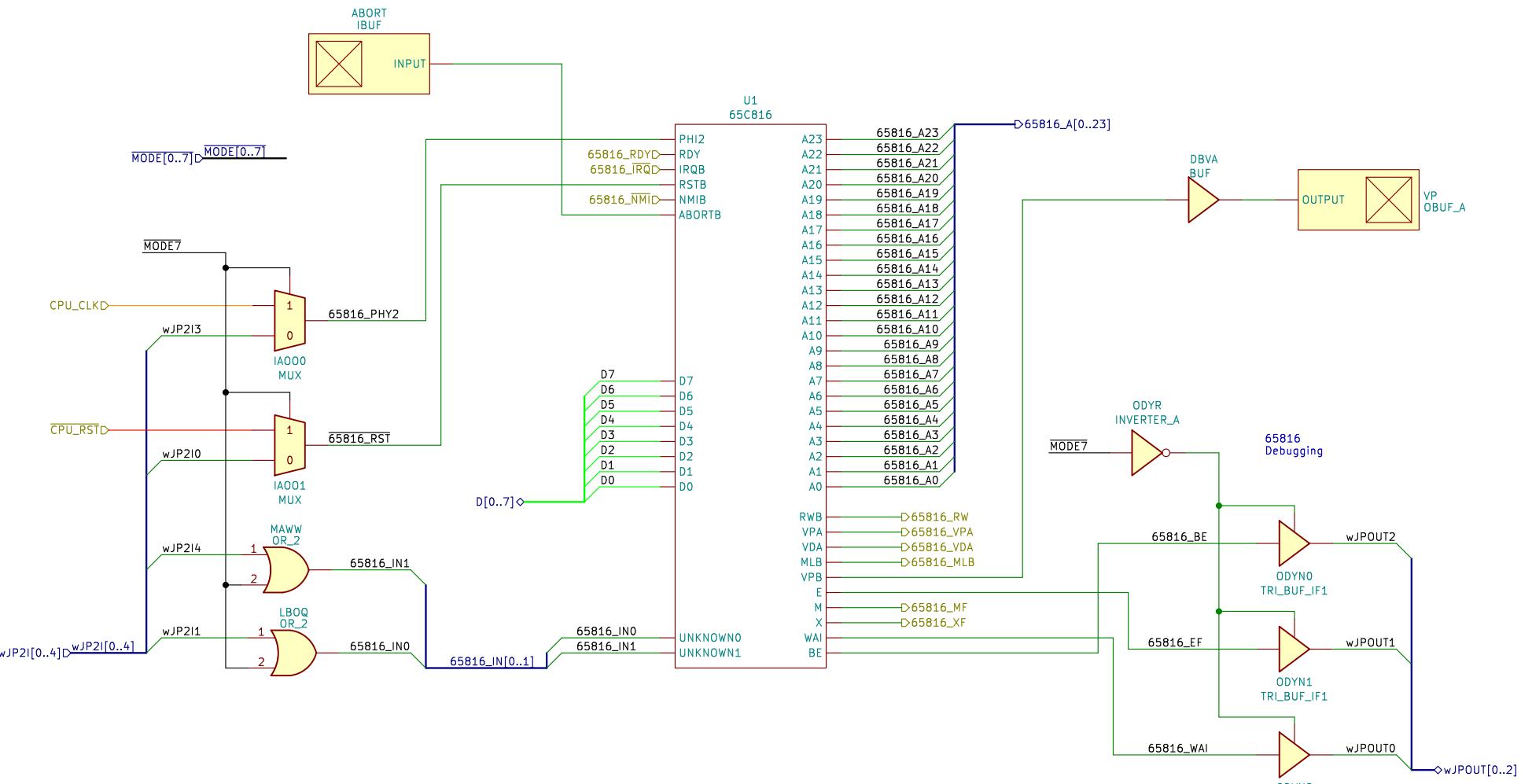
Sheet: /MODES/
File: modes.kicad_sch

Title: Reverse Engineered SNES S-CPU Schematics

Size: A4 Date: 2024-02-12
KiCad E.D.A. kicad 7.0.10-7.0.10~ubuntu22.04.1

Rev: 0.1
Id: 14/20





There 3 outputs which I guess must be:
 - Wait for interrupt output (multiplexed with RDY pin in W65C816 chip)
 - Emulation flag
 - Bus Enable (not needed as full 24-address bus is presented at all times)

Author: Regis Galland

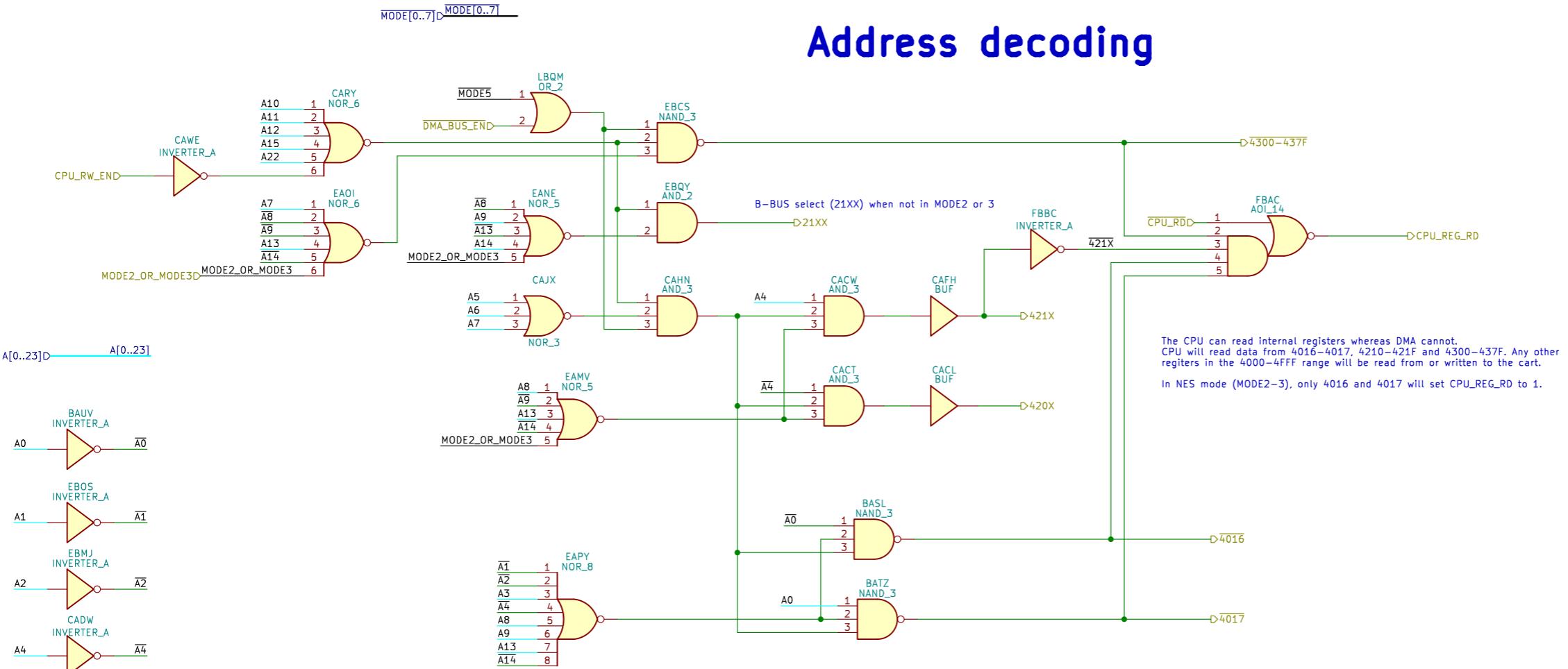
Sheet: /65C816 CPU/
File: 65c816.kicad_sch

Title: Reverse Engineered SNES S-CPU Schematics

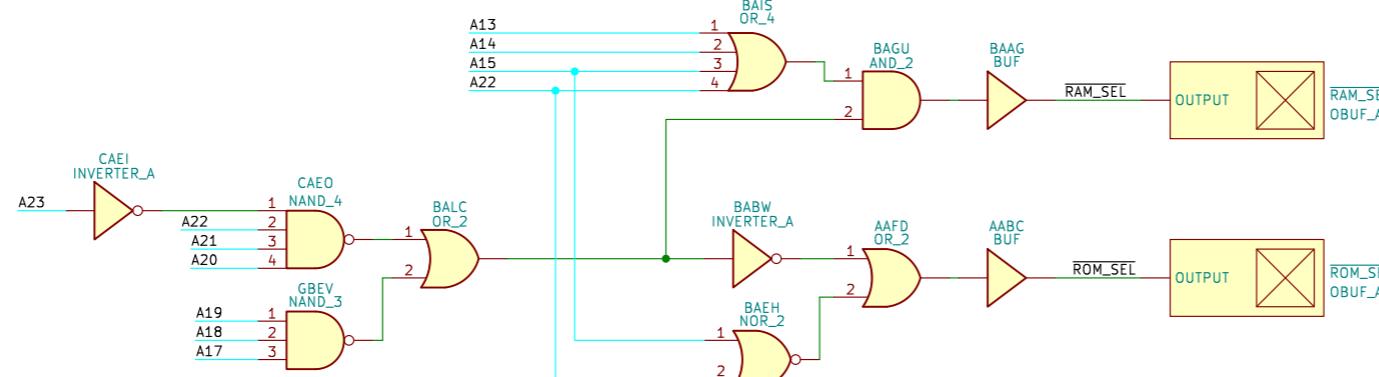
Size: A4 Date: 2024-02-12
KiCad E.D.A. kicad 7.0.10-7.0.10~ubuntu22.04.1

Rev: 0.1
Id: 17/20

Address decoding



RAM and RAM Selection



ROMSEL = $\overline{A23} \cdot A22 \cdot A21 \cdot A20 \cdot A19 \cdot A18 \cdot A17 + A22 \cdot A15$
Consistent with access to:
- 00-3F/80-BF:8000-FFFF or
- 40-70/C0-FF:0000-FFFF

RAMSEL = $\overline{(A23 \cdot A22 \cdot A21 \cdot A20 \cdot A19 \cdot A18 \cdot A17 + A22 \cdot A15 \cdot A14 \cdot A13)}$
Consistent with access to:
- 00-3F/80-BF:0000-1FFF or
- 7E-7F:0000-FFFF

Author: Regis Galland

Sheet: /ADDRESS REGION DECODING/
File: addrdecod.kicad_sch

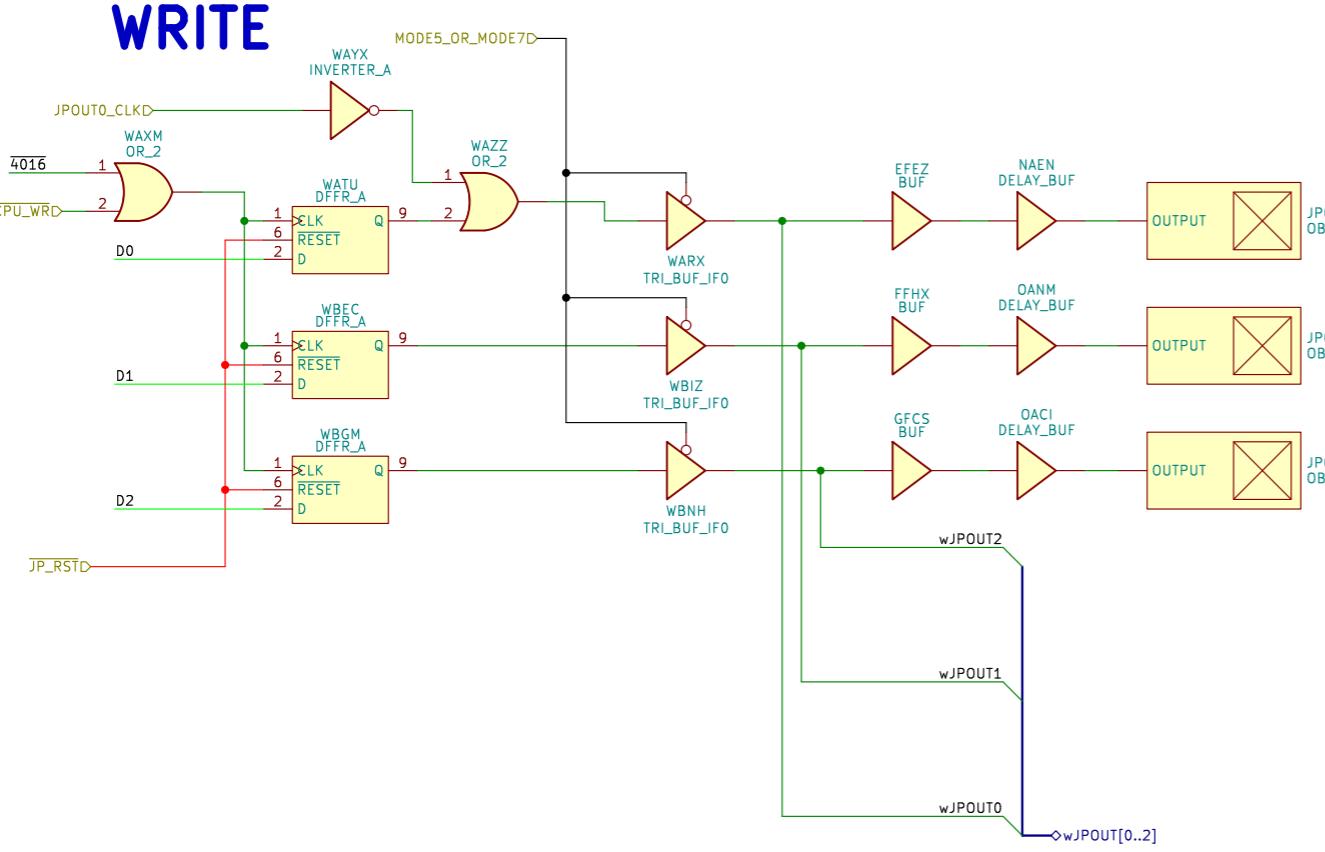
Title: Reverse Engineered SNES S-CPU Schematics

Size: A3 Date: 2024-02-12
KiCad E.D.A. kicad 7.0.10-7.0.10-ubuntu22.04.1

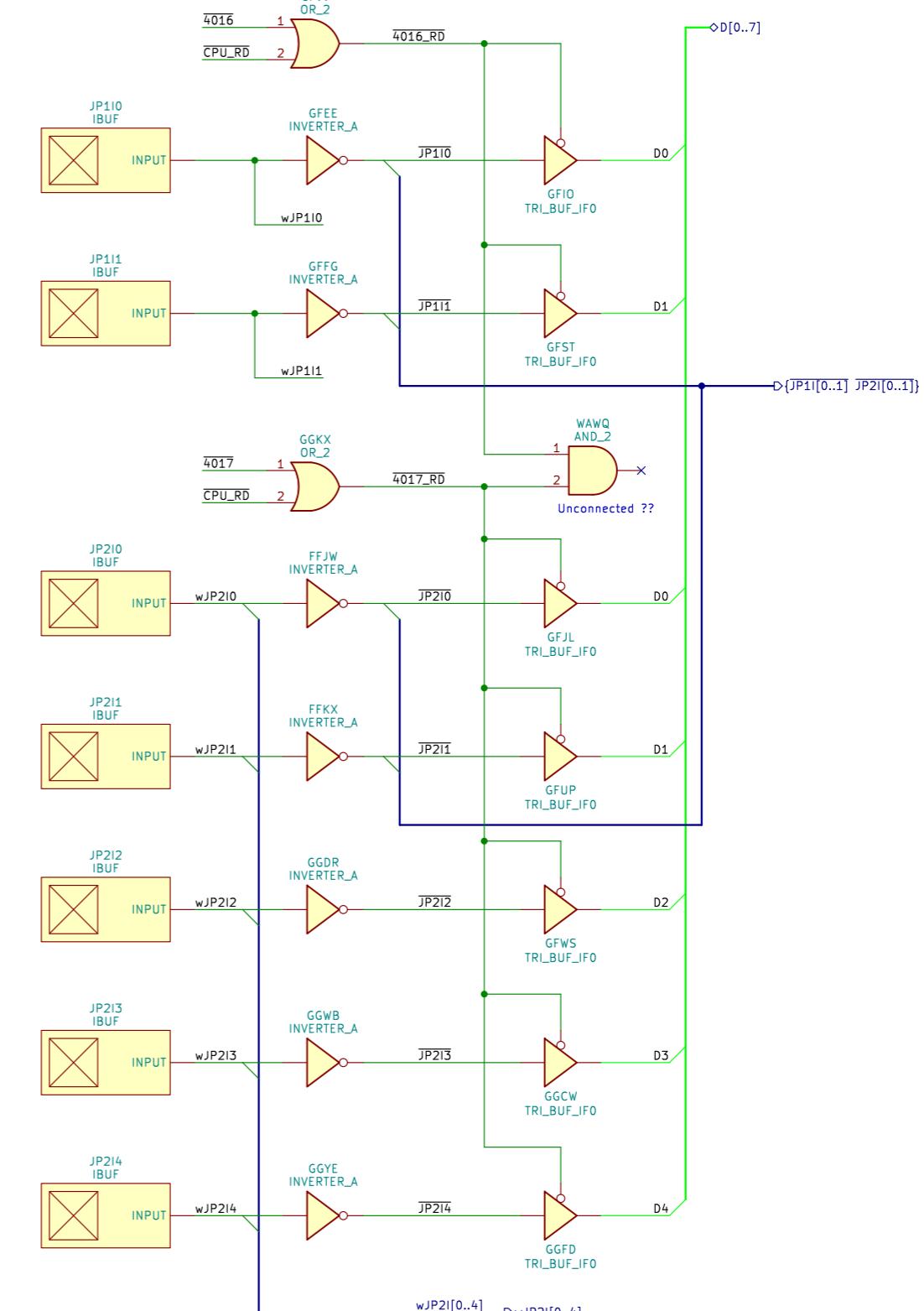
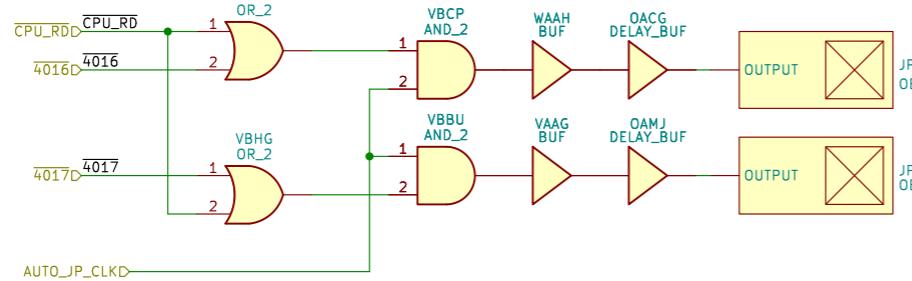
Rev: 0.1
Id: 18/20

4016/4017 READ

4016 WRITE



JPCLK: 4016/4017 READ OR SNES AUTO JP

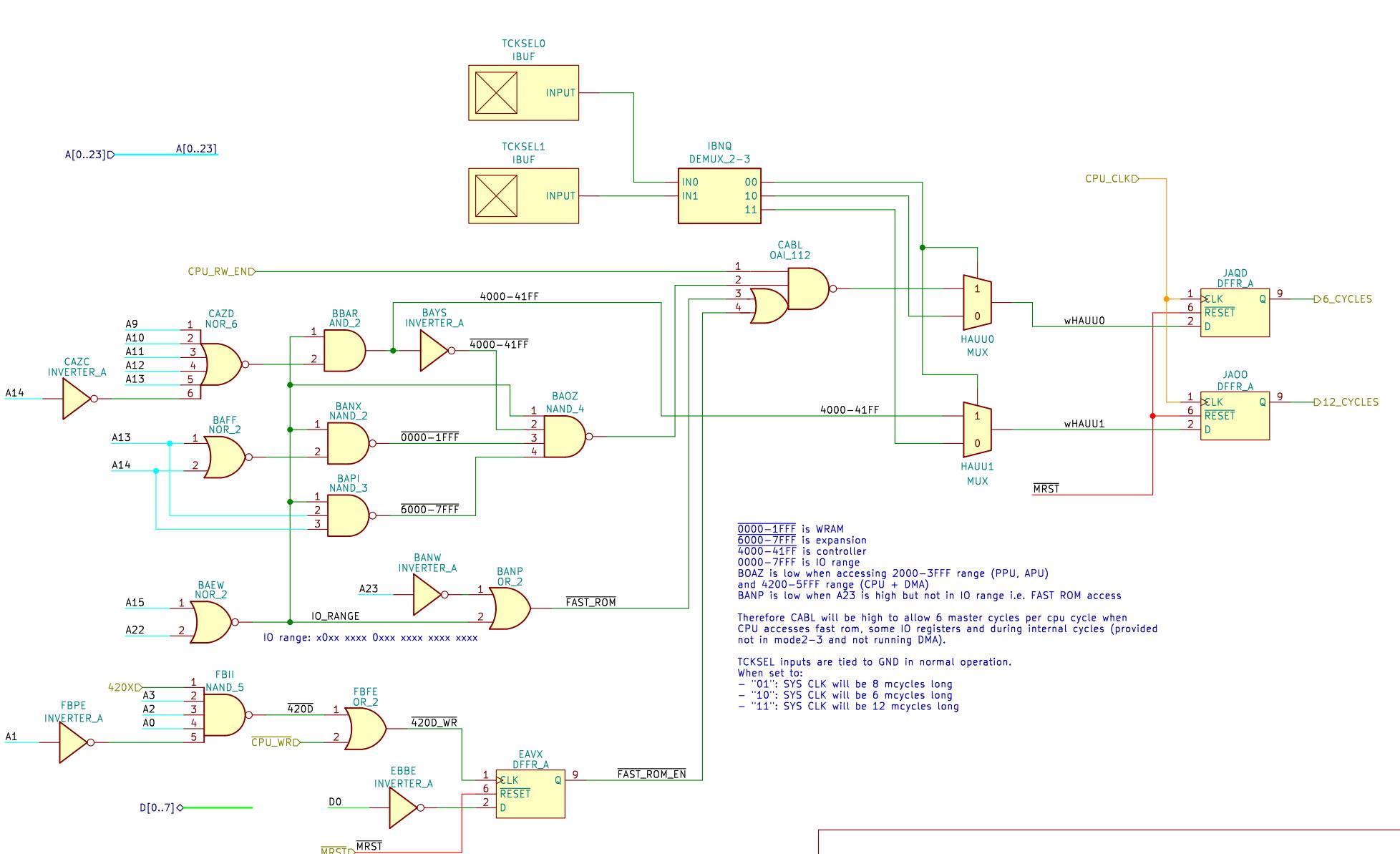


Author: Regis Galland
Sheet: /LEGACY JP REGISTERS/
File: legacyjpres.kicad_sch

Title: Reverse Engineered SNES S-CPU Schematics

Size: A3 Date: 2024-02-12
KiCad E.D.A. kicad 7.0.10-7.0.10-ubuntu22.04.1

Rev: 0.1
Id: 19/20



0000-1FFF is WRAM
6000-7FFF is expansion
4000-41FF is controller
0000-7FFF is IO range
BAOZ is low when accessing 2000-3FFF range (PPU, APU)
and 4200-5FFF range (CPU + DMA)
BANP is low when A23 is high but not in IO range i.e. FAST ROM access

Therefore CABL will be high to allow 6 master cycles per cpu cycle when CPU accesses fast rom, some IO registers and during internal cycles (provided not in mode2-3 and not running DMA).

TCKSEL inputs are tied to GND in normal operation.

When set to:

- "01": SYS CLK will be 8 mcycles long
- "10": SYS CLK will be 6 mcycles long
- "11": SYS CLK will be 12 mcycles long

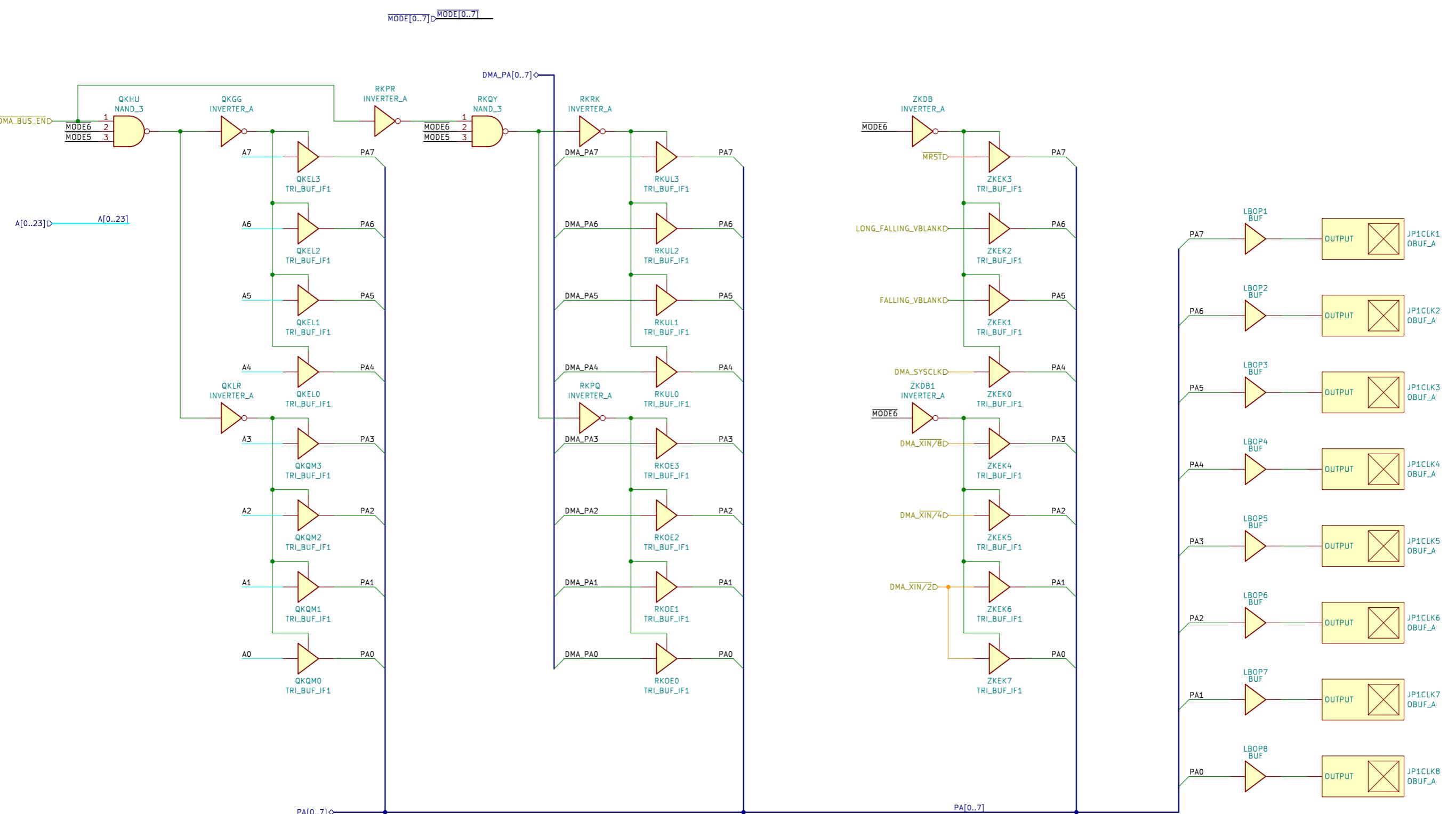
Author: Regis Galland

Sheet: /FAST ROM REG/
File: fastromreg.kicad_sch

Title: Reverse Engineered SNES S-CPU Schematics

Size: A4 Date: 2024-02-12
KiCad E.D.A. kicad 7.0.10-7.0.10~ubuntu22.04.1

Rev: 0.1
Id: 20/20



B-BUS and debug mode signals

Author: Regis Galland
Sheet: /DMA AND B-BUS/B-BUS/
File: bbus.kicad_sch

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Size: A3 Date: 2024-02-12
KiCad E.D.A. kicad 7.0.10-7.0.10-ubuntu22.04.1

Rev: 0.1 Id: 21/20