

R1, R2, 0R. C2, C3 N.M. for the first step


To daughter board (dfs_c096v01a)

JTAG

Version WLCSP 42 pins

REVISION HISTORY

V1.0 Initial Design



ON Semiconductor®

ON Semiconductor Switzerland SA

Champs-Montants 12a

CH-2074 Marin, Switzerland

Montana SV3

TITLE SCHEMATIC

top

SIZE	TITLE PROJECT	REV
A3	dfs_c101v01a	1.0

AUTHOR	DATE	SHEET
NLi	31/10/2019:06:44	1 of 1