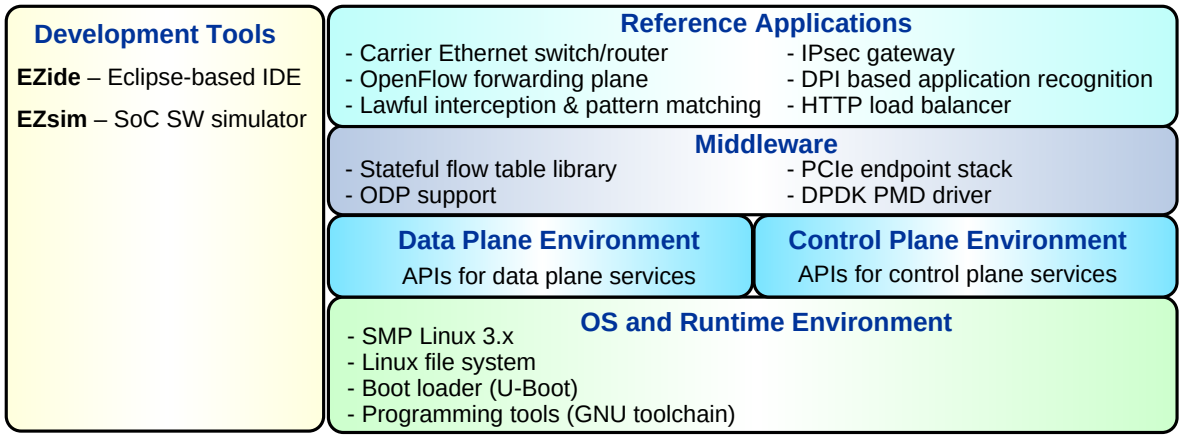
NPS Software Libraries

Product Brief

EZchip offers a rich set of NPS software middleware and reference applications for use in conjunction with the SoC. The NPS is EZchip's family of network processors for smart networks.

Software Development Kit for NPS



Middleware

The items in this category are reusable building blocks, modules or stacks that build on the basic data and control plane API to provide optimized higher level functionality to facilitate the fast and simple creation of applications.

Stateful Flow Library

The stateful flow table (SFT) provides bi-directional stateful flow awareness at wire speed in a client agnostic implementation.

- Six tuple bi-directional flow classification.
- L4 state machine.
- Multiple contexts (e.g. user and session awareness) provided through a single HW accelerated lookup.
- Supports IPv4 (including defragmentation) and IPv6.
- Out of Order and fragmentation support.
- Flow based fast path APIs
- Optimized to parallel execution so that clients need not use locking in flow based stateful business logic.
- Scales to millions of concurrent sessions. Number of sessions only limited by amount of RAM.

Among the clients using the SFT are the DPI based Application Recognition, Lawful Interception and HTTP Load Balancer solutions (see flip side).

ODP Support

OpenDataPlane (ODP) is a cross-platform open-source initiative. EZchip is a contributing member of ODP driving the SDK definition to support hardware accelerated high end NPUs.

- Full support of ODP APIs
- Hardware accelerated support of key functionalities such as QOS and Crypto.

PCIe Endpoint Stack

The PCIe Endpoint Stack provides a framework for efficient communication of the NPS data plane with host-based control or data plane applications over the PCIe interface.

- Support for generic software data and frame data transport.
- Support for software defined flexible DMA buffer structure for any application.
- Support for software defined flexible configuration space for any application.
- Supports multiple controllers, physical functions and SR-IOV virtual functions.
- Supports a flexible number of queues per application, instances and more.
- Linux® network device driver included.
- DPDK network device driver included.

DPDK PMD Driver

The virtual Ethernet port switch/aggregator builds upon the PCIe Endpoint Stack to implement a fully featured PCIe smart NIC engine.

- Provides up to 128 zero copy virtual NICs using PCIe SR-IOV virtual.
- Supports Linux virtual machines and Xen, KVM, Qemu and any VFIO compatible hypervisor.
- May easily be extended to support additional OS and hypervisors.
- Supports QinQ, VxLAN and NVGRE network overlays.
- Designed with high-scale OpenVSwitch acceleration at the NIC level in mind.
- Scales to 200 Gbps network traffic overall.

Reference Applications

Carrier Ethernet Switch/Router

The CESR reference application is a full featured carrier Ethernet switch router implemented using the NPS data plane APIs.

- Performs L2 switching and L3 forwarding.
- Recognizes IEEE 802.1Q VLAN, IEEE 802.1ad QinQ and MPLS tagging.
- Implements Ethernet OAM and IEEE1588v2 Synchronous Ethernet timers.
- Supports IEEE 802.3ad Link Aggregation Groups.
- Incorporates flexible multi-stage frame classification and access control lists.
- Features class of service based traffic shaping.
- Provides performance monitoring, statistics and port mirroring services.
- Scales up to millions of subscribers, 400 Gbps network traffic and 600 Mpps at 64-byte packet size.

OpenFlow Forwarding Plane

The OpenFlow Forwarding Plane reference application provides an OpenFlow forwarding plane.

- Compliant to OpenFlow™ 1.3 specification.
- Based on the open source OpenFlow reference implementation.
- Supports multiple tables and groups.
- Supports MPLS and VLAN tagging.
- Supports virtual ports.
- Supports per-flow meters.

Lawful Interception and Pattern Matching

The Lawful Interception and Pattern Matching reference application provides hardware-accelerated, flow-based, cross-packet, Bloom filter-based pattern matching. A PCRE compiler identifies key sub strings which are loaded into the Bloom filter. Suspected signatures are then inspected, and residual inspection is offloaded to a host.

- Hardware accelerated, optimized, Bloom-filter pattern matching.
- PCRE compiler.
- Flow based, stateful, cross packet inspection.
- Solution built to be extended through the use of an external DPI engine.
- The application scales to millions of concurrent TCP connections for total of 400 Gbps network traffic.

IPsec Gateway

The IPsec Gateway reference application provides a fully featured IPsec data plane based on the security API which is able to terminate both transport and tunnel IPsec sessions.

- Supports IPsec-v2 and IPsec-v3.
- Supports manual keying and/or ISAKMP (IKE control plane not included).
- Implements Encapsulating Security Payload (ESP) and Authentication Header (AH).
- Includes optimized anti-replay architecture.
- Supports Tunnel mode.
- Allows use of the encryption and authentication algorithms supported by NPS cryptography acceleration hardware.
- Supports Extended Sequence Numbers (ESN).
- Supports performance and scalability ranging from a single session to up to millions of sessions with aggregated performance of 200 Gbps.

DPI based Application Recognition

The DPI based Application Recognition application provides up to 800 Gbps application recognition. A DPI engine is loaded with up to 1500 compiled signatures. Packets are processed by the engine after they have been mapped to flows by the SFT. Application IDs for the classified flows are stored in the SFT. The DPI engine is bypassed for all packets belonging to classified flows.

- DPI engine optimized for massively parallel execution.
- Cross packet inspection and field extraction.

- DPI engine agnostic of loaded signatures.
- Stateful HTTP parser supporting metadata extraction.
- Scales to millions of flows with performance up to 800Gbps when integrated into a CESR router.

HTTP Load Balancer

The HTTP Load Balancer application provides a reference implementation for a layer 7, content-aware, HTTP load balancer. The application transparently intercepts HTTP requests to server IPs, answers as a proxy for the server, and based on the request of the client transparently redirects the connection to an available web server out of a pool to service it. The solution utilizes the SFT and DPI AR's HTTP parser as its infrastructure.

- Supports dynamic server pool selection based on requested URL and headers.
- Supports static (round robin) and dynamic (load based) server selection.
- Implements transparent TCP connection splicing for connecting client to server.
- Scales to millions of TCP connections, clients and servers at up to 400 Gbps of network traffic for any number of sessions.

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