Lab Synthesis – Group 2

a. Critical path:
   Slack (setup path): 6.957ns (requirement - (data path - clock path skew + uncertainty))
   Source: bicycle_fsm/beat_32/flipflop/q_20 (FF)
   Destination: bicycle_fsm/beat_32/flipflop/q_20 (FF)

In our logic, it comes from the bicycle_fsm module.

b. We consumed 201/53,200 of all slice LUTs in the FPGA, of which 194 are used as logic and 4 used as route-thrus. 68/13300 slices are occupied. Our implementation used 147 Slice registers (125 as flip flops and 22 as latches.)

c.