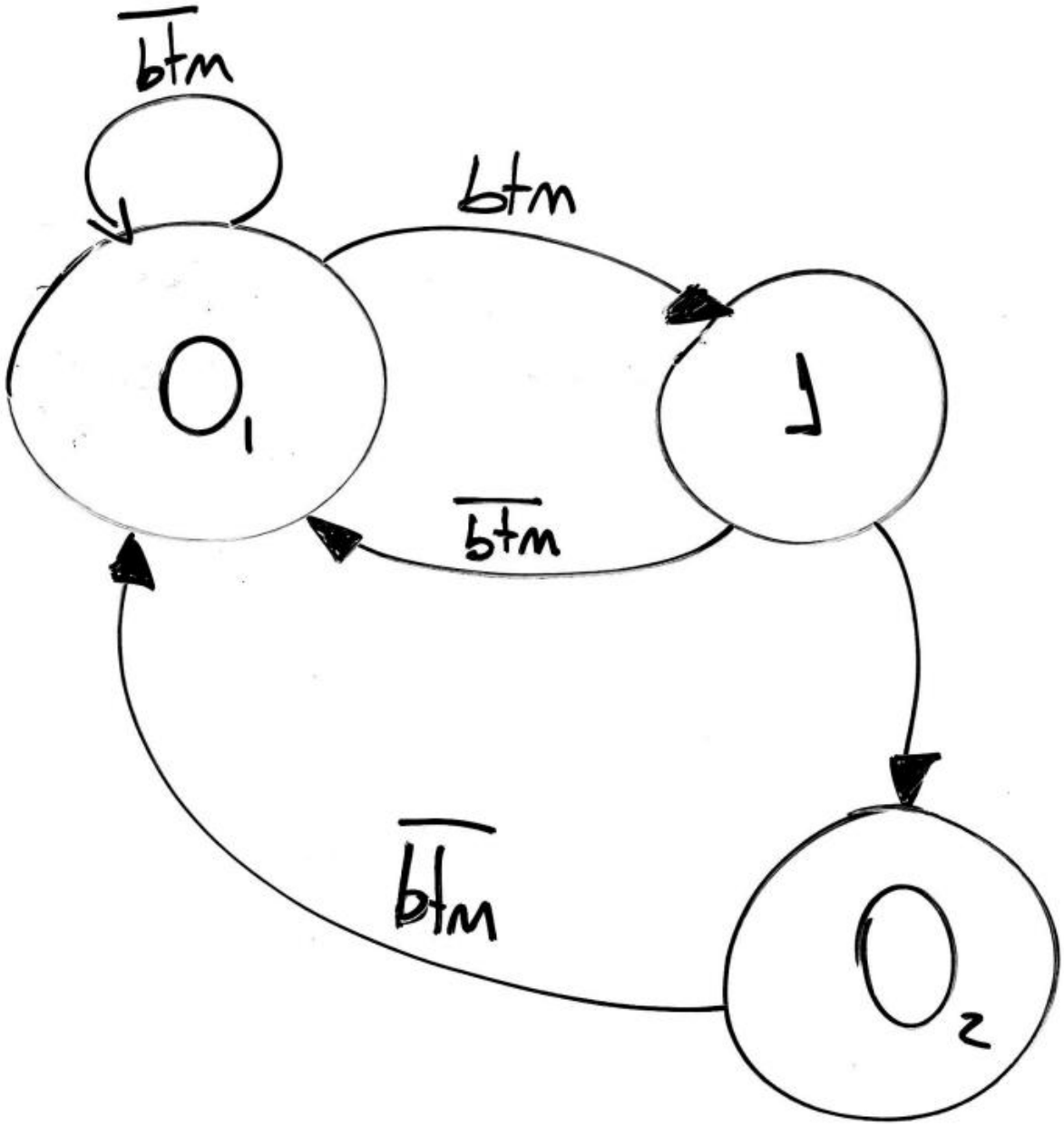
Lab Discussion – Group 2



a.

b. Assume some stray radiation hits the state bits of a one-hot encoded FSM and one of those bits is flipped such that either two state bits are high or zero state bits are high. What will happen to the design if it was written as a Verilog case statement with no default entry? What if there was a default entry?

If there is no default statement, a latch will be inferred. In case there is a default entry, that is the one that will be evaluated.