Lab Questions – Demo Session

Group 2: Kylee, Raul, Sam

1. Slice LUTs: 1553

Logic: 1509

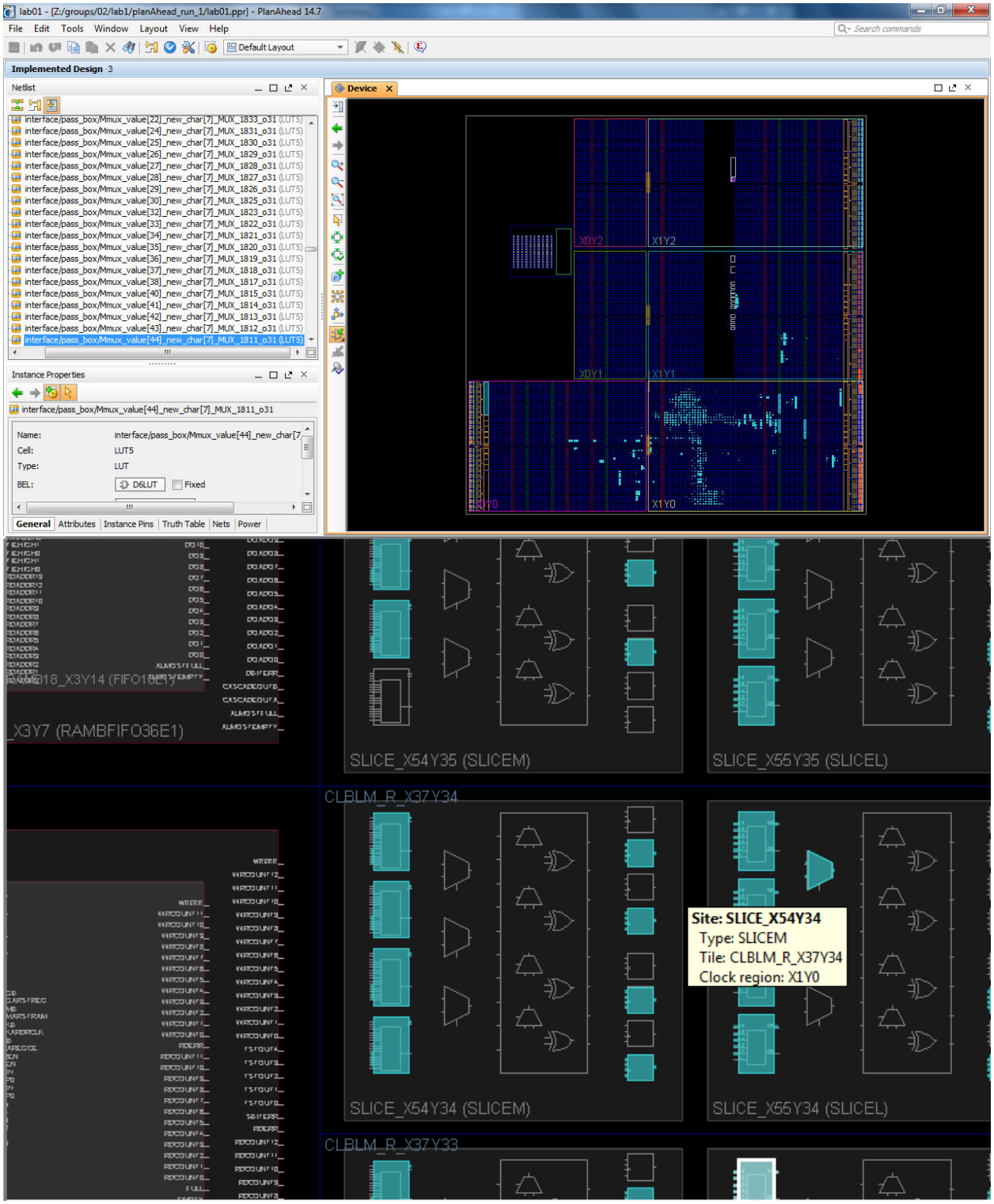
Route-through: 31

(Route through means an LUT that forwards a signal through it)

Number of occupied slices: 542

2. No latches!

3.



4. Synthesizable means that it can be implemented on the FPGA board. An example of an unsynthesizable piece of code is a delay #[number] or a loop because in hardware everything happens at once

5. A tiny bit less hand holding (we need practice designing circuits). We would prefer if lab files were due at the same time as the demo files. Trying to work with both deadlines is exhausting.