ICSS-G IEP PWM PRU FIRMWARE DESIGN GUIDE

IEP PWM PRU Firmware

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This document is intended for users interested the IEP PWM firmware design. It discusses details of the firmware design and implementation, and includes information concerning the memory maps, structures, state machines, and software flow of the firmware. Those users only concerned with using the firmware may not need to read this document.

The PWM firmware was developed on the AM654x EVM based on AM6548 SR1.0 silicon. There is no intent or commitment for updates to the firmware, and the firmware can be used for customer reference in their own development and maintenance.

Version	Date	Description of changes
0.1	04-13-19	Initial Draft
0.5	05-18-19	Added detailed descriptions of FW registers. Added FW register bit field type descriptions. Added FW register bit field default values. Added PWM_CTRL & PWM_STAT FW registers. Added details on configurability (Init, Post-Init) of PWM parameters. Added Initialization flow chart. Updated State Machine.
0.6	05-22-19	Added references & definitions. Added introduction & feature set. Added details on PWM Module behavior. Added PWM signal levels & action tables. Added details on Host & FW communication. Added State Machine flow charts. Added PRU memory requirements. Added EVM support to Test Plan section. Added FW source files.
0.7	08-19-19	Updated Duty Cycle count calculation in description of for IEPx_PWMm_DC_COUNT. Added FW version information. Add PWM_CTRL:PWM_EN & PWM_STAT:PWM_EN_ACK to allow Host reconfiguration of FW registers before FW initialization is started.
1.0	07-01-20	Editorial update to cover page and footer for publication

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 References

The following references are related to the feature described in this document and shall be consulted as necessary.

No	Referenced Document	Link
1	AM65x/DRA80xM Processors Technical Reference Manual (Rev. C)	http://www.ti.com/lit/pdf/spruid7

Table 1. Referenced Materials

2 Definitions

Acronym	Description
API	Application Programming Interface
BB	Breakout Board
CMPL	Complementary
DB	Deadband
DC	Duty Cycle
FW	Firmware
IEP	Industrial Ethernet Peripheral
LHS	Left Hand Side
NEG	Complementary PWM Negative Signal
POS	Complementary PWM Positive Signal
PRU_ICSSG	Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem – Gigabit
PWM	Pulse Width Modulation
RHS	Right Hand Side
SM	State Machine
SNGL	Single-Ended PWM
SPWM	“Sacrificial” PWM

Table 2. Definitions

3 Introduction

PWM signals have several uses, including:

- Dimming an LED
- Providing analog output; if the digital output is filtered, it will provide an analog voltage between 0% and 100%
- Generating audio signals
- Providing variable speed control for motors
- Generating a modulated signal, for example to drive an infrared LED for a remote control.

The PRU_ICSSG integrates one PWM module. The PWM module uses IEP0 and IEP1 compare events to generate PWM outputs. IEP0 and IEP1 each support 2 PWM sets of 3 phased motor

control PWM outputs with 6 primary (positive) and 6 complimentary (negative) programmable PWM outputs per set. Additional details of the PWM module are contained in [1].

The IEP PWM PRU firmware (FW) provides Host application/driver software access to the PRU_ICSSG PWM module. The FW implements a Host API which abstracts the PWM module hardware. This abstraction simplifies utilization of the PWM module by Host application/driver software since details of PWM hardware configuration and servicing are hidden by the Host API. Figure 1 shows the Host & FW design layers.

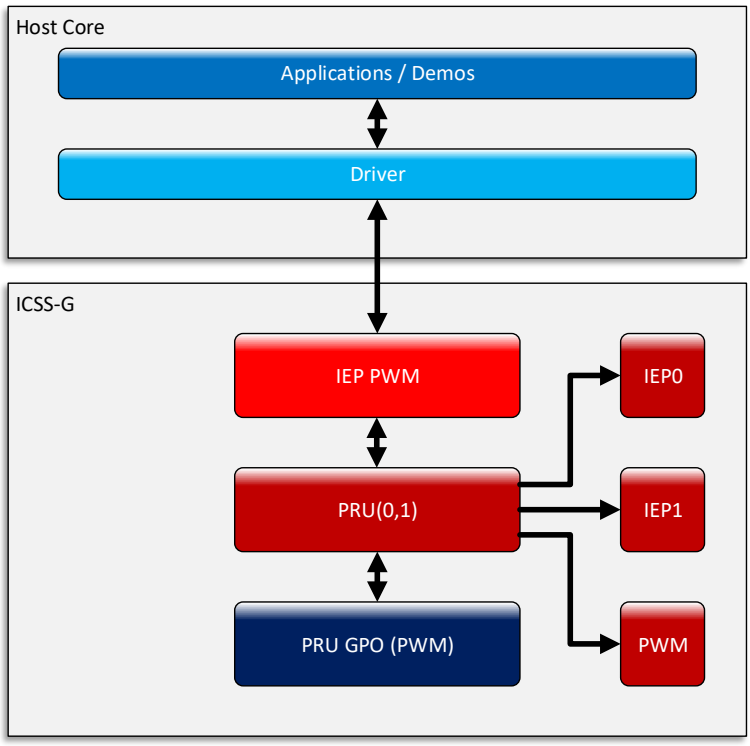


Figure 1. Host & Firmware Design Layers

4 Feature Set

The IEP PWM FW supplies the following configuration options:

- Mode for each POS/NEG signal pair, where each pair can be configured as 2 Single-Ended PWMs or 1 Complementary PWM.
- Disable/Enable for all Single-Ended and Complementary PWMs.
- PWM Period, tested up to 1 msec. (1 kHz PWM frequency).
- PWM Duty Cycle, tested up to 8-bit (256 level) resolution.
- PWM Dead Band time for Complementary PWMs.

PWM Mode can only be configured at FW initialization time, i.e. once set PWM Mode can only be reconfigured by re-downloading the FW to PRU_ICSSG PRU memories. All other PWM FW parameters (Disable/Enable, PWM period, etc.) can be dynamically reconfigured.

5 Design Description

5.1 Firmware Registers

5.1.1 Register Memory Map

The register memory map for the FW executing on a particular PRU is located in the data memory associated with the PRU, i.e. the map is located in DRAM0 for PRU0 and DRAM1 for PRU1.

Memory offset	Size (Bytes)	Register name	Description
0x00000000	4	Firmware Magic Number	Magic number for ICSSG PWM PRU firmware
0x00000004	4	Firmware Type	Firmware type information
0x00000008	4	Firmware Version	Firmware version information
0x0000000C	4	Firmware Feature	Firmware feature information
0x00000010	4	Firmware Extended Feature	Firmware extended feature information
0x00000014	4	PWM_CTRL	PWM Control
0x00000018	4	PWM_STAT	PWM Status
0x0000001C	4	IEP0_PWM_RECFG	IEP0 PWM Reconfiguration. Flags for controlling which PWM parameters are reconfigured. • Host writes '1' to request update of associated parameter. • Firmware clears flag to '0' to inform Host update of parameter is complete.
0x00000020	4	IEP0_PWM_MODE	IEP0 PWM Mode. Flags for selecting PWM mode (Single-Ended or Complementary).
0x00000024	4	IEP0_PWM_EN	IEP0 PWM Enable. Flags for enabling / disabling PWMs.
0x00000028	4	IEP0_PWM_PRD_COUNT	IEP0 PWM Period Count. IEP counter value necessary for desired PWM frequency.
0x0000002C	4	IEP0_PWM0_DC_COUNT	IEP0 PWM0 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000030	4	IEP0_PWM1_DC_COUNT	IEP0 PWM1 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000034	4	IEP0_PWM2_DC_COUNT	IEP0 PWM2 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000038	4	IEP0_PWM3_DC COUNT	IEP0 PWM3 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x0000003C	4	IEP0_PWM4_DC COUNT	IEP0 PWM4 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000040	4	IEP0_PWM5_DC COUNT	IEP0 PWM5 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000044	4	IEP0_PWM6_DC COUNT	IEP0 PWM6 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000048	4	IEP0_PWM7_DC COUNT	IEP0 PWM7 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x0000004C	4	IEP0_PWM8_DC COUNT	IEP0 PWM8 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000050	4	IEP0_PWM9_DC COUNT	IEP0 PWM9 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000054	4	IEP0_PWM10_DC COUNT	IEP0 PWM10 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000058	4	IEP0_PWM11_DC COUNT	IEP0 PWM11 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x0000005C	2	IEP0_PWM0_1_DEADBAND	IEP0 PWM0 & 1 Dead Band Count. IEP counter value necessary for desired complementary mode dead band.
0x0000005E	2	IEP0_PWM2_3_DEADBAND	IEP0 PWM2 & 3 Dead Band Count. IEP counter value necessary for desired complementary mode dead band.
0x00000060	2	IEP0_PWM4_5_DEADBAND	IEP0 PWM4 & 5 Dead Band Count. IEP counter value necessary for desired complementary mode dead band.
0x00000062	2	IEP0_PWM6_7_DEADBAND	IEP0 PWM6 & 7 Dead Band Count. IEP counter value necessary for desired complementary mode dead band.
0x00000064	2	IEP0_PWM8_9_DEADBAND	IEP0 PWM8 & 9 Dead Band Count. IEP counter value necessary for desired complementary mode dead band.
0x00000066	2	IEP0_PWM10_11_DEADBAND	IEP0 PWM10 & 11 Dead Band Count. IEP counter value necessary for desired complementary mode dead band.

0x00000068	4	IEP1_PWM_RECFG	IEP1 PWM Reconfiguration. Flags for controlling which PWM parameters are reconfigured. • Host writes '1' to request update of associated parameter. • Firmware clears flag to '0' to inform Host update of parameter is complete.
0x0000006C	4	IEP1_PWM_MODE	IEP1 PWM Mode. Flags for selecting PWM mode (Single-Ended or Complementary).
0x00000070	4	IEP1_PWM_EN	IEP1 PWM Enable. Flags for enabling / disabling PWMs.
0x00000074	4	IEP1_PWM_PRD_COUNT	IEP1 PWM Period Count. IEP counter value necessary for desired PWM frequency.
0x00000078	4	IEP1_PWM0_DC_COUNT	IEP1 PWM0 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x0000007C	4	IEP1_PWM1_DC COUNT	IEP1 PWM1 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000080	4	IEP1_PWM2_DC COUNT	IEP1 PWM2 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000084	4	IEP1_PWM3_DC COUNT	IEP1 PWM3 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000088	4	IEP1_PWM4_DC COUNT	IEP1 PWM4 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x0000008C	4	IEP1_PWM5_DC COUNT	IEP1 PWM5 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000090	4	IEP1_PWM6_DC COUNT	IEP1 PWM6 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000094	4	IEP1_PWM7_DC COUNT	IEP1 PWM7 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x00000098	4	IEP1_PWM8_DC COUNT	IEP1 PWM8 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x0000009C	4	IEP1_PWM9_DC COUNT	IEP1 PWM9 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x000000A0	4	IEP1_PWM10_DC COUNT	IEP1 PWM10 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x000000A4	4	IEP1_PWM11_DC COUNT	IEP1 PWM11 Duty Cycle Count. IEP counter value necessary for desired PWM duty cycle.
0x000000A8	2	IEP1_PWM0_1_DEADBAND	IEP1 PWM0 & 1 Dead Band Count. IEP counter value necessary for desired complementary mode dead band.
0x000000AA	2	IEP1_PWM2_3_DEADBAND	IEP1 PWM2 & 3 Dead Band Count. IEP counter value necessary for desired complementary mode dead band.
0x000000AC	2	IEP1_PWM4_5_DEADBAND	IEP1 PWM4 & 5 Dead Band Count. IEP counter value necessary for desired complementary mode dead band.
0x000000AE	2	IEP1_PWM6_7_DEADBAND	IEP1 PWM6 & 7 Dead Band Count. IEP counter value necessary for desired complementary mode dead band.
0x000000B0	2	IEP1_PWM8_9_DEADBAND	IEP1 PWM8 & 9 Dead Band Count. IEP counter value necessary for desired complementary mode dead band.
0x000000B2	2	IEP1_PWM10_11_DEADBAND	IEP1 PWM10 & 11 Dead Band Count. IEP counter value necessary for desired complementary mode dead band.
0x000000B4	Remaining	Reserved	

Table 3. Firmware Register Memory Map

5.1.2 Register Descriptions

5.1.2.1 Firmware Magic Number

The table below contains descriptions of the Firmware Magic Number FW register bit fields.

Bit	Field	Type	Description
31-24	Magic Number Byte 3	R-4Dh	'M'
23-16	Magic Number Byte 2	R-57h	'W'
15-8	Magic Number Byte 1	R-50h	'P'
7-0	Magic Number Byte 0	R-47h	'G'

LEGEND: R/W = Read/Write; R = Read Only; -n = value after firmware load

Table 4. Firmware Magic Number FW Register Description

5.1.2.2 Firmware Type

The table below contains descriptions of the Firmware Type FW register bit fields.

Bit	Field	Type	Description
31-24	Firmware ICSS version	R-01h	01h – ICSS Revision 2
23-8	Firmware Protocol Type	R-0002h	0002h – Control Class
7-0	Firmware Protocol Type Version	R-01h	01h – ICSSG PWM version (arbitrary, no PWM specification)

LEGEND: R/W = Read/Write; R = Read Only; -n = value after firmware load

Table 5. Firmware Type FW Register Description

5.1.2.3 Firmware Version

The table below contains descriptions of the Firmware Version FW register bit fields.

Bit	Field	Type	Description
31	Firmware Release or Internal Version	R-1b	0b – Release version 1b – Internal version
30-24	Firmware Version Major	R-0000001b	Major version number
23-8	Firmware Version Minor	R-00h	Minor version number
7-0	Firmware Version Build	R-00h	Build version number

LEGEND: R/W = Read/Write; R = Read Only; -n = value after firmware load

Table 6. Firmware Version FW Register Description

5.1.2.4 Firmware Feature

The table below contains descriptions of the Firmware Feature FW register bit fields.

Bit	Field	Type	Description
31-13	RESERVED	-	-
12-9	Firmware IEP1 Number of Supported PWMs	R-1100b	Firmware supports supports 12 PWMs on IEP1.
8-5	Firmware IEP0 Number of Supported PWMs	R-1100b	Firmware supports supports 12 PWMs on IEP0.
4-0	Firmware Number of Supported PWMs	R-11000b	Firmware supports 24 PWMs

LEGEND: R/W = Read/Write; R = Read Only; -n = value after firmware load

Table 7. Firmware Feature FW Register Description

5.1.2.5 Firmware Extended Feature

The table below contains descriptions of the Firmware Extended Feature FW register bit fields.

Bit	Field	Type	Description
31-0	Offset to extended feature structure for future use	R-00000000h	Reserved for future use

LEGEND: R/W = Read/Write; R = Read Only; -n = value after firmware load

Table 8. Firmware Extended Feature FW Register Description

5.1.2.6 PWM_CTRL

The table below contains descriptions of the PWM_CTRL FW register bit fields.

Bit	Field	Type	Description
31-3	RESERVED	-	-
2	IEP1_PWM_GBL_EN	R/W-0b	IEP1 PWMs global enable. Controls whether IEP1 PWMs are disabled or enabled. This flag is only read during firmware initialization time. 0b – IEP1 PWMs disabled. 1b – IEP1 PWMs enabled.
1	IEP0_PWM_GBL_EN	R/W-0b	IEP0 PWMs global enable. Controls whether IEP1 PWMs are disabled or enabled. This flag is only read during firmware initialization time. 0b – IEP0 PWMs disabled. 1b – IEP0 PWMs enabled.
0	PWM_EN	R/W-0b	PWM enable. FW continuously polls this bit in a loop at start of initialization until the bit is set to '1'. This allows Host driver software to configure FW registers with non-default values before FW initialization commences. 0b – PWMs disabled. 1b – PWMs enabled.

LEGEND: R/W = Read/Write; R = Read Only; -n = value after firmware load

Table 9. PWM_CTRL FW Register Description

5.1.2.7 PWM_STAT

The table below contains descriptions of the PWM_STAT FW register bit fields.

Bit	Field	Type	Description
31-4	RESERVED	-	-
3	FW_INIT	R-0b	Firmware initialized flag: 0b – Firmware initialization not complete. 1b – Firmware initialization complete. After enabling PRU, Host must wait for firmware initialization complete before writing to any firmware registers.
2	IEP1_PWM_GBL_EN_ACK	R-0b	IEP1 PWMs global enable acknowledge. Acknowledge flag corresponding to IEP1 enable control. 0b – IEP1 PWMs disabled. 1b – IEP1 PWMs enabled.
1	IEP0_PWM_GBL_EN_ACK	R-0b	IEP0 PWMs global enable acknowledge. Acknowledge flag corresponding to IEP0 enable control. 0b – IEP0 PWMs disabled. 1b – IEP0 PWMs enabled.
0	PWM_EN_ACK	R-0b	PWM enable acknowledge. Acknowledge flag corresponding to PWM enable control. 0b – PWMs disabled. 1b – PWMs enabled.

LEGEND: R/W = Read/Write; R = Read Only; -n = value after firmware load

Table 10. PWM_STAT FW Register Description

5.1.2.8 IEPx_PWM_RECFG

The table below contains descriptions of the IEP*x*_PWM_MODE FW register bit fields, where *x* = 0, 1.

Bit	Field	Type	Description
31-20	RESERVED	-	-
19-14	RECFG_IEPx_PWM_DB_COUNT	R/W-000000b	Reconfigure IEPx PWM Deadband Count. Bit *n* in field corresponds with PWM 2*n*_2*n+1*, e.g. Bit 0 is for PWM0_1. For any bit in field: 0 – no reconfiguration requested 1 – reconfiguration requested
13-2	RECFG_IEPx_PWM_DC_COUNT	R/W-000h	Reconfigure IEPx PWM Duty Cycle Count. Bit *n* in field corresponds with PWM *n*, e.g. Bit 0 is for PWM 0. For any bit in field: 0 – no reconfiguration requested 1 – reconfiguration requested
1	RECFG_IEPx_PWM_PRD_COUNT	R/W-0b	Reconfigure IEPx PWM Period Count: 0 – no reconfiguration requested 1 – reconfiguration requested
0	RECFG_IEPx_PWM_EN	R/W-0b	Reconfigure IEPx PWM Enable: 0 – no reconfiguration requested 1 – reconfiguration requested

LEGEND: R/W = Read/Write; R = Read Only; -n = value after firmware load

Table 11. IEPx_PWM_RECFG FW Register Description

5.1.2.9 IEP*x*_PWM_MODE

The table below contains descriptions of the IEP*x*_PWM_MODE FW register bit fields, where *x* = 0, 1.

Bit	Field	Type	Description
31-6	RESERVED	-	-
5	PWM10_11_MODE	R/W-0b	PWM 10 & 11 mode select: 0 – Single-Ended mode 1 – Complementary mode In Single-Ended mode, PWM10 and PWM11 are enabled/disabled individually, i.e.: • IEPx_PWM_EN:PWM10_EN = <0 or 1> • IEPx_PWM_EN:PWM11_EN = <0 or 1> In Complementary mode, PWM10 and PWM11 are enabled/disabled as a pair, i.e.: • IEPx_PWM_EN:PWM10_EN = 0, IEPx_PWM_EN:PWM11_EN = X : PWM10 & 11 disabled • IEPx_PWM_EN:PWM10_EN = 1, IEPx_PWM_EN:PWM11_EN = X : PWM10 & 11 enabled
4	PWM8_9_MODE	R/W-0b	PWM 8 & 9 mode select: 0 – Single-Ended mode 1 – Complementary mode In Single-Ended mode, PWM6 and PWM7 are enabled/disabled individually, i.e.: • IEPx_PWM_EN:PWM8_EN = <0 or 1> • IEPx_PWM_EN:PWM9_EN = <0 or 1> In Complementary mode, PWM8 and PWM9 are enabled/disabled as a pair, i.e.: • IEPx_PWM_EN:PWM8_EN = 0, IEPx_PWM_EN:PWM9_EN = X : PWM8 & 9 disabled • IEPx_PWM_EN:PWM8_EN = 1, IEPx_PWM_EN:PWM9_EN = X : PWM8 & 9 enabled
3	PWM6_7_MODE	R/W-0b	PWM 6 & 7 mode select: 0 – Single-Ended mode 1 – Complementary mode In Single-Ended mode, PWM6 and PWM7 are enabled/disabled individually, i.e.: • IEPx_PWM_EN:PWM6_EN = <0 or 1> • IEPx_PWM_EN:PWM7_EN = <0 or 1> In Complementary mode, PWM6 and PWM7 are enabled/disabled as a pair, i.e.: • IEPx_PWM_EN:PWM6_EN = 0, IEPx_PWM_EN:PWM7_EN = X : PWM6 & 7 disabled • IEPx_PWM_EN:PWM6_EN = 1, IEPx_PWM_EN:PWM7_EN = X : PWM6 & 7 enabled
2	PWM4_5_MODE	R/W-0b	PWM 4 & 5 mode select: 0 – Single-Ended mode 1 – Complementary mode In Single-Ended mode, PWM4 and PWM5 are enabled/disabled individually, i.e.: • IEPx_PWM_EN:PWM4_EN = <0 or 1> • IEPx_PWM_EN:PWM5_EN = <0 or 1> In Complementary mode, PWM4 and PWM5 are enabled/disabled as a pair, i.e.: • IEPx_PWM_EN:PWM4_EN = 0, IEPx_PWM_EN:PWM5_EN = X : PWM4 & 5 disabled • IEPx_PWM_EN:PWM4_EN = 1, IEPx_PWM_EN:PWM5_EN = X : PWM4 & 5 enabled

1	PWM2_3_MODE	R/W-0b	PWM 2 & 3 mode select: 0 – Single-Ended mode 1 – Complementary mode In Single-Ended mode, PWM2 and PWM2 are enabled/disabled individually, i.e.: • IEPx_PWM_EN:PWM2_EN = <0 or 1> • IEPx_PWM_EN:PWM3_EN = <0 or 1> In Complementary mode, PWM0 and PWM1 are enabled/disabled as a pair, i.e.: • IEPx_PWM_EN:PWM2_EN = 0, IEPx_PWM_EN:PWM3_EN = X : PWM2 & 3 disabled • IEPx_PWM_EN:PWM2_EN = 1, IEPx_PWM_EN:PWM3_EN = X : PWM2 & 3 enabled
0	PWM0_1_MODE	R/W-0b	PWM 0 & 1 mode select: 0 – Single-Ended mode 1 – Complementary mode In Single-Ended mode, PWM0 and PWM1 are enabled/disabled individually, i.e.: • IEPx_PWM_EN:PWM0_EN = <0 or 1> • IEPx_PWM_EN:PWM1_EN = <0 or 1> In Complementary mode, PWM0 and PWM1 are enabled/disabled as a pair, i.e.: • IEPx_PWM_EN:PWM0_EN = 0, IEPx_PWM_EN:PWM1_EN = X : PWM0 & 1 disabled • IEPx_PWM_EN:PWM0_EN = 1, IEPx_PWM_EN:PWM1_EN = X : PWM0 & 1 enabled

LEGEND: R/W = Read/Write; R = Read Only; -n = value after firmware load

Table 12. IEP*x*_PWM_MODE FW Register Description

5.1.2.10 IEP*x*_PWM_EN

The table below contains descriptions of the IEP*x*_PWM_EN FW register bit fields, where *x* = 0, 1.

Bit	Field	Type	Description
31-12	RESERVED	-	-
11	PWM11_EN	R/W-0b	PWM 11 enable: 0 – disabled 1 – enabled
10	PWM10_EN	R/W-0b	PWM 10 enable: 0 – disabled 1 – enabled
9	PWM9_EN	R/W-0b	PWM 9 enable: 0 – disabled 1 – enabled
8	PWM8_EN	R/W-0b	PWM 8 enable: 0 – disabled 1 – enabled
7	PWM7_EN	R/W-0b	PWM 7 enable: 0 – disabled 1 – enabled
6	PWM6_EN	R/W-0b	PWM 6 enable: 0 – disabled 1 – enabled
5	PWM5_EN	R/W-0b	PWM 5 enable: 0 – disabled 1 – enabled
4	PWM4_EN	R/W-0b	PWM 4 enable: 0 – disabled 1 – enabled
3	PWM3_EN	R/W-0b	PWM 3 enable: 0 – disabled 1 – enabled
2	PWM2_EN	R/W-0b	PWM 2 enable: 0 – disabled 1 – enabled
1	PWM1_EN	R/W-0b	PWM 1 enable: 0 – disabled 1 – enabled
0	PWM0_EN	R/W-0b	PWM 0 enable: 0 – disabled 1 – enabled

LEGEND: R/W = Read/Write; R = Read Only; -n = value after firmware load

Table 13. IEP*x*_PWM_EN FW Register Description

5.1.2.11 IEP*x*_PWM_PRD_COUNT

The table below contains descriptions of the IEP*x*_PWM_EN FW register bit fields, where *x* = 0,1.

Bit	Field	Type	Description
31-0	PRD_COUNT	R/W-0007A120h	IEP counter value necessary for desired PWM period. PRD_COUNT = (IEP clock freq)/(PWM freq)/2*5, where 5 is default IEP counter increment value. E.g. PWM freq = 1 kHz: • IEP clock freq = 250 MHz: PRD_COUNT = (250e6)/(1e3)/2*5 = 625e3. • IEP clock freq = 200 MHz: PRD_COUNT = (200e6)/(1e3)/2*5 = 500e3.

LEGEND: R/W = Read/Write; R = Read Only; -n = value after firmware load

Table 14. IEP*x*_PWM_PRD_COUNT FW Register Description

5.1.2.12 IEP*x*_PWM*m*_DC_COUNT

The table below contains descriptions of the IEP*x*_PWM*m*_DC_COUNT FW register bit fields, where *x* = 0, 1 and *m* = 0…11.

Bit	Field	Type	Description
31-0	DC_COUNT	R/W-0007A120h	IEP counter value necessary for desired PWM duty cycle. DC_COUNT = round(DC% *(2*PRD_COUNT)), where DC% is the Duty Cycle percentage. E.g. PWM freq = 1 kHz, DC% = 50: • IEP clock freq = 250 MHz: DC_COUNT = round(0.5 * (2*625e3)) = 6.25e3. • IEP clock freq = 200 MHz: DC_COUNT = round(0.5 * (2*500e3)) = 500e3.

LEGEND: R/W = Read/Write; R = Read Only; -n = value after firmware load

Table 15. IEPx_PWM*m*_DC_COUNT FW Register Description

5.1.2.13 IEP*x*_PWM*n*_*n*+1_DB_COUNT

The table below contains descriptions of the IEP*x*_PWM*n*_*n*+1_DB_COUNT FW register bit fields, where *x* = 0, 1 and *n* = 0, 2, 4, 6, 8, 10.

Bit	Field	Type	Description
15-0	DB_COUNT	R/W-0A00h	IEP counter value necessary for desired complementary mode deadband. DB_COUNT = (IEP clock freq)*(Dead band time)*5 E.g. Dead band time = 2.56 usec.: • IEP clock freq = 250 MHz: DB_COUNT = (250e6)*(2.56e-6)*5 = 3200 • IEP clock freq = 200 MHz: DB_COUNT = (200e6)*(2.56e-6)*5 = 2560

LEGEND: R/W = Read/Write; R = Read Only; -n = value after firmware load

Table 16. IEP*x*_PWM*n*_*n*+1_DB_COUNT FW Register Description

5.2 PWM Module Behavior

The PWM module exhibits the following behaviors for each IEP PWM set CMP*x*, *x* = 1…5:

1. The first CMP*x* event for the set causes the set to transition from Init to Active State, but the Active State update (High, Low, Toggle) for the PWM signal associated with the CMP*x* event doesn't occur.

2. The IEP CMP*x* event which triggers the Active State in the IEP CMP0 period must be cleared by software before the CMP*x* event can occur in next IEP CMP0 period.

Generating proper output signals from the PWM module requires software to account for these behaviors. Different software design approaches can be used for this purpose, each with different tradeoffs. The design selected for implementation of IEP PWM FW was chosen because it

provides the highest number of features from among the design methods considered. Specifically, the selected design provides symmetric (vs. left justified) PWMs together with:

1. Operation of all PWM module output signals.
2. Complementary PWMs.

The cost of providing these features is the FW must:

1. Continuously clear CMP*x*, resulting in a tight real-time deadline.
2. Write the CMP*x* Shadow Register each IEP CMP0 (1/2 PWM) period.
3. Implement PWM Enable/Disable, DC = 0%, and DC = 100% by moving the CMP*x* Shadow Register "inside" and "outside" the CMP0 period according to table of PWM state transitions.

5.3 Design Details

The FW design approach is summarized below.

- For each ICSSG PWM set *m*, *m* = 0, 1, 2, 3 (2 sets/IEP * 2 IEP = 4): set ICSSG_PWM*m*:PWM*m*_TRIP_CMP0_EN = 0 so that (Active ⇒ Initial) State transition does not occur on CMP0 event.

- For each ICSSG PWM set *m*, *m* = 0, 1, 2, 3: Select 1 (of 6) PWMs in each PWM set as "Sacrificial" PWM (SPWM), where SPWM handles missing Active State update in first IEP CMP0 period:
  - Set Active State Signal for all PWMs to Toggle.
  - For SPWM: set CMP PWM inside CMP0 period & Initial State Signal to opposite other PWMs.
  - For other PWMs: set CMP outside CMP0 period.
  - Upon completion of first IEP CMP period: set CMP for other PWMs inside CMP0 period.

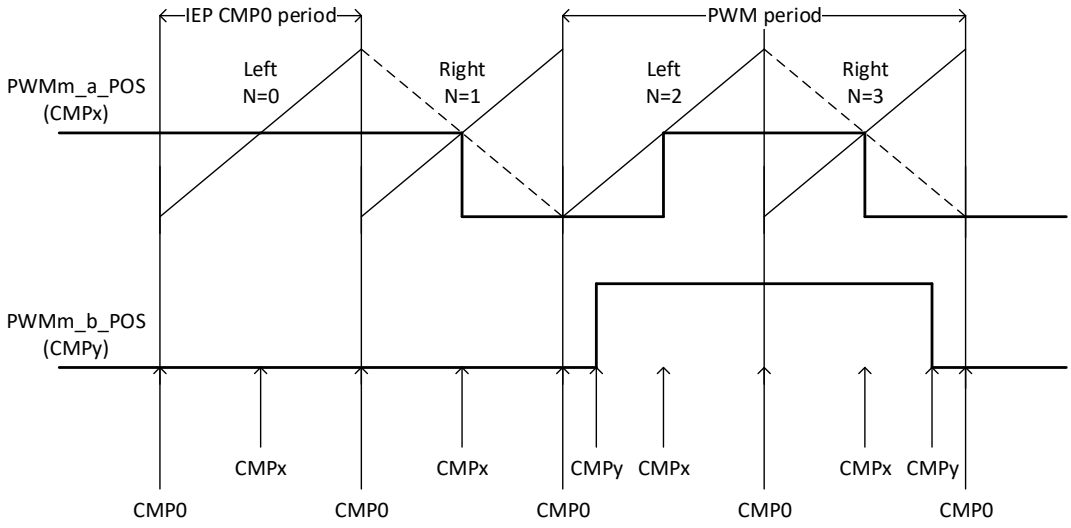
- Continuously clear CMP*x* for each IEP. Worst-case deadline before next CMP*x*: Deadline = (PWM period)/(PWM resolution), e.g. 1 msec./256 = 3.91 usec.

- Write CMP*x* Shadow Registers for enabled PWMs each IEP CMP0 period.

- Handle PWM Enable/Disable, DC = 0% & DC = 100% by moving CMP*x* "inside" and "outside" CMP0 period.

The symmetric PWM signals generated using this design approach are show in Figure 2. As can be observed, the symmetric PWM period is twice the IEP CMP0 period. Each PWM period starts with the "Left" or LHS (first IEP0 CMP0 period) followed by the "Right" or RHS (second IEP0 CMP0 period).

Figure 3 shows the method for handling PWM Enable/Disable and DC = 0%, while the method for handling DC = 100% and DC != 100% is shown in Figure 4.



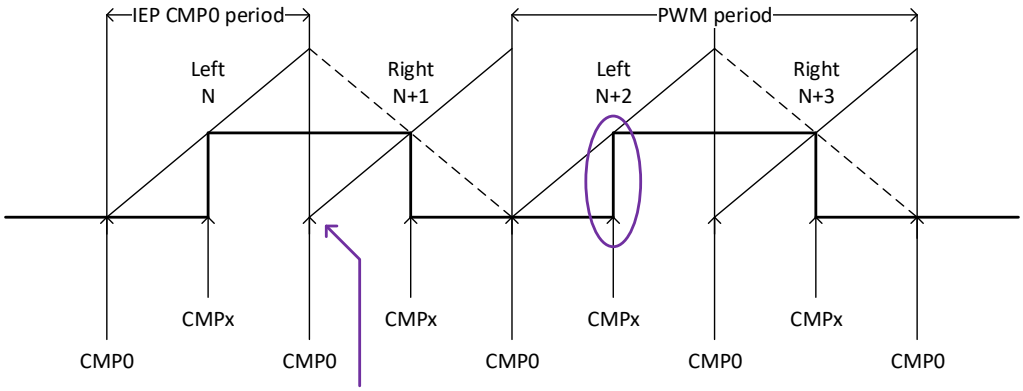
CMP0:
- HW: Counter Reset
- SW: Write CMP Shadow Regs

SW: continuous clear CMP1-6

CMPx N=1:
- HW: Initial to Active
- HW: Active, Toggle

CMPx, CMPy N>=1:
- HW: Active, Toggle

Figure 2. Symmetric PWM Signals



Disable PWM:
- **Set CMPx SR >= CMP0**
- **Disable SW CMPx SR updates**

Enable PWM:
- **Set CMPx SR < CMP0**
- **Enable CMPx SR updates**

Figure 3. Method for PWM Disable/Enable & DC = 0%

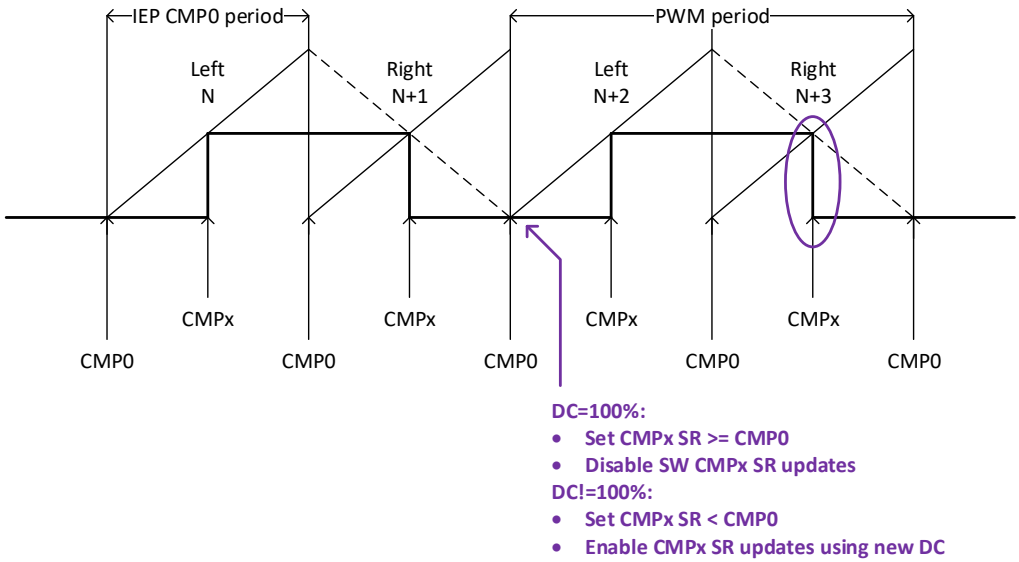


Figure 4. Method for DC = 100% & DC != 100%

5.3.1 PWM Signal Levels

The PWM signal levels are fixed in the current FW design. PWM signal levels are described below.

Initial signal levels for PWM

- SNGL PWM : High
- CMPL PWM POS/NEG : High/Low

Initial signal levels for SPWM

- SNGL PWM : Low
- CMPL PWM POS/NEG : Low/High

Active signal levels for CMPL PWMs

- POS : High
- NEG : Low

Active signal levels for disabled PWMs

- SNGL PWM : Low
- CMPL PWM POS/NEG : Low/High

5.3.2 PWM Action Tables

The FW must take certain actions to prepare for the next LHS or RHS of the PWM signal. These actions are a function of the current PWM enable and DC, together with any new PWM enable and DC received from reconfiguration requests. The required actions also depend on whether PWMs are being initialized (i.e. during first time initialization or period reconfiguration), or updated as part of normal (post-initialization) execution.

The actions required in all circumstances are presented in Table 18 - Table 23 below. The terms used in these tables are described in Table 17.

Term Column(s)	Term	Description
Latch	En_new = <value>	Latch new PWM enable setting <value> received from enable reconfiguration request to internal FW state
Latch	DC_new = <value>	Latch new PWM DC setting <value> received from DC reconfiguration request to internal FW state
LHS / RHS prepare action	CMP SR = EV	Set Compare Shadow Register to Early Value inside IEP0 Period, e.g. 5.
LHS / RHS prepare action	CMP SR = PRD	Set Compare Shadow Register to value outside CMP0 Period
LHS / RHS prepare action	CMP SR = PRD-DC_LHS_X	Set Compare Shadow Register to (CMP0 Period minus LHS value for DC = X)
LHS / RHS prepare action	CMP SR = PRD-DC_LHS_Y	Set Compare Shadow Register to (CMP0 Period minus LHS value for DC = Y)
LHS / RHS prepare action	Enable SR update	Enable write to CMP Shadow Register during LHS / RHS preparation
LHS / RHS prepare action	Disable SR update	Disable write to CMP Shadow Register during LHS / RHS preparation

Table 17. PWM Action Table Terms

5.3.2.1 Initialization

En_new	DC_cur	LHS prepare action	RHS prepare action
0	<any>	-	-
1	0	-	-
1	100	CMP SR = EV & Enable SR update	CMP SR = PRD & Disable SR update
1	X	CMP SR = PRD-DC_LHS_X & Enable SR update	-

Table 18. Action Table, Normal PWM Initialization

En_new	DC_cur	LHS prepare action	RHS prepare action
0	<any>	CMP SR = PRD & Disable SR update	-
1	0	CMP SR = PRD & Disable SR update	-
1	100	-	CMP SR = PRD & Disable SR update
1	X	CMP SR = PRD-DC_LHS_X & Enable SR update	-

Table 19. Action Table, Sacrificial PWM Initialization

5.3.2.2 Normal Execution

En_old	En_new	DC_cur	DC_new	PWM State cur	PWM State new	Latch	LHS prepare Action	RHS prepare action
0	0	X	X	L/H	L/H	-	-	-
0	0	X	Y	L/H	L/H	DC_new = Y	-	-
0	0	X	0	L/H	L/H	DC_new = 0	-	-
0	0	X	100	L/H	L/H	DC_new = 100	-	-
0	0	0	Y	L/H	L/H	DC_new = Y	-	-
0	0	0	0	L/H	L/H	-	-	-
0	0	0	100	L/H	L/H	DC_new = 100	-	-
0	0	100	Y	L/H	L/H	DC_new = Y	-	-
0	0	100	0	L/H	L/H	DC_new = 0	-	-
0	0	100	100	L/H	L/H	-	-	-

Table 20. Action Table, No PWM Enable Reconfiguration & PWM Disabled

En_old	En_new	DC_cur	DC_new	PWM State cur	PWM State new	Latch	LHS prepare Action	RHS prepare Action
1	1	X	X	DC_x	DC_x	-	-	-
1	1	X	Y	DC_x	DC_y	DC_new = Y	CMP SR = PRD–DC_LHS_Y	-
1	1	X	0	DC_x	L/H	DC_new = 0	CMP SR = PRD & Disable SR update	-
1	1	X	100	DC_x	H/L	DC_new = 100	-	CMP SR = PRD & Disable SR update
1	1	0	Y	L/H	DC_y	DC_new = Y	CMP SR = PRD–DC_LHS_Y & Enable SR update	-
1	1	0	0	L/H	L/H	-	-	-
1	1	0	100	L/H	H/L	DC_new = 100	CMP SR = EV & Enable SR update	CMP SR = PRD & Disable SR update
1	1	100	Y	H/L	DC_y	DC_new = Y	-	CMP SR = DC_RHS_Y & Enable SR update
1	1	100	0	H/L	L/H	DC_new = 0	CMP SR = EV & Enable SR update	CMP SR = PRD & Disable SR update
1	1	100	100	H/L	H/L	-	-	-

Table 21.Action Table, No PWM Enable Reconfiguration & PWM Enabled

En_old	En_new	DC_cur	DC_new	PWM State cur	PWM State new	Latch	LHS prepare Action	RHS prepare action
0	1	X	X	L/H	DC_x	En_new = 1	CMP SR = PRD–DC_LHS_X & Enable SR update	-
0	1	X	Y	L/H	DC_y	En_new = 1, DC_new = Y	CMP SR = PRD–DC_LHS_Y & Enable SR update	-
0	1	X	0	L/H	L/H	En_new = 1, DC_new = 0	-	-
0	1	X	100	L/H	H/L	En_new = 1, DC_new = 100	CMP SR = EV & Enable SR update	CMP SR = PRD & Disable SR update
0	1	0	Y	L/H	DC_y	En_new = 1, DC_new = Y	CMP SR = PRD–DC_LHS_Y & Enable SR update	-
0	1	0	0	L/H	L/H	En_new = 1	-	-
0	1	0	100	L/H	H/L	En_new = 1, DC_new = 100	CMP SR = EV & Enable SR update	CMP SR = PRD & Disable SR update
0	1	100	Y	L/H	DC_y	En_new = 1, DC_new = Y	CMP SR = PRD–DC_LHS_Y & Enable SR update	-
0	1	100	0	L/H	L/H	En_new = 1, DC_new = 0	-	-
0	1	100	100	L/H	H/L	En_new = 1	CMP SR = EV & Enable SR update	CMP SR = PRD & Disable SR update

Table 22. Action Table, PWM Enable Reconfiguration & PWM Enable

En_old	En_new	DC_cur	DC_new	PWM State Cur	PWM State new	Latch	LHS prepare Action	RHS prepare action
1	0	X	X	DC_x	L/H	En_new = 0	CMP SR = PRD & Disable SR update	-
1	0	X	Y	DC_x	L/H	En_new = 0, DC_new = Y	CMP SR = PRD & Disable SR update	-
1	0	X	0	DC_x	L/H	En_new = 0, DC_new = 0	CMP SR = PRD & Disable SR update	-
1	0	X	100	DC_x	L/H	En_new = 0, DC_new = 100	CMP SR = EV & Enable SR update	-
1	0	0	Y	L/H	L/H	En_new = 0, DC_new = Y	-	-
1	0	0	0	L/H	L/H	En_new = 0	-	-
1	0	0	100	L/H	L/H	En_new = 0, DC_new = 100	-	-
1	0	100	Y	H/L	L/H	En_new = 0, DC_new = Y	CMP SR = EV & Enable SR update	CMP SR = PRD & Disable SR update
1	0	100	0	H/L	L/H	En_new = 0, DC_new = 0	CMP SR = EV & Enable SR update	CMP SR = PRD & Disable SR update
1	0	100	100	H/L	L/H	En_new = 0	CMP SR = EV & Enable SR update	CMP SR = PRD & Disable SR update

Table 23. Action Table, PWM Enable Reconfiguration & PWM Disable

5.3.3 Host & PRU Firmware Communication

5.3.3.1 Initialization

Host and PRU interaction for FW initialization is shown below in Figure 5.

The primary responsibilities of the Host for PRU FW initialization include: (1) configuring the IEP clock; (2) loading the FW PRU IMEM and DMEM images; (3) writing PRU FW registers with desired non-default values; and (4) initiating execution of the PRU FW. The FW registers are initialized to default values on load of PRU FW DMEM image (FW register default values are described below in Section 5.1), and any non-default values must be written after load of the FW DMEM image.

The PRU FW parses the information provided by the Host in the PRU FW registers and applies the requested initial configuration. The following parameters are only parsed (and associated configuration applied) at FW initialization time:

- PWM_CTRL FW register, IEP0 & IEP1 Global Enable: IEP and PWM registers are only configured when the associated Global Enable bit is set. This allows the FW to use IEP0 PWMs, IEP1 PWMs, or IEP0 and IEP1 PWMs. Further, the IEP PWM FW image can be simultaneously executed from PRU0 and PRU1, provided the Global Enable settings are

consistent (e.g. PRU0 sets IEP0 Global Enable, while PRU1 sets IEP1 Global Enable). The FW informs the Host concerning observed Global Enable settings using the PWM_STAT Global Enable Acknowledge bits.

- IEPx_PWM_MODE FW register, IEP0 & IEP1 Mode: Each POS/NEG PWM signal pair is configured as 2 Single-Ended PWMs or 1 Complementary PWM.

The FW informs the Host that FW initialization is complete by setting the PWM_STAT FW_INIT flag bit. Upon observing this bit, the Host can issue commands to dynamically reconfigure PWMs.

The PWM_CTRL and PWM_STAT bits are shown below in Figure 6. FW Register Bits for .

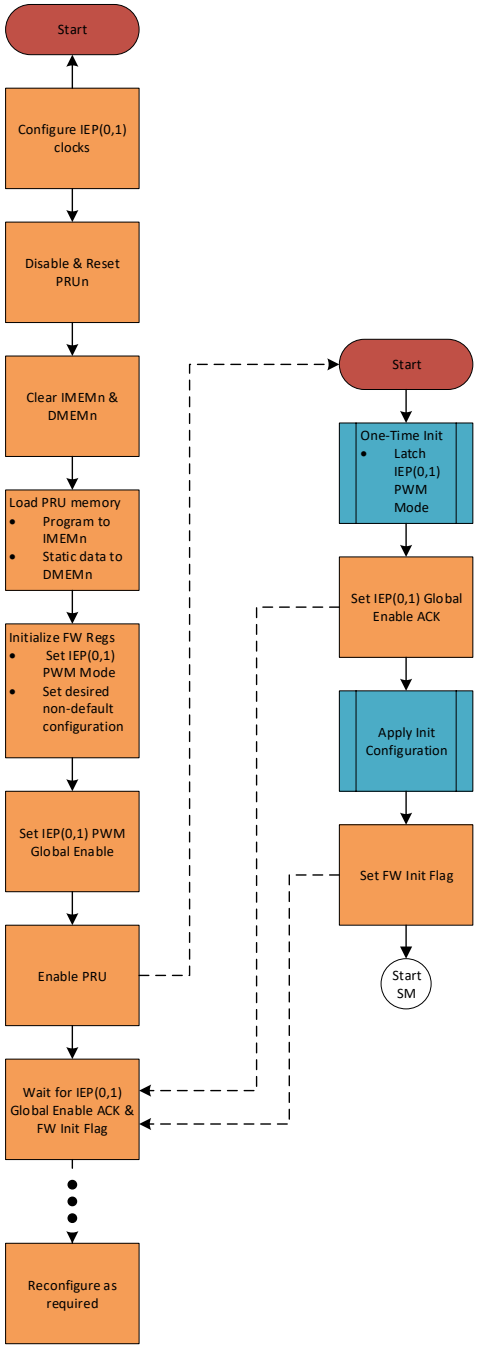


Figure 5. Firmware Initialization

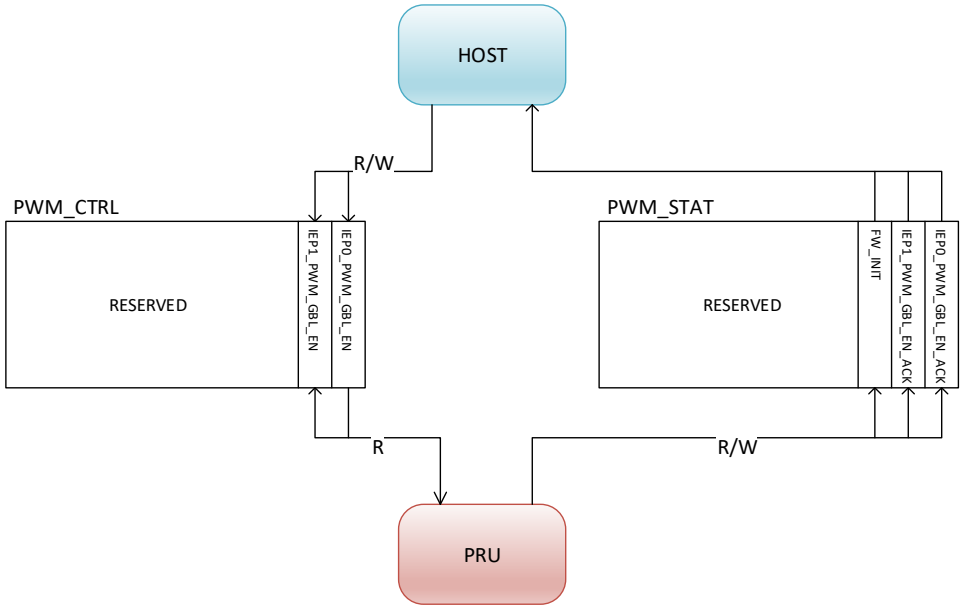


Figure 6. FW Register Bits for FW Initialization

5.3.3.2 Reconfiguration

The Host can dynamically reconfigure all PWM parameters except IEP0 & IEP1 Global Enable and IEP0 & IEP1 PWM Mode. PWM parameter reconfiguration is achieved as follows:

1. Host writes updated parameter value to FW register
2. Host triggers reconfiguration by setting associated reconfiguration request bit in IEPx_PWM_RECFG.

For example, to reconfigure the IEP0 PWM Period, the Host:

1. Writes new PWM period to IEP0_PWM_PRD_COUNT
2. Writes '1' IEP0_PWM_RECFG: RECFG_IEP0_PWM_PRD_COUNT.

The PRU FW services reconfiguration requests on PWM period boundaries in the LHS_RECFG (Host) reconfiguration State Machine state. The FW State Machine is described below in Section 5.3.4.

The IEPx_PWM_RECFG bits are shown below in Figure 7.

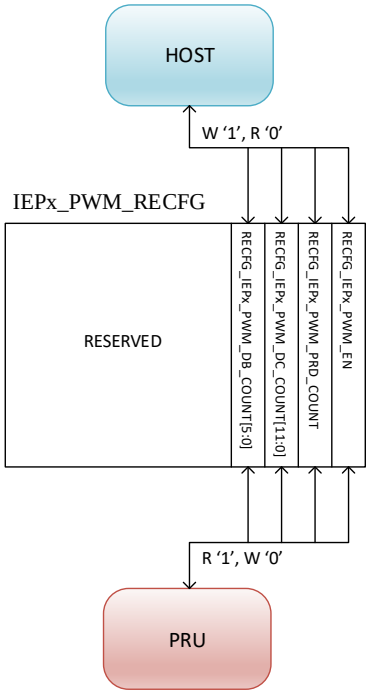


Figure 7. FW Register Bits for FW Reconfiguration

PWM parameter (re-)configuration is summarized in Table 24.

Configuration Parameter	Initialization, Dynamic	Affects
IEP*x*_GBL_EN	Initialization	All PWMs in 2 IEP PWM sets
IEP*x*_PWM_MODE [5:0]	Initialization	Each bit: 2 SNGL / 1 CMPL PWM
IEP*x*_PWM_EN [11:0]	Dynamic	Each bit: 1 SNGL / 1 CMPL PWM
IEP*x*_PWM_PRD_COUNT	Dynamic	All PWMs in 2 IEP PWM sets
IEP*x*_PWM*m*_DC_COUNT	Dynamic	1 SNGL / 1 CMPL PWM
IEP*x*_PWM*n*_*n*+1_DB_COUNT	Dynamic	1 CMPL PWM

Table 24. PWM Parameter Configurability

5.3.4 Firmware State Machine

After One-Time Initialization and Application of the Initial Configuration (see Figure 5), the FW begins execution of the State Machine (SM). The SM includes five states, details of which are presented in Table 25. A diagram of the SM is presented in Figure 8, and detailed flow charts for all SM states are presented in Figure 9 - Figure 21.

State	Event Trigger	Description
INIT	IEPx CMP0	Initialize IEPx CMP Shadow Registers for PWM initialization. Set LHS/RHS actions according to configuration in FW registers & Initialization Action Tables.
LHS	IEPx CMP0	Write LHS DC values to CMP Shadow Registers for enabled SNGL / CMPL PWMs.
LHS_RECFG	None, executes after LHS	Check for Host reconfiguration requests. For all reconfiguration requests: • Determine LHS & RHS actions using Execution Action Tables • Execute LHS actions • Stash RHS actions. Note the SM transitions to the INIT state in case of a PWM Period reconfiguration request.
RHS	IEPx CMP0	Write RHS DC values to CMP Shadow Registers for enabled SNGL / CMPL PWMs.
RHS_RECFG	None, executes after RHS	Execute stashed (pending) RHS actions determined in LHS_RECFG state.

Table 25. State Machine State Descriptions

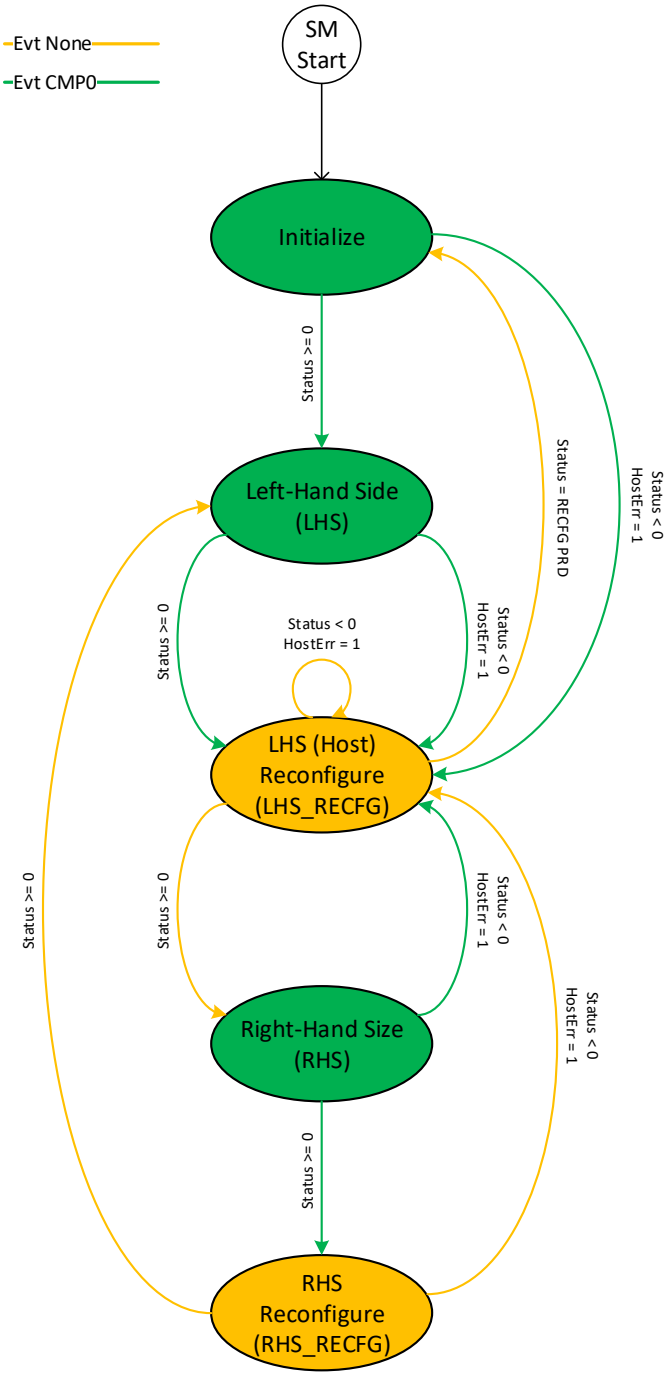


Figure 8. Firmware State Machine

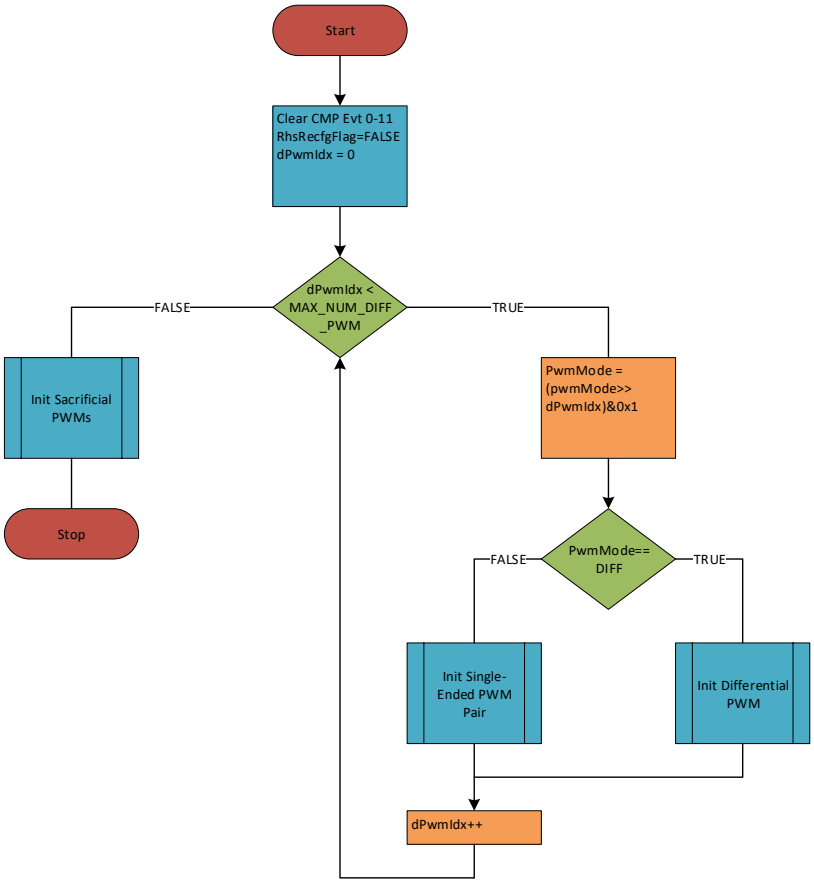


Figure 9. SM INIT State, Top-Level Flow Chart

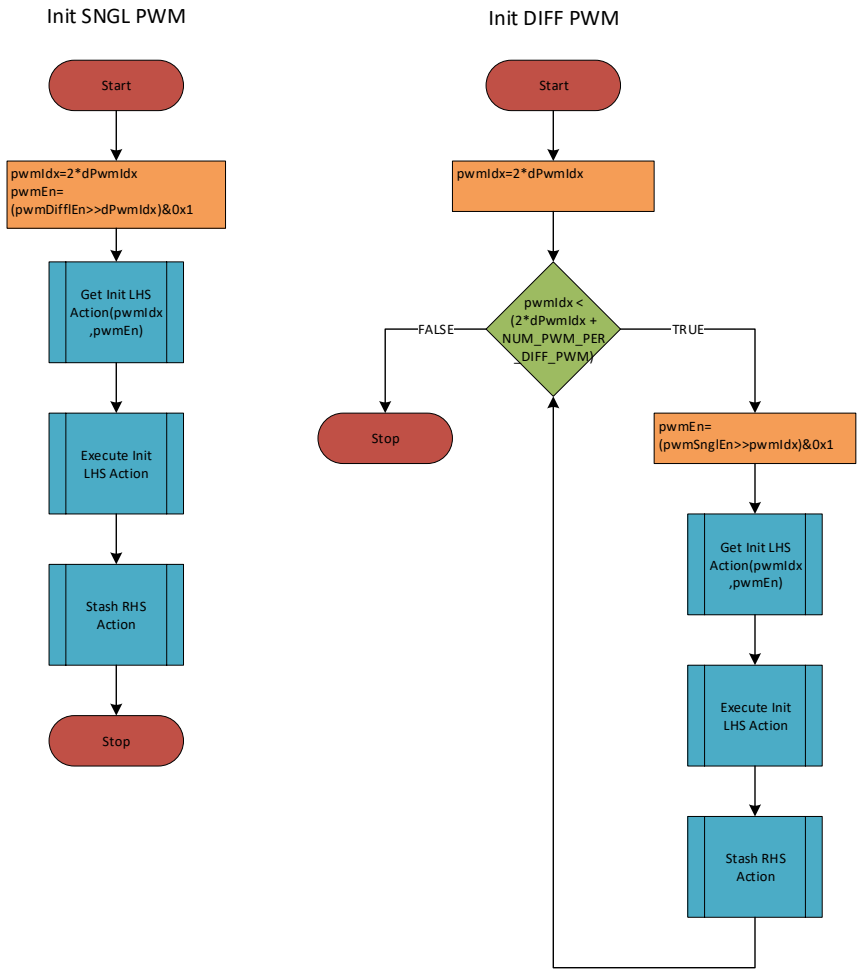


Figure 10. SM INIT State, Initialize SNGL/CMPL PWM Flow Charts

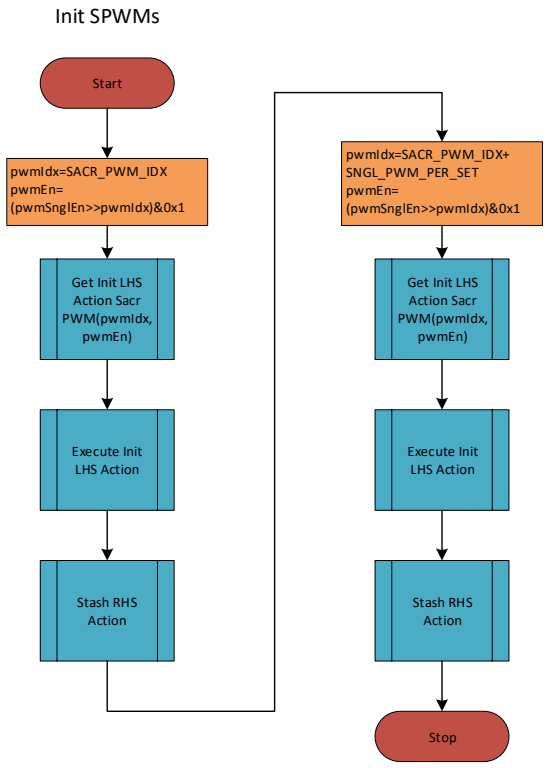


Figure 11. SM INIT State, Initialize SPWM Flow Chart

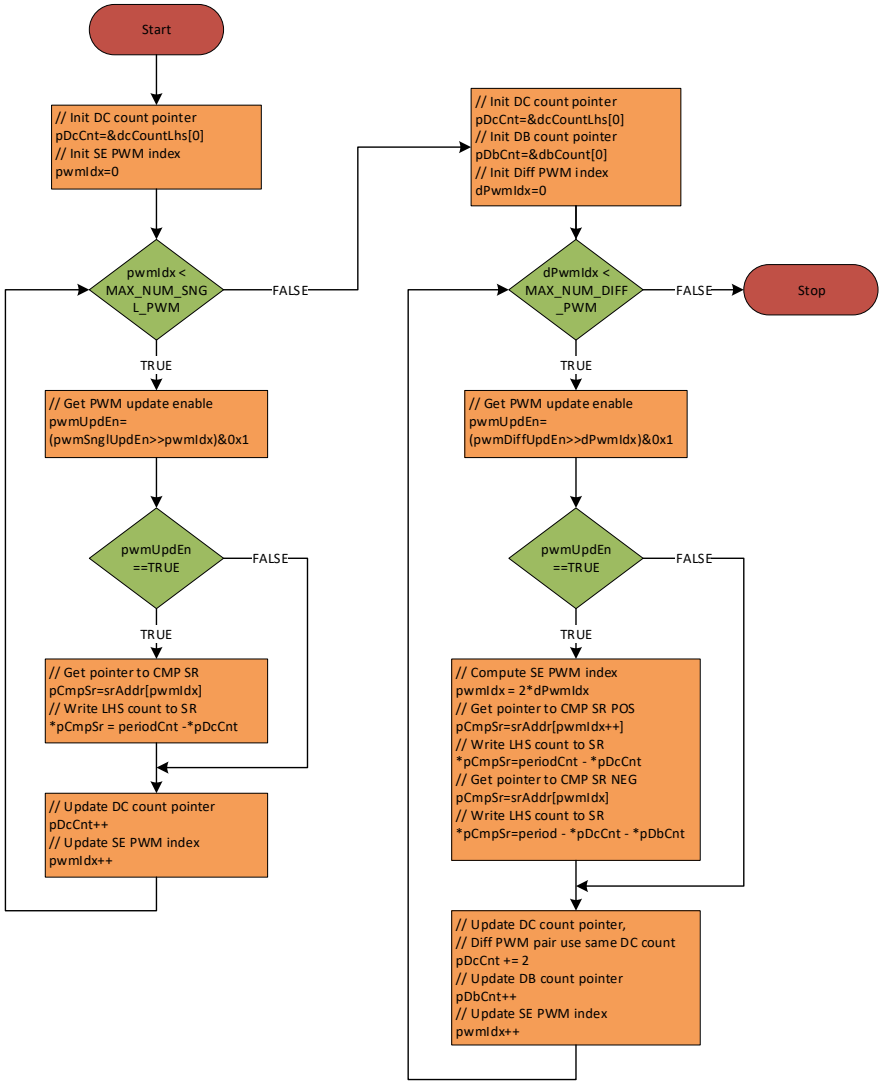


Figure 12. SM LHS State, Top-Level Flow Chart

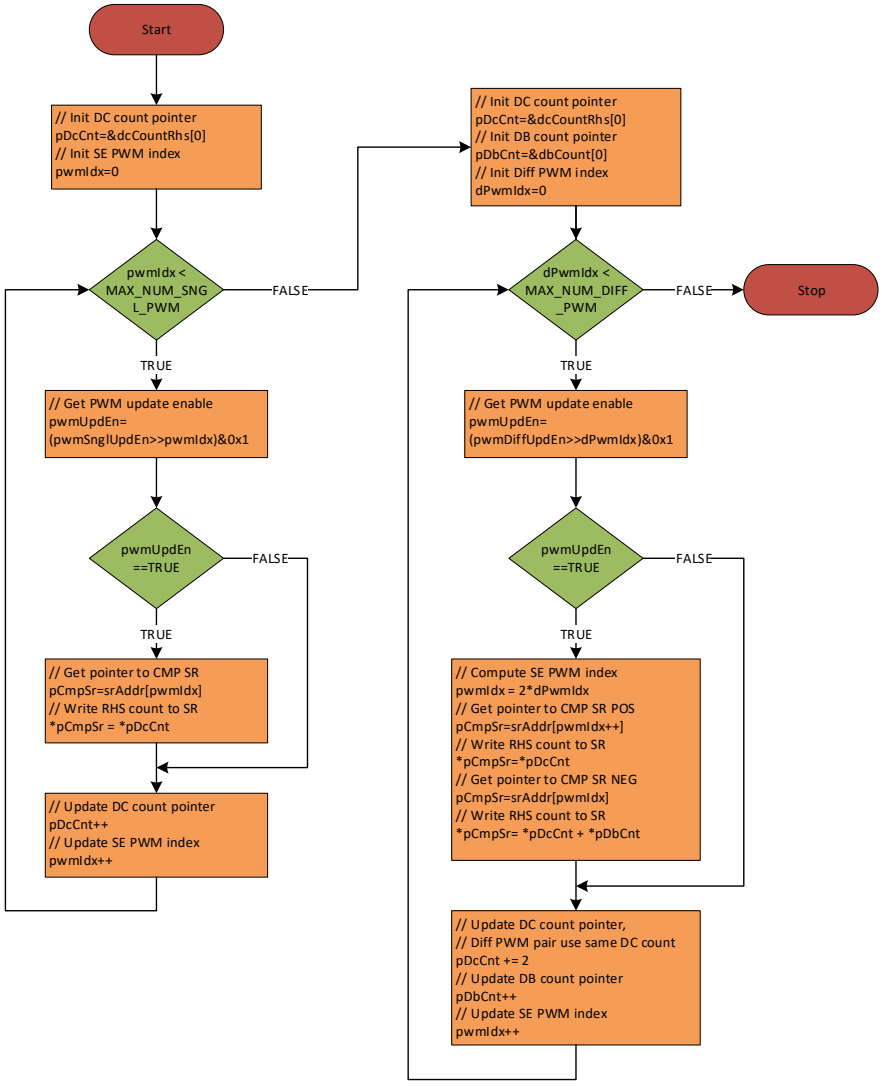


Figure 13. SM RHS State, Top-Level Flow Chart

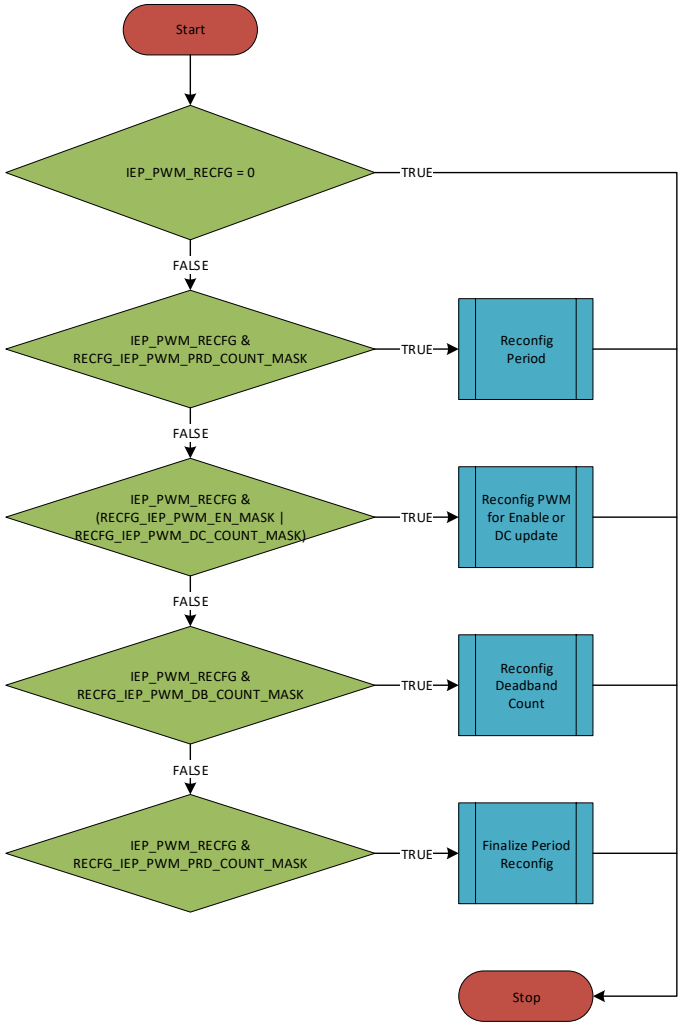


Figure 14. SM LHS_RECFG State, Top-Level Flow Chart

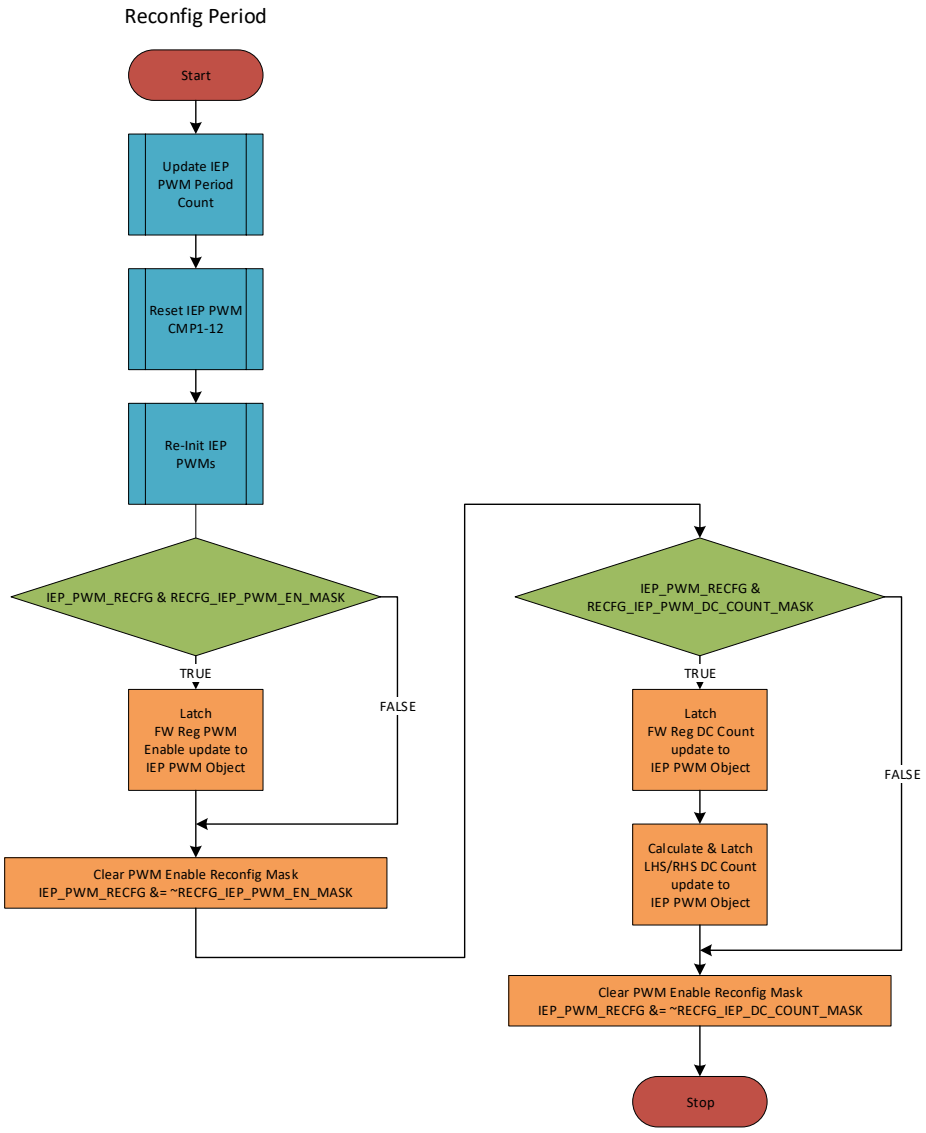


Figure 15. SM LHS_RECFG State, Reconfigure Period Flow Chart

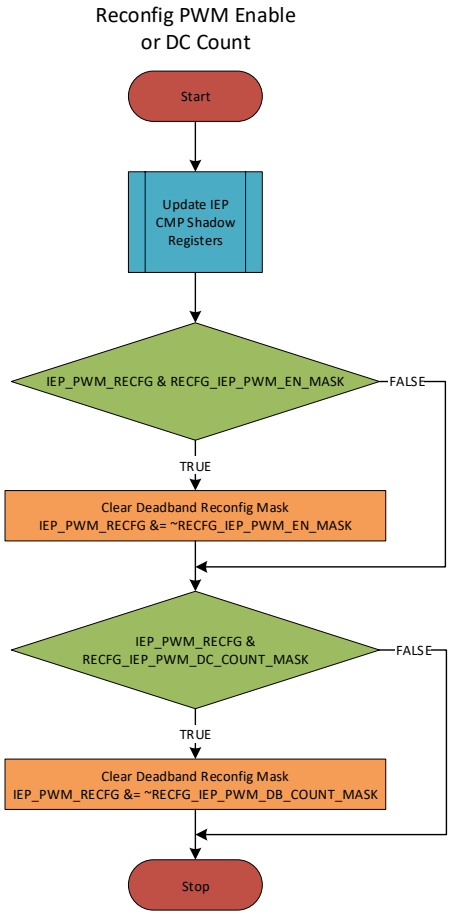


Figure 16. SM LHS_RECFG State, Reconfigure PWM Enable or DC Flow Chart

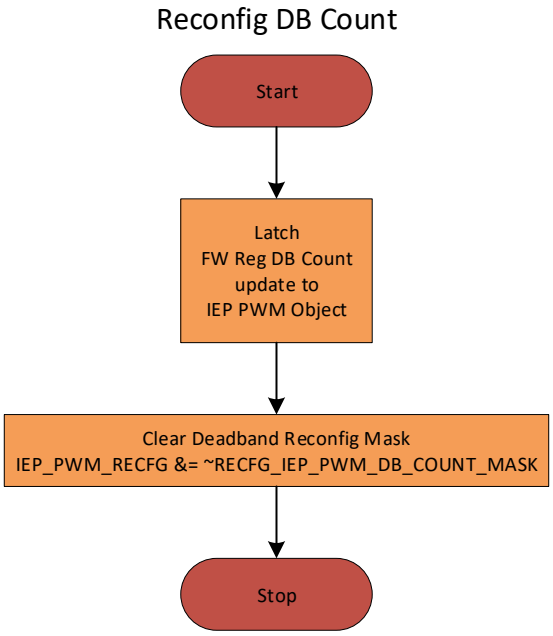


Figure 17. SM LHS_RECFG State, Reconfigure DB Flow Chart

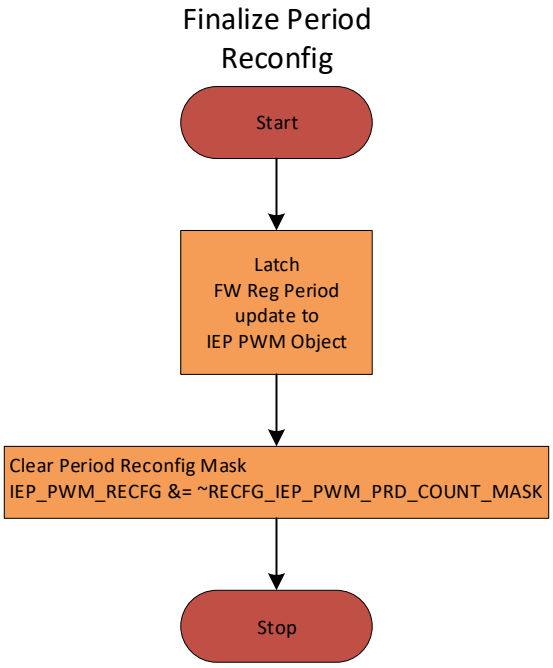


Figure 18. SM LHS_RECFG State, Finalize Period Reconfiguration Flow Chart

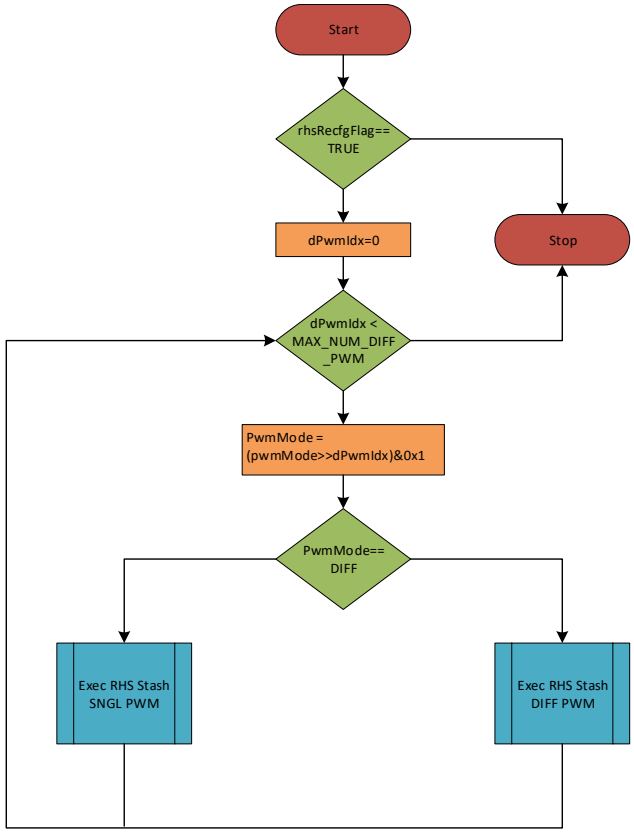


Figure 19. SM RHS_RECFG State, Top-Level Flow Chart

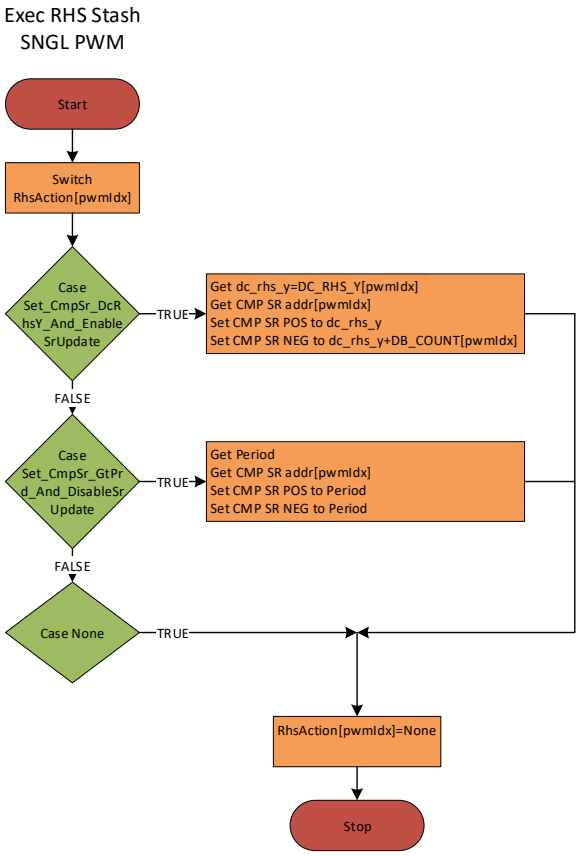


Figure 20. SM RHS_RECFG State, Execute RHS Stash for SNGL PWM Flow Chart

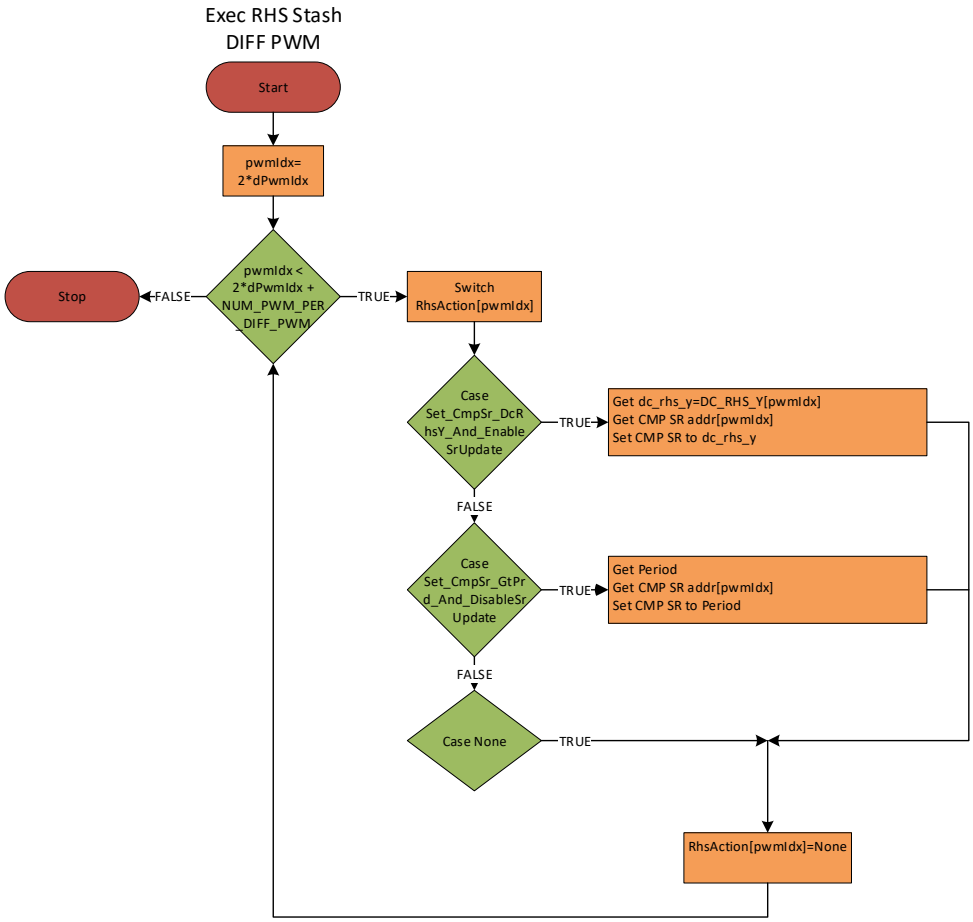


Figure 21. SM RHS_RECFG State, Execute RHS Stash for CMPL PWM Flow Chart

5.4 PRU Resource Usage

The FW is written entirely in C and no effort has been invested in optimizing the code to reduce PRU cycle or memory requirements.

5.4.1 PRU Cycles

Not Measured

5.4.2 PRU Memory

FW memory requirements are shown in Table 26. Memory types not listed in the table (i.e. Scratch-Pad Memory and Shared Memory) are not used by the FW.

Memory Type	Required Memory (Bytes)
IMEM	7412
DMEM	1072

Table 26. FW Memory Usage

5.5 Firmware Source Code

Table 27 lists the firmware source code files.

File	Description
AM654x_PRU.cmd	Linker command file for firmware build
icssg_iep_pwm.h	Header file, contains Host API FW register definitions
iepPwm.c	Contains code for State Machine and supporting functions
iepPwm.h	Header file, contains definitions for State Machine and supporting functions
iepPwmFwRegs.c	Contains code for FW default register settings
iepPwmFwRegs.h	Header file, contains FW register definitions
iepPwmHwRegs.h	Header file, contains hardware register definitions
main.c	Contains main function with top-level flow

Table 27. Firmware Source Files

6 ICSSG Release Target

6.1 EVM Platform

The PWM firmware was developed on the AM654x EVM based on AM6548 SR1.0 silicon.

6.1.1 AM654x EVM + Breakout Board

ICSSG	PRU	Instance	PWM Set	PRU GPIO Pin	PRU PWM Pin	BB Port	BB Pin
ICSSG1	PRU0	IEP0 PWM	0	PRG1_PRU0_GPO12	PRG1_PWM0_A0	J8	5
			0	PRG1_PRU0_GPO13	PRG1_PWM0_B0	J8	7
			0	PRG1_PRU0_GPO14	PRG1_PWM0_A1	J8	9
			0	PRG1_PRU0_GPO15	PRG1_PWM0_B1	J8	11
			0	PRG1_PRU0_GPO16	PRG1_PWM0_A2	J8	13
			0	PRG1_PRU0_GPO17	PRG1_PWM0_B2	J8	15
			1	PRG1_PRU1_GPO12	PRG1_PWM1_A0	J10	5
			1	PRG1_PRU1_GPO13	PRG1_PWM1_B0	J10	7
			1	PRG1_PRU1_GPO14	PRG1_PWM1_A1	J10	9
			1	PRG1_PRU1_GPO15	PRG1_PWM1_B1	J10	11
			1	PRG1_PRU1_GPO16	PRG1_PWM1_A2	J10	13
			1	PRG1_PRU1_GPO17	PRG1_PWM1_B2	J10	15
		IEP1 PWM	2	PRG1_PRU0_GPO2	PRG1_PWM2_A0	J7	5
			2	PRG1_PRU0_GPO4	PRG1_PWM2_B0	J7	7
			2	PRG1_PRU0_GPO8	PRG1_PWM2_A1	J7	9
			2	PRG1_PRU0_GPO10	PRG1_PWM2_B1	J8	1
			2	PRG1_PRU1_GPO2	PRG1_PWM2_A2	J9	5
			2	PRG1_PRU1_GPO4	PRG1_PWM2_B2	J9	9
			3	PRG1_PRU0_GPO0	PRG1_PWM3_A0	J7	1
			3	PRG1_PRU0_GPO1	PRG1_PWM3_B0	J7	3
			3	PRG1_PRU0_GPO6	PRG1_PWM3_A1	J7	13
			3	PRG1_PRU0_GPO7	PRG1_PWM3_B1	J7	15
			3	PRG1_PRU0_GPO3	PRG1_PWM3_A2	J7	7
			3	PRG1_PRU0_GPO5	PRG1_PWM3_B2	J7	11

Table 28. AM654x PWMs