Reduced Instruction Set Computer (RISC-V)

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**Abstract**

This paper focuses on Reduced Instruction Set Computer (RISC-V). Initially Designed at the University of California, Berkeley, RISC architecture evolved into RISC-V. While several RISC implementations were available in the market, they were often limited by restricted access. In 2011, the first version of RISC-V was released, and after several iterations, it has been adopted by numerous organizations. RISC-V offers simplicity, modularity, and extensibility, driving its growing adoption across various industries. As an open-source instruction set architecture (ISA), RISC-V provides extensive customization options, enabling developers to tailor it to specific use cases. This flexibility has led to its adoption across industries ranging from embedded systems and IoT devices to high-performance computing and artificial intelligence. This report will provide examples of the RISC-V instruction set, details on memory and I/O handling, and highlight specialized processing units, with a focus on parallel processing and pipelining for enhanced performance. It will discuss the performance characteristics of RISC-V, examining factors such as instruction throughput and efficiency. Furthermore, it will explore RISC-V's application and suitability across various industries, from embedded systems like IoT to high-performance sectors such as AI.

**Keywords:** RISC-V, Reduced Instruction Set Computing, modularity, microprocessors, low-power computing, computer architecture, hardware development, System-on-Chip, edge computing

**9.** **REFERENCES**

We require three references. We request you follow the APA (American Psychological Association) guidelines to cite sources. Following are examples of typical citation items:

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