

Name	Description
α_R	overhead area per kB of register-memory per vector-unit
α_M	overhead area per kB of shared-memory per SM
α_{L1}	L1 cache overhead area per SM-pair
α_{L2}	L2 cache overhead area
α_{oh}	common overhead area (I/O, global routing etc) per SM
β_R	area per register-file-bank per kB per vector-unit
β_M	area per shared-memory-bank per kB per SM
β_{L1}	L1 cache area per kB per SM-pair
β_{L2}	L2 cache area per kB
β_{VU}	core-logic area within a vector-unit
n_{SM}	total number of SM on the GPU chip
n_V	number of vector-units per SM
R_{VU}	kB of register files per vector-unit
M_{SM}	kB of shared memory per SM
$L1_{SMpair}$	kB of L1 cache per SM-pair
$L2_{SM}$	kB of L2 cache
\mathcal{A}_{tot}	total GPU chip die area
\mathcal{A}_{SM}	total shared-memory die area
\mathcal{A}_{cache}	total cache die area
\mathcal{A}_{oh}	total on-chip overhead die area
\mathcal{A}_{LSU}	total load-store unit die area
\mathcal{A}_{SFU}	total special-function unit die area
\mathcal{A}_{FPU}	total fetch-decode unit die area
\mathcal{A}_{Icache}	total instruction-cache die area
$\mathcal{A}_{LSUperSM}$	load-store unit die area per SM
$\mathcal{A}_{LSUperV}$	load-store unit die area per vector-unit
\mathcal{A}_{MperSM}	memory die area per SM
$\mathcal{A}_{SFUperV}$	special-function unit die area per vector-unit