Reorder Buffer	2.7GHz, 256-entry, max fetch/retire per cycle: 4/2, 5 pipeline (latency of non-mem instr)
L1 Cache	Private, 32KB, 4-way, 64B cache line, 9 CPU cycles hit (4+5)
L2 Cache	Private, 256KB, 8-way, 64B cache line, 15 CPU cycles hit (10+5)
L3 Cache	Shared, 16-way, 64B cache line, 1MB/core, 45 CPU cycles hit (40+5)
Memory Controller	2 buffer schedulers/MC, Read/Write Queue: 64/64
Link Bus	2.7GHz, point-to-point, read/write bus width: 16/16
Buffer Scheduler	FRFCFS , closed page Channel-interleave mapping
DRAM Parameters	
Memory	2 64-bit Channels, 2 Ranks/Channel, 8 devices/Rank, 8 sub-ranks/rank, x8-width sub-rank, 1 device/sub-rank
DRAM Device	DDR3-1333MHz, x8, 8 banks, 32768 Rows/bank, 1024 Columns/Row 8 KB Row Buffer per Bank, BL=8, Time and power parameters from Micron 2Gb SDRAM