

| Workload | Correlation Coefficients | |
|--------------------|---------------------------------|-------|
| PARSEC | L3 cache miss | 0.899 |
| | L2 cache miss | 0.513 |
| | Data TLB miss | 0.375 |
| | L1 instruction miss | 0.295 |
| | Instruction fetch stall | 0.877 |
| HPCC-COMM | L3 cache miss | 0.999 |
| | L2 cache miss | 0.988 |
| | Kernel-mode instruction | 0.980 |
| | Branch misprediction | 0.495 |
| | L1 instruction miss | 0.400 |
| HPCC-DGEMM | L3 cache miss | 0.988 |
| | L2 cache miss | 0.751 |
| | Data TLB miss | 0.662 |
| | Branch misprediction | 0.611 |
| | Instruction TLB miss | 0.353 |
| HPCC-FFT | L3 cache miss | 0.997 |
| | L2 cache miss | 0.961 |
| | Instruction TLB miss | 0.828 |
| | L1 instruction miss | 0.459 |
| | kernel-mode instruction | 0.435 |
| HPCC-HPL | L3 cache miss | 0.859 |
| | L2 cache miss | 0.834 |
| | Kernel-mode instruction | 0.597 |
| | Data TLB miss | 0.589 |
| | Instruction TLB miss | 0.435 |
| HPCC-PTRANS | L3 cache miss | 0.871 |
| | Kernel-mode instruction | 0.812 |
| | Instruction TLB miss | 0.809 |
| | Reservation buffer full store | 0.734 |
| | ReOrder Buffer full stall | 0.645 |
| HPCC-Random Access | L3 cache miss | 0.999 |
| | L2 cache miss | 0.999 |
| | Data TLB miss | 0.999 |
| | L1 instruction miss | 0.911 |
| | Instruction fetch stall | 0.890 |
| HPCC-Stream | L3 cache miss | 0.995 |
| | L2 cache miss | 0.978 |
| | L1 instruction cache miss | 0.873 |
| | Data TLB miss | 0.674 |
| | Application instruction retired | 0.398 |
| SPEC INT | L2 cache miss | 0.767 |
| | Data TLB miss | 0.699 |
| | Instruction TLB miss | 0.493 |
| | Kernel-mode instruction | 0.454 |
| | L3 cache miss | 0.389 |
| SPEC CFP | Data TLB miss | 0.719 |
| | Instruction TLB miss | 0.582 |
| | Kernel-mode instruction | 0.549 |
| | L2 cache miss | 0.452 |
| | L3 cache miss | 0.308 |