Parameter	Value
Pipeline width	4 (2 ALUs, 2 memory, 1 mult)
Pipeline depth	19 (4 fetch, 4 decode, 2 dispatch, 5 issue, 1 execute, 2 writeback, 1 commit)
IFQ, RUU, LSQ	16 instructions, 128 entries, 64 entries
Branch predictor	2-level
First level	13-bit register (xored with PC)
Second level	8192 entries
BTB	4096 entries, 2-way
Instruction set	PISA
L1 cache	32KB I & D, 4-assoc, 64B lines, 1 cycle hit
L2 cache	512KB, 8-assoc, 256B lines, 5 cycles hit
L3 cache	2MB, 8-assoc, 256B lines, 20 cycles hit
Memory	200 cycles first chunk, 20 cycles next chunk