

$n$	10				15			
process	TSMC 90nm CMOS							
$T$	8	16	32	64	32	64	128	256
CPD (ns)	0.555				0.588			
regular PU array area ( $\mu m^2$ )	27650	55259	113902	225418	150951	308640	602509	1212359
fine grained PU array area ( $\mu m^2$ )	19280	34131	59048	101377	104434	190615	334927	594048
area saving	30							