

Secret (bits)	Implementation		
	Serial	Parallel	Hybrid
Area (core cells)			
128	1546	10676	2243
256	2253	21171	3467
512	3698	44978	6553
Latency (cycles)			
128	339	8	48
256	603	12	72
512	1131	20	120
Throughput (cycles/byte)			
128	0,088	30	0,625
256	0,076	46	0,639
512	0,069	76	0,650