

90 taps	Vivado 2016.2	Quartus Prime 16.0
systolic structure	XC7A35T-3CSG324	5CEFA5F23C6
straightforward	238.10 MHz	145.65 MHz
partial break ( $z^{-1}$ )	303.03 MHz	148.82 MHz
full break ( $z^{-1}$ )	476.19 MHz	218.77 MHz
full break ( $z^{-2}$ )	526.32 MHz	231.75 MHz
Xilinx FIR Compiler	434.78 MHz	not applicable
Altera FIR Compiler	not applicable	213.72 MHz