	JSSC'14	JSSC'05	JSSC'03	This work	
Process	65 nm	110 nm	110 nm	130 nm	65  nm
				(Measured)	(Simulated)
Interconnect type	On-chip	Off-chip	Off-chip	On-Chip	
Synchronizer type	Mesochronous	Plesiochronous	Plesiochronous	Mesochronous	
Controller type	Digital	Analog	Digital	Coarse digital + fine analog	
Adaptive control	No	Yes	Yes	Yes	
Clock domain transfer	No	No	No	Yes	
Data rate	3  Gb/s	$10 \; \mathrm{Gb/s}$	$10 \; \mathrm{Gb/s}$	$1.3~\mathrm{Gb/s}$	4  Gb/s
Power consumption	1.08 mW	220 mW	129 mW	1.4 mW	1.5 mW
Supply Voltage	0.9 V	1.5 V	1.2 V	1.2 V	1 V
Area $(\mu m \times \mu m)$	Not reported	$250 \times 1400$	$1600 \times 2600$	$76 \times 80$	$48 \times 50$