Scenario	Appli. 1	Appli. 2	Appli. 3	Appli. 4
Channel Coding	Rate=1/3 Code block size = 1024			
QAM Modulation	QPSK			
(I)FFT Size	256	512	1024	2048
TX antenna	2			
Data quantization	14 bits			
FPGA Type	Xilinx Virtex-6 LX240T			
Clock Frequency	50 MHz			
Simulation time	Generation of 5 LTE sub-frames			