HIGH-VOLTAGE MIXED-SIGNAL IC

UC1618

128 x 268 4S STN LCD Controller-Driver

MP Specifications
Datasheet Revision: 1.3

IC Version: t_A
October 7, 2013

ULTRACHIP

The Coolest LCD Driver, Ever!!

TABLE OF CONTENT

UC1618

Single-Chip, Ultra-Low Power
128COM x 268SEG Matrix
Passive LCD Controller-Driver

INTRODUCTION

UC1618t is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture and FRM (Frame Rate Modulation) gray-shade modulation scheme to achieve near crosstalk free images, with well balanced gray shades.

In addition to low power COM and SEG drivers, UC1618t contains all necessary circuits for high-V LCD power supply, bias voltage generation, temperature compensation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Automotive Entertainment Displays

FEATURE HIGHLIGHTS

- RA items implemented to accord with AEC-Q100
- Single chip controller-driver for 128x268 matrix STN LCD with 4 gray shades and B/W Mode.
- A software-readable ID pin to support configurable vender identification.
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.
- Support both page ordered and column ordered display buffer RAM access.
- Support industry standard 2-wire, 3-wire serial buses (S8, S9), and 8-bit, 16-bit parallel bus (8080 or 6800).
- Special driver structure and gray shade modulation scheme. Consistent low power consumption under all display patterns.
- Fully programmable Mux Rate, partial display window, Bias Ratio and Line Rate allow many flexible power management options.
- Four software programmable frame rates up to 66Hz. Support the use of fast Liquid Crystal material for speedy LCD response.
- Software programmable 4 temperature compensation coefficients.
- On-chip Software RESET command, make RST pin optional.
- Self-configuring 10x charge pump with on-chip pumping capacitors. Only 3/5 external capacitors are required to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Very low pin count (9~10 pins with S8 or S9) allows exceptional image quality in COG format on conventional ITO glass.
- Many on-chip and I/O pad layout features to support optimized COG applications.
- V_{DD} (digital) range (Typ.) : 2.8V ~ 3.3V
  V_{DD} (analog) range (Typ.) : 2.8V ~ 3.3V
  LCD V_{OP} range: 6.3V ~ 16.0V
- Available in gold bump dies
  Bump pitch: 24 μM
  Bump gap: 12 μM
  Bump surface: 1,800 μM^2

ORDERING INFORMATION

Part Number	MTP	I^2C	Description
UC1618tGAA-U5P	No	No	Gold bumped die, V_{LCD} fine-tuned by VR

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

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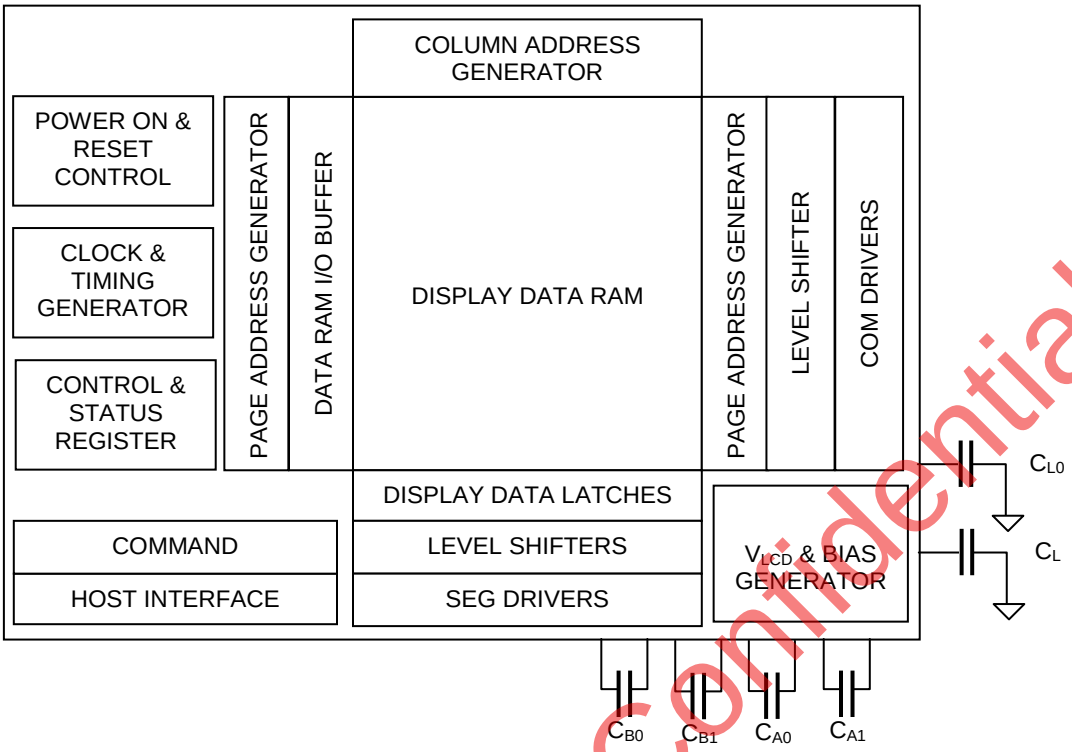
BLOCK DIAGRAM



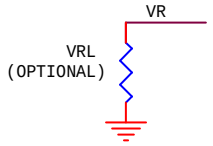
PIN DESCRIPTION

Name	Type	# of Pins	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	5 6 2	V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. Please maintain the following relationship: $V_{DD}+1.3V \geq V_{DD2/3} \geq V_{DD}$ Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{DD0}	PWR	2	Connect to V_{DD} pins on FPC and minimize the trace resistance for this node.
V_{SS} V_{SS2}	GND	5 6	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for this node.
V_{SS0}	GND	2	Connect to V_{SS} pins on FPC and minimize the trace resistance for this node.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{A0+}, V_{A0-} V_{A1+}, V_{A1-} V_{B0+}, V_{B0-} V_{B1+}, V_{B1-}	PWR	4, 4 4, 4 4, 4 4, 4	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{AX} / C_{BX} of values between V_{AX+}~ V_{AX-} / V_{BX+}~V_{BX-}, respectively. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
V_{LCD0}	PWR	2	Capacitor C_{L0} should be connected between V_{LCD0} and V_{SS}. Minimize the trace resistance for this node.
V_{LCDIN} V_{LCDOUT}	PWR	1 1	High voltage LCD Power Supply. Capacitor C_L should be connected between V_{LCDOUT} and V_{SS}. When C_L is used, keep the trace resistance under 70 Ω. When using internal pump, connect these pins together. When using external pump, connect V_{LCDIN} to external power and keep V_{LCDOUT} floating.

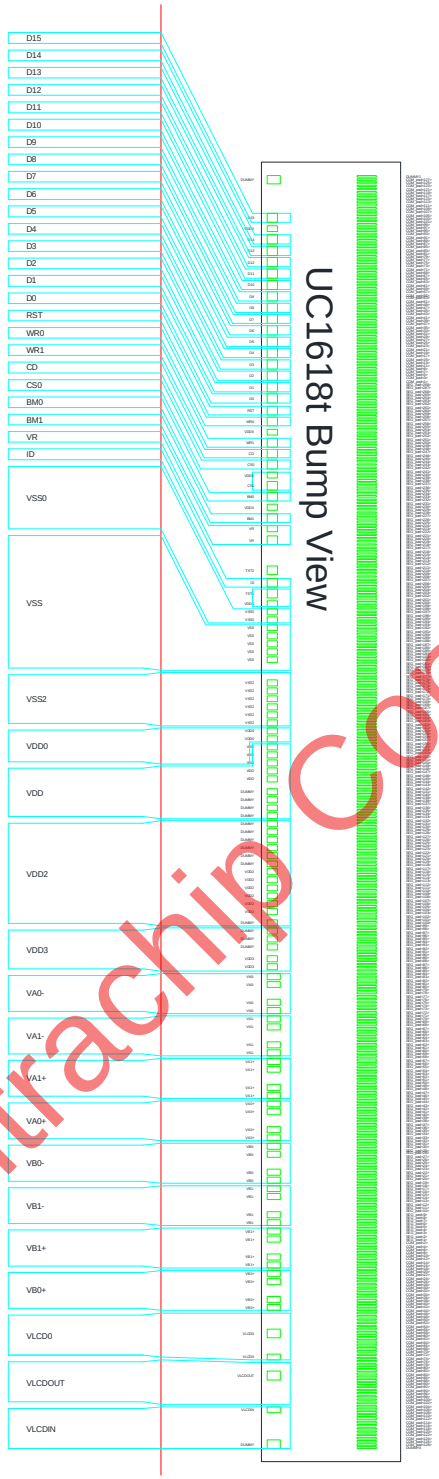
NOTE

- Recommended capacitor values:
  C_{AX}, C_{BX} : For panels of 3-inch or smaller, use 2.2uF (5V) capacitor;
  For panels bigger than 3 inches, use 5μF (5V) capacitor or higher.
  (Capacitor size depends on panel capacitance loading and actual image performance.)
  C_L : 330nF (25V) is appropriate for most applications.
  C_{L0} : 1uF (25V) is appropriate for most applications.
- To avoid the correction of digital signals being affected by the charging/discharging of V_{AX} or V_{BX}, do not overlay C_{AX}, C_{BX} with the digital layout while FPC wiring.

<table>
<tr><th>Name</th><th>Type</th><th># of Pins</th><th>Description</th></tr>
<tr><td colspan="4">HOST INTERFACE</td></tr>
<tr><td>BM0
BM1</td><td>I</td><td>1
1</td><td>Bus mode: The interface bus mode is determined by BM[1:0] and D15 with the following relationship:
<table>
<tr><th colspan="2">Mode</th><th>BM[1:0]</th><th>D15</th></tr>
<tr><td>8080</td><td rowspan="2">16-bit</td><td>10</td><td>Data</td></tr>
<tr><td>6800</td><td>11</td><td>Data</td></tr>
<tr><td>8080</td><td rowspan="2">8-bit</td><td>00</td><td>0</td></tr>
<tr><td>6800</td><td>01</td><td>0</td></tr>
<tr><td colspan="2">4-wire SPI w/ 8-bit token (S8)</td><td>00</td><td>1</td></tr>
<tr><td colspan="2">3-wire SPI w/ 9-bit token (S9)</td><td>01</td><td>1</td></tr>
</table></td></tr>
<tr><td>CS0
CS1</td><td>I</td><td>1
1</td><td>Chip Select. Chip is selected when CS1=”H” and CS0 = “L”. When the chip is not selected, D[7:0] will be high impedance.</td></tr>
<tr><td>RST</td><td>I</td><td>1</td><td>When RST=”L”, IC is in RESET state and all control registers are re-initialized to their default states.
An RC Filter has been included on-chip. There is no need for external RC noise filter.</td></tr>
<tr><td>CD</td><td>I</td><td>1</td><td>Select Control data or Display data for read/write operation.
”L”: Control data ”H”: Display data
In S9 mode, this pin is not used. Connect it to Vss.</td></tr>
<tr><td>ID</td><td>I</td><td>1</td><td>ID pin is for production control.
The connection will affect the content of PID when using the <code>Get Status</code> command. Connect to V_{DD} for “H” or V_{SS} for “L”.</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td>1
1</td><td>WR[1:0] controls the read/write operation of the host interface. See section Host Interface for more detail.
In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</td></tr>
<tr><td>D15~D0</td><td>I/O</td><td>16</td><td>Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect D[0] to SCK, D[3] to SDA,
<table>
<tr><th></th><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>16-bit (BM=1x)</td><td colspan="16">DB[15:0]</td></tr>
<tr><td>8-bit (BM=0x)</td><td>0</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td colspan="8">DB[7:0]</td></tr>
<tr><td>S8/S9 (BM=0x)</td><td>1</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>–</td><td>SDA</td><td>–</td><td>–</td><td>SCK</td></tr>
</table>
Connect unused pins to V_{SS}.</td></tr>
<tr><td colspan="4">HIGH VOLTAGE LCD DRIVER OUTPUT</td></tr>
<tr><td>SEG1 ~ SEG268</td><td>HV</td><td>268</td><td>SEG (column) driver outputs. Support up to 268 pixels.
Leave unused drivers open-circuit.</td></tr>
<tr><td>COM1 ~ COM128</td><td>HV</td><td>128</td><td>COM (row) driver outputs. Support up to 128 rows. Leave unused COM drivers open-circuit.</td></tr>
<tr><td colspan="4">Note:
Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COMx or SEGx will correspond to index x-1, and the value ranges for those index registers will be 0~127 for COM and 0~267 for SEG.</td></tr>
</table>

Name	Type	# of Pins	Description
MISC. PINS			
V_{DDX}	PWR	5	Auxiliary V_{DD}. These pins are connected to the main V_{DD} bus on chip. They are provided to facilitate chip configurations in COG application. These pins should not be used to provide V_{DD} power to the chip. It is not necessary to connect V_{DDX} to main V_{DD} externally.
VR	O	2	For fine-tuning V_{LCD}. Resistor VR_L should be connected between VR and V_{SS}. Leave them open when the IC does not use the function. 
TST2	I/O	1	Test I/O pin for UltraChip's use only. Leave it open during normal use.
TST5	I	1	For UltraChip's test use only. Connect to V_{DDx} for "H" on ITO circuit.
Dummy	–	18	Dummy pins are NOT connected inside the IC.
Note: R_L: 3.3MΩ ~ 10MΩ to act as a draining circuit when V_{DD} is shut down abruptly. VR_L: 0~500kΩ for fine-tuning V_{LCD}.			

RECOMMENDED COG LAYOUT



NOTES FOR V_{DD} WITH COG:

The typical operation condition of UC1618t, V_{DD}=2.8V, should be met under all operating conditions. Unless V_{DD} and $V_{DD2/3}$ ITO trances can each be controlled to be 20 Ω or lower; otherwise V_{DD}-$V_{DD2/3}$ separation can cause the actual on-chip V_{DD} to drop below 2.7V during high speed data-write condition. Therefore, for COG, V_{DD}-$V_{DD2/3}$ separation requires very careful ITO layout and very stringent testing before MP.

CONTROL REGISTERS

UC1618t contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meanings and their default values. Commands supported by UC1618t will be described in the next two sections. First, a summary table, followed by a detailed instruction-by-instruction description.

Name: The Symbolic reference of the register.
Note that some symbol names refer to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after System-Reset.

Name	# of Bits	Default	Description
SL	7	00H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (no scrolling) and (127– 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.
FLT FLB	4 4	0H 0H	Fixed Lines. The first FLTx2 lines and the last FLBx2 lines (relative to CEN) of each frame are fixed and are not affected by scrolling (SL). When FLT and/or FLB are non-zero, the screen is effectively separated into three regions: one scrollable, surrounded by two non-scrollable regions. When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three sections, 2xFLT on one side non-scrollable, 2XFLB on the other side also non-scrollable, and scrollable DST~DEN in the middle.
CR	9	000H	Returned Column Address. Useful for cursor implementation.
CA	9	000H	Column Address of Display Data RAM (Used in Host for Display Data RAM access)
PA	5	00H	Page Address of Display Data RAM (Used in Host to access Display Data RAM) When DC[4:3]=10b PA[4] : select Write Pattern 0 or 1 PA[3:0] : set SRAM page address When DC[4:3]=00b PA[4:0] : set SRAM page address
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b: 6 01b: 9 10b: 10 **11b: 11**
TC	2	0H	Temperature Compensation (per ^{o}C) **00b: -0.05%** 01b: -0.10% 10b: -0.15% 11b: -0.20%
PM	8	C3H	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PC	3	6H	Power Control. PC[1:0]: 00b: LCD <= 17nF 01b: : 17nF < LCD <= 20nF **10b: 20 < LCD <= 40nF** 11b: : 40nF < LCD PC[2]: 0b: External V_{LCD} **1b: Internal V_{LCD}** (10x pump, standard)

Name	# of Bits	Default	Description
DC	6	08H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) DC[3]: Gray Shade and B/W mode 0b: B/W Mode **1b: 4-Shade Mode** DC[4]: Input type for On/Off mode **0b: 2 bits per pixel** 1b: 1 bit per pixel DC[5]: Display pattern selection **0b: Pattern 0** 1b: Pattern 1 (Enabled only when On/Off mode and DC[4]=1)
AC	5	01H	Address Control: AC[0]: WA: Automatic column/page Wrap Around (Default **1: ON**) AC[1]: Auto-Increment order **0 : Column (CA) first** 1 : Row (PA) first AC[2]: RID: PA (Page Address) auto increment direction (**0 : +1** 1 : -1) AC[3]: Window Program Enable **0 : Disable** 1 : Enable AC[4]: CUM – Cursor Update Mode. (Default **0:OFF**) When CUM=1, CA increase on Write only
LC	10	130H	LCD Control: LC[0]: Enable the first FLTx2 and last FLBx2 lines in partial display mode (Default: **OFF**) LC[1]: MX, Mirror X. SEG/Page_C sequence inversion (Default: **OFF**) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: **OFF**) LC[4:3]: Line Rate (= Frame-Rate * Mux-Rate) 00b: 14.1 Klps 01b: 17.4 Klps **10b: 20.8 Klps** 11b: 25.4 Klps Line Rate (for On/Off mode): 00b: 6.9 Klps 01b: 8.5 Klps **10b: 10.2 Klps** 11b: 12.5 Klps (Klps: Kilo-line-per-second) LC[8:5]: Gray-Shade control. LC[8:7] / Gray-shade Level 2: 00→3, 01→4, **10→5**, 11→6 LC[6:5] / Gray-shade Level 1: 00→1, **01→2**, 10→3, 11→4 LC[9]: Partial Display Control **0b: Disable** Mux-Rate = CEN+1 (DST, DEN not used) 1b: Enabled Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB) x 2
NIV	7	00H	N-line Inversion: NIV[5:0]: **00000b: Disable Inversion Function** 000001b~111111b: Invert every 2~64 lines NIV[6]: 0b: **no-XOR** 1b: XOR
CSF	1	0H	COM Scan Function **0: Interlace Scan** 1: Progressive Scan
CEN DST DEN	7 7 7	7FH 00H 7FH	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN >= DEN >= DST+ 9

Name	# of Bits	Default	Description
WPC0	9	000H	Window program starting column address. Value range: **0** ~267.
WPP0	5	00H	Window program starting Page Address. Value range: **0**~31. When DC[4:3]=10b, Value range: 0~15
WPC1	9	10BH	Window program ending column address. Value range: 0~**267**.
WPP1	5	1FH	Window program ending Page Address. Value range: 0~**31**. When DC[4:3]=10b, Value range: 0~15. (Default : 0FH)
APC0~3 [7:0]	8x4	N/A	Advanced Product Configuration. For UltraChip only. Do *NOT* use.
Status Register			
MX, MY	1, 1		MX : Mirror X, that is LC[1]. MY : Mirror Y, that is LC[2].
WA, DE	1, 1		WA : automatic column/page Wrap Around, i.e. AC[0]. DE : display enabled.
Ver	2		Ver : IC version. Default : 00b
Prod, PID	2, 1	PIN	Prod[1:0] : Product Code, =10b. PID : Access the connected status of ID pin.

COMMAND SUMMARY

The following is a list of host commands supported by UC1618t:

C/D: 0: Control, 1: Data W/R: 0: Write Cycle, 1: Read Cycle D7-D0: # : Useful Data bits –: Don't Care

No	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3.	Get Status	0	1	0	MX	MY	WA	DE	0	0	0	Get {MX, MY, WA, DE Ver, Prod, PID}	N/A
				Ver[1:0]		0	0	0	0	0	0		
				Prod		PID	0	0	0	0	0		
4.	Set Column Address	0	0	0	0	0	0	0	0	0	0	Set CA[8:0]	000H
				#	#	#	#	#	#	#	#		
				-	-	-	-	-	-	-	#		
5.	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6.	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7.	Set Pump Control	0	0	0	0	1	0	1	1	0	#	Set PC[2]	1b
8.	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0], R = 0~3	N/A
		0	0	#	#	#	#	#	#	#	#		
9.	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0H
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0H
10.	Set Page Address LSB	0	0	0	1	1	0	#	#	#	#	Set PA[3:0]	0H
	Set Page Address MSB	0	0	0	1	1	1	-	-	-	#	Set PA[4]	0H
11.	Set V_{BIAS} Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	C3H
				#	#	#	#	#	#	#	#		
12.	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[9]	0: Disable
13.	Set COM Scan Function	0	0	1	0	0	0	0	1	1	#	Set CSF[0]	0b
14.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
15.	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set FLT[3:0], FLB[3:0]	00H
				#	#	#	#	#	#	#	#		
16.	Set Display mode	0	0	1	0	0	1	0	1	#	#	Set DC[5:4]	00b
17.	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
18.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
19.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
20.	Set Display Enable	0	0	1	0	1	0	1	1	#	#	Set DC[3:2]	10b
21.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
22.	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[6:0]	00H
				-	#	#	#	#	#	#	#		
23.	Set LCD Gray Shade 1	0	0	1	1	0	1	0	0	#	#	Set LC[6:5]	01b
24.	Set LCD Gray Shade 2	0	0	1	1	0	1	0	1	#	#	Set LC[8:7]	10b
25.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
26.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
27.	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
				#	#	#	#	#	#	#	#		
28.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 11
29.	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[4]=0, CA=CR	N/A
30.	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[4]=1, CR=CA	N/A
31.	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	127
				-	#	#	#	#	#	#	#		
32.	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
				-	#	#	#	#	#	#	#		
33.	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	127
				-	#	#	#	#	#	#	#		

No	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
34.	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Set WPC0	0
				#	#	#	#	#	#	#	#		
				-	-	-	-	-	-	-	#		
35.	Set Window Programming Starting Page Address	0	0	1	1	1	1	0	1	0	1	Set WPP0	0
				-	-	-	#	#	#	#	#		
36.	Set Window Programming Ending Column Address	0	0	1	1	1	1	0	1	1	0	Set WPC1	267
				#	#	#	#	#	#	#	#		
				-	-	-	-	-	-	-	#		
37.	Set Window Programming Ending Page Address	0	0	1	1	1	1	0	1	1	1	Set WPP1	31
				-	-	-	#	#	#	#	#		
38.	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[3]	0: Disable
SERIAL READ COMMAND (ENABLED ONLY IN S8/S9 MODE)													
39.	Get Status	0	0	1	1	1	1	1	1	1	0	Get status until chip disabled	N/A
		0	1	0	MX	MY	WA	DE	0	0	0		
				Ver		0	0	0	0	0	0		
				Prod		PID	0	0	0	0	0		

Warning: Any bit patterns other than the commands listed above may result in undefined behavior.

COMMAND DESCRIPTION

C/D: 0: Control, 1: Data W/R: 0: Write Cycle, 1: Read Cycle D7-D0: # : Useful Data bits –: Don't Care

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8-bit data write to SRAM							

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8-bit data from SRAM							

Write/Read Data Byte (command 1, 2) operation uses internal Page Address register (PA) and Column Address register (CA). Four rows of LCD pixel image are defined as one row in SRAM. Each column of pixel corresponds to one column of SRAM data. PA and CA registers can be programmed by issuing `Set Page Address` and `Set Column Address` commands. If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the CA boundary, and system programmers need to set the values of PA and CA explicitly. If WA is ON (1), when CA reaches end of column address, CA will be reset to 0 and PA will be increased or decreased, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 31), PA will be wrapped around to the other end of RAM and continue.

For 8-bit / 16-bit interface, the first cycle of read is a dummy read. Please ignore the data read out.

(3) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	**0**	MX	MY	WA	DE	**0**	**0**	**0**
			Ver[1:0]		**0**	**0**	**0**	**0**	**0**	**0**
			Prod		PID	**0**	**0**	**0**	**0**	**0**

Status 1 definitions:
- MX: Status of register LC[1], mirror X.
- MY: Status of register LC[2], mirror Y.
- WA: Status of register AC[0]. Automatic column/page wrap around.
- DE: Display enable flag. DE=1 when display is enabled

Status 2 definitions:
- Ver[1:0]: IC Version Code, 00 ~ 11. Default: 00

Status 3 definitions:
- Prod: Product Code. 10b.
- PID: Provide connection status of accessing to ID pin.

If multiple `Get Status` commands are issued consecutively within one single CD 1⇨0⇨1 transaction, the `Get Status` command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

(4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address CA[8:0]	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
			CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
			-	-	-	-	-	-	-	CA8

Set SRAM column address for read/write access. Each CA corresponds to one individual SEG electrode.

CA value range: **0**~267

(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

TC[1:0]	Temperature Compensation
00b	**-0.05% per ^{o}C**
01b	-0.10% per ^{o}C
10b	-0.15% per ^{o}C
11b	-0.20% per ^{o}C

(6) SET PANEL LOADING

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	**0**	**0**	**1**	**0**	**1**	**0**	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

PC[1:0]	Panel loading
00b	⩽17nF
01b	17~20nF
10b	**20~40nF**
11b	>40nF

(7) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[2]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	**0**	PC2

Set PC[2] to program the build-in charge pump stages.

PC[2]	Pump Control
0b	External V_{LCD}
1b	**Internal V_{LCD} (10x pump, standard)**

When using external pump, setting BR and setting PM are still necessary.

(8) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R][7:0] (Double-byte command)	0	0	**0**	**0**	**1**	**1**	**0**	**0**	R	R
	0	0	APC[R][7:0] register parameter							

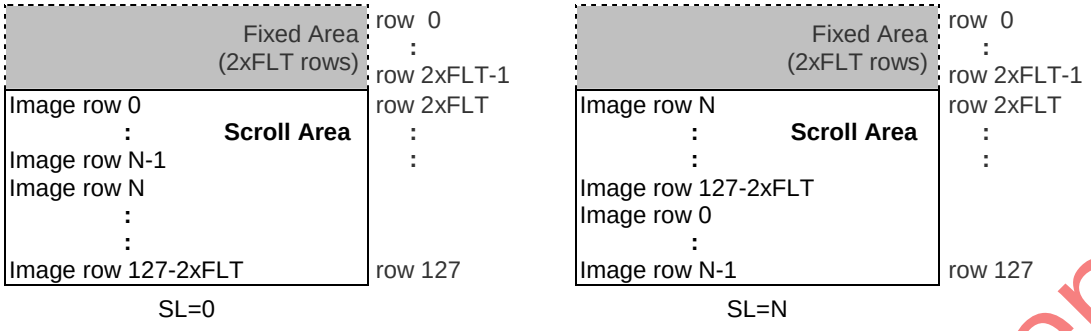
For UltraChip only. Please do NOT use.

(9) SET SCROLL LINE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[6:4]	0	0	**0**	**1**	**0**	**1**	**-**	SL6	SL5	SL4

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 127-2x(FLT+FLB) (full scrolling). FLT and FLB are the register values programmed by `Set Fixed Lines` command.



(10) SET PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address PA [3:0]	0	0	**0**	**1**	**1**	**0**	PA3	PA2	PA1	PA0
Set Page Address PA [4]	0	0	**0**	**1**	**1**	**1**	**-**	**-**	**-**	PA4

Set SRAM Page Address for read/write access. Possible value = **0**~31. UC1618t can store 2 B/W mode pictures in SRAM. Set PA[4] to specify which one to store. (Also refer to command "Set Display Mode".)

When DC[4:3]=10b
PA[4] : used to select Write Pattern 0 or 1
PA[3:0] : set SRAM page address

When DC[4:3] not = 10b
PA[4:0] : set SRAM page address

(11) SET V_{BIAS} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0] (Double-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: **0 ~ 255**

(12) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [9]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	**0**	LC9

This command is used to enable partial display function.

LC[9]	Partial Display function	Mux-Rate
0b	**Disable**	= CEN+1 (DST, DEN not used.)
1b	Enable	= DEN-DST+1+LC[0] x (FLT+FLB) x 2

(13) SET COM SCAN FUNCTION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set COM Scan Function CSF[0]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	**1**	CSF0

CSF[0]	COM scan function
0b	**Interlace scan**
1b	Progressive Scan

(14) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/page wrap around.
0: CA or PA (depends on AC[1]= 0 or 1) will stop increasing after reaching boundary
1: CA or PA (depends on AC[1]= 0 or 1) will restart, and PA or CA will increase by one.

AC[1]: Auto-Increment order
0 : column (CA) increase (+1) first until CA reaches CA boundary, then PA will increase by (+/-1).
1 : page (PA) increase (+/-1) first until PA reach PA boundary, then CA will increase by (+1).

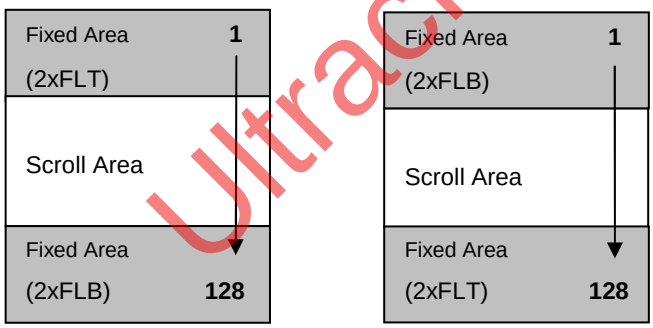
AC[2]: RID, Page Address (PA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, PID controls whether Page Address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and PA. When Window Program is enabled (AC[3]=ON), see Command Description (34) ~ (37) for more details. When Window Program is disabled (AC[3]=OFF), the behavior of CA, PA auto-increment is the same as WPC[1:0] and WPP[1:0] values are the default values and AC[3]=ON.

(15) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines {FLT,FLB} (Double-byte command)	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
	0	0	FLT[3:0]				FLB[3:0]			

The fixed line function is used to implement the partial scroll function by dividing the screen into Scroll and Fixed areas. The `Set Fixed Lines` command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFLT and bottom 2xFLB rows for mirror Y (MY) is 0, or covers the top 2xFLB and bottom 2xFLT rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



MY = 0 MY = 1

When partial display mode is activated, the display of these 2x(FLT+FLB) lines is also controlled by LC[0]. Before turning on LC[0], please make sure:

MY=0 DST >= FLTx2
DEN <= (CEN-FLBx2).

MY=1 DST >= FLBx2
DEN <= (CEN-FLTx2)

(16) SET DISPLAY MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Mode DC [5:4]	0	0	**1**	**0**	**0**	**1**	**0**	**1**	DC5	DC4

This command is enabled only when on/off mode. UC1618t can store 2 B/W mode pictures in SRAM. Set DC[5] to specify which one to display. (Also refer to command "Set Page Address".)

DC[4]: Input type for On/off mode
0b: 2 bits per pixel 1b: 1 bit per pixel
DC[5]: Display Pattern selection (enabled only when DC[4]=1)
0b: Pattern 0 1b: Pattern 1

(17) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC4	LC3

Program LC [4:3] for line rate setting (Line-Rate = Frame-Rate x Mux-Rate). The line rate is automatically scaled down by 2/3, 1/2, 1/3 and 1/4 at Mux-Rate = 85, 64, 43, and 32.

LC [4:3]	Line rate	
	when Mux Rate = 86~128	On/Off mode
00b	14.1 Klps	6.9 Klps
01b	17.4 Klps	8.5 Klps
10b	**20.8 Klps**	**10.2 Klps**
11b	25.4 Klps	12.5 Klps

(Klps: Kilo-Line-per-second)

(18) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(19) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

(20) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [3:2]	0	0	**1**	**0**	**1**	**0**	**1**	**1**	DC3	DC2

This command is for programming register DC[3:2].

When DC[2] is set to 0, the IC will put itself into Sleep mode. All drivers, voltage generation circuit, and timing circuit will be halted to conserve power. When any of the DC[2] bits is set to 1, UC1618t will first exit from Sleep Mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[3]: Gray Shade and B/W mode
0b: B/W Mode **1b: 4-Shade Mode**

For B/W mode, use data format for 4-shade-mode and UC1618t will convert them for B/W mode automatically.

Note : When the internal DC-DC converter starts to operate and pump out current to V_{LCD}, there will be an in-rush pulse current between V_{DD2} and V_{SS2} initially. To avoid this current pulse from causing potential harmful noise, do *NOT* issue any command or write any data to UC1618t for 5~10mS after setting DC[2] to 1.

(21) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	LC0

This command is used for programming LC[2:0] for COM (page) mirror (MY), SEG (column) mirror (MX).

LC2 controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

LC1 controls Mirror X (MX): MX is implemented by selecting the CA or 31-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

LC0 controls whether the soft icon section (0~ 2xFL) is display or not during partial display mode.

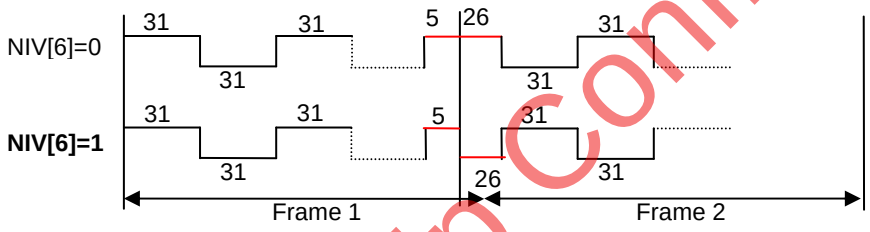
(22) SET N-LINE INVERSION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-Line Inversion NIV [6:0] (Double-byte command)	0	0	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
	0	0	**-**	NIV6	NIV5	NIV4	NIV3	NIV2	NIV1	NIV0

This command is used for programming NIV[6:0] for N-Line Inversion.

NIV[6]	Exclusive
0b	**no-XOR**
1b	XOR

NIV [5:0]	Inversion
000000b	**Disable Inversion Function**
000001b	Invert every 2 lines
:	:
111111b	Invert every 64 lines



(23) SET LCD GRAY SHADE 1

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Gray Shade LC[6:5]	0	0	**1**	**1**	**0**	**1**	**0**	**0**	LC6	LC5

This command sets gray scale register LC[6:5] to control the voltage RMS separation between gray shade levels “01” and “10”.

LC[6:5]	Gray-shade Level	Gray-shade Intensity Mapped
00b	1	9 (full range: 0~36)
01b	**2**	**12** (full range: 0~36)
10b	3	15 (full range: 0~36)
11b	4	21 (full range: 0~36)

(24) SET LCD GRAY SHADE 2

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Gray Shade LC[8:7]	0	0	**1**	**1**	**0**	**1**	**0**	**1**	LC8	LC7

This command sets gray scale register (LC[8:7]) to control the voltage RMS separation between gray shade levels “01” and “10”.

LC[8:7]	Gray-shade Level	Gray-shade Intensity Mapped
00b	3	15 (full range: 0~36)
01b	4	21 (full range: 0~36)
10b	**5**	**24 (full range: 0~36)**
11b	6	27 (full range: 0~36)

(25) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(26) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

(27) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
(double-byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Please do not use.

(28) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition:

00b = 6 01b = 9 10b = 10 **11b = 11**

(29) RESET CURSOR UPDATE MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Return the cursor. AC[4]=0, CA=CR	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

This command is used to reset cursor update mode function. It will clear cursor update mode flag (AC[4]=0), and CA will be restored to its previous value, which was stored in CR (via Set Cursor Update Mode command), and CA and PA increment will return to its normal condition.

(30) SET CURSOR UPDATE MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[4]=1, CR=CA	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**1**

Set Cursor Update mode is used to turn ON the Cursor Update mode function. AC[4] will be set to 1 and register CR will be set to the value of register CA.

When AC[4]=1, column address (CA) will only increase with write RAM operation but not on read RAM operation. The address CA wraps around will also be suspended no matter what WA setting is. The purpose of this combination of features is to support “Read-Modify-Write” for cursor implementation.

(31) SET COM END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
(double-byte command)	0	0	**-**	CEN [6:0] register parameter						

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-pages in the LCD. Default : **127**.

(32) SET DISPLAY START

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST (double-byte command)	0	0	1	1	1	1	0	0	1	0
	0	0	-	*DST [6:0]* register parameter						

This command programs the starting COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse. Default value :**0**.

(33) SET DISPLAY END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN (double-byte command)	0	0	1	1	1	1	0	0	1	1
	0	0	-	*DEN [6:0]* register parameter						

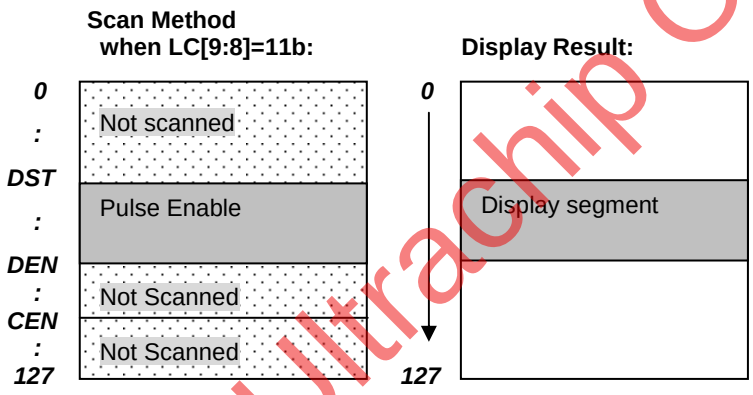
This command programs the ending COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse. Default value : **127**.

CEN, DST DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[9]=1b, the Mux-Rate is narrowed down to DEN-DST+1 + LC[0]x(FLT+FLB)x2. When MUX rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also requires BR and V_{LCD} to be readjusted. When Mux-Rate is under 33, it is recommend to set BR=6.

For minimum power consumption, set LC[9]=1b, set (DST, DEN, FLT, FLB, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use B/W mode, set PC[1:0]=00b, and use lowest BR and lowest V_{LCD} which satisfies the contrast requirement.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(34) SET WINDOW PROGRAM STARTING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 (Triple-byte command)	0	0	1	1	1	1	0	1	0	0
	0	0	*WPC0[7:0]* register parameter							
	0	0	-	-	-	-	-	-	-	WPC0[8]

This command is to program the starting column address of RAM program window.

(35) SET WINDOW PROGRAM STARTING PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 (double-byte command)	0	0	1	1	1	1	0	1	0	1
	0	0	-	*WPP0[6:0]* register parameter						

This command is to program the starting Page Address of RAM program window.

(36) SET WINDOW PROGRAM ENDING PAGE_C ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (Triple-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	*WPC1[7:0]* register parameter							
	0	0	-	-	-	-	-	-	-	WPC1[8]

This command is to program the ending column address of RAM program window.

(37) SET WINDOW PROGRAM ENDING PAGE ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	-	*WPP1[6:0]* register parameter						

This command is to program the ending Page Address of RAM program window.

(38) SET WINDOW PROGRAM ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[3]	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	AC3

This command is to enable the Window Program Function. Window Program Enable should always be reset when changing the window program boundary and then set right before starting the new boundary program.

Window Program Function can be used to refresh the RAM data in a specified window of SRAM address. When window programming is enabled, the CA and PA increment and wrap around will be automatically adjusted, and therefore allow effective data update within the window.

The direction of Window Program will depend on the WA (AC[0]), PID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting. WA decides whether the program RAM address advances to next page / column after reaching the specified window column / page boundary. PID controls the RAM address increasing from WPP0 toward WPP1 (PID=0) or reverse the direction (PID=1). Auto-increment order directs the RAM address increment vertically (AC[1]=1) or horizontally (AC[1]=0). MX results the RAM column address increasing from 127-WPC0 to 127-WPC1 (MX=1) or WPC0 to WPC1 (MX=0).

Display Data Direction	Function Setting			Image in Display Data Ram (Start : ●) (Physical origin: upper left corner)
	AIO AC[1]	MX LC[1]	RID AC[2]	
Normal	0	0	0	
Y-mirror	0	0	1	
X-mirror	0	1	0	
X-mirror Y-mirror	0	1	1	

- Serial Read Command (Enable only in S8/S9 mode):

(39) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**
	0	1	**0**	MX	MY	WA	DE	**0**	**0**	**0**
			Ver[1:0]		**0**	**0**	**0**	**0**	**0**	**0**
			Prod		PID	**0**	**0**	**0**	**0**	**0**

Please refer to command (3).

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1618t via registers CEN, DST, DEN, and partial display control LC[9:8].

Combined with low power partial display mode and a low bias ratio of 6, UC1618t can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$BR = V_{LCD}/V_{BIAS}$,
where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=128), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally cannot maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as the Mux Rate decreases, and the shades near the two ends of the spectrum will start to loose visibility.

UC1618t supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	6	9	10	11

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per °C	-0.05	-0.10	-0.15	-0.20

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[2].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\,\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in °C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

Gray shade LCD is sensitive to even a 1.5% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

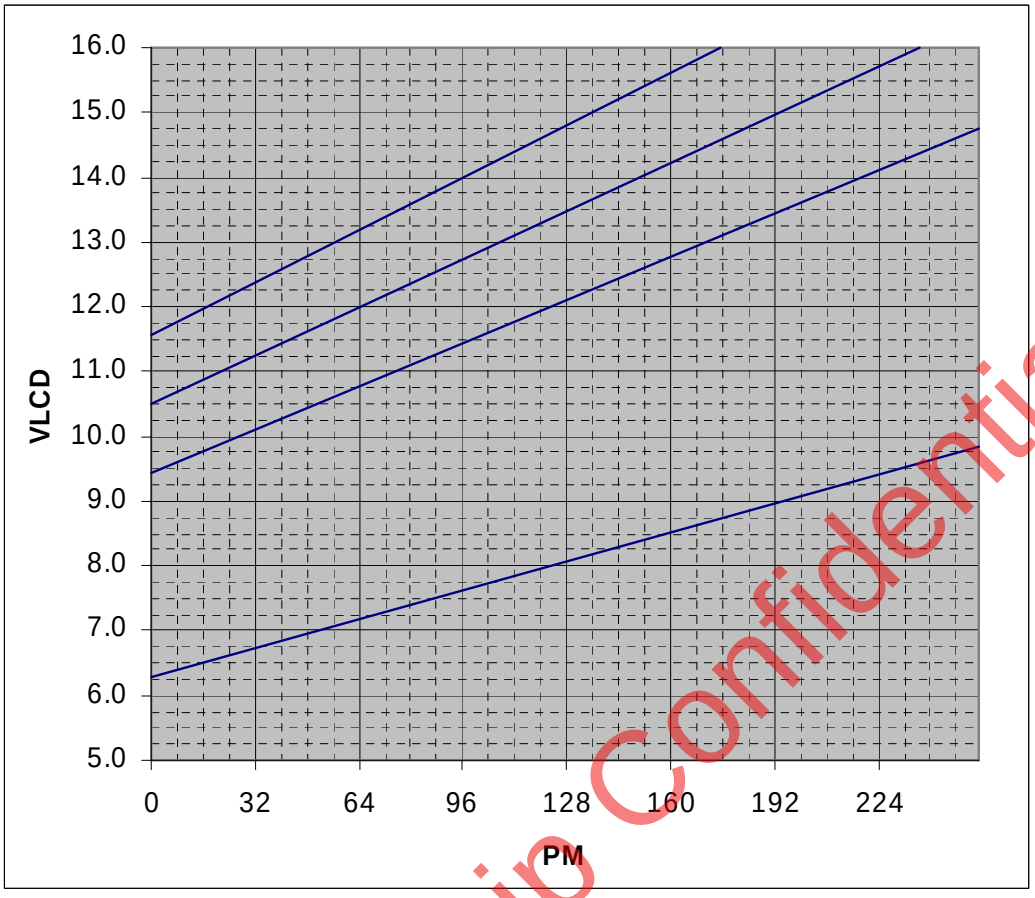
UC provides a V_{LCD} fine-tuning function by adding a variable resistor between Vr and Ground, ranging from 0Ω to 500KΩ. V_{LCD} adjustable range is ±3%. Yet, the result of V_R adjustment is still limited in between PM=0 ~ PM=255.

For the best results, software V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH

The power supply circuit of UC1618t is designed to handle LCD panels with load capacitance up to ~15nF when V_{DD2} = 2.7V. 15nF is also the recommended limit for LCD panel size for COG applications. For larger LCD panels, use higher V_{DD}.

V_{LCD} QUICK REFERENCE



V_{LCD} Relationship to BR and PM at 25 °C

BR	C_{V0} (V)	CPM (mV)	PM	V_{LCD} (V)
6	6.310	13.91	0	6.31
			255	9.86
9	9.458	20.82	0	9.46
			255	14.77
10	10.507	23.13	0	10.51
			237	15.99
11	11.549	25.43	0	11.55
			175	16.00

Note:

1. For good product reliability, keep $V_{LCD(MAX)}$ under **16.0V** under all operating temperature.
2. The integer values of BR above are for reference only and may have slight shift.
3. At 25 °C, V_{LCD} voltage has a ±1% output variation.

HI-V GENERATOR REFERENCE CIRCUIT

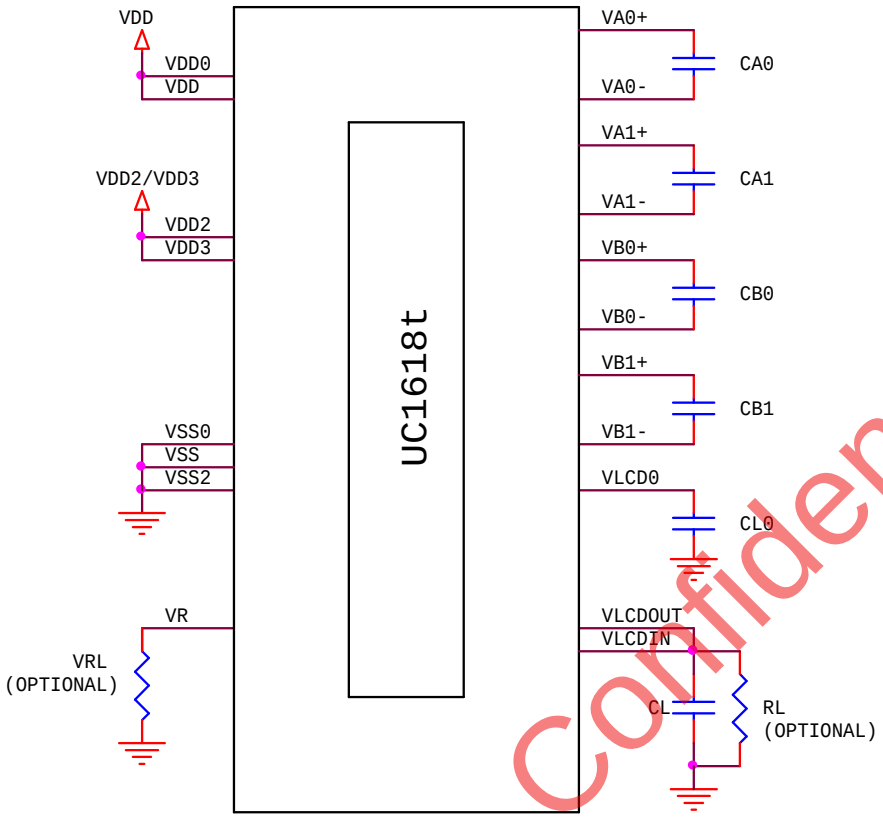


FIGURE 1: Reference circuit using internal Hi-V generator circuit

Sample component values:

CAX, CBX : For panels of 3-inch or smaller, use 2.2uF (5V) capacitor;
For panels bigger than 3 inches, use 5µF (5V) capacitor or higher.
(Capacitor size depends on panel capacitance loading and actual image performance.)

CL0: 1uF (25V) is appropriate for most applications.

CL: 330nF (25V) is appropriate for most applications.

RL: 3.3M Ω ~10M Ω to act as a draining circuit when V_{DD} is shut down abruptly.

VRL: 0~500 k Ω, for fine-tuning VLCD.

Note:

The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1618t contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 86, frame rate is calculated as:

Frame Rate = Line-Rate / Mux-Rate.

When Mux-Rate is lowered to 85, 64, 43 and 32, line rate will be scaled down by 1.5, 2, 3 and 4 times automatically to reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When fast LC material with ($t_r + t_f$) < 160mS is used, faster line rate may be required under 4-shade mode to maintain good contrast ratio at operating temperature >50^{o}C.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When COM drivers are in idle mode, their outputs are high-impedance (open circuit). When SEG drivers are in idle mode, their outputs are shorted to V_{SS}.

DRIVER ARRANGEMENTS

The naming conventions are: COM(x), where x=1~128, refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via the `Set Display Enable` command. When DC[2] is set to OFF (logic “0”), both COM and SEG drivers will become idle and UC1618t will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”, and UC1618t will first exit from Sleep Mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

Control register FL specifies a region of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. The FL register can be used to implement fixed region when the other part of the display is scrolled by SL.

PARTIAL DISPLAY

UC1618t provides flexible control of Mux Rate and active display area. Please refer to related Command Description for more detail.

GRAY-SHADE MODULATION

UC1618t uses a proprietary line rate modulation scheme to generate 8 levels of gray shade. The relative levels of the gray shades can be programmed by setting register bit LC[7:5]. It controls the relative position of the light gray and dark gray shades. For detailed value, please refer to the register definition table.

ITO LAYOUT CONSIDERATIONS

Since the COM scanning pulses of UC1618t can be as short as 30µS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

For COG applications, low resistance ITO glass will help reduce SEG signal RC decay, minimize V_{DD}, V_{SS} noise, and ensure sufficient V_{DD2}, V_{SS2} supply for on-chip DC-DC converter.

COM TRACE

Excessive RC decay of COM scanning pulse can cause fluctuation of contrast and increase the crosstalk of COM direction.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 1.8\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

(Use worst case values for all calculations)

In addition, please limit the min-max spread of RC decay to be:

$$| RC_{MAX} – RC_{MIN} | < 0.44\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

SEG TRACE

Excessive RC decay of SEG signal can cause image dependent changes of medium gray shades and sharply increase the crosstalk of SEG direction.

To minimize crosstalk, please limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.5\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD}/#_column, where C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too high, image contrast will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, visibility of shades will suffer, and crosstalk may increase sharply for medium shades.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10}) / V_{10} = (V_{ON}-V_{OFF}) / V_{OFF} \times 0.72\sim0.80$$

where V_{90} and V_{10} are the LC characteristics. V90 and V10 refers to the applied voltage required to achieve 90% and 10% of the ultimate transmission at saturating voltages respectively.and

V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/128	1/11	8.98%	7.2%	6.5%
1/128	1/10	8.79%	7.0%	6.3%

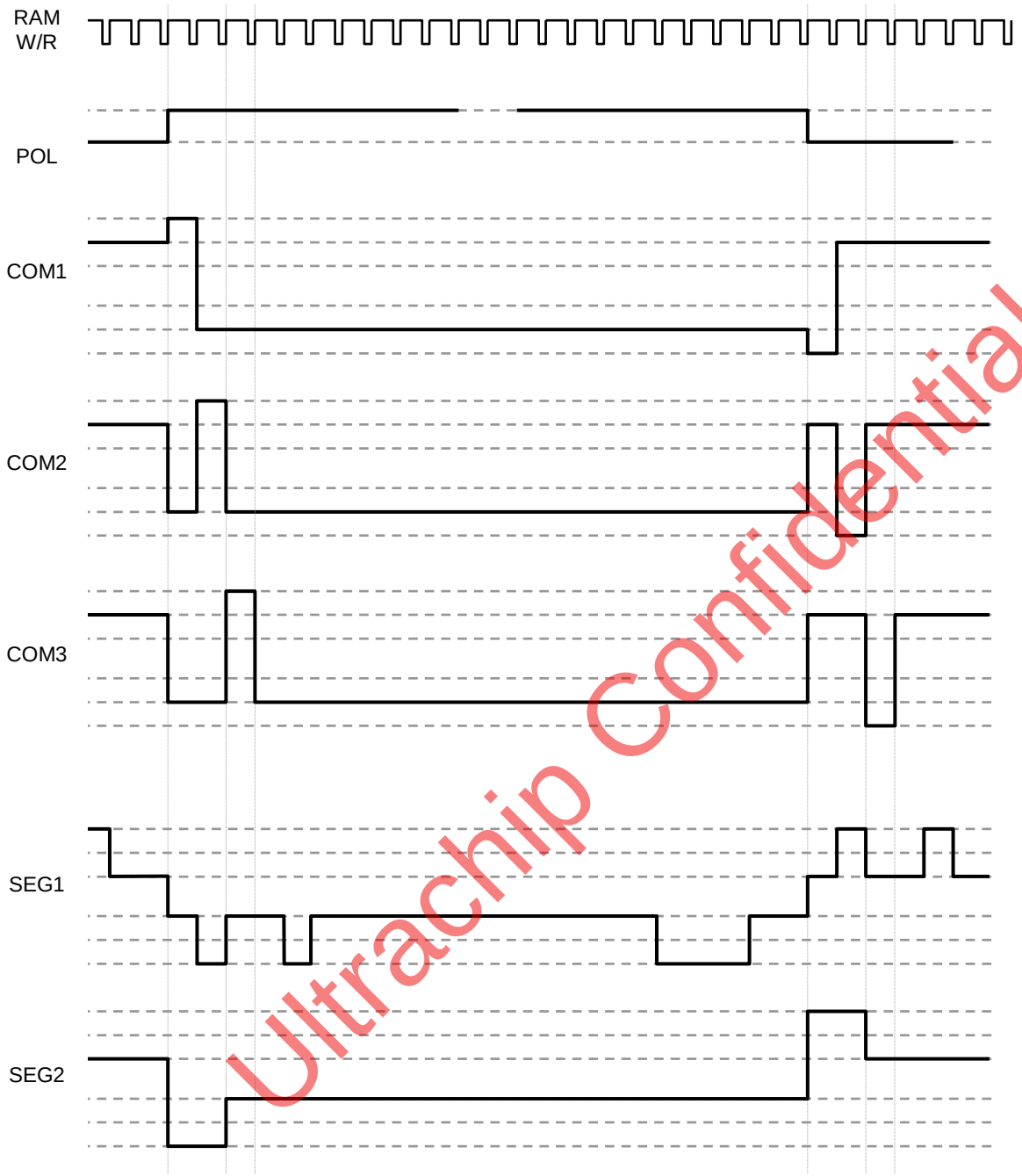


FIGURE 2: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1618t supports 2 parallel bus protocols in 16-bit and 8-bit bus widths, and 2 serial bus protocols.

Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

		Bus Type					
		Parallel				Serial	
		8080		6800		S8 (4-wire)	S9 (3-wire)
Width		16-bit	8-bit	16-bit	8-bit	–-	
Access		Read (data and status) / Write				Read status / Write	
Control & Data Pins	BM[1:0]	10	00	11	01	00	01
	D[15]	Data	0	Data	0	1	1
	CS[1:0]	Chip Select					
	CD	Control/Data					–
	WR0	$\overline{WR}$		R/$\overline{W}$		0	
	WR1	$\overline{RD}$		EN		0	
	D[14:8]	Data	–	Data	–	–	
	D[7:4]	Data		Data		–	
	D[3:0]	Data		Data		D3=SDA, D0=SCK	

* Connect unused control pins and data bus pins to V_{SS}.

Table 3: Host interfaces Choices

PARALLEL INTERFACE

The timing relationship between UC1618t internal control signals, RD and WR, and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, by either `Set CA`, or `Set PA` command, a dummy read cycle need to be performed before the actual data can propagate through the pipe-line and be read from data port D[15].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

16-/8-BIT BUS OPERATION

UC1618t supports both 16-bit and 8-bit bus width.

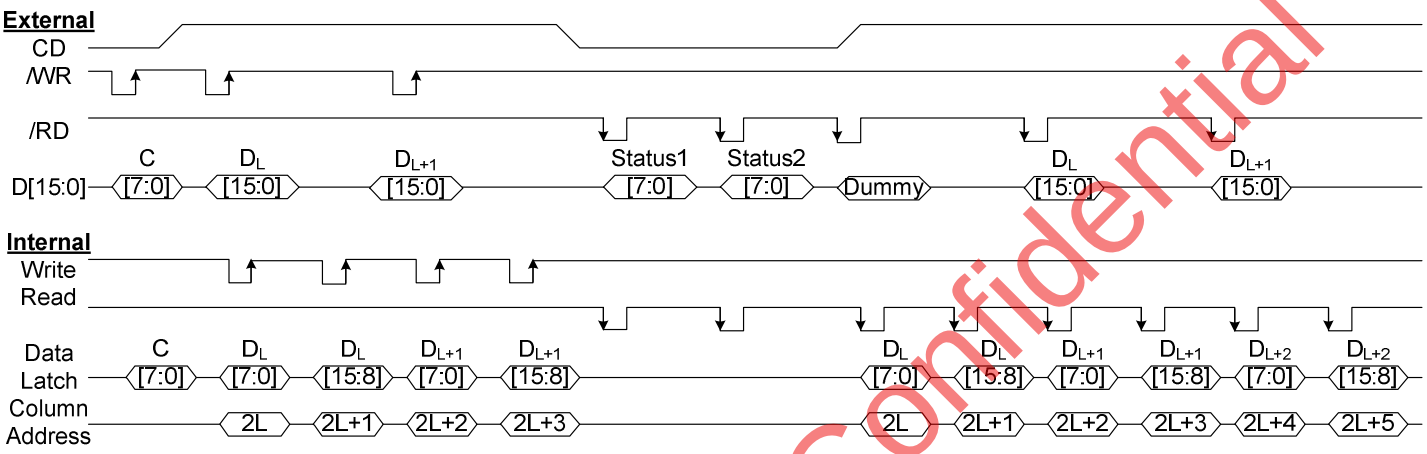


FIGURE 3.a: 16-bit Parallel Interface & Related Internal Signals

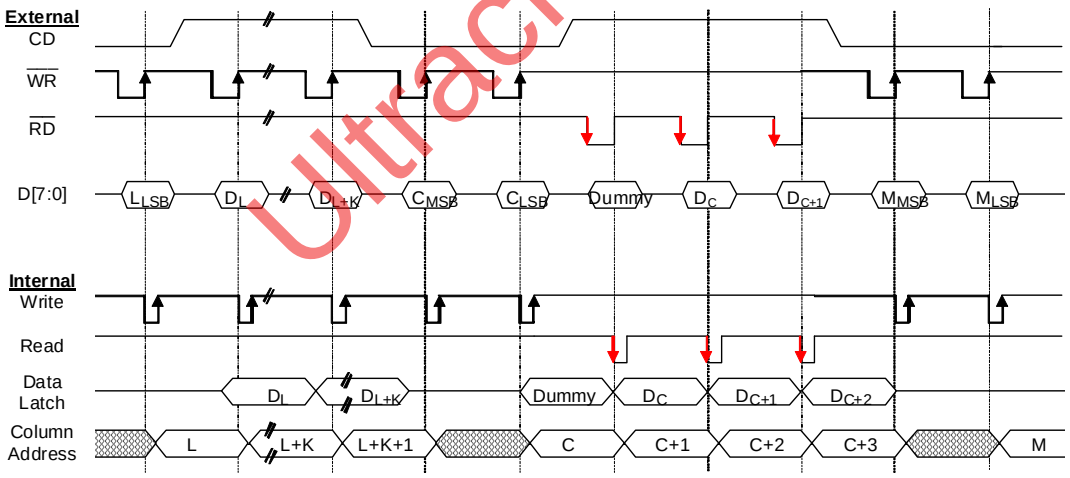


FIGURE 3.b: 8-bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1618t supports 2 serial modes, a 4-wire SPI mode (S8) and a compact 3-wire mode (S9). Bus interface mode is determined by the wiring of the BM[1:0] and D[15]. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Read status and write operations are supported in 4-wire serial mode. Pin CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

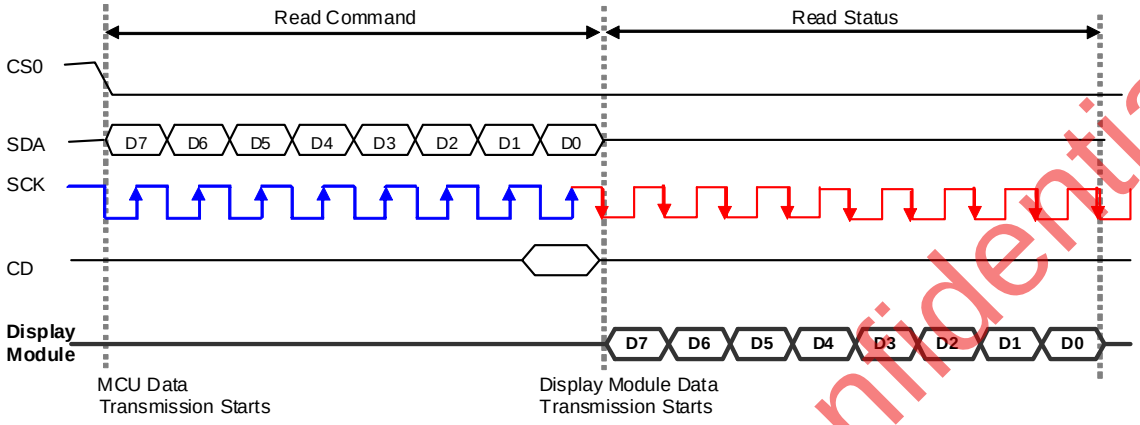


FIGURE 4.a: 4-wire Serial Interface (S8) – Read

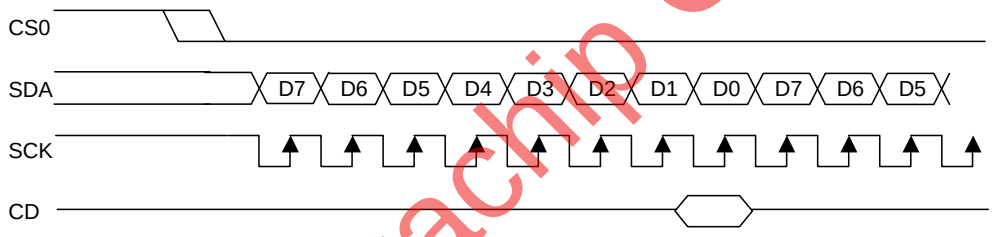


FIGURE 4.b: 4-wire Serial Interface (S8) – Write

S9 (3-WIRE) INTERFACE

Read status and write operations are supported in this 3-wire serial mode. Pin CS[1-0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command/data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 or CS1 for each byte of data/command is recommended but optional.

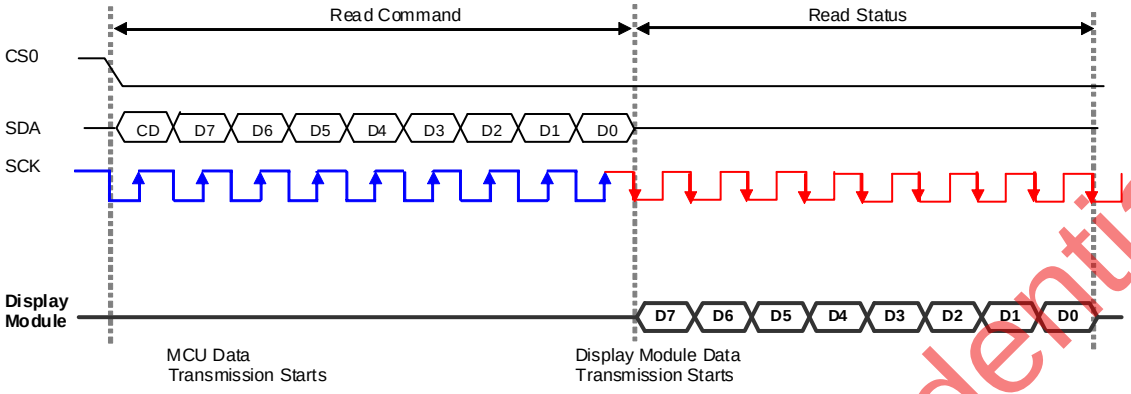


FIGURE 5.a: 3-wire Serial Interface (S9) – Read

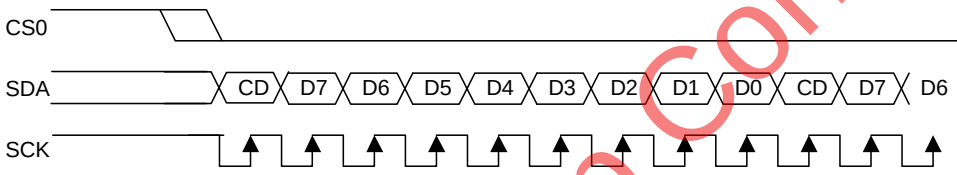


FIGURE 5.b: 3-wire Serial Interface (S9) – Write

HOST INTERFACE REFERENCE CIRCUIT

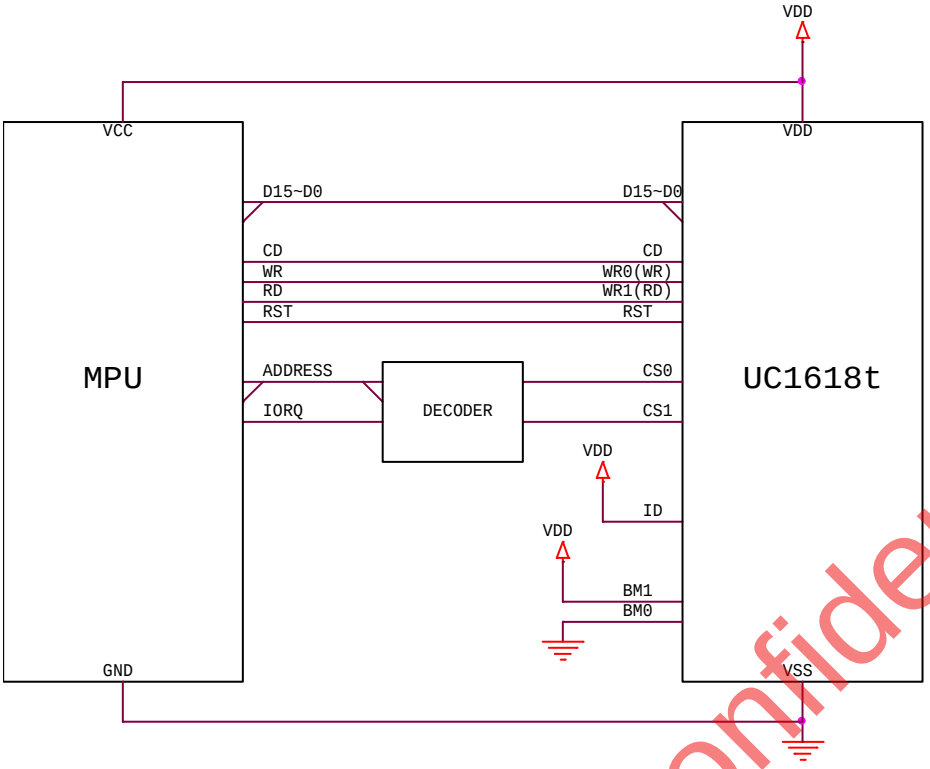


FIGURE 6: 8080/16-bit parallel mode reference circuit

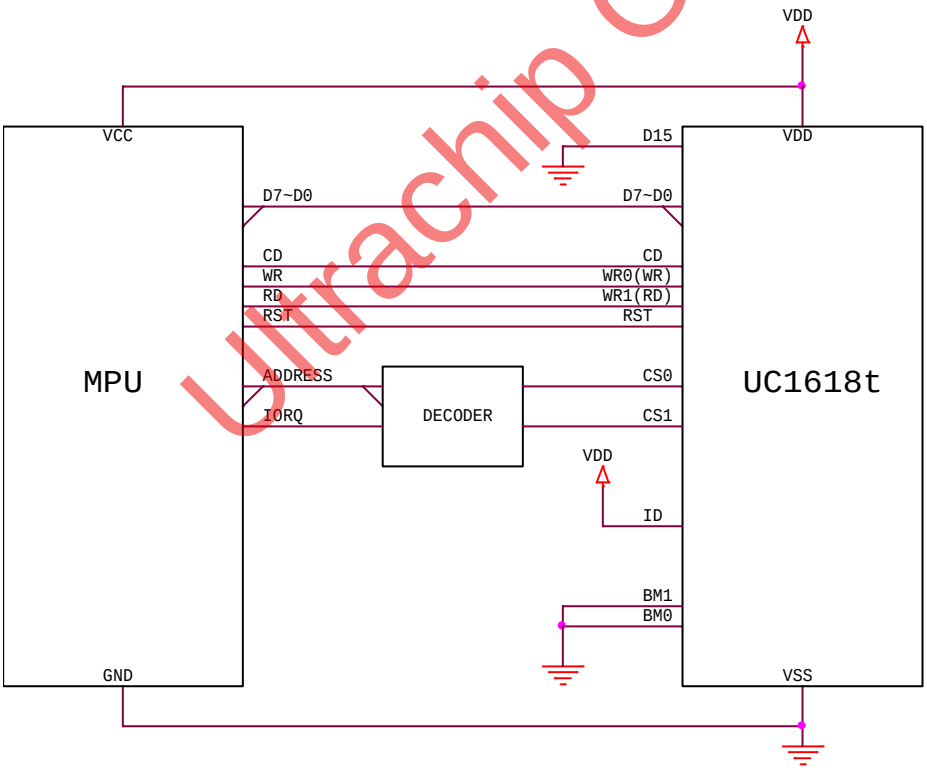


FIGURE 7: 8080/8-bit parallel mode reference circuit

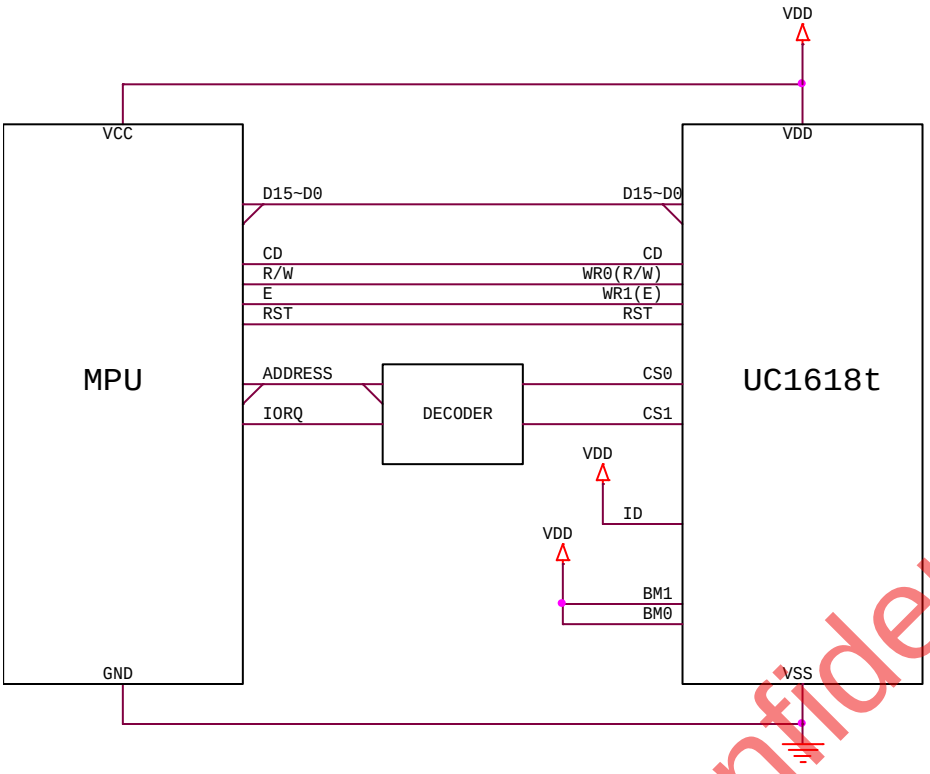


FIGURE 8: 6800/16-bit parallel mode reference circuit

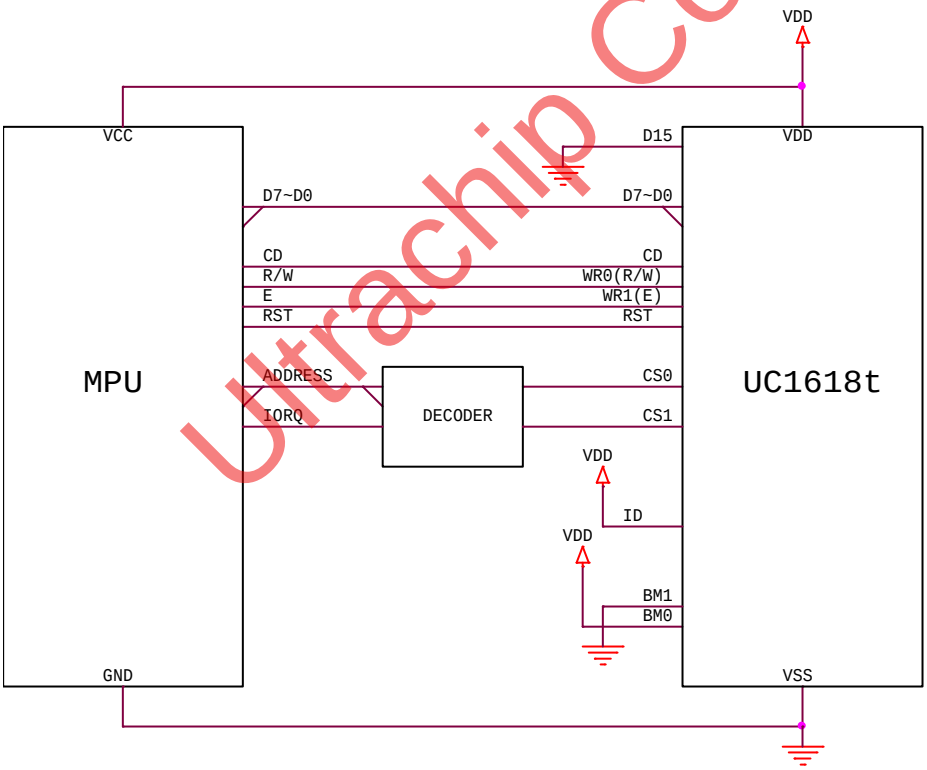


FIGURE 9: 6800/8-bit parallel mode reference circuit

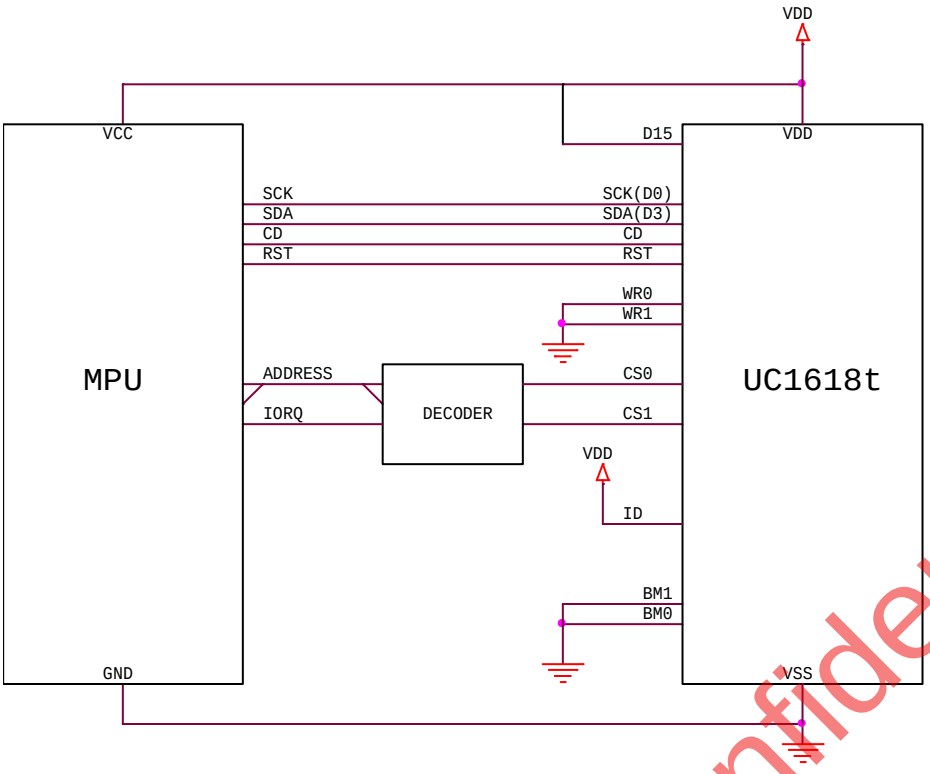


FIGURE 10: 4-Wire SPI (S8) serial mode reference circuit

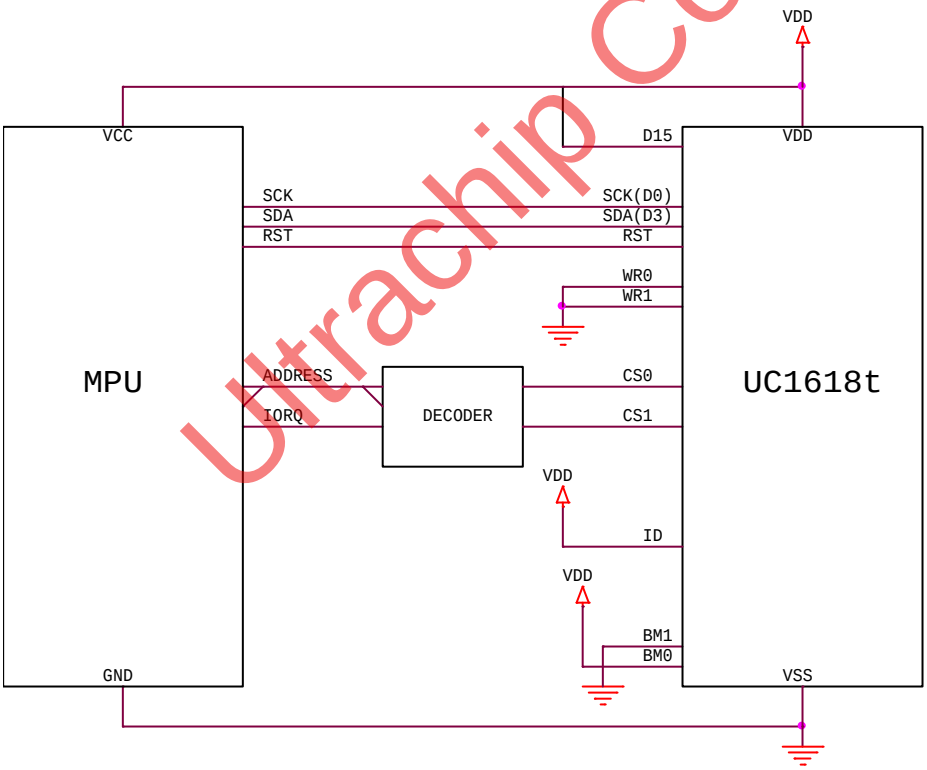


FIGURE 11: 3-Wire SPI (S9) serial mode reference circuit

Note:

1. When using Read function:

(8080) Set WR1=0 (6800) Set WR1=1 → data output will be enabled. (Serial) Set SCK=0	(8080) Set WR1=1 (6800) Set WR1=0 → data output will be disabled. (Serial) Set SCK=1

2. It is REQUIRED to set MPU's data port to 1 before Data Read or Status Read actions.

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data is stored to a dual port static RAM (RAM, for Display Data RAM) organized as 128x268x2.

After setting CA and PA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and page data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing `Set Page Address` and `Set Page_C Address` commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the end of row (127), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of row, CA will be reset to 0 and PA will increase or decrease, depending on the setting of row Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 127), PA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (267–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FLT & FLB) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FLT & FLB=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *SL*

Otherwise
Line = Mod(*Line*+1, 128)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the “loop around” effect as it effectively resets *Line* to 0 when *Line+1* reaches *128*. Effects such as row scrolling, row swapping can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(*SL + MUX-1*, *128*)
where MUX = CEN + 1

Otherwise
Line = Mod(*Line-1* , *128*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

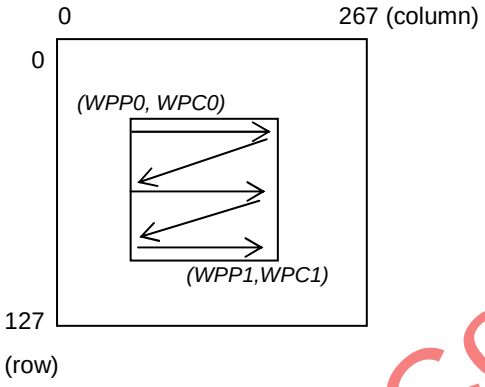
WINDOW PROGRAM

Window program is designed for data write in a specified window range of SRAM address. The procedure should start with window boundary registers setting (*WPP0*, *WPP1*, *WPC0* and *WPC1*) and then enable AC[3]. After AC[3] sets, data can be written to SRAM within the window address range which is specified by (*WPP0, WPC0*) and (*WPP1, WPC1*). AC[3] should be cleared after any modification of window boundary registers and then set again in order to initialize another window program.

The data write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data write can be consecutive within the range of the specified window. AC[1] will control the data write in either column or page direction. AC[2] will result the data write starting either from row *WPP0* or WPP1. MX is for the initial column address either from *WPC0* to *WPC1* or from (*MC-WPC0* to *MC-WPC1*).

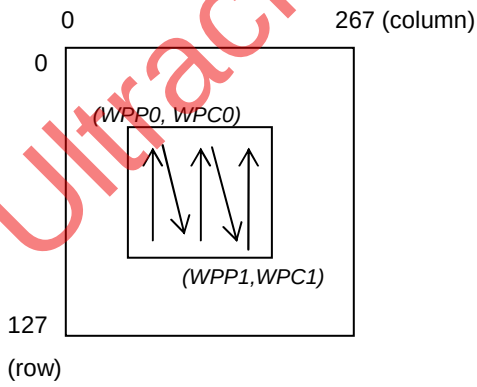
Example1: AC[2:0] = 001, MX=0

(PA auto INCREASING, COLUMN increasing first, auto wrap around, Mirror-X OFF)



Example 2: AC[2:0] = 111 MX = 0

(PA auto DESCREASING, PAGE increasing first, auto wrap around, Mirror-X OFF)



For DC[4:3] = 01b (2-bit per pixel, 4-Shade mode)

Data	Line Addr	RAM	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
D1:0	00H	11 00 … Page0	R1	R113	R128	R16
D3:2	01H	10 11 … Page0	R2	R114	R127	R15
D5:4	02H	01 10 … Page0	R3	R115	R126	R14
D7:6	03H	00 01 … Page0	R4	R116	R125	R13
D1:0	04H	… Page1	R5	R117	R124	R12
D3:2	05H	… Page1	R6	R118	R123	R11
D5:4	06H	… Page1	R7	R19	R122	R10
D7:6	07H	… Page1	R8	R120	R121	R9
D1:0	08H	… Page2	R9	R121	R120	R8
D3:2	09H	… Page2	R10	R122	R119	R7
D5:4	0AH	… Page2	R11	R123	R118	R6
D7:6	0BH	… Page2	R12	R124	R117	R5
D1:0	0CH	… Page3	R13	R125	R116	R4
D3:2	0DH	… Page3	R14	R126	R115	R3
D5:4	0EH	… Page3	R15	R127	R114	R2
D7:6	0FH	… Page3	R16	R128	R113	R1
…	…	…	…	…	…	…
D1:0	70H	… Page28	R113	R97	R16	R32
D3:2	71H	… Page28	R114	R98	R15	R31
D5:4	72H	… Page28	R115	R99	R14	R30
D7:6	73H	… Page28	R116	R100	R13	R29
D1:0	74H	… Page29	R117	R101	R12	R28
D3:2	75H	… Page29	R118	R102	R11	R27
D5:4	76H	… Page29	R119	R103	R10	R26
D7:6	77H	… Page29	R120	R104	R9	R25
D1:0	78H	… Paage30	R121	R105	R8	R24
D3:2	79H	… Paage30	R122	R106	R7	R23
D5:4	7AH	… Paage30	R123	R107	R6	R22
D7:6	7BH	… Paage30	R124	R108	R5	R21
D1:0	7CH	… Page31	R125	R109	R4	R20
D3:2	7DH	… Page31	R126	R110	R3	R19
D5:4	7EH	… Page31	R127	R111	R2	R18
D7:6	7FH	… Page31	R128	R112	R1	R17
						MUX=128

									…							
MX=0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	…			SEG265	SEG266	SEG267	SEG268
MX=1	SEG268	SEG267	SEG266	SEG265	SEG264	SEG263	SEG262	SEG261	…			SEG4	SEG3	SEG2	SEG1

Example: when MX=0, MY=0, SL=0, the corresponding data in SRAM as the pixels shown is:

For 8-bit bus width:

Page0, SEG1 : D[7:0] : 00011011b
Page0, SEG2 : D[7:0] : 01101100b

For 16-bit bus width:

Page0, SEG1 : D[7:0] : 00011011b
Page0, SEG2 : D[15:8] : 01101100b

For DC[4:3] = 10b (1-bit per pixel, B/W mode)

Data	Line Addr	RAM	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
D0	00H	Page0	R1	R113	R128	R16
D1	01H		R2	R114	R127	R15
D2	02H		R3	R115	R126	R14
D3	03H		R4	R116	R125	R13
D4	04H		R5	R117	R124	R12
D5	05H		R6	R118	R123	R11
D6	06H		R7	R19	R122	R10
D7	07H		R8	R120	R121	R9
D0	08H	Page1	R9	R121	R120	R8
D1	09H		R10	R122	R119	R7
D2	0AH		R11	R123	R118	R6
D3	0BH		R12	R124	R117	R5
D4	0CH		R13	R125	R116	R4
D5	0DH		R14	R126	R115	R3
D6	0EH		R15	R127	R114	R2
D7	0FH		R16	R128	R113	R1
…	…	…	…	…	…	…
D0	70H	Page14	R113	R97	R16	R32
D1	71H		R114	R98	R15	R31
D2	72H		R115	R99	R14	R30
D3	73H		R116	R100	R13	R29
D4	74H		R117	R101	R12	R28
D5	75H		R118	R102	R11	R27
D6	76H		R119	R103	R10	R26
D7	77H		R120	R104	R9	R25
D0	78H	Page15	R121	R105	R8	R24
D1	79H		R122	R106	R7	R23
D2	7AH		R123	R107	R6	R22
D3	7BH		R124	R108	R5	R21
D4	7CH		R125	R109	R4	R20
D5	7DH		R126	R110	R3	R19
D6	7EH		R127	R111	R2	R18
D7	7FH		R128	R112	R1	R17
					MUX=128	

MX=0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8				SEG265	SEG266	SEG267	SEG268
MX=1	SEG268	SEG267	SEG266	SEG265	SEG264	SEG263	SEG262	SEG261				SEG4	SEG3	SEG2	SEG1

Example: when MX=0, MY=0, SL=0, the corresponding data in SRAM as the pixels shown is:

For 8-bit bus width:

Page0, SEG1 : D[7:0] : 00011011b
Page0, SEG2 : D[7:0] : 01101100b

For 16-bit bus width:

Page0, SEG1 : D[7:0] : 00011011b
Page0, SEG2 : D[15:8] : 01101100b

RESET & POWER MANAGEMENT

SYSTEM RESET

UC1618t can be reset with *System-Reset*, which can be activated either by software command or by connecting RST pin to ground.

RESET STATUS

When UC1618t enters RESET sequence:

- Operation mode will be "Reset"
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1618t has three operating modes (OM):
Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

Two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep Mode.

OM changes are synchronized with the edges of UC1618t internal clock. To ensure consistent system states, wait at least 10µS after `Set Display Enable` *or* `System Reset` commands.

Action	Mode	OM
Reset command RST_ pin pulled "L"	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1618t consumes very little energy in Sleep mode (typically under 2µA).

EXITING SLEEP MODE

UC1618t contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1618t internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

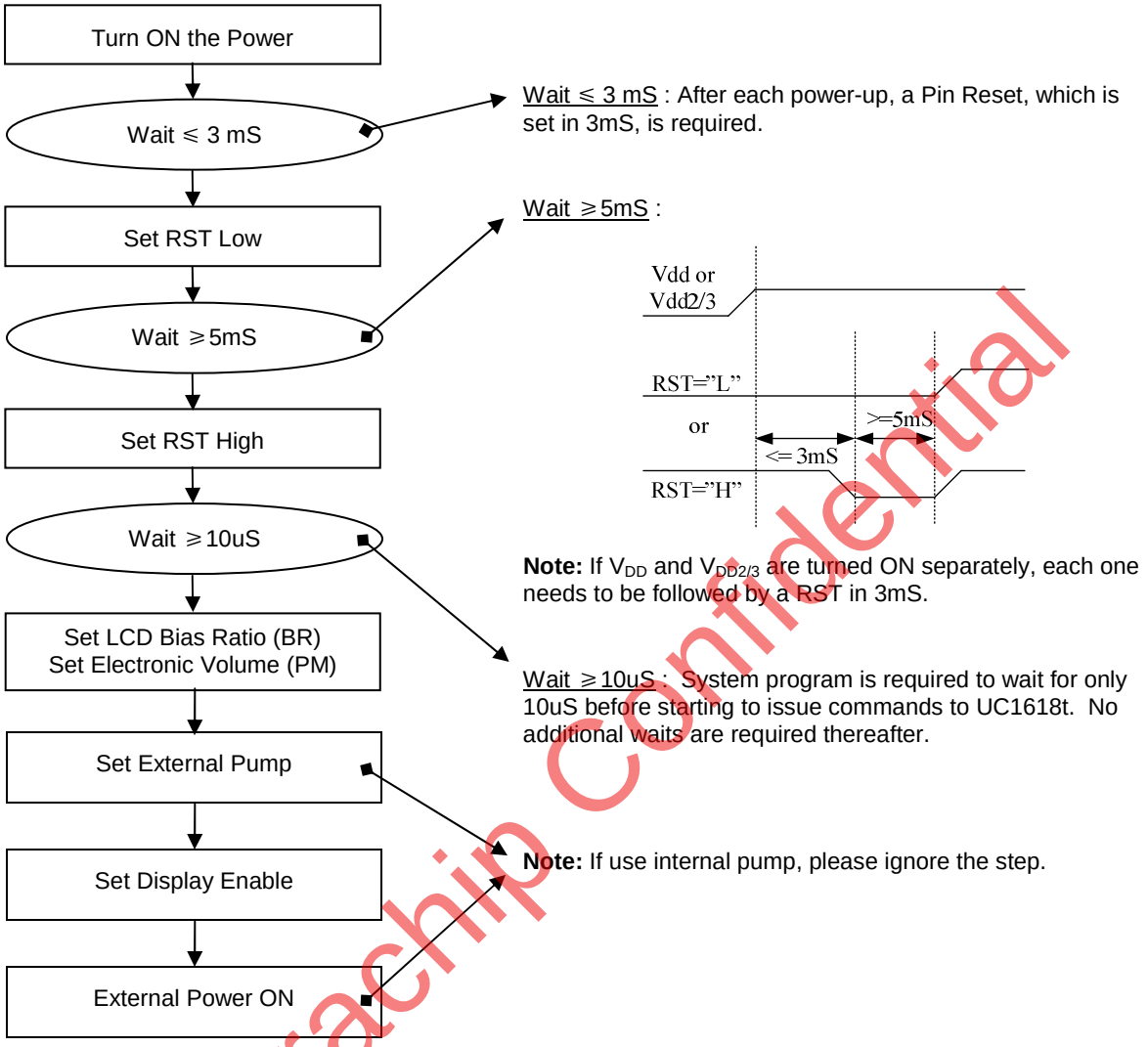


Figure 12: Reference Power-Up Sequence

There's no delay needed while turning ON V_{DD} and $V_{DD2/3}$, and either one can be turned on first:

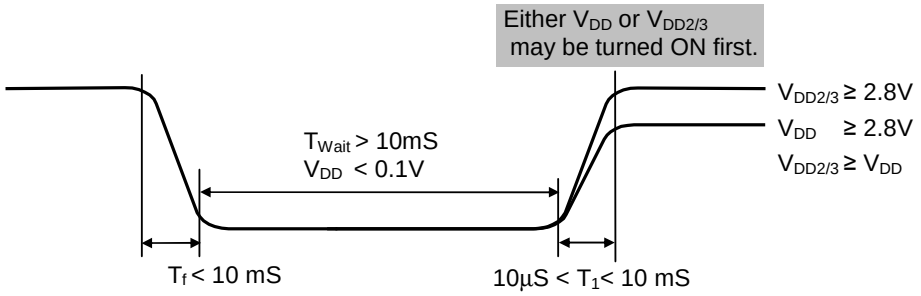
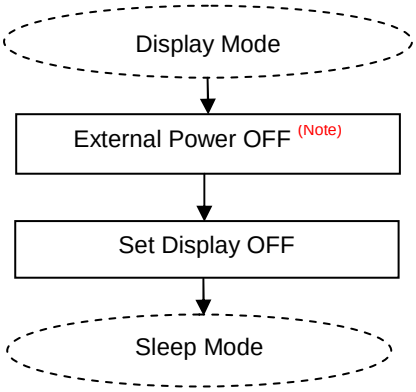


Figure 13: Power Off-On Sequence

ENTER/EXIT SLEEP MODE SEQUENCE

UC1618t enters Sleep mode from Display mode by issuing Set Display Disable command.



To exit Sleep mode, issue Set Display Enable.

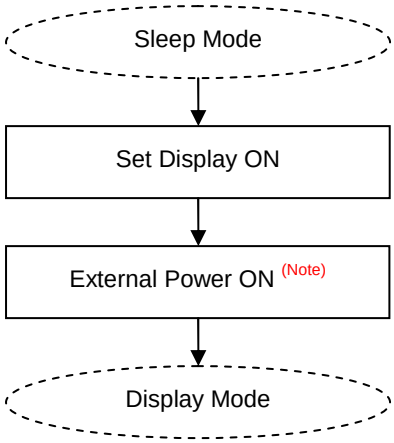


FIGURE 14: Reference Enter/Exit Sleep Mode Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitor C_L from causing abnormal residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

When internal V_{LCD} is not used, UC1618t will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

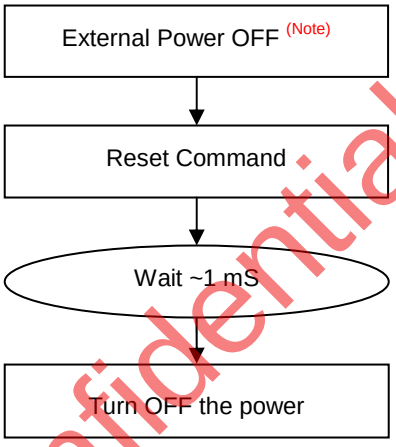


FIGURE 15: Reference Power-Down Sequence

Note: When using internal pump, ignore the "External Power OFF" step.

SAMPLE POWER MANAGEMENT COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

Type	Required:	These items are required
	Customized:	These items are not necessary if customer parameters are the same as default
	Advanced:	We recommend new users to skip these commands and use default values.
	Optional:	These commands depend on what users want to do.
C/D	The type of the interface cycle. It can be either Command (0) or Data (1)	
W/R	The direction of dataflow of the cycle. It can be either Write (0) or Read (1).	

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R	–	–	–	–	–	–	–	–	–	–	Wait ≤ 3mS	
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 5mS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	Wait 10uS after RST is High.
C	0	0	0	0	1	0	0	1	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	Set LCD Mapping	
C	0 0	0 0	0 1	0 1	1 1	1 1	0 1	0 0	0 1	0 0	Set APC0	EMI Enhancement
A	0	0	1	0	1	0	0	0	#	#	Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	0	1	0	1	#	#	Set Gray Shade	
C	0	0	1	1	1	0	1	0	#	#	Set Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set V_{BIAS} Potentiometer	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~1mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is therefore highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

Machine Mode		Human Body Mode	
V_{DD} mode	V_{SS} mode	V_{DD} mode	V_{SS} mode
200 V	200 V	4.0 KV	3.5 KV

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1 and 2.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.6	V
V_{LCD}	LCD Generated voltage (-40^{O}C ~ +95^{O}C)	-0.3	+19.8	V
V_{IN}	Digital input signal	-0.4	V_{DD} + 0.5	V
T_{OPR}	Operating temperature range	-40	+95	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Note:

1. V_{DD} is based on V_{SS} = 0V
2. Stress beyond ranges listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		2.7	2.8~3.3	3.6	V
$V_{DD2/3}$	Supply for bias & pump		2.7	2.8~3.3	3.6	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geqslant$ 2.7V, 25°C		14	16.0	V
V_D	LCD data voltage	$V_{DD2/3} \geqslant$ 2.7V, 25°C	0.89		1.78	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	µA
I_{SB}	Standby current	$V_{DD} = V_{DD2/3}$ = 3.3V, Temp = 95 °C			50	µA
C_{IN}	Input capacitance			5	10	pF
C_{OUT}	Output capacitance			5	10	pF
$R_{ON(SEG)}$	SEG output impedance	V_{LCD} = 16.0V		1.20	1.70	kΩ
$R_{ON(COM)}$	Upward COM output impedance	V_{LCD} = 16.0V		1.20	1.70	kΩ
f_{LINE}	Average Line rate	LC[4:3] = 10b	-10%	20.8	+10%	klps

POWER CONSUMPTION

V_{DD} = 2.7 V, Bias Ratio = 11b , PM = 195,
V_{LCD} = 16.51V, Line Rate = 20.8 Klps, Panel Loading = 20~40 nF,
Mux Rate = 128, Bus mode = 6800, C_L = 330nF,
C_B = 5µF, Temperature = 25°C, All HV outputs are open circuit.

Display Pattern	Conditions	Typical	Maximum	Unit
All-OFF	Bus = idle	1309	1964	µA
2-pixel checker	Bus = idle	1450	2175	µA
-	Reset (standby current)	< 3	10	µA

AC CHARACTERISTICS

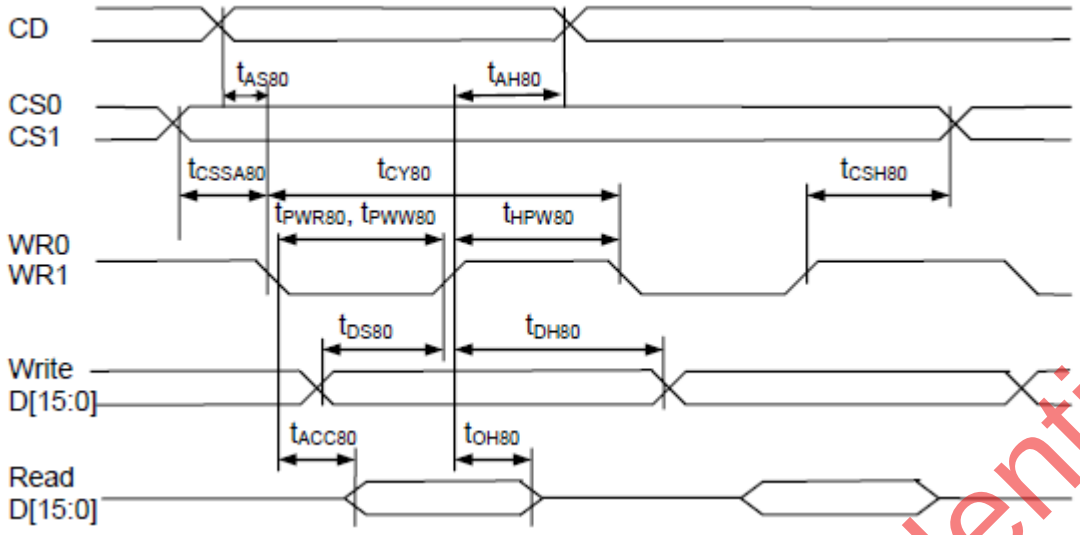


FIGURE 16: Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description		Condition	Min.	Max.	Unit
(2.7V ≤ V_{DD} ≤ 3.6V, Ta= –40 to +95°C)					(read / write)		
t_{AS80} t_{AH80}	CD	Address setup time Address hold time			15 20	–	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time Chip select hold time			5 5	–	nS
t_{CY80}	WR0, WR1	System cycle time	16-bit bus		530 / 450	–	nS
t_{PWR80}		Pulse width	16-bit bus		155 / --		
t_{PWW80}		Pulse width	16-bit bus		-- / 180		
t_{HPW80}		High pulse width	16-bit bus		345 / 240		
t_{CY80}		System cycle time	8-bit bus		350 / 280		
t_{PWR80}		Pulse width	8-bit bus		160 / --		
t_{PWW80}		Pulse width	8-bit bus		-- / 125		
t_{HPW80}		High pulse width	8-bit bus		160 / 125		
t_{DS80} t_{DH80}	Write D15~D0	Data setup time Data hold time			-- / 45 -- / 10	–	nS
t_{ACC80} t_{OD80}	Read D15~D0	Read access time Output disable time	16-bit bus 8-bit bus	C_L = 100pF	– / -- 100 / -- 100 / --	150 – –	nS

Note: tr (rising time), tf (falling time) : ≤ 15nS

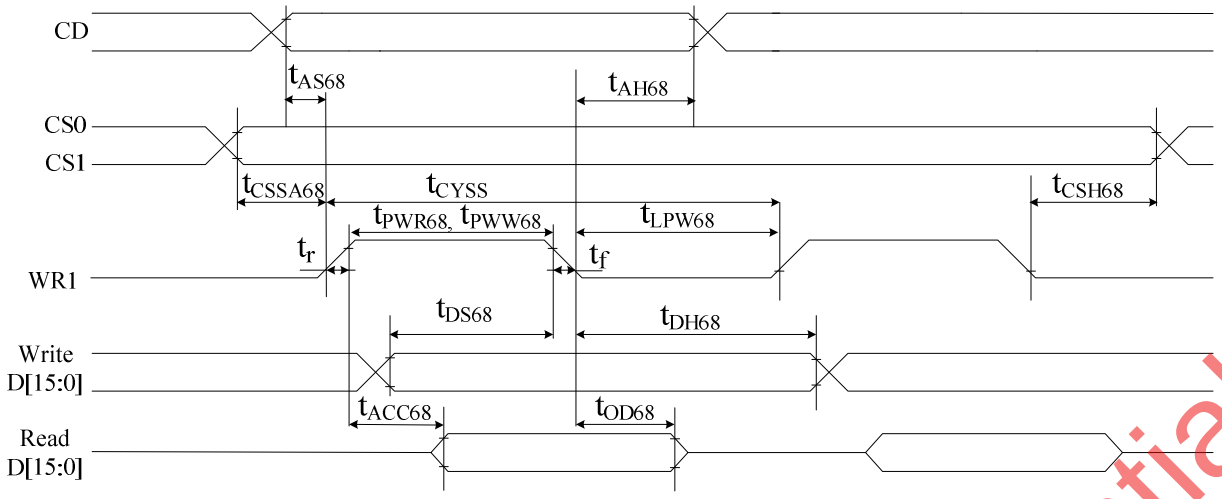


FIGURE 17: Parallel Bus Timing Characteristics (for 6800 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ≤ V_{DD} ≤ 3.6V, Ta= –40 to +95°C)				(read / write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		15 20	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CY68}	WR0, WR1	System cycle time 16-bit bus		530 / 450	–	nS
t_{PWR68}		Pulse width 16-bit bus		155 / --		
t_{PWW68}		Pulse width 16-bit bus		-- / 180		
t_{LPW68}		High pulse width 16-bit bus		345 / 240		
t_{CY68}		System cycle time 8-bit bus		350 / 280		
t_{PWR68}		Pulse width 8-bit bus		160 / –-		
t_{PWW68}		Pulse width 8-bit bus		–- / 125		
t_{LPW68}		High pulse width 8-bit bus		160 / 125		
t_{DS68} t_{DH68}	Write D15~D0	Data setup time Data hold time		-- / 45 -- / 10	–	nS
t_{ACC68} t_{OD68}	Read D15~D0	Read access time Output disable time 16-bit bus 8-bit bus	C_L = 100pF	– / -- 100 / -- 100 / --	150 – –	nS

Note: tr (rising time), tf (falling time) : ≤ 15nS

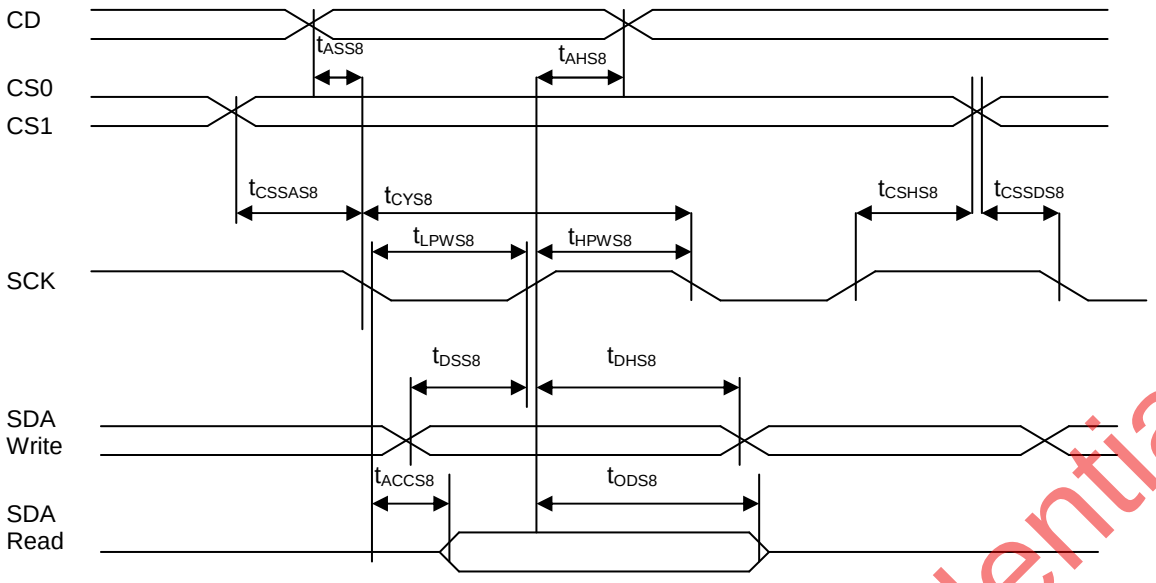


FIGURE 18: Serial Bus Timing Characteristics (for S8)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ⩽ V_{DD} ⩽ 3.6V, Ta= –40 to +95°C)				(read / write)		
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		30		
t_{CSSAS8}	CS1/CS0	Chip select setup time		5	–	nS
t_{CSHS8}		Chip select hold time		30		
t_{CYS8}	SCK	System cycle time		250 / 220	–	nS
t_{LPWS8}		Low pulse width		110 / 95		
t_{HPWS8}		High pulse width		110 / 95		
t_{DSS8}	SDA (Write)	Data setup time		-- / 25	–	nS
t_{DHS8}		Data hold time		-- / 30		
t_{ACCS8}	SDA (Read)	Read access time	C_L = 100pF	– / --	110	nS
t_{ODS8}		Output disable time		80 / --	–	

Note: tr (rising time), tf (falling time) : ⩽ 15nS

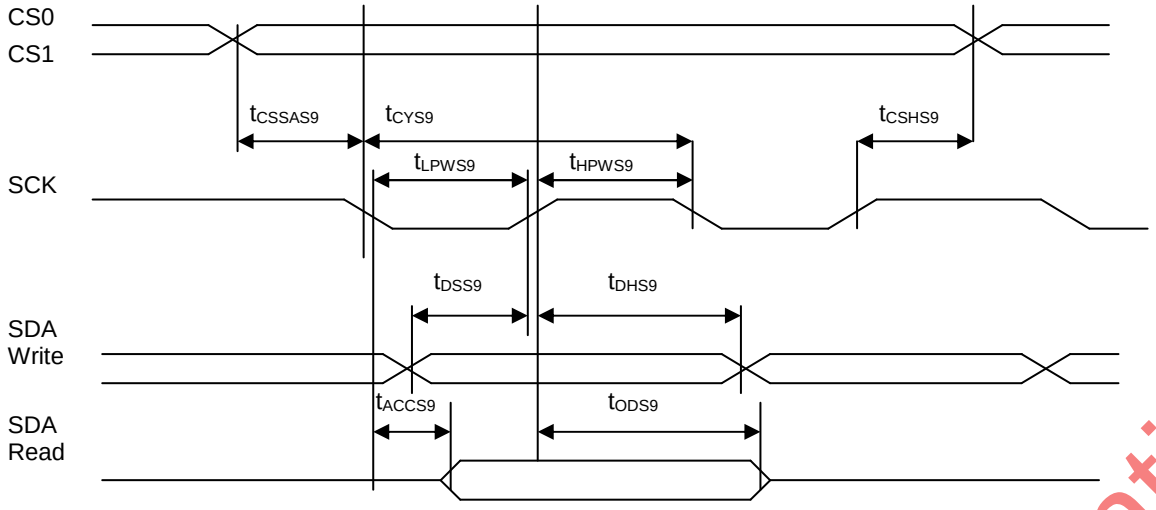


FIGURE 19: Serial Bus Timing Characteristics (for S9)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.7V ⩽ V_{DD} ⩽ 3.6V, Ta= –40 to +95°C)				(read / write)		
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time Chip select hold time		5 30	–	nS
t_{CYS9}	SCK	System cycle time		250 / 220	–	nS
t_{LPWS9}		Low pulse width		110 / 95		
t_{HPWS9}		High pulse width		110 / 95		
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		-- / 25 -- / 30	–	nS
t_{ACCS9} t_{ODS9}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / -- 80 / --	110 –	nS

Note: tr (rising time), tf (falling time) : ⩽ 15nS

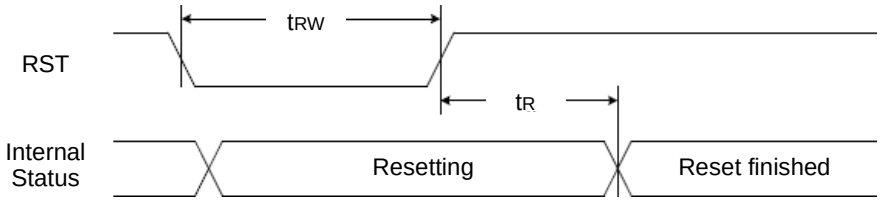
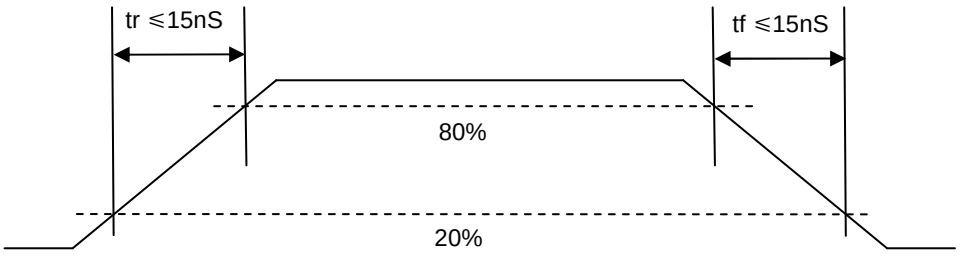


FIGURE 20: Reset Characteristics

Symbol	Signal	Description	Min.	Max.	Unit
(2.7V ⩽ V_{DD} ⩽ 3.6V, Ta= –40 to +95°C)					
t_{RW}	RST	Reset low pulse width	5	–	mS
t_R	RST, Internal Status	Reset to Internal Status pulse delay	10	–	uS
		Wait before Power Down	1	–	mS

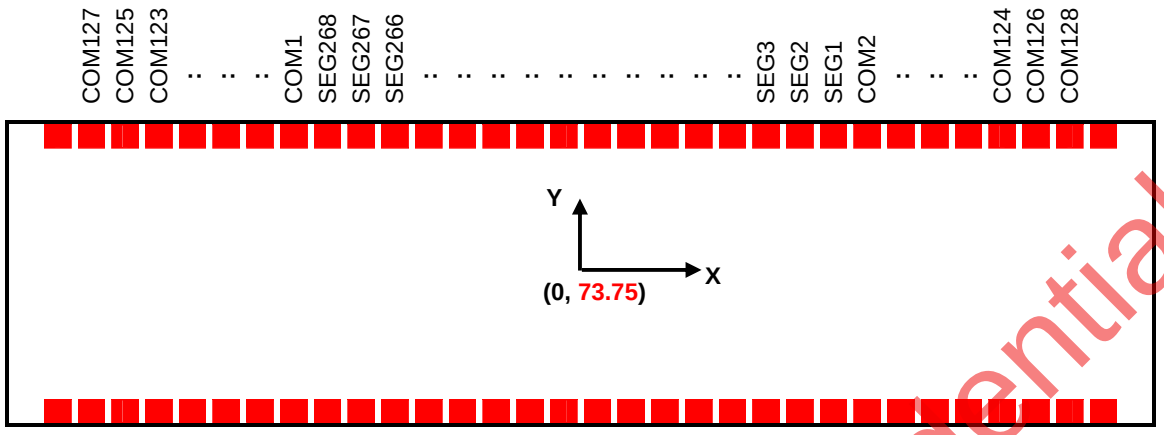
Note:

For each mode, the signal's rising and falling times (tr, tf) are stipulated to be equal to or less than 15nS each.



PHYSICAL DIMENSIONS

Circuit / Bump View:

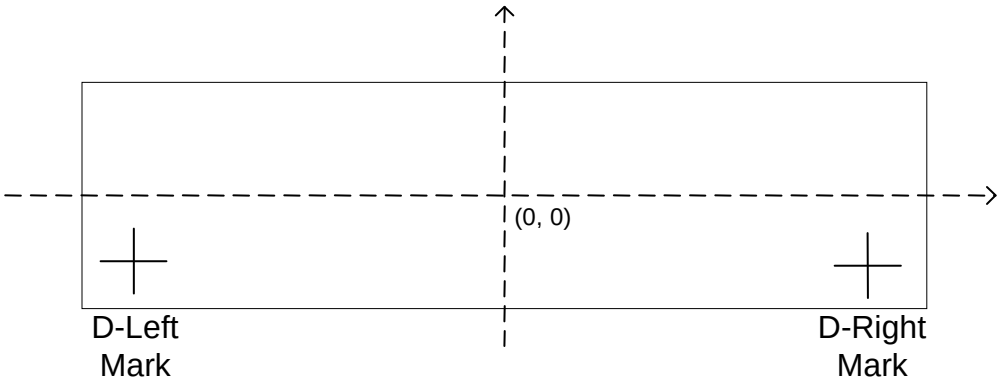


Die / Bump Information:

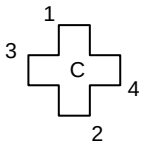
Die Size:	(9740µM ± 40µM) x (1096µM ± 40µM)
Die Thickness:	400µM ± 20µM
Die TTV:	$D_{MAX} – D_{MIN} \leqslant 2µM$
Hardness:	90Hv ± 25Hv
Bump Height:	15µM ± 3µM
	$H_{MAX} – H_{MIN} \leqslant 2µM$

Bump Size:	12µM x 150µM
Bump Pitch:	24µM
Bump Gap:	12µM
Shear force:	>5 g/mil^2
Coordinate origin:	(0, 0)
Chip center:	(0, 73.75)
Pad reference:	Pad center

ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

Alignment mark is on Metal4 under Passivation.

The "+" mark is symmetric both horizontally and vertically.

COORDINATES:

	D-Left Mark		D-Right Mark	
	X	Y	X	Y
1	-4620.5	-359.25	4600.5	-359.25
2	-4600.5	-419.25	4620.5	-419.25
3	-4640.5	-379.25	4580.5	-379.25
4	-4580.5	-399.25	4640.5	-399.25
C	-4610.5	-389.25	4610.5	-389.25

TOP METAL AND PASSIVATION:

Remark:
Alignment marks are on Metal4 under Passivation

PAD COORDINATES

#	PAD	X	Y	W	H
1	DUMMY	-4738	-377.75	65	103
2	D15	-4452.7	-388.025	69.1	82.45
3	vddx	-4371.15	-388.025	45	82.45
4	D14	-4289.6	-388.025	69.1	82.45
5	D13	-4204.5	-388.025	69.1	82.45
6	D12	-4119.4	-388.025	69.1	82.45
7	D11	-4034.3	-388.025	69.1	82.45
8	D10	-3949.2	-388.025	69.1	82.45
9	D9	-3864.1	-388.025	69.1	82.45
10	D8	-3779	-388.025	69.1	82.45
11	D7	-3693.9	-388.025	69.1	82.45
12	D6	-3608.8	-388.025	69.1	82.45
13	D5	-3523.7	-388.025	69.1	82.45
14	D4	-3438.6	-388.025	69.1	82.45
15	D3	-3353.5	-388.025	69.1	82.45
16	D2	-3268.4	-388.025	69.1	82.45
17	D1	-3183.3	-388.025	69.1	82.45
18	D0	-3098.2	-388.025	69.1	82.45
19	RST	-3007.85	-388.025	65.6	82.45
20	WR0	-2926.25	-388.025	65.6	82.45
21	vddx	-2846.45	-388.025	45	82.45
22	WR1	-2766.65	-388.025	65.6	82.45
23	CD	-2685.05	-388.025	65.6	82.45
24	CS0	-2603.45	-388.025	65.6	82.45
25	vddx	-2523.65	-388.025	45	82.45
26	CS1	-2443.85	-388.025	65.6	82.45
27	BM0	-2362.25	-388.025	65.6	82.45
28	vddx	-2282.45	-388.025	45	82.45
29	BM1	-2202.65	-388.025	65.6	82.45
30	VR	-2122.85	-388.025	45	82.45
31	VR	-2035.85	-388.025	65	82.45
32	TST2	-1811.5	-388.025	65	82.45
33	ID	-1718.45	-388.025	65.6	82.45
34	TST5	-1636.85	-388.025	65.6	82.45
35	vddx	-1560.05	-388.025	45	82.45
36	Vss0	-1500.05	-388.025	45	82.45
37	Vss0	-1440.05	-388.025	45	82.45
38	vss	-1380.05	-388.025	45	82.45
39	vss	-1320.05	-388.025	45	82.45
40	vss	-1260.05	-388.025	45	82.45
41	vss	-1200.05	-388.025	45	82.45
42	vss	-1140.05	-388.025	45	82.45
43	vss2	-967.35	-388.025	45	82.45
44	vss2	-907.35	-388.025	45	82.45
45	vss2	-847.35	-388.025	45	82.45
46	vss2	-787.35	-388.025	45	82.45
47	vss2	-727.35	-388.025	45	82.45
48	vss2	-667.35	-388.025	45	82.45
49	Vdd0	-607.35	-388.025	45	82.45

#	PAD	X	Y	W	H
50	Vdd0	-547.35	-388.025	45	82.45
51	vdd	-487.35	-388.025	45	82.45
52	vdd	-427.35	-388.025	45	82.45
53	vdd	-367.35	-388.025	45	82.45
54	vdd	-307.35	-388.025	45	82.45
55	vdd	-247.35	-388.025	45	82.45
56	DUMMY	-151.3	-388.025	45	82.45
57	DUMMY	-91.3	-388.025	45	82.45
58	DUMMY	-31.3	-388.025	45	82.45
59	DUMMY	28.7	-388.025	45	82.45
60	DUMMY	88.7	-388.025	45	82.45
61	DUMMY	148.7	-388.025	45	82.45
62	DUMMY	208.7	-388.025	45	82.45
63	DUMMY	268.7	-388.025	45	82.45
64	DUMMY	328.7	-388.025	45	82.45
65	DUMMY	388.7	-388.025	45	82.45
66	vdd2	448.7	-388.025	45	82.45
67	vdd2	508.7	-388.025	45	82.45
68	vdd2	568.7	-388.025	45	82.45
69	vdd2	628.7	-388.025	45	82.45
70	vdd2	688.7	-388.025	45	82.45
71	vdd2	748.7	-388.025	45	82.45
72	DUMMY	831.7	-388.025	45	82.45
73	DUMMY	891.7	-388.025	45	82.45
74	DUMMY	951.7	-388.025	45	82.45
75	DUMMY	1011.7	-388.025	45	82.45
76	vdd3	1100.5	-388.025	45	82.45
77	vdd3	1160.5	-388.025	45	82.45
78	VA0-	1233.6	-377.75	45	103
79	VA0-	1293.6	-377.75	45	103
80	VA0-	1427.6	-377.75	45	103
81	VA0-	1487.6	-377.75	45	103
82	VA1-	1551.6	-377.75	45	103
83	VA1-	1611.6	-377.75	45	103
84	VA1-	1745.6	-377.75	45	103
85	VA1-	1805.6	-377.75	45	103
86	VA1+	1869.6	-377.75	45	103
87	VA1+	1929.6	-377.75	45	103
88	VA1+	2063.6	-377.75	45	103
89	VA1+	2123.6	-377.75	45	103
90	VA0+	2187.6	-377.75	45	103
91	VA0+	2247.6	-377.75	45	103
92	VA0+	2381.6	-377.75	45	103
93	VA0+	2441.6	-377.75	45	103
94	VB0-	2505.6	-377.75	45	103
95	VB0-	2565.6	-377.75	45	103
96	VB0-	2699.6	-377.75	45	103
97	VB0-	2759.6	-377.75	45	103
98	VB1-	2823.6	-377.75	45	103

#	PAD	X	Y	W	H
99	VB1-	2883.6	-377.75	45	103
100	VB1-	3017.6	-377.75	45	103
101	VB1-	3077.6	-377.75	45	103
102	VB1+	3141.6	-377.75	45	103
103	VB1+	3201.6	-377.75	45	103
104	VB1+	3335.6	-377.75	45	103
105	VB1+	3395.6	-377.75	45	103
106	VB0+	3459.6	-377.75	45	103
107	VB0+	3519.6	-377.75	45	103
108	VB0+	3653.6	-377.75	45	103
109	VB0+	3713.6	-377.75	45	103
110	VLCD0	3908.6	-377.75	65	103
111	VLCD0	4084.85	-377.75	45	103
112	VLCDOUT	4224.2	-377.75	65	103
113	VLCDIN	4481.2	-377.75	45	103
114	DUMMY	4738	-377.75	65	103
115	DUMMY	4764	355.25	12	150
116	COM128	4740	355.25	12	150
117	COM126	4716	355.25	12	150
118	COM124	4692	355.25	12	150
119	COM122	4668	355.25	12	150
120	COM120	4644	355.25	12	150
121	COM118	4620	355.25	12	150
122	COM116	4596	355.25	12	150
123	COM114	4572	355.25	12	150
124	COM112	4548	355.25	12	150
125	COM110	4524	355.25	12	150
126	COM108	4500	355.25	12	150
127	COM106	4476	355.25	12	150
128	COM104	4452	355.25	12	150
129	COM102	4428	355.25	12	150
130	COM100	4404	355.25	12	150
131	COM98	4380	355.25	12	150
132	COM96	4356	355.25	12	150
133	COM94	4332	355.25	12	150
134	COM92	4308	355.25	12	150
135	COM90	4284	355.25	12	150
136	COM88	4260	355.25	12	150
137	COM86	4236	355.25	12	150
138	COM84	4212	355.25	12	150
139	COM82	4188	355.25	12	150
140	COM80	4164	355.25	12	150
141	COM78	4140	355.25	12	150
142	COM76	4116	355.25	12	150
143	COM74	4092	355.25	12	150
144	COM72	4068	355.25	12	150
145	COM70	4044	355.25	12	150
146	COM68	4020	355.25	12	150
147	COM66	3996	355.25	12	150
148	COM64	3972	355.25	12	150

#	PAD	X	Y	W	H
149	COM62	3948	355.25	12	150
150	COM60	3924	355.25	12	150
151	COM58	3900	355.25	12	150
152	COM56	3876	355.25	12	150
153	COM54	3852	355.25	12	150
154	COM52	3828	355.25	12	150
155	COM50	3804	355.25	12	150
156	COM48	3780	355.25	12	150
157	COM46	3756	355.25	12	150
158	COM44	3732	355.25	12	150
159	COM42	3708	355.25	12	150
160	COM40	3684	355.25	12	150
161	COM38	3660	355.25	12	150
162	COM36	3636	355.25	12	150
163	COM34	3612	355.25	12	150
164	COM32	3588	355.25	12	150
165	COM30	3564	355.25	12	150
166	COM28	3540	355.25	12	150
167	COM26	3516	355.25	12	150
168	COM24	3492	355.25	12	150
169	COM22	3468	355.25	12	150
170	COM20	3444	355.25	12	150
171	COM18	3420	355.25	12	150
172	COM16	3396	355.25	12	150
173	COM14	3372	355.25	12	150
174	COM12	3348	355.25	12	150
175	COM10	3324	355.25	12	150
176	COM8	3300	355.25	12	150
177	COM6	3276	355.25	12	150
178	COM4	3252	355.25	12	150
179	COM2	3228	355.25	12	150
180	SEG1	3204	355.25	12	150
181	SEG2	3180	355.25	12	150
182	SEG3	3156	355.25	12	150
183	SEG4	3132	355.25	12	150
184	SEG5	3108	355.25	12	150
185	SEG6	3084	355.25	12	150
186	SEG7	3060	355.25	12	150
187	SEG8	3036	355.25	12	150
188	SEG9	3012	355.25	12	150
189	SEG10	2988	355.25	12	150
190	SEG11	2964	355.25	12	150
191	SEG12	2940	355.25	12	150
192	SEG13	2916	355.25	12	150
193	SEG14	2892	355.25	12	150
194	SEG15	2868	355.25	12	150
195	SEG16	2844	355.25	12	150
196	SEG17	2820	355.25	12	150
197	SEG18	2796	355.25	12	150
198	SEG19	2772	355.25	12	150

#	PAD	X	Y	W	H
199	SEG20	2748	355.25	12	150
200	SEG21	2724	355.25	12	150
201	SEG22	2700	355.25	12	150
202	SEG23	2676	355.25	12	150
203	SEG24	2652	355.25	12	150
204	SEG25	2628	355.25	12	150
205	SEG26	2604	355.25	12	150
206	SEG27	2580	355.25	12	150
207	SEG28	2556	355.25	12	150
208	SEG29	2532	355.25	12	150
209	SEG30	2508	355.25	12	150
210	SEG31	2484	355.25	12	150
211	SEG32	2460	355.25	12	150
212	SEG33	2436	355.25	12	150
213	SEG34	2412	355.25	12	150
214	SEG35	2388	355.25	12	150
215	SEG36	2364	355.25	12	150
216	SEG37	2340	355.25	12	150
217	SEG38	2316	355.25	12	150
218	SEG39	2292	355.25	12	150
219	SEG40	2268	355.25	12	150
220	SEG41	2244	355.25	12	150
221	SEG42	2220	355.25	12	150
222	SEG43	2196	355.25	12	150
223	SEG44	2172	355.25	12	150
224	SEG45	2148	355.25	12	150
225	SEG46	2124	355.25	12	150
226	SEG47	2100	355.25	12	150
227	SEG48	2076	355.25	12	150
228	SEG49	2052	355.25	12	150
229	SEG50	2028	355.25	12	150
230	SEG51	2004	355.25	12	150
231	SEG52	1980	355.25	12	150
232	SEG53	1956	355.25	12	150
233	SEG54	1932	355.25	12	150
234	SEG55	1908	355.25	12	150
235	SEG56	1884	355.25	12	150
236	SEG57	1860	355.25	12	150
237	SEG58	1836	355.25	12	150
238	SEG59	1812	355.25	12	150
239	SEG60	1788	355.25	12	150
240	SEG61	1764	355.25	12	150
241	SEG62	1740	355.25	12	150
242	SEG63	1716	355.25	12	150
243	SEG64	1692	355.25	12	150
244	SEG65	1668	355.25	12	150
245	SEG66	1644	355.25	12	150
246	SEG67	1620	355.25	12	150
247	SEG68	1596	355.25	12	150
248	SEG69	1572	355.25	12	150

#	PAD	X	Y	W	H
249	SEG70	1548	355.25	12	150
250	SEG71	1524	355.25	12	150
251	SEG72	1500	355.25	12	150
252	SEG73	1476	355.25	12	150
253	SEG74	1452	355.25	12	150
254	SEG75	1428	355.25	12	150
255	SEG76	1404	355.25	12	150
256	SEG77	1380	355.25	12	150
257	SEG78	1356	355.25	12	150
258	SEG79	1332	355.25	12	150
259	SEG80	1308	355.25	12	150
260	SEG81	1284	355.25	12	150
261	SEG82	1260	355.25	12	150
262	SEG83	1236	355.25	12	150
263	SEG84	1212	355.25	12	150
264	SEG85	1188	355.25	12	150
265	SEG86	1164	355.25	12	150
266	SEG87	1140	355.25	12	150
267	SEG88	1116	355.25	12	150
268	SEG89	1092	355.25	12	150
269	SEG90	1068	355.25	12	150
270	SEG91	1044	355.25	12	150
271	SEG92	1020	355.25	12	150
272	SEG93	996	355.25	12	150
273	SEG94	972	355.25	12	150
274	SEG95	948	355.25	12	150
275	SEG96	924	355.25	12	150
276	SEG97	900	355.25	12	150
277	SEG98	876	355.25	12	150
278	SEG99	852	355.25	12	150
279	SEG100	828	355.25	12	150
280	SEG101	804	355.25	12	150
281	SEG102	780	355.25	12	150
282	SEG103	756	355.25	12	150
283	SEG104	732	355.25	12	150
284	SEG105	708	355.25	12	150
285	SEG106	684	355.25	12	150
286	SEG107	660	355.25	12	150
287	SEG108	636	355.25	12	150
288	SEG109	612	355.25	12	150
289	SEG110	588	355.25	12	150
290	SEG111	564	355.25	12	150
291	SEG112	540	355.25	12	150
292	SEG113	516	355.25	12	150
293	SEG114	492	355.25	12	150
294	SEG115	468	355.25	12	150
295	SEG116	444	355.25	12	150
296	SEG117	420	355.25	12	150
297	SEG118	396	355.25	12	150
298	SEG119	372	355.25	12	150

#	PAD	X	Y	W	H
299	SEG120	348	355.25	12	150
300	SEG121	324	355.25	12	150
301	SEG122	300	355.25	12	150
302	SEG123	276	355.25	12	150
303	SEG124	252	355.25	12	150
304	SEG125	228	355.25	12	150
305	SEG126	204	355.25	12	150
306	SEG127	180	355.25	12	150
307	SEG128	156	355.25	12	150
308	SEG129	132	355.25	12	150
309	SEG130	108	355.25	12	150
310	SEG131	84	355.25	12	150
311	SEG132	60	355.25	12	150
312	SEG133	36	355.25	12	150
313	SEG134	12	355.25	12	150
314	SEG135	-12	355.25	12	150
315	SEG136	-36	355.25	12	150
316	SEG137	-60	355.25	12	150
317	SEG138	-84	355.25	12	150
318	SEG139	-108	355.25	12	150
319	SEG140	-132	355.25	12	150
320	SEG141	-156	355.25	12	150
321	SEG142	-180	355.25	12	150
322	SEG143	-204	355.25	12	150
323	SEG144	-228	355.25	12	150
324	SEG145	-252	355.25	12	150
325	SEG146	-276	355.25	12	150
326	SEG147	-300	355.25	12	150
327	SEG148	-324	355.25	12	150
328	SEG149	-348	355.25	12	150
329	SEG150	-372	355.25	12	150
330	SEG151	-396	355.25	12	150
331	SEG152	-420	355.25	12	150
332	SEG153	-444	355.25	12	150
333	SEG154	-468	355.25	12	150
334	SEG155	-492	355.25	12	150
335	SEG156	-516	355.25	12	150
336	SEG157	-540	355.25	12	150
337	SEG158	-564	355.25	12	150
338	SEG159	-588	355.25	12	150
339	SEG160	-612	355.25	12	150
340	SEG161	-636	355.25	12	150
341	SEG162	-660	355.25	12	150
342	SEG163	-684	355.25	12	150
343	SEG164	-708	355.25	12	150
344	SEG165	-732	355.25	12	150
345	SEG166	-756	355.25	12	150
346	SEG167	-780	355.25	12	150
347	SEG168	-804	355.25	12	150
348	SEG169	-828	355.25	12	150

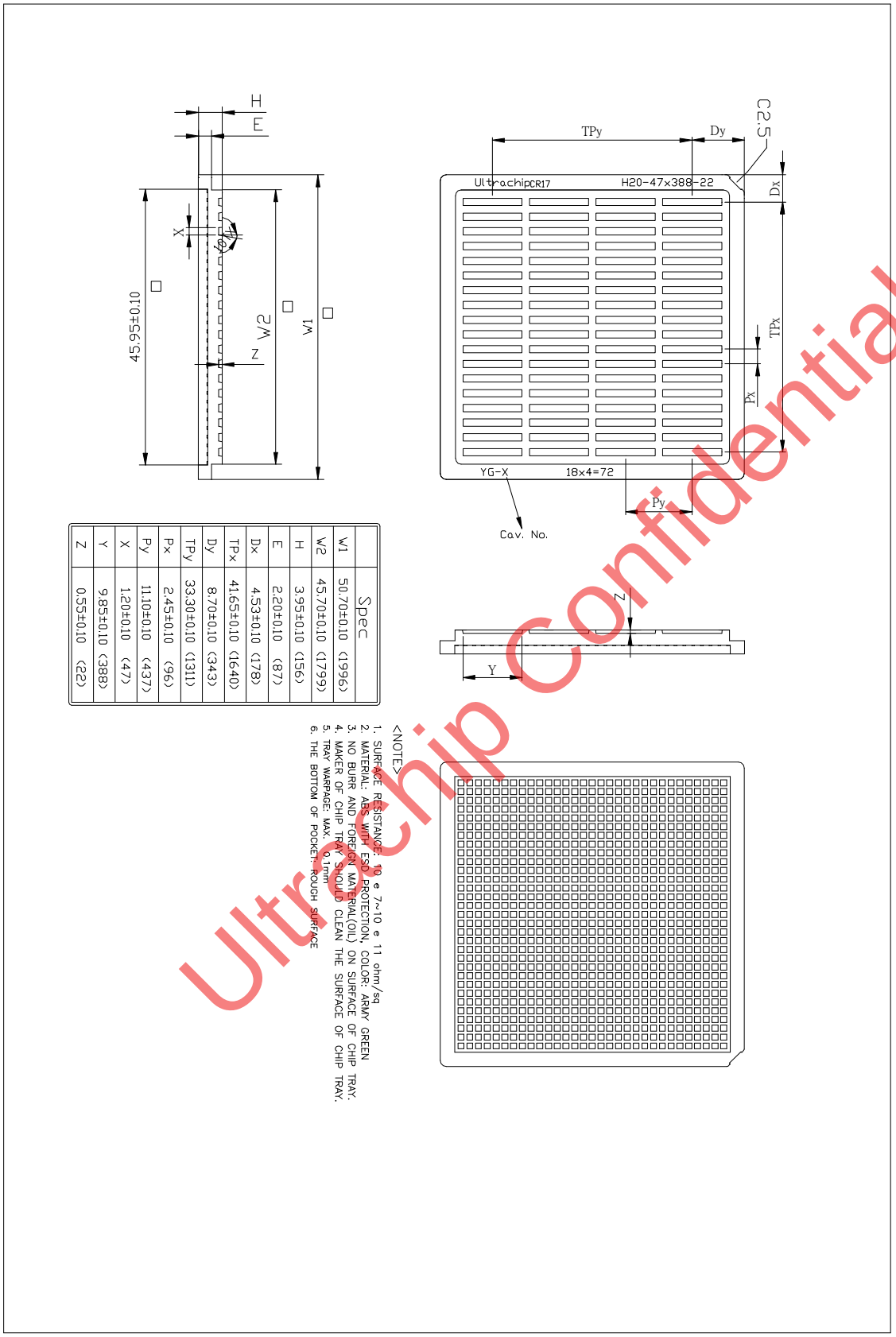
#	PAD	X	Y	W	H
349	SEG170	-852	355.25	12	150
350	SEG171	-876	355.25	12	150
351	SEG172	-900	355.25	12	150
352	SEG173	-924	355.25	12	150
353	SEG174	-948	355.25	12	150
354	SEG175	-972	355.25	12	150
355	SEG176	-996	355.25	12	150
356	SEG177	-1020	355.25	12	150
357	SEG178	-1044	355.25	12	150
358	SEG179	-1068	355.25	12	150
359	SEG180	-1092	355.25	12	150
360	SEG181	-1116	355.25	12	150
361	SEG182	-1140	355.25	12	150
362	SEG183	-1164	355.25	12	150
363	SEG184	-1188	355.25	12	150
364	SEG185	-1212	355.25	12	150
365	SEG186	-1236	355.25	12	150
366	SEG187	-1260	355.25	12	150
367	SEG188	-1284	355.25	12	150
368	SEG189	-1308	355.25	12	150
369	SEG190	-1332	355.25	12	150
370	SEG191	-1356	355.25	12	150
371	SEG192	-1380	355.25	12	150
372	SEG193	-1404	355.25	12	150
373	SEG194	-1428	355.25	12	150
374	SEG195	-1452	355.25	12	150
375	SEG196	-1476	355.25	12	150
376	SEG197	-1500	355.25	12	150
377	SEG198	-1524	355.25	12	150
378	SEG199	-1548	355.25	12	150
379	SEG200	-1572	355.25	12	150
380	SEG201	-1596	355.25	12	150
381	SEG202	-1620	355.25	12	150
382	SEG203	-1644	355.25	12	150
383	SEG204	-1668	355.25	12	150
384	SEG205	-1692	355.25	12	150
385	SEG206	-1716	355.25	12	150
386	SEG207	-1740	355.25	12	150
387	SEG208	-1764	355.25	12	150
388	SEG209	-1788	355.25	12	150
389	SEG210	-1812	355.25	12	150
390	SEG211	-1836	355.25	12	150
391	SEG212	-1860	355.25	12	150
392	SEG213	-1884	355.25	12	150
393	SEG214	-1908	355.25	12	150
394	SEG215	-1932	355.25	12	150
395	SEG216	-1956	355.25	12	150
396	SEG217	-1980	355.25	12	150
397	SEG218	-2004	355.25	12	150
398	SEG219	-2028	355.25	12	150

#	PAD	X	Y	W	H
399	SEG220	-2052	355.25	12	150
400	SEG221	-2076	355.25	12	150
401	SEG222	-2100	355.25	12	150
402	SEG223	-2124	355.25	12	150
403	SEG224	-2148	355.25	12	150
404	SEG225	-2172	355.25	12	150
405	SEG226	-2196	355.25	12	150
406	SEG227	-2220	355.25	12	150
407	SEG228	-2244	355.25	12	150
408	SEG229	-2268	355.25	12	150
409	SEG230	-2292	355.25	12	150
410	SEG231	-2316	355.25	12	150
411	SEG232	-2340	355.25	12	150
412	SEG233	-2364	355.25	12	150
413	SEG234	-2388	355.25	12	150
414	SEG235	-2412	355.25	12	150
415	SEG236	-2436	355.25	12	150
416	SEG237	-2460	355.25	12	150
417	SEG238	-2484	355.25	12	150
418	SEG239	-2508	355.25	12	150
419	SEG240	-2532	355.25	12	150
420	SEG241	-2556	355.25	12	150
421	SEG242	-2580	355.25	12	150
422	SEG243	-2604	355.25	12	150
423	SEG244	-2628	355.25	12	150
424	SEG245	-2652	355.25	12	150
425	SEG246	-2676	355.25	12	150
426	SEG247	-2700	355.25	12	150
427	SEG248	-2724	355.25	12	150
428	SEG249	-2748	355.25	12	150
429	SEG250	-2772	355.25	12	150
430	SEG251	-2796	355.25	12	150
431	SEG252	-2820	355.25	12	150
432	SEG253	-2844	355.25	12	150
433	SEG254	-2868	355.25	12	150
434	SEG255	-2892	355.25	12	150
435	SEG256	-2916	355.25	12	150
436	SEG257	-2940	355.25	12	150
437	SEG258	-2964	355.25	12	150
438	SEG259	-2988	355.25	12	150
439	SEG260	-3012	355.25	12	150
440	SEG261	-3036	355.25	12	150
441	SEG262	-3060	355.25	12	150
442	SEG263	-3084	355.25	12	150
443	SEG264	-3108	355.25	12	150
444	SEG265	-3132	355.25	12	150
445	SEG266	-3156	355.25	12	150
446	SEG267	-3180	355.25	12	150
447	SEG268	-3204	355.25	12	150
448	COM1	-3228	355.25	12	150

#	PAD	X	Y	W	H
449	COM3	-3252	355.25	12	150
450	COM5	-3276	355.25	12	150
451	COM7	-3300	355.25	12	150
452	COM9	-3324	355.25	12	150
453	COM11	-3348	355.25	12	150
454	COM13	-3372	355.25	12	150
455	COM15	-3396	355.25	12	150
456	COM17	-3420	355.25	12	150
457	COM19	-3444	355.25	12	150
458	COM21	-3468	355.25	12	150
459	COM23	-3492	355.25	12	150
460	COM25	-3516	355.25	12	150
461	COM27	-3540	355.25	12	150
462	COM29	-3564	355.25	12	150
463	COM31	-3588	355.25	12	150
464	COM33	-3612	355.25	12	150
465	COM35	-3636	355.25	12	150
466	COM37	-3660	355.25	12	150
467	COM39	-3684	355.25	12	150
468	COM41	-3708	355.25	12	150
469	COM43	-3732	355.25	12	150
470	COM45	-3756	355.25	12	150
471	COM47	-3780	355.25	12	150
472	COM49	-3804	355.25	12	150
473	COM51	-3828	355.25	12	150
474	COM53	-3852	355.25	12	150
475	COM55	-3876	355.25	12	150
476	COM57	-3900	355.25	12	150
477	COM59	-3924	355.25	12	150
478	COM61	-3948	355.25	12	150
479	COM63	-3972	355.25	12	150
480	COM65	-3996	355.25	12	150
481	COM67	-4020	355.25	12	150
482	COM69	-4044	355.25	12	150
483	COM71	-4068	355.25	12	150
484	COM73	-4092	355.25	12	150
485	COM75	-4116	355.25	12	150
486	COM77	-4140	355.25	12	150
487	COM79	-4164	355.25	12	150
488	COM81	-4188	355.25	12	150
489	COM83	-4212	355.25	12	150
490	COM85	-4236	355.25	12	150
491	COM87	-4260	355.25	12	150
492	COM89	-4284	355.25	12	150
493	COM91	-4308	355.25	12	150
494	COM93	-4332	355.25	12	150
495	COM95	-4356	355.25	12	150
496	COM97	-4380	355.25	12	150
497	COM99	-4404	355.25	12	150
498	COM101	-4428	355.25	12	150

#	PAD	X	Y	W	H
499	COM103	-4452	355.25	12	150
500	COM105	-4476	355.25	12	150
501	COM107	-4500	355.25	12	150
502	COM109	-4524	355.25	12	150
503	COM111	-4548	355.25	12	150
504	COM113	-4572	355.25	12	150
505	COM115	-4596	355.25	12	150
506	COM117	-4620	355.25	12	150
507	COM119	-4644	355.25	12	150
508	COM121	-4668	355.25	12	150
509	COM123	-4692	355.25	12	150
510	COM125	-4716	355.25	12	150
511	COM127	-4740	355.25	12	150
512	DUMMY	-4764	355.25	12	150

TRAY INFORMATION



	Spec
W1	50.70±0.10 (1996)
W2	45.70±0.10 (1799)
H	3.95±0.10 (156)
E	2.20±0.10 (87)
Dx	4.53±0.10 (178)
TPx	41.65±0.10 (1640)
Dy	8.70±0.10 (343)
TPy	33.30±0.10 (1311)
Px	2.45±0.10 (96)
Py	11.10±0.10 (437)
X	1.20±0.10 (47)
Y	9.85±0.10 (388)
Z	0.55±0.10 (22)

<NOTE>
1. SURFACE RESISTANCE: 10 e 7~10 e 11 ohm/sq
2. MATERIAL: ABS WITH ESD PROTECTION, COLOR: ARMY GREEN
3. NO BURR AND FOREIGN MATERIAL(OIL) ON SURFACE OF CHIP TRAY.
4. MAKER OF CHIP TRAY SHOULD CLEAN THE SURFACE OF CHIP TRAY.
5. TRAY WARPAGE: MAX. 0.1mm
6. THE BOTTOM OF POCKET: ROUGH SURFACE

REVISION HISTORY

Revision	Contents	Date
0.6	First release	Mar. 5, 2012
0.8	(1) For Command (22), a Figure is added to illustrate Line Inversion.	Jun. 7, 2012
	(2) Figures 3a, 3b, 4a and 5a are updated for each interface.	
	(3) 2 notes are appended to section Host Interface Reference Circuit.	
	(4) Power Consumption data present.	
	(5) Some AC timings are corrected.	
1.0	ESD data are updated.	Jun. 21, 2012
1.1	ESD data are updated.	Oct. 9, 2012
1.11	Figure 13, Power OFF-ON Sequence, is update.	Nov. 22, 2012
1.12	The AC timing drawing for 8080 mode is corrected.	Apr. 25, 2013
1.13	(1) For all the Host Interface Reference Circuit drawings, connect the RST pin to MPU.	Jun. 14, 2013
	(2) Alignment Marks: on Metal3 → on Metal4	
1.2	Recommended capacitor values for CAx and CBx: 2.2uF/5uF → 2.2uF(5V)/5uF(5V)	Jul. 18, 2013
1.3	AEC-Q100 related description is added.	Oct. 7, 2013