

PL FPGA 125 MHz

LUT AWG

AXI
ControllerFIFO
Re,Im
[31:0]

FFT

 $u[n]$ CIC
 $\downarrow 8$ FIFO
Re,Im
[31:0]

FFT

 $y[n]$ CIC
 $\downarrow 8$

RE

OS Application

PS ARM 800 MHz

DRAM

Network

Client
PC $V[13:0]$

DAC

RF

-DA
+ $v(t)$ 50 Ω $D_u[13:0]$

ADC

AAF

 $u(t)$ $D_y[13:0]$

ADC

AAF

 $y(t)$ C_f
 R_f -TIA
+ $i(t)$ 50 Ω MEA
 Z