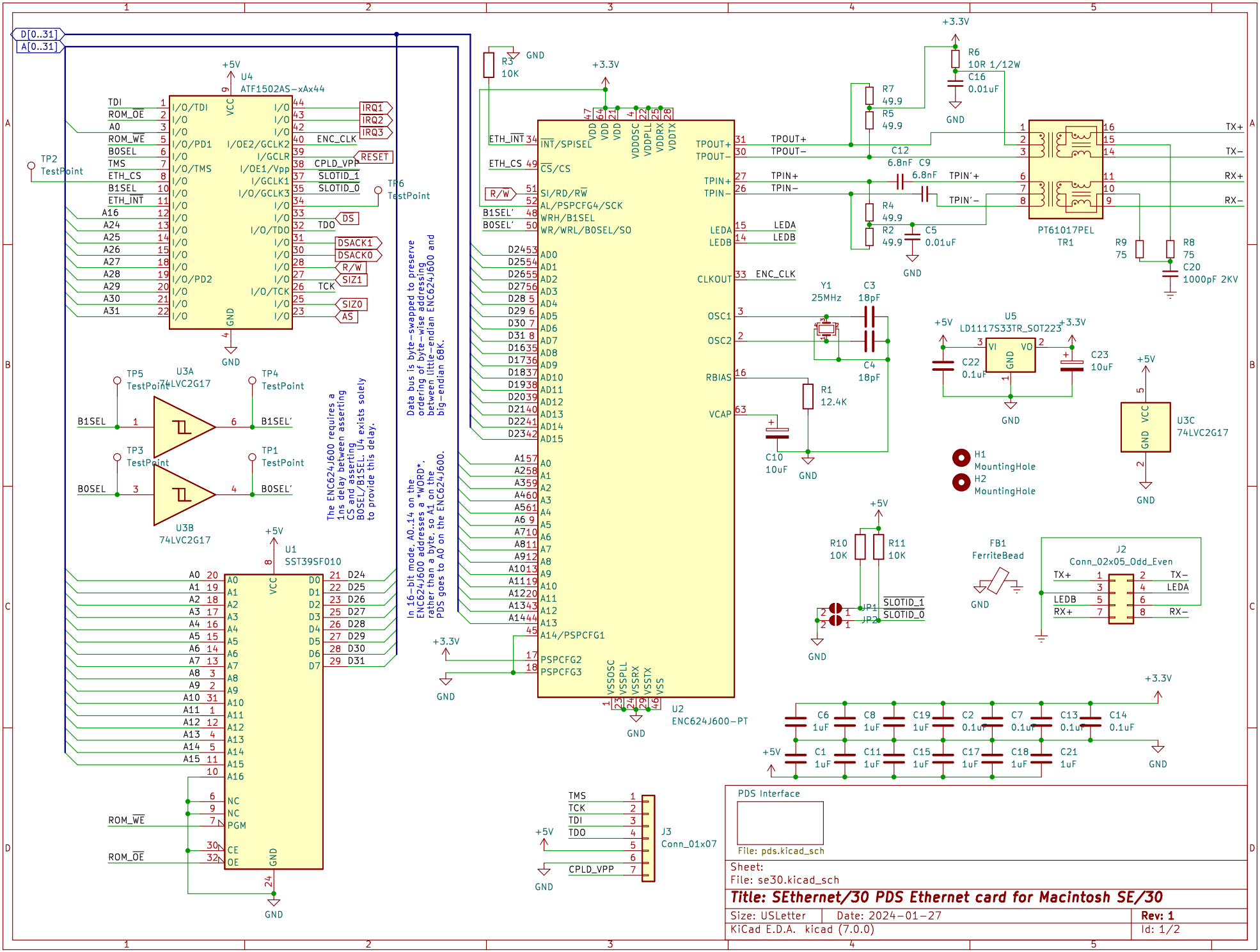
D[0..31]
A[0..31]
U4
ATF1502AS-xAx44
+5V
TDI
ROM_OE
A0
ROM_WE
BOSEL
TMS
ETH_CS
B1SEL
ETH_INT
A16
A24
A25
A26
A27
A28
A29
A30
A31
IRQ1
IRQ2
IRQ3
ENC_CLK
RESET
CPLD_VPP
SLOTID_1
SLOTID_0
TDO
DS
DSACK1
DSACK0
R/W
SIZ1
TCK
SIZ0
AS
GND
TP2
TestPoint
TP6
TestPoint
TP5
TestPoint
TP4
TestPoint
TP3
TestPoint
TP1
TestPoint
U3A
74LVC2G17
U3B
74LVC2G17
B1SEL´
BOSEL´
The ENC624J600 requires a 1ns delay between asserting CS and asserting BOSEL/B1SEL. U4 exists solely to provide this delay.
Data bus is byte-swapped to preserve ordering of byte-wise addressing between little-endian ENC624J600 and big-endian 68K.
In 16-bit mode, A0..14 on the ENC624J600 addresses a *WORD*, rather than a byte, so A1 on the PDS goes to A0 on the ENC624J600.
U1
SST39SF010
D24
D25
D26
D27
D28
D29
D30
D31
NC
PGM
CE
OE
R3
10K
+3.3V
ETH_INT
ETH_CS
R/W
B1SEL´
BOSEL´
INT/SPISEL
CS/CS
SI/RD/RW
AL/PSPCFG4/SCK
WRH/B1SEL
WR/WRL/BOSEL/SO
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
A14/PSPCFG1
PSPCFG2
PSPCFG3
VDD
VDDOSC
VDDPLL
VDDRX
VDDTX
VSSOSC
VSSPLL
VSSRX
VSSTX
VSS
TPOUT+
TPOUT−
TPIN+
TPIN−
LEDA
LEDB
CLKOUT
OSC1
OSC2
RBIAS
VCAP
U2
ENC624J600-PT
R7
49.9
R5
49.9
R6
10R 1/12W
C16
0.01uF
C12
6.8nF
C9
6.8nF
R4
49.9
R2
49.9
C5
0.01uF
TPIN´+
TPIN´−
PT61017PEL
TR1
TX+
TX−
RX+
RX−
R9
75
R8
75
C20
1000pF 2KV
Y1
25MHz
C3
18pF
C4
18pF
R1
12.4K
C10
10uF
U5
LD1117S33TR_SOT223
VI
VO
C22
0.1uF
C23
10uF
U3C
74LVC2G17
H1
MountingHole
H2
MountingHole
R10
10K
R11
10K
JP1
JP2
SLOTID_1
SLOTID_0
FB1
FerriteBead
J2
Conn_02x05_Odd_Even
C6
1uF
C8
1uF
C19
1uF
C2
0.1uF
C7
0.1uF
C13
0.1uF
C14
0.1uF
C1
1uF
C11
1uF
C15
1uF
C17
1uF
C18
1uF
C21
1uF
TMS
TCK
TDI
TDO
CPLD_VPP
J3
Conn_01x07
PDS Interface
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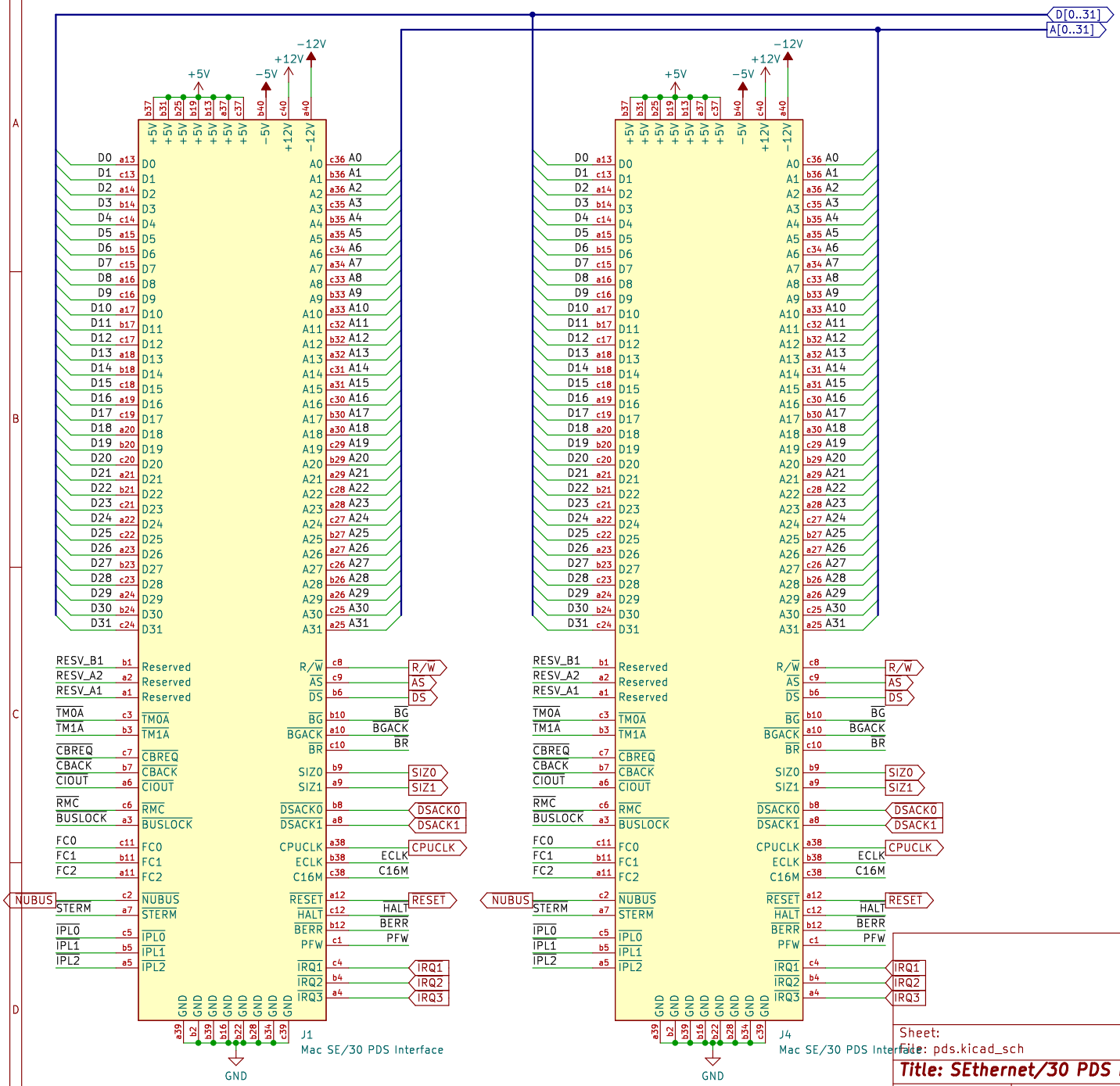
Title: SEthernet/30 PDS Ethernet card for Macintosh SE/30
Size: USLetter
Date: 2024-01-27
Rev: 1
KiCad E.D.A. kicad (7.0.0)
Id: 1/2



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Title: SEthernet/30 PDS Ethernet card for Macintosh SE/30

Size: USLetter	Date: 2024-01-27	Rev: 1
KiCad E.D.A. kicad (7.0.0)		Id: 2/2