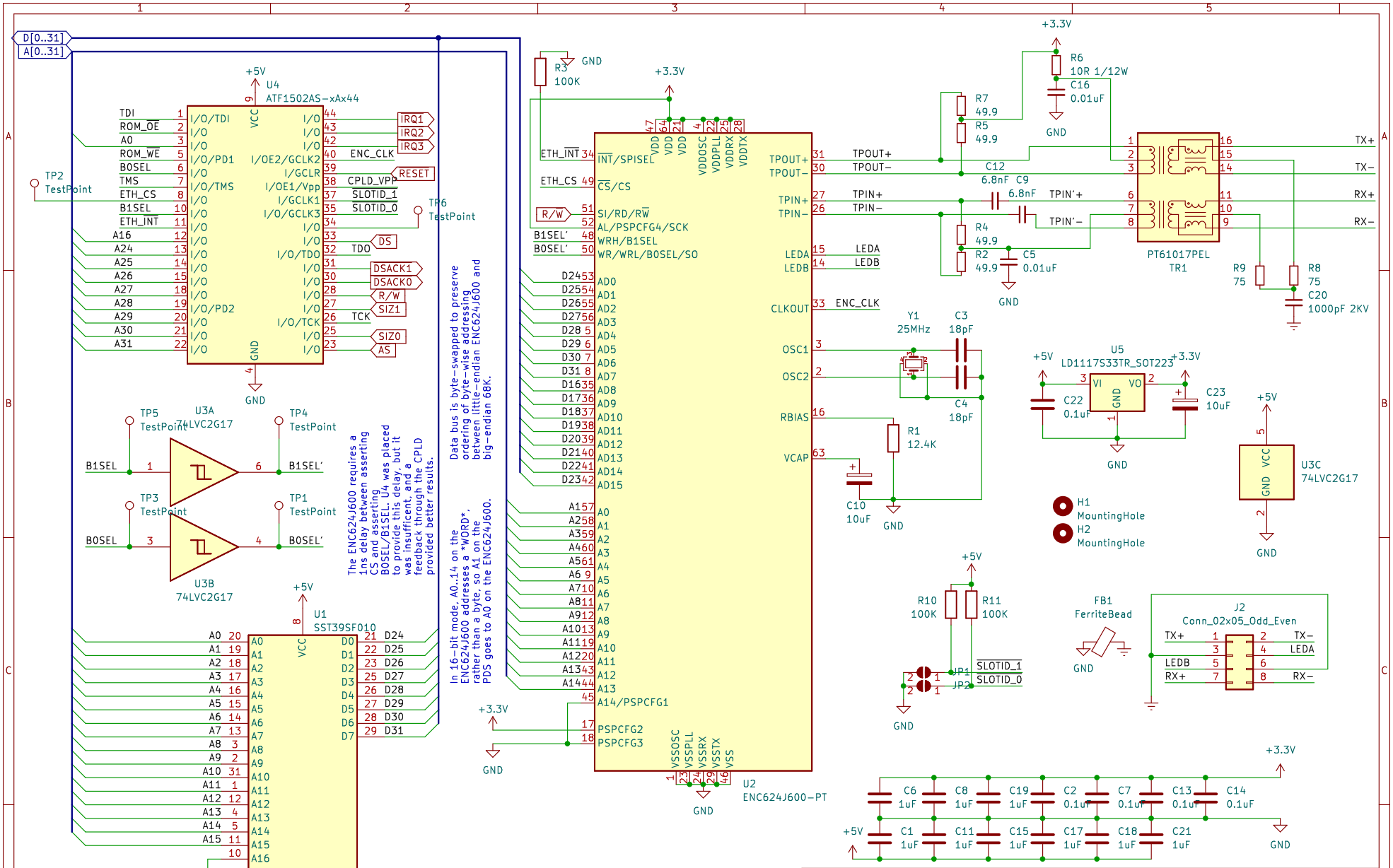
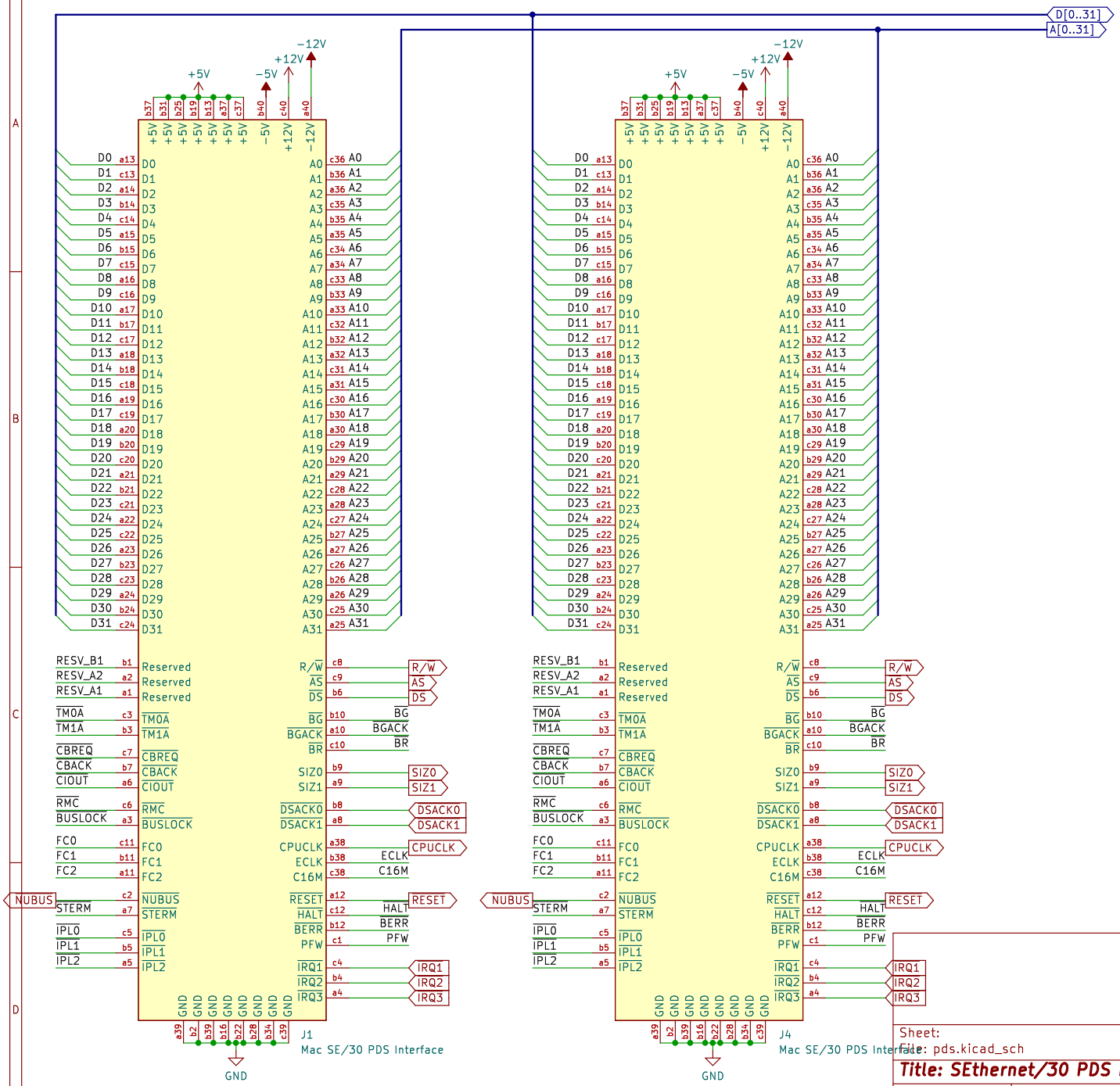

D[0..31]
A[0..31]
U4
ATF1502AS-xAx44
+5V
TDI
ROM_OE
A0
ROM_WE
B0SEL
TMS
ETH_CS
B1SEL
ETH_INT
A16
A24
A25
A26
A27
A28
A29
A30
A31
IRQ1
IRQ2
IRQ3
ENC_CLK
RESET
CPLD_VPP
SLOTID_1
SLOTID_0
TDO
DS
DSACK1
DSACK0
R/W
SIZ1
TCK
SIZ0
AS
TP2
TestPoint
TP6
TestPoint
GND
TP5
TestPoint
TP4
TestPoint
U3A
74LVC2G17
B1SEL
B1SEL'
TP3
TestPoint
TP1
TestPoint
B0SEL
B0SEL'
U3B
74LVC2G17
The ENC624J600 requires a 1ns delay between asserting CS and asserting B0SEL/B1SEL. U4 was placed to provide this delay, but it was insufficent, and a feedback through the CPLD provided better results.
Data bus is byte-swapped to preserve ordering of byte-wise addressing between little-endian ENC624J600 and big-endian 68K.
In 16-bit mode, A0..14 on the ENC624J600 addresses a *WORD*, rather than a byte, so A1 on the PDS goes to A0 on the ENC624J600.
U1
SST39SF010
ROM_WE
ROM_OE
R3
100K
+3.3V
ETH_INT
ETH_CS
R/W
B1SEL'
B0SEL'
D24
D25
D26
D27
D28
D29
D30
D31
U2
ENC624J600-PT
TPOUT+
TPOUT-
TPIN+
TPIN-
LEDA
LEDB
CLKOUT
OSC1
OSC2
RBIAS
VCAP
R7
49.9
R5
49.9
R6
10R 1/12W
C16
0.01uF
C12
6.8nF
C9
6.8nF
TPIN'+
TPIN'-
R4
49.9
R2
49.9
C5
0.01uF
PT61017PEL
TR1
TX+
TX-
RX+
RX-
R9
75
R8
75
C20
1000pF 2KV
Y1
25MHz
C3
18pF
C4
18pF
R1
12.4K
C10
10uF
U5
LD1117S33TR_SOT223
C22
0.1uF
C23
10uF
U3C
74LVC2G17
H1
MountingHole
H2
MountingHole
R10
100K
R11
100K
JP1
JP2
SLOTID_1
SLOTID_0
FB1
FerriteBead
J2
Conn_02x05_Odd_Even
C6
1uF
C8
1uF
C19
1uF
C2
0.1uF
C7
0.1uF
C13
0.1uF
C14
0.1uF
C1
1uF
C11
1uF
C15
1uF
C17
1uF
C18
1uF
C21
1uF
J3
Conn_01x07
TMS
TCK
TDI
TDO
CPLD_VPP
PDS Interface
File: pds.kicad_sch
Sheet:
File: se30.kicad_sch
Title: SEthernet/30 PDS Ethernet card for Macintosh SE/30
Size: USLetter
Date: 2024-01-27
Rev: 1
KiCad E.D.A. kicad (7.0.0)
Id: 1/2



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Title: SEthernet/30 PDS Ethernet card for Macintosh SE/30

Size: USLetter	Date: 2024-01-27	Rev: 1
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