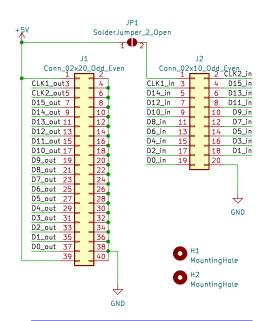
R15

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Per HP documentation, the +5V supply is only to be used for powering probe logic, and should be a no-connect on the DUT.

For safety, JP1 is open by default, and must be closed to supply +5V to J2.

For details on termination network specs and pinouts, see HP/Agilent document 5962-8620E "Minimizing Intrusion Effects When Probing With a Logic Analyzer", dated July 1995.

The termination RC networks are as described in Figure 1. ICs implementing this network were available from HP under part number 1810–1278 but appear to NLA (or at least not available to mere mortals at a reasonable price).

The pinout of J1 corresponds to the 40-pin pod connector described in Figure 5A.

The pinout of J2 corresponds to the 20-pin device-under-test connector on the 01650-63203 termination adapter, described in Figure 5B.

J1 and J2 are conventional 0.1"-pitch 2-row shrouded IDC headers.

On the original 01650-63203 adapter, the J2 connector was an IDC receptacle on a short section of flexible PCB, for direct connection to the device under test. In this design, J2 is instead an IDC header, and a small length of ribbon cable can serve as the flexible section, or individual probes can be connected directly to the pins.

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