Team #4

Project #28: LogicBlockz

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Capstone Proposal

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Requirements and Solution Report

Introduction

This document describes the objectives of the capstone project being done by Team # 4. Our project is an educational puzzle that will teach children the basics of discrete logic and logic gates. We are doing this project because we feel strongly that logic is a good way to introduce children to engineering and computers and that the concepts are simple enough for anyone to learn. We are disappointed this subject was not introduced to us until college, and aim to provide a tool that will increase the exposure of discrete logic to middle and high school students.

Client Background

The client for this project is us: Ryan Hart, Stephen Coombes, and David Tyler. We all have an interest in developing an educational, marketable product to both act as a great capstone project as well as possibly make some money after graduation. Our budget for this project is limited to a few hundred dollars, but additional funding can be found upon critical need.

Problem Statement

As noted in the introduction, digital logic is not introduced until college, by which point a student has already chosen their field of study. Younger students are not given an introduction to digital logic and design at an earlier age.

Project Objectives

The goal is to create a hands-on puzzle that will teach children ages 12-18 the basics of logic gates and logic design. This puzzle toy must also be reasonably priced to encourage widespread adoption.

Research Summary

The major reason we chose to do this project was that we could find no product that does what we are trying to accomplish. However, a couple devices performing fairly similar functions were found.

The most interesting product we found during research was the LogicBlocks Kit [1]. This is basically a do-it-yourself kit that provides small printed circuit boards each containing one logic gate. The circuit boards can be plugged into each other using header pins. The kit provides input, gate, and power blocks. Each gate circuit has an LED on the output to show the logic level. This kit appears appealing to tinker with, but it seems to be geared towards

a hobbyist who already has a basic understanding of logic as it does not have a puzzle to solve or any objective. The whole thing is run on a button battery.

The other logic design products we found were mostly computer based. We were already familiar with Logicworks, a logic design software package for engineers [2]. This software was created for professionals and students to design discrete logic circuits. To use it, one essentially draws the schematic on screen and then runs a simulation of the circuit. This software is excellent for aspiring engineers to learn to intricacies of logic design, but most children would get lost in the amount of detail provided. Nevertheless, this software provides some interesting features such as a logic analyzer that we could use in our project.

Another example of a software product is a computer game that challenges the player to solve logic puzzles by designing semiconductors called Kohctpytop [3]. This game is too hard and complex to serve as an introduction to logic, but provides some interesting puzzles, which might be altered to be in our product. Also the angle of semiconductor fabrication is an extremely interesting one. Maybe our product can include some hints as to the underlying operation of the logic gates beyond teaching simply what they do.

Requirements

The device shall:

- Demonstrate the basics of logic design to children aged twelve and up
- Run on battery power for at least four hours
- Be a toy
- Be able to provide time-variant puzzles

The device shall not:

- In any way represent a hazard to persons in the room

Potential Solutions

1. The first solution is to link tiles together via small cables, such as USB cables (which are cheap and widely available). These cables would be able to provide signal and power connections, and the flexibility of cables prevents any complications of angling tiles. On the downside, it creates a less-than-elegant solution.

2. The second solution is to link tiles together via physical connectors, e.g. male/female connector ends. Like USB cables, this can provide signal and power through single connections, but it could lead to fitment concerns. On the upside, it is sleeker than having an array of cables spilling around, and there are no cables to lose.

3. The third solution is to build a rigid snap board, with connectors through the bottom of each tile. The path of the tiles would be defined by the board itself.

4. The fourth solution is to run a daisy-chain of wireless communications and inductive power. This is the most elegant and technologically advanced concept, however, the net power efficiency on a simple ten block array is under 30%.

5. The fifth solution is to use an inductive power mat beneath all the blocks, which eliminates cascading inefficiencies. This solution would also necessitate wireless communication of the signal, and thus it remains a very elegant and sleek solution.

Chosen Solution

Metric

Table 1: Grabber Mechanism Metric

	Cost	Reliability	Ease Use	Expansion	Replace	Efficiency	Total
Cables	4	4	3	4	4	5	3.8
Hard Link	4	4	2	4	4	5	3.6
Snap Grid	2	3.5	1	0	1	5	2.25
Daisy-Chain	1	2	4	3	2	0	2.0
Mat	2	3	3	2	1	3	2.5
Weights	0.35	0.30	0.20	0.05	0.05	0.05	1.0

Explaination

The daisy chain solution is not viable due to its severe inefficiency, despite the desirable characteristics of creating an exceptionally futuristic design. The daisy chain shares, to a greater extent, the problem that eliminates the power mat design, in that it is very costly. This cost concern is largely responsible for the elimination of the power mat design from consideration. The rigid snap board suffers from poor expansion and lack of creativity possible. Thus the consideration comes down to hard links versus the cables, and the cables take a slight edge due to the simplicity of connecting cables in any imaginable configuration.

Schedule

		Name	Duration	Start	Finish	Predecessors
1		**Research**	**4 days?**	**4/28/14 8:00 AM**	**5/1/14 5:00 PM**	
2		**Microprocessor**	**4 days?**	**4/28/14 8:00 AM**	**5/1/14 5:00 PM**	
3		Operating Voltage	4 days?	4/28/14 8:00 AM	5/1/14 5:00 PM	
4		Current Draw	1 day?	4/28/14 8:00 AM	4/28/14 5:00 PM	
5		GPIO	1 day?	4/28/14 8:00 AM	4/28/14 5:00 PM	
6		USB	1 day?	4/28/14 8:00 AM	4/28/14 5:00 PM	
7		**Power**	**1 day?**	**4/28/14 8:00 AM**	**4/28/14 5:00 PM**	
8		DC-DC Converter	1 day?	4/28/14 8:00 AM	4/28/14 5:00 PM	
9		**Battery**	**3 days?**	**4/28/14 8:00 AM**	**4/30/14 5:00 PM**	
10		LiPo	3 days?	4/28/14 8:00 AM	4/30/14 5:00 PM	
11		Alkaline	1 day?	4/28/14 8:00 AM	4/28/14 5:00 PM	
12		Li-ion	2 days?	4/28/14 8:00 AM	4/29/14 5:00 PM	
13		**CMOS Gates**	**1 day?**	**4/29/14 8:00 AM**	**4/29/14 5:00 PM**	
14		Use CMOS Logic Ch...	1 day?	4/29/14 8:00 AM	4/29/14 5:00 PM	
15		Use Transistors	1 day?	4/29/14 8:00 AM	4/29/14 5:00 PM	
16		**Design**	**18 days?**	**5/2/14 8:00 AM**	**5/27/14 5:00 PM**	**1**
17		**Software**	**3 days?**	**5/5/14 8:00 AM**	**5/7/14 5:00 PM**	
18		**LCD**	**3 days?**	**5/5/14 8:00 AM**	**5/7/14 5:00 PM**	
19		SPI vs I2C	3 days?	5/5/14 8:00 AM	5/7/14 5:00 PM	
20		Define Output signal...	1 day?	5/2/14 8:00 AM	5/2/14 5:00 PM	
21		**UI**	**2 days?**	**5/2/14 8:00 AM**	**5/5/14 5:00 PM**	
22		**Computer**	**2 days?**	**5/2/14 8:00 AM**	**5/5/14 5:00 PM**	
23		Choose Language	1 day?	5/2/14 8:00 AM	5/2/14 5:00 PM	
24		Mock Up Interface	2 days?	5/2/14 8:00 AM	5/5/14 5:00 PM	
25		On-Board	2 days?	5/2/14 8:00 AM	5/5/14 5:00 PM	
26		**CMOS Gates**	**12 days**	**5/12/14 8:00 AM**	**5/27/14 5:00 PM**	
27		Design NAND gate	2 days	5/12/14 8:00 AM	5/13/14 5:00 PM	
28		Design AND gate	2 days	5/14/14 8:00 AM	5/15/14 5:00 PM	27
29		Design NOR gate	2 days	5/16/14 8:00 AM	5/19/14 5:00 PM	28
30		Design OR gate	2 days	5/20/14 8:00 AM	5/21/14 5:00 PM	29
31		Design NOT gate	2 days	5/22/14 8:00 AM	5/23/14 5:00 PM	30
32		Design XOR gate	2 days	5/26/14 8:00 AM	5/27/14 5:00 PM	31
33		**Power**	**1 day?**	**5/2/14 8:00 AM**	**5/2/14 5:00 PM**	
34		**Design DC-DC C...**	**1 day?**	**5/2/14 8:00 AM**	**5/2/14 5:00 PM**	
35		Order components	1 day?	5/2/14 8:00 AM	5/2/14 5:00 PM	

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		Name	Duration	Start	Finish	Predecessors
36		**⊟Choose Battery**	**1 day?**	**5/2/14 8:00 AM**	**5/2/14 5:00 PM**	
37		Order Battery	1 day?	5/2/14 8:00 AM	5/2/14 5:00 PM	
38		**⊟Mechanical**	**3 days?**	**5/2/14 8:00 AM**	**5/6/14 5:00 PM**	
39		Choose Material	2 days?	5/2/14 8:00 AM	5/5/14 5:00 PM	
40		Choose Size	3 days	5/2/14 8:00 AM	5/6/14 5:00 PM	
41		**⊟Microprocessor**	**4 days?**	**5/2/14 8:00 AM**	**5/7/14 5:00 PM**	
42		**⊟Choose Processor**	**1 day?**	**5/2/14 8:00 AM**	**5/2/14 5:00 PM**	
43		Order Processor	1 day?	5/2/14 8:00 AM	5/2/14 5:00 PM	
44		Mock-up wiring di...	4 days?	5/2/14 8:00 AM	5/7/14 5:00 PM	
45		**⊟Prototype**	**2 days?**	**5/28/14 8:00 AM**	**5/29/14 5:00 PM**	**16**
46		**⊟Software**	**1 day?**	**5/28/14 8:00 AM**	**5/28/14 5:00 PM**	
47		Write LCD Initial code	1 day?	5/28/14 8:00 AM	5/28/14 5:00 PM	42
48		Write initial signal...	1 day?	5/28/14 8:00 AM	5/28/14 5:00 PM	42
49		CMOS Gates	1 day?	5/28/14 8:00 AM	5/28/14 5:00 PM	
50		**⊟Power**	**2 days?**	**5/28/14 8:00 AM**	**5/29/14 5:00 PM**	
51		Prototype DC-DC...	2 days	5/28/14 8:00 AM	5/29/14 5:00 PM	
52		Confirm Voltage O...	1 day?	5/28/14 8:00 AM	5/28/14 5:00 PM	
53		Check noise	1 day?	5/28/14 8:00 AM	5/28/14 5:00 PM	
54		**⊟Mechanical**	**1 day?**	**5/28/14 8:00 AM**	**5/28/14 5:00 PM**	
55		3D Print Ideas	1 day?	5/28/14 8:00 AM	5/28/14 5:00 PM	
56		**⊟Build**	**9 days?**	**5/30/14 8:00 AM**	**6/11/14 5:00 PM**	**45**
57		Software	1 day?	5/30/14 8:00 AM	5/30/14 5:00 PM	
58		**⊟Finalize CMOS Gates**	**7 days?**	**6/3/14 8:00 AM**	**6/11/14 5:00 PM**	
59		Build NAND gate	1 day?	6/3/14 8:00 AM	6/3/14 5:00 PM	
60		Build AND gate	1 day?	6/4/14 8:00 AM	6/4/14 5:00 PM	59
61		Build NOR gate	1 day?	6/4/14 8:00 AM	6/4/14 5:00 PM	59
62		Build OR gate	1 day?	6/5/14 8:00 AM	6/5/14 5:00 PM	61
63		Build NOT gate	2 days?	6/6/14 8:00 AM	6/9/14 5:00 PM	62
64		Build XOR gate	2 days?	6/10/14 8:00 AM	6/11/14 5:00 PM	63
65		**⊟Power**	**1 day?**	**6/3/14 8:00 AM**	**6/3/14 5:00 PM**	
66		**⊟Build DC-DC Co...**	**1 day?**	**6/3/14 8:00 AM**	**6/3/14 5:00 PM**	
67		Confirm by powe...	1 day?	6/3/14 8:00 AM	6/3/14 5:00 PM	51
68		Let system run till f...	1 day?	6/3/14 8:00 AM	6/3/14 5:00 PM	
69		**⊟Mechanical**	**4 days?**	**6/3/14 8:00 AM**	**6/6/14 5:00 PM**	
70		Build enclosures o...	4 days?	6/3/14 8:00 AM	6/6/14 5:00 PM	

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		Name	Duration	Start	Finish	Predecessors
71		**⊟UI**	**1 day?**	**6/3/14 8:00 AM**	**6/3/14 5:00 PM**	
72		Build computer int...	1 day?	6/3/14 8:00 AM	6/3/14 5:00 PM	
73		Build on-board de...	1 day?	6/3/14 8:00 AM	6/3/14 5:00 PM	
74		**⊟Test**	**12 days?**	**6/12/14 8:00 AM**	**6/27/14 5:00 PM**	**56**
75		Hardware	6 days?	6/12/14 8:00 AM	6/19/14 5:00 PM	
76		**⊟Durability Testing**	**7 days?**	**6/19/14 8:00 AM**	**6/27/14 5:00 PM**	
77		Drop Test	7 days?	6/19/14 8:00 AM	6/27/14 5:00 PM	
78		Durability Test	1 day?	6/19/14 8:00 AM	6/19/14 5:00 PM	
79		**⊟Connection Testing**	**6 days?**	**6/19/14 8:00 AM**	**6/26/14 5:00 PM**	
80		**⊟Microprocessor**	4 days?	6/19/14 8:00 AM	6/24/14 5:00 PM	
81		Operating Voltage	2 days?	6/25/14 8:00 AM	6/26/14 5:00 PM	80
82		**⊟Software**	**5 days?**	**6/19/14 8:00 AM**	**6/25/14 5:00 PM**	
83		**⊟Find Bugs**	**5 days?**	**6/19/14 8:00 AM**	**6/25/14 5:00 PM**	
84		Use Product	2 days?	6/19/14 8:00 AM	6/20/14 5:00 PM	
85		Have others use...	5 days?	6/19/14 8:00 AM	6/25/14 5:00 PM	
86		Run test cases	3 days?	6/19/14 8:00 AM	6/23/14 5:00 PM	
87		**⊟Usability**	**4 days?**	**6/19/14 8:00 AM**	**6/24/14 5:00 PM**	
88		Alkaline	4 days?	6/19/14 8:00 AM	6/28/14 5:00 PM	
89		**⊟Re-design**	**6 days?**	**6/30/14 8:00 AM**	**7/7/14 5:00 PM**	**74**
90		**⊟Hardware**	**5 days?**	**6/30/14 8:00 AM**	**7/4/14 5:00 PM**	
91		Use CMOS Logic C...	5 days?	6/30/14 8:00 AM	7/4/14 5:00 PM	
92		Software	1 day?	6/30/14 8:00 AM	6/30/14 5:00 PM	
93		⊟Design	6 days?	6/30/14 8:00 AM	7/7/14 5:00 PM	
94		Delivery	1 day?	7/8/14 8:00 AM	7/8/14 5:00 PM	89

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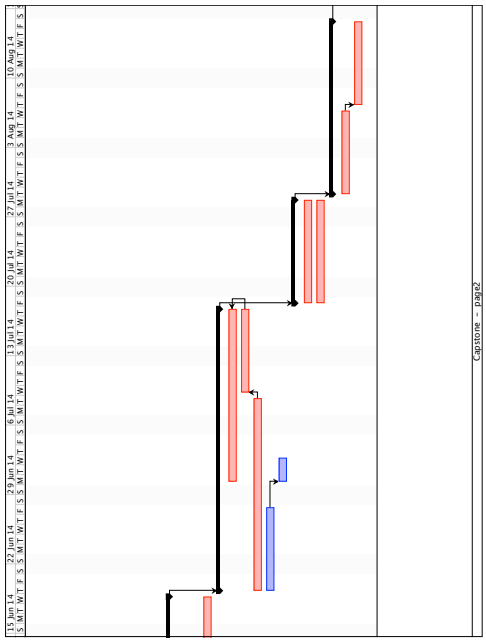
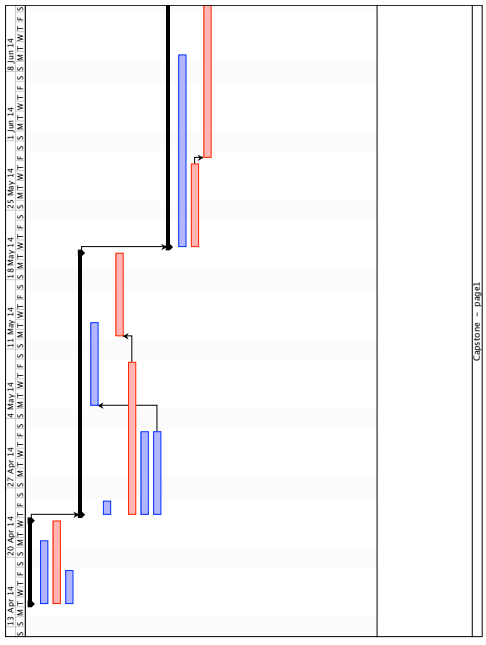
Gantt Chart





Hazard Assessment

The dangers from any of our proposed solutions is very minor. There is a slight choking hazard depending on the final size of the blocks, as well as the ability for the device to emit small sparks from the contacts. However, the electrical hazard is very minor on battery power and is unlikely to shock a human or cause a fire.

Conclusion

This document has presented the overall progress of our logic block puzzle device. Our current proposed solution should teach children the basics of digital logic, be suitable for a classroom environment, not endanger anyone using it, and get children interested in science, math, and computers.

Bibliography

[1] "Logicblocks kit." https://www.sparkfun.com/products/11006, 2014.

[2] "Capilano computing systems 'logicworks 5'." http://www.capilano.com/lww_5, 2014.

[3] "Zachtronics industries 'kohctpyktop'." http://www.zachtronics.com/kohctpyktop/kohctpyktop.htm, 2014.