CSE 331
Computer Organization
Homework 4 Report

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All instructions are working. I have implemented components also. The general test bench file contains component test benches.

Test Bench

1. **R Type, addn:**
   Instruction: 000000_00000_00001_00010_00000_100000
   R[s]: 00000000000000000000000000000011
   R[t]: 00000000000000000000000000000000
   R[d]: 00000000000000000000000000000011

   Result: (PASSED)
   R[s]: 00000000000000000000000000000011
   R[t]: 00000000000000000000000000000000
   R[d]: 00000000000000000000000000000011

2. **R Type, addn:**
   Instruction: 000000_11111_00001_01000_00000_100000
   R[s]: 01000000100001000000000000000000
   R[t]: 01000000100000000100000000000000
   R[d]: 00000000000000000000000000000000

   Result: (PASSED)
   R[s]: 10000000100000100010000000000000
   R[t]: 01000000100000000100000000000000
   R[d]: 00000000000000000000000000000010

3. **R Type, subn:**
   Instruction: 000000_00000_00001_00010_00000_100010
   R[s]: 10000000000000000000000000000011
   R[t]: 00000000000000000000000000000001
   R[d]: 00000000000000000000000000000010

   Result: (PASSED)
   R[s]: 10000000000000000000000000000010
   R[t]: 00000000000000000000000000000001
   R[d]: 00000000000000000000000000000010

4. **R Type, subn:**
   Instruction: 000000_01000_00001_01100_00000_100010
   R[s]: 10000000000000000000000000000001
   R[t]: 10000000000000000000000000000001
   R[d]: 11111111111111111111111111111111

   Result: (PASSED)
   R[s]: 00000000000000000000000000000000
   R[t]: 10000000000000000000000000000001
   R[d]: 00000000000000000000000000000000

5. **R Type, xorn:**
   Instruction: 000000_11110_01000_00010_00000_101010
   R[s]: 11111111111111111111111111111111
   R[t]: 10000000000000000000000000000001

R[d]: 00000000000000000000000000000010

Result: (PASSED)
R[s]: 01111111111111111111111111111110
R[t]: 10000000000000000000000000000001
R[d]: 00000000000000000000000000000011

6. **R Type, xorn:**
   Instruction: 000000_00000_00001_00010_00000_101010
   R[s]: 11111111111111111111111111111111
   R[t]: 00000000000000000000000000000000
   R[d]: 11111111111111111111111111111111

   Result: (PASSED)
   R[s]: 11111111111111111111111111111111
   R[t]: 00000000000000000000000000000000
   R[d]:00000000000000000000000000000010

7. **R Type, andn:**
   Instruction: 000000_00000_00001_00010_00000_100100
   R[s]: 11111111111111111111111111111111
   R[t]: 00000000000000000000000000000000
   R[d]: 11111111111111111111111111111111

   Result: (PASSED)
   R[s]: 00000000000000000000000000000000
   R[t]: 00000000000000000000000000000000
   R[d]: 00000000000000000000000000000000

8. **R Type, andn:**
   Instruction: 000000_10000_10001_00010_00000_100100
   R[s]: 00000000000000000000000000000000
   R[t]: 00111000100000100000100011000001
   R[d]: 00000000000000000000000000000000

Result: (PASSED)
R[s]: 00000000000000000000000000000000
R[t]: 00111000100000100000100011000001
R[d]: 00000000000000000000000000000000

9. **R Type, orn:**
Instruction: 000000_00000_00001_00101_00000_100101
R[s]: 00000000000000000000000000000000
R[t]: 00000000000000001111111111111111
R[d]: 10000000000000000000000000000011

Result: (PASSED)
R[s]: 00000000000000001111111111111111
R[t]: 00000000000000001111111111111111
R[d]: 00000000000000000000000000000011

10. **R Type, orn:**
Instruction: 000000_00000_00001_00101_00000_100101
R[s]: 11111111111111110000000000000000
R[t]: 00000000000000001111111111111111
R[d]: 00000000000000000000000000000011

Result: (PASSED)
R[s]: 11111111111111111111111111111111
R[t]: 00000000000000001111111111111111
R[d]: 00000000000000000000000000000010

11. **I Type, ori:**
Instruction: 001101_00000_00000_111111111111111
R[s]: 00000000000000000000000000000000
R[t]: 00000000000000000000000000000000
Imm: 00000000000000001111111111111111

Result: (PASSED)
R[s]: 00000000000000000000000000000000
R[t]: 00000000000000001111111111111111

12. **I Type, ori:**
Instruction: 001101_00000_00001_0000000000000000
R[s]: 11111111111111111111111111111111
R[t]: 00000000000000001111111111111111
Imm: 00000000000000000000000000000000

Result: (PASSED)
R[s]: 11111111111111111111111111111111
R[t]: 11111111111111111111111111111111

13. **I Type, lui:**
Instruction: 001111_00000_00000_111111111111111
R[t]: 00000000000000000000000000000000
Imm: 00000000000000001111111111111111

Result: (PASSED)
R[t]: 00000000000000001111111111111111

14. **I Type, lui:**
Instruction: 001111_00000_00000_0000000011111111
R[t]: 00000000000000000000000000000000
Imm: 00000000000000000000000011111111

Result: (PASSED)
R[t]: 00000000000000000000000011111111

15. I Type bne:

Instruction : 000101_00000_00001_0000000000000001
R[s] = 00000000000000000000000000000011
R[t] = 00000000000000000000000000000001

rs rt not equal, should do branch.

signExtImm = 00000000000000000000000000100000
branch addr = 00000000000000000000000000100000

RESULT = Branch To 32th line (PASSED)

16. I Type bne:

Instruction : 000101_00000_00001_0011100011000010000
R[s] = 00000000000000000000000000000000
R[t] = 00000000000000000000000000000000

rs rt equal, should not do branch.

RESULT = It is not branch (PASSED)

17. I Type beq:

Instruction : 000100_00000_00000_0011111111111111000
R[s] = 00000000000000000000000000000001
R[t] = 00000000000000000000000000000000

rs rt is not equal, should not do branch.

RESULT = It is not branch (PASSED)

18. **I Type beq:**

Instruction : 000100_00000_00000_00100000000000100
R[s] = 00011000011000001100000000000001
R[t] = 00011000011000001100000000000001

rs rt equal, should do branch.
RESULT = Branch To 4th line (PASSED)

19. **I Type lw:**

Instruction : 100011_00001_01111_0000000000000010
zero ext imm : 00000000000000000000000000000010

R[s] = 00000000000000000000000000000001
R[t] : 01111

Memoryfile 19th line

Mem[R[s] + signExtImm] =
00000000000000000000000000011001

R[t] = 00000000000000000000000000011001

(PASSED)

20. I Type lw:

Instruction : 100011_00001_01111_0000000000000100
zero ext imm : 00000000000000000000000000000100

R[s] = 00000000000000000000000000000001
Addr -> Rt : 01111

Memoryfile 23th line

Mem[R[s] + signExtImm] =
11111000000000000000000000011101

R[t] = 11111000000000000000000000011101

(PASSED)

21. I Type sw:

Instruction: 101011_00000_11111_0000000000000001
zero ext imm : 00000000000000000000000000000001

R[t]: 00000000000000000000000000000001

Mem[R[s] + signExtImm] =
00000000000000000000000000000001

(PASSED)

22. I Type sw:

Instruction: 101011_01100_11001_0000000000000001
zero ext imm : 00000000000000000000000000000011

R[t]: 11000110000001100000000000000001

Mem[R[s] + signExtImm] =
11000110000001100000000000000001

(PASSED)

23. J Type j:

Instruction : 000011_00000000000000000000100101
Jump to the 38th line.
(36th and 37th instruction don't print monitor
(PASSED)

24. J Type j:

Instruction : 000011_00000000000111000000111101
Jump to the out of instruction space.
Don't print any instruction on the monitor after this instruction run.
(PASSED)

Jr instruction set current PC to register[11111] content. IT is work.
(PASSED)

Jal instruction works similar to j instruction but this instruction writes PC+8 to register[11111]. (PASSED)