



## MSP432P401x Mixed-Signal Microcontrollers

### 1 Device Overview

#### 1.1 Features

- Core
  - ARM® 32-Bit Cortex®-M4F CPU With Floating Point Unit and Memory Protection Unit
  - Frequency up to 48 MHz
  - Performance Benchmark:
    - 1.196 DMIPS/MHz (Dhrystone 2.1)
    - 3.41 CoreMark/MHz
  - Energy Benchmark:
    - 167.4 ULPBench® Score
- Memories
  - Up to 256KB of Flash Main Memory (Simultaneous Read and Execute During Program or Erase)
  - 16KB of Flash Information Memory
  - Up to 64KB of SRAM (Including 8KB of Backup Memory)
  - 32KB of ROM With MSPWare Driver Libraries
- Code Security Features
  - JTAG and SWD Lock
  - IP Protection (Up to Four Secure Flash Zones, Each With Configurable Start Address and Size)
- Operating Characteristics
  - Wide Supply Voltage Range: 1.62 V to 3.7 V
  - Temperature Range (Ambient): –40°C to 85°C
- Ultra-Low-Power Operating Modes
  - Active: 90 µA/MHz
  - Low-Frequency Active: 90 µA (at 128 kHz)
  - LPM3 (With RTC): 850 nA
  - LPM3.5 (With RTC): 800 nA
  - LPM4.5: 25 nA
- Flexible Clocking Features
  - Programmable Internal DCO (up to 48 MHz)
  - 32.768-kHz Low-Frequency Crystal Support (LFXT)
  - High-Frequency Crystal Support (HFXT) up to 48 MHz
  - Low-Frequency Trimmed Internal Reference Oscillator (REFO)
  - Very Low-Power Low-Frequency Internal Oscillator (VLO)
  - Module Oscillator (MODOSC)
  - System Oscillator (SYSOSC)
- Enhanced System Options
  - Programmable Supervision and Monitoring of Supply Voltage
  - Multiple-Class Resets for Better Control of Application and Debug
  - Eight-Channel DMA
  - Real-Time Clock (RTC) With Calendar and Alarm Functions
- Timing and Control
  - Up to Four 16-Bit Timers, Each With up to Five Capture, Compare, PWM Capability
  - Two 32-Bit Timers, Each With Interrupt Generation Capability
- Serial Communication
  - Up to Four eUSCI\_A Modules
    - UART With Automatic Baud-Rate Detection
    - IrDA Encode and Decode
    - SPI (up to 16 Mbps)
  - Up to Four eUSCI\_B Modules
    - I²C (With Multiple-Slave Addressing)
    - SPI (up to 16 Mbps)
- Flexible I/O Features
  - Ultra-Low-Leakage I/Os (±20 nA Maximum)
  - Up to Four High-Drive I/Os (20-mA Capability)
  - All I/Os With Capacitive Touch Capability
  - Up to 48 I/Os With Interrupt and Wake-up Capability
  - Up to 24 I/Os With Port Mapping Capability
  - Eight I/Os With Glitch Filtering Capability
- Advanced Low-Power Analog Features
  - 14-Bit, 1-MSPS SAR ADC
  - Internal Voltage Reference With 10-ppm/°C Typical Stability
  - Two Analog Comparators
- Encryption and Data Integrity Accelerators
  - 128-, 192-, or 256-Bit AES Encryption and Decryption Accelerator
  - 32-Bit Hardware CRC Engine
- JTAG and Debug Support
  - Support for 4-Pin JTAG and 2-Pin SWD Debug Interfaces
  - Support for Serial Wire Trace
  - Support for Power Debug and Profiling of Applications



## 1.2 Applications

- Industrial and Automation
  - Home Automation
  - Smoke Detectors
  - Barcode Scanners
- Metering
  - Electric Meters
  - Flow Meters
- Health and Fitness
  - Watches
  - Activity Monitors
  - Fitness Accessories
  - Blood Glucose Meters
- Consumer Electronics
  - Mobile Devices
  - Sensor Hubs

## 1.3 Description

The MSP432P401x device family is TI's latest addition to its portfolio of efficient ultra-low-power mixed-signal MCUs. The MSP432P401x family features the ARM Cortex-M4 processor in a wide configuration of device options including a rich set of analog, timing, and communication peripherals, thereby catering to a large number of application scenarios where both efficient data processing and enhanced low-power operation are paramount.

Overall, the MSP432P401x is an ideal combination of the TI MSP430™ low-power DNA, advance mixed-signal features, and the processing capabilities of the ARM 32-bit Cortex-M4 RISC engine. The devices ship with bundled driver libraries and are compatible with standardized components of the ARM ecosystem.

**Device Information<sup>(1)</sup>**

PART NUMBER	PACKAGE (PIN)	BODY SIZE <sup>(2)</sup>
MSP432P401RIPZ MSP432P401MIPZ	LQFP (100)	14 mm × 14 mm
MSP432P401RIZXH MSP432P401MIZXH	NFBGA (80)	5 mm × 5 mm
MSP432P401RIRGC MSP432P401MIRGC	VQFN (64)	9 mm × 9 mm

- (1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in [Section 9](#), or see the TI website at [www.ti.com](http://www.ti.com).
- (2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 9](#).

## 1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the MSP432P401x devices.

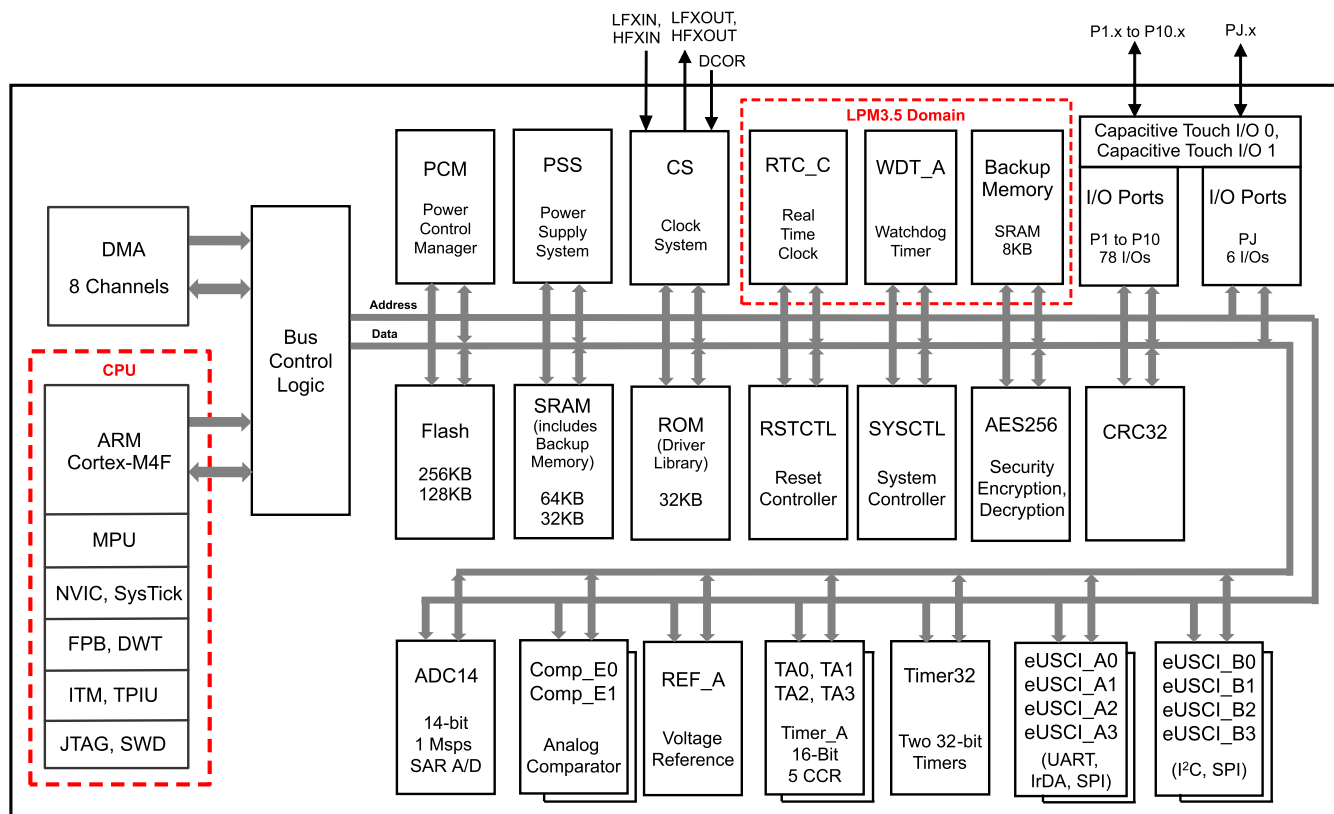


Figure 1-1. MSP432P401x Functional Block Diagram

The CPU and all the peripherals in the device interact with each other through a common AHB matrix. In some cases, there are bridges between the AHB ports and the peripherals. These bridges are transparent to the application from a memory map perspective and hence not shown in the block diagram.

PRODUCT PREVIEW

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## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 19, 2015 to March 30, 2015	Page
• Changed "Energy Benchmark" score from 153.3 to 167.4	1