## **Nicolas Kireyev, WORK LOG**

**MILESTONE 1-6 WORK:**

Wednesday, April 3, 2024

Met with team [3.5 hours]

* We decided to build a memory-memory based processor. A memory-memory based processor is convenient for the end user (programmers) as the instructions are simple and clean. We also have a lot of overlap between instruction types which is really convenient for implementation. We decided to include special allocated memory spots for built in purposes such as a dedicated zero (m0: immutable), a pseudocode temporary (m1: use by pseudocode instructions in case an additional memory space for temporary data is needed), a program counter (m2), and a stack pointer (m3). There are 4 total instruction types, all of which runs on 104-bit architecture.
* Helped with everything on the design doc and the brainstorming and creation of our intended implementation.

Thursday April 4, 2024 [2.5 hours]

* We opted to switch designs after meeting with Dr.Sher to a memory-memory approach with the exception of 4 registers: SP, VP, RA, and potentially a dedicated zero.

Saturday April 13, 2024 [3 hours]

* Brainstormed and started to create the instruction types and designating the allocated bits for each. We started to eliminate the use of some registers and decided to boil down our design to a single SP register design.

Sunday April 14, 2024 [1.5 hours]

* Talked and brainstormed more on how we would go about implementing the instruction types.

Monday April 15, 2924 [2 hours]

* We went through the first initial write up in our hardware to determine the likely list of components that we will need for the processor.

Tuesday April 16, 2024 [2 hours]

* Worked on creating the components list along with listing their inputs, outputs, behavior, and RTL symbols.

Wednesday April 17, 2024 [2 hours]

* Worked with team to design the RTL and created it via Lucid Charts. Talked about potentially going through with multicycle for the next milestone as it significantly shortens time it takes to branch.

Wednesday April 24, 2024 [2 hours]

* Worked with team to design the Datapath diagram and started to created it via Lucid Charts.

Friday April 26, 2024 [3 hours]

* Finished designing the datapath diagram via lucid charts with connection by name.

Sunday April 28, 2024 [2 hours]

* Finished designing the datapath diagram via lucid charts with full wire connections.

Tuesday April 30, 2024 [2 hours]

* Finished designing the datapath diagram via lucid charts with full wire connections and the control
* Overall Documentation Fixes

Friday May 3, 2024 [2 hours]

* Went over some of the tests that were completed and started documenting the tests on the document.

Monday May 13 [3 hours]

* Worked with team on documentation corrections. Continued to work on document.

Wednesday May 15 [4 hours]

* Worked with team on component testing documentation. Reviewed tests. Worked on document.
* Started to work on making the presentation.

Saturday-Sunday May 18-19 [4.5 hours]

* Finished working on presentation.