Mateo Olson Work Log

Wednesday, April 3

Met with team (3 hours)  
 We decided on our initial design of a memory-memory architecture that had 104-bit instructions. As a tradeoff for this, we decided to have few instruction types to shorten the opcode

Thursday, April 4

Met with team (2.5 hours)

After meeting with Stephen, we changed our design to a memory-memory with significantly less instruction space that used 4 user-accessible registers. We drew out designs and planned out 3 of the 4 registers.

Saturday, April 13

Met with team (3 hours)

We started to flesh out our idea, removing most of the registers as some were redundant and decided on having one dedicated implied register instead. This register would use a stack system making it so all that needed to be sent in an instruction would be an offset of the stack rather than an address. We also made a list of all of the function types we would need and decided on the bit allocations.

Sunday, April 14

Met with team (1 hour)

We went more in depth on the instruction types, and also worked out some strange quirks with how calling convention would go with our stack register

Monday, April 15

Met with team (2 hours)

We started writing the design document and made a basic hardware design, as well as finalizing our calling convention.

Tuesday, April 16

Met with team (2 hours)

Worked on making a list of all of the instructions, as well as working out a potential issue with the branch function.

Wednesday, April 17

Met with team (2 hours)

We worked through the cycles needed per each instruction and discussed a multicycle implementation, as well as fixing formatting issues with the documentation.

Monday, April 22

Uploaded empty Verilog files (1 hour)

I worked on making blank Quartus projects for each component we would need, as well as started on designing the MUX.

Wednesday, April 24

Met with team (2 hours)

We worked on the datapath, and I kept working on the basic components and writing a testbench. Realized that for the code to be edited in ModelSim and update within the simulation, it would have to be saved and compiled, and the simulation would have to stop and be restarted.

Friday, April 26

Finished MUX file and testbench, worked on register and adder files and testbenches (2 hours)

Wednesday, May 1

Finished the register files, as well as a left shift testbench and file (3 hours)

Friday, May 3

Finished the adder and adder TB (1 hour)

Saturday, May 11

Worked on trying to get multiple files to work together to implement a combination of Verilog files for a testbench (2 hours)

Sunday, May 12

Finished combined file and started writing testbench (4 hours)

Monday, May 13

Met with team (2 hours)

Worked on documentation with team, updated figures for the testbenches

Wednesday, May 15

Met with team (4 hours)

Worked on combined testbench and updated figures, also cleaned up document formatting

Wednesday, May 22

Met with team (2 hours)

Finalized our presentation and documentation, decided to divide up slides