Tulsi Manohar, Work Log

Team Lime, Section 1

MILESTONE 1:

Tuesday, December 19th, 2023.

- Discussed with the team during class time to get a sense of how we planned to take the project forward. Establishing smaller, achievable tasks and ensuring everyone is on the same page every step of the way.
- Set up communication channels and decided when we'd be available to meet. We also talked about the need to prioritize the project and make changes in individual schedules to accommodate work times where everyone would be able to attend rather than having smaller meetings and having to spend more time bringing the others to the same level of understanding.

Thursday, December 21st, 2023. @6pm

- Worked on instruction sets and bifurcating them into categories based on requirements. How we could optimize our work based on the limitations of the project requirements as compared to what we are comfortable with in RISC-V.
- Discussed and analyzed RISC-V instructions to understand what we needed vs what we could go without for our specific processor and language.
- We all worked on the descriptions and specific notes for instructions as required.
- Created a memory map, and list of registers and worked on space allocation.

Thursday, December 28th, 2023. @2am (Indian Standard Time)

- The meeting was planned and held an hour later, unfortunately, at that time I was asleep and I couldn't attend. However, I did work on understanding what was worked on by my fellow team members before I attended the next meeting to ensure that I could contribute to subsequent meetings effectively.

Tuesday, January 9th, 2024 @2pm

- We rechecked all past work to ensure our solutions make sense.
- We then spent a considerable amount of time working on translating our code from assembly language to machine code. The same was done for our example code fragments as well.
- I worked mainly on the relPrime, greater, gcd_end, and other instances where jalr and jal were called which needed work based off of addressing indexes.