Milestone 1:

Wednesday, September 27, 2023

Met with team [40 min]

- We talked about the basics of our project, eventually deciding that a Load/Store architecture would work best. We then planned a meeting for the following Sunday, and assigned members to research parts of the project we'd need to talk about.

Thursday, September 28, 2023

Instruction Research [15 min]

- Looked at examples of common instructions used and developed a list to bring to the group on Sunday.

Sunday, October 1, 2023

Group Meeting [4 hours]

- Started design document. Made decisions on register, and instruction design. Everyone took charge of a certain part of the document, and we finished all the content needed for Milestone 1.

Monday, October 2, 2023

Formatting [15 min]

- Finished up formatting the design document, and submitted to GitHub.

Milestone 2:

Saturday, October 7, 2023

Individual Milestone 2 Work [1 hour]

- Changed document name to be inline with guidelines
- Fixed various errors within instruction set
- Wrote Half of U-Type RTL instructions
- Wrote out file naming conventions
    - Wanted to prioritize something that was easy to write, while still being understandable
- Changed names of instruction types
    - Pokemon

Sunday, October 8, 2023

Group Milestone 2 Meeting [1 hour 40 min]

- Went over naming conventions
- Deliberated on RTL instructions and fixed a few errors
- Decided on generic components
    - Wanted the minimum amount to make sure our processor works
- Branching
    - Went over how we want to branch. Decided to base everything off of BEQ

Milestone 3:

Thursday, October 12, 2023

Group Milestone 3 Meeting [20 min]

- Divided up work for milestone 3.

Sunday, October 15, 2023

Individual Work [4 hrs]

- Reworked the entire component table to meet naming standards
    - Added symbols, missing signals
- Wrote out Register, Mux files (and their test benches), as well as their implementation plans.
    - Wanted Mux to be 2:1, since we can easily build other bigger muxes from it
    - Wanted Registers to reset or get value on a positive clock edge to allow for more reading/writing in the register file
- Wrote testing plan for Register File
    - Wanted the Register File to be able to read on positive edge, and write on negative edge to make our Register File more capable.
- Updated RTL tables
    - We decided to go back to a multicycle design to make it easier to program/create, over the harder to conceptualize Pipelining.

Wednesday, October 18, 2023

Group Meeting [50 mins]

- Talked about adding an ALUControl Component
    - Wanted a way to read select bits from the Immediate Genie, and use those bits to determine ALU's opcode. Wanted it to be separate from control to make things more modular/easier for the programmer (us).
- Divided up tasks for Milestone 4

Milestone 4:

Thursday, October 19, 2023

Individual Work [2 hrs]

- Wrote Register File, Testbench

    - Wanted to have everything in an array for easy storage
    - Decided to have it read/write on the positive clock edge for an easier time writing/debugging later
    - Had a function to zero all of the registers on startup to avoid issues with registers having junk values
    - Wrote the writing function so that it cannot write to x0, should always be grounded/zero
- Wrote Instruction Register, Testbench
    - Will always read the three registers (Rd, Rs1, Rs2), immediate will be handled by the ImmediateGenie based on the OpCode

Sunday, October 29, 2023

Individual/Partner Work [3 hrs]

- Debugging
- Wrote out integration plan for Register File, Instruction Register, and Immediate Genie
- Worked on Lab7 with Reilly

Milestone 5:

Thursday, October 30, 2023

Individual/Partner Work [3 hrs]

- Finished Lab7 with Reilly
- Implemented/Wrote/Tested Memory Wrapper
    - Decided to have our memory start at zero, and go up to 0x3FF
    - Had memory wrapper clamp top end of memory to ensure ^
- Worked on I/O
    - Decided to do different instructions for input and output, to allow for easy programming/logic

Tuesday, October 31, 2023

Group Work [2 hrs]

- Started on Processor Implementation

Wednesday, November 1, 2023

Group Work [2 hrs]

- Continued on Processor Implementation

Milestone 6:

Wednesday, November 2, 2023

Group Work [2 hrs]

- Worked on fixing issues identified in design meeting

Tuesday, November 7, 2023

Individual Work [8 hrs]

- Debugged lw/sw
- Reworked control states to have everything go to a reset state at the beginning -> proper control/flow of states
- Changed our IR to be negatively clocked, Regfile to be negatively clocked -> allowed for instructions to be read as quick as possible, so that they could be used in time. Broke a lot of things
- Fixed all of the broken things from ^

Group Work [2 hrs]

- Debugging branching and jumping

Wednesday, November 8, 2023

Group Work [2 hrs]

- Got processor to work with all instructions
- Debugged relPrime

Individual Work [1 hrs]

- Did all of the performance evaluations for the milestone
- Debugging and cleaning up code