Design Journal – henderae

Milestone 1

04/03/2022 – Group Meeting @ 6:00 p.m.

Was unable to make it to the meeting as some other commitments ran long, and then I had to still get dinner. I found out from Helen the next day that I was put in charge of the last three bullet points of number 1 under heading 3.

04/06/2022 – Individual Work

Was unable to come to lab period because I was still sick from the day prior. Opened the document and edited some formatting. Turned the instruction description and example programs into a table format. I also finished out the code fragments (while loop, for loop, if-else statements) with our assembly translation, machine code translation, and addresses.

Milestone 2

04/18/2022 to 04/21/2022 – Individual Work

Did not make it to the lab on the morning of 04/21, as I did not feel 100%. I did spend the entire lab time in my room working on the document. I created the set-up, calling, and use of return value for relPrime, and the input/output/control signal names/bit size/description. Spent ~8 hours on Milestone 2.

Milestone 3

04/24/2022 – Group Meeting

Met starting at 4:00 p.m., went until 6:30 p.m. working through the requirements for milestone three. I explained the bullet points about the descriptions of how to implement different components and what it meant by the integration plan. We decided to split the integration into four main parts, one for each person. The PC is separated as the first piece, as it combines some combinational logic plus the mux for the input into the PC. The second piece we decided was memory plus IR and MDR since the complex part of that is the mux going into memory and IR and MDR are just registers. The third piece was the accumulator itself plus SP because those are the core of our processor and how it functions. The fourth piece is the multiplexers that determine the input to the ALU, the ALU itself, and the pathway out of the ALU.

We also decided that I would digitize the data path and update the Input/Output/Control table with the control inputs from the data path plus whatever was added to the RTL descriptions after Zeen updated them. Jermaine oversaw writing up the integration plan and how each piece was going to be tested. Helen oversaw figuring out how to test individual components and the description of how to implement them. Finally, Zeen was to update the RTL symbols based on the feedback from Dr. Williamson at our milestone meeting and work on the partial implementation of some components.

04/27/2022 – Lab Time

Zeen didn't make it to the lab, and Jermaine was late, so Helen and I worked on the control bubble diagram. I spent the lab period digitizing it as well as making any last-minute changes to the data path. We discussed combining some of the stages Jermaine had done for the integration plan, but I didn't catch exactly what we were combining. Helen also clarified some things with Dr. Williamson about how our tests were expected to function in terms of timing since we are reading on the rising edge and writing on the falling edge.

Milestone 4

04/30/2022 – Group Meeting

We decided to split the integration plan up between people and give the components inside those steps to the people who were working on the integration plan step itself to minimize the need to wait for others to finish their work. I took the wires subsystem (Acc + Sp) and volunteered to make the left shift and test the zero extend and the sign extend plus making the 5-to-1 mux.

05/01/2022 – Individual Work

Made progress on my assigned part of the milestone and made the left shift and the 5-to-1 mux. Struggled to get the testbench to work.

05/02/2022 – Individual Work

Finally got the test benches to work and connected properly to test the component. Wrote the test benches for the zero extend and sign extend. At this point, I have all my components individually created and tested effectively. I just need to get the wires subsystem done.

Milestone 5

05/08/2022 to 05/09/2022 – Group Meeting/Class Time

I couldn't make the group meeting, as my mom surprised me by driving to Terre Haute for Mother's Day. Did connect with Helen on what I missed, and she talked with Jermaine and me on Monday about how this milestone was getting divided. She and Jermaine decided to do the data path full connection and integration as they had more time later in the milestone timeline. Zeen and I need to implement control.

05/11/2022 – Lab Time

I finished up the wires subsystem with a stupid number of typos on my part. I still need to finish the test bench, but Zeen and Helen told me about the memory incident they ran into. They said that we still have 16 bits, but it only acts and seems as if we have 10 bits, so the stack pointer must get preset to a specific value each time. Plus, the information from the stack pointer must get processed someway to add five zeros to it each time. Zeen said he would tell me what needs to be changed when he does the math to figure it out.