The main aim of this project is to produce a prototype of a magnetic device capable of inhibiting preterm uterine contractions and eventually preterm birth

Magnetic Field Pulse Generator to Inhibit Preterm Uterine Contractions

Project Report

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Introduction

This project entails the development of a new medical device to inhibit preterm uterine contractions using a magnetic field pulse. Premature birth and the attendant complications are the main cause of neonatal death and mortality and a major cause of maternal complications from preterm labour. It is among the greatest health problems in the world. Inhibiting preterm uterine contractions and eventually preterm birth is still an unsolved major problem for medicine and society with costs more than 25 billion dollars per year in the United States alone.

Our novel device will replace the electrical pulse with a magnetic pulse designed to have the same inhibitory effect on the contracting human preterm uterus without the discomforting side effect. Eventually our magnetic inhibition device would require human clinical trials to test the safety and feasibility of inhibiting preterm uterine contractions. The FDA is already aware of this innovative device concept and will review our device when it is ready for human clinical trials.

A pulsed magnetic field is known to alter cardiac contractions. The spontaneously contracting uterus, either at term or preterm is like the heart, physiologically and functionally. Based on these similarities the contracting preterm uterus should also respond to a pulsed magnetic field with decreased contractions.

The magnetic pulse parameters are technically likely to duplicate the electrical pulse parameters and have the same results without the pain side-effect. Demonstrating this with in vitro human myometrial studies is needed before FDA approval for human clinical studies.

These magnetic pulse parameters are similar to those used in transcranial magnetic stimulation, but because the uterine myometrial tissue has different conduction properties compared to the brain tissue, specific magnetic pulse parameters are needed to inhibit the preterm uterine muscle contractions.

This project mainly focuses to delineate the power supply and magnetic implementation of the prototyped device currently under works.

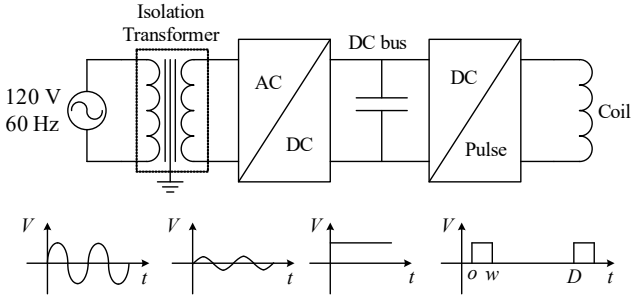

Fig. 1. Proposed power supply to drive the coils.

Power Supply

The basic idea is to generate low voltage high current pulses at 100-200 Hz to validate the data via a buck converter IC at a low voltage and constant current configuration, at 3A (the max current the IC supports). The system was controlled via an 8-bit microcontroller to take input from the HMI (Human Machine Interface) and generate the signals as require driving the power regulator IC (Analog's A6211/A6213).

To simplify the explanation, we will break down our system comprised of the multiple subsystems and delve into details with each one.

Power Regulator IC

We require a constant current, high frequency switching PWM controlled Buck converter.

A buck converter (step-down converter) is a DC-to-DC power converter which steps down voltage (while stepping up current) from its input (supply) to its output (load). It is a class of switched-mode power supply (SMPS) typically containing at least two semiconductors (a diode and a transistor, although modern buck converters frequently replace the diode with a second transistor used for synchronous rectification) and at least one energy storage element, a capacitor, inductor, or the two in combination. To reduce voltage ripple, filters made of capacitors (sometimes in combination with inductors) are normally added to such a converter's output (load-side filter) and input (supply-side filter).

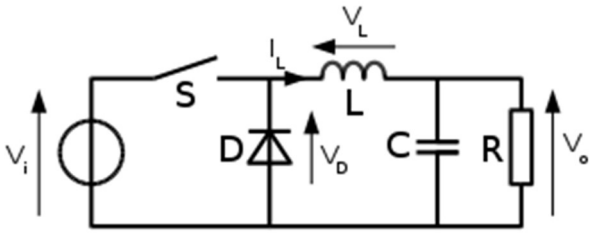

Fig. 2: Buck converter circuit diagram.

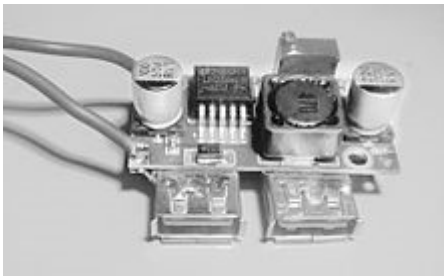

Fig. 3: A buck converter.

Switching converters (such as buck converters) provide much greater power efficiency as DC-to-DC converters than linear regulators, which are simpler circuits that lower voltages by dissipating power as heat, but do not step up output current.

Buck converters can be highly efficient (often higher than 90%), making them useful for tasks such as converting a computer's main (bulk) supply voltage (often 12 V) down to lower voltages needed by USB, DRAM and the CPU (1.8 V or less).

Theory of operation

The basic operation of the buck converter has the current in an inductor controlled by two switches (usually a transistor

and a diode). In the idealised converter, all the components are perfect. Specifically, the switch and the diode have zero voltage drop when on and zero current flow when off, and the inductor has zero series resistance. Further, it is assumed that the input and output voltages do not change over the course of a cycle (this would imply the output capacitance as being infinite).

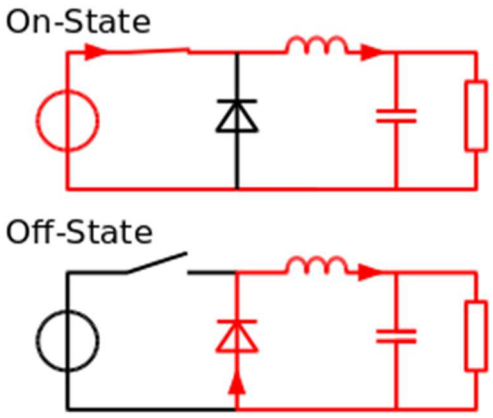

Fig. 4: The two circuit configurations of a buck converter: on-state, when the switch is closed; and off-state, when the switch is open (arrows indicate current according to the direction conventional current model).

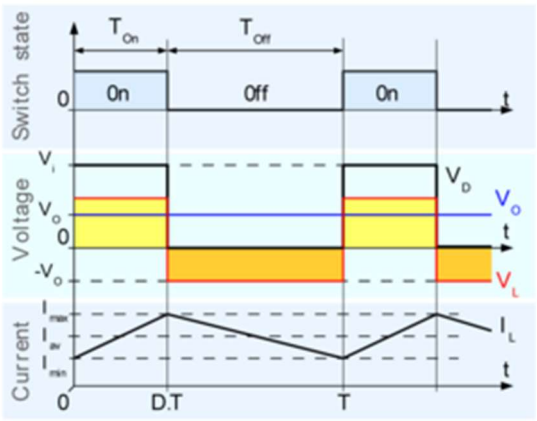

Fig. 5: Evolution of the voltages and currents with time in an ideal buck converter operating in continuous mode.

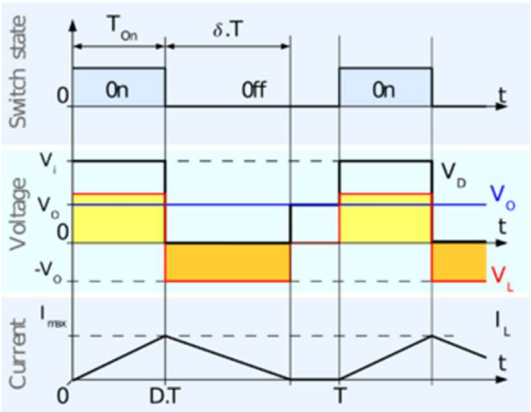

Fig. 6: Evolution of the voltages and currents with time in an ideal buck converter operating in discontinuous mode.

Non-ideal circuit

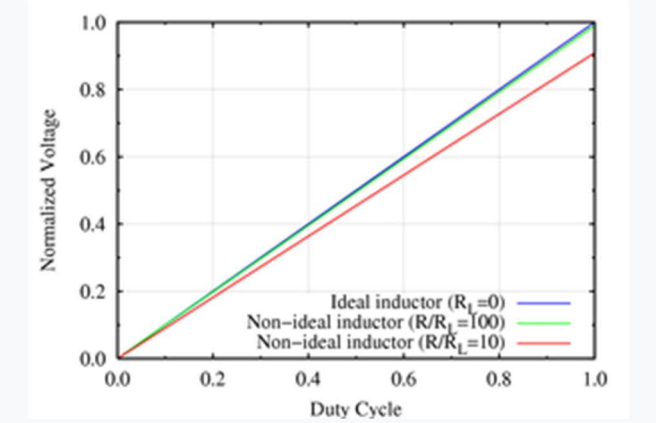

Fig. 7: Evolution of the output voltage of a buck converter with the duty cycle when the parasitic resistance of the inductor increases.

The previous study was conducted with the following assumptions:

- The output capacitor has enough capacitance to supply power to the load (a simple resistance) without any noticeable variation in its voltage.
- The voltage drops across the diode when forward biased is zero.
- No commutation losses in the switch nor in the diode.

These assumptions can be far from reality, and the imperfections of the real components can have a detrimental effect on the operation of the converter.

Efficiency factors

Conduction losses that depend on load:

- Resistance when the transistor or MOSFET switch is conducting.
- Diode forward voltage drop (usually 0.7 V or 0.4 V for Schottky diode)
- Inductor winding resistance
- Capacitor equivalent series resistance

Switching losses:

- Voltage-Ampere overlap loss
- Frequency $_{switch}$ x CV^2 loss
- Reverse latency loss
- Losses due driving MOSFET gate and controller consumption.
- Transistor leakage current losses, and controller standby consumption

The following were the drivers that were considered for this project too that were not used due to complexity issues with the implementation but are worth mentioning. *LT8613, LT3955*

LT8613

The LT8613 is a compact, high efficiency, high speed synchronous monolithic step-down switching regulator that consumes only 3µA of quiescent current. Top and bottom power switches are included with all necessary circuitry to minimize the need for external components. The built-in current sense amplifier with monitor and control pins allows accurate input or output current regulation and limiting. Low ripple Burst Mode operation enables high efficiency down to very low output currents while keeping the output ripple below $10mV_{P-P}$. A SYNC pin allows synchronization to an external clock. Internal compensation with peak current mode topology allows the use of small inductors and results in fast transient response and good loop stability. The EN/UV pin has an accurate 1V threshold and can be used to program V_{IN} undervoltage lockout or to shut down the LT8613 reducing the input supply current to 1µA. A capacitor on the TR/SS pin programs the output voltage ramp rate during start-up. The PG flag signals when VOUT is within ±9% of the programmed output voltage as well as fault conditions.

Features

- Rail-to-Rail Current Sense Amplifier with Monitor
- Wide Input Voltage Range: 3.4V to 42V
- Ultralow Quiescent Current Burst Mode Operation: 3µA IQ Regulating $12V_{IN}$ to $3.3V_{OUT}$
- Output Ripple < $10mV_{P-P}$
- High Efficiency Synchronous Operation: 95% Efficiency at 3A, $5V_{OUT}$ from $12V_{IN}$ 94% Efficiency at 3A, $3.3V_{OUT}$ from $12V_{IN}$
- Fast Minimum Switch-On Time: 40ns
- Low Dropout Under All Conditions: 250mV at 3A
- Allows Use of Small Inductors
- Adjustable and Synchronize-able: 200kHz to 2.2MHz
- Current Mode Operation
- Accurate 1V Enable Pin Threshold
- Internal Compensation
- Output Soft-Start and Tracking

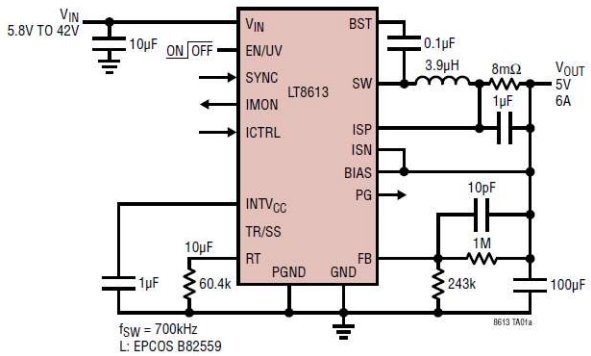

Fig. 8: 5V Step-Down Converter with 6A Output Current Limit.

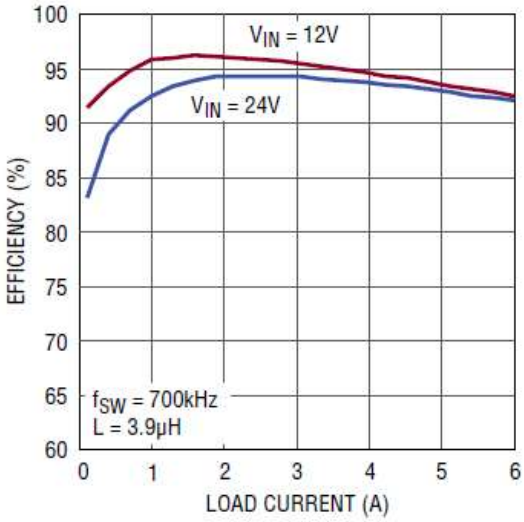

Fig. 9: Efficiency at 5V OUT.

LT3955

The LT3955 is a DC/DC converter designed to operate as a constant-current source and constant-voltage regulator. It features an internal low side N-channel MOSFET rated for 80V/3.5A. The LT3955 is ideally suited for driving high current LEDs, but also has features to make it suitable for charging batteries and supercapacitors. The fixed frequency, current mode architecture results in stable operation over a wide range of supply and output voltages. A voltage feedback pin serves as the input for several LED protection features and makes it possible for the converter to operate as a constant-voltage source. A frequency adjust pin allows the user to program the frequency from 100kHz to 1MHz to optimize efficiency, performance or external component size.

The LT3955 senses output current at the high side or at the low side of the load. The PWM input can be configured to self-oscillate at fixed frequency with duty ratio programmable from 4% to 96%. When driven by an external signal, the PWM input provides LED dimming ratios of up to 3000:1. The CTRL input provides additional analog dimming capability.

Features

- 3000:1 True Color PWM™ Dimming for LEDs
- Wide V_{IN} Range: 4.5V to 60V
- Rail-to-Rail Current Sense Range: 0V to 80V
- Internal 80V/3.5A Switch
- Programmable PWM Dimming Signal Generator
- Constant Current (±3%) and Constant-Voltage (±2%) Regulation
- Accurate Analog Dimming
- Drives LEDs in Boost, SEPIC, CUK, Buck Mode, Buck-Boost Mode, or Fly back Configuration
- Output Short-Circuit Protected Boost
- Open LED Protection and Reporting
- Adjustable Switching Frequency: 100kHz to 1MHz
- Programmable V_{IN} UVLO with Hysteresis
- C/10 Indication for Battery Chargers
- Low Shutdown Current: <1µA

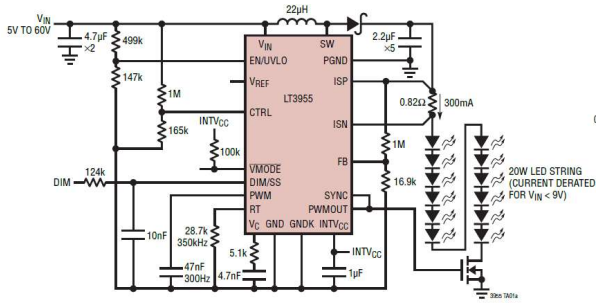

Fig. 10: 94% Efficiency 20W Boost LED Driver with Internal PWM Dimming.

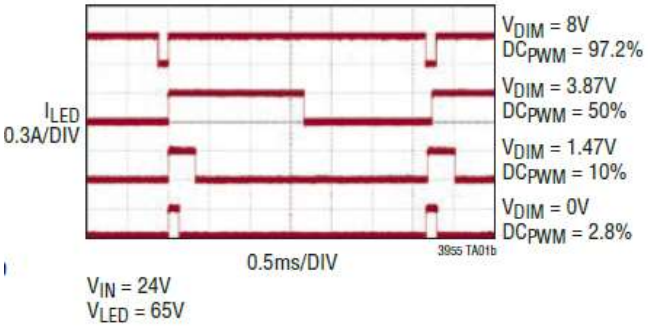

Fig. 11: PWM Dimming Waveforms at Various DIM Voltage Settings.

Basic Idea of Our Design

- We use an 8-Bit microcontroller to generate the PWM in our design.
- We'll be able to dynamically display the settings of the waveform on an OEM LCD display. This will help us perform all the tests with a lot of ease.
- The logic level of the circuitry will be 5V and the system will be powered via a Low Drop Out Linear Regulator with a High PSRR Value for noise suppression.
- The mode of operation of the external crystal will be a full swing oscillation mode at 16 Mhz.

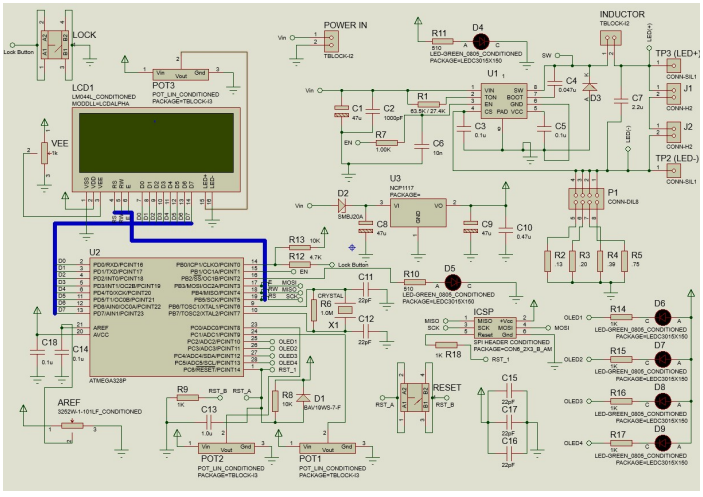

Fig. 12: The schematic design of the prototype designed.

Now let's dive deep into the subsystem design of this project

To simplify the entire project, we will break it down into following subsystems and go through each one of them in details.

Power System

- Power Regulation
- Power Conditioning
- ESD protection
- Surge and reverse polarity protection
- Voltage conflict resolution for USB input power supply

Control System

- Microcontroller Unit
- Oscillator circuitry
- Reset circuitry
- ICSP Interface

Human Machine Interface (I/O)

- Input for Frequency control
- Input for duty cycle control
- Input for LCD's brightness control
- LCD for displaying the circuit parameters
- Feedback LEDs

Power Switching system for driving the magnetic coils

- Inductor Drive Circuitry
- Current Sense Feedback Network
- Output Load
- Filter Circuits
- Protection systems
- Switcher Frequency Preset

Power System

It is the main system of the device that controls and conditions the power to be supplied to the controller and I/O system of the devices. It comprises of the following subsystems

Power Regulation

Power regulation is taken care of by a high PSRR (Power Supply Rejection Ratio) Low Drop Out (LDO) value linear regulator that outputs 5Volts to the microcontroller unit and the LCD. Here we have employed a NCP1117 series IC for its versatility and high current sourcing capacity that eliminates additional requirements for the power systems like staged power conversion.

The NCP1117 series are low dropout positive voltage regulators that can provide an output current that is more than 1.0 A with a maximum dropout voltage of 1.2 V at 800 mA over temperature.

Power Conditioning

This subsystem makes sure that the energy remains stable and doesn't fluctuate with switching or any sudden loading or fluctuations. It also makes sure that voltage post regulation remains constant and glitch free.

To achieve this, we used 2 different value capacitors rated 47uF and .1uF in parallel both of which acts a band pass filter for all the substantial frequencies that filters out majority of the ripples out of the circuitry to provide a stable and constant power supply.

ESD (Electrostatic Discharge) protection

Electrostatic Discharge (ESD) is the sudden flow of electricity between two electrically charged objects caused by contact, an electrical short, or dielectric breakdown. A buildup of static electricity can be caused by tribocharging or by electrostatic induction. The ESD occurs when differently-charged objects are brought close together or when the dielectric between them breaks down, often creating a visible spark. The energy flow during the discharge can easily fry the circuit that is in touch with it including but not limited to reset circuitry or any of the microcontroller GPIO pins or even the Vcc pins rendering the entire IC useless.

Mainly we are supposed to employ it on the reset circuitry on our device as we will be programming via an external programmer that has its own USB ESD protection system. So, we ended up employing BAV19WS-7-F Schottky Diode connected to reset pins that can direct the surges back to the regulator instead of harming the reset circuit.

But in case we need to incorporate this into our design at all points, The TPD4S012 is a four-channel Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode array for USB chargers and USB On-The-Go (OTG) interfaces.

Surge and reverse polarity protection

Surges are sudden increase of power in the circuit that might be caused by sudden discharges or switching. So, to make sure that the circuit is protected against surges, reverse biased Zener diodes as well as filter capacitors are employed at all the sensitive power areas that are prone to surges. Any surges and power inflections on the voltage side will be taken are by the Zener diodes and the capacitors. The current limiting resistors on each GPIO and communication pins makes sure that the current in any component does not exceed its rating. Suitable termination resistors are employed at the end of each communication pins to eliminate reflections as well as deter and induced noise.

To deal with reverse polarity protection (to make sure we don't fry the circuit in case we accidently connect the circuit in a wrong order i.e., power to ground and ground to power.), we use diodes in the input connections that only allows the power to flow in the circuit if the correct polarity is established.

Voltage conflict resolution for USB input power supply

The Dual Supply Problem

Our prototype device allows us to connect a voltage source at the power input terminal connector and through the ICSP pin header, and while it's obvious that the ICSP V_{CC} pin and input power terminal shouldn't be used simultaneously, there are many cases where we might need to keep the prototype device powered by a battery during a USB connect/disconnect.

When you connect the USB cable, you instantly provide a 5V source that you know can power the device when it's just sitting on the desk. However, you also have an external power connection to it that is creating a nicely regulated 5V through the methods covered in power regulation section. Since the 5V Fixed LDO Regulator and the ICSP 5V supply would both be trying to supply voltage and current at the same time, to the same things, that means they'd essentially be connected to each other. Neither of those are ideal voltage sources, meaning that neither is EXACTLY 5.00000V, they all have tolerance ranges and output will vary based on environmental conditions like temperature – TL/DR: their voltage level won't be equal. What happens when we connect two voltage sources of different levels in parallel? We get a current loop flowing from the high voltage source to the low voltage source, and that's bad, particularly if that current flow is going back up our USB cable into our laptop. We don't want that to happen.

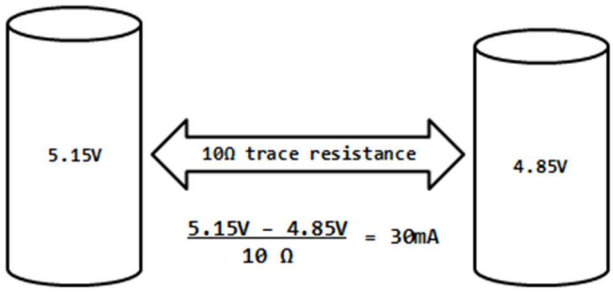

Fig. 13: Current flow calculation for low voltage difference with a low trace resistance.

The solution is to automatically cut the 5V line coming from the ICSP (just the 5V supply, not the SPI serial communication), the moment any voltage is detected on V_{IN} high enough to kick on the 5V Fixed LDO. It would be great if we could just write some code that says, "**if (VIN >= 7V) then turn off (USB_5V);**". Well, for this, how about implementing that "**if**" statement in hardware. To do that we need to use an Operational Amplifier (op-amp).

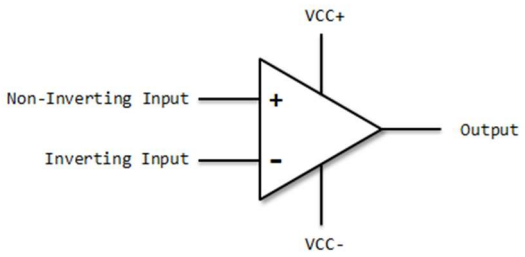

Fig. 14: Op-Amp used as a comparator.

For our requirements, an op-amp is an integrated circuit that accepts two inputs, the "non-inverting" and the "inverting" inputs and attempts to balance any difference — even very small differences — between the two by driving the output as close to the op-amp's supply voltages as it can, VCC+ and VCC-. This simple transaction can be harnessed to

accomplish many different tasks. You can take the output and feed it back to one of the inputs, you can add resistors and capacitors in there to create amplification. But here, what we care about is: if there's a difference between the non-inverting and inverting inputs, it will try to balance it by driving the output to VCC+ or VCC- and doing it very fast.

Voltage Conflict Management: The Op-amp as Comparator

Let's list what we know about our circuit before we delve into how we're going to mitigate it.

Voltages

- We have +5V coming from our ICSP cable. Call this USB_{VCC} (since it is originally coming from USB only).
- We have +5V coming from our 5V Fixed LDO. Let's call this 5V_LDO.
- We have some higher voltage coming from the Input power terminal header. Let's call this V_{IN}.
- We have +3.3V coming from a 3V3 Fixed LDO. Let's call this 3V3_LDO.

Desired Outcomes

- When USB_{VCC} is connected, and V_{IN} is not connected, we want to allow USB_{VCC} to supply 5V.
- When USB_{VCC} is not connected and V_{IN} is connected, we want to allow V_{IN} to generate 5V_LDO to supply 5V.
- When USB_{VCC} is connected, and V_{IN} is connected, we want to cut off USB_{VCC} and allow V_{IN} to generate 5V_LDO to supply 5V.

Using the four different voltages and some hardware, we want to be able to create the three outcomes. We do this by using an op-amp as a comparator. We'll test the voltage level of the V_{IN} rail, and if it's below some reference voltage, we'll allow the USB_{VCC} rail to supply voltage. If it's above some reference voltage, we'll prevent the USB_{VCC} rail from supplying voltage.

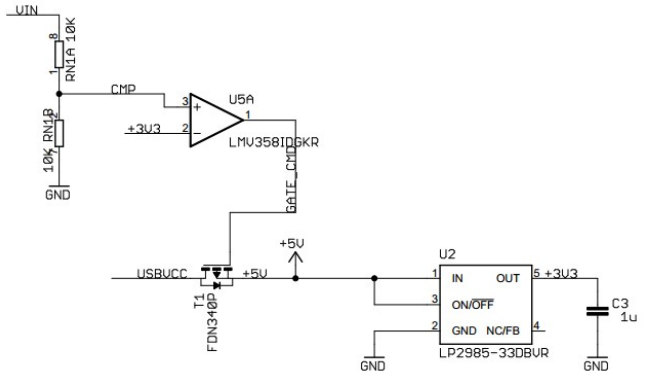

Fig. 15: Voltage Conflict Management Circuit.

When V_{IN} is disconnected, the CMP net entering the non-inverting input of the op-amp, U5, is at GND (tied through the 10K resistor, RN1B, to GND), and the inverting input of U5 is held at a reference voltage of +3.3V. Because the non-inverting input is lower than the inverting input, the output is driven to VCC-, in this case GND. The output is connected to the gate of the P-channel MOSFET, T1, and since it's at GND, that means the MOSFET will allow electrons to flow like a closed switch. USB_{VCC} is then connected to the +5V net, and powers U2, which is a 3.3V Fixed LDO Regulator. The output of that LDO supplies the 3V3 voltage to the shield pin header, but also is used as the voltage reference for the comparator.

When V_{IN} is connected, it energizes the voltage divider at the non-inverting input of U5. The op-amp will compare this against the 3V3 reference on the inverting input. The voltage divider is comprised of a pair of 10K resistors, so you'll see exactly half the V_{IN} voltage at the non-inverting input. For anything to happen that's different than our previous state, we would need at least **6.61V (6.61V / 2 = 3.305V)**. Realistically, because of the drop out voltage, this voltage will be at least 7V (divided by two) and more likely 9V (divided by two). Regardless, as soon as you cross that threshold, the op-amp will flip to the opposite state and will send VCC+ to the output. With 5V at the output, that means 5V at the gate of the P-channel MOSFET and it flips the MOSFET into an OFF state, cutting USB_{VCC} out. Since in this case, USB_{VCC} isn't connected, it doesn't really matter. 5V is still supplied to the 3V3 Fixed LDO from the +5V rail (from the 5V Fixed LDO), which preserves the reference voltage of the comparator.

Control System

Basically, acting the brains in the device that takes all the inputs by the user, processes it and sets the output to the desired values and displays them on the LCD is the control system is the functioning control system that we are now going to study in detail. But some major subsystems can be expounded as follows.

Microcontroller Unit: this is the main processing unit of the systems that handles all the processing works. For our project we have used an ATmega-328p, an 8 Bit RISC architecture based AVR microcontroller in PDIP packaging operated over an external oscillator at 16Mhz.

Oscillator circuitry: This acts as the clock source for the microcontroller that operates at 5 volts at full-swing to provide strong signals. Although, this increases the net power consumption of the circuitry, we still use it to make sure that any interference source in the vicinity does not render our clock circuitry vulnerable.

A load capacitor is connected in parallel to each rail the value of which is recommended by the manufacturer of the crystal and is used to provide stability to the oscillator circuitry. The value is usually in tens of Picofarads and ours came with a recommendation of 22pF.

Usually the other development platforms, say, Arduino employs ceramic resonators to generate clock signals over the same microcontroller interface to save space and reduce production costs by eliminating load capacitor costs, but

those oscillators are less accurate and as compared to crystal oscillators.

This type of oscillators frequency varies with the input power. Let's see the following diagram to get a better idea.

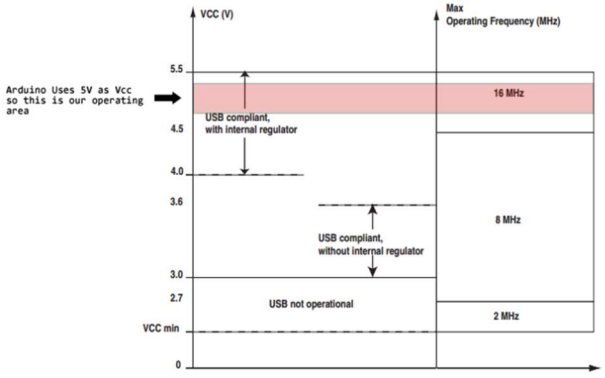

Fig. 16: Different Oscillation Frequency over different voltage levels.

Parallel Resistor

The parallel resistor of 1M ohms is acting as a feedback resistor for the microcontroller's internal inverter to which the crystal is connected and biases the inverter's input into the linear region. "Biasing into the linear region", means that it is amplifying the crystal's oscillation without ever fully saturating at one of the voltage rails. When power is first applied to the system, this feedback resistor helps the components that make up the oscillator circuit, both internal to the micro and the external parts we provide, to get oscillations at the correct frequency faster.

Reset circuitry

This circuit provides a manual interface to reset the microcontroller via a press of a button and is also forms an important part in the ICSP port that allows us to load program the microcontroller in the circuit itself over an SPI bus. This operates in an active low operation mode. An external 10k pull-up resistor is used to make ensure an additional pull-up input apart from the internal 1M ohm resistor.

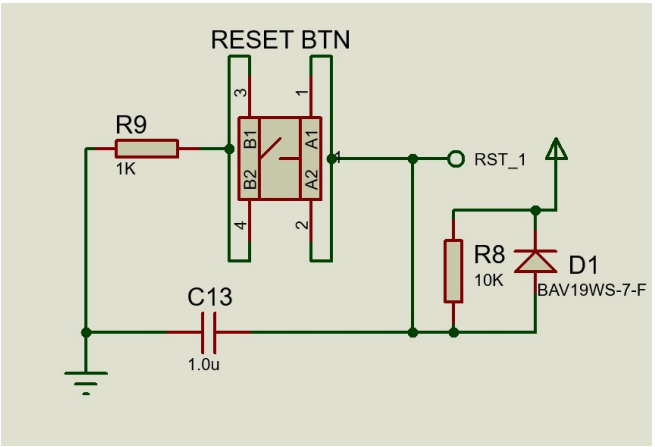

Fig. 17: Reset Schematic (ESD protection not shown).

When the reset button is pressed, the microcontroller's reset pin goes low. The ground and the reset pin are shorted via a 1k resistor to avoid a sudden current flow in the trace that might damage the circuit in any way.

Also, to take care of the bouncing caused by the press button, we use a 1µF capacitor that discharges the current slowly through the current limiting resistor.

ICSP Interface

ICSP stands for In Circuit Serial Programming is a 6-pin interface that allows us to program the microcontroller board via a SPI bus. It basically transmits the data in the EEPROM of the microcontroller after conducting a device check and compatibility routine (like device's signature etc.). To program via ISCP port we use an external programmer (for this device we employ a Pocket AVR Programmer) that takes the compiled code in hex format and burn it in the controller's memory. The Pins functionality goes as follows:

MISO: Master in Slave Out, VCC: input voltage (here 5V), SCK: Serial Clock, MOSI: Master Out Slave In, RST: Reset, GND: Ground

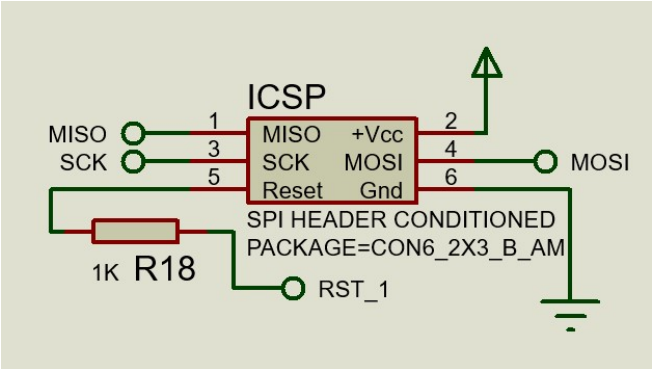

Fig. 18: ICSP header pin configuration for in circuit serial programming implemented in the device (Pull-up resistors not shown).

Its recommended to pull-up MOSI, MISO and SCK lines via a 10k resistors if there is a possibility that the field in which debugging is going to be conducted is prone to noise.

Human Machine Interface (I/O)

The following are the inputs that are used to set the control parameters of the buck converter IC. The following 3 inputs are given by 3 independent1K volume potentiometer

- Input for Frequency control
- Input for duty cycle control
- Input for LCD's brightness control

Push Button is purposed used to lock the parameters of the frequency and duty cycle. Once the microcontroller reads these parameters via a multiplexed ADC peripheral, the press of the button acknowledged the controller to set the required settings. To tackle the button bouncing issues, a software delay based debouncing function is implemented.

LCD is used for displaying the circuit parameters, the offset value settings, the conditioned values to effortlessly convert the read ADC values to human readable format.

Feedback LEDs are used to debug and read flags for interrupt driven functions as well as control parameters. One of the LEDs are connected to mirror the exact PWM output of the main driver line to get a dynamic feedback (a bit crude though) of the current PWM state. The microcontroller sources the PWM driven LED and sinks the rest of the LEDs for an optimal implementation. (this is because the controller can source currents as high as 20mA but can sink up to 40mA per pin)

And for futureproofing purposes, added are some more worm gear based linear potentiometer that can be used to change ADC peripheral's reference voltage as well as LCD screen's contrast should the ground references need be altered.

Power Switching system for driving the magnetic coils

A led drier IC is used to generate PWM pulses at 3 Amps to power up an inductor that will generate magnetic fields inside an inductor coils to stimulate the muscles/tissue areas over which the device will be mounted on.

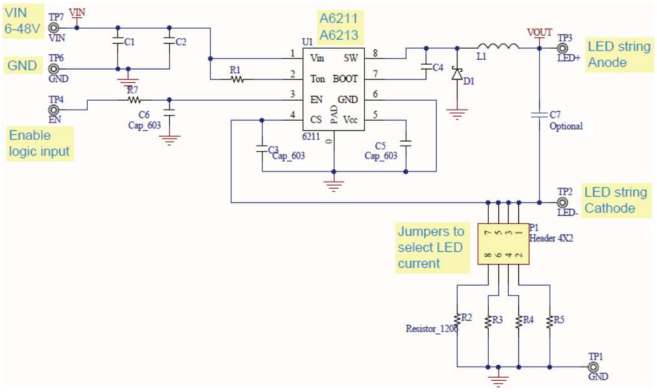

Fig. 19: A6211 Schematic Implementation.

A true average current is output using a cycle-by-cycle, controlled on-time method. Output current is user-selectable by an external current sense resistor. Output voltage is automatically adjusted to drive various numbers of LEDs in a single string. This ensures the optimal system efficiency.

Pulses are accomplished by a direct logic input pulse width modulation (PWM) signal at the enable pin. We have connected the enable pin of the IC to the PWM output pin of the microcontroller.

Functional Description

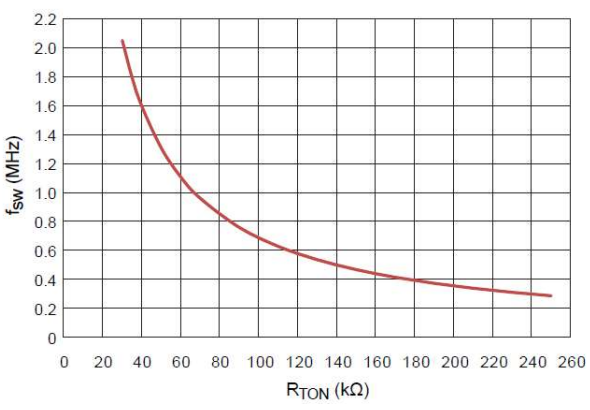

Fig. 20: Switching Frequency versus R_{TON} Resistance.

The A6211 operates in fixed on-time mode during switching. The on-time (and hence switching frequency) is programmed using an external resistor connected between the V_{IN} and T_{ON} pins, as given by the following equation:

$$t_{ON} = k \times (R_{ON} + R_{INT}) \times (V_{OUT} / V_{IN})$$
$$f_{SW} = 1 / [\, k \times (R_{ON} + R_{INT})]$$

where k = 0.0139, with f_{SW} in MHz, t_{ON} in µs, and R_{ON} and R_{INT} (internal resistance, 5 kΩ) in kΩ (see Figure 20).

Enable and Dimming

The IC is activated when a logic high signal is applied to the EN (enable) pin. The buck converter ramps up the LED current to a target level set by R_{SENSE}. When the EN pin is forced from high to low, the buck converter is turned off, but the IC remains in standby mode for up to 10 ms. If EN goes high again within this period, the LED current is turned on immediately. Active dimming of the LED is achieved by sending a PWM (pulse-width modulation) signal to the EN pin. The resulting LED brightness is proportional to the duty cycle (t_{ON} / Period) of the PWM signal. A practical range for PWM dimming frequency is between 100 Hz (Period = 10 ms) and 2 kHz. At a 200 Hz PWM frequency, the dimming duty cycle can be varied from 100% down to 1% or lower. If EN is low for more than 17 ms, the IC enters shutdown mode to reduce power consumption. The next high signal on EN will initialize a full startup sequence, which includes a startup delay of approximately 130 µs. This startup delay is not present during PWM operation. The EN pin is high-voltage tolerant and can be directly connected to a power supply. However, if EN is higher than the V_{IN} voltage at any time, a series resistor (1 kΩ) is required to limit the current flowing into the EN pin. This series resistor is not necessary if EN is driven from a logic input.

Output Voltage and Duty Cycle

Essentially, the output voltage of a buck converter is approximately given as:

$$V_{OUT} = V_{IN} \times D - V_{D1} \times (1 - D) \approx V_{IN} \times D,$$
$$\text{if } V_{D1} << V_{IN}$$
$$D = t_{ON} / (t_{ON} + t_{OFF})$$

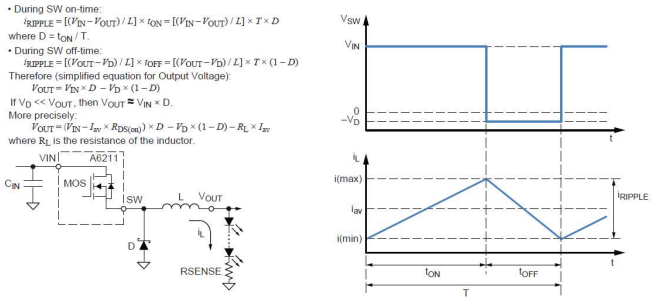

Fig. 21: Buck Controller Equations, and Reference Circuit and Waveforms.

where D is the duty cycle, and V_{D1} is the forward drop of the Schottky diode D1 (typically under 0.5 V).

Figure 22 shows how the minimum and maximum output voltages vary with LED current (assuming R_{DS} (on) = 0.4 Ω, inductor DCR = 0.1 Ω, and diode V_f = 0.6 V).

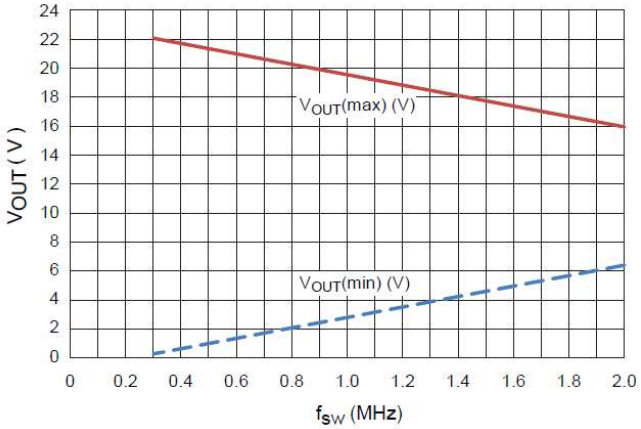

Fig. 22: Minimum and Maximum Output Voltage versus Switching Frequency (V_{IN} = 24 V, i_{LED} = 2 A, minimum t_{ON} and t_{OFF} = 150 ns)

If the required output voltage is lower than that permitted by the minimum t_{ON}, the controller will automatically extend the t_{OFF}, to maintain the correct duty cycle. This means that the switching frequency will drop lower when necessary, while the LED current is always kept in regulation.

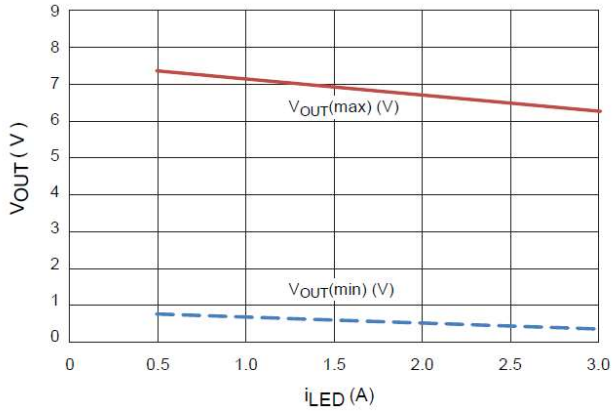

Fig. 23: Minimum and Maximum Output Voltage versus i_{LED} current (V_{IN} = 9 V, f_{SW} = 1 MHz, minimum t_{ON} and t_{OFF} = 150 ns)

Thermal Budgeting

The A6211 can supply a 3 A current through its high-side switch. However, depending on the duty cycle, the conduction loss in the high-side switch may cause the package to overheat. Therefore, care must be taken to ensure the total power loss of package is within budget. For example, if the maximum temperature rise allowed is ΔT = 50 K at the device case surface, then the maximum power dissipation of the IC is 1.4 W. Assuming the maximum R_{DS} (on) = 0.4 Ω and a duty cycle of 85%, then the maximum LED current is limited to 2 A approximately. At a lower duty cycle, the LED current can be higher.

Fault Handling

The A6211 is designed to handle the following faults:

- Pin-to-ground short
- Pin-to-neighboring pin short
- Pin open
- External component open or short
- Output short to GND

Note that the SW pin overcurrent protection is tripped at around 3.75 A, and the part shuts down immediately. The part then goes through startup retry after approximately 380 µs of cool-down period.

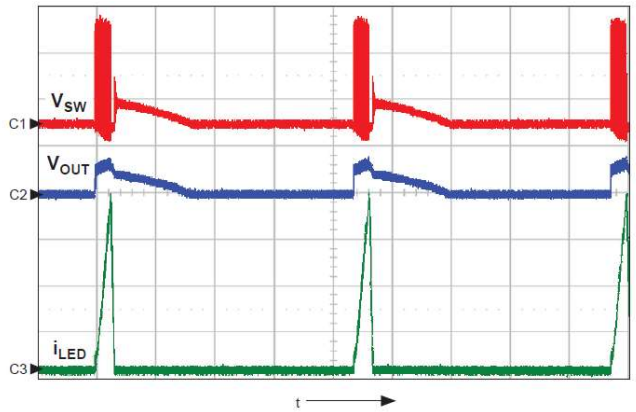

Fig. 24: A6211 overcurrent protection tripped in the case of a fault caused by the sense resistor pin shorted to ground; shows switch node, V_{SW} (ch1, 10 V/div.), output voltage, V_{OUT} (ch2, 10 V/div.), LED current, i_{LED} (ch3, 1 A/div.), t = 100µs/div.

As another example, the waveform in Figure 25 shows the fault case where external Schottky diode D1 is missing or open. As LED current builds up, a larger-than-normal negative voltage is developed at the SW node during off-time. This voltage trips the missing Schottky detection function of the IC. The IC then shuts down immediately and waits for a cool-down period before retrying.

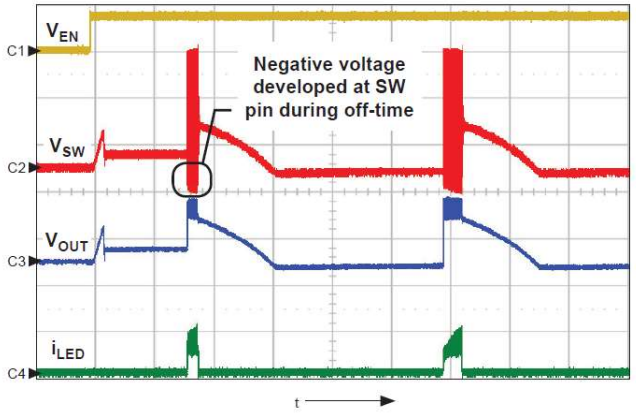

Fig. 25: Startup waveform with a missing Schottky diode; shows Enable, V_{EN} (ch1, 5 V/div.), switch node, V_{SW} (ch2, 5 V/div.), output voltage, V_{OUT} (ch3, 5 V/div.), LED current, i_{LED} (ch4, 500 mA/div.), t = 100µs/div.

Inductor Selection Chart

The chart in Figure 26 summarizes the relationship between LED current, switching frequency, and inductor value. Based on this chart: Assuming LED current = 2 A and f_{SW} =1 MHz, then the minimum inductance required is L = 10 µH to keep the ripple current at 30% or lower. (Note: V_{OUT} = V_{IN} / 2 is the worst case for ripple current). If the switching frequency is lower, then either a larger inductance must be used, or the ripple current requirement must be relaxed.

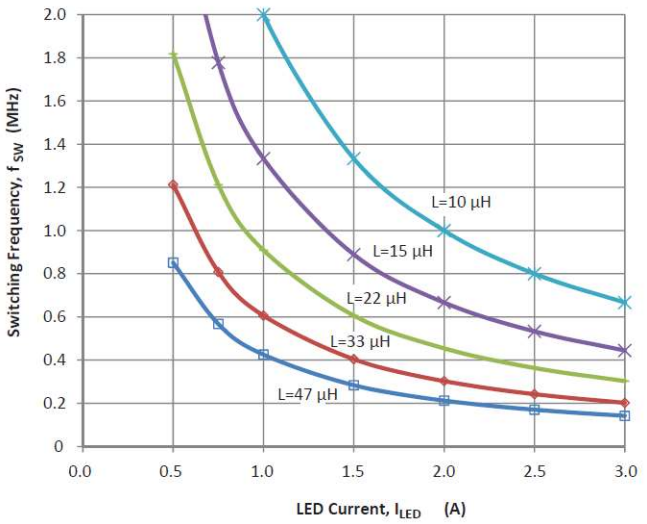

Fig. 26: Inductance selection based on I_{LED} and f_{SW}; V_{IN} = 24 V, V_{OUT} = 12 V, ripple current = 30%

Additional Notes on Ripple Current

- For consistent switching frequency, it is recommended to choose the inductor and switching frequency to ensure the inductor ripple current percentage is at least 10% over normal operating voltage range (ripple current is lowest at lowest V_{IN}). If ripple current is less than 10%, the switching frequency may jitter due to insufficient ripple voltage at CS pin. However, the average LED current is still regulated.
- There is no hard limit on the highest ripple current percentage allowed. A 60% ripple current is still acceptable, if both the inductor and LEDs can handle the peak current (average current × 1.3 in this case). However, care must be taken to ensure the valley of the inductor ripple current never drops to zero at the highest input voltage (which implies a 200% ripple current).
- In general, allowing a higher ripple current percentage enables lower-inductance inductors to be used, which results in smaller size and lower cost. The only down-side is the core loss of the inductor increases with larger ripple currents. But this is typically a small factor.
- If lower ripple current is required for the LED string, one solution is to add a small capacitor (such as 2.2 µF) across the LED string from LED+ to LED–. In this case, the inductor ripple current remains high while the LED ripple current is greatly reduced.

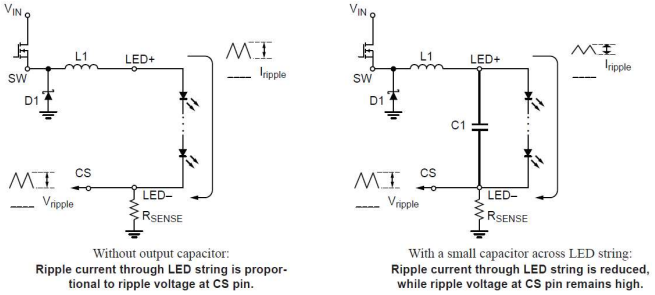

Fig. 27: Ripple current and voltage, with and without Shunt Capacitor.

Output Filter Capacitor

The A6211 is designed to operate without an output filter capacitor, to save cost. Adding a large output capacitor is not recommended. In some applications, it may be required to add a small filter capacitor (up to several µF) across the LED string (between LED+ and LED-) to reduce output ripple voltage and current. It is important to note that:

- The effectiveness of this filter capacitor depends on many factors, such as: switching frequency, inductors used, PCB layout, LED voltage and current, and so forth.
- The addition of this filter capacitor introduces a longer delay in LED current during PWM dimming operation. Therefore, the maximum PWM dimming ratio is reduced.
- The filter capacitor should NOT be connected between LED+ and GND. Doing so may create instability because the control loop must detect a certain amount of ripple current at the CS pin for regulation.

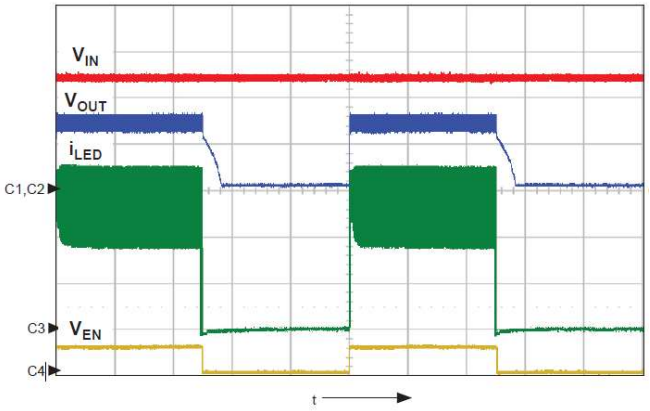

Fig. 28: Operation without using any output capacitor across the LED string Operating conditions: at 200 Hz, V_{IN} = 24 V, V_{OUT} = 15 V, f_{SW} = 500 kHz, L = 10 µH, duty = 50%

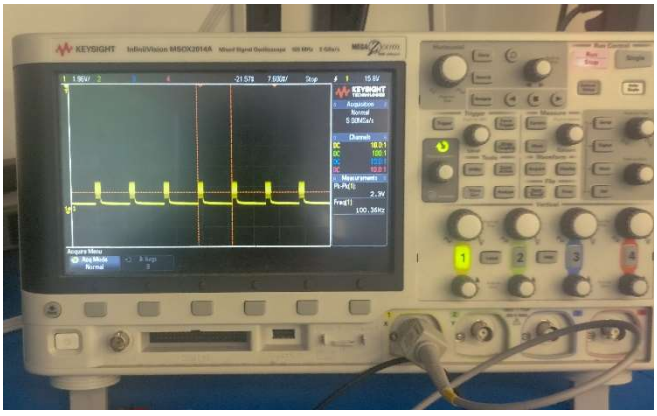

Fig. 29: Obtained waveform without using any output capacitor across the LED string. Operating conditions: at 100 Hz, V_{IN} = 12 V, V_{OUT} = 2.1 V, f_{SW} = 1.1 MHz, L = 12 µH(not correct), duty cycle = 20%

Figure 29 above shows the obtained waveform that our device under test generates when no output capacitor is connected. We can observe that the ripples obtained are very substantial.

We will observe that these ripples will be reduced when we connect a 0.68µF capacitor (Fig. 31/ Fig. 32).

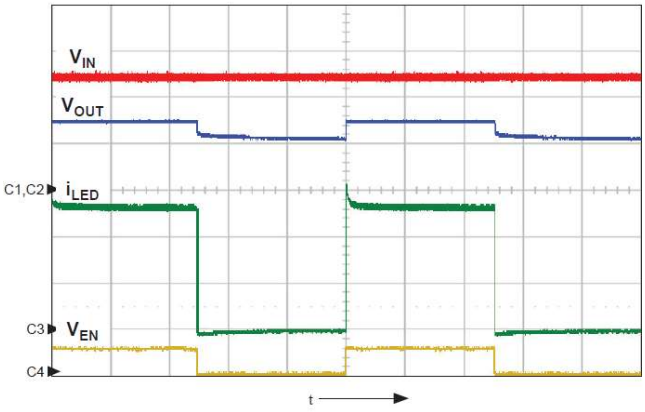

Fig. 30: Operation with a 0.68µF ceramic capacitor connected across the LED string. Operating conditions: at 200 Hz, V_{IN} = 24 V, V_{OUT} = 15 V, f_{SW} = 500 kHz, L = 10µH, duty cycle = 50%

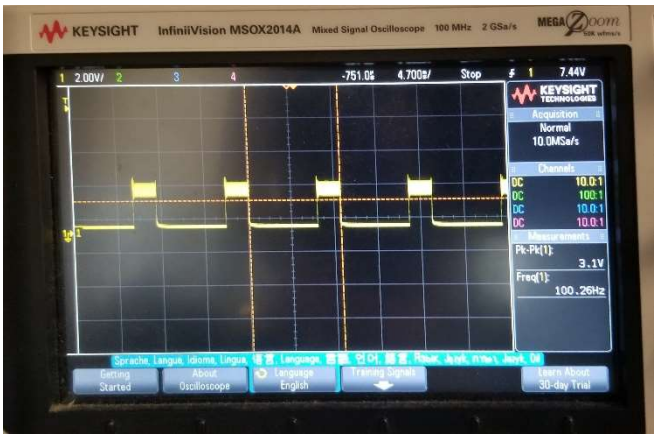

Fig. 31: Obtained waveform with .68µF output capacitor across the LED string. Operating conditions: at 100 Hz, V_{IN} = 12 V, V_{OUT} = 2.8 V, f_{SW} = 1.1 MHz, L = 12µH(not correct), duty cycle = 25%

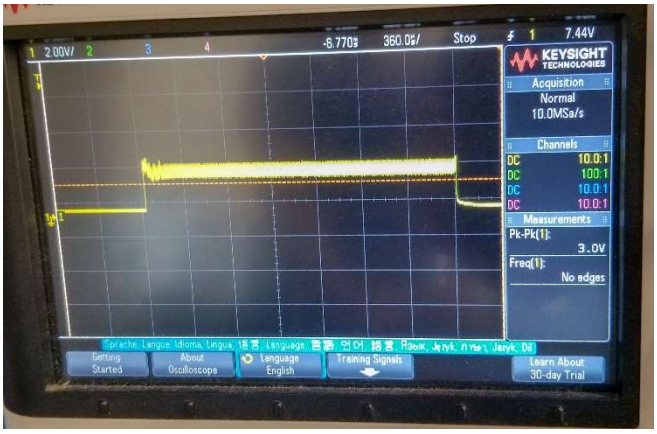

Fig. 32: A closer view of the obtained waveform when the IC is turned on.

Application Circuit

The application circuit in Figure 33 shows a design for driving a 15 V LED string at 1.3 A (set by R_{SENSE}). The switching frequency is 500 kHz, as set by R1. A 0.68µF ceramic capacitor is added across the LED string to reduce the ripple current through the LEDs.

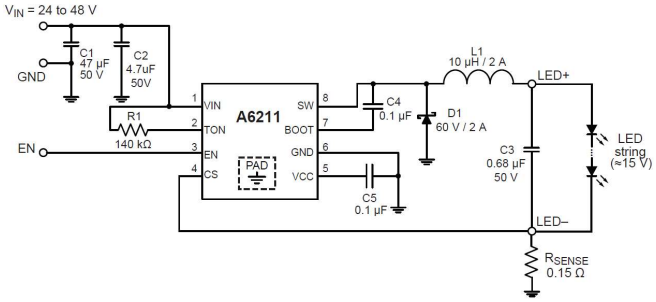

Fig. 33: Simplified Application Circuit Diagram.

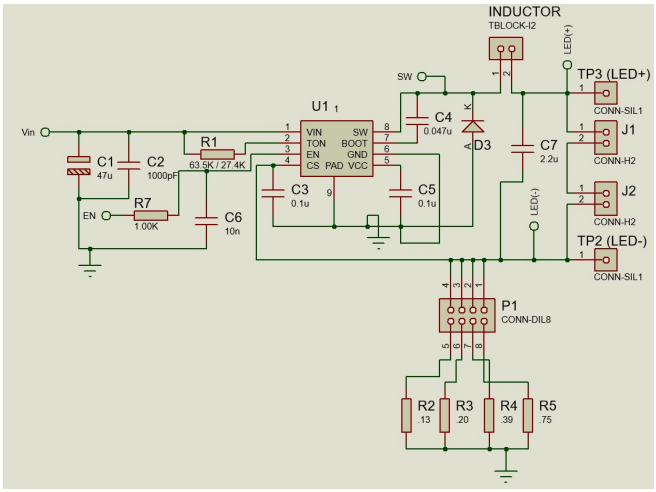

Fig. 34: Circuit implemented to drive the inductor for our device.

Component Placement and PCB Layout Guidelines

PCB layout is critical in designing any switching regulator. A good layout reduces emitted noise from the switching device and ensures better thermal performance and higher efficiency. The following guidelines help to obtain a high-quality PCB layout. Figure 35 shows the three critical current loops that should be minimized and connected by relatively wide traces. Figure 36 shows an example for components placement.

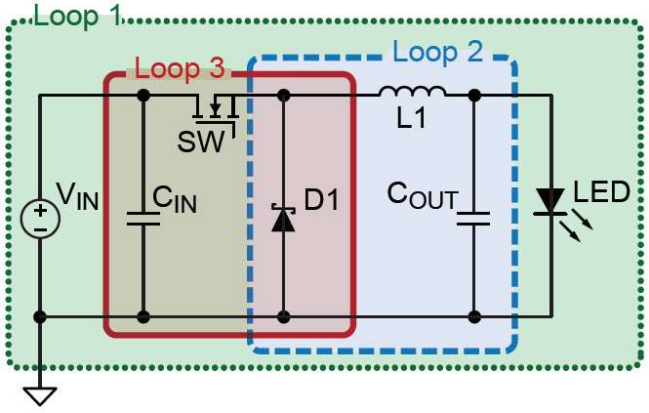

Fig. 35: Three Different Current Loops in a Buck Converter

- When the upper FET (integrated inside the A6211) is on, current flows from the input supply/capacitors, through the upper FET, into the load via the output inductor, and back to ground as shown in loop 1. This loop should have relatively wide traces. Ideally this connection is made on both the top (component) layer and via the ground plane. When the upper FET is off, free-wheeling current flows from ground

through the asynchronous diode D1, into the load via the output inductor, and back to ground as shown in loop.

- This loop should also be minimized and have relatively wide traces. Ideally this connection is made on both the top (component) layer and via the ground plane. This loop should also be minimized and have relatively wide traces. Ideally this connection is made on both the top (component) layer and via the ground plane.
- The highest *di/dt* occurs at the instant the upper FET turns on and the asynchronous diode D1 undergoes reverse recovery as shown in loop 3. The ceramic input capacitors C2 must deliver this high instantaneous current. C1 electrolytic capacitor) should not be too far off C2. Therefore, the loop from the ceramic input capacitor through the upper FET and asynchronous diode to ground should be minimized.
- The voltage on the SW node (pin 8) transitions from 0 V to V_{IN} very quickly and may cause noise issues. It is best to place the asynchronous diode and output inductor close to the A6211 to minimize the size of the SW polygon.
- Keep sensitive analog signals (CS, and R1 of switching frequency setting) away from the SW polygon.
- For accurate current sensing, the LED current sense resistor R_{SENSE} should be placed close to the IC.
- Place the boot strap capacitor C4 near the BOOT node (pin 7) and keep the routing to this capacitor short.
- When routing the input and output capacitors (C1, C2, and C3 if used), use multiple via to the ground plane and place the via as close as possible to the A6211 pads.
- To minimize PCB losses and improve system efficiency, the input (V_{IN}) and output (V_{OUT}) traces should be wide and duplicated on multiple layers, if possible.
- Connection to the LED array should be kept short. Excessively long wires can cause ringing or oscillation.

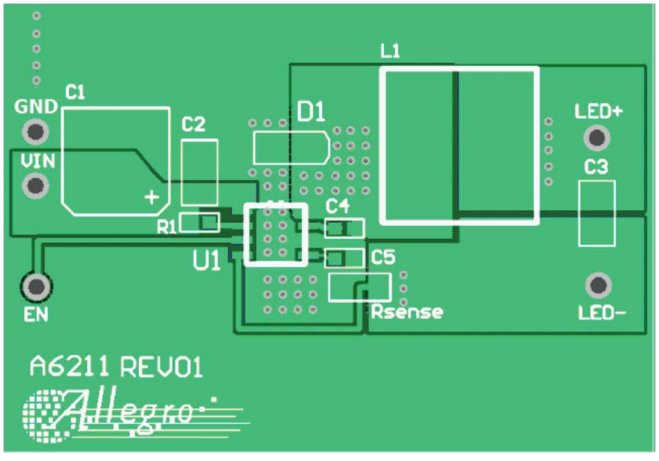

Fig. 36: Example Layout for the A6211 Evaluation Board

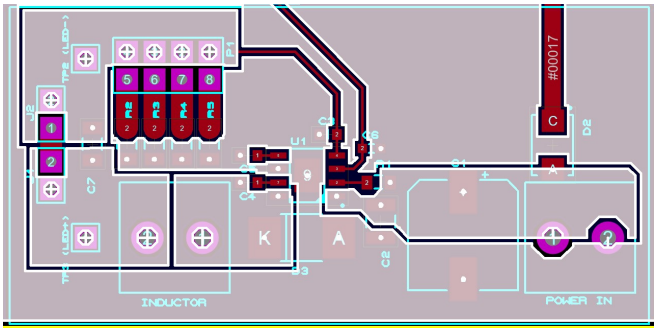

Fig. 37: Generated layout of the converter section in the PCB

Thermal Dissipation

The amount of heat that can pass from the silicon of the A6211 to the surrounding ambient environment depends on the thermal resistance of the structures connected to the A6211. The thermal resistance, RθJA, is a measure of the temperature rise created by power dissipation and is usually measured in degrees Celsius per watt (°C/W). The temperature rise, ΔT, is calculated from the power dissipated, PD, and the thermal resistance, RθJA, as:

$$\Delta T = PD \times R\theta JA$$

A thermal resistance from silicon to ambient, RθJA, of approximately 35°C/W can be achieved by mounting the A6211 on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the A6211. Additional improvements in the range of 20% may be achieved by optimizing the PCB design.

Optimizing Thermal Layout

The features of the printed circuit board, including heat conduction and adjacent thermal sources such as other components, have a very significant effect on the thermal performance of the device.

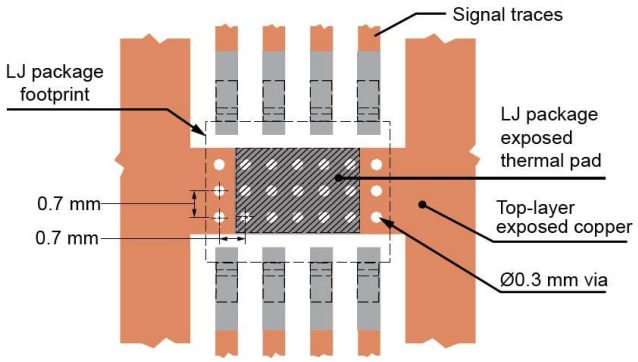

Fig. 37: Suggested PCB Layout for Thermal Optimization

To optimize thermal performance, the following considerations should be considered:

- The device exposed thermal pad should be connected to as much copper area as is available and Copper thickness should be as high as possible (for example, 2 oz. or greater for higher power applications).
- The greater the quantity of thermal via, the better the dissipation. If the expense of via is a concern, studies have shown that concentrating the via directly under

the device in a tight pattern, as shown in Figure 37, has the greatest effect.

- Additional exposed copper area on the opposite side of the board should be connected by means of the thermal via. The copper should cover as much area as possible.
- Other thermal sources should be placed as remote from the device as possible.
- Place as many via as possible to the ground plane around the anode of the asynchronous diode.

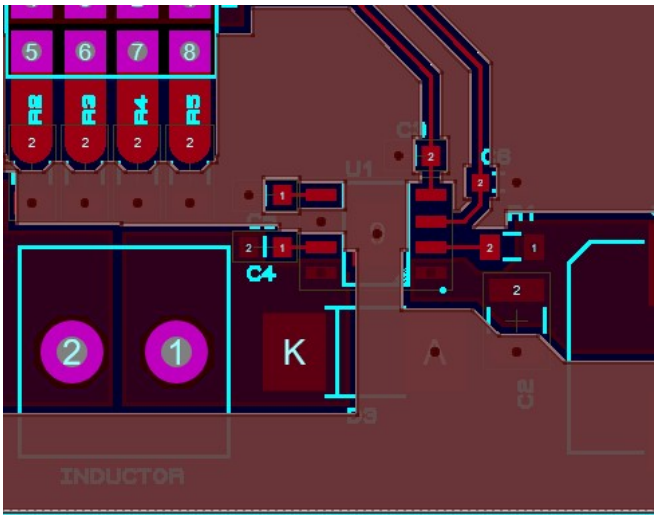

Fig. 38: Generated PCB Layout for Thermal Optimization

Final PCB Layout Design

The final designed PCBs for this test prototype are shown below.

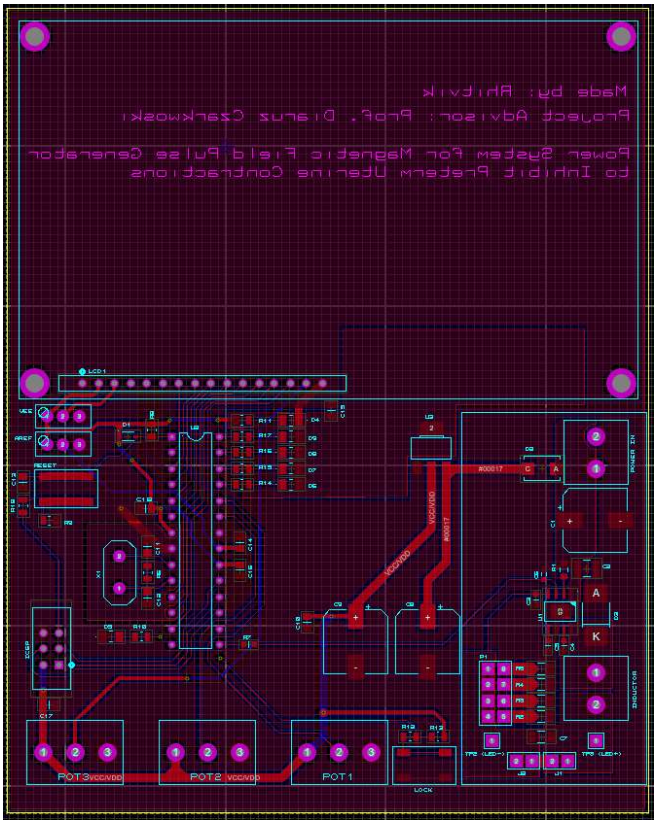

Fig. 39: PCB Layout Design (Top Copper)

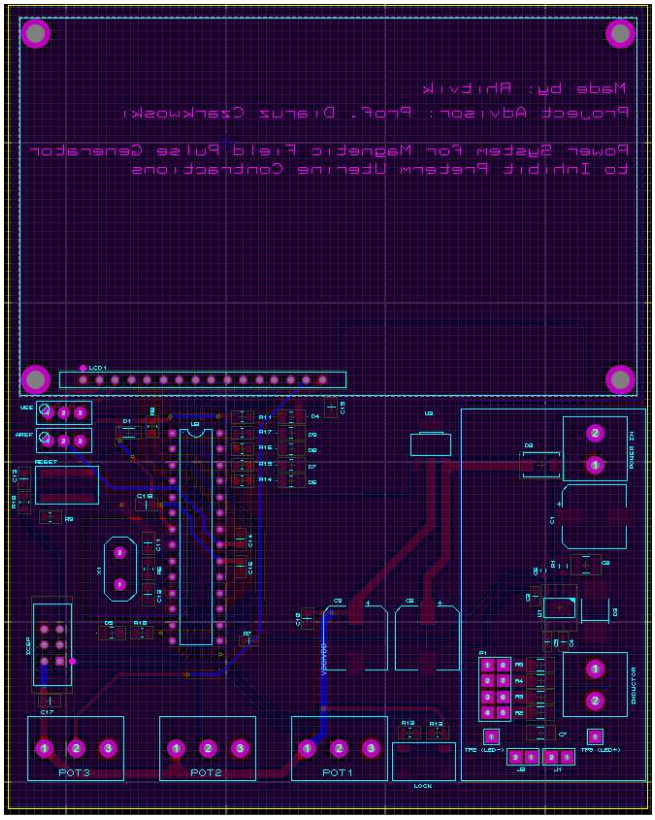

Fig. 40: PCB Layout Design (Bottom Copper)

And the manufactured PCB we got is shown in the image below.

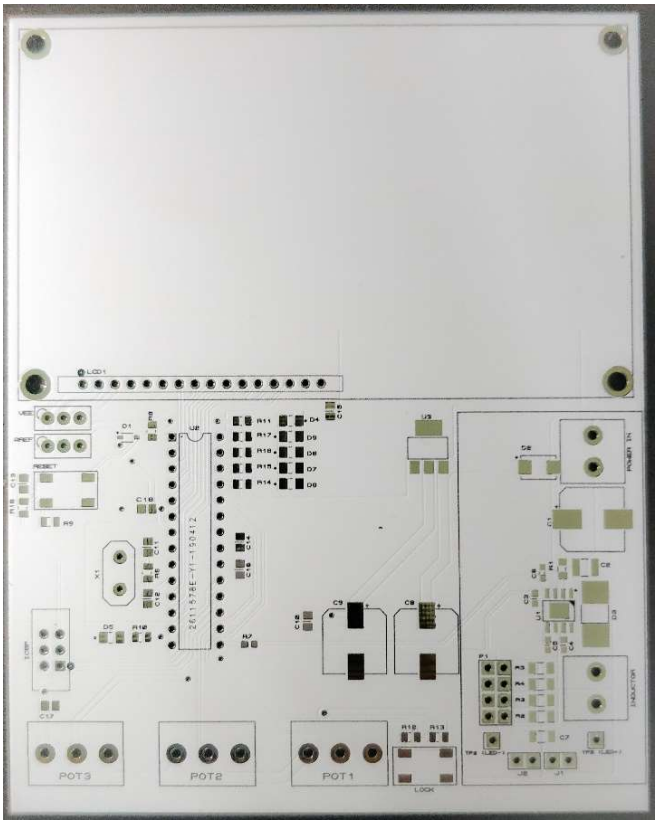

Fig. 41: Final PCB manufactured.

Final Design

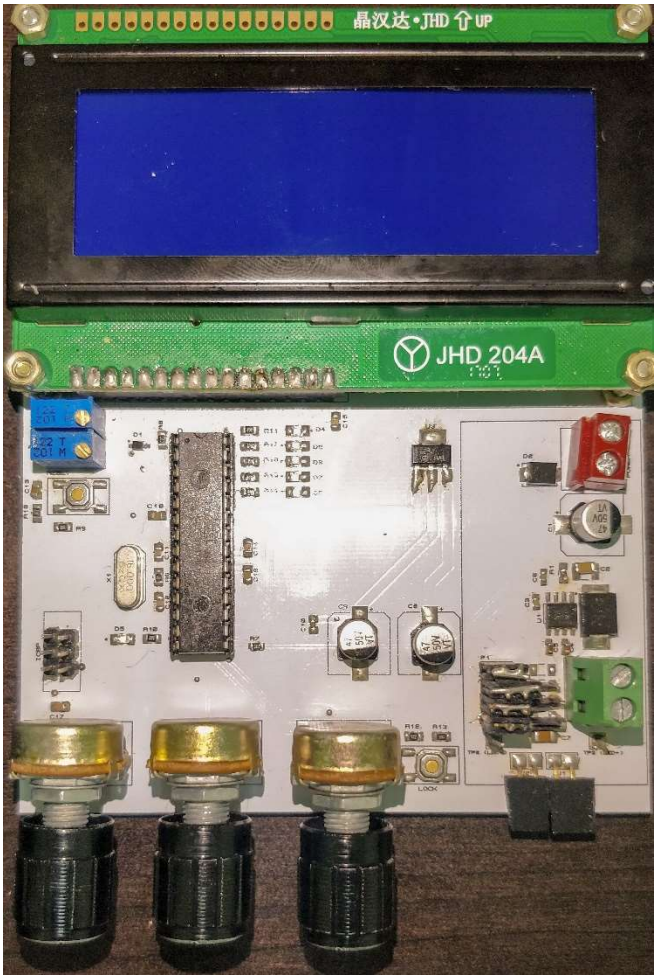

Fig. 42: Final device we obtain after mounting component.

The END

Inductor Design and conclusions to be appended after testing the inductor circuit.