Bachelor of Science in Computer Engineering (4 Years, 240 ECTS)

> A comprehensive, industry-aligned syllabus covering hardware, software, and systems engineering with strong lab and project components. Designed around 8 semesters, 30 ECTS per semester.

Program Overview

- **Award:** B.Sc. in Computer Engineering
- **Duration:** 8 Semesters (4 academic years)
- **Total Credits:** 240 ECTS (≈ 60 courses + labs, projects, and internships)
- **Delivery:** Lectures (L), Tutorials (T), Laboratories (P), Studio/Project (S)
- **Typical Workload:** 1 ECTS ≈ 25–30 hours (contact + independent study)
- **Pillars:** Digital & Analog Electronics, Computer Architecture, Embedded Systems, Operating Systems, Networks, Signals & Control, VLSI/FPGA, Cyber-Physical Systems, Software Engineering, AI/ML fundamentals, Cloud & DevOps, Security, Ethics.

Graduate Learning Outcomes

Graduates will be able to: 1. **Design** digital/analog circuits and embedded systems from requirements to prototype/production.
2. **Specify & analyze** computer architectures and real-time systems using quantitative metrics.
3. **Develop** reliable software in C/C++/Python/HDL with unit/integration testing and CI/CD.
4. **Deploy** networked, secure systems; reason about risk, privacy, and resilience.
5. **Apply** signals, control, and DSP to mechatronics/IoT/communications.
6. **Model & verify** systems using simulation, formal methods, and hardware debug tools.
7. **Collaborate** effectively, communicate design decisions, and manage engineering projects ethically.
8. **Learn** independently and adapt to emerging technologies.

Curriculum Map (By Semester)

Each course lists **ECTS**, **L-T-P-S** hours/week, **Prerequisites (Pre)**, **Co-requisites (Co)**, **Assessment** split, **Tools**, and **Brief Description** with detailed topics and labs.

Semester 1 (30 ECTS)

1. **CE101 Foundations of Programming** (6 ECTS, 2-1-2-0)
   Assessment: Labs 35%, PA 15%, Midterm 20%, Final 30%
   Tools: Python, Git, VS Code, PyTest
   Description: Problem solving, control flow, data structures (lists, dicts), functions, modularity, testing, basic complexity, style.

Detailed Topics: Variables & types; iteration/recursion; file I/O; exceptions; unit testing; algorithmic thinking; intro to OOP; simple data parsing; command-line interfaces.
Labs: Build a CLI data analyzer, test-driven development mini-kata, style and linting (flake8).
Outcomes: Write readable, tested Python programs; use Git; estimate time/space at a high level.

2. **CE102 Digital Logic Design I** (6 ECTS, 3-0-2-0)
   Assessment: Labs 30%, Midterm 25%, Design Project 15%, Final 30%
   Tools: Logisim/Quartus, Verilator, waveform viewers
   Description: Number systems, Boolean algebra, combinational circuits, minimization, MSI components, intro to sequential logic.
   Detailed Topics: K-maps; multiplexers/decoders/encoders; adders; hazards; latches/flip-flops; timing.
   Labs: Design & simulate ALU slice; FPGA demo of a 7-segment controller.
   Outcomes: Synthesize and test basic digital modules.

3. **CE103 Linear Algebra & Discrete Mathematics** (6 ECTS, 3-1-0-0)
   Assessment: Problem Sets 30%, Midterm 25%, Final 45%
   Description: Matrices, vectors, eigen-systems; logic, sets, relations, graphs; counting, probability.
   Detailed Topics: Gaussian elimination; determinants; spectral decomposition; graph traversal; modular arithmetic; combinatorics; discrete probability for algorithms.
   Outcomes: Apply linear/discrete tools to circuits, graphics, ML, cryptography.

4. **CE104 Electrical Circuits & Measurements** (6 ECTS, 2-1-2-0)
   Assessment: Labs/Reports 35%, Midterm 20%, Final 45%
   Tools: SPICE, oscilloscopes, DMMs, function generators
   Description: DC/AC analysis, Thevenin/Norton, first-order dynamics, power, measurement uncertainty.
   Labs: RC step response; bridge circuits; frequency response; safety/ESD.
   Outcomes: Analyze basic circuits; use instruments safely.

5. **CE105 Engineering Communication & Ethics I** (6 ECTS, 2-1-0-1)
   Assessment: Written Reports 25%, Presentations 25%, Ethics Case Study 20%, Final 30%
   Description: Technical writing, visual communication, teamwork, ethical frameworks (ACM/IEEE).
   Studio: Peer review, audience analysis, bias & accessibility.
   Outcomes: Produce clear reports; identify ethical risks in projects.

Semester 2 (30 ECTS)

1. **CE106 Object-Oriented Programming & Data Structures** (6 ECTS, 2-1-2-0)
   Pre: CE101
   Assessment: Labs 35%, Midterm 20%, Final 35%, Code Review 10%
   Tools: C++ (or Java), Git, Catch2/GoogleTest
   Topics: ADTs, complexity, lists, stacks, queues, trees, heaps, hash maps, graphs, templates, exceptions, RAII.
   Labs: Generic container library; pathfinding; profiler intro.

2. **CE107 Digital Logic Design II (HDL & FSMs)** (6 ECTS, 3-0-2-0)
   Pre: CE102
   Tools: Verilog/VHDL, ModelSim/Verilator, FPGA board
   Topics: Sequential design, FSMs, timing closure, RTL coding styles, testbenches, synthesis, CDC, basic AXI.
   Project: Traffic light controller + UART interface on FPGA.

3. **CE108 Calculus & Differential Equations for CE** (6 ECTS, 3-1-0-0)
   Topics: Multivariable calculus, series, ODEs, Laplace, numerical methods.
   Applications: RLC circuits, control, signals.

4. **CE109 Electronics I: Devices & Amplifiers** (6 ECTS, 2-1-2-0)
   Pre: CE104
   Topics: Diodes, BJTs, MOSFETs, biasing, small-signal models, op-amps, filters, data converters overview.
   Labs: Op-amp instrumentation amplifier; active filters.

5. **CE110 Engineering Communication & Ethics II** (6 ECTS, 2-1-0-1)
   Pre: CE105
   Focus: Requirements to specs; risk registers; privacy-by-design; inclusive design.

Semester 3 (30 ECTS)

1. **CE201 Computer Organization & Microarchitecture** (6 ECTS, 3-0-2-0)
   Pre: CE107
   Topics: ISA design (RISC-V), datapath & control, pipelines, hazards, caches, memory hierarchy, branch prediction, performance analysis.
   Labs: Build a 5-stage pipelined RISC-V CPU in HDL; benchmark it.

2. **CE202 Embedded Systems I (Bare-Metal C)** (6 ECTS, 2-0-3-0)
   Pre: CE107, CE106
   Tools: ARM Cortex-M, CMSIS, J-Link, logic analyzer
   Topics: GPIO, timers, interrupts, ADC/DAC, UART/SPI/I2C, DMA, low-power modes.
   Project: Sensor node with low-power logging & serial protocol.

3. **CE203 Probability & Random Processes** (6 ECTS, 3-1-0-0)
   Topics: Random variables, estimation, LLN/CLT, Poisson processes, Markov chains, queuing basics.
   Applications: Noise, reliability, networking.

4. **CE204 Signals & Systems** (6 ECTS, 3-1-0-0)
   Topics: LTI systems, convolution, Fourier/Laplace/ZS, sampling, stability, discrete-time systems.
   MATLAB/Python mini-labs.

5. **CE205 Software Engineering & DevOps** (6 ECTS, 2-1-2-0)
   Topics: Requirements, UML, design patterns, testing pyramid, CI/CD, containers, IaC basics, Git

strategies, code quality, agile/lean.
Project: Team builds a RESTful service with CI, containerization, and monitoring.

Semester 4 (30 ECTS)

1. **CE206 Operating Systems** (6 ECTS, 3-0-2-0)
   Pre: CE201, CE205
   Topics: Processes, threads, scheduling, synchronization, memory management, filesystems, virtualization basics.
   Labs: Implement a user-level thread library; memory allocator; toy FS.

2. **CE207 Computer Networks** (6 ECTS, 3-0-2-0)
   Topics: Link, IP, transport, routing, congestion, DNS, HTTP/2/3, Wi-Fi/BT/LoRa, SDN, network measurement.
   Labs: Packet sniffing; router configs; build a TCP over raw sockets.

3. **CE208 Digital Signal Processing** (6 ECTS, 3-0-2-0)
   Pre: CE204
   Topics: DFT/FFT, FIR/IIR design, spectral estimation, multirate, fixed-point DSP, audio processing.
   Labs: Real-time audio effects on ARM/DSP or FPGA.

4. **CE209 Electronics II: Mixed-Signal & Data Conversion** (6 ECTS, 2-1-2-0)
   Pre: CE109
   Topics: Sample-and-hold, ADC/DAC architectures, PLL basics, clocking & jitter, power integrity.
   Labs: SAR ADC modeling; PLL loop simulation.

5. **CE210 Human-Centered Systems & Tech Policy** (6 ECTS, 2-1-0-1)
   Topics: UX fundamentals, safety & usability in embedded/medical/automotive, standards overview (IEC/ISO/DO-178C), accessibility, sustainability, governance.

Semester 5 (30 ECTS)

1. **CE301 Advanced Computer Architecture** (6 ECTS, 3-0-2-0)
   Pre: CE201
   Topics: Superscalar, OoO, memory consistency, coherence, NUMA, GPUs, accelerators, performance modeling.
   Labs: Cache coherence simulator; GPU kernel optimization.

2. **CE302 Embedded Systems II (RTOS & IoT)** (6 ECTS, 2-0-3-0)
   Pre: CE202, CE206
   Topics: RTOS primitives, scheduling, device drivers, BLE/MQTT, OTA updates, secure boot, firmware update strategy.
   Project: Secure IoT device (sensor→gateway→cloud) with telemetry and OTA.

3. **CE303 Control Systems & Mechatronics** (6 ECTS, 2-1-2-0)
   Topics: Feedback, PID, state-space, observers, discretization, embedded control, motor drives.
   Labs: Inverted pendulum or quadrotor sim→hardware tuning.

4. **CE304 Databases & Data Engineering** (6 ECTS, 2-1-2-0)
   Topics: Relational modeling, SQL, transactions, indexing, NoSQL, streaming, data pipelines, time-series DBs for telemetry.
   Project: Time-series ingestion + dashboard.

5. **CE3E1 Technical Elective I** (6 ECTS) — pick from tracks below.

Semester 6 (30 ECTS)

1. **CE305 Cybersecurity for Systems & Devices** (6 ECTS, 3-0-2-0)
   Topics: Threat modeling, crypto basics, secure protocols, HW security (TPM/TEE), side-channels, secure coding, fuzzing, penetration testing, SBOMs.
   Labs: MitM lab; firmware hardening; static/dynamic analysis.

2. **CE306 Communication Systems** (6 ECTS, 3-0-2-0)
   Topics: Modulation, coding, link budgets, OFDM, MIMO concepts, SDR, 5G/6G overview.
   Labs: SDR experiments; BER vs SNR analysis.

3. **CE307 Parallel & Distributed Systems** (6 ECTS, 2-0-3-0)
   Topics: Threads, OpenMP, CUDA/OpenCL basics, RPC, consensus, fault tolerance, containers & orchestration, edge-cloud systems.
   Project: Distributed processing pipeline with observability.

4. **CE3E2 Technical Elective II** (6 ECTS)

5. **CE398 Summer Internship (0 ECTS recorded, required)**
   Deliverables: Learning plan + supervisor feedback + reflective report.

Semester 7 (30 ECTS)

1. **CE401 VLSI/FPGA Design** (6 ECTS, 2-0-3-0)
   Pre: CE107, CE201
   Topics: RTL→synthesis→place&route, constraints, timing analysis, CDC, AXI/AMBA IP, HLS overview, verification (UVM basics), DFT.
   Project: FPGA SoC with custom accelerator.

2. **CE402 Reliability, Safety & Verification** (6 ECTS, 3-0-2-0)
   Topics: FMEA, FTA, MTBF, redundancy, formal methods (model checking), property-based testing, HW/SW co-verification, standards (ISO 26262, IEC 61508).
   Labs: Model checking on protocol FSM; HW fault injection.

3. **CE403 Applied Machine Learning for Engineers** (6 ECTS, 2-0-3-0)
   Topics: Regression/classification, SVMs, trees, ensembles, shallow networks, feature engineering, MLOps light, embedded ML (TinyML).
   Project: Edge ML model on microcontroller/SoC with quantization.

4. **CE4E3 Technical Elective III** (6 ECTS)

5. **CE490 Capstone Design I (Proposal & Architecture)** (6 ECTS, 0-1-0-4)
   Activities: Requirements, architecture, risk mgmt, ethics, IRB/CE compliance if applicable, design review.

Semester 8 (30 ECTS)

1. **CE491 Capstone Design II (Implementation & Validation)** (12 ECTS, 0-0-2-6)
   Deliverables: Working prototype, test plan & evidence, design history file, poster + public demo, reproducible repo with CI.
   Examples: Autonomous rover; low-power medical wearable; FPGA accelerator; secure IoT gateway; SDR-based comm link.

2. **CE404 Cloud, Edge & DevOps for Devices** (6 ECTS, 2-0-3-0)
   Topics: Cloud services, messaging, time-series at scale, device fleet mgmt, CI/CD for firmware, observability, digital twins.
   Project: Fleet OTA simulation with monitoring and rollback.

3. **CE4E4 Technical Elective IV** (6 ECTS)

4. **CE405 Entrepreneurship & Productization** (6 ECTS, 2-1-2-0)
   Topics: Product discovery, MVPs, BoM & DFM/DFA, compliance & certification (EMC/CE/FCC), IP and licensing, tech transfer, business cases.
   Studio: Go-to-market plan for capstone or spin-off idea.

Technical Elective Tracks & Detailed Courses

Choose at least **4 electives** across tracks; at least **2** must be design-oriented.

Track A — Embedded & Real-Time Systems

- **CE451 Real-Time Systems & Scheduling** (6 ECTS, 2-0-3-0)
  Pre: CE206, CE302
  Topics: Rate-monotonic/EDF, response-time analysis, worst-case execution time, mixed-criticality, measurement & tuning.
  Lab: Integrate CAN/EtherCAT; latency measurement harness.

- **CE452 Advanced Device Drivers & BSP** (6 ECTS)
  MMIO, DMA, interrupts, bus frameworks, bootloaders, secure boot chains; board bring-up notebooks.
- **CE453 TinyML & DSP on Microcontrollers** (6 ECTS)
  Feature extraction vs. learned features, quantization, CMSIS-NN, on-device evaluation.

Track B — Networks, Security & Systems

- **CE461 Applied Cryptography & Key Management** (6 ECTS)
  Symmetric/asymmetric, ECC, protocols (TLS, SSH), PKI, HSM/TPM/TEE, secure storage, post-quantum overview.
- **CE462 Network Security & Zero Trust** (6 ECTS)
  IDS/IPS, segmentation, mTLS, authN/Z, OAuth/OIDC, SD-WAN, SASE, SIEM.
- **CE463 Wireless & Mobile Systems** (6 ECTS)
  PHY/MAC of Wi-Fi/BT/LE, LPWAN (LoRa, NB-IoT), 5G slicing, network planning, SDR labs.

Track C — VLSI, Digital Design & EDA

- **CE471 ASIC Design Flow & Verification** (6 ECTS)
  RTL, lint, CDC, synthesis, STA, power/area/timing closure, DFT, UPF, UVM, coverage.
- **CE472 High-Level Synthesis & Hardware Acceleration** (6 ECTS)
  C/C++→RTL, pragmas, performance trade-offs, HBM/PCIe, RISC-V vector ext overview.
- **CE473 Analog IC Design Intro** (6 ECTS)
  Current mirrors, op-amp topologies, references, layout intro, matching, noise.

Track D — AI, Data & Vision for CE

- **CE481 Computer Vision & Perception** (6 ECTS)
  Geometric vision, features, CNN basics, SLAM overview, embedded vision pipelines.
- **CE482 Edge AI Systems** (6 ECTS)
  Model compression, quantization/pruning, NN accelerators, runtimes (TFLM, ONNX Runtime, TVM).
- **CE483 Data-Centric Engineering** (6 ECTS)
  Data lifecycle for devices, labeling, telemetry quality, drift, MLOps for embedded.

Track E — Systems, Cloud & Software

- **CE491* Advanced DevOps & SRE** (6 ECTS)
  Observability, SLIs/SLOs, incident response, reliability patterns, chaos eng.
- **CE492 Distributed Messaging & Streaming** (6 ECTS)
  MQTT/Kafka/NATS, backpressure, exactly-once semantics, time windows, edge buffering.
- **CE493 High-Performance C/C++** (6 ECTS)
  Memory models, intrinsics/SIMD, profiling, cache-aware algorithms, sanitize/fuzz.

  *Note: CE491 here denotes an elective code, not the Capstone course code; institutions may renumber to avoid collision.

Laboratory Infrastructure & Toolchain

- **Hardware:** FPGA boards (e.g., mid-range Xilinx/Intel), ARM Cortex-M dev kits, logic analyzers, oscilloscopes, SDRs, robot kits, sensor suites, power supplies.
- **Software:** HDL simulators (Verilator/ModelSim), EDA flows, SPICE, MATLAB/Octave, Python (NumPy/SciPy), C/C++, GCC/Clang, CMake, Docker/Podman, Kubernetes (student cluster), GitLab/GitHub CI/CD.
- **Practices:** Version control, code reviews, unit/integration testing, static/dynamic analysis, pair programming, documentation standards.

Capstone Design Sequence (CE490/CE491 Detailed)

- **Phase 1 — Inception & Architecture (CE490):**
  Problem framing, stakeholder interviews, system context, requirements (functional/non-functional), hazard analysis, architectural views (C4/SysML), technology selection, prototype plan, ethics review, risk register, verification plan.
- **Gate Review A:** Architecture & risk sign-off, test plan approval.
- **Phase 2 — Implementation & Validation (CE491):**
  Iterative builds, hardware bring-up journals, driver development, integration tests, performance tuning, field tests, compliance pre-checks (EMC), DFM/DFA considerations, deployment guide.
- **Gate Review B:** Final demo, poster/paper, public code (where possible), peer assessment, post-mortem.

Professional Practice & Experiential Learning

- **Internship (after Sem 6):** 6–10 weeks in industry or research lab.
- **Co-op (optional):** 20–24 weeks extending Sem 7–8 timeline with academic credit substitution.
- **Industry Seminars:** Monthly talks on safety-critical systems, silicon start-ups, cloud-edge device mgmt, and security incidents.

Assessment & Quality Assurance

- **Rubrics:** Clarity on correctness, efficiency, robustness, documentation, and ethics.
- **Authentic assessment:** Open-ended labs, design critiques, code reviews, oral exams.
- **Academic integrity:** Tooling for plagiarism detection; viva voce for major submissions.
- **Program review:** Annual board with external advisors; graduate/industry feedback loops.

Suggested Texts & References (Non-Exhaustive)

- Digital Design & Computer Architecture (Harris & Harris)
- Computer Organization and Design RISC-V (Patterson & Hennessy)

- Operating Systems: Three Easy Pieces (Remzi & Andrea Arpaci-Dusseau)
- The Art of Electronics (Horowitz & Hill)
- CMOS VLSI Design (Weste & Harris)
- Modern Operating Systems (Tanenbaum)
- Computer Networking: A Top-Down Approach (Kurose & Ross)
- Pattern Classification (Duda, Hart, Stork) or Hands-On ML (Géron)
- Designing Data-Intensive Applications (Kleppmann)
- Clean Code (Martin) & Effective C++ (Meyers)

Admission & Progression Rules (Template)

- **Math readiness:** Calculus & linear algebra prerequisites or bridging module.
- **Progression:** Minimum 45 ECTS/year, core course pass required before advanced courses.
- **Capstone eligibility:** ≥ 150 ECTS completed, internship report approved.
- **Honors track (optional):** Research thesis (12 ECTS) replacing two electives with faculty supervision.

Mapping to Accreditation Criteria (Template)

- **Engineering Design:** ≥ 60 ECTS of design-focused courses/labs/projects including Capstone.
- **Math & Science:** ≥ 45 ECTS across calculus, linear algebra, probability, physics/electronics.
- **Professional Skills & Ethics:** ≥ 12 ECTS communication/ethics/policy + integrated ethics checkpoints.
- **Experiential Learning:** Mandatory internship + capstone with external review.

Customization Notes for Institutions

- Swap ECTS↔local credit units; adjust lab kits to budget.
- Offer language/local law modules as general electives.
- Integrate regional standards (e.g., automotive, medical devices) where relevant.
- Provide accessibility accommodations and inclusive pedagogy plans.

Appendix A — Weekly Syllabi Snapshots (Examples)

CE202 Embedded Systems I (Weeks 1–14):
- W1: Toolchain, GPIO; W2: Interrupts; W3: Timers; W4: UART; W5: SPI; W6: I2C; W7: ADC/DAC; W8: DMA; W9: Low power; W10: Board bring-up clinic; W11: Protocol design; W12: Reliability & debugging; W13: Project integration; W14: Demo day.
Assessments: Labs (7) 35%, Midterm 20%, Final 25%, Project 20%.

CE206 Operating Systems (Weeks 1–14):
- W1: OS overview; W2: Processes; W3: Threads; W4: Sync; W5: Scheduling; W6: Memory; W7: Virtual

memory; W8: Filesystems; W9: I/O; W10: Virtualization; W11: Security; W12: Measuring & tracing; W13: Project clinic; W14: Review.
Assessments: Labs (4) 30%, Midterm 20%, Final 35%, Project 15%.

CE401 VLSI/FPGA (Weeks 1–14):
- W1: Flow overview; W2: RTL style; W3: Constraints; W4: STA; W5: CDC; W6: Verification 1; W7: Verification 2; W8: IP integration; W9: AXI; W10: Timing closure; W11: Power; W12: DFT; W13: HLS; W14: Demos.

Appendix B — Example Capstone Briefs

- **Autonomous Delivery Rover:** Perception (embedded vision), path planning, motor control, V2X comms, safety case (ISO 26262-inspired), fleet ops demo.
- **Wearable Health Patch:** Low-power sensors, BLE, embedded ML arrhythmia detection, privacy & security model, IEC 62304-inspired software lifecycle.
- **FPGA CNN Accelerator:** RTL or HLS design, systolic array, quantized model, PCIe/AXI integration, throughput/latency/energy benchmarking.

Appendix C — Rubrics (Abbreviated)

- **Design Project (Generic):** Requirements clarity (15), Architecture & trade-offs (20), Implementation quality (25), Verification evidence (20), Documentation (10), Ethics & safety (10).
- **Coding Assignment:** Correctness (40), Tests (20), Code quality (20), Performance (10), Documentation (10).

This syllabus is a comprehensive template. Institutions should tailor prerequisites, hour allocations, and toolchains to local facilities and accreditation requirements while preserving learning outcomes and design depth.