North Carolina State University

Department of Electrical and Computer Engineering

ECE 506: Fall 2019
Project 2: Cache Coherence

by

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1) Performance with different cache sizes

Associativity: 8

Blocksize: 64B

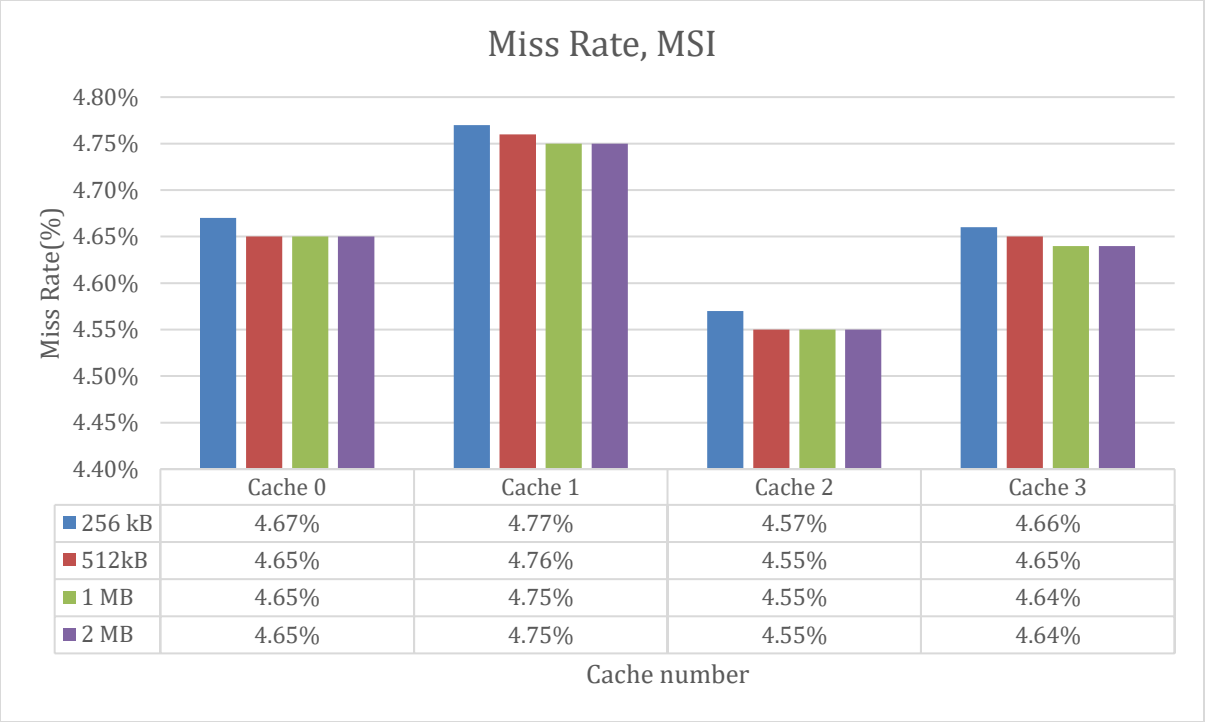
MSI:

Cache Size		Cache 0	Cache 1	Cache 2	Cache 3
256 kB	Reads	112661	110830	114938	113428
	Read Misses	5775	5805	5771	5813
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.67%	4.77%	4.57%	4.66%
	Writebacks	254	235	278	234
	C-C transfers	0	0	0	0
	Memory Transactions	6745	6740	6774	6761
	Interventions	68	47	81	63
	Invalidations	2014	2034	2008	2020
	Flushes	113	92	120	88
	BusRdX	716	700	725	714

Cache Size		Cache 0	Cache 1	Cache 2	Cache 3
512 kB	Reads	112661	110830	114938	113428
	Read Misses	5757	5792	5756	5796
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.65%	4.76%	4.55%	4.65%
	Writebacks	170	170	205	171
	C-C transfers	0	0	0	0
	Memory Transactions	6663	6662	6686	6681
	Interventions	71	47	82	63
	Invalidations	2014	2034	2008	2020
	Flushes	116	92	121	88
	BusRdX	716	700	725	714

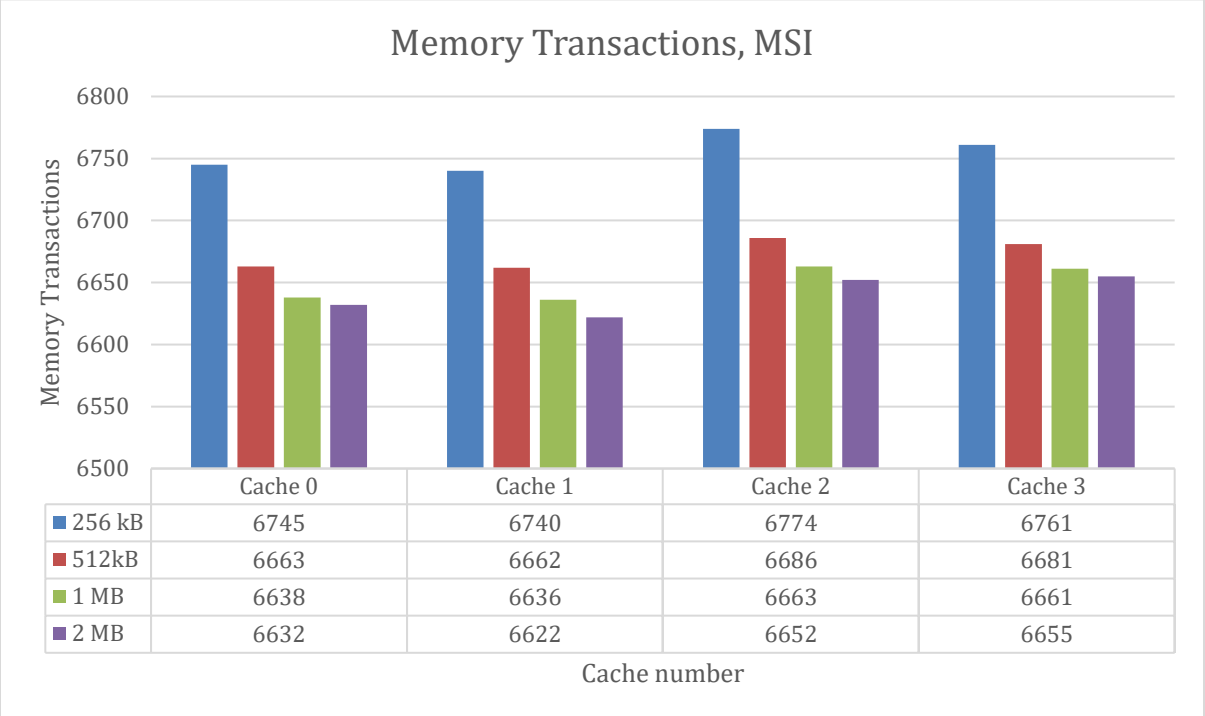
Cache Size		Cache 0	Cache 1	Cache 2	Cache 3
1 MB	Reads	112661	110830	114938	113428
	Read Misses	5752	5781	5752	5790
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.65%	4.75%	4.55%	4.64%
	Writebacks	170	155	186	157
	C-C transfers	0	0	0	0
	Memory Transactions	6638	6636	6663	6661
	Interventions	71	48	82	64
	Invalidations	2014	2034	2008	2020
	Flushes	116	93	121	89
	BusRdX	716	700	725	714

Cache Size		Cache 0	Cache 1	Cache 2	Cache 3
2 MB	Reads	112661	110830	114938	113428
	Read Misses	5750	5779	5751	5789
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.65%	4.75%	4.55%	4.64%
	Writebacks	166	143	176	152
	C-C transfers	0	0	0	0
	Memory Transactions	6632	6622	6652	6655
	Interventions	71	48	82	64
	Invalidations	2014	2034	2008	2020
	Flushes	116	93	121	89
	BusRdX	716	700	725	714



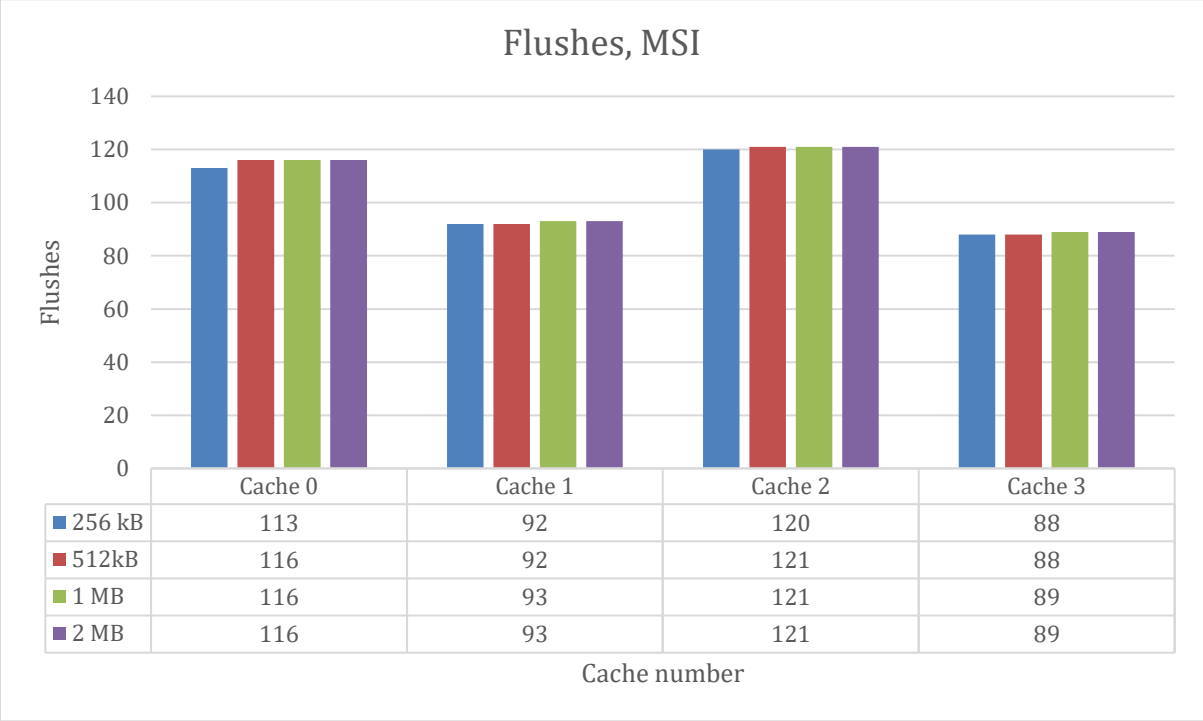
	Cache 0	Cache 1	Cache 2	Cache 3
256 kB	4.67%	4.77%	4.57%	4.66%
512kB	4.65%	4.76%	4.55%	4.65%
1 MB	4.65%	4.75%	4.55%	4.64%
2 MB	4.65%	4.75%	4.55%	4.64%

The miss rate stays almost constant on increasing the cache size. It does decrease though because of the decrease in capacity misses.



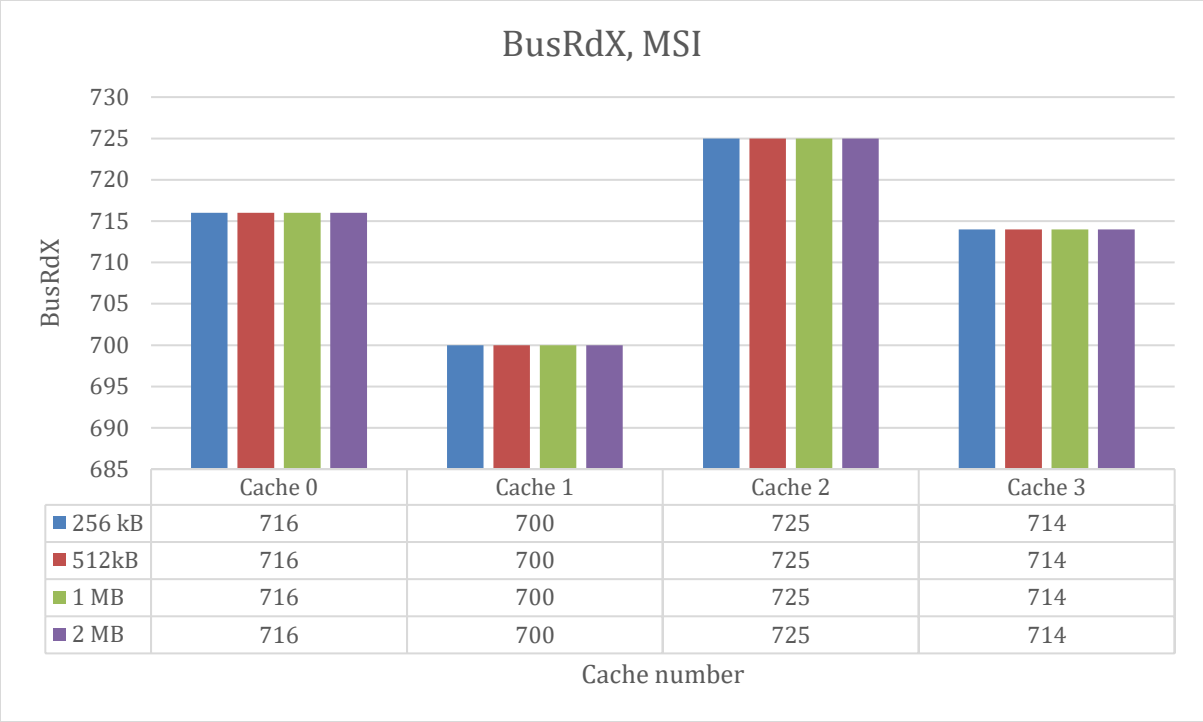
	Cache 0	Cache 1	Cache 2	Cache 3
256 kB	6745	6740	6774	6761
512kB	6663	6662	6686	6681
1 MB	6638	6636	6663	6661
2 MB	6632	6622	6652	6655

The memory transactions look like they reduce exponentially with the cache size. This is because of a larger cache can accommodate more blocks and give a better spatial and temporal locality.



	Cache 0	Cache 1	Cache 2	Cache 3
256 kB	113	92	120	88
512kB	116	92	121	88
1 MB	116	93	121	89
2 MB	116	93	121	89

Flushes depend on the current state of the cache(modified or shared) and on the bus messages. Therefore, cache size has hardly any effect on flushes which is seen from the graph above.



Again, BusRdX does not depend on the cache size. It depends on the instruction coming from the processor and the current state of the cache of the particular processor. Hence, the values read constant on varying the cache size.

MESI:

Cache Size		Cache 0	Cache 1	Cache 2	Cache 3
256 kB	Reads	112661	110830	114938	113428
	Read Misses	5775	5805	5771	5813
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.67%	4.77%	4.57%	4.66%
	Writebacks	254	235	278	234
	C-C transfers	4405	4441	4406	4411
	Memory Transactions	1663	1640	1685	1675
	Interventions	1468	1432	1469	1479
	Invalidations	2014	2034	2008	2020

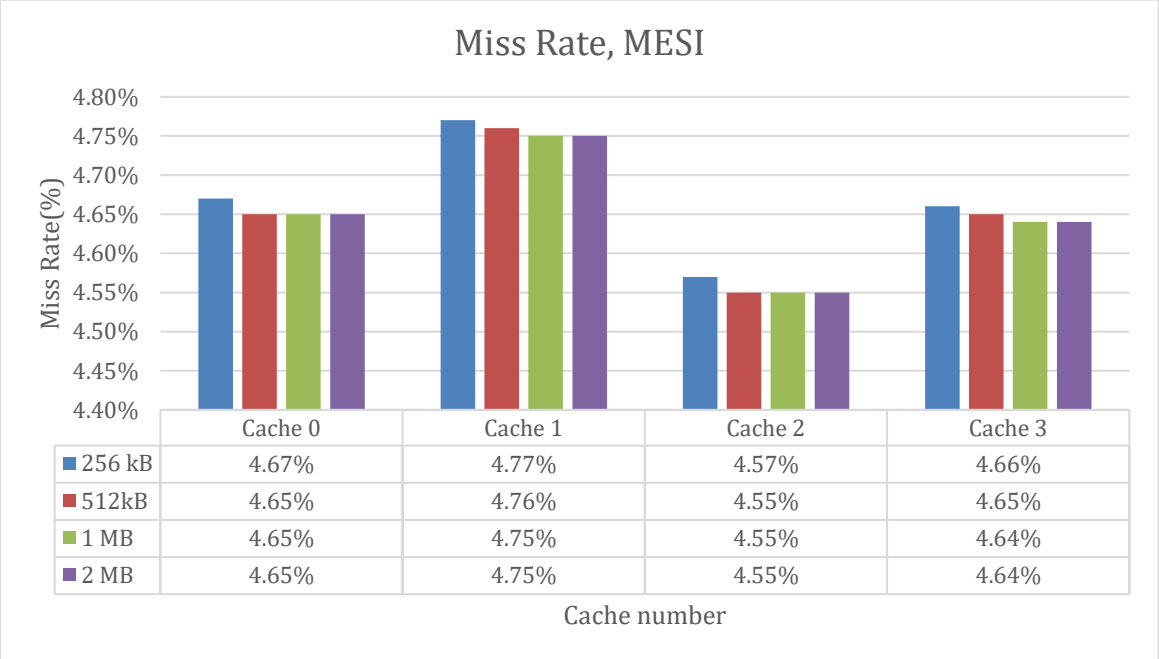
	Flushes	113	92	120	88
	BusRdX	39	41	42	39

Cache Size		Cache 0	Cache 1	Cache 2	Cache 3
512 kB	Reads	112661	110830	114938	113428
	Read Misses	5757	5792	5756	5796
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.65%	4.76%	4.55%	4.65%
	Writebacks	190	170	205	171
	C-C transfers	4392	4431	4396	4400
	Memory Transactions	1594	1572	1607	1606
	Interventions	1466	1429	1465	1474
	Invalidations	2014	2034	2008	2020
	Flushes	116	92	121	88
	BusRdX	39	41	42	39

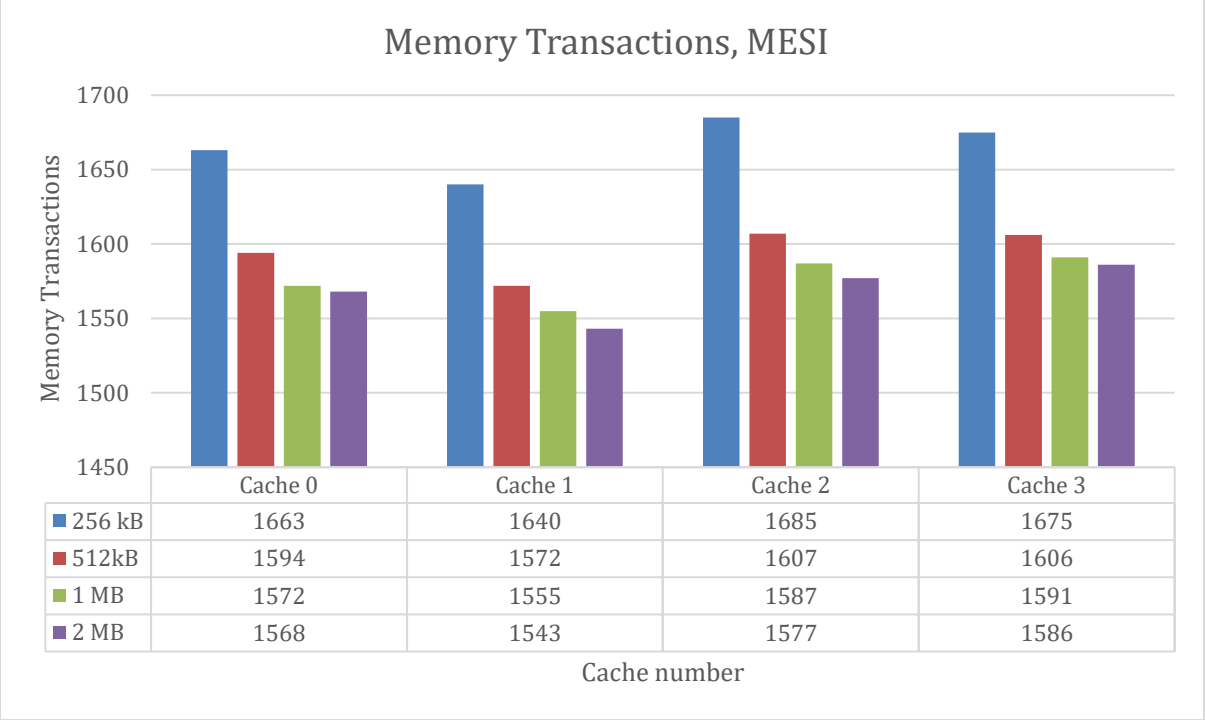
Cache Size		Cache 0	Cache 1	Cache 2	Cache 3
1 MB	Reads	112661	110830	114938	113428
	Read Misses	5752	5781	5752	5790
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.65%	4.75%	4.55%	4.64%
	Writebacks	170	155	186	157
	C-C transfers	4389	4422	4393	4395
	Memory Transactions	1572	1555	1587	1591
	Interventions	1464	1428	1464	1474
	Invalidations	2014	2034	2008	2020

	Flushes	116	93	121	89
	BusRdX	39	41	42	39

Cache Size		Cache 0	Cache 1	Cache 2	Cache 3
2 MB	Reads	112661	110830	114938	113428
	Read Misses	5750	5779	5751	5789
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.65%	4.75%	4.55%	4.64%
	Writebacks	166	143	176	152
	C-C transfers	4387	4420	4392	4394
	Memory Transactions	1568	1543	1577	1586
	Interventions	1464	1428	1464	1474
	Invalidations	2014	2034	2008	2020
	Flushes	116	93	121	89
	BusRdX	39	41	42	39

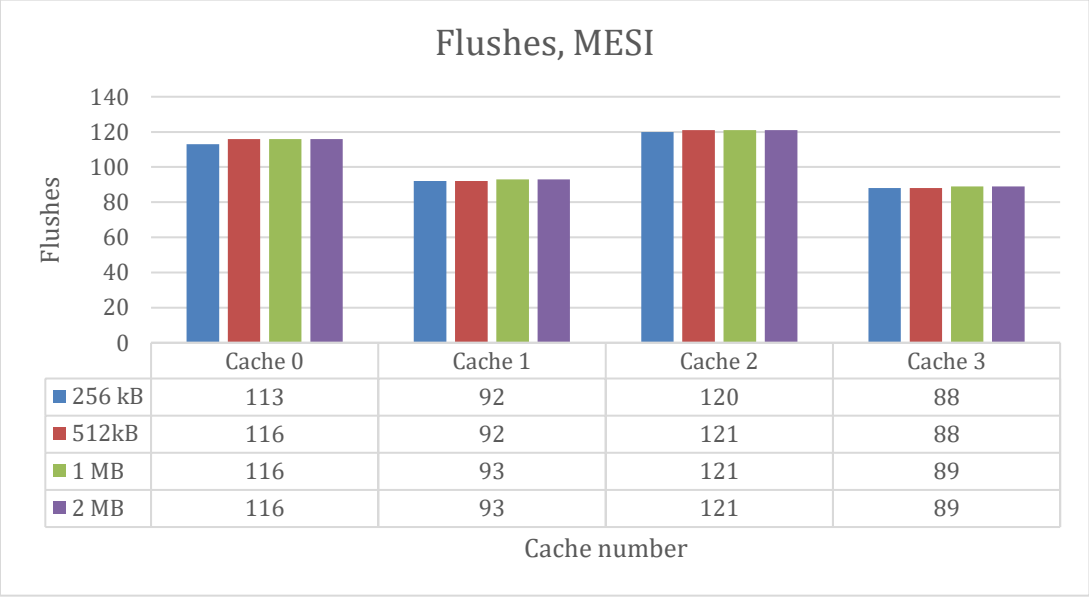


Similar to what was described in MSI miss rate graph, the miss rate drops by a small quantity on increasing cache size.



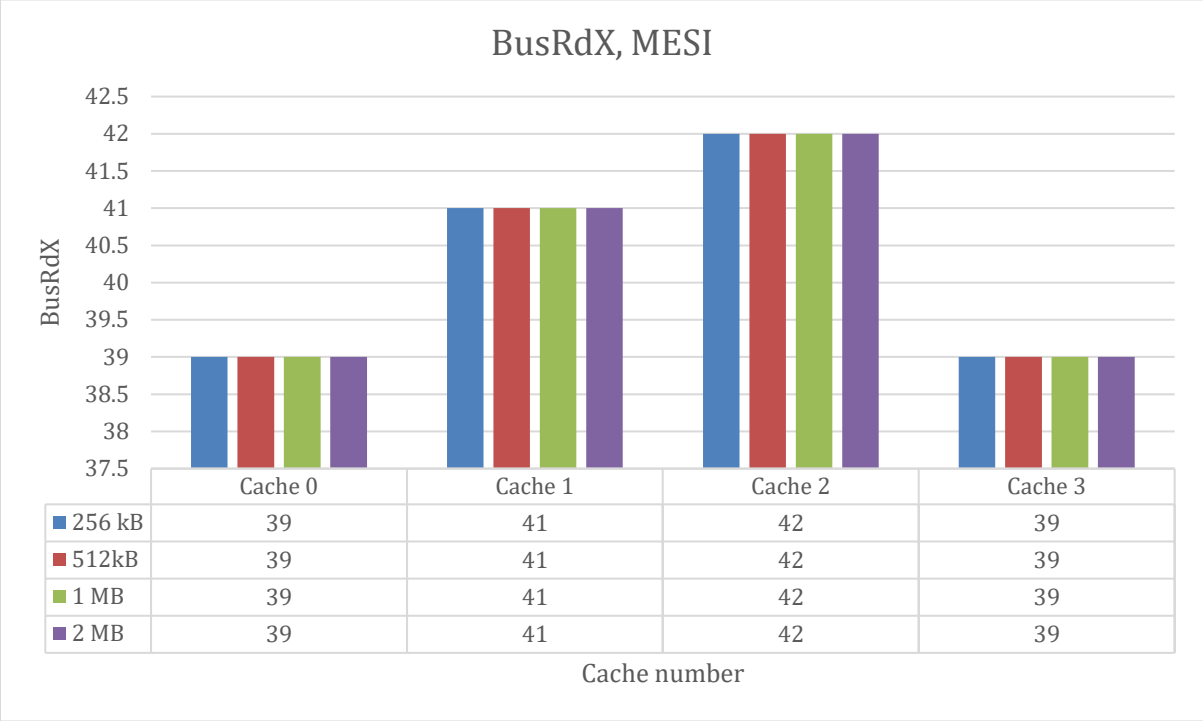
	Cache 0	Cache 1	Cache 2	Cache 3
256 kB	1663	1640	1685	1675
512kB	1594	1572	1607	1606
1 MB	1572	1555	1587	1591
2 MB	1568	1543	1577	1586

Memory transactions reduce a lot due to increase in cache size and does not depend on the protocol used. Therefore, it is the same in the case of MSI, MESI and Dragon.



	Cache 0	Cache 1	Cache 2	Cache 3
256 kB	113	92	120	88
512kB	116	92	121	88
1 MB	116	93	121	89
2 MB	116	93	121	89

A flush occurs if the cache is in modified state (M) and snoops a BusRd or a BusRdX. Therefore, it does not depend on cache size. Similarly, a BusRdX is sent on the bus if an invalid block gets a processor write request. Therefore, it will also not change with cache size



Dragon:

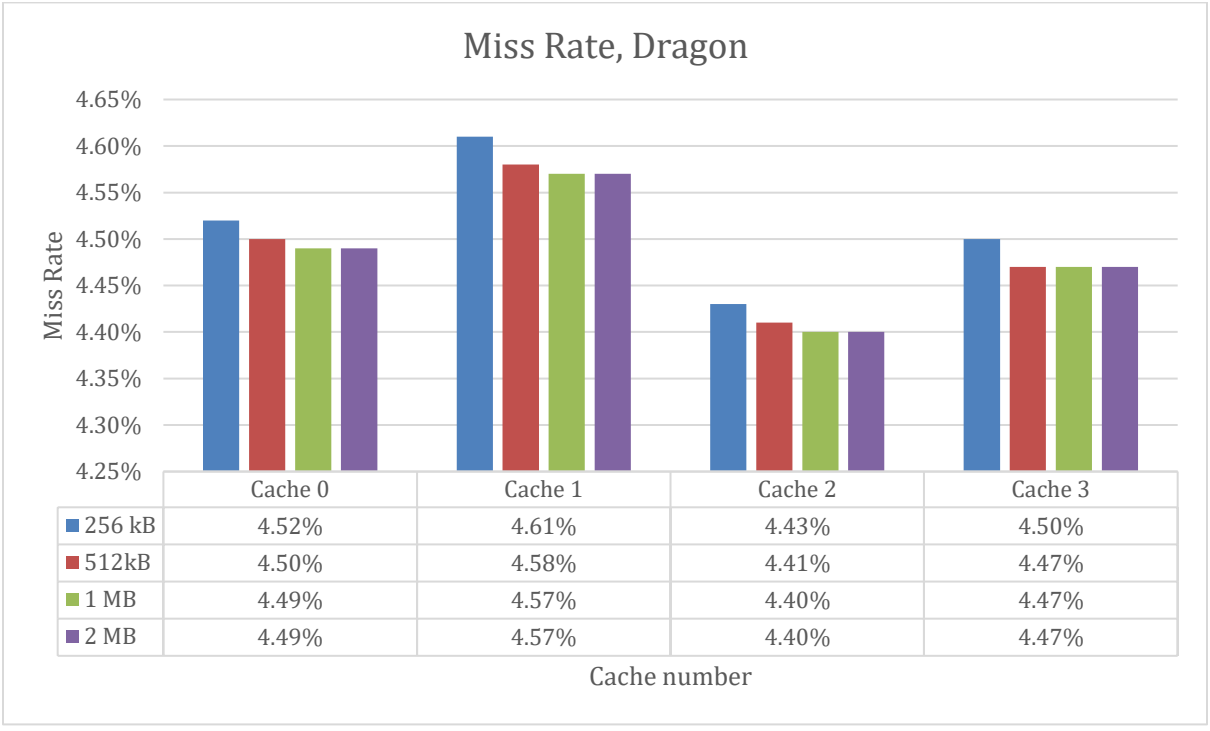
Cache Size		Cache 0	Cache 1	Cache 2	Cache 3
256 kB	Reads	112661	110830	114938	113428
	Read Misses	5635	5646	5644	5652
	Writes	11942	11710	12383	12108
	Write Misses	3	2	2	0
	Miss Rate	4.52%	4.61%	4.43%	4.50%
	Writebacks	226	243	232	234
	C-C transfers	0	0	0	0
	Memory Transactions	5864	5891	5878	5886
	Interventions	1405	1396	1397	1430
	Invalidations	0	0	0	0
	Flushes	3	9	6	9

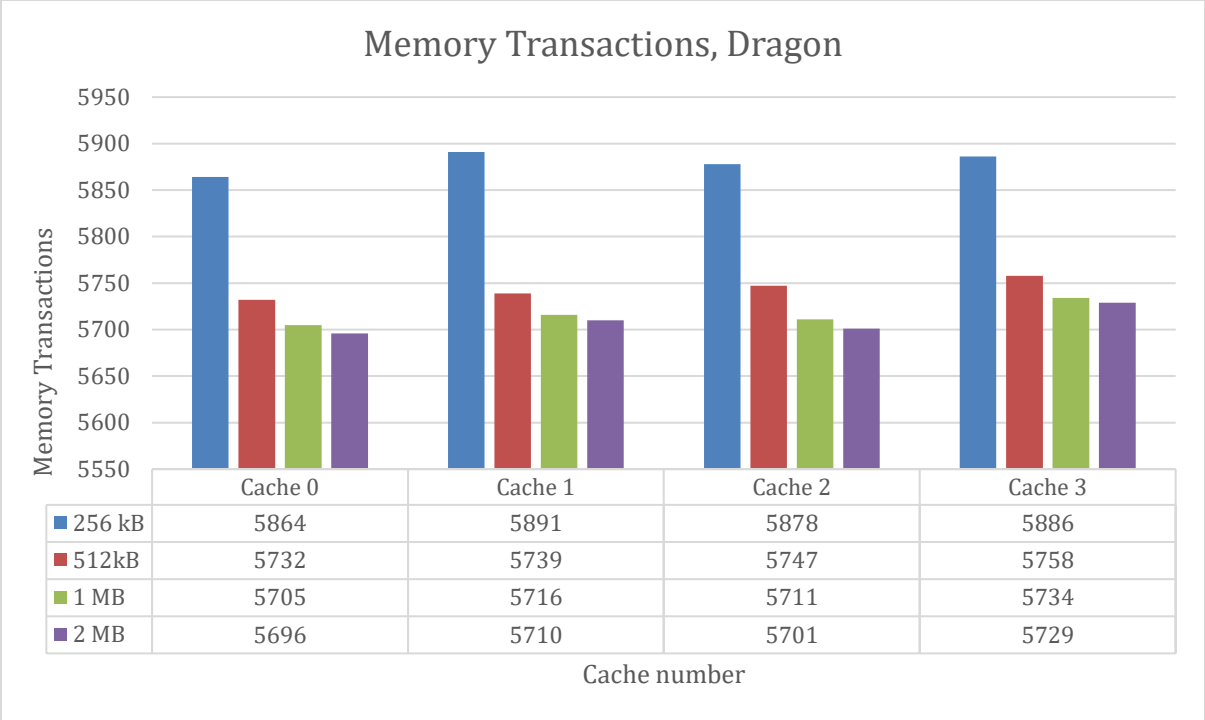
	BusRdX	0	0	0	0

Cache Size		Cache 0	Cache 1	Cache 2	Cache 3
512 kB	Reads	112661	110830	114938	113428
	Read Misses	5601	5610	5610	5617
	Writes	11942	11710	12383	12108
	Write Misses	3	2	2	0
	Miss Rate	4.50%	4.58%	4.41%	4.47%
	Writebacks	128	127	135	141
	C-C transfers	0	0	0	0
	Memory Transactions	5732	5739	5747	5758
	Interventions	1400	1388	1389	1418
	Invalidations	0	0	0	0
	Flushes	3	9	6	6
	BusRdX	0	0	0	0

Cache Size		Cache 0	Cache 1	Cache 2	Cache 3
1 MB	Reads	112661	110830	114938	113428
	Read Misses	5595	5604	5604	5611
	Writes	11942	11710	12383	12108
	Write Misses	3	2	2	0
	Miss Rate	4.49%	4.57%	4.40%	4.47%
	Writebacks	107	110	105	123
	C-C transfers	0	0	0	0
	Memory Transactions	5705	5716	5711	5734
	Interventions	1398	1387	1387	1417
	Invalidations	0	0	0	0
	Flushes	3	9	6	6
	BusRdX	0	0	0	0

Cache Size		Cache 0	Cache 1	Cache 2	Cache 3
2 MB	Reads	112661	110830	114938	113428
	Read Misses	5591	5603	5601	5608
	Writes	11942	11710	12383	12108
	Write Misses	3	2	2	0
	Miss Rate	4.49%	4.57%	4.40%	4.47%
	Writebacks	102	105	98	121
	C-C transfers	0	0	0	0
	Memory Transactions	5696	5710	5701	5729
	Interventions	1396	1387	1387	1416
	Invalidations	0	0	0	0
	Flushes	3	9	6	6
	BusRdX	0	0	0	0



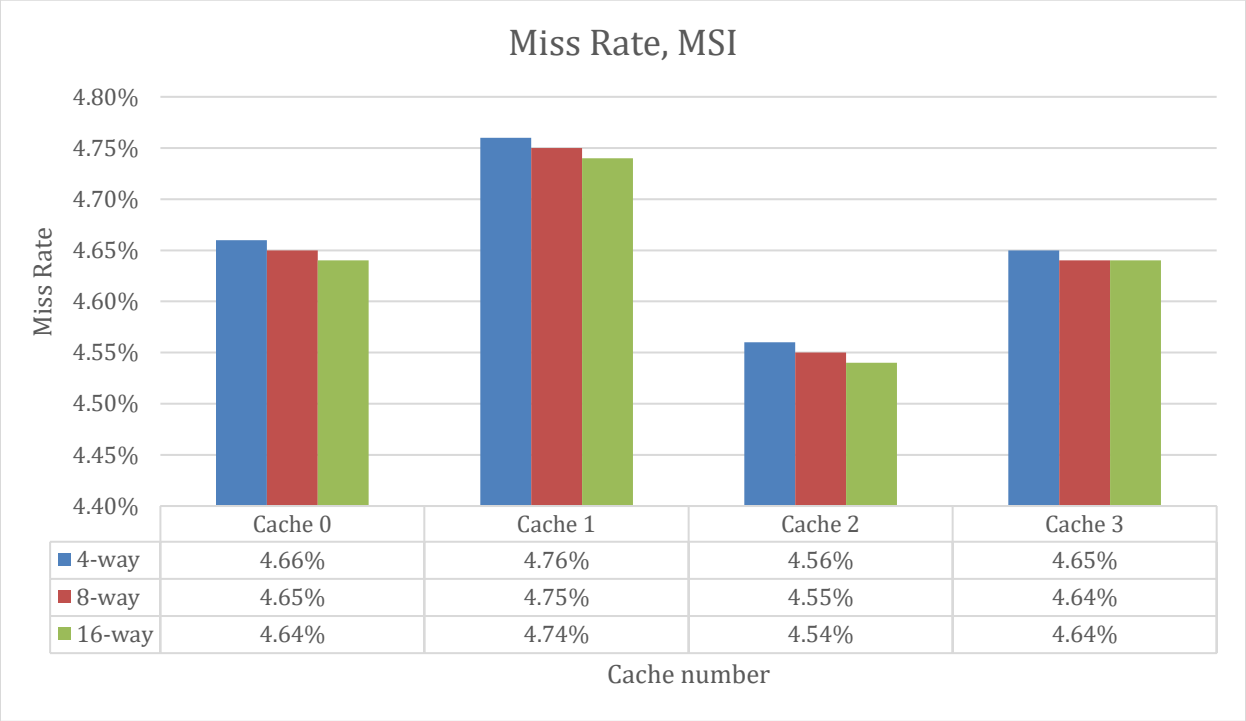


	Cache 0	Cache 1	Cache 2	Cache 3
256 kB	5864	5891	5878	5886
512kB	5732	5739	5747	5758
1 MB	5705	5716	5711	5734
2 MB	5696	5710	5701	5729

2) Performance with different associativity
Cache Size: 1MB
Blocksize: 64B
MSI:

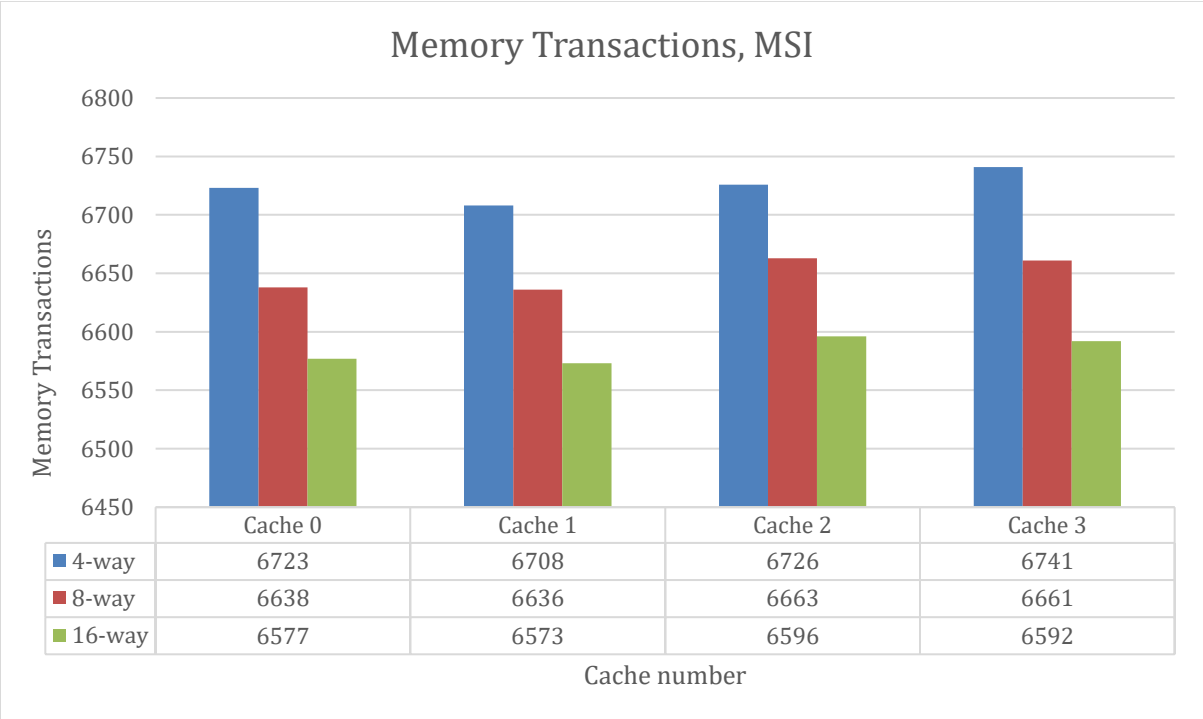
Associativity		Cache 0	Cache 1	Cache 2	Cache 3
4-way	Reads	112661	110830	114938	113428
	Read Misses	5768	5797	5762	5803
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.66%	4.76%	4.56%	4.65%
	Writebacks	239	211	2239	224
	C-C transfers	0	0	0	0
	Memory Transactions	6723	6708	6726	6741
	Interventions	69	47	81	63

	Invalidations	2014	2034	2008	2020
	Flushes	114	92	120	88
	BusRdX	716	700	725	714
Associativity		Cache 0	Cache 1	Cache 2	Cache 3
8-way	Reads	112661	110830	114938	113428
	Read Misses	5752	5781	5752	5790
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.65%	4.75%	4.55%	4.64%
	Writebacks	170	155	186	157
	C-C transfers	0	0	0	0
	Memory Transactions	6638	6636	6663	6661
	Interventions	71	48	82	64
	Invalidations	2014	2034	2008	2020
	Flushes	116	93	121	89
	BusRdX	716	700	725	714
Associativity		Cache 0	Cache 1	Cache 2	Cache 3
16-way	Reads	112661	110830	114938	113428
	Read Misses	5741	5772	5741	5780
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.64%	4.74%	4.54%	4.64%
	Writebacks	120	101	130	98
	C-C transfers	0	0	0	0
	Memory Transactions	6577	6573	6596	6592
	Interventions	71	48	83	64
	Invalidations	2014	2034	2008	2020
	Flushes	116	93	122	89
	BusRdX	716	700	725	714



	Cache 0	Cache 1	Cache 2	Cache 3
4-way	4.66%	4.76%	4.56%	4.65%
8-way	4.65%	4.75%	4.55%	4.64%
16-way	4.64%	4.74%	4.54%	4.64%

Miss rate decreases but not to a large extent as a single index can hold more than one block now.

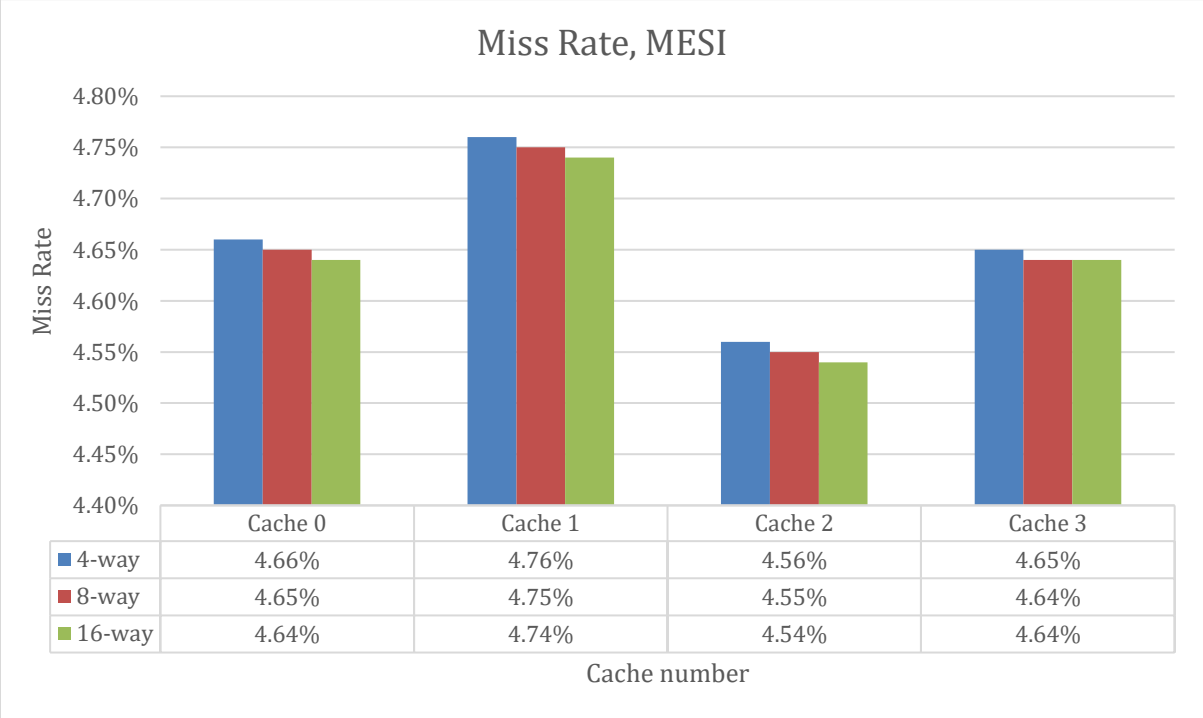


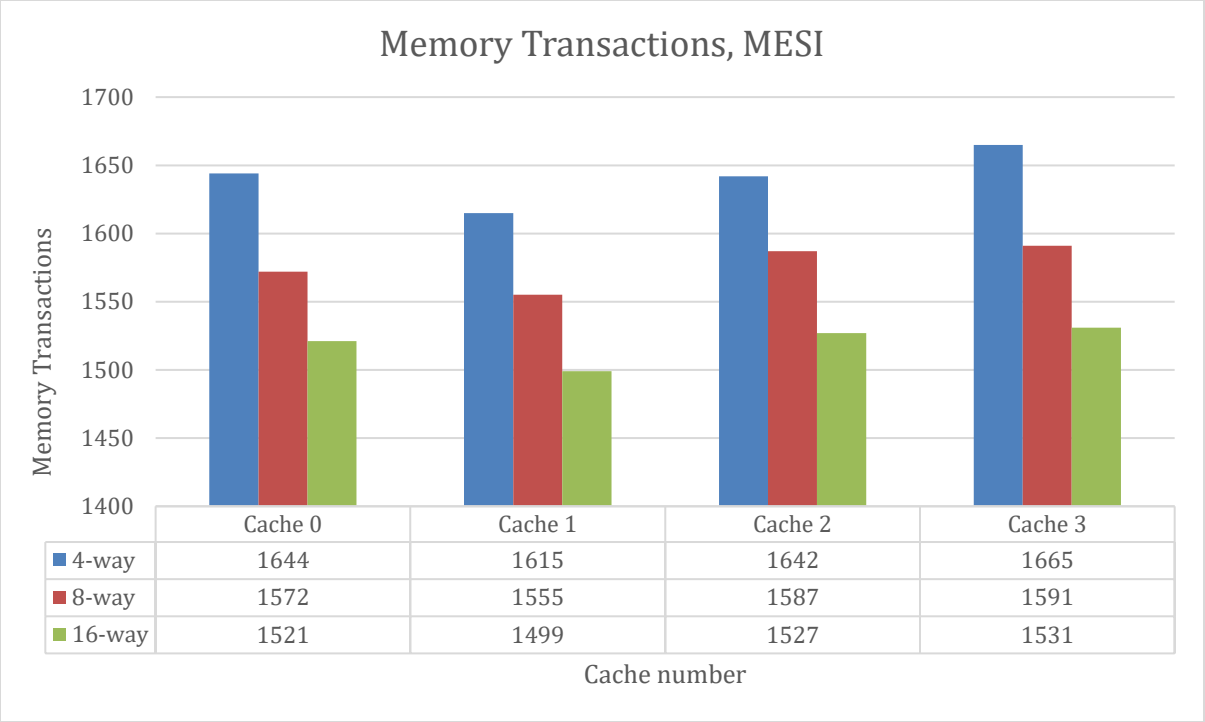
	Cache 0	Cache 1	Cache 2	Cache 3
4-way	6723	6708	6726	6741
8-way	6638	6636	6663	6661
16-way	6577	6573	6596	6592

MESI:

Associativity		Cache 0	Cache 1	Cache 2	Cache 3
4-way	Reads	112661	110830	114938	113428
	Read Misses	5768	5797	5762	5803
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.66%	476.00%	4.56%	4.65%
	Writebacks	239	211	239	224
	C-C transfers	4402	4434	4401	4401
	Memory Transactions	1644	1615	1642	1665
	Interventions	1465	1431	1465	1480
	Invalidations	2014	2034	2008	2020
	Flushes	114	92	120	88
	BusRdX	39	41	42	39
Associativity		Cache 0	Cache 1	Cache 2	Cache 3
8-way	Reads	112661	110830	114938	113428
	Read Misses	5752	5781	5752	5790
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.65%	4.75%	4.55%	4.64%
	Writebacks	170	155	186	157
	C-C transfers	4389	4422	4393	4395
	Memory Transactions	1572	1555	1587	1591
	Interventions	1464	1428	1464	1474
	Invalidations	2014	2034	2008	2020
	Flushes	116	93	121	89
	BusRdX	39	41	42	39

Associativity		Cache 0	Cache 1	Cache 2	Cache 3
16-way	Reads	112661	110830	114938	113428
	Read Misses	5741	5772	5741	5780
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.64%	4.74%	4.54%	4.64%
	Writebacks	120	101	130	98
	C-C transfers	4379	4415	4386	4386
	Memory Transactions	1521	1499	1527	1531
	Interventions	1463	1426	1461	1473
	Invalidations	2014	2034	2008	2020
	Flushes	116	93	122	89
	BusRdX	39	41	42	39

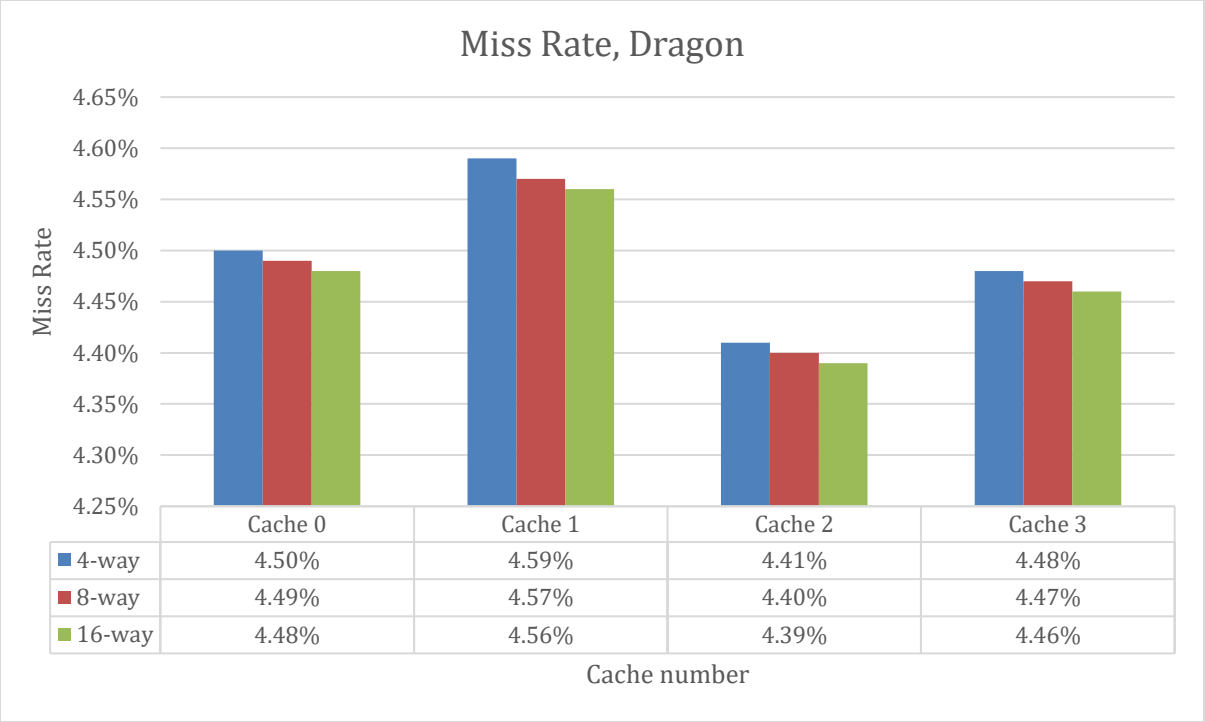




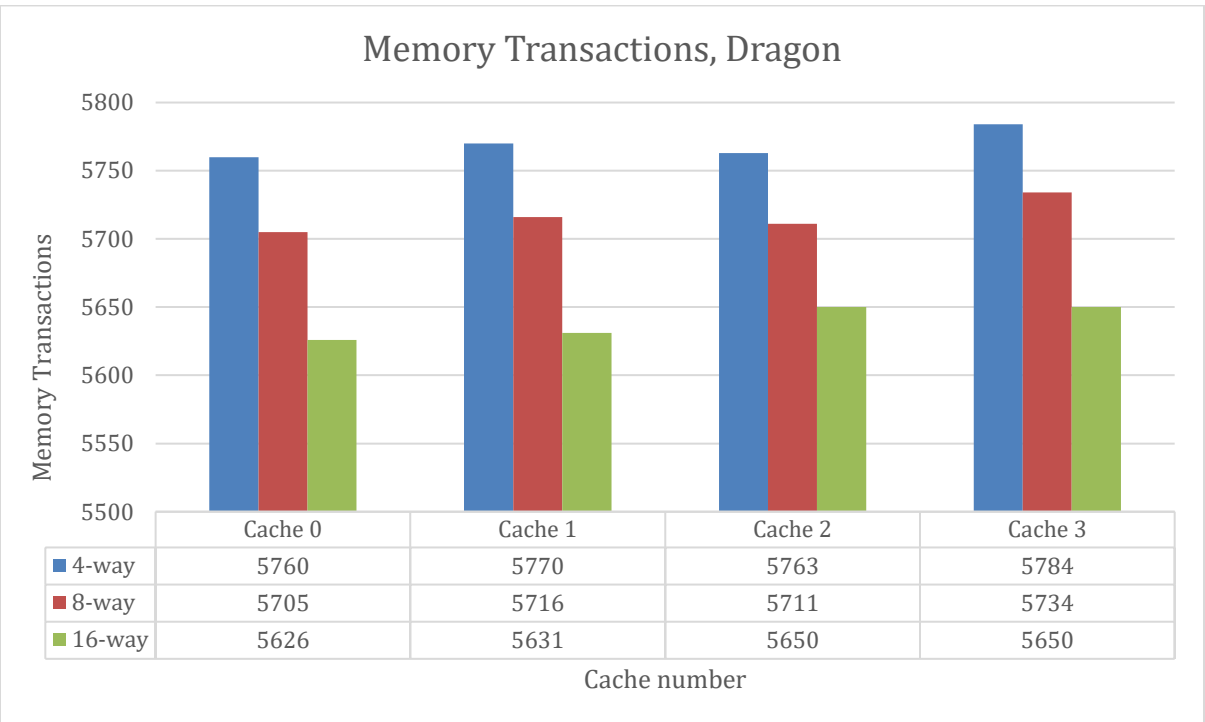
Dragon:

Associativity		Cache 0	Cache 1	Cache 2	Cache 3
4-way	Reads	112661	110830	114938	113428
	Read Misses	5609	5619	5619	5626
	Writes	11942	11710	12383	12108
	Write Misses	3	2	2	0
	Miss Rate	4.50%	4.59%	4.41%	4.48%
	Writebacks	148	149	142	158
	C-C transfers	0	0	0	0
	Memory Transactions	5760	5770	5763	5784
	Interventions	1400	1392	1388	1424
	Invalidations	0	0	0	0
	Flushes	3	9	6	6

	BusRdX	0	0	0	0
Associativity		Cache 0	Cache 1	Cache 2	Cache 3
8-way	Reads	112661	110830	114938	113428
	Read Misses	5595	5604	5604	5611
	Writes	11942	11710	12383	12108
	Write Misses	3	2	2	0
	Miss Rate	4.49%	4.57%	4.40%	4.47%
	Writebacks	107	110	105	123
	C-C transfers	0	0	0	0
	Memory Transactions	5705	5716	5711	5734
	Interventions	1398	1387	1387	1417
	Invalidations	0	0	0	0
	Flushes	3	9	6	6
	BusRdX	0	0	0	0
Associativity		Cache 0	Cache 1	Cache 2	Cache 3
16-way	Reads	112661	110830	114938	113428
	Read Misses	5576	5586	5586	5593
	Writes	11942	11710	12383	12108
	Write Misses	3	2	2	0
	Miss Rate	4.48%	4.56%	4.39%	4.46%
	Writebacks	47	43	62	57
	C-C transfers	0	0	0	0
	Memory Transactions	5626	5631	5650	5650
	Interventions	1395	1382	1383	1411
	Invalidations	0	0	0	0
	Flushes	3	9	6	6
	BusRdX	0	0	0	0



	Cache 0	Cache 1	Cache 2	Cache 3
4-way	4.50%	4.59%	4.41%	4.48%
8-way	4.49%	4.57%	4.40%	4.47%
16-way	4.48%	4.56%	4.39%	4.46%



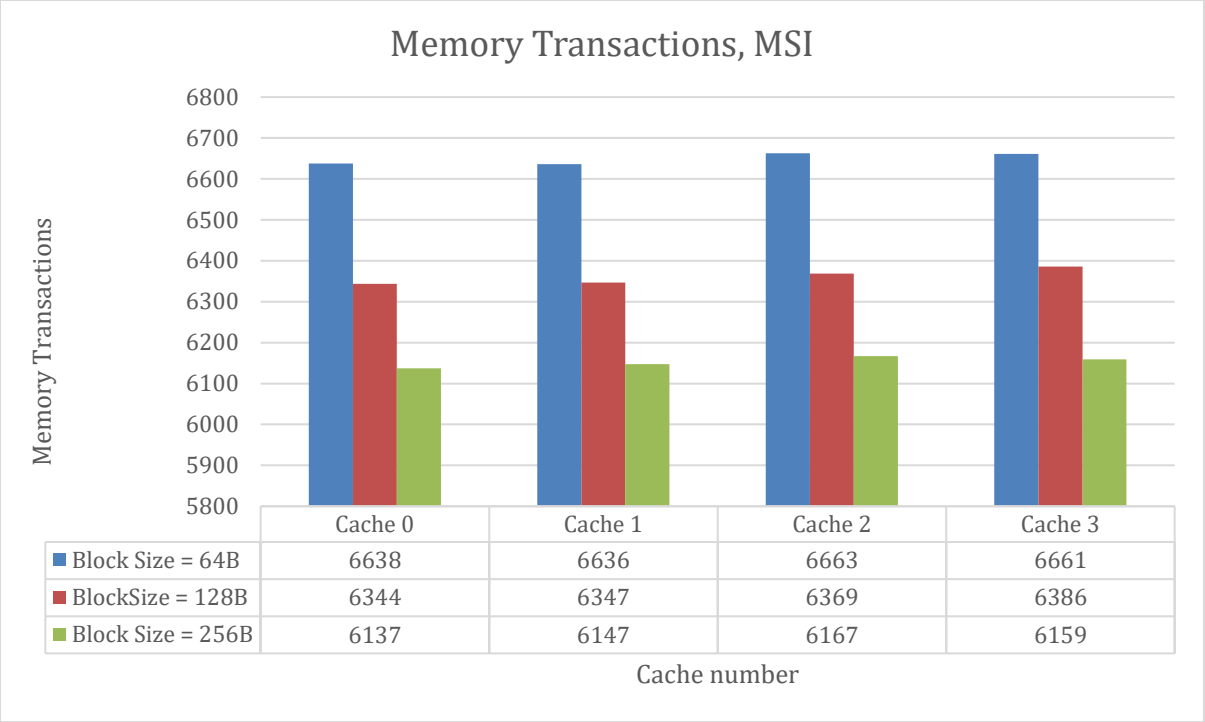
	Cache 0	Cache 1	Cache 2	Cache 3
4-way	5760	5770	5763	5784
8-way	5705	5716	5711	5734
16-way	5626	5631	5650	5650

3) Performance with different block sizes
   Cache Size: 1MB
   Cache Associativity: 8

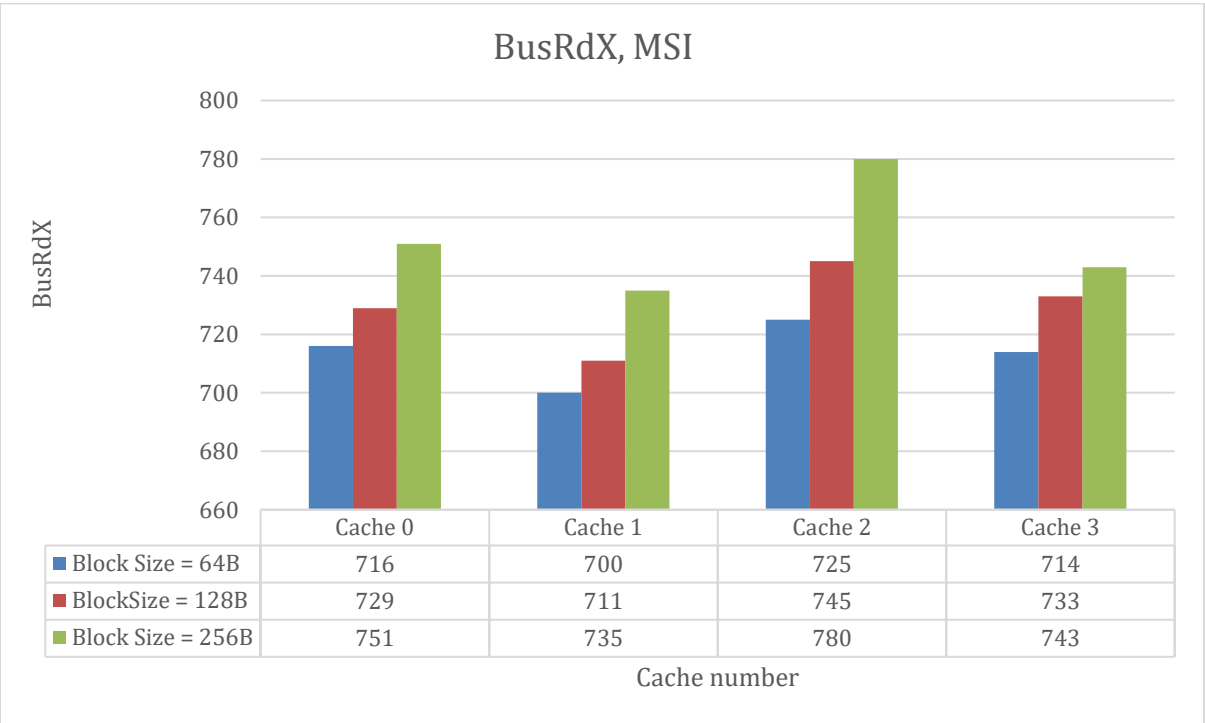
   MSI:

Block Size		Cache 0	Cache 1	Cache 2	Cache 3
64B	Reads	112661	110830	114938	113428
	Read Misses	5752	5781	5752	5790
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.65%	4.75%	4.55%	4.64%
	Writebacks	170	155	186	157
	C-C transfers	0	0	0	0
	Memory Transactions	6638	6636	6663	6661
	Interventions	71	48	82	64
	Invalidations	2014	2034	2008	2020
	Flushes	116	93	121	89
	BusRdX	716	700	725	714
Block Size		Cache 0	Cache 1	Cache 2	Cache 3
128B	Reads	112661	110830	114938	113428
	Read Misses	5340	5386	5341	5384
	Writes	11942	11710	12383	12108
	Write Misses	39	40	42	39
	Miss Rate	4.32%	4.43%	4.23%	4.32%
	Writebacks	275	250	283	269
	C-C transfers	0	0	0	0
	Memory Transactions	6344	6347	6369	6386
	Interventions	119	84	127	110
	Invalidations	2066	2089	2053	2068
	Flushes	164	129	166	135
	BusRdX	729	711	745	733

Block Size		Cache 0	Cache 1	Cache 2	Cache 3
256B	Reads	112661	110830	114938	113428
	Read Misses	5023	5070	5004	5084
	Writes	11942	11710	12383	12108
	Write Misses	39	40	42	39
	Miss Rate	4.06%	4.17%	3.96%	4.08%
	Writebacks	363	342	383	332
	C-C transfers	0	0	0	0
	Memory Transactions	6137	6147	6167	6159
	Interventions	166	133	192	145
	Invalidations	2132	2157	2107	2148
	Flushes	211	178	231	170
	BusRdX	751	735	780	743



	Cache 0	Cache 1	Cache 2	Cache 3
Block Size = 64B	6638	6636	6663	6661
BlockSize = 128B	6344	6347	6369	6386
Block Size = 256B	6137	6147	6167	6159

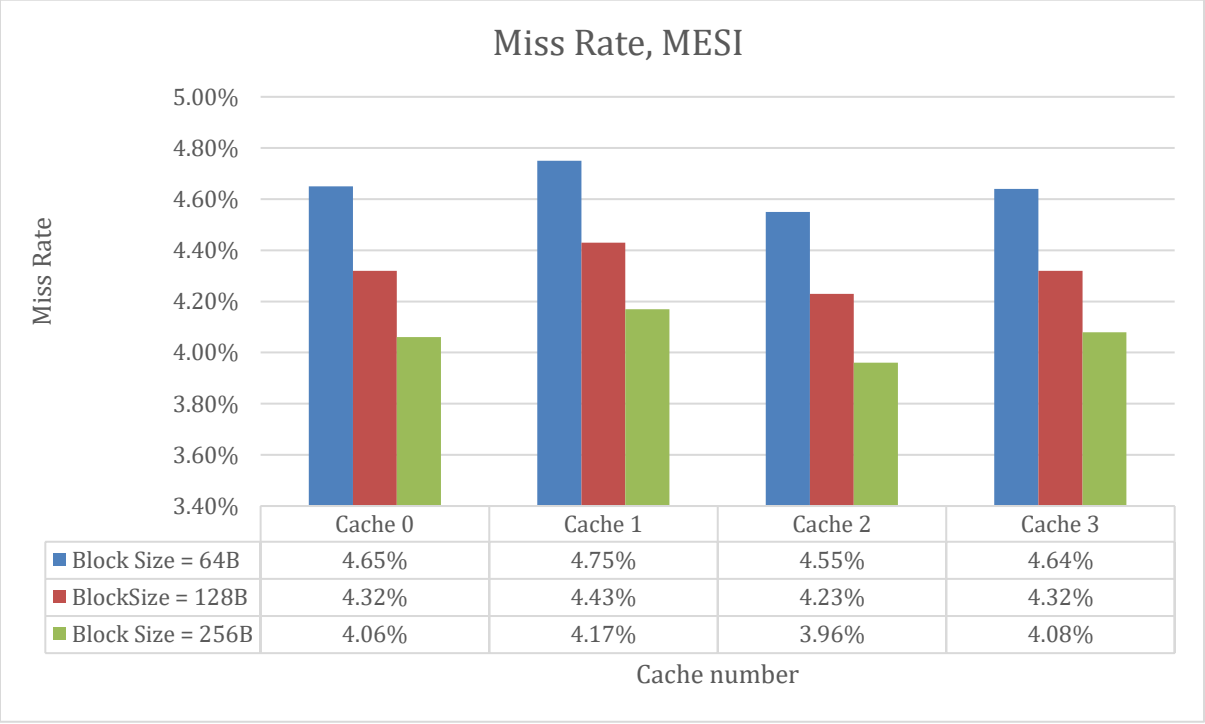


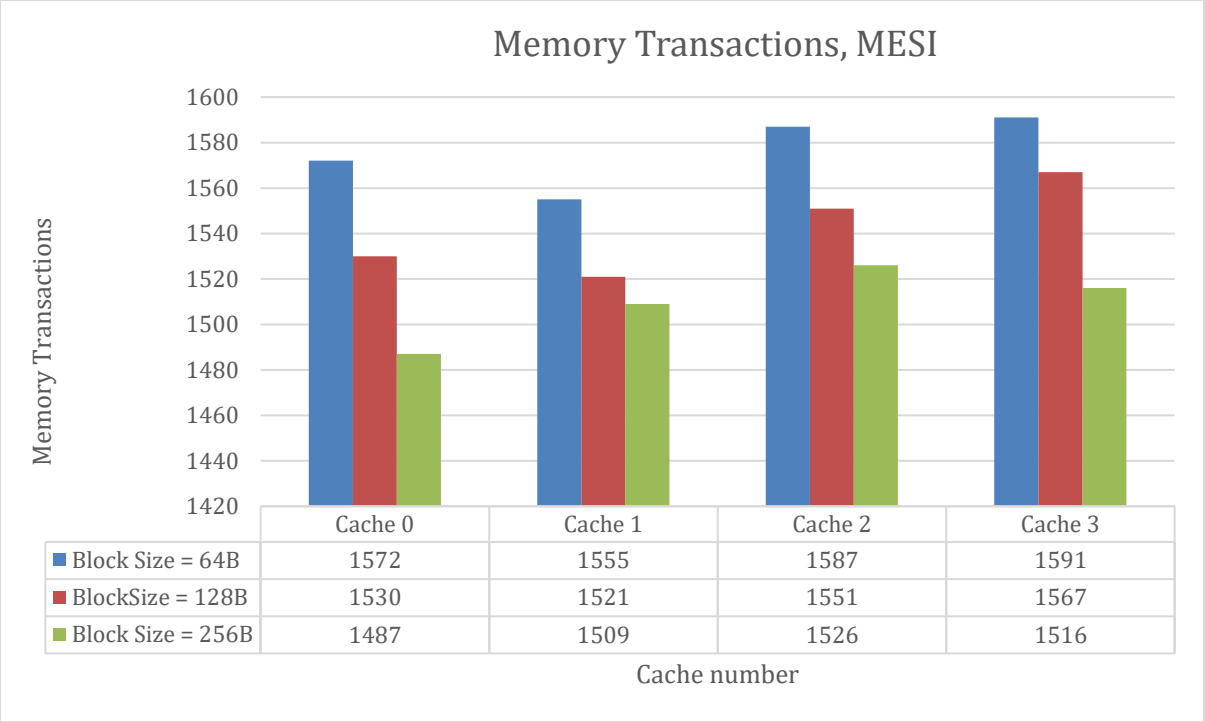
	Cache 0	Cache 1	Cache 2	Cache 3
Block Size = 64B	716	700	725	714
BlockSize = 128B	729	711	745	733
Block Size = 256B	751	735	780	743

MESI:

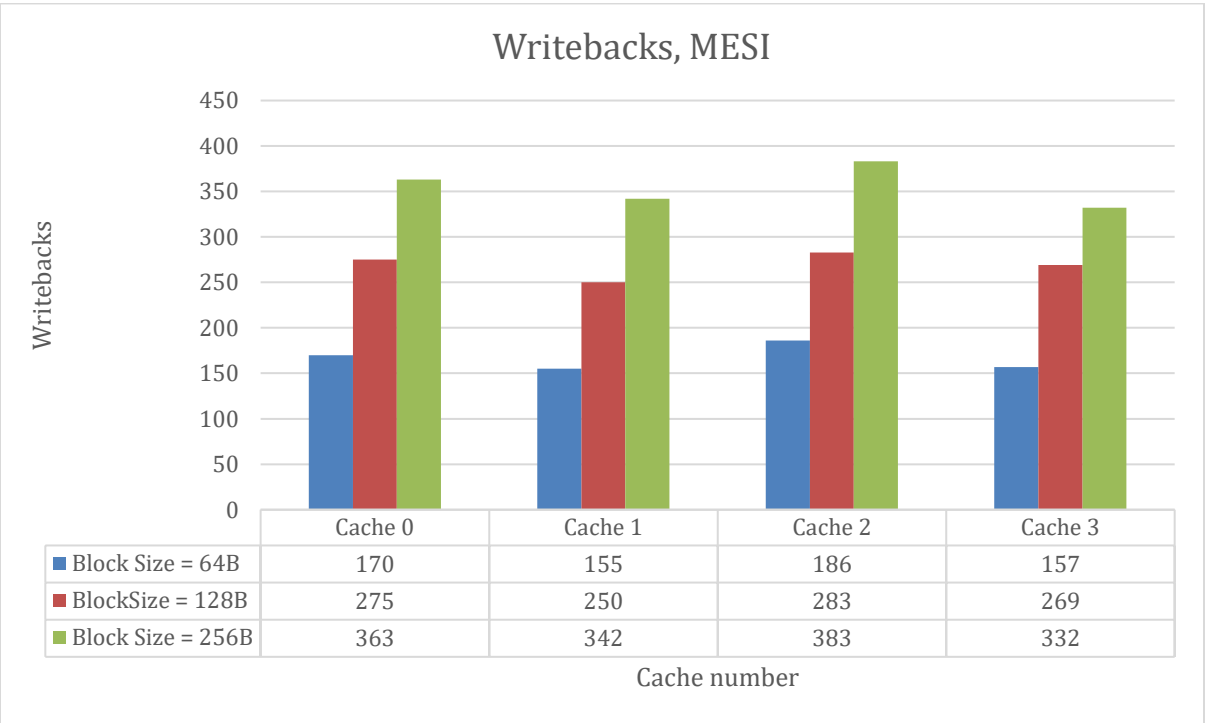
Block Size		Cache 0	Cache 1	Cache 2	Cache 3
64B	Reads	112661	110830	114938	113428
	Read Misses	5752	5781	5752	5790
	Writes	11942	11710	12383	12108
	Write Misses	39	41	42	39
	Miss Rate	4.65%	4.75%	4.55%	4.64%
	Writebacks	170	155	186	157
	C-C transfers	4389	4422	4393	4395
	Memory Transactions	1572	1555	1587	1591
	Interventions	1464	1428	1464	1474
	Invalidations	2014	2034	2008	2020
	Flushes	116	93	121	89
	BusRdX	39	41	42	39
Block Size		Cache 0	Cache 1	Cache 2	Cache 3
128B	Reads	112661	110830	114938	113428
	Read Misses	5340	5386	5341	5384
	Writes	11942	11710	12383	12108
	Write Misses	39	40	42	39
	Miss Rate	4.32%	4.43%	4.23%	4.32%
	Writebacks	275	250	283	269
	C-C transfers	4124	4155	4115	4125
	Memory Transactions	1530	1521	1551	1567
	Interventions	1367	1337	1377	1385
	Invalidations	2066	2089	2053	2068
	Flushes	164	129	166	135
	BusRdX	39	40	42	39
Block Size		Cache 0	Cache 1	Cache 2	Cache 3

256B	Reads	112661	110830	114938	113428
	Read Misses	5023	5070	5004	5084
	Writes	11942	11710	12383	12108
	Write Misses	39	40	42	39
	Miss Rate	4.06%	4.17%	3.96%	4.08%
	Writebacks	363	342	383	332
	C-C transfers	3938	3943	3903	3939
	Memory Transactions	1487	1509	1526	1516
	Interventions	1283	1284	1321	1309
	Invalidations	2132	2157	2107	2148
	Flushes	211	178	231	170
	BusRdX	39	40	42	39





	Cache 0	Cache 1	Cache 2	Cache 3
Block Size = 64B	1572	1555	1587	1591
BlockSize = 128B	1530	1521	1551	1567
Block Size = 256B	1487	1509	1526	1516

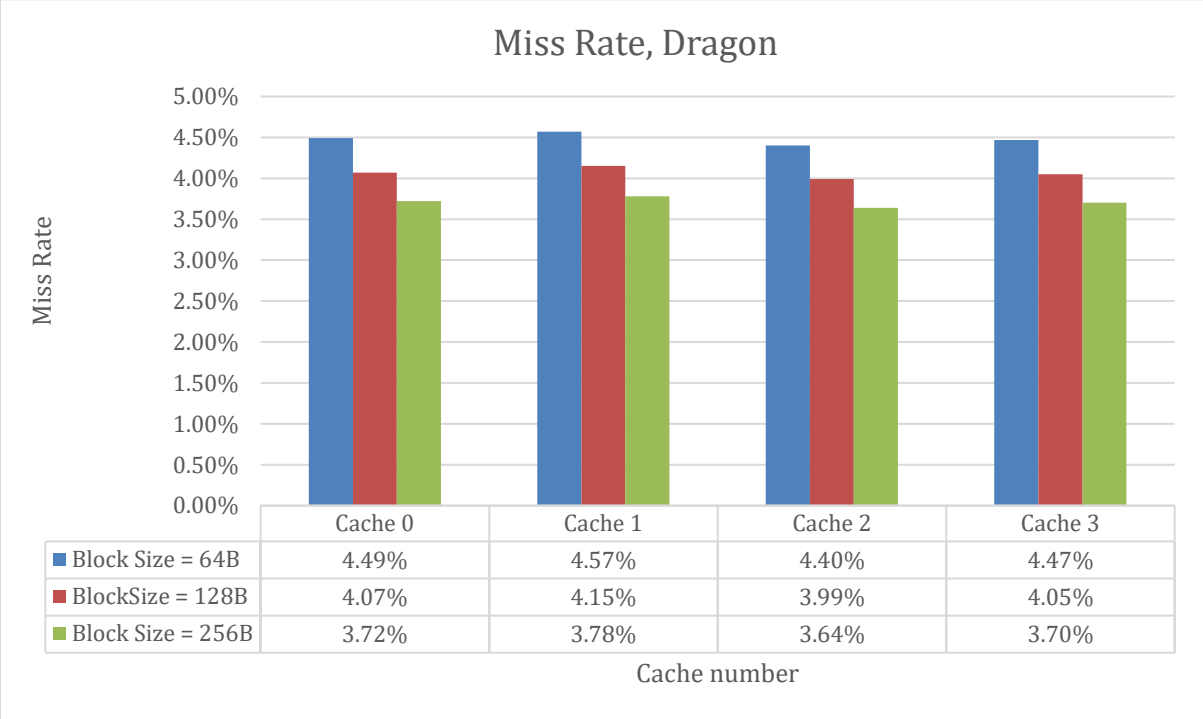


	Cache 0	Cache 1	Cache 2	Cache 3
Block Size = 64B	170	155	186	157
BlockSize = 128B	275	250	283	269
Block Size = 256B	363	342	383	332

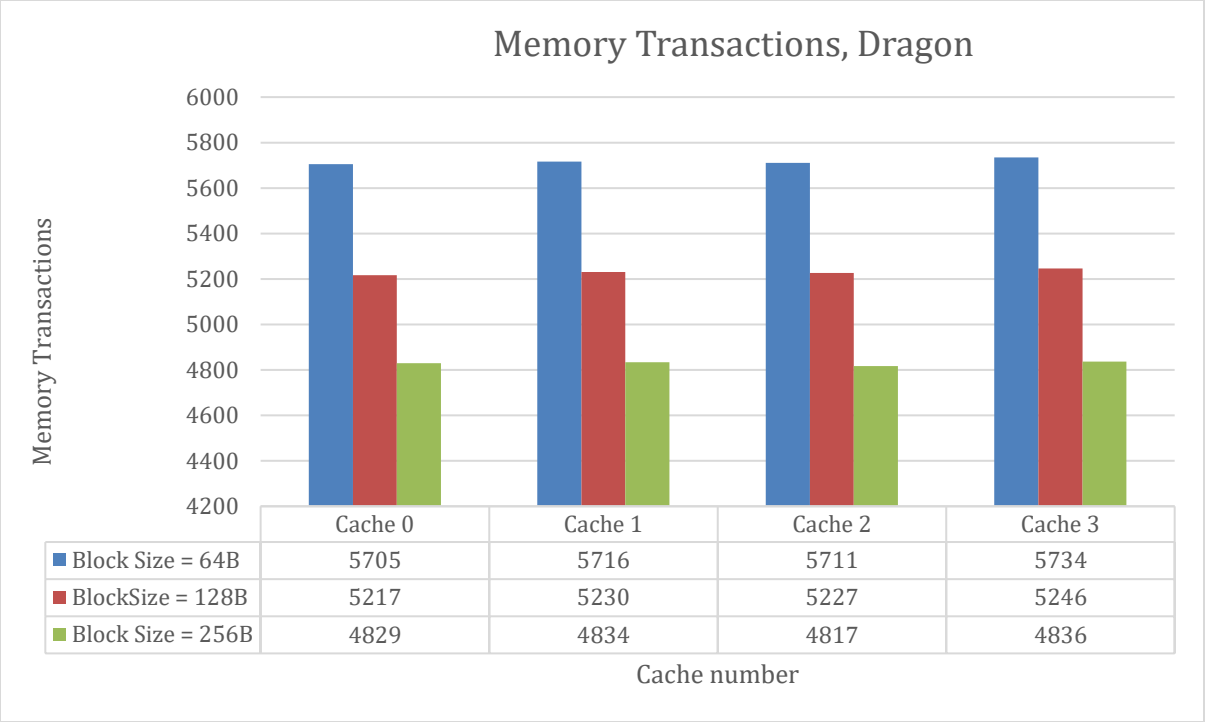
Dragon:

Block Size		Cache 0	Cache 1	Cache 2	Cache 3
64B	Reads	112661	110830	114938	113428
	Read Misses	5595	5604	5604	5611
	Writes	11942	11710	12383	12108
	Write Misses	3	2	2	0
	Miss Rate	4.49%	4.57%	4.40%	4.47%
	Writebacks	107	110	105	123
	C-C transfers	0	0	0	0
	Memory Transactions	5705	5716	5711	5734
	Interventions	1398	1387	1387	1417
	Invalidations	0	0	0	0
	Flushes	3	9	6	6
	BusRdX	0	0	0	0
Block Size		Cache 0	Cache 1	Cache 2	Cache 3
128B	Reads	112661	110830	114938	113428
	Read Misses	5069	5080	5080	5086
	Writes	11942	11710	12383	12108
	Write Misses	3	1	2	0
	Miss Rate	4.07%	4.15%	3.99%	4.05%
	Writebacks	145	149	145	160
	C-C transfers	0	0	0	0
	Memory Transactions	5217	5230	5227	5246
	Interventions	1256	1266	1257	1287
	Invalidations	0	0	0	0
	Flushes	3	9	6	9
	BusRdX	0	0	0	0
Block Size		Cache 0	Cache 1	Cache 2	Cache 3

256B	Reads	112661	110830	114938	113428
	Read Misses	4628	4633	4630	4640
	Writes	11942	11710	12383	12108
	Write Misses	3	1	2	0
	Miss Rate	3.72%	3.78%	3.64%	3.70%
	Writebacks	198	200	185	196
	C-C transfers	0	0	0	0
	Memory Transactions	4829	4834	4817	4836
	Interventions	1125	1175	1143	1176
	Invalidations	0	0	0	0
	Flushes	3	11	9	9
	BusRdX	0	0	0	0

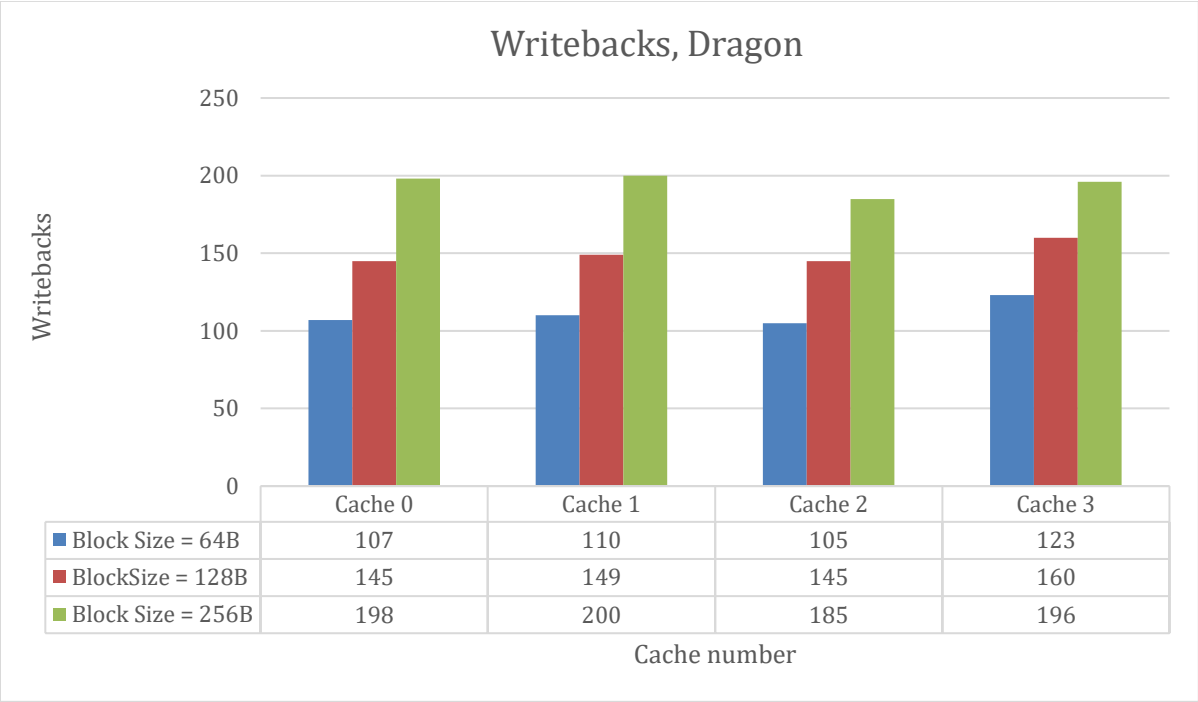


As the block size increases, the miss rate drops because a larger block size helps in spatial locality. The miss rates of all the cache are very similar because of the similar configurations of the cache. The variation of block size with miss rate also depends on the cache size. A smaller cache size can lead to an increase in the miss rate because of increase in conflict misses due to increase in block size.



	Cache 0	Cache 1	Cache 2	Cache 3
Block Size = 64B	5705	5716	5711	5734
BlockSize = 128B	5217	5230	5227	5246
Block Size = 256B	4829	4834	4817	4836

The above trend is observed because of a good spatial locality. Bigger block size helps improve the spatial locality which leads to a decrease in the number of times the memory has to be accessed since a bigger block brings a larger chunk of memory into the cache at a time.



	Cache 0	Cache 1	Cache 2	Cache 3
Block Size = 64B	107	110	105	123
BlockSize = 128B	145	149	145	160
Block Size = 256B	198	200	185	196

4) Comparison between MSI, MESI and Dragon Protocols
   Cache Size: 1MB
   Associativity: 8
   Block Size: 128B

MSI:

	Cache 0	Cache 1	Cache 2	Cache 3
Reads	112661	110830	114938	113428
Read Misses	5340	5386	5341	5384
Writes	11942	11710	12383	12108
Write Misses	39	40	42	39
Miss Rate	4.32%	4.43%	4.23%	4.43%
Writebacks	275	250	283	269
C-C transfers	0	0	0	0
Memory Transactions	6344	6347	6369	6386
Interventions	119	84	127	110
Invalidations	2066	2089	2053	2068
Flushes	164	129	166	135
BusRdX	729	711	745	733

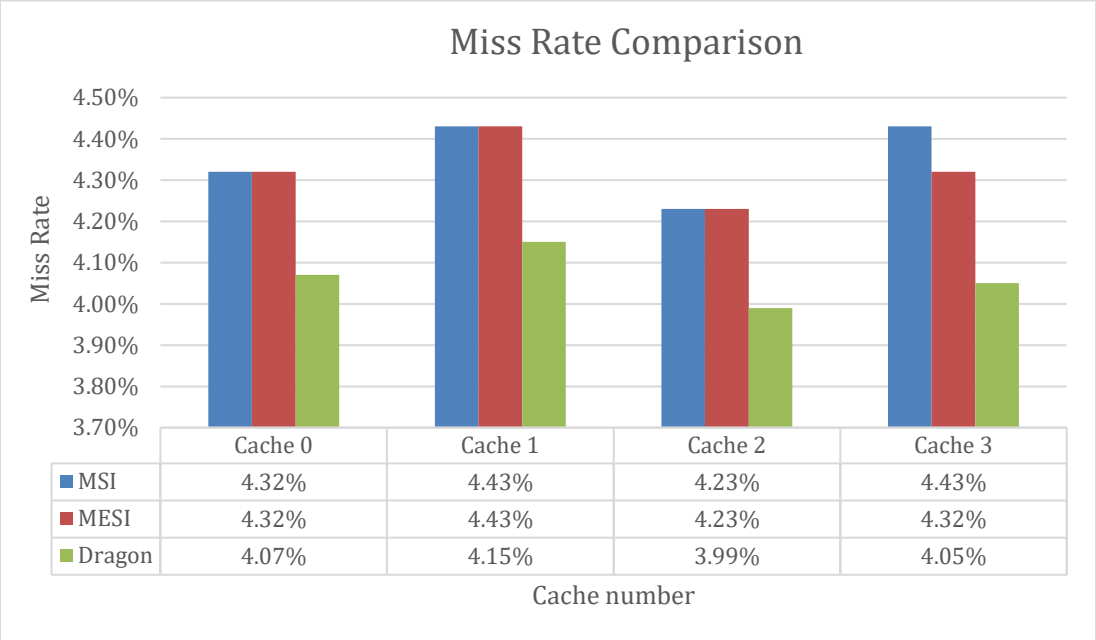
MESI:

	Cache 0	Cache 1	Cache 2	Cache 3
Reads	112661	110830	114938	113428
Read Misses	5340	5386	5341	5384
Writes	11942	11710	12383	12108
Write Misses	39	40	42	39
Miss Rate	4.32%	4.43%	4.23%	4.32%
Writebacks	275	250	283	269
C-C transfers	4124	4155	4115	4125
Memory Transactions	1530	1521	1551	1567
Interventions	1367	1337	1377	1385
Invalidations	2066	2089	2053	2068
Flushes	164	129	166	135

BusRdX	39	40	42	39

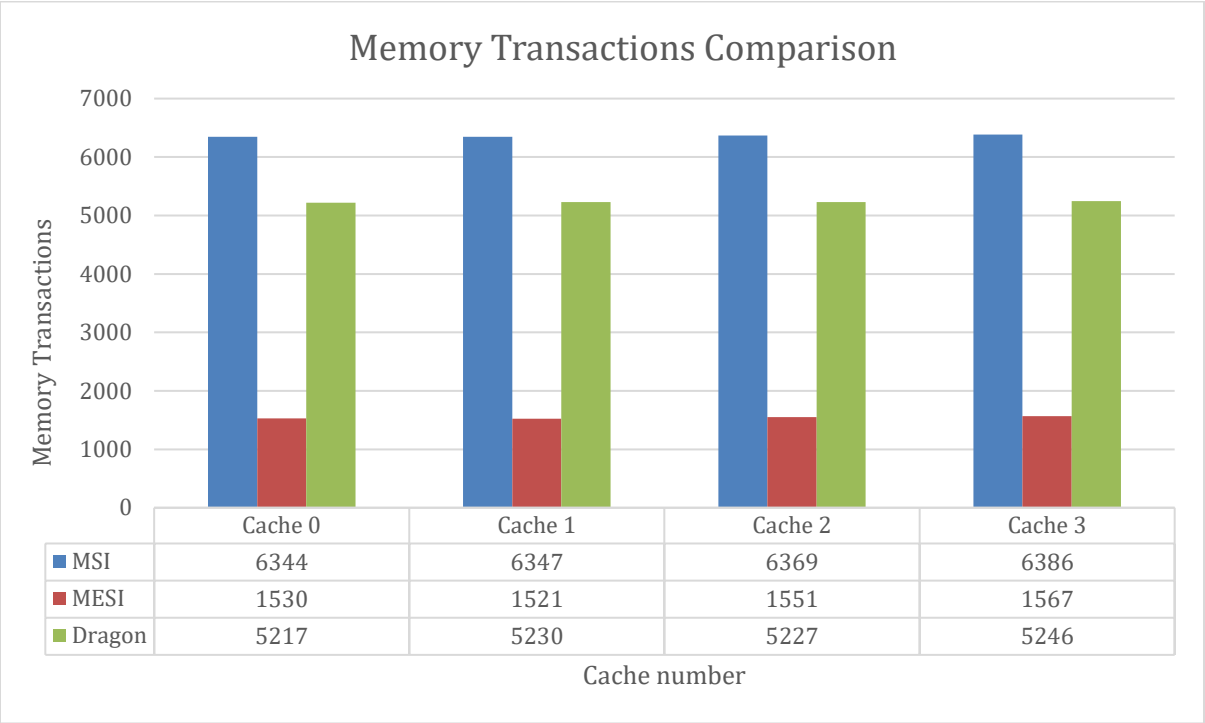
Dragon:

	Cache 0	Cache 1	Cache 2	Cache 3
Reads	112661	110830	114938	113428
Read Misses	5069	5080	5080	5086
Writes	11942	11710	12383	12108
Write Misses	3	1	2	0
Miss Rate	4.07%	4.15%	3.99%	4.05%
Writebacks	145	149	145	160
C-C transfers	0	0	0	0
Memory Transactions	5217	5230	5227	5246
Interventions	1256	1266	1257	1287
Invalidations	0	0	0	0
Flushes	3	9	6	9
BusRdX	0	0	0	0



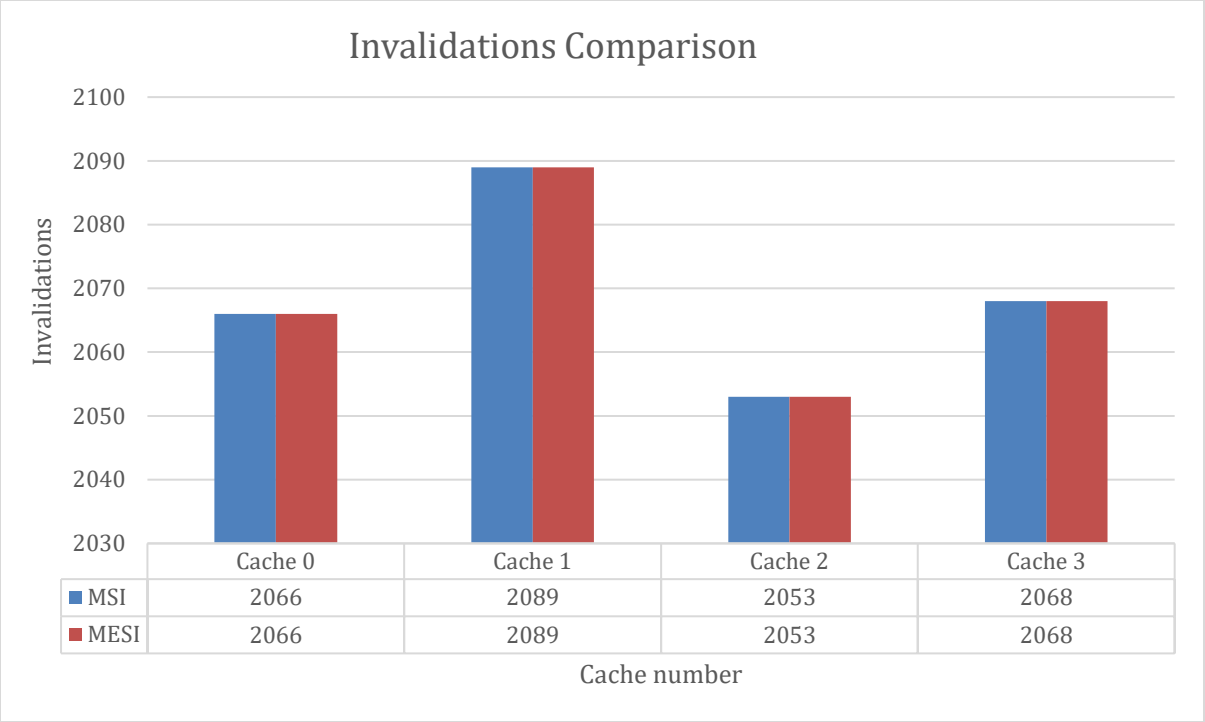
As expected, the Dragon protocol has a lesser miss rate than MSI and MESI. In MSI, when there is a processor write request, the processor posts a BusRdX on the bus. The other caches respond to this by invalidating their cache blocks. Similarly,

cache blocks can be invalidated in MESI as well. However, there is no invalid state in Dragon protocol. Hence, the miss rate of MSI and MESI is a bit higher than that of Dragon protocol because of the invalidations.



	Cache 0	Cache 1	Cache 2	Cache 3
MSI	6344	6347	6369	6386
MESI	1530	1521	1551	1567
Dragon	5217	5230	5227	5246

The cache-to-cache transfer in MESI in the case of FlushOpt reduces the number of memory transactions in MESI. The main memory does not need to be updated when a FlushOpt is issued on the bus. In case of a BusRd one of the cache supplies the value to the processor through FlushOpt. In case of a BudRdX, one of the copies if flushed to the bus and then invalidated.



Whenever a BusRdX is placed by any of the processor, invalidation takes place and is applicable for both MSI and MESI. Dragon protocol does not have an Invalid state. Therefore, invalidations are not shown for Dragon protocol.