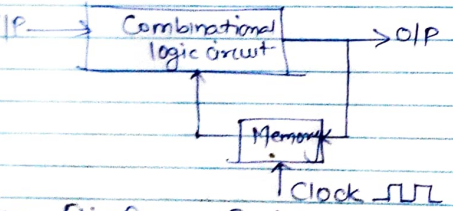
Flipflops

Combinational circuit :-

- o/p depends only on level present at i/p terminals
- Don't use memory
- Clock signal is not used.
- e.g. full adder, full subtractor, multiplexer

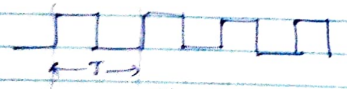
Sequential circuit

- o/p depends upon present i/p, previous o/p,
- for previous o/p memory is required.
- Clock signal is present.



- eg. Flipflops, Register, counter

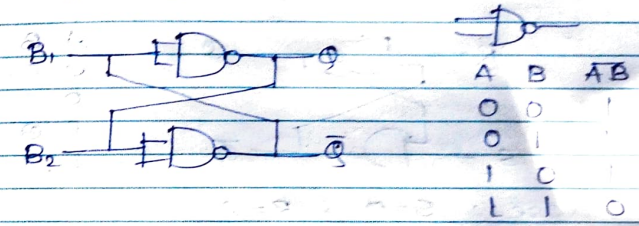
Clock signal



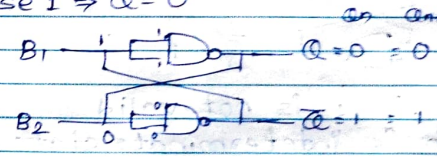
It is a timing signal applied as an i/p signal with duty cycle.

Flip Flop

- It is a basic memory elements.
- It is a 1 bit memory cell.
- It is designd using two NAND/NOR gates & has two stable states 0 & 1.
- o/p of gate 1 is connected to i/p of gate 2 & o/p of gate 2 is connected to i/p of gate 1.



Case 1 ⇒ Q = 0



Case 2 ⇒ Q = 1

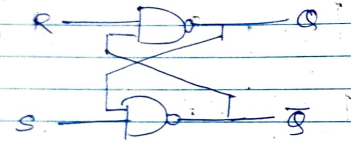
① They will never be equal.
$Q = \bar{Q} \neq 0 \quad Q = \bar{Q} \neq 1$

② $Q = 1 \quad \bar{Q} = 0 \longrightarrow$ Set state
$Q = 0 \quad \bar{Q} = 1 \longrightarrow$ Reset state

Flip flop

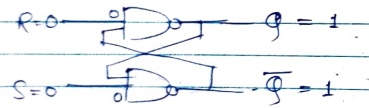
1. SR latch
2. SR flip flop
3. D flip flop
4. T flip flop
5. JK flip-flop

① SR Latch using NAND gates



A	B	$A\bar{B}$
0	0	1
0	1	1
1	0	1
1	1	0

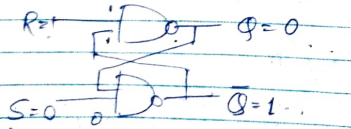
Case 1: S=0 & R=0



$Q = \bar{Q} = 1$ is not valid

which is indeterminate state & called as "RACE condition".

Case 2: S=0 R=1

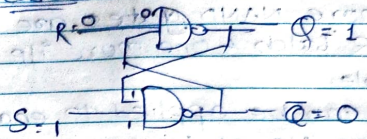


if S=0 & R=1 then

we get $Q = 0$ & $\bar{Q} = 1$

This is called "RESET condition".

Case 3: S=1 R=0

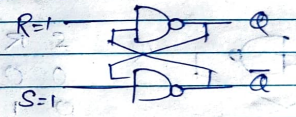


When S=1 & R=0 then

we get $Q = 1$ & $\bar{Q} = 0$

This is set condition.

Case 4 S=1 R=1



$Q = \overline{R\bar{Q}}$ $\quad \bar{Q} = \overline{SQ}$

$= \bar{R} + \bar{\bar{Q}}$ $\quad = \bar{S} + \bar{Q}$

$= 0 + Q$ $\quad = 0 + \bar{Q}$

$= Q$ $\quad = \bar{Q}$

When S=1 & R=1

we get $Q = Q$ $\bar{Q} = \bar{Q}$

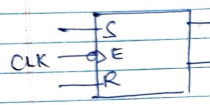
This is "No change condition".

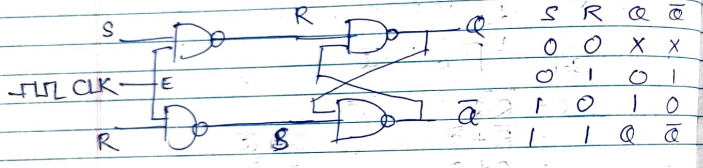
Truth Table of SR Latch

S	R	Q_n	$\bar{Q}_n$	
0	0	X	X	RACE
0	1	0	1	RESET
1	0	1	0	SET
1	1	Q	$\bar{Q}$	No change

Gated Latch - SRFF

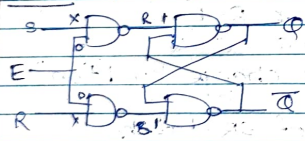
- In this 2 more NAND gates are added to basic SR latch & one more i/p called Enable
- Clock signal can be applied to enable(E)
- FF are called "level triggered FF"/ gated latch/clocked FF.





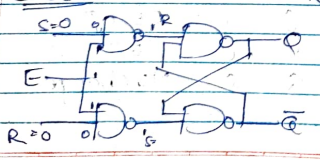
S	R	Q	$\bar{Q}$
0	0	X	X
0	1	0	1
1	0	1	0
1	1	Q	$\bar{Q}$

case 1: E=0 S=X R=X



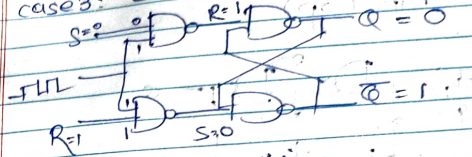
No change

case 2: E=1 S=0 R=0



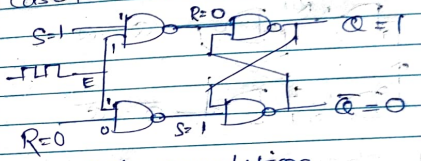
No change

case 3: E=1 S=0 R=1



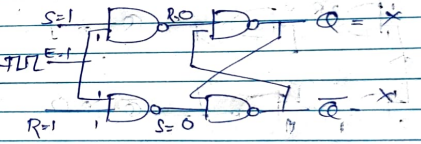
Reset condition

case 4: E=1 S=1 R=0



Set condition

case 5: E=1 S=1 R=1

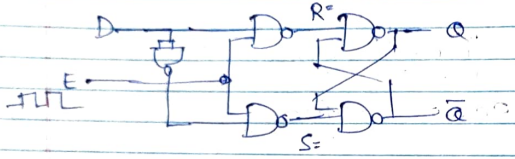


RACE condition

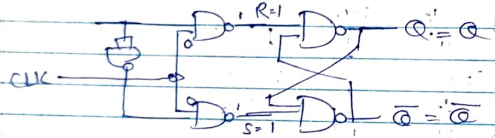
Truth Table SRFF

E	S	R	Q	$\bar{Q}$	
0	X	X	Q	$\bar{Q}$	No change
1	0	0	Q	$\bar{Q}$	No change
1	0	1	0	1	RESET
1	1	0	1	0	SET
1	1	1	X	X	RACE

DFF (Gated D Latch)
(Data flip flop)

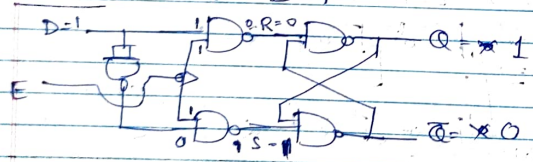


case 1 E=0 D=X



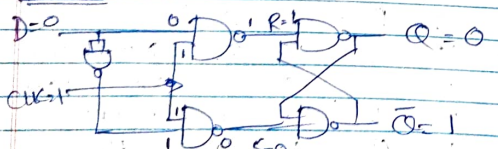
NO change

case 2 E=1 D=1



Set condition

case 3 E=1 D=0

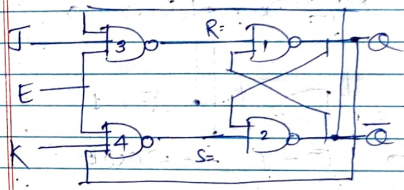


RESET cond^n

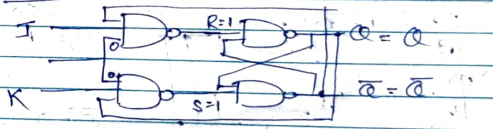
Truth Table

E	D	Q	$\bar{Q}$	
0	X	Q	$\bar{Q}$	NO change
1	0	0	1	Reset cond^n
1	1	1	0	Set cond^n

JKFF (JK flip flop)
(Jack kilby : Invented IC in 1958

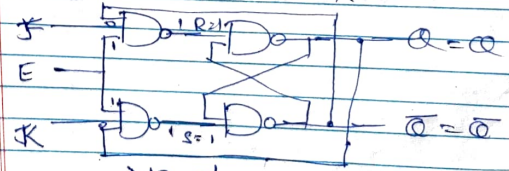


case 1 E=0 J=X K=X



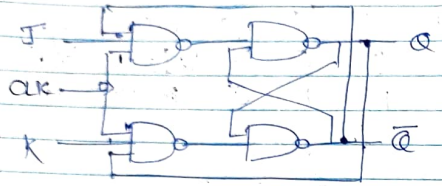
NO change

case 2 E=1 J=0 K=0

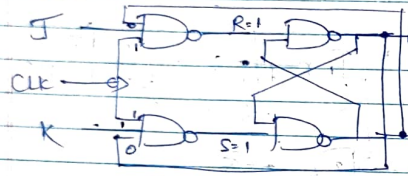


NO change

Case 3 E=1 J=0 K=1

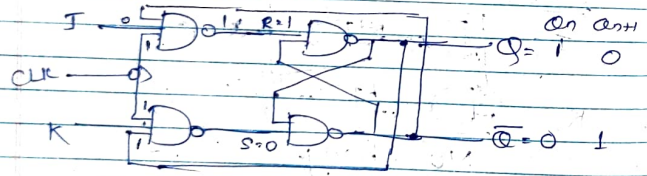


① Q=0 J=0 K=1



Q=0 $\overline{Q}$=1 — Reset

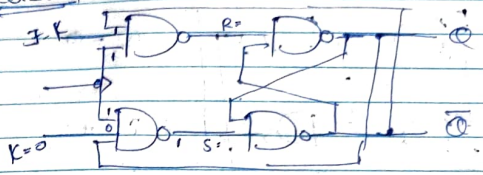
② Q=1 J=0 K=1



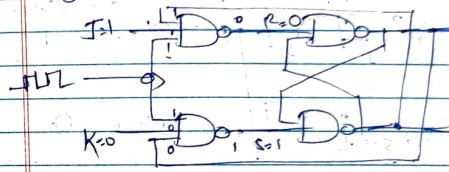
Q=1 $\overline{Q}$=0 S=0 R=1

Q=0 $\overline{Q}$=1 → Reset

Case 4 E=1 J=1 K=0



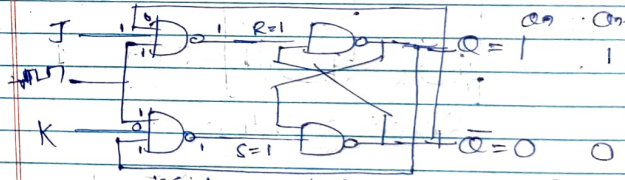
① Q=0 J=1 K=0



When S=1 R=0

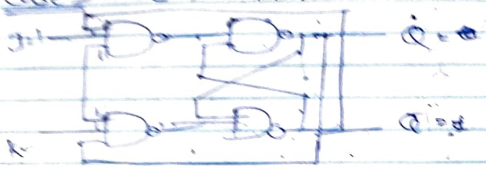
Set condition

② Q=1 J=1 K=0

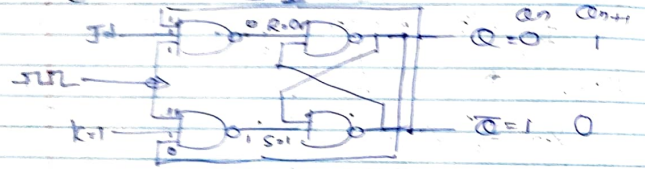


Set condition

Case 5 J=1 K=1

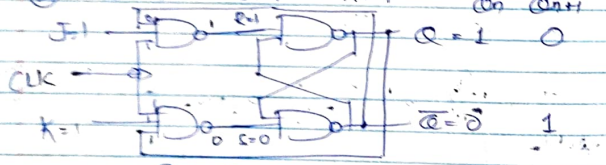


① Q=0 J=1 K=1



Set condition

② Q=1 J=1 K=1

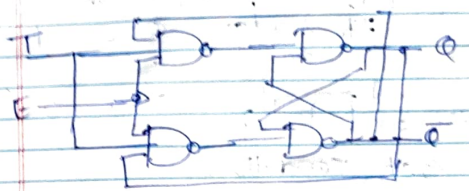


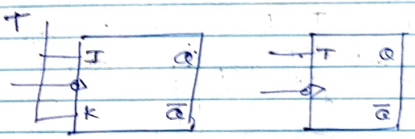
Reset condition

① Q=0 J=1 K=1 Set } Toggle
② Q=1 J=1 K=1 Reset }

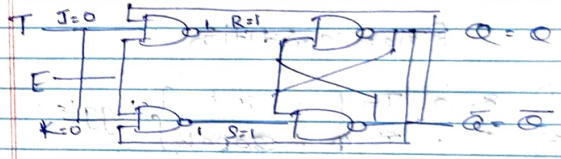
E	J	K	Q	$\overline{Q}$	
0	X	X	Q	$\overline{Q}$	No change
1	0	0	Q	$\overline{Q}$	No change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	$\overline{Q}$	Q	Toggle

TFT (Toggle flip flop)



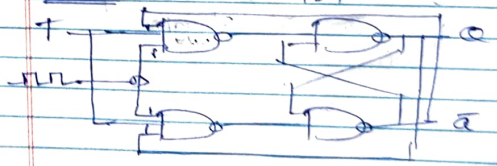


Case 1 E=1 T=0

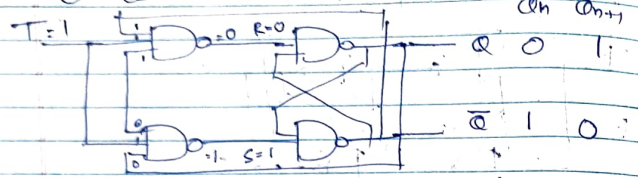


No change

Case 2 E=1 T=1

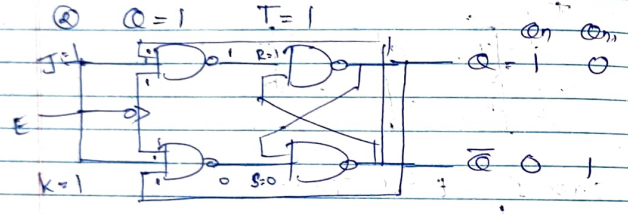


① $Q=0$ $T=1$



Set condition

② $Q=1$ $T=1$



Reset condition

① $Q=0$ $T=1$ – set
② $Q=1$ $T=0$ – Reset
} Toggle

E	T	Q	$\bar{Q}$	
1	0	Q	$\bar{Q}$	No change
1	1	$\bar{Q}$	Q	Toggle

Truth Table

SR Latch

S	R	Q	$\bar{Q}$	
0	0	X	X	RACE
0	1	0	1	RESET
1	0	1	0	SET
1	1	Q	$\bar{Q}$	Nochange

SR FF

S	R	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	Nochange
0	1	0	1	RESET
1	0	1	0	SET
1	1	X	X	RACE

DFF

D	Q	$\bar{Q}$	
0	0	1	RESET
1	1	0	SET

TFF

T	Q	$\bar{Q}$	
0	Q	$\bar{Q}$	Nochange
1	$\bar{Q}$	Q	Toggle

JK FF

J	K	Q	$\bar{Q}$	
0	0	Q	$\bar{Q}$	Nochange
0	1	0	1	RESET
1	0	1	0	SET
1	1	$\bar{Q}$	Q	Toggle

Excitation Table

excitation table shows that minimum i/p that are necessary to generate next state, when current state is known.

		Present		Next	
S	R	Q_n	$\bar{Q}_n$	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	⊗	⊗	X	X
1	1	⊗	⊗	X	X

Present	Next	S	R	
0	0	0	X	□
0	1	1	0	△
1	0	0	1	○
1	1	X	0	⌂

D	Q	$\bar{Q}$
0	0	1
1	1	0

Excitation Table of DFF

	Present		Next	
D	Q_n	$\bar{Q}_n$	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	1	0	1
	1	0	0	1
1	0	1	1	0
	1	0	1	0

Excitation Table

Present	Next	
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

T	Q	$\bar{Q}$
0	0	1
	1	0
1	0	1
	1	0

Excitation Table of T-FF

	Present		Next	
T	Q_n	$\bar{Q}_n$	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	1	0	1
	1	0	1	0
1	0	1	1	0
	1	0	0	1

Excitation Table

Present	Next	
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table of JKFF

		Present		Next	
J	K	Q_n	$\bar{Q}_n$	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	0	1	0	1
		1	0	1	0
0	1	0	1	0	1
		1	0	0	1
1	0	0	1	1	0
		1	0	1	0
1	1	0	1	1	0
		1	0	0	1

Excitation Table

Present Q_n	Next Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table

Present	Next	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

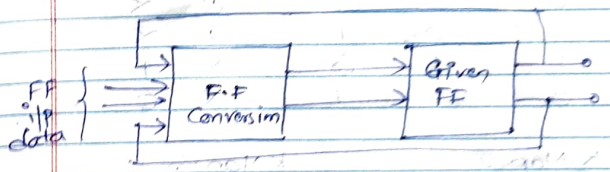
Present	Next	D
0	0	0
0	1	1
1	0	0
1	1	1

Present	Next	T
0	0	0
0	1	1
1	0	1
1	1	0

Present	Next	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Flip flop conversion

To convert one type of FF to another type of FF we use excitation Table & K-Map



convert SRFF to DFF

D	Present Q_n	Next Q_{n+1}	S	R
0	0	0	0	X
1	0	1	1	0
0	1	0	0	1
1	1	1	X	0

K-Map for S

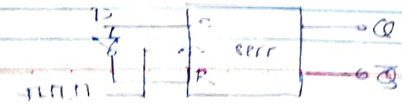
D \ Q_n	$\bar{Q}_n$	Q_n
$\bar{D}$	0	0
D	1	X

S = D

K-Map for R

D \ Q_n	$\bar{Q}_n$	Q_n
$\bar{D}$	X	1
D	0	0

$R = \bar{D}$



JKFF TO TFF

T	Present Q_n	Next Q_{n+1}	J	K
0	0	0	0	X
1	0	1	1	X
1	1	0	X	1
0	1	1	X	0

K-Map J

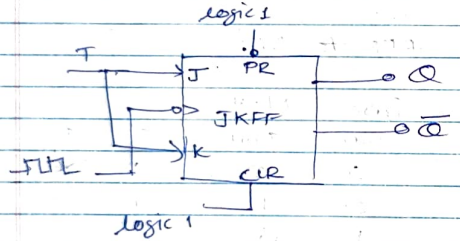
T \ Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$	0 (0)	X (1)
T	1 (2)	X (3)

k-Map for K

T \ Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$	X (0)	0 (1)
T	X (2)	1 (3)

J=T

K=T



SRFF TO TFF

T	Present Q_n	Next Q_{n+1}	S	R
0	0	0	0	X
1	0	1	1	0
1	1	0	0	1
0	1	1	X	0

K-Map for S

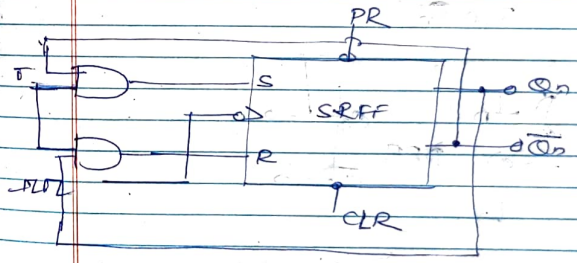
T \ Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$	0 (0)	X (1)
T	1 (2)	0 (3)

K-Map for R

T \ Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$	X (0)	0 (1)
T	0 (2)	1 (3)

$S = T\bar{Q}_n$

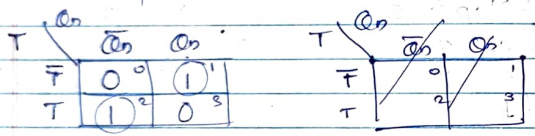
$R = TQ_n$



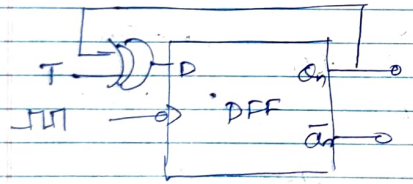
D-FF to TFF

T	Present	Next	D
0	0	0	0
1	0	1	1
1	1	0	0
0	1	1	1

K-Map for D



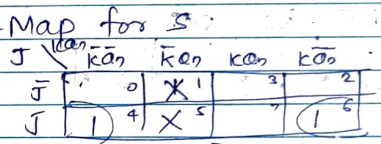
$$D = T\bar{Q}_n + TQ_n$$
$$= T \oplus \bar{Q}_n$$



SRFF TO JKFF

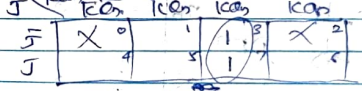
	J	K	Present	Next	S	R
0	0	0	0	0	0	X
2	0	1	0	0	0	X
4	1	0	0	1	1	0
6	1	1	0	1	1	0
3	0	1	1	0	0	1
7	1	1	1	0	0	1
1	0	0	1	1	X	0
5	1	0	1	1	X	0

K-Map for S

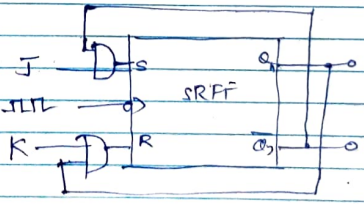


$$S = J\bar{Q}_n$$

K-Map for R



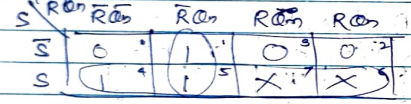
$$R = K\bar{Q}_n$$



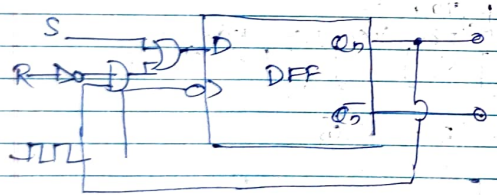
DFF to SRFF

	S	R	Present	Next	D
0	0	0	0	0	0
2	0	1	0	0	0
4	1	0	0	1	1
4	1	0	0	1	1
3	0	1	1	0	0
3	0	1	1	0	0
1	0	0	1	1	1
5	1	0	1	1	1

K Map for D



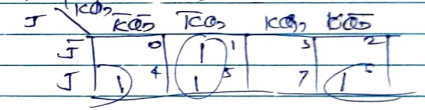
$D = S + \bar{R}Q_n$



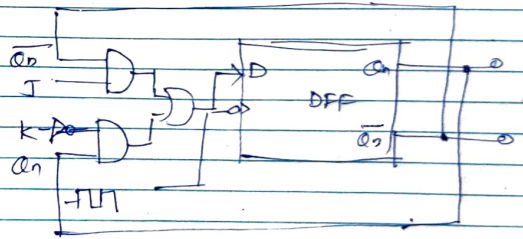
DFF to JKFF

	J	K	Q_n	Q_{n+1}	D
0	0	0	0	0	0
2	0	1	0	0	0
4	1	0	0	1	1
6	1	1	0	1	1
3	0	1	1	0	0
7	1	1	1	0	0
1	0	0	1	1	1
5	1	0	1	1	1

K-Map for D



$D = J\bar{Q}_n + \bar{K}Q_n$



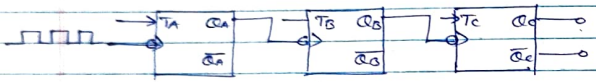
Counter

A digital circuit used for counting the pulses is known as counters.

Types of counter
① Asynchronous
② Synchronous

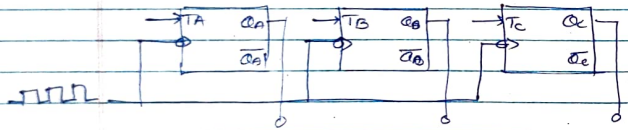
Up
Down
Up/Down counter

Asynchronous counter



In these external clk signal is applied to one FF & then o/p of preceding FF is connected to clk of next FF.

Synchronous counter



In these all FF receive the external clk pulse applied simultaneously.

Up counter: count from small to big
0-1-2-3-4-5-6-7-0

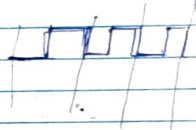
Down counter: count from Big to small
e.g. 7-6-5-4-3-2-1-0-7

Up/Down counter: combination of up & down counter.

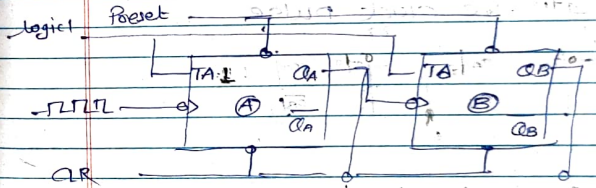
Asynchronous Up counter (Ripple)

We will use TFF as we need toggle o/p for counting

T	Q	$\overline{Q}$
0	$\overline{Q}$	Q
1	Q	$\overline{Q}$

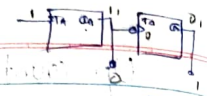


We can also use JKFF.



let initial cond^n of FF be reset
$Q_B Q_A = 00$

① On 1st -ve clock edge
FFA → will toggle $T_A = 1$ we get $Q_A = 1$
FFB → $Q_A = 1$ so positive edge trigger.
$Q_B = 0$
$Q_B Q_A = 01$



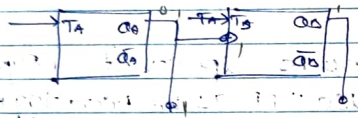
② On 2nd -ve clock pulse

FFA → will toggle TA=1 we get $Q_A=0$

FFB → TB=1 we get $Q_B=1$

$Q_B Q_A = 01$

③ On 3rd -ve clock pulse

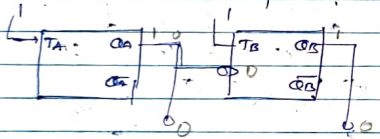


FFA → will toggle TA=1 we get $Q_A=1$

FFB → for FFB positive clk pulse so no change in Q_B ∴ $Q_B=1$

$Q_B Q_A = 11$

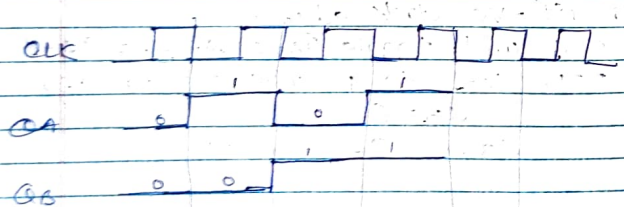
④ On 4th -ve clock pulse



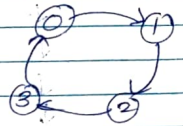
FFA → will toggle TA=1 we get $Q_A=0$

FFB → will toggle TB=1 we get $Q_B=0$

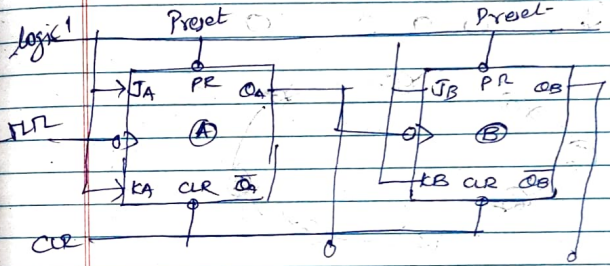
$Q_B Q_A = 00$



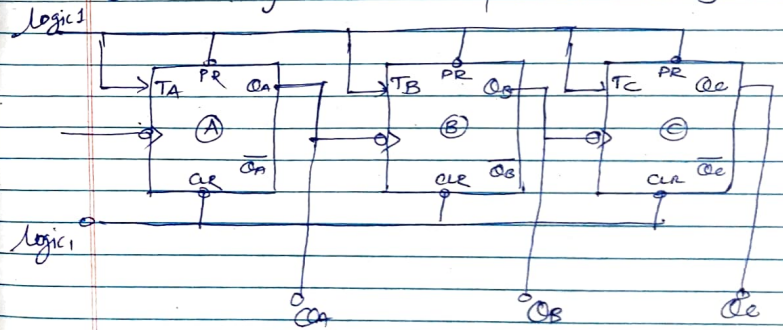
CLK	Q_B	Q_A	State
↓	0	0	0
↓	0	1	1
↓	1	0	2
↓	1	1	3
↓	0	0	0



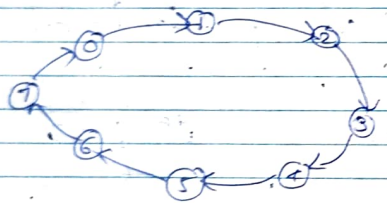
3 bit Asynchronous up counter using JKFF



3 bit Asynchronous up counter using TFF

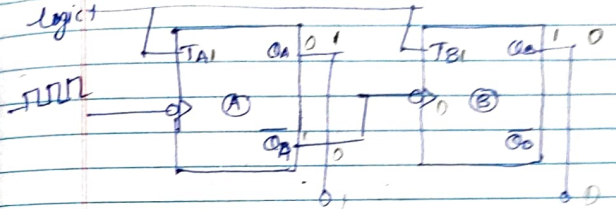


CLK	Q_C	Q_B	Q_A	Decimal
↓	0	0	0	0
↓	0	0	1	1
↓	0	1	0	2
↓	0	1	1	3
↓	1	0	0	4
↓	1	0	1	5
↓	1	1	0	6
↓	1	1	1	7
↓	0	0	0	0



Asynchronous up counter using JKFF

Asynchronous down counter using JFF 2 bit



Initially $Q_B Q_A = 00$

① 1st Negative clock cycle
FFA → will ~~trigger~~ toggle the o/p $Q_A = 1$
FFB → will also trigger the o/p $Q_B = 1$
$Q_B Q_A = 11$

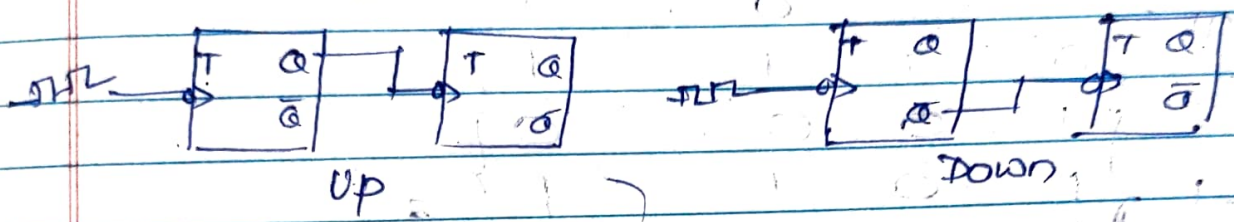
② 2nd Negative clock cycle
FFA → will ~~trigger~~ toggle the o/p $Q_A = 0$
FFB → FF will get positive clk ⊗ → $Q_B = 1$
$Q_B Q_A = 10$

③ 3rd Negative clock cycle
FFA → will toggle the o/p → $Q_A = 1$
FFB → FF get negative supply & FFB toggle the o/p → $Q_B = 0$
$Q_B Q_A = 01$

④ 4th Negative clock cycle.
FFA → will toggle the o/p → $Q_A = 0$
FFB → FF will get positive supply & FFB remain same with no change - $Q_B = 0$
$Q_B Q_A = 00$

Up/Down counter

Up & down counters are combined together. A mode control (M) i/p is used to select either up count or down count mode.



Up/Down Ripple

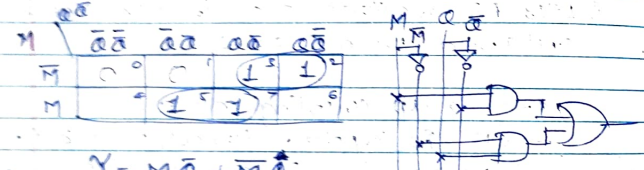
1. All FF operate in Toggle mode (T/JKFF)
2. LSB FF receives clk directly others obtained from Q or $\bar{Q}$

M=0 → up counting mode
→ clk is applied directly to clk i/p of LSB & remaining FF Q o/p of preceding FF is connected to next clk.

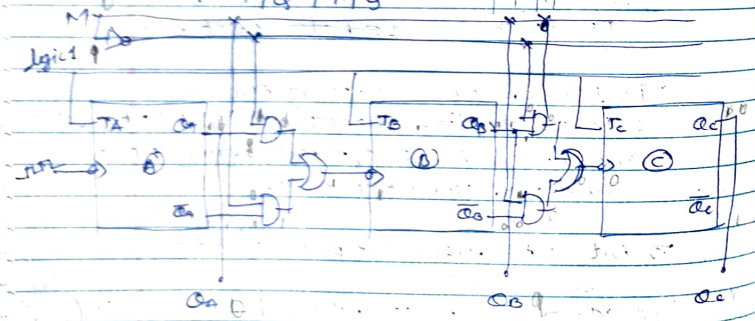
M=1 → down counting mode
clk is applied directly to clk i/p of LSB FF & remaining FF $\bar{Q}$ o/p preceding FF is connected to next clk.

3 bit up/down ripple counter
3 bit = 3 FF
If M=0 ; up counting → Q to clk
M=1 down counting → $\bar{Q}$ to clk

M	Q	$\bar{Q}$	Y	
0	0	0	0	M=0 Upcount $\bar{Q}$ as CLK → Q
0	0	1	0	
0	1	0	1	
0	1	1	1	
1	0	0	0	M=1 down count Q as clk → $\bar{Q}$
1	0	1	1	
1	1	0	0	
1	1	1	1	



$Y = M\bar{Q} + \bar{M}Q$



Modulus of counter (MOD-N counter)

1 bit ripple counter is called MOD-2 counter

2 bit MOD-4

3 bit ripple counter is called MOD-8

$N=4 \quad 2^n \geq N \quad 2^1 = 2 \quad 4 \leq 4$

$2^2 = 4$

is the number states in its count sequence.

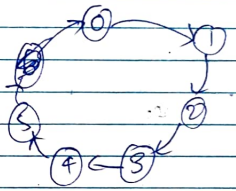
MOD-10 0 to 9 | MOD 7 0 to 6 | MOD 8 0-7

Q. Design MOD-6 Asynchronous counter using JK FF

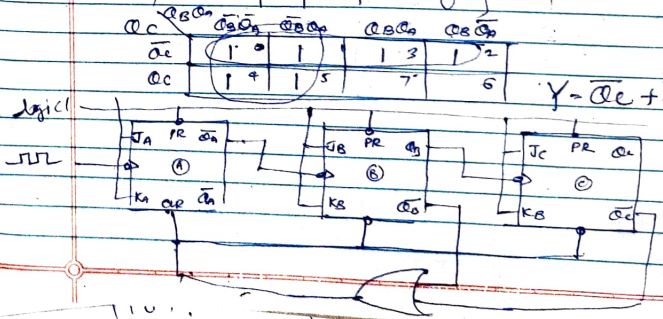
Number of flip-flop required to design MOD-6

$N=6 \quad 2^n \geq N \quad 2^n \geq 6$

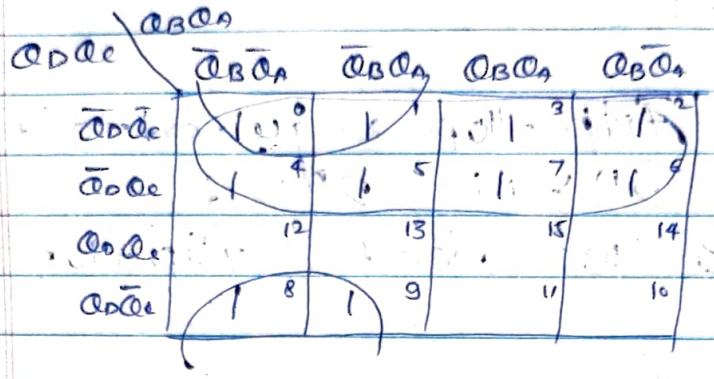
$n=3$ we need 3 flip flops.



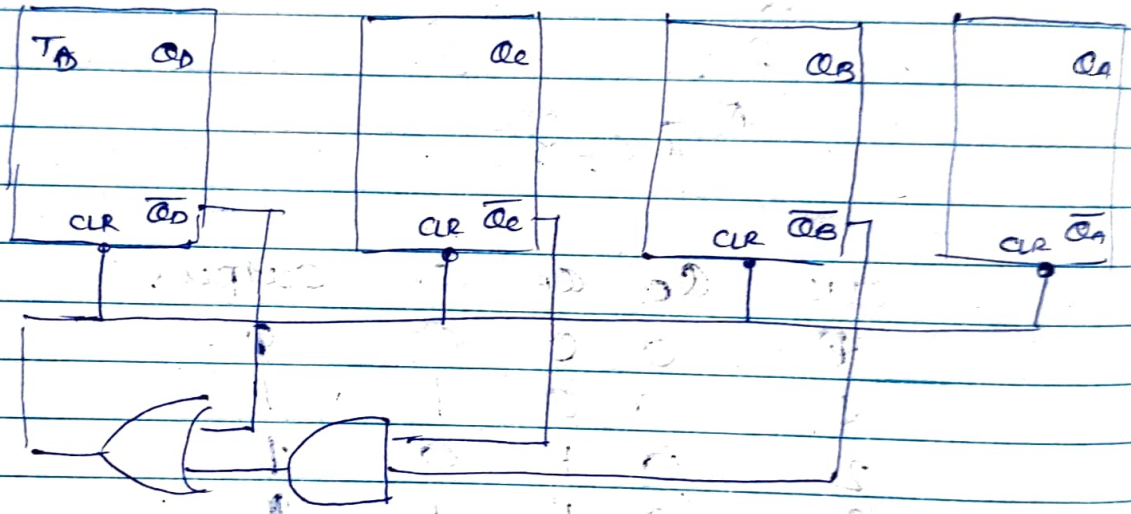
CLK	Q_C	Q_B	Q_A	output	
↓	0	0	0	0	
↓	0	0	1	1	
2	0	1	0	2	
3	0	1	1	3	
4	1	0	0	4	
5	1	0	1	5	
6	1	1	0	0	Invalid
7	1	1	1	0	



MOD-10 Asynchronous counter (BCD counter)



$Y = \bar{Q}_D + \bar{Q}_C \bar{Q}_B$



CLK	Q_D	Q_C	Q_B	Q_A	Y
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1