

Counters

A sequential circuit used to count the clock pulses is called counter.

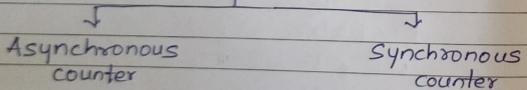
A flip-flop can store 1 bit of information.

If we want 2 bit binary counter, then it uses two flip-flops.

If three bit binary output is required, the counter uses 3 flip-flops.

Types of counters

Counter

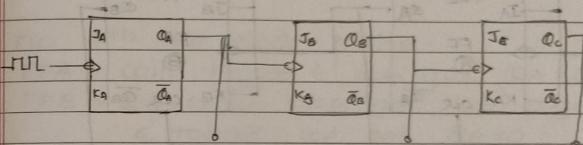


Classification of counter

- ① Up-counter
- ② Down-counter
- ③ Up/Down counter

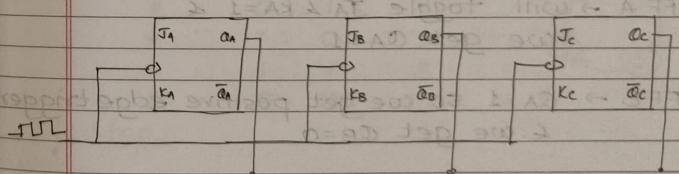
Asynchronous counter

In these external clk signal is applied to one FF and then QP of preceding FF is connected to clk of next FF.



Synchronous Counter

In these all FF receive the external clk pulse applied simultaneously.



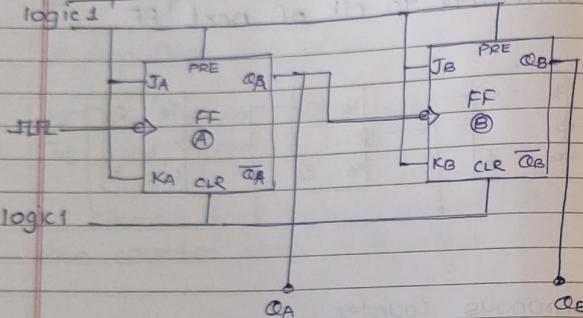
Up counter count from small to big
0 - 1 - 2 - 3 - 4 - 5 - 6 - 7 - 0

Down counter count from big to small
7 - 6 - 5 - 4 - 3 - 2 - 1 - 0 - 7

Up/Down counter is combination of Up & down Counter

Q Design 2 bit Asynchronous Ripple Counter using JKFF.

Step 1 logic 1



Initial Condition of FF be reset.

$$Q_2 Q_1 = 00$$

① On 1st -ve clock edge

FFA \rightarrow will toggle JA & KA=1 &
we get $Q_A=1$

FFB \rightarrow $Q_A=1$ so we get positive edge trigger
& we get $Q_B=0$

$$Q_2 Q_1 = 01$$

② On 2nd -ve clock pulse

FFA \rightarrow will toggle & we get $Q_A=0$

FFB \rightarrow $Q_A=0$ so FFB get negative edge trigger
& we get $Q_B=1$

$$Q_2 Q_1 = 10$$

③ On 3rd -ve clock pulse

FFA \rightarrow will toggle & we get $Q_A=1$

FFB \rightarrow $Q_A=1$ so FFB get tve edge trigger
& we get $Q_B=1$

$$Q_2 Q_1 = 11$$

④ On 4th -ve clock pulse

FFA \rightarrow will toggle & we get $Q_A=0$

FFB \rightarrow $Q_A=0$ so FFB get -ve edge trigger
& toggle we get $Q_B=0$

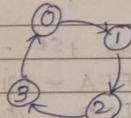
$$Q_2 Q_1 = 00$$

Step 2

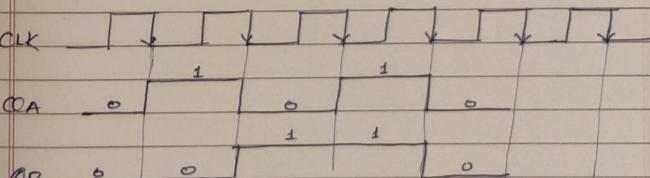
CLK Q2 Q1 state

\downarrow	0	0	0
\downarrow	0	1	
\downarrow	1	0	
\downarrow	0	1	
\downarrow	0	0	0

Step 3



Step 4

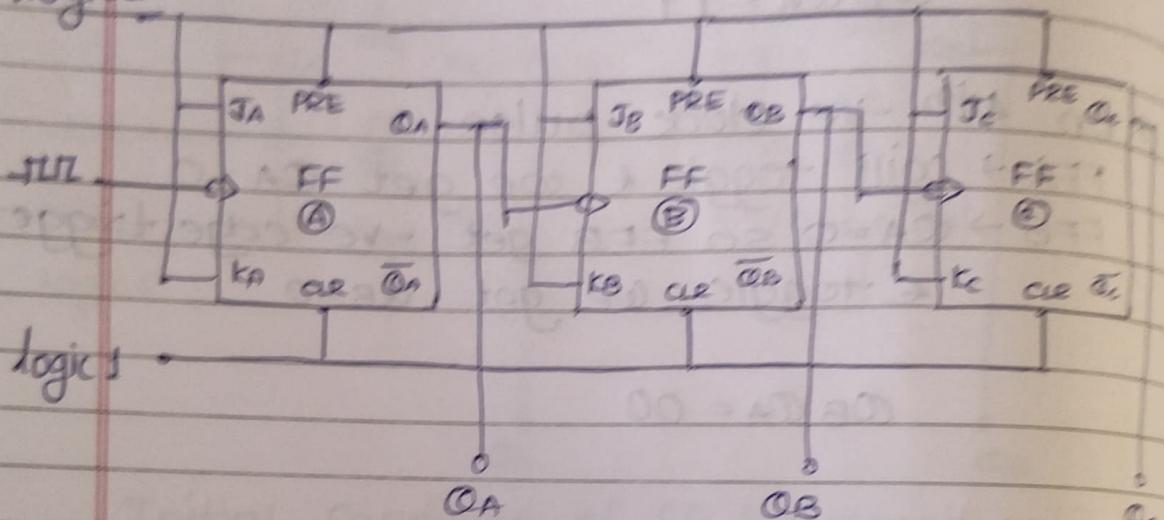


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Q Design 3 bit Asynchronous / Ripple Up Counter using JKFF

Step 1

Logic 1



Initial condition of FF be reset
 $Q_C Q_B Q_A = 000$

Q On 1st -ve clock edge

FFA - will toggle & we get $Q_A = 1$

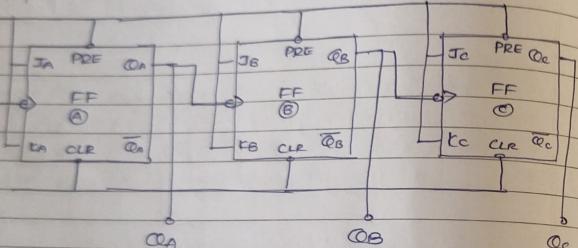
FFB - $Q_A = 1$ & we get $Q_B = 0$

FFC -

Q Design 3 bit Asynchronous/Ripple Up counter using JKFF

Step 1

logic.

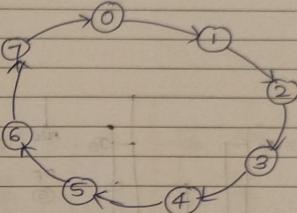


logic 1

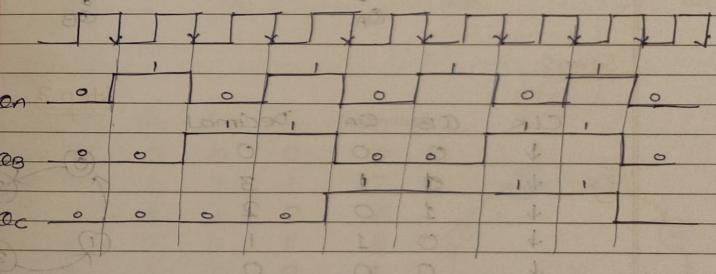
Step 3

	CLR	Q _C	Q _B	Q _A	Decimal
↓	0	0	0	0	0
↓	0	0	1	1	1
↓	0	1	0	0	2
↓	0	1	1	1	3
↓	1	0	0	0	4
↓	1	0	1	1	5
↓	1	1	0	0	6
↓	1	1	1	1	7
↓	0	0	0	0	0

Step 3

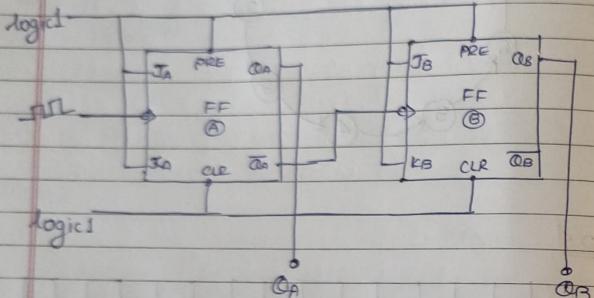


Step 4



Q Design 2 bit Asynchronous/Ripple Down Counter

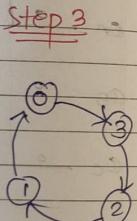
Step 1



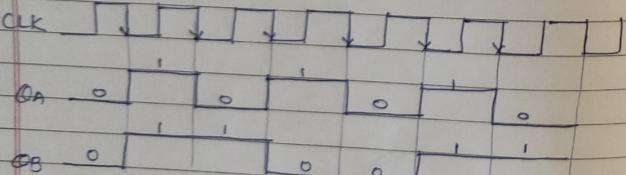
Step 2

CLK	Q _B	Q _A	Decimal
↓	0	0	0
↓	1	1	3
↓	1	0	2
↓	0	1	1
↓	0	0	0

Step 3

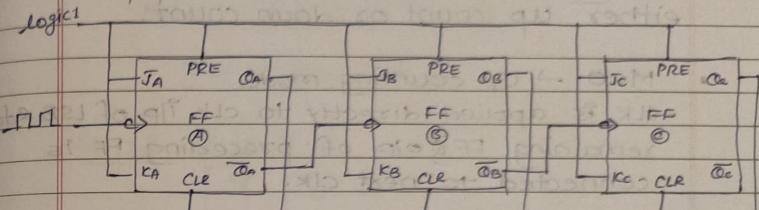


Step 4



Q Design 3 bit Asynchronous/Ripple Down Counter.

Step 1

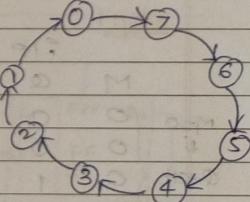


Step 2

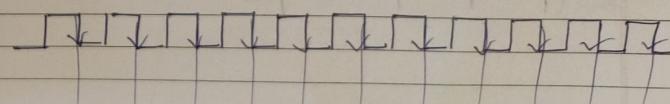
Step 2

CLK	Q _C	Q _B	Q _A	Decimal
↓	0	0	0	0
↓	1	1	1	7
↓	1	1	0	6
↓	1	0	1	5
↓	1	0	0	4
↓	0	1	1	3
↓	0	1	0	2
↓	0	0	1	1
↓	0	0	0	0

Step 3



Step 4



Design 2 bit Up/Down Asynchronous Counter

A mode control (M) I/P is used to select either up count or down count.

- M=0 → Up counting mode
 - CLK is applied directly to CLK I/P of LSB & for remaining FF Q O/P of preceding FF is connected to next CLK.
- M=1 → down counting mode
 - CLK is applied directly to CLK I/P of LSB & remaining FF \bar{Q} O/P preceding FF is connected to next CLK.

if M=0 Up counting $\rightarrow Q$ to CLK
 M=1 down counting $\rightarrow \bar{Q}$ to CLK

Step 1

		Q IP	\bar{Q} IP	Y	
M=0 ↓	0	0	0	0	
	0	0	1	1	
	0	1	0	1	
	0	1	1	1	
\bar{Q} → CLK ↓	1	0	0	0	
	1	0	1	1	
	1	1	0	0	
	1	1	1	1	

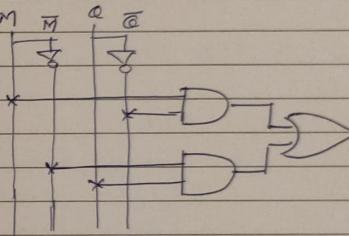
Step 2

K-Map for Y

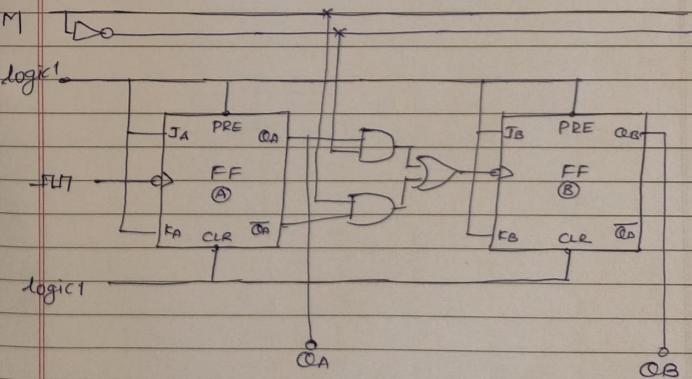
M	$\bar{Q}\bar{Q}$	$\bar{Q}Q$	$Q\bar{Q}$	QQ
M	0	1	(1 ³)	(1 ²)
M	1	(1 ⁵)	(1 ⁷)	6

$$Y = M\bar{Q} + \bar{M}Q$$

Step 3



Step 4



Q Design MOD-6 Asynchronous counter using JKFF

Step 1

No. of FF required to design MOD-6

$$N = 6$$

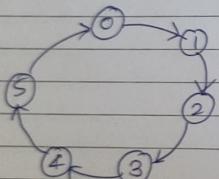
$$2^n > N$$

$$2^n > 6$$

$$n = 3$$

we need 3 flip flops.

Step 2 State diagram



Step 3

CLK	Q _C	Q _B	Q _A	O/P
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	0
7	1	1	1	0

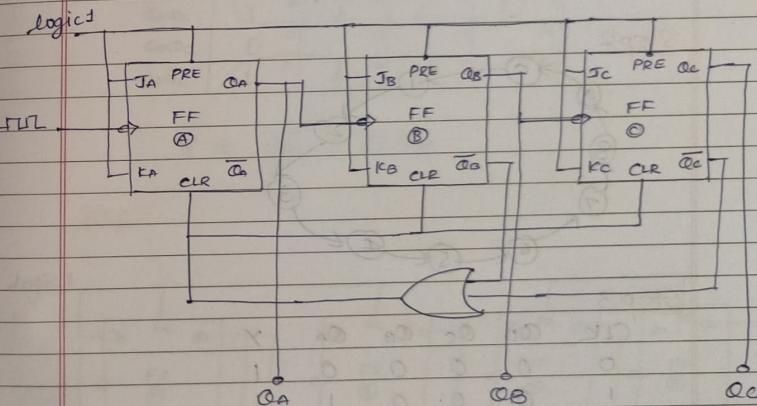
Step 4

K-Map for O/P

Q _C	Q _B	Q _A	O/P
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$$O/P = \bar{Q}_C + \bar{Q}_B$$

Step 5



Q Design MOD-10 Asynchronous Counter
Decade Counter / BCD Counter

Step 1

No. of FF required to design MOD-10

$$N = 10$$

$$2^n > N$$

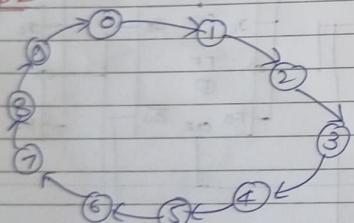
$$2^n > 10$$

$$2^4 > 10$$

$$n = 4$$

we need 4 flip flop

Step 2



Step 3

CLK	QD	QC	QB	QA	Y
0	0	0	0	0	-1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1

CLK	QD	QC	QB	QA	Y
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	0	1	0	0
15	1	0	1	1	0

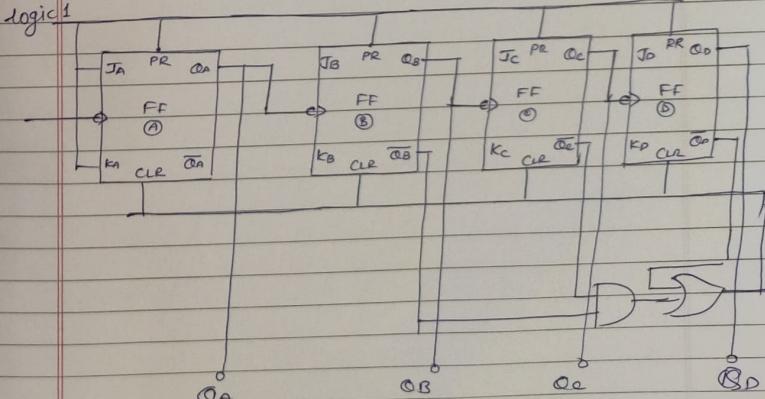
Step 4

QD QC QB QA	$\bar{Q}_D \bar{Q}_C$	$\bar{Q}_B \bar{Q}_A$	$\bar{Q}_D Q_C$	$Q_B \bar{Q}_A$	$Q_D \bar{Q}_C$	$Q_B Q_A$
1 0 0 0	1	1	1	1	1	1
1 0 0 1	1	1	1	1	1	0
0 1 0 0	0	1	1	1	0	1
0 1 0 1	0	1	1	0	0	0
0 1 1 0	0	1	0	1	0	1
0 1 1 1	0	1	0	0	0	0
1 0 0 0	1	0	1	1	1	0
1 0 0 1	1	0	1	0	1	1
1 0 1 0	1	0	0	1	0	1
1 0 1 1	1	0	0	0	0	0
1 1 0 0	0	1	1	1	0	0
1 1 0 1	0	1	1	0	0	0
1 1 1 0	0	1	0	1	0	0
1 1 1 1	0	1	0	0	0	0

$$Y = \bar{Q}_D + \bar{Q}_C \bar{Q}_B$$

Step 5

Logic:



Q Design MOD-5 Asynchronous/Ripple Down counter

counter 1 0 1 11

 0 0 1 1 11

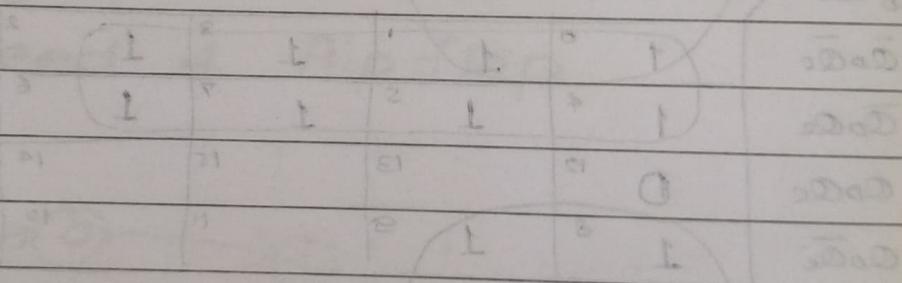
 0 0 1 1 11

 0 0 1 1 11

 0 0 1 1 11

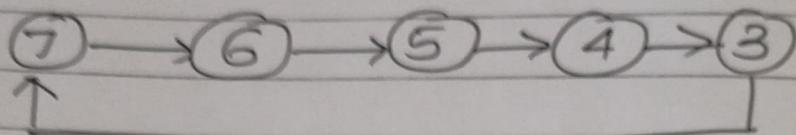
 0 0 1 1 11

நிலை ஏற்றும் வகுக்கு தகவல்



$$555 + 5 = ?$$

Q Design a ~~synchronous~~ counter for the state shown in fig.



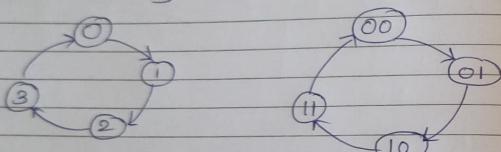
Q Design 2 bit synchronous Up Counter

Step 1

No. of flip flop required for 2 bit counter is 2 flip flop.

Step 2

state diagram



Step 3

Excitation Table of JKFF

\bar{Q}_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Truth Table

CLK	Present state		Next state		Output							
					Q_A	Q_B	Q_{AH}	Q_{BH}	JA	KA	JB	KB
0	0	0	0	1	0	X	1	X				
1	0	1	1	0	1	X	X	1				
2	1	0	1	1	X	0	1	X				
3	1	1	0	0	X	1	X	1				

Step 4

K-Map for JA

\bar{Q}_A	\bar{Q}_B	Q_B
\bar{Q}_A	X	1
Q_A	X	X

$$JA = \bar{Q}_B$$

K-Map for KA

\bar{Q}_A	\bar{Q}_B	Q_B
\bar{Q}_A	X	(X)
Q_A	X	1

$$KA = Q_B$$

K-Map for JB

\bar{Q}_A	\bar{Q}_B	Q_B
\bar{Q}_A	1	X
Q_A	1	X

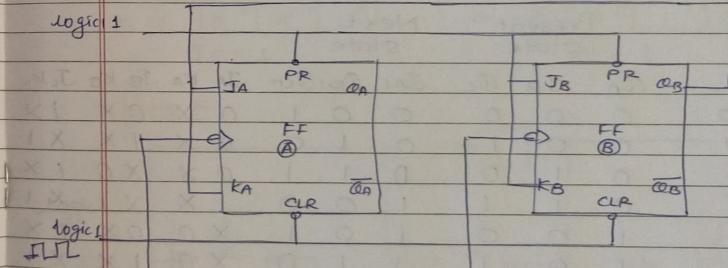
$$JB = 1$$

K-Map for KB

\bar{Q}_A	\bar{Q}_B	Q_B
\bar{Q}_A	X	1
Q_A	X	1

$$KB = 1$$

Step 5



Design 3 bit synchronous UP Counter

Step 1

No. of flip flops required to design 3 bit flip flop are 3 flip flop counter.

Step 2

$$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7$$

Step 3

Excitation table JKFF

0 0	0 x
0 1	1 x
1 0	x 1
1 1	x 0

Truth Table

Present State	Next State
---------------	------------

Q _A	Q _B	Q _C	Q _A '	Q _B '	Q _C '	J _A	K _A	J _B	K _B	J _C	K _C
0	0	0	0	0	1	0	x	0	x	1	x
1	0	0	1	0	1	0	x	1	x	x	1
2	0	1	0	0	1	1	0	x	x	0	1
3	0	1	1	1	0	0	1	x	x	0	1
4	1	0	0	1	0	0	1	x	x	1	x
5	1	0	1	1	0	1	0	x	0	x	1
6	1	1	0	1	1	1	0	x	x	0	1
7	1	1	1	0	0	0	x	1	x	x	1

Step 4

K-Map for J_A

Q _A '	Q _B '	Q _C '	Q _A	Q _B	Q _C
0	0	1	1	1	0
1	1	0	0	0	1

$$J_A = Q_B Q_C$$

K-Map for K_A

Q _A '	Q _B '	Q _C '	Q _A	Q _B	Q _C
0	0	1	x	x	1
1	1	0	1	1	0

$$K_A = Q_B Q_C$$

K-Map for J_B

Q _A '	Q _B '	Q _C '	Q _A	Q _B	Q _C
0	0	1	x	x	1
1	1	0	1	1	0

$$J_B = Q_C$$

K-Map for K_B

Q _A '	Q _B '	Q _C '	Q _A	Q _B	Q _C
0	0	1	x	x	1
1	1	0	1	1	0

$$K_B = Q_C$$

K-Map for J_C

Q _A '	Q _B '	Q _C '	Q _A	Q _B	Q _C
0	0	1	x	x	1
1	1	0	1	1	0

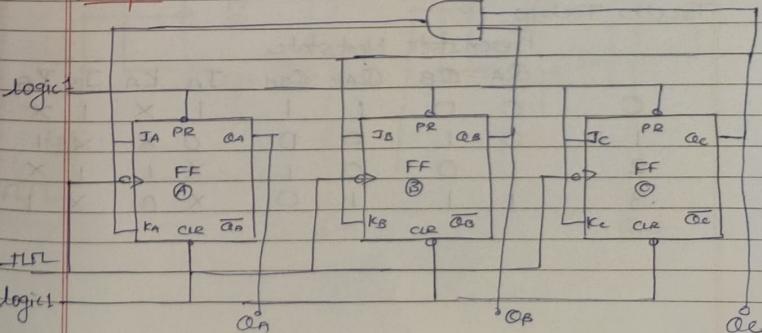
$$J_C = 1$$

K-Map for K_C

Q _A '	Q _B '	Q _C '	Q _A	Q _B	Q _C
0	0	1	x	x	1
1	1	0	1	1	0

$$K_C = 1$$

Step 5

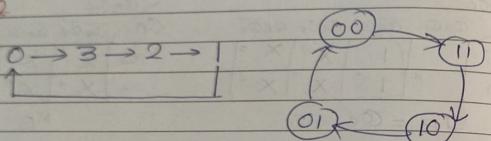


Design 2 bit synchronous down counter

Step 1

No. of flip flops required to design 2 bit counter are 2 flip flop

Step 2



Step 3

Excitation table of JKFF

J	K	\bar{Q}	\bar{Q}
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Truth Table

Present state Next state

	Q_A	Q_B	Q_{AH}	Q_{BH}	J_A	K_A	J_B	K_B
0	0	0	1	1	1	X	1	X
1	0	1	0	0	0	X	X	1
2	1	0	0	1	X	1	1	X
3	1	1	1	0	X	0	X	1

Step 4

K-Map for JA

\bar{Q}_A	Q_B	Q_B	Q_B
\bar{Q}_A	(1)	0	1
Q_A	(X)	2	X

K-Map for KA

\bar{Q}_A	Q_B	Q_B	Q_B
\bar{Q}_A	(X)	0	X
Q_A	(*)	2	0

$$JA = \bar{Q}_B$$

$$KA = \bar{Q}_B$$

K-Map for JB

\bar{Q}_A	Q_B	Q_B	Q_B
\bar{Q}_A	(1)	X	1
Q_A	1	2	X

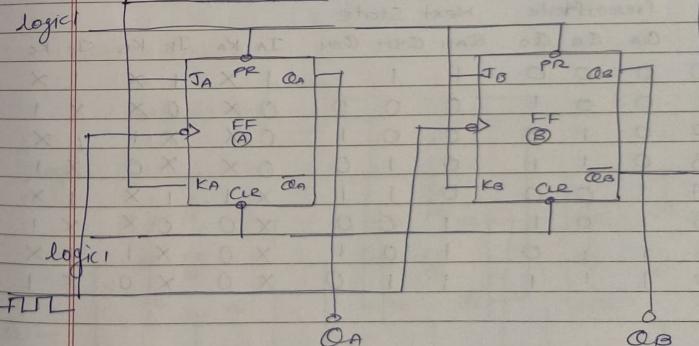
K-Map for KB

\bar{Q}_A	Q_B	Q_B	Q_B
\bar{Q}_A	X	1	1
Q_A	1	2	X

$$JB = 1$$

$$KB = 1$$

Step 5



Design 3 bit synchronous down counter using JKFF

Step 1

No. of flip flop are required to design 3 bit counters are 3 flip flop

Step 2

$$0 \rightarrow 7 \rightarrow 6 \rightarrow 5 \rightarrow 4 \rightarrow 3 \rightarrow 2 \rightarrow 1$$

Step 3 Excitation Table JKFF

0 0	0 X
0 1	1 X
1 0	X 1
1 1	X 0

Present State Next State

QA	QB	QC	QAH	QBH	QCH	JA	KA	JB	KB	Jc	Kc
0	0	0	1	1	1	1	X	1	X	1	X
1	0	0	0	0	0	0	X	0	X	X	1
2	0	1	0	0	0	0	X	X	1	X	1
3	0	1	1	0	1	0	X	X	1	1	X
4	1	0	0	0	1	1	X	0	X	X	1
5	1	0	1	1	0	X	1	1	X	1	X
6	1	1	0	1	0	X	0	0	X	X	1
7	1	1	1	1	0	X	0	X	1	1	X

Step 4

K-Map for JA

QA	QB	QC	QAH	QBH	QCH	JA
1	0	0	1	1	1	1
1	1	0	X	X	X	X

$$JA = \overline{QB} \overline{QC}$$

K-Map for KA

QA	QB	QC	QAH	QBH	QCH	KA
1	0	0	X	X	X	X
1	1	0	1	1	1	1

$$KA = \overline{QB} \overline{QC}$$

K-Map for JB

QA	QB	QC	QAH	QBH	QCH	JB
1	0	0	1	X	X	1
1	1	0	X	X	X	X

$$JB = \overline{QC}$$

K-Map for KB

QA	QB	QC	QAH	QBH	QCH	KB
1	0	0	X	X	X	1
1	1	0	X	X	X	1

$$KB = \overline{QC}$$

K-Map for JC

QA	QB	QC	QAH	QBH	QCH	Jc
1	0	0	1	X	X	1
1	1	0	X	X	X	1

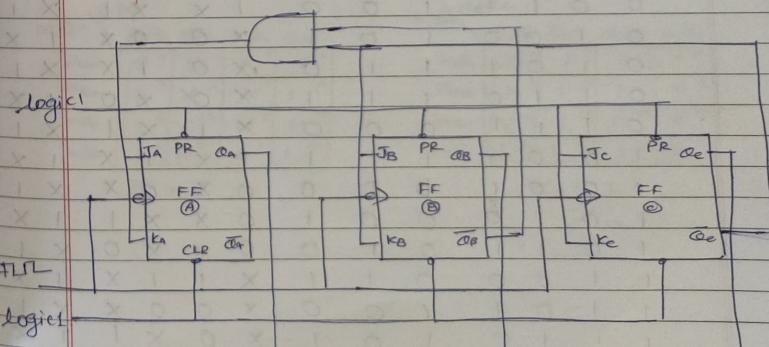
$$Jc = 1$$

K-Map for KC

QA	QB	QC	QAH	QBH	QCH	KC
1	0	1	1	1	X	1
1	1	1	X	X	X	1

$$KC = 1$$

Step 5

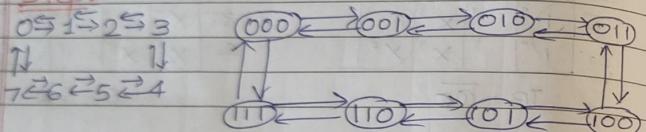


Design 3 bit synchronous Up/down counter using JKFF

Step 1

No. of flipflops required to design 3 bit up-down counter are 3 flipflop

Step 2



$M=0$ Up counting from 0 to 7

$M=1$ down counting from 7 to 0

	A_2	A_1	A_0	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	0	0	X	0	X
1	0	0	1	0	1	0	X	1	X
2	0	1	0	0	1	0	X	X	0
3	0	1	1	0	0	1	X	X	1
4	1	0	0	1	0	1	X	0	X
5	1	0	1	1	1	0	X	1	X
6	0	1	0	1	1	1	X	0	X
7	0	0	1	1	1	1	X	1	X
8	1	0	0	0	0	0	X	0	X
9	1	0	0	0	0	0	X	1	X
10	1	1	0	0	0	0	X	0	X
11	1	1	0	0	0	0	X	0	X
12	1	1	1	0	0	0	X	0	X
13	1	1	1	1	0	0	X	0	X
14	1	1	1	1	1	0	X	0	X
15	1	1	1	1	1	1	X	1	X

Step 3

K-Map for JA

$\bar{A}_2\bar{A}_1\bar{A}_0$	$\bar{A}_2\bar{A}_1A_0$	$\bar{A}_2A_1\bar{A}_0$	$A_2\bar{A}_1\bar{A}_0$
\bar{M}_{JA}	0	1	1
M_{JA}	X^4	X^5	X^7
\bar{M}_{JA}	X^{12}	X^{13}	X^{15}
M_{JA}	1	0	0

$$JA = \bar{M}_4\bar{M}_5\bar{M}_7 + \bar{M}_{12}\bar{M}_{13}\bar{M}_{15}$$

K-Map for KA

$\bar{A}_2\bar{A}_1\bar{A}_0$	$\bar{A}_2\bar{A}_1A_0$	$\bar{A}_2A_1\bar{A}_0$	$A_2\bar{A}_1\bar{A}_0$
\bar{M}_{KA}	0	1	1
M_{KA}	X^4	X^5	X^7
\bar{M}_{KA}	1	0	0
M_{KA}	X^8	X^9	X^{10}

$$KA = \bar{M}_4\bar{M}_5\bar{M}_7 + \bar{M}_8\bar{M}_9\bar{M}_{10}$$

K-Map for JB

$\bar{A}_2\bar{A}_1\bar{A}_0$	$\bar{A}_2\bar{A}_1A_0$	$\bar{A}_2A_1\bar{A}_0$	$A_2\bar{A}_1\bar{A}_0$
\bar{M}_{JB}	0	1	1
M_{JB}	0	1	1
\bar{M}_{JB}	1	0	0
M_{JB}	X^{12}	X^{13}	X^{14}

$$JB = \bar{M}_{12} + \bar{M}_{13}$$

K-Map for JB

$\bar{A}_2\bar{A}_1\bar{A}_0$	$\bar{A}_2\bar{A}_1A_0$	$\bar{A}_2A_1\bar{A}_0$	$A_2\bar{A}_1\bar{A}_0$
\bar{M}_{KB}	0	1	1
M_{KB}	X^4	X^5	X^7
\bar{M}_{KB}	X^{12}	X^{13}	X^{14}
M_{KB}	1	0	0

$$KB = \bar{M}_{12} + \bar{M}_{13}$$

K-Map for JC

$\bar{A}_2\bar{A}_1\bar{A}_0$	$\bar{A}_2\bar{A}_1A_0$	$\bar{A}_2A_1\bar{A}_0$	$A_2\bar{A}_1\bar{A}_0$
\bar{M}_{JC}	1	0	1
M_{JC}	1	0	1
\bar{M}_{JC}	1	1	0
M_{JC}	X^{12}	X^{13}	X^{14}

$$JC = 1$$

K-Map for KC

$\bar{A}_2\bar{A}_1\bar{A}_0$	$\bar{A}_2\bar{A}_1A_0$	$\bar{A}_2A_1\bar{A}_0$	$A_2\bar{A}_1\bar{A}_0$
\bar{M}_{KC}	0	1	1
M_{KC}	X^4	X^5	X^7
\bar{M}_{KC}	X^{12}	X^{13}	X^{14}
M_{KC}	1	0	0

$$KC = 1$$

Step 4

$$J_A = M_0 \bar{B} Q_0 + \bar{M}_0 B Q_0$$

$$J_B = M_0 \bar{Q}_0 + \bar{M}_0 Q_0$$

$$J_C = 1$$

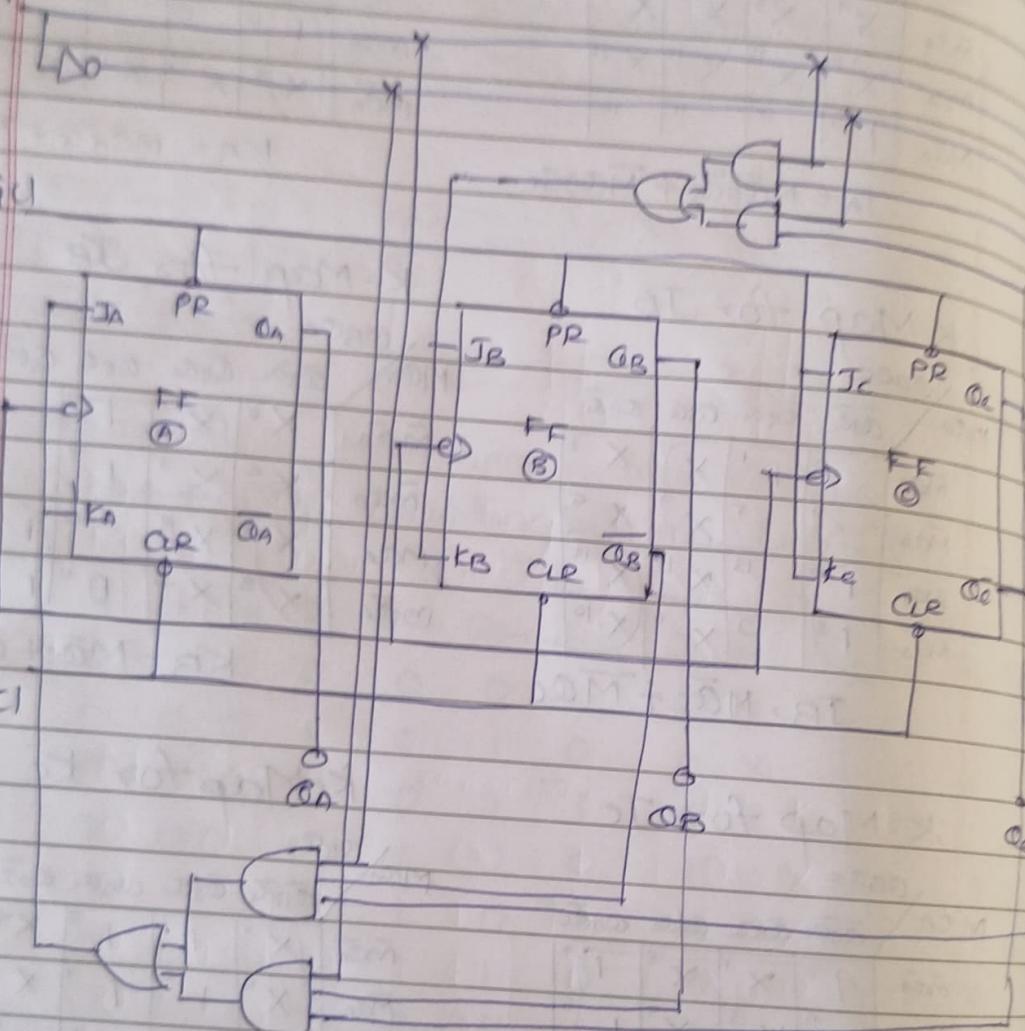
$$K_A = M_0 \bar{B} \bar{Q}_0 + \bar{M}_0 B \bar{Q}_0$$

$$K_B = M_0 \bar{Q}_0 + \bar{M}_0 Q_0$$

$$K_C = 1$$

M

logic1



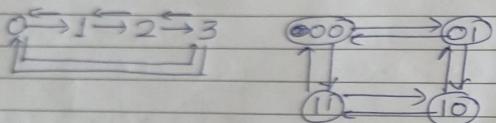
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Design 2 bit synchronous Updown counter using JKFF

Step 1

No. of flipflops required to design 2 bit updown counters are 2 flip flop

Step 2



$M = 0$ Up counting from 0 to 3

$M = 1$ down counting from 3 to 0

Step 3

000 X
011 X
10 X 1
11 X 0

M	CA	CB	CAB	CBA	JA	KA	JB	KB
0	0	0	0	1	0	X	1	X
0	0	1	1	0	1	X	X	1
0	1	0	1	1	X	0	1	X
0	1	1	0	0	X	1	X	1
1	0	0	1	1	1	X	1	X
1	0	1	0	0	0	X	X	1
1	1	0	0	1	X	1	1	X
1	1	1	1	0	X	0	X	1

Step 4

K-Map for JA

M	CA	CB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
M	1	0	1	X	1	X	1	X	1	X	1	X	1	X	1	X	1	X
M	1	1	X	1	X	1	X	1	X	X	1	X	1	X	X	1	X	1

$$JA = \overline{M}CB + M\overline{C}\overline{B}$$

K-Map for KA

M	CA	CB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
M	1	0	1	X	1	X	1	X	1	X	1	X	1	X	1	X	1	X
M	1	1	X	1	X	1	X	1	X	X	1	X	1	X	X	1	X	1

$$KA = \overline{M}CB + M\overline{C}\overline{B}$$

K-Map for JB

M	CA	CB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
M	1	0	1	X	1	X	1	X	1	X	1	X	1	X	1	X	1	X
M	1	1	X	1	X	1	X	1	X	X	1	X	1	X	X	1	X	1

$$JB = J$$

K-Map for KB

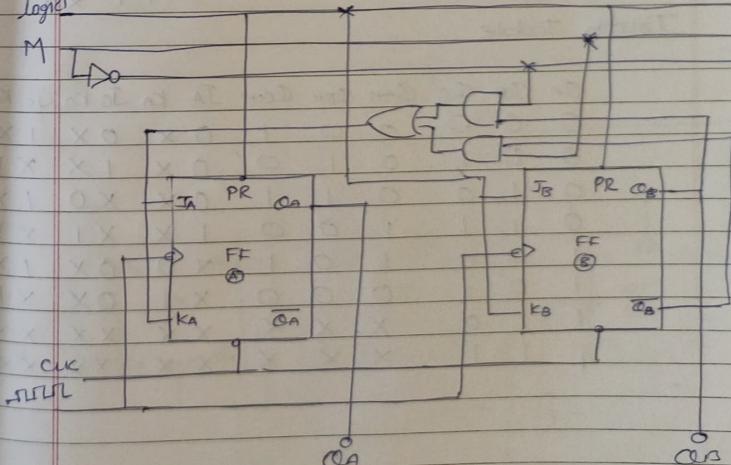
M	CA	CB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
M	1	0	1	X	1	X	1	X	1	X	1	X	1	X	1	X	1	X
M	1	1	X	1	X	1	X	1	X	X	1	X	1	X	X	1	X	1

$$KB = 1$$

Step 5

Logic

M
L
D



Design MOD-6 synchronous counter.

Step 1

No. of flip flop required to design MOD-6

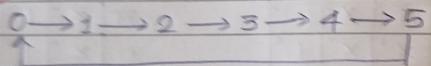
$$N = 6$$

$$2^n > 6$$

$$n = 3$$

We need 3 flip flop.

Step 2



Step 3 Excitation Table of JKFF

CA	CB	CC	CBH	CCH	JA	KA	JB	KB	Jc	Kc
0	0	0	0	0	1	0	X	0	X	1
0	0	1	0	1	0	0	X	1	X	1
0	1	0	0	1	1	0	X	X	0	1
0	1	1	1	0	0	1	X	X	1	X
1	0	0	1	0	0	1	X	X	1	X
1	0	1	0	1	0	1	X	0	X	X
1	1	0	0	0	0	X	1	0	X	X
1	1	0	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X

Truth Table

CA	CB	CC	CBH	CCH	JA	KA	JB	KB	Jc	Kc
0	0	0	0	0	1	0	X	0	X	1
0	0	1	0	1	0	0	X	1	X	1
0	1	0	0	1	1	0	X	X	0	1
0	1	1	1	0	0	1	X	X	1	X
1	0	0	1	0	0	1	X	X	1	X
1	0	1	0	1	0	1	X	0	X	X
1	1	0	0	0	X	1	0	X	X	X
1	1	0	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X

Step 4

K-Map for JA

CA	CB	CC	CBH	CCH	JA
00	0	0	0	0	1
00	1	0	0	0	X

$$JA = \overline{CB}C\bar{c}$$

K-Map for JB

CA	CB	CC	CBH	CCH	JB
00	0	0	0	0	1
00	1	0	0	0	X

$$JB = \overline{CB}C\bar{c}$$

K-Map for Jc

CA	CB	CC	CBH	CCH	Jc
00	0	0	0	0	1
00	1	0	0	0	X

$$Jc = 1$$

K-Map for KA

CA	CB	CC	CBH	CCH	KA
00	0	0	0	0	1
00	1	0	0	0	X

$$KA = \overline{CB}C\bar{c}$$

K-Map for KB

CA	CB	CC	CBH	CCH	KB
00	0	0	0	0	1
00	1	0	0	0	X

$$KB = \overline{CB}C\bar{c}$$

Step 5

