Counters

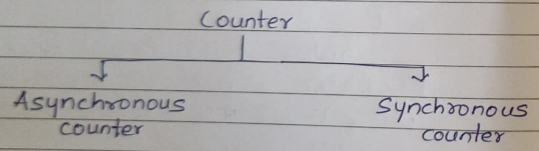
A sequential circuit used to count the clock pulses is called counter.

A flip flop can store 1 bit of information

If we want 2 bit binary counter, then it uses two flipflops.

If three bit binary output is required, the counter uses 3 flipflops.

Types of counters

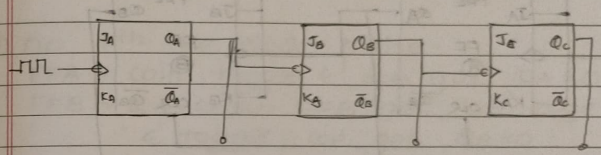


Classification of counter

1. Up- counter
2. Down- counter
3. Up/Down counter

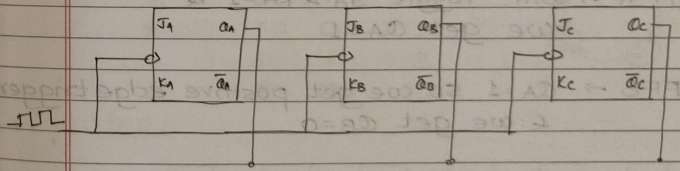
Asynchronous counter

In these external clk signal is applied to one FF and then o/p of preceding FF is connected to clk of next FF.



Synchronous Counter

In these all FF receive the external clk pulse applied simultaneously.



Up counter count from small to big

0-1-2-3-4-5-6-7-0

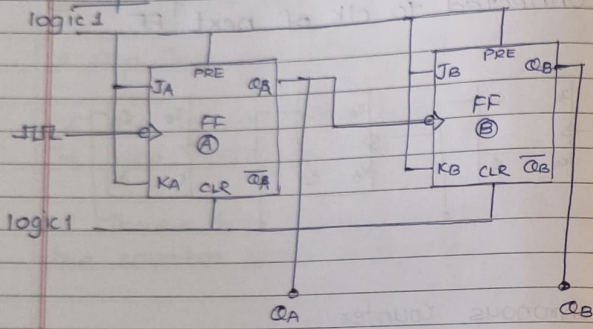
Down counter count from big to small

7-6-5-4-3-2-1-0-7

Up/Down counter is combination of Up & down Counte

Q Design 2 bit Asynchronous/Ripple counter using JKFF.

Step 1



Initial Condition of FF be reset

$Q_B Q_A = 00$

① On 1st -ve clock edge

FF A → will toggle J_A & $K_A = 1$ &

we get $Q_A = 1$

FFB → $Q_A = 1$ so we get positive edge trigger

& we get $Q_B = 0$

$Q_B Q_A = 01$

② On 2nd -ve clock pulse

FFA → will toggle & we get $Q_A = 0$

FFB → $Q_A = 0$ so FFB get negative edge trigger

& we get $Q_B = 1$

$Q_B Q_A = 10$

③ On 3rd -ve clock pulse

FFA → will toggle & we get $Q_A = 1$

FFB → $Q_A = 1$ so FFB get +ve edge trigger

& we get $Q_B = 1$

$Q_B Q_A = 11$

④ On 4th -ve clock pulse

FFA → will toggle & we get $Q_A = 0$

FFB → $Q_A = 0$ so FFB get -ve edge trigger

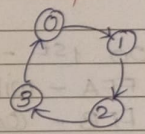
& toggle we get $Q_B = 0$

$Q_B Q_A = 00$

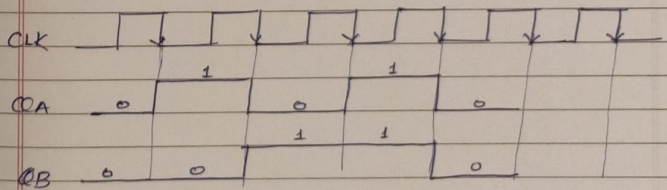
Step 2

CLK	Q_B	Q_A	state
↓	0	0	0
↓	0	1	1
↓	1	0	2
↓	1	1	3
↓	0	0	0

Step 3

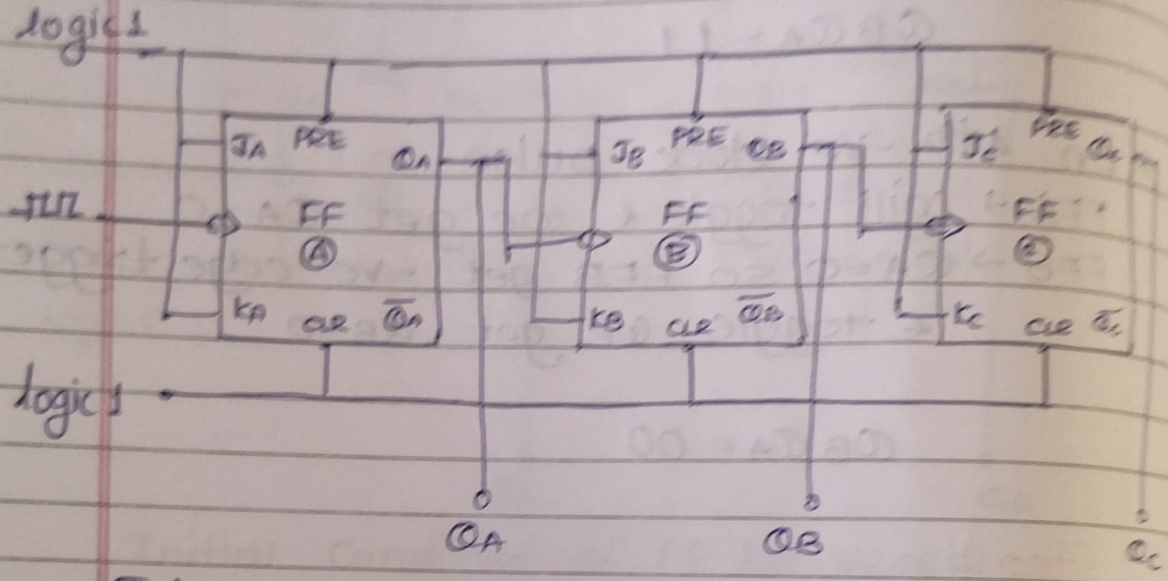


Step 4



Q Design 3 bit Asynchronous / Ripple Up counter using JKFF

Step1



Initial condition of FF be reset

$Q_C\ Q_B\ Q_A = 000$

① On 1st -ve clock edge

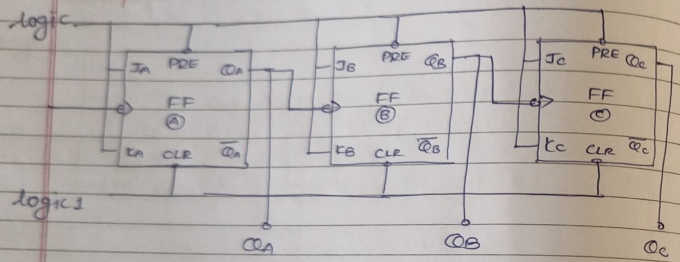
FFA - will toggle & we get $Q_A = 1$

FFB - $Q_A = 1$ & we get $Q_B = 0$

FFC -

Q Design 3 bit Asynchronous/Ripple Up counter using JKFF

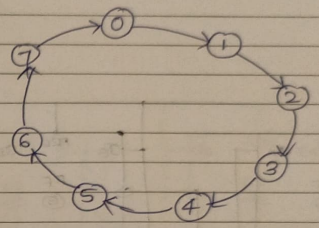
Step 1



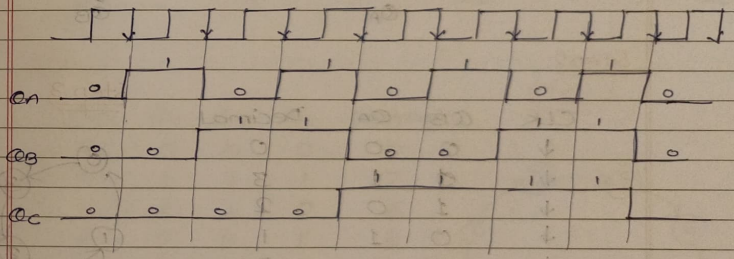
Step 2

CLR	QC	QB	QA	Decimal
↓	0	0	0	0
↓	0	0	1	1
↓	0	1	0	2
↓	0	1	1	3
↓	1	0	0	4
↓	1	0	1	5
↓	1	1	0	6
↓	1	1	1	7
↓	0	0	0	0

Step 3

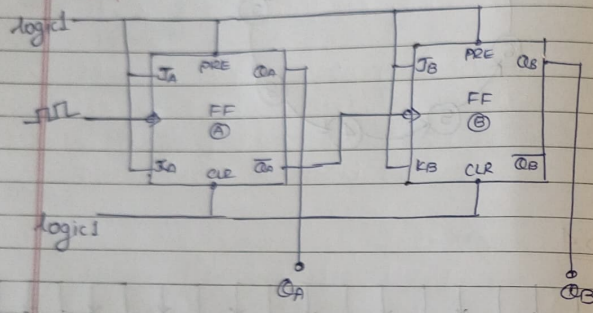


Step 4



Q. Design 2 bit Asynchronous/Ripple Down Counter

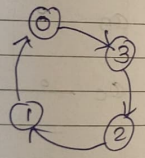
Step 1



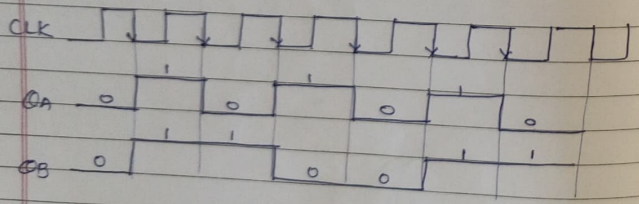
Step 2

CLK	Q_B	Q_A	Decimal
↓	0	0	0
↓	1	1	3
↓	1	0	2
↓	0	1	1
↓	0	0	0

Step 3

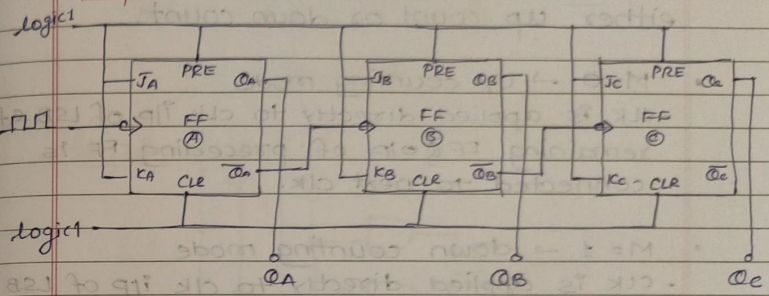


Step 4



Q. Design 3 bit Asynchronous/Ripple Down Counter.

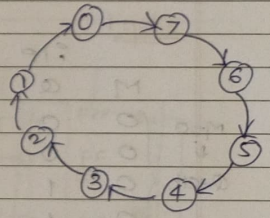
Step 1



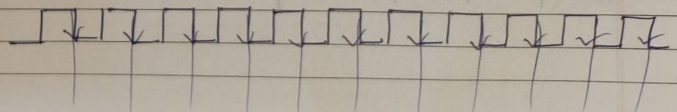
Step 2

CLK	Q_C	Q_B	Q_A	Decimal
↓	0	0	0	0
↓	1	1	1	7
↓	1	1	0	6
↓	1	0	1	5
↓	1	0	0	4
↓	0	1	1	3
↓	0	1	0	2
↓	0	0	1	1
↓	0	0	0	0

Step 3



Step 4



Design 2 bit Up/Down Asynchronous counter

A mode control (M) i/p is used to select either up count or down count.

- M=0 → Up counting mode
- clk is applied directly to clk i/p of LSB & for remaining FF Q o/p of preceding FF is connected to next clk.

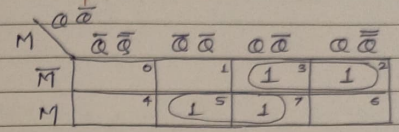
- M=1 → down counting mode
- clk is applied directly to clk i/p of LSB & remaining FF $\overline{Q}$ o/p preceding FF is connected to next clk.

if M=0 Up counting → Q to clk
M=1 down counting → $\overline{Q}$ to clk

Step 1

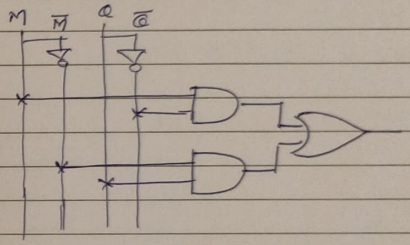
	i/p M	i/p Q	i/p $\overline{Q}$	o/p Y
M=0, Q→clk	0	0	0	0
	0	0	1	0
	0	1	0	1
	0	1	1	1
M=1, $\overline{Q}$→clk	1	0	0	0
	1	0	1	1
	1	1	0	0
	1	1	1	1

Step 2
K-Map for Y

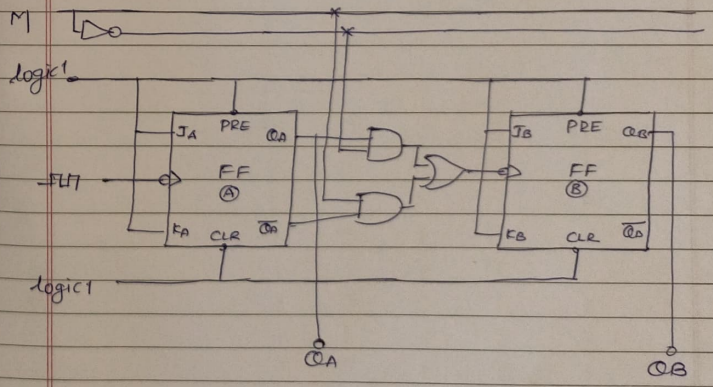


$$Y = M\overline{Q} + \overline{M}Q$$

Step 3



Step 4



Q Design MOD-6 Asynchronous counter using JKFF

Step 1

No. of FF required to design MOD-6

$N = 6$

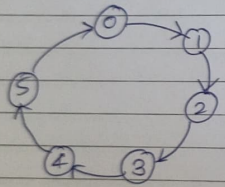
$2^n \geq N$

$2^n \geq 6$

$n = 3$

we need 3 flip flops.

Step 2 State diagram

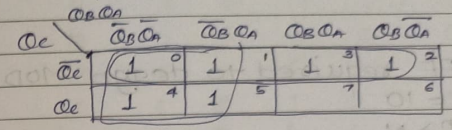


Step 3

CLK	Q_C	Q_B	Q_A	O/P
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	0
7	1	1	1	0

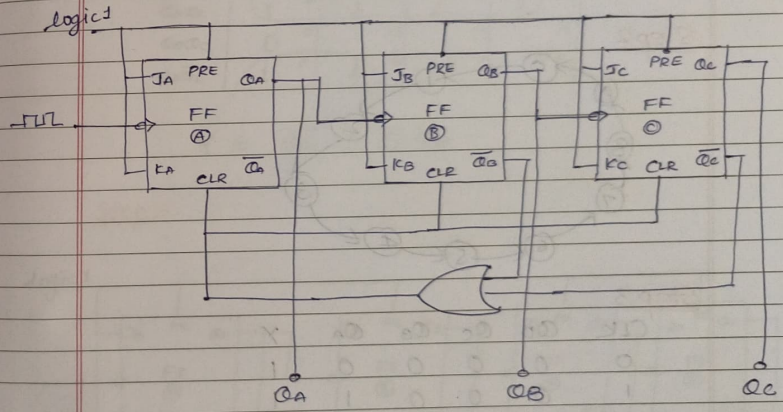
Step 4

K-Map for O/P



$O/P = \overline{Q_C} + \overline{Q_B}$

Step 5



Q. Design MOD-10 Asynchronous counter
Decade counter / BCD counter

Step1

No. of FF required to design MOD-10

$N = 10$

$2^n \geq N$

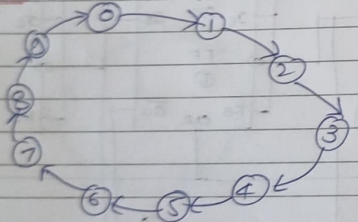
$2^n \geq 10$

$2^4 \geq 10$

$n = 4$

we need 4 flip flop

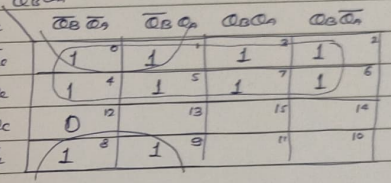
Step2



Step3

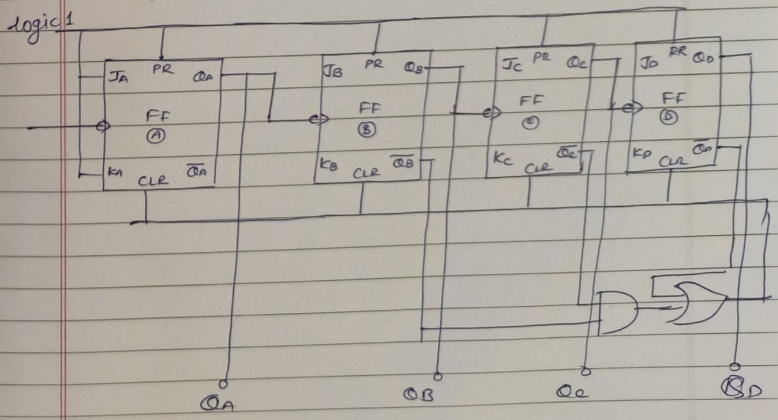
CLK	Q_D	Q_C	Q_B	Q_A	Y
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	ϕ	1	0	0
15	1	ϕ	1	1	0

Step4



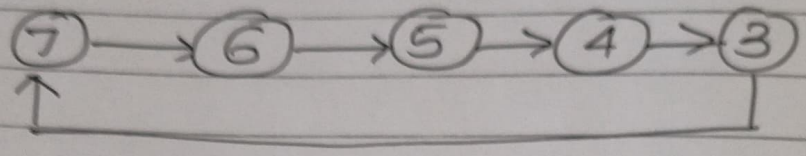
$$Y = \overline{Q_D} + \overline{Q_C}\,\overline{Q_B}$$

Step5



Q Design MOD-5 Asynchronous/Ripple Down counter

Q Design a ripple counter for the state shown in fig.



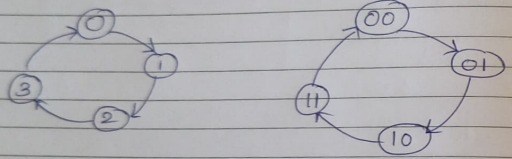
Q Design 2 bit synchronous Up Counter

Step 1

No. of filpflop required for 2 bit counter is 2 flip flop.

Step 2

State diagram



Step 3

Excitation Table of JKFF

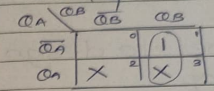
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Truth Table

	Present state		Next state		O/P			
CLK	Q_A	Q_B	Q_{AH}	Q_{BH}	J_A	K_A	J_B	K_B
0	0	0	0	1	0	X	1	X
1	0	1	1	0	1	X	X	1
2	1	0	1	1	X	0	1	X
3	1	1	0	0	X	1	X	1

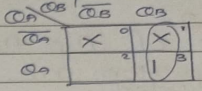
Step 4

K-Map for J_A



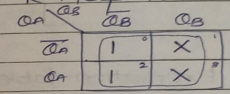
$J_A = Q_B$

K-Map for K_A



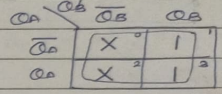
$K_A = Q_B$

K-Map for J_B



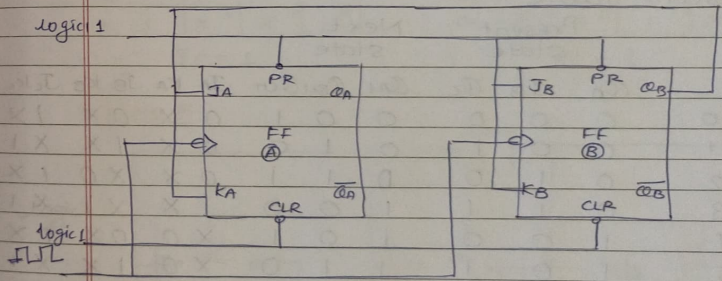
$J_B = 1$

K-Map for K_B



$K_B = 1$

Step 5



7

Design 3 bit synchronous up counter

Step 1

No. of flip flops requires to design 3 bit ~~flip flop~~ counter are 3 flip flop.

Step 2

$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6 \rightarrow 7$ (cyclic)

Step 3

Excitation table JKFF

0 0	0 x
0 1	1 x
1 0	x 1
1 1	x 0

Truth Table

	Present state			Next state								
	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	X	1
2	0	1	0	0	1	1	0	X	X	0	1	X
3	0	1	1	1	0	0	1	X	X	1	X	1
4	1	0	0	1	0	1	X	0	0	X	1	X
5	1	0	1	1	1	0	X	0	1	X	X	1
6	1	1	0	1	1	1	X	0	X	0	1	X
7	1	1	1	0	0	0	X	1	X	1	X	1

Step 4

K-Map for J_A

Q_A \ $Q_B Q_C$	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_B Q_C$	$Q_B Q_C$	$Q_B\bar{Q}_C$
$\bar{Q}_A$	0	1	3	2
Q_A	X 4	X 5	X 7	X 6

$J_A = Q_B Q_C$

K-Map for K_A

Q_A \ $Q_B Q_C$	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_B Q_C$	$Q_B Q_C$	$Q_B\bar{Q}_C$
$\bar{Q}_A$	X 0	X 1	X 3	X 2
Q_A	4	5	1 7	6

$K_A = Q_B Q_C$

K-Map for J_B

Q_A \ $Q_B Q_C$	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_B Q_C$	$Q_B Q_C$	$Q_B\bar{Q}_C$
$\bar{Q}_A$	0	1 1	X 3	X 2
Q_A	4	1 5	X 7	X 6

$J_B = Q_C$

K-Map for K_B

Q_A \ $Q_B Q_C$	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_B Q_C$	$Q_B Q_C$	$Q_B\bar{Q}_C$
$\bar{Q}_A$	X 1	X 2	1 3	2
Q_A	X 4	X 5	1 7	6

$K_B = Q_C$

K-Map for J_C

Q_A \ $Q_B Q_C$	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_B Q_C$	$Q_B Q_C$	$Q_B\bar{Q}_C$
$\bar{Q}_A$	1 0	X 1	X 3	1 2
Q_A	1 4	X 5	X 7	1 6

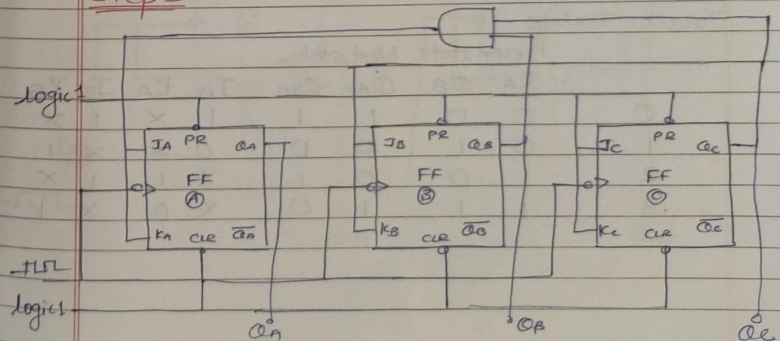
$J_C = 1$

K-Map for K_C

Q_A \ $Q_B Q_C$	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_B Q_C$	$Q_B Q_C$	$Q_B\bar{Q}_C$
$\bar{Q}_A$	X 0	1 1	1 3	X 2
Q_A	X 4	1 5	1 7	X 6

$K_C = 1$

Step 5

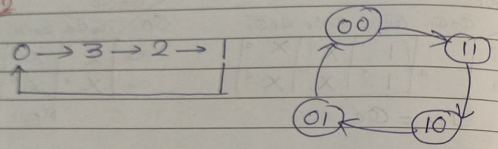


Design 2 bit synchronous down counter

Step 1

No. of flip flops required to design 2 bit counter are 2 flip flop

Step 2



Step 3

Excitation table of JKFF

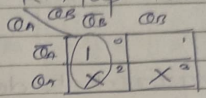
J	K	Q	$\overline{Q}$
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Truth Table

	Present state		Next state					
	Q_A	Q_B	Q_{A+1}	Q_{B+1}	J_A	K_A	J_B	K_B
0	0	0	1	1	1	X	1	X
1	0	1	0	0	0	X	X	1
2	1	0	0	1	X	1	1	X
3	1	1	1	0	X	0	X	1

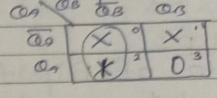
Step 4

K-Map for J_A



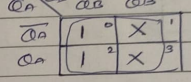
$J_A = \overline{Q_B}$

K-Map for K_A



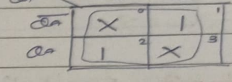
$K_A = \overline{Q_B}$

K-Map for J_B



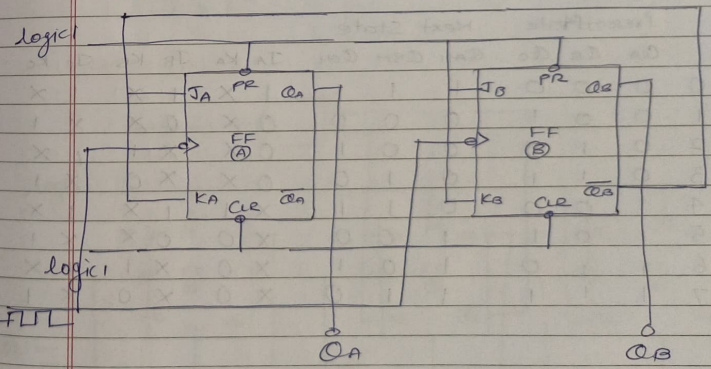
$J_B = 1$

K-Map for K_B



$K_B = 1$

Step 5

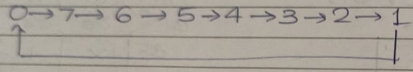


Design 3bit synchronous down counter using JKFF

Step 1

No. of flip flop are required to design 3 bit counters are 3 flip flop

Step 2



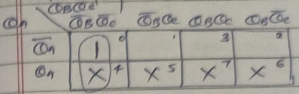
Step 3 Excitation Table JKFF

0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

	Present State			Next State								
	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	1	1	1	1	X	1	X	1	X
1	0	0	1	0	0	0	0	X	0	X	X	1
2	0	1	0	0	0	1	0	X	X	1	1	X
3	0	1	1	0	1	0	0	X	X	0	X	1
4	1	0	0	0	1	1	X	1	1	X	1	X
5	1	0	1	1	0	0	X	0	0	X	X	1
6	1	1	0	1	0	1	X	0	X	1	1	X
7	1	1	1	1	1	0	X	0	X	0	X	1

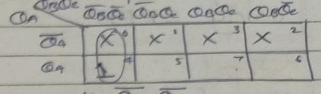
Step 4

K-Map for J_A



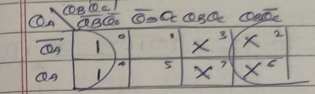
$J_A = \bar{Q}_B\bar{Q}_C$

K-Map for K_A



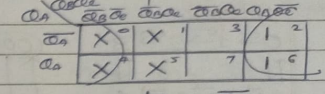
$K_A = \bar{Q}_B\bar{Q}_C$

K-Map for J_B



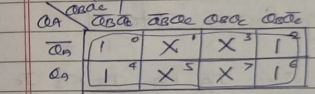
$J_B = \bar{Q}_C$

K-Map for K_B



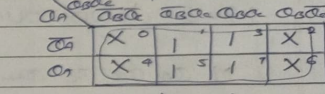
$K_B = \bar{Q}_C$

K-Map for J_C



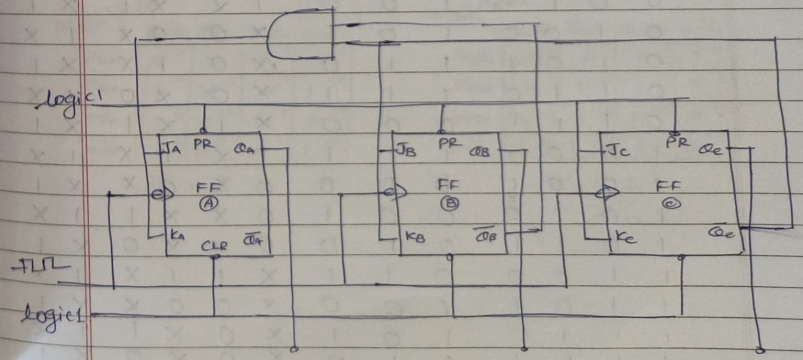
$J_C = 1$

K-Map for K_C



$K_C = 1$

Step 5

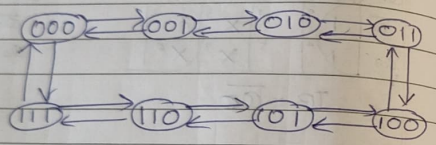


Design 3 bit Synchronous Up/down counter using JKFF

Step1

No. of flipflops required to design 3bit up-down counter are 3 flipflop

Step2

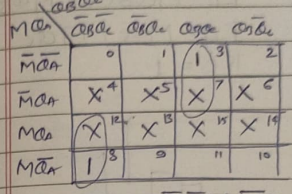


M=0 Up counting from 0 to 7
M=1 down counting from 7 to 0

M	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	0	1	0	1	0	0	X	1	X	X	1
0	0	1	0	0	1	1	0	X	X	0	1	X
0	0	1	1	1	0	0	1	X	X	1	X	1
0	1	0	0	1	0	1	X	0	0	X	1	X
0	1	0	1	1	1	0	X	0	1	X	X	1
0	1	1	0	1	1	1	X	0	X	0	1	X
0	1	1	1	0	0	0	X	1	X	1	X	1
1	0	0	0	1	1	1	1	X	1	X	1	X
1	0	0	1	0	0	0	0	X	0	X	X	1
1	0	1	0	0	0	1	0	X	X	1	1	X
1	0	1	1	0	1	0	0	X	X	0	X	1
1	1	0	0	0	1	1	X	1	1	X	1	X
1	1	0	1	0	0	0	X	1	0	X	X	1
1	1	1	0	1	0	1	X	0	X	1	1	X
1	1	1	1	1	1	0	X	0	X	0	X	1

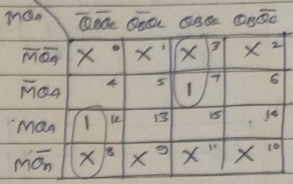
Step3

K-Map for J_A



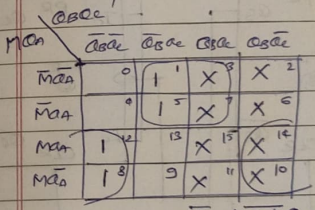
$J_A = M\bar{Q}_B\bar{Q}_C + \bar{M}Q_BQ_C$

K-Map for K_A



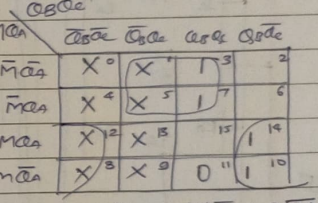
$K_A = M\bar{Q}_B\bar{Q}_C + \bar{M}Q_BQ_C$

K-Map for J_B



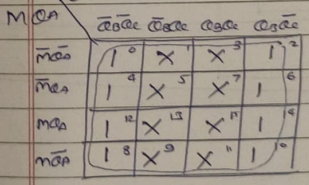
$J_B = M\bar{Q}_C + \bar{M}Q_C$

K-Map for J_B



$K_B = M\bar{Q}_C + Q_C\bar{M}$

K-Map for J_C



$J_C = 1$

K-Map for K_C

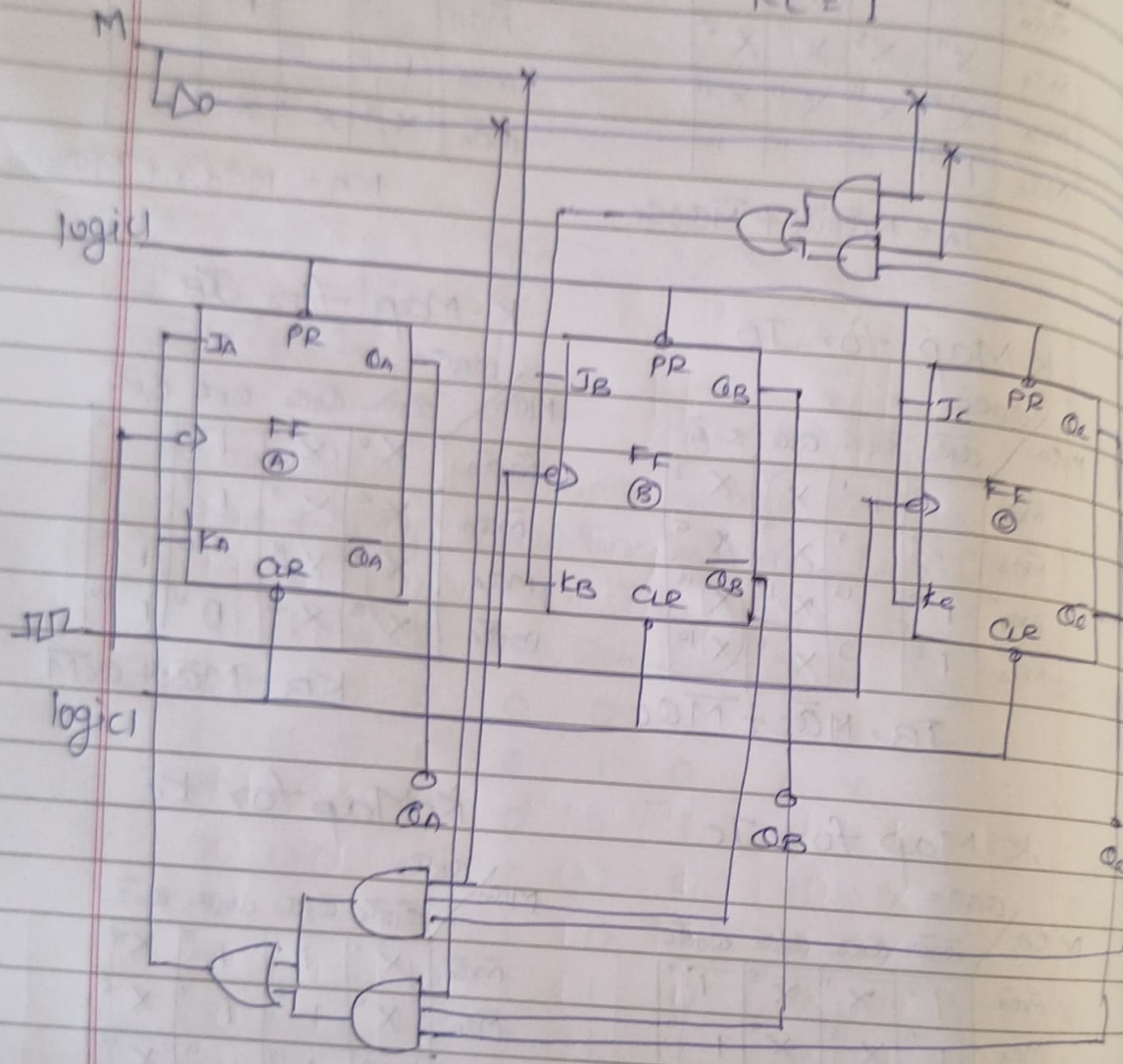
$K_C = 1$

Step 4

$J_A = M\bar{Q}_B\bar{Q}_C + \bar{M}Q_BQ_C$ $K_A = M\bar{Q}_BQ_C + \bar{M}Q_BQ_C$

$J_B = M\bar{Q}_C + \bar{M}Q_C$ $K_B = M\bar{Q}_C + \bar{M}Q_C$

$J_C = 1$ $K_C = 1$

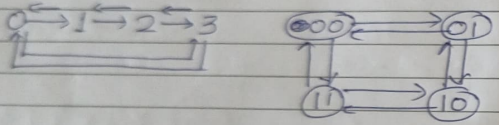


Design 2 bit synchronous Updown counter using JKFF

Step1

No. of flipflops required to design 2 bit updown counters are 2 flipflop

Step2



M=0 Up counting from 0 to 3
M=1 down counting from 3 to 0

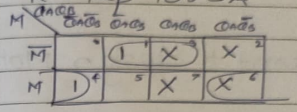
Step3

00	0X
01	1X
10	X1
11	X0

M	Q_A	Q_B	Q_{A+1}	Q_{B+1}	J_A	K_A	J_B	K_B
0	0	0	0	1	0	X	1	X
0	0	1	1	0	1	X	X	1
0	1	0	1	1	X	0	1	X
0	1	1	0	0	X	1	X	1
1	0	0	1	1	1	X	1	X
1	0	1	0	0	0	X	X	1
1	1	0	0	1	X	1	1	X
1	1	1	1	0	X	0	X	1

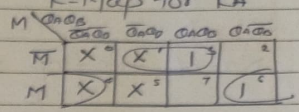
Step 4

K-Map for J_A



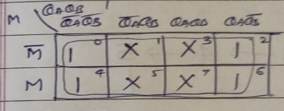
$J_A = \overline{M}Q_B + M\overline{Q_B}$

K-Map for K_A



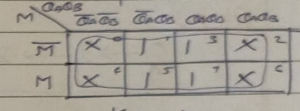
$K_A = \overline{M}Q_B + M\overline{Q_B}$

K-Map for J_B



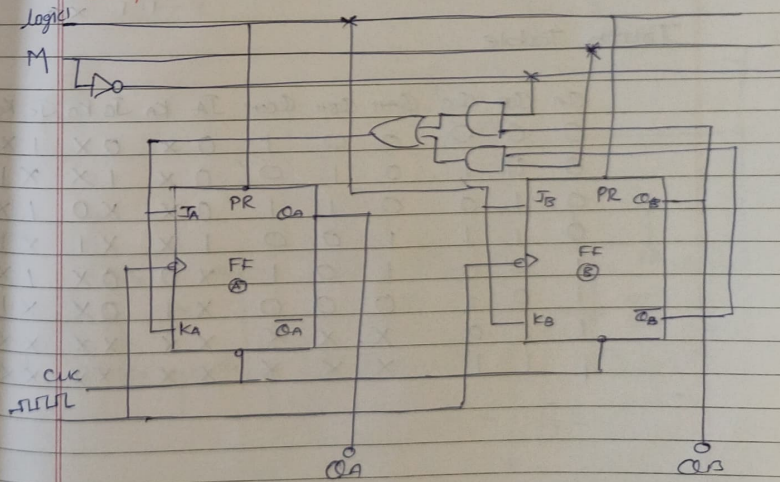
$J_B = 1$

K-Map for K_B



$K_B = 1$

Step5



Design MOD-6 synchronous counter.

Step 1

No. of flip flop required to design MOD-6

$N = 6$

$2^n \geq 6$

$n = 3$

We need 3 flip flop.

Step 2

$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5$ (with a feedback arrow from 5 back to 0)

Step 3 Excitation Table of JKFF

0 0	0 X
0 1	1 X
1 0	X 1
1 1	X 0

Truth Table

Q_A	Q_B	Q_C	Q_{An+1}	Q_{Bn+1}	Q_{Cn+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

Step 4

K-Map for J_A

Q_A \ $Q_B Q_C$	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_B Q_C$	$Q_B Q_C$	$Q_B\bar{Q}_C$
$\bar{Q}_A$	0	1	3	2
Q_A	X 4	X 5	X 7	X 6

$J_A = Q_B Q_C$

K-Map for K_A

Q_A \ $Q_B Q_C$	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_B Q_C$	$Q_B Q_C$	$Q_B\bar{Q}_C$
$\bar{Q}_A$	X 0	X 1	X 3	X 2
Q_A	4	1 5	X 7	X 6

$K_A = Q_C$

K-Map for J_B

Q_A \ $Q_B Q_C$	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_B Q_C$	$Q_B Q_C$	$Q_B\bar{Q}_C$
$\bar{Q}_A$	0	1 1	X 3	X 2
Q_A	4	5	X 7	X 6

$J_B = Q_A Q_C$

K-Map for K_B

Q_A \ $Q_B Q_C$	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_B Q_C$	$Q_B Q_C$	$Q_B\bar{Q}_C$
$\bar{Q}_A$	0	1	1 3	2
Q_A	X 4	X 5	X 7	X 6

$K_B = Q_B Q_C$

K-Map for J_C

Q_A \ $Q_B Q_C$	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_B Q_C$	$Q_B Q_C$	$Q_B\bar{Q}_C$
$\bar{Q}_A$	1 0	X 1	X 3	1 2
Q_A	1 4	X 5	X 7	X 6

$J_C = 1$

K-Map for J_C

Q_A \ $Q_B Q_C$	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_B Q_C$	$Q_B Q_C$	$Q_B\bar{Q}_C$
$\bar{Q}_A$	X 0	1 1	1 3	X 2
Q_A	X 4	1 5	X 7	X 6

$K_C = 1$

Step 5