Programmable Logic Devices

A programmable logic device is an integrated circuit capable of implementing logic functions.

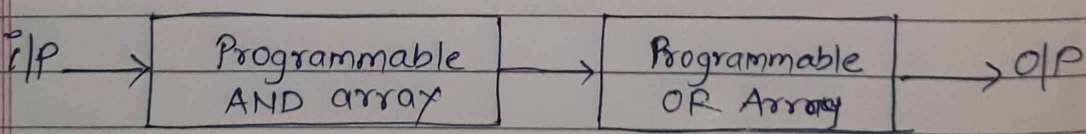
The main advantage of PLD is that they can replace a number of circuits in many applications.

Classification of PLD's

1. Programmable Logic Array (PLA)
2. Programmable Array Logic (PAL)
3. Programmable Read Only Memory (PROM)

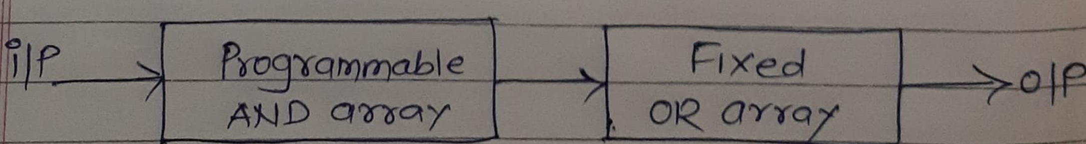
Programmable Logic Array (PLA)

PLA is a logic device with both AND and OR arrays programmable.



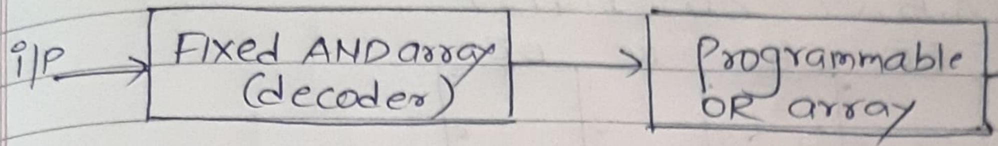
Programmable Array Logic (PAL)

PAL is a logic device with programmable AND array & a fixed OR array.

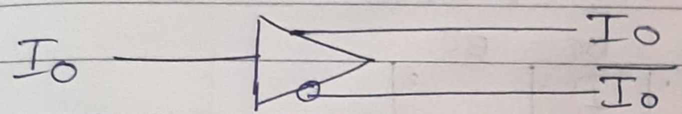


Programmable Read Only Memory (PROM)

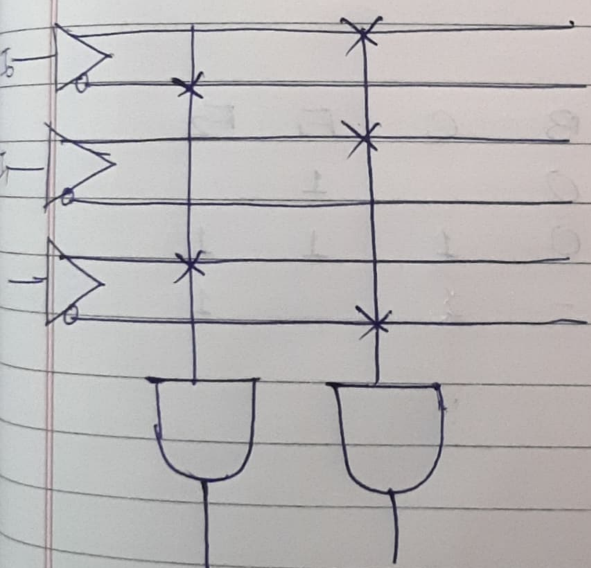
It has a fixed AND array that is constructed as a decoder and a programmable OR array.



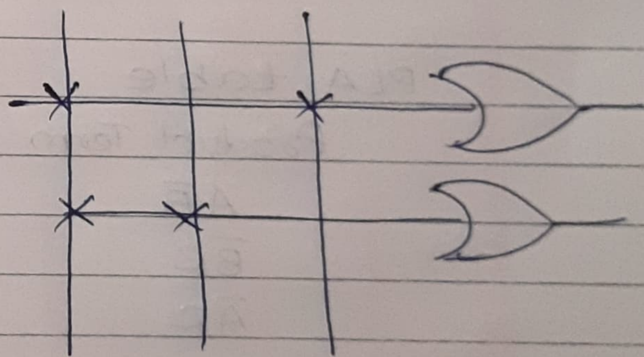
Input buffer



AND matrix



OR matrix



Programmable Logic Array (PLA)

A combinational circuit is defined by function

$F_1(A,B,C) = \sum m(1,4,5)$

$F_2(A,B,C) = \sum m(1,3,5)$

Implement circuit with PLA.

$F_1(A,B,C) = \sum m(1,4,5)$

$A \backslash BC$	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$		1		
A	1	1		

$F_1 = A\bar{B} + \bar{B}C$

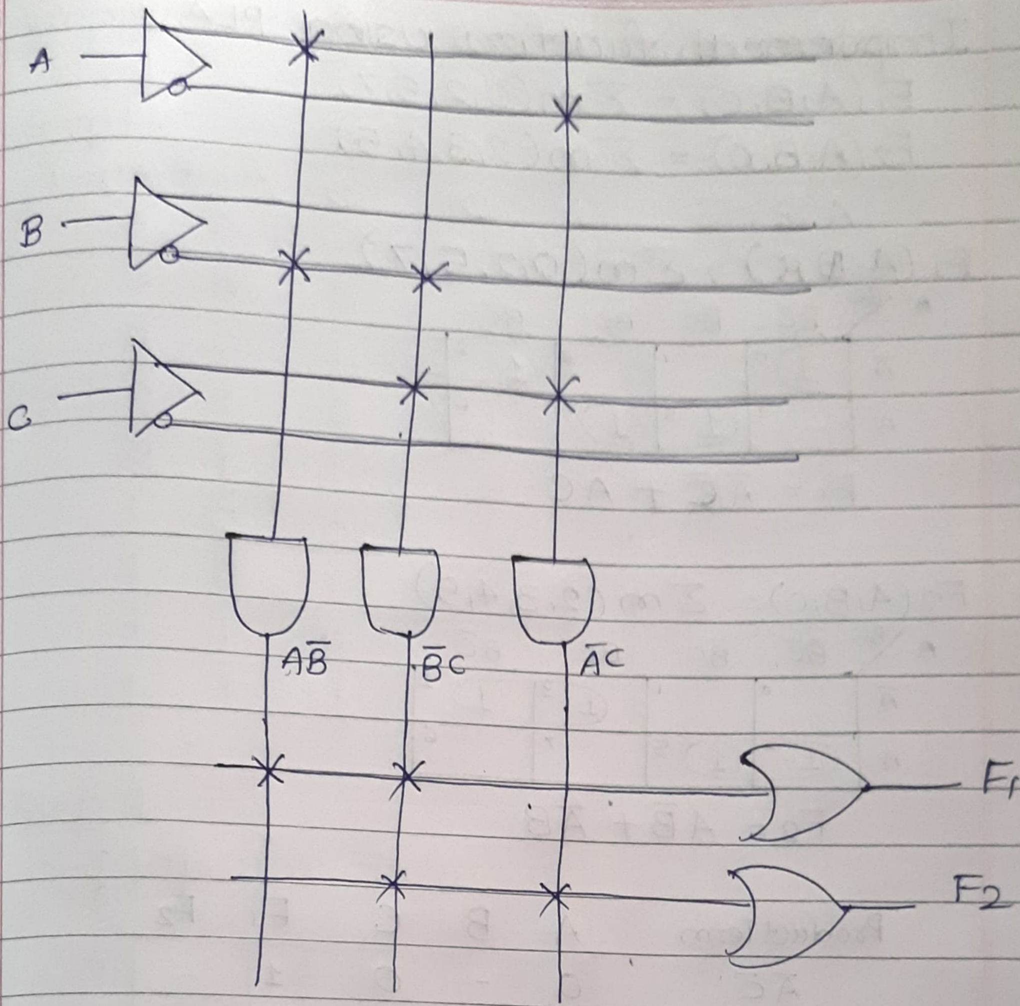
$F_2(A,B,C) = \sum m(1,3,5)$

$A \backslash BC$	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$		1	1	
A		1		

$F_2 = \bar{B}C + \bar{A}C$

PLA table

Product Term	A	B	C	F_1	F_2
$A\bar{B}$	1	0		1	
$\bar{B}C$	-	0	1	1	1
$\bar{A}C$	0	-	1		1


A
B
C
$A\bar{B}$
$\bar{B}C$
$\bar{A}C$
F_1
F_2

Implement function using PLA

$F_1(A,B,C) = \sum m(0,2,5,7)$

$F_2(A,B,C) = \sum m(2,3,4,5)$

$F_1(A,B,C) = \sum m(0,2,5,7)$

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1 (0)	(1)	(3)	1 (2)
A	(4)	1 (5)	1 (7)	(6)

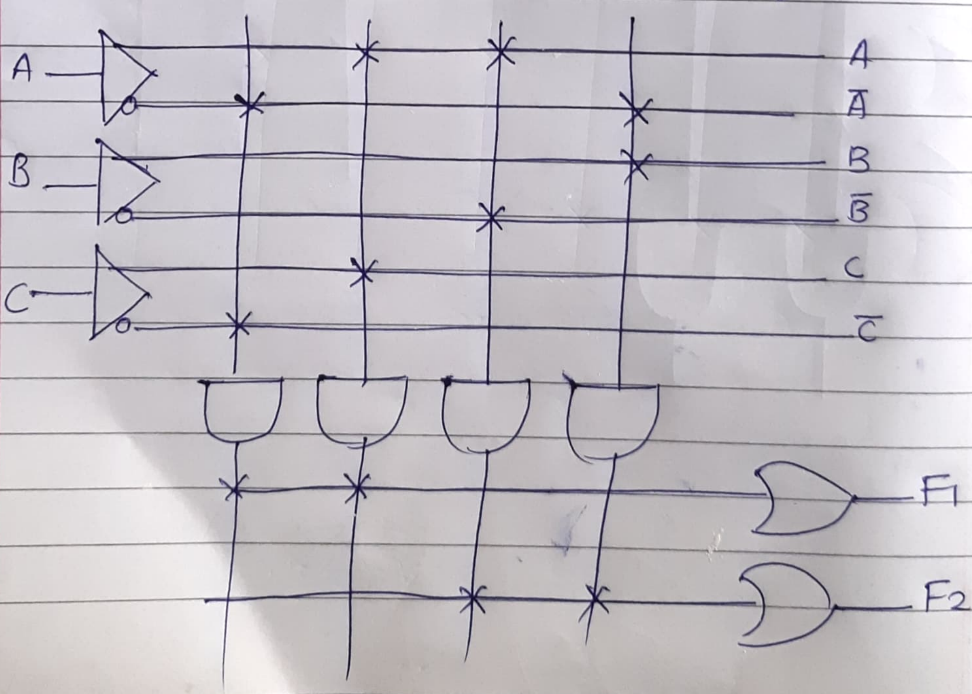
$F_1 = \bar{A}\cancel{B}\bar{C} + AC$

$F_2(A,B,C) = \sum m(2,3,4,5)$

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	(0)	(1)	1 (3)	1 (2)
A	1 (4)	1 (5)	(7)	(6)

$F_2 = A\bar{B} + \bar{A}B$

Product Term	A	B	C	F_1	F_2
$\bar{A}\bar{C}$	0	-	0	1	
AC	1	-	1	1	
$A\bar{B}$	1	0	-		1
$\bar{A}B$	0	1	-		1



Implement full Adder using PLA

Step 1

Truth Table

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Step 2

K-Map for Sum

A \ BC_{in}	$\bar{B}\bar{C}_{in}$	$\bar{B}C_{in}$	BC_{in}	$B\bar{C}_{in}$
$\bar{A}$	(0)	1 (1)	(3)	1 (2)
A	1 (4)	(5)	1 (7)	(6)

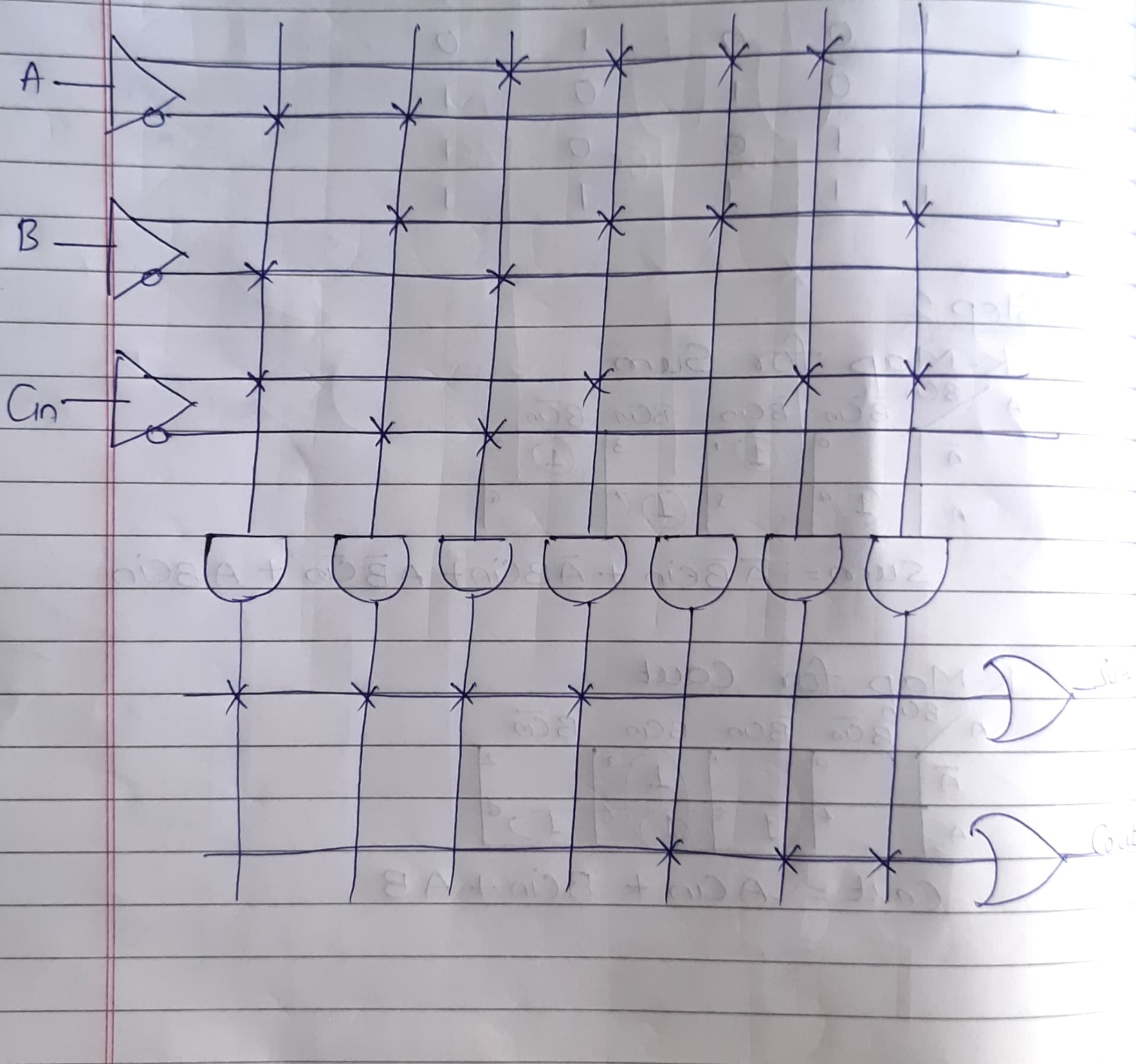
$$Sum = \bar{A}\bar{B}C_{in} + \bar{A}BC_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$$

K-Map for Cout

A \ BC_{in}	$\bar{B}\bar{C}_{in}$	$\bar{B}C_{in}$	BC_{in}	$B\bar{C}_{in}$
$\bar{A}$	(0)	(1)	1 (3)	(2)
A	(4)	1 (5)	1 (7)	1 (6)

$$C_{out} = AC_{in} + BC_{in} + AB$$

Product Term	A	B	Cin	Sum	Cout
$\bar{A}\bar{B}C_{in}$	0	0	1	1	-
$\bar{A}B\bar{C}_{in}$	0	1	0	1	-
$A\bar{B}\bar{C}_{in}$	1	0	0	1	-
ABC_{in}	1	1	1	1	-
AB	1	1	-	-	1
AC_{in}	1	-	1	-	1
BC_{in}	-	1	1	-	1



Implement following function using PLA

$F_1(A,B,C,D) = \sum m(3,7,8,9,11,15)$

$F_2(A,B,C,D) = \sum m(3,4,5,7,10,14,15)$

Step1

K-Map for F_1

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	1 (3)	2
$\bar{A}B$	4	5	1 (7)	6
AB	12	13	1 (15)	14
$A\bar{B}$	1 (8)	1 (9)	1 (11)	10

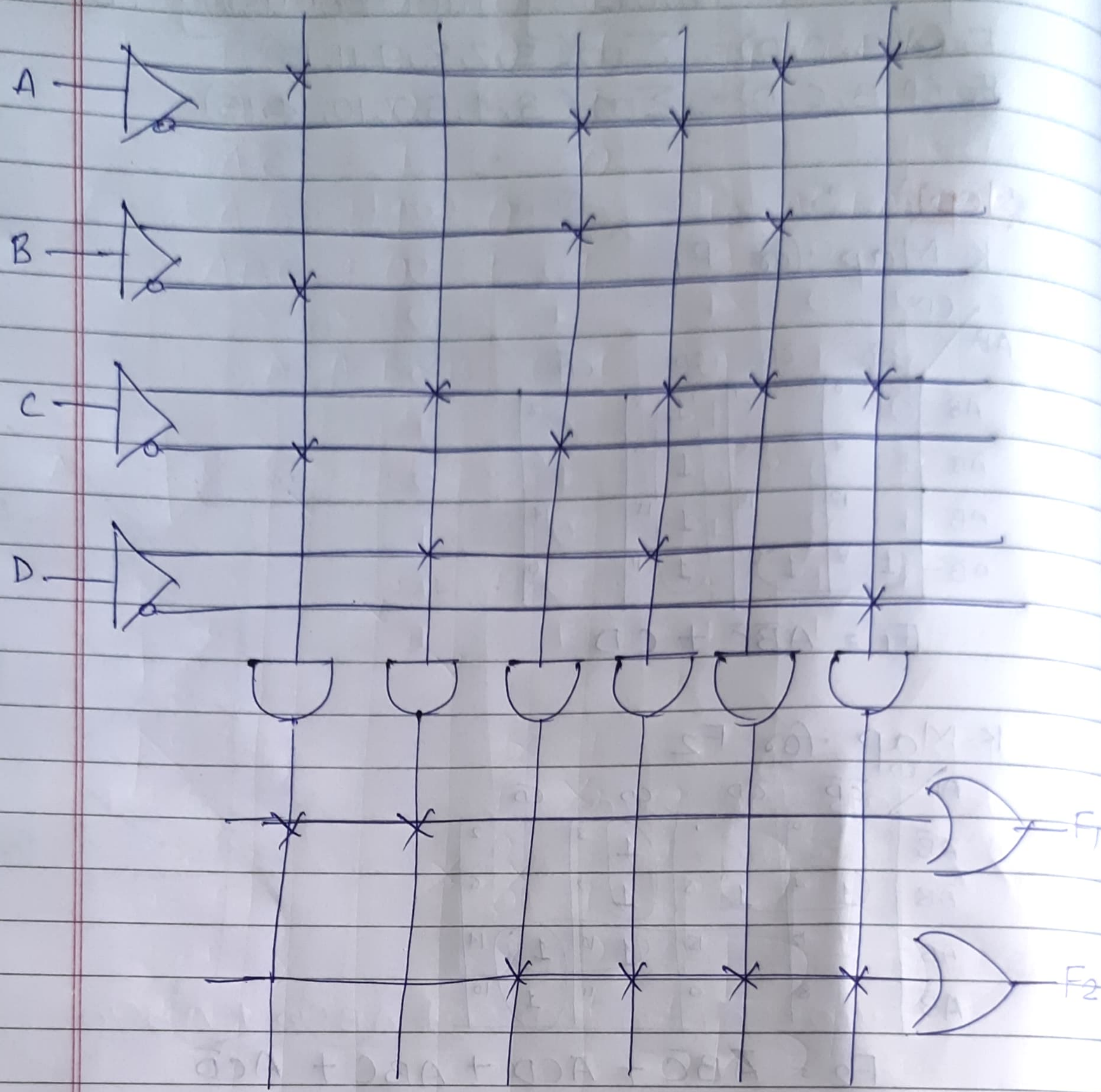
$F_1 = A\bar{B}\bar{C} + CD$

K-Map for F_2

$AB \backslash CD$	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	1 (3)	2
$\bar{A}B$	1 (4)	1 (5)	1 (7)	6
AB	12	13	1 (15)	1 (14)
$A\bar{B}$	8	9	11	1 (10)

$F_2 = \bar{A}B\bar{C} + \bar{A}CD + ABC + AC\bar{D}$

Product Term	A	B	C	D	F_1	F_2
$A\bar{B}\bar{C}$	1	0	0	-	1	
CD	-	-	1	1	1	
$\bar{A}B\bar{C}$	0	1	0	-	-	1
$\bar{A}CD$	0	-	1	1	-	1
ABC	1	1	1	-	-	1
ACD	1	-	1	1	-	1


A
B
C
D
F1
F2

Programmable Array Logic (PAL)

It is a programmable logic device that has programmable AND array & fixed OR Array

i/p → | Programmable AND array | → | Fixed OR array | → o/p

Implement the following function using PAL

$F_1(A,B,C) = \Sigma m(0,1,3,4)$

$F_2(A,B,C) = \Sigma m(3,4,5,6)$

Step 1

K-Map for F_1

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1 ⁽⁰⁾	1 ⁽¹⁾	1 ⁽³⁾	⁽²⁾
A	1 ⁽⁴⁾	⁽⁵⁾	⁽⁷⁾	⁽⁶⁾

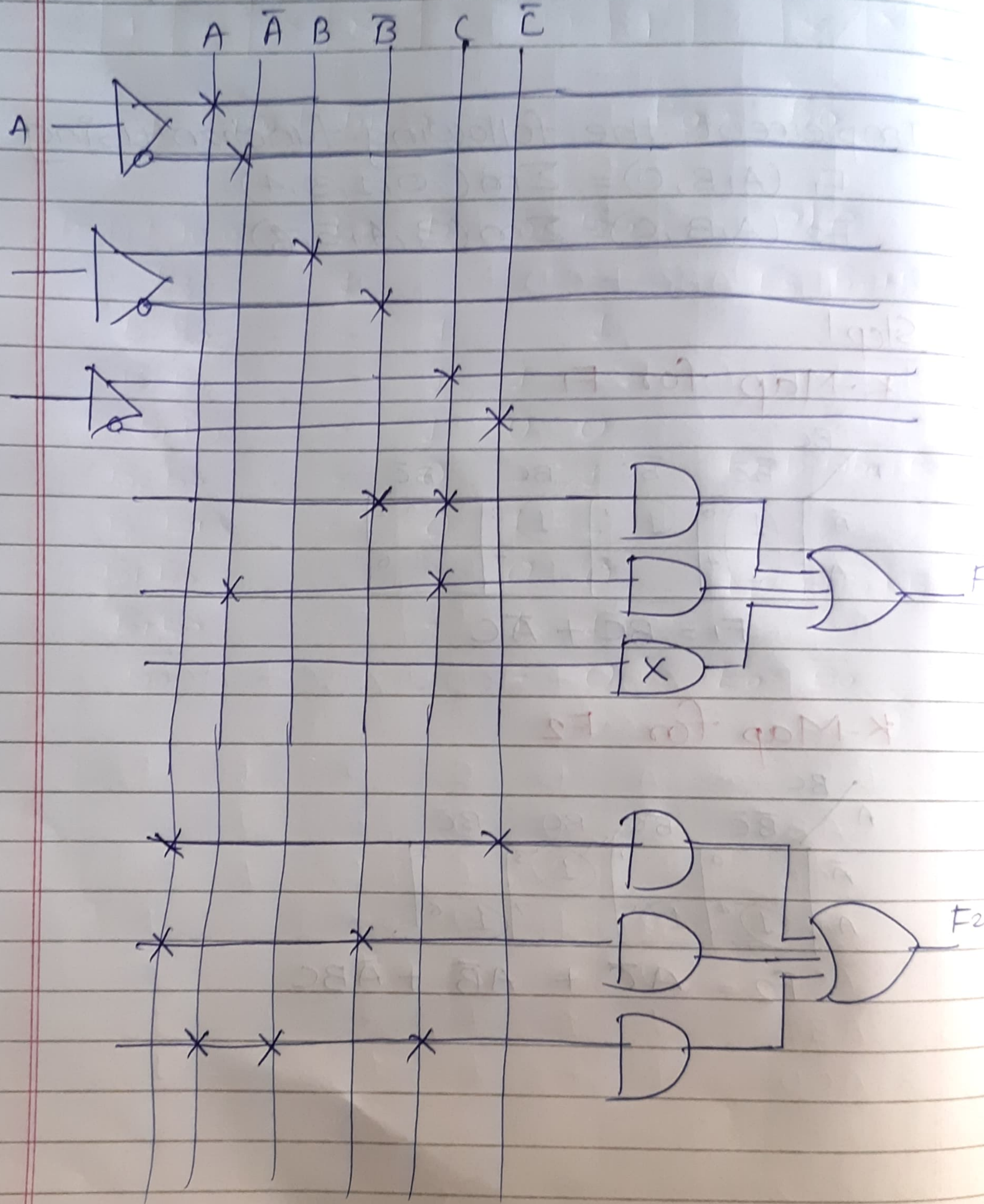
$F_1 = \bar{B}\bar{C} + \bar{A}C$

K-Map for F_2

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	⁽⁰⁾	⁽¹⁾	1 ⁽³⁾	⁽²⁾
A	1 ⁽⁴⁾	1 ⁽⁵⁾	⁽⁷⁾	1 ⁽⁶⁾

$F_2 = A\bar{C} + A\bar{B} + \bar{A}BC$

Product Term	A	B	C	O/P
$\bar{B}C$	-	0	1	$F_1 = \bar{B}C + \bar{A}C$
$\bar{A}C$	0	-	1	
$A\bar{C}$	1	-	0	
$A\bar{B}$	1	0		$F_2 = A\bar{C} + A\bar{B} + \bar{A}BC$
$\bar{A}BC$	0	1	1	



Design BCD to Excess-3 code converter using PAL

Step 1 Truth Table

Decimal	BCD				Excess-3			
	B_3	B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

~~10~~

Step 2

K-Map for E_3

$B_3B_2 \backslash B_1B_0$	$\overline{B_1}\,\overline{B_0}$	$\overline{B_1}B_0$	B_1B_0	$B_1\overline{B_0}$
$\overline{B_3}\,\overline{B_2}$	0	1	3	2
$\overline{B_3}B_2$	4	1 5	1 7	1 6
B_3B_2	X 12	X 13	X 15	X 14
$B_3\overline{B_2}$	1 8	1 9	X 11	X 10

$$E_3 = B_3 + B_2B_0 + B_2B_1$$

K-Map for E_2

$B_3B_2 \backslash B_1B_0$	$\overline{B_1}\,\overline{B_0}$	$\overline{B_1}B_0$	B_1B_0	$B_1\overline{B_0}$
$\overline{B_3}\,\overline{B_2}$	0	1 1	1 3	1 2
$\overline{B_3}B_2$	1 4	5	7	6
B_3B_2	X 12	X 13	X 15	X 16
$B_3\overline{B_2}$	X 8	1 9	X 11	X 10

$$E_2 = B_2\overline{B_1}\,\overline{B_0} + \overline{B_2}B_0 + \overline{B_2}B_1$$

K-Map for E_1

$B_3B_2 \backslash B_1B_0$	$\bar{B}_1\bar{B}_0$	$\bar{B}_1B_0$	B_1B_0	$B_1\bar{B}_0$
$\bar{B}_3\bar{B}_2$	1 (0)	(1)	1 (3)	(2)
$\bar{B}_3B_2$	1 (4)	(5)	1 (7)	(6)
B_3B_2	X (12)	X (13)	X (15)	X (14)
$B_3\bar{B}_2$	1 (8)	(9)	X (11)	X (10)

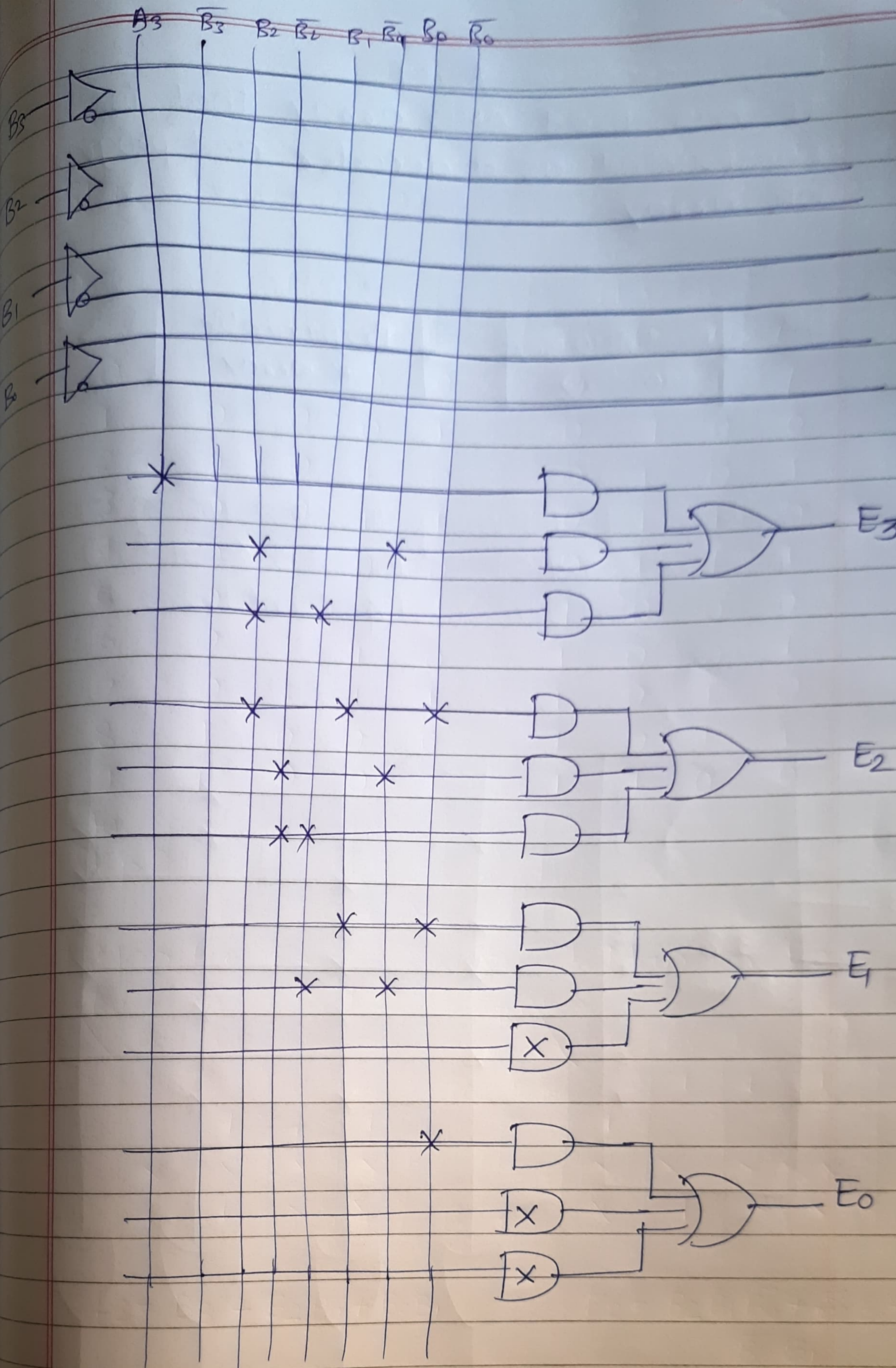
$E_{\cancel{3}1} = \bar{B}_1\bar{B}_0 + B_1B_0$

K-Map for E_0

$B_3B_2 \backslash B_1B_0$	$\bar{B}_1\bar{B}_0$	$\bar{B}_1B_0$	B_1B_0	$B_1\bar{B}_0$
$\bar{B}_3\bar{B}_2$	1 (0)	(1)	(3)	1 (2)
$\bar{B}_3B_2$	1 (4)	(5)	(7)	1 (6)
B_3B_2	X (12)	X (13)	X (15)	X (14)
$B_3\bar{B}_2$	1 (8)	(9)	X (11)	X (10)

$E_0 = \bar{B}_0$

Product Term	B_3	B_2	B_1	B_0	O/P
B_3	1	-	-	-	$E_3 = B_3 + B_2B_0 + B_2B_1$
B_2B_0	-	1	-	1	
B_2B_1	-	1	1	-	
$B_2\bar{B}_1\bar{B}_0$	-	1	0	0	
$\bar{B}_2B_0$	-	0	-	1	$E_2 = B_2\bar{B}_1\bar{B}_0 + \bar{B}_2B_0 + \bar{B}_2B$
$\bar{B}_2B_1$	-	0	1	-	
$\bar{B}_1\bar{B}_0$	-	-	0	0	$E_1 = \bar{B}_1\bar{B}_0 + B_1B_0$
B_1B_0	-	-	1	1	
$\bar{B}_0$	-	-	-	0	$E_0 = \bar{B}_0$


A3
$\overline{B_3}$
B2
$\overline{B_2}$
B1
$\overline{B_1}$
B0
$\overline{B_0}$
B3
B2
B1
B0
E3
E2
E1
E0

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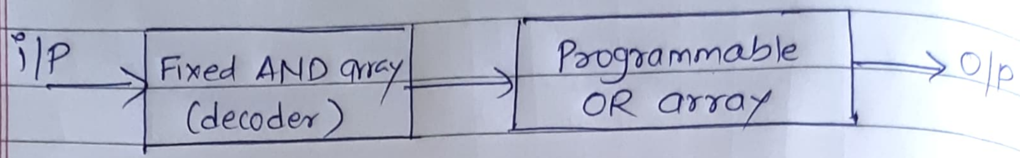
Programmable ROM

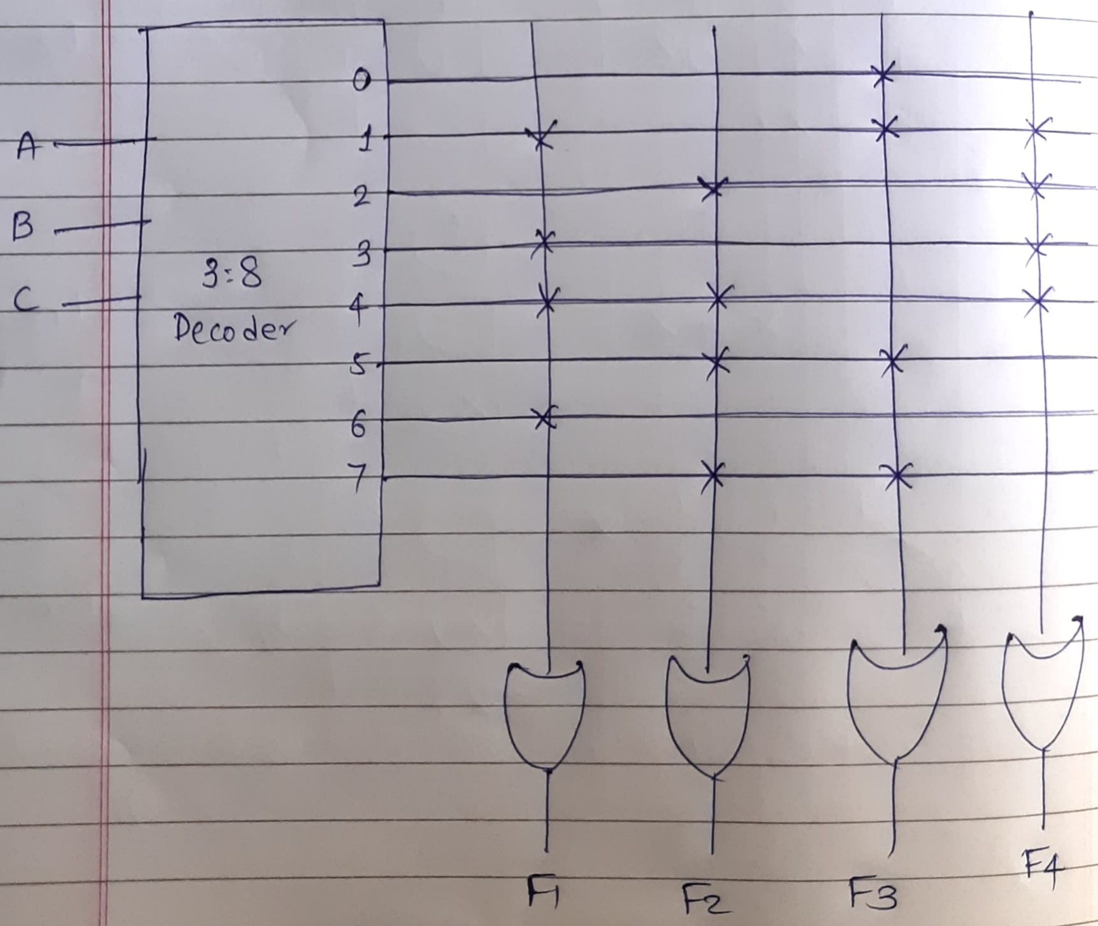
It has fixed AND array that is constructed as a decoder and programmable OR array.



Implement following function using PROM.

$F_1 = \Sigma m(1,3,4,6)$ $F_2 = \Sigma m(2,4,5,7)$

$F_3 = \Sigma m(0,1,5,7)$ $F_4 = \Sigma m(1,2,3,4)$



Design 3 bit Binary to Gray code converter using PROM.

Step 1 Truth Table

	Binary Code			Gray Code		
	B_2	B_1	B_0	G_2	G_1	G_0
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	1
3	0	1	1	0	1	0
4	1	0	0	1	1	0
5	1	0	1	1	1	1
6	1	1	0	1	0	1
7	1	1	1	1	0	0

$G_2 = \Sigma m(4,5,6,7)$ $\quad$ $G_1 = \Sigma m(2,3,4,5)$

$G_0 = \Sigma m(1,2,5,6)$