Product Brief

PC202

Integrated Baseband Processor

Features

- picoArray Baseband Processor Array
- ARM®926EJ-S Processor
  - 280MHz
  - 64KB I + 64KB D cache
  - 128KB Tightly Coupled Memory (TCM)
  - 128KB on-chip SRAM
  - RS-232/JTAG for debug
- Quad FFT Block
- Cryptographic Engine
  - AES, DES and 3DES
- FEC Accelerator
  - Turbo-code
  - Reed-Solomon
  - Viterbi
- 10/100 Ethernet MAC and MII
  - Reverse MII mode
- DDR2 SDRAM Interface
  - 16/32-bit
  - 200MHz clock
  - 256Mbit to 2Gbit
- Multiple Boot Options
  - Flash Memory
  - External Processor
  - MII Boot Packet
- General Purpose I/O - 32 pins
  - SIM Interface
  - Sigma Delta DAC
  - SPI/I^2C
- Commercial Temperature Range
- 672 PBGA Package (27x27)
  - Lead-free RoHS Compliant

Description

The picoChip PC202 is a highly integrated and cost effective baseband processor for broadband wireless access subscriber station applications.

The PC202 consists of a flexible software defined modem, powerful ARM®926EJ-S processor, cryptographic engine, optimized co-processors, and peripherals capable of supporting all of the mandatory features of WCDMA together with optional features, including advanced CTC (Convolutional Turbo Coder). All physical layer (PHY), lower MAC, upper MAC, and cryptographic features are integrated, enabling a greatly reduced BOM.

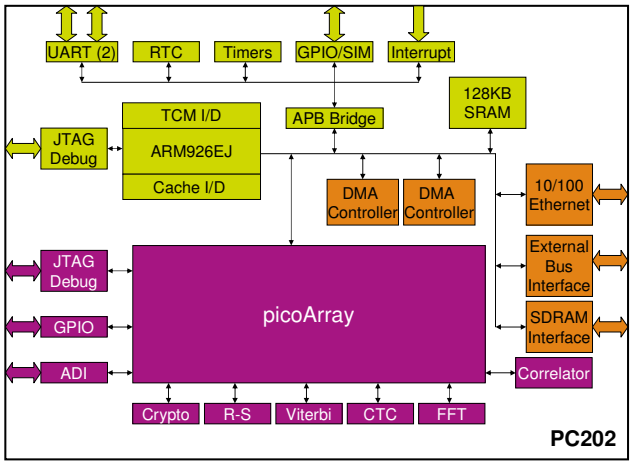
Flexible interfaces support multiple boot options, SDRAM memory, LAN, and radio interfaces minimize glue logic for a complete system solution.

A corresponding reference design for 802.16 PHY and MAC is available, enabling high-performance systems (improved rate/reach), beyond minimum performance requirements. The system supports upgrades (future-proof) to support interoperability, changes to the standard, or manufacturer specific features.

A WCDMA Picocell base station reference design is also available.

Applications

- HSDPA WCDMA Femtocell/Access Point
- CDMA 2000/EVDO Femtocells
- GSM/EDGE Femtocell
- Broadband Wireless Access
- Advanced Wireless
  - JTRS
  - Software Defined Radio
- Test and Measurement
- Medical Imaging



PC202 Simplified Block Diagram

PicoArray Sub-System

The picoArray is a software defined signal processor responsible for executing the PHY and lower MAC software. The advantage of picoArray is that it maintains flexibility within the PHY and lower MAC functions, allowing software upgrades to be simply applied as necessary in line with product release, localisation, standardisation updates, bug fixes, performance enhancements etc.

Multicore DSP Array (picoArray)

The picoArray consists an array of LIW DSPs (AEs) capable of up to 6 operations per cycle. Each AE has dedicated instruction memory and data memory. Each AE also has access to shared on-chip SRAM and off-chip DRAM. Dedicated instruction and data memory for each processor means very little contention for shared memory resources. There are three different types of AEs in the PC202. The table on the right lists the number and type of each AE along with its dedicated memory sizes.

AE Type	Number of AEs	Memory (Bytes)
STAN	196	768
MEM	50	8,704
CTRL	2	65,536
Total	248	716,800

Flexible interconnect provides point-to-point and point-to-multipoint connections between any two AEs with dedicated bandwidth.

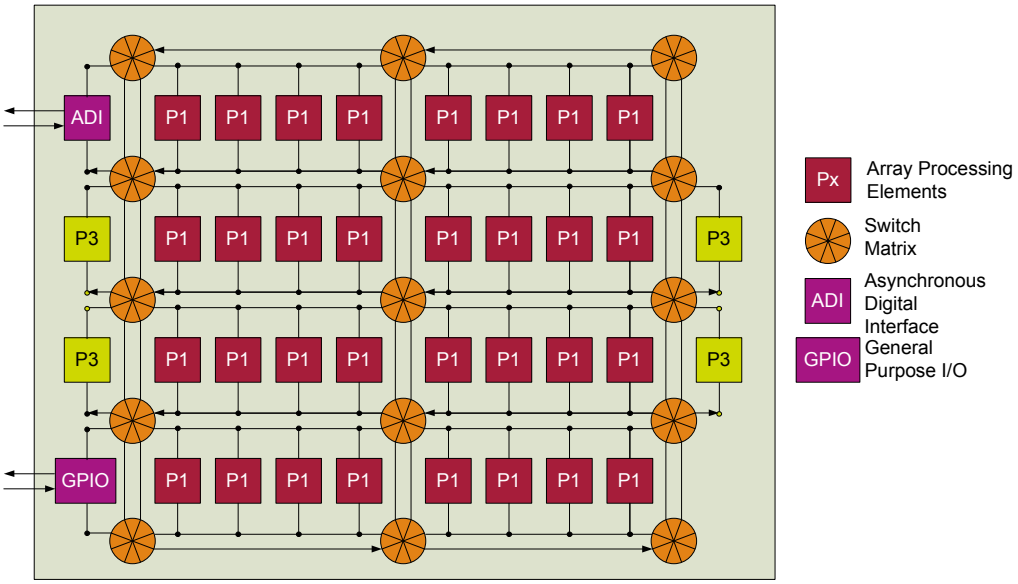


Figure 1 picoArray of DSP Processors and Interconnect

Convolutional Turbo Code (CTC) Block

PC202 incorporates a hardware defined CTC block capable of supporting data rates up to 8 Mbps. The CTC algorithm which is optionally required in the SOFDMA air interface of IEEE 802.16e, and mandatory in TTA WiBRO allows much enhanced bit error rates in a data channel compared to CC and R-S coding. The CTC also supports all the 3GPP turbo code requirements. Soft input values are 8 bits, with a maximum number of 4800 soft inputs.

FFT/IFFT

FFT hardware accelerator designed to optimise the performance of OFDM based systems. The FFT engine can support complex FFT sizes of 128, 256, 512 and 1024 points. (FFTs up to 2048 points can be accommodated in software.) Features of the FFT block include on-the-fly FFT/IFFT, 16-bit input and output with scaling, bit reversal capability, and self-flushing mechanism.

Viterbi
Viterbi hardware accelerator block is used to accelerate the Viterbi decoding process in wireless systems. The Viterbi block is optimised for WiMAX and HSDPA systems. It is configurable for constraint lengths of 2 to 9, and rates of 1/2, 1/3, 1/4, 1/5, 1/6, 1/7 or 1/8. Multiple puncturing rates are also supported. Block sizes are from 16 to 1024.

Reed-Solomon (R-S)
The PC202 incorporates a Reed-Solomon accelerator block for use in R-S block coding requirements.

Cryptographic Engine
The PC202 incorporates the support of AES, DES & 3DES algorithms as required by the MAC security sub-layer and IPSec. Additional standards supported include NIST FIPS PUB 197, PUB 46-3, 800-38C, SP 800-38A.

Feature	Perf.	Units
picoArray	31	GMAC/s
	230	GIP/s
	8	GMUL/s
FFT (aggregate)	80	MS/s
Crypto Engine	12	Mb/s
Turbo Code (8 iter.)	8	Mb/s
Viterbi	8	Mb/s
R-S	8	Mb/s
ADI	1x160	MS/s
ARM	280	MHz

ARM® Sub-System

The ARM® sub-system is based around the ARM®926EJ-S core from ARM® Ltd. This powerful 32-bit RISC processor is highly optimised for low power, high performance computing. Being an industry standard core, the ARM® is supported by various openly available tool chains and debuggers. JTAG ports support a simple and familiar development environment.

ARM® Memory Architecture

The memory architecture supports a full range of memory types, allowing flexible memory map allocation depending upon the particular application requirements. The cache and tightly coupled memory deliver maximum processor performance. The memory types are summarised as follows

- On-chip memory for maximum performance
  - 64KB instruction, 64KB data cache, 32 bits wide
  - 64KB instruction, 64KB data TCM (Tightly Coupled Memory), 32-bit wide single state access
  - 128MB SRAM, 32 bits wide, two state access
- External Bus Interface (EBI) supporting following memory types
  - DDR2-SDRAM via dedicated interface
  - NOR Flash for system boot and parameter storage

ARM® Peripherals

PC202 integrates a number of peripheral blocks allowing a reduction in total system BOM cost, as well as providing flexible interfaces to application-specific sub-systems. The ARM® peripherals are logically mapped into the ARM® memory map, and are conveniently configurable by way of dedicated registers per block. The principle ARM® peripheral blocs are summarised as follows:

- General purpose timer block e.g. for operating system tick
- Watchdog Timer
- Dual UART RS-232 interface for real time tracing of MAC software
- 10/100 Ethernet MAC
  - Reverse MII interface allowing direct connection to MII interfaces of router/WiFi chipsets
  - Built-in DMA controller
- GPIO – SPI radio control, I2C, SIM card interface
- Vectored Interrupt Controller

Applications Examples

WCDMA Home Basestation

An emerging application is the use of in-home internet access connections like ADSL and low-cost flexible wireless PHY technology like the PC202 to create an in-home 3G/2G femto-cell basestation.

The PC202 PHY implementation and an ADSL link for backhaul allows mobile phone operators to offer a new level of service where customers can use their mobile phones at home; even in areas of poor coverage. picoChip offers a complete WCDMA reference design for small basestation applications.

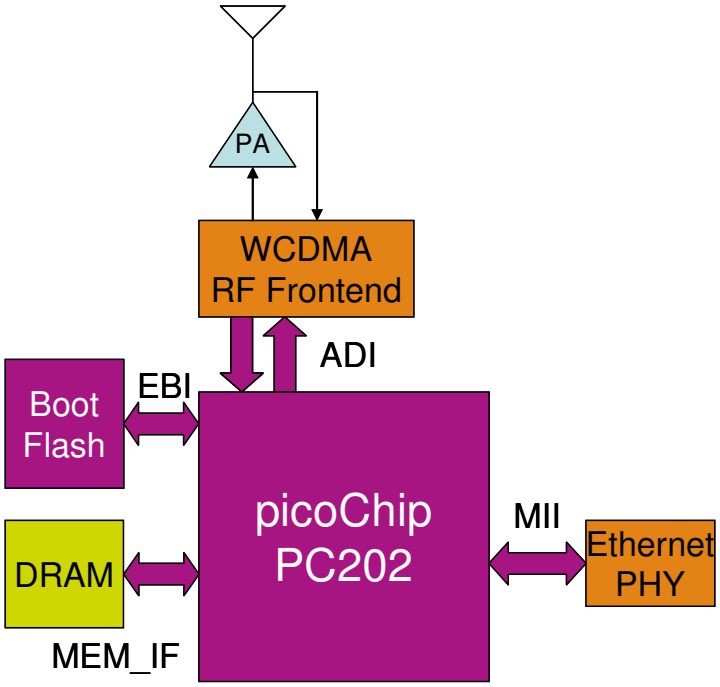


Figure 2 WCDMA Femtocell