MEMO: TSR-06
DATE: February 9, 2018
TO: EFC LaBerge
FROM: Sabbir Ahmed, Jeffrey Osazuwa, Howard To, Brian Weber
SUBJECT: Team Status Report

1 Introduction

The Galois Field Arithmetic Unit will accept two inputs a and b and determine the desired arithmetic result n, and to establish the field generating polynomial. The unit would serve as a computation engine for a relatively low-powered microcontroller, and would enable complex code and encryption algorithms. Project will include implementation of a Reed Solomon encoder and decoder using the GFAU. The purpose of this report is to detail the progress of the GFAU in the period of December 7, 2017 through February 9, 2018. This is the sixth and first status report for the second semester for the GFAU team.

2 Completed Tasks

During this work period, the team has continued to make progress on the GFAU. Including the following achievements:

a) Most VHDL coding is done with issues detail in the Current Issues section of this document.

b) Updated system block diagram (see Figure 1 below).

c) Completed breakout board design.

3 Planned Tasks

a) Order breakout board.

b) Program FPGA with VHDL code and resolve any issues arise.

c) Interface FPGA with external memory.

4 Current Issues

Current issues the team are having include:

a) Need to receive testing instruments from Dr. LaBerge to verify design.

b) Timing issue with zero and the zeroth term and their memory address.

c) Timing issue with generating polynomials.

d) Problem generating one symbol per clock cycle.

e) Not sure how to simulate memory and IO with VHDL.

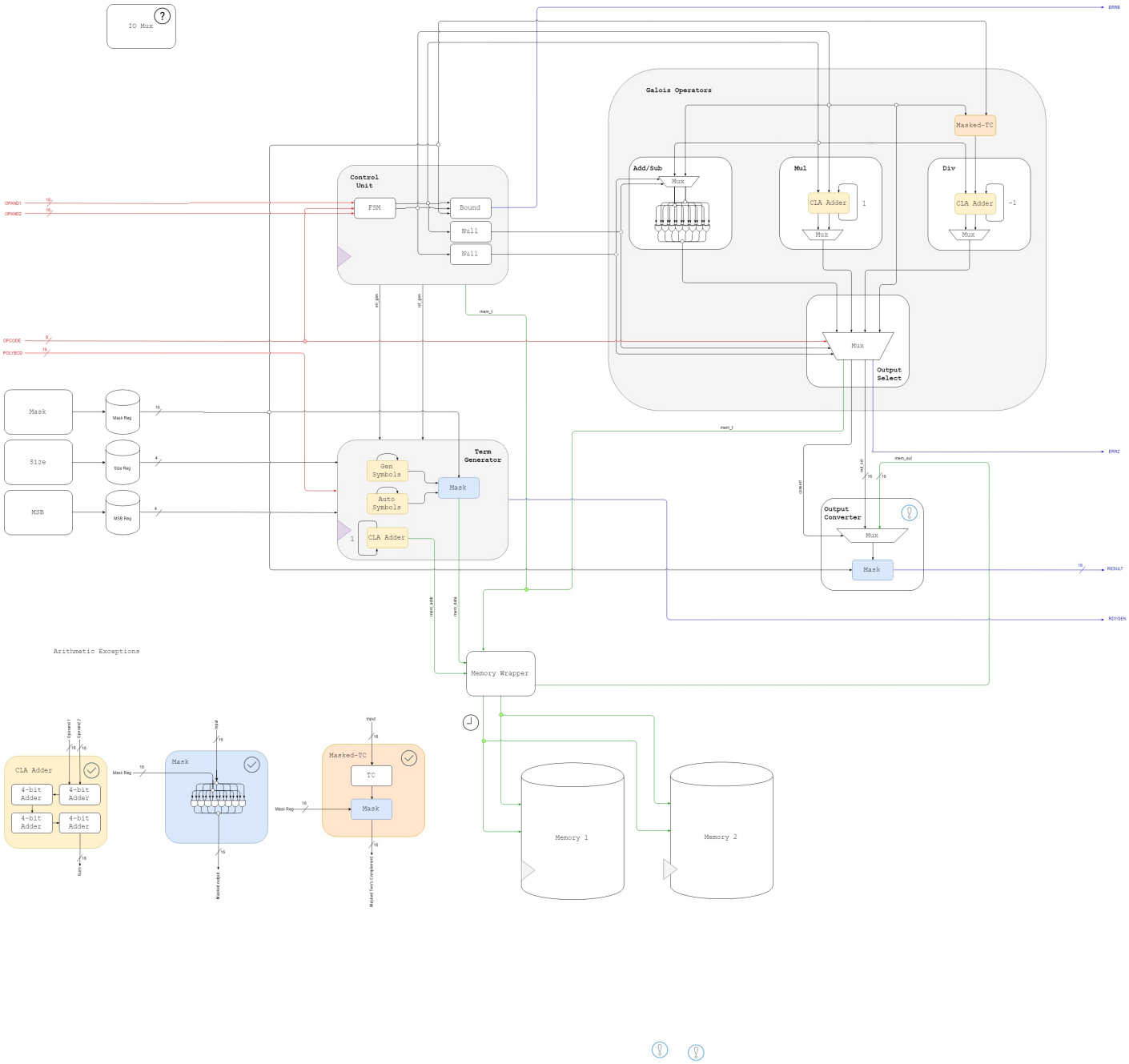

Figure 1: Figure 1. System block diagram