MEMO NUMBER: GFAU-SOW
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TO: EFC LaBerge
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SUBJECT: Galois Field Arithmetic Unit Statement of Work

1 Introduction

A Galois field is a field with a finite number of elements. The nomenclature $GF(q)$ is used to indicate a Galois field with q elements. For $GF(q)$ in general, q must be a power of a prime. For each prime power, there exists exactly one finite field. The best known and most used Galois field is $GF(2)$, the binary field.

The Galois Field Arithmetic Unit handles irreducible polynomials in $GF(2^n)$, where $\{2 \leq n \leq 16\}$. The ALU generates all the terms in the field of the polynomial, and allows the user to view and apply the following binary operations:

- Addition
- Subtraction
- Multiplication
- Division
- Logarithm

1.1 Purpose and Scope

This Statement of Work outlines and elaborates the tasks necessary to implement the project. The document also details their corresponding milestones and deadlines and how the contribution will be divided within the team.

2 Roles and Division of Labor

This project requires equal team work on all tasks because of the steep learning curve on implementing coprocessors with programmable boards. None of the team members have comprehensive prior knowledge or training on field programmable gate array units, and are therefore required to learn the concepts concurrently.

Although there is no clear division of labor within the team, each members have been implicitly designated unofficial roles.

Howard has been chosen to act as the point of contact between the team and the project manager and other consultants. He has also been trusted with the scheduling of team meetings and milestones.

Sabbir is responsible for validating the system inputs and outputs through the operations in the unit. He is also accountable for providing background information on the Galois field and its operations related to the arithmetic unit.

Brian has been put in charge with the digital design of the system at various levels. He is also responsible for overseeing the designing of the system using the hardware description language.

Jeffrey supports the designing processes by providing test benches and by synthesizing the individual modules.

Each members of the GFAU shall contribute to designing the individual modules and the entire system.

3 Tasks

3.1 Research

3.1.1 Background

3.1.2 Devices

3.1.2.1 Field Programmable Gate Array (FPGA)

3.1.2.2 External Devices

3.2 Design

3.2.1 System Boundary

3.2.2 Schematics

3.3 Software Implementation

3.3.1 Design in VHSIC Hardware Description Language (VHDL)

3.3.2 Simulation and Synthesis in VHDL

3.3.3 External Devices

3.4 Purchases

3.5 Hardware

3.5.1 Integration

4 Deliverables