605.611 - Foundations of Computer Architecture

Assignment 09 - Paging

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1. Calculate the size of memory if its address consists of 22 bits and the memory is 2-byte addressable.

   Answer: 22 bits = 2^{22} locations possible. Since one location is 2 bytes:

   $$= 2^{22} \cdot 2 \text{ bytes}$$
   $$= 2^{23} \text{ bytes}$$

   = 222 x 2 bytes

   = 223 bytes

   = 8 MB

2. Calculate the number of bits required in the address for memory having size of 16 GB. Assume the memory is 4-byte addressable.

   Answer: Let 'n' number of bits are required. Then, Size of memory = 2n x 4 bytes.

   Since, the given memory has size of 16 GB, so we have-

   2n x 4 bytes = 16 GB

   2n x 4 = 16 G

   2n x 22 = 234

   2n = 232

   n = 32 bits

3. Consider a system with byte-addressable memory, 32 bit logical addresses, 4 kilobyte page size and page table entries of 4 bytes each. The size of the page table in the system in megabytes is .

   (a) 2

   (b) 4

   (c) 8

   (d) 16

   Answer: Given-

   Number of bits in logical address = 32 bits Page size = 4KB Page table entry size = 4 bytes

   Process Size-

   Number of bits in logical address = 32 bits

   Thus,

   Process size

   = 232 B

   = 4 GB

   Number of Entries in Page Table-

   Number of pages the process is divided

   = Process size / Page size

   = 4 GB / 4 KB

   = 220 pages

   Thus,

   Number of entries in page table = 220 entries

   Page Table Size-

   Page table size

= Number of entries in page table x Page table entry size

= 220 x 4 bytes

= 4 MB

Thus, Option (B) is correct.

4. Consider a machine with 64 MB physical memory and a 32 bit virtual address space. If the page size is 4 KB, what is the approximate size of the page table?

   16 MB 8 MB 2 MB 24 MB

   Answer: Given-

   Size of main memory = 64 MB Number of bits in virtual address space = 32 bits Page size = 4 KB

   We will consider that the memory is byte addressable.

   Number of Bits in Physical Address-

   Size of main memory

   = 64 MB

   = 226 B

   Thus, Number of bits in physical address = 26 bits

   Number of Frames in Main Memory-

   Number of frames in main memory

   = Size of main memory / Frame size

   = 64 MB / 4 KB

   = 226 B / 212 B

   = 214

   Thus, Number of bits in frame number = 14 bits

   Number of Bits in Page Offset-

   We have,

Page size

= 4 KB

= 212 B

Thus, Number of bits in page offset = 12 bits

So, Physical address is-

Process Size-

Number of bits in virtual address space = 32 bits

Thus,

Process size

= 232 B

= 4 GB

Number of Entries in Page Table-

Number of pages the process is divided

= Process size / Page size

= 4 GB / 4 KB

= 220 pages

Thus, Number of entries in page table = 220 entries

Page Table Size-

Page table size

= Number of entries in page table x Page table entry size

= Number of entries in page table x Number of bits in frame number

= 220 x 14 bits

= 220 x 16 bits (Approximating 14 bits 16 bits)

= 220 x 2 bytes

= 2 MB

Thus, Option (C) is correct.

5. In a virtual memory system, size of virtual address is 32-bit, size of physical address is 30-bit, page size is 4 Kbyte and size of each page table entry is 32-bit. The main memory is byte addressable. Which one of the following is the maximum number of bits that can be used for storing protection and other information in each page table entry?

   2 10 12 14

   Answer:

   Given-

   Number of bits in virtual address = 32 bits Number of bits in physical address = 30 bits Page size = 4 KB Page table entry size = 32 bits

   Size of Main Memory-

   Number of bits in physical address = 30 bits

   Thus,

   Size of main memory

   = 230 B

   = 1 GB

   Number of Frames in Main Memory-

   Number of frames in main memory

   = Size of main memory / Frame size

   = 1 GB / 4 KB

   = 230 B / 212 B

   = 218

   Thus, Number of bits in frame number = 18 bits

   Number of Bits used for Storing other Information-

Maximum number of bits that can be used for storing protection and other information

= Page table entry size – Number of bits in frame number

= 32 bits – 18 bits

= 14 bits

Thus, Option (D) is correct.

Pipeline Register	**Size (bits)**	**Values**
`IF/ID`	64	Instruction (32) PC (32)
`ID/EX`	147	Control bits (9) PC (32) Read data (64) Sign-extended immediate (32) `rs` from `IF/ID` (5) `rt` from `IF/ID` (5)
`EX/MEM`	107	Control bits (5) PC (32) ALU result (32) ALU zero (1) Read data 2 (32) `rt`/`rs` (5)
`MEM/WB`	103	Control bits (2) Read data (64) ALU result from `EX/MEM` (32) `rt`/`rs` (5)