

Figure , ADC Qsys System

Figure 1 show the Qsys system. Qsys creates a system from IP blocks. The blocks are easily connected by clicking on the available nodes. Connecting to port is done by exporting the connections. The exported connections are mapped to the development kit using Quartus.

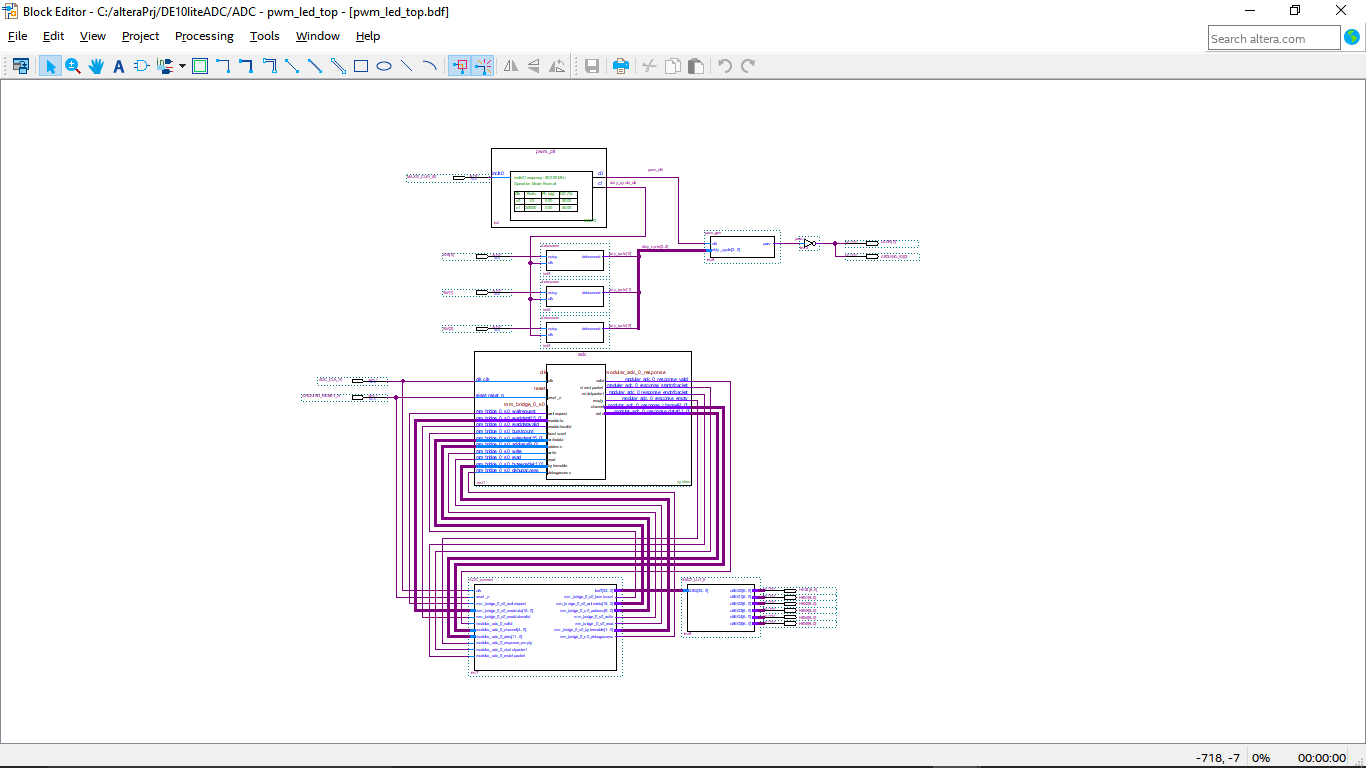


Figure , ADC block Diagram

The block diagram consists of the PWM circuit and the added ADC circuit. The symbols we created from the HDL files of the Qsys circuits. Connecting the various nodes was done manually and required attention to detail.

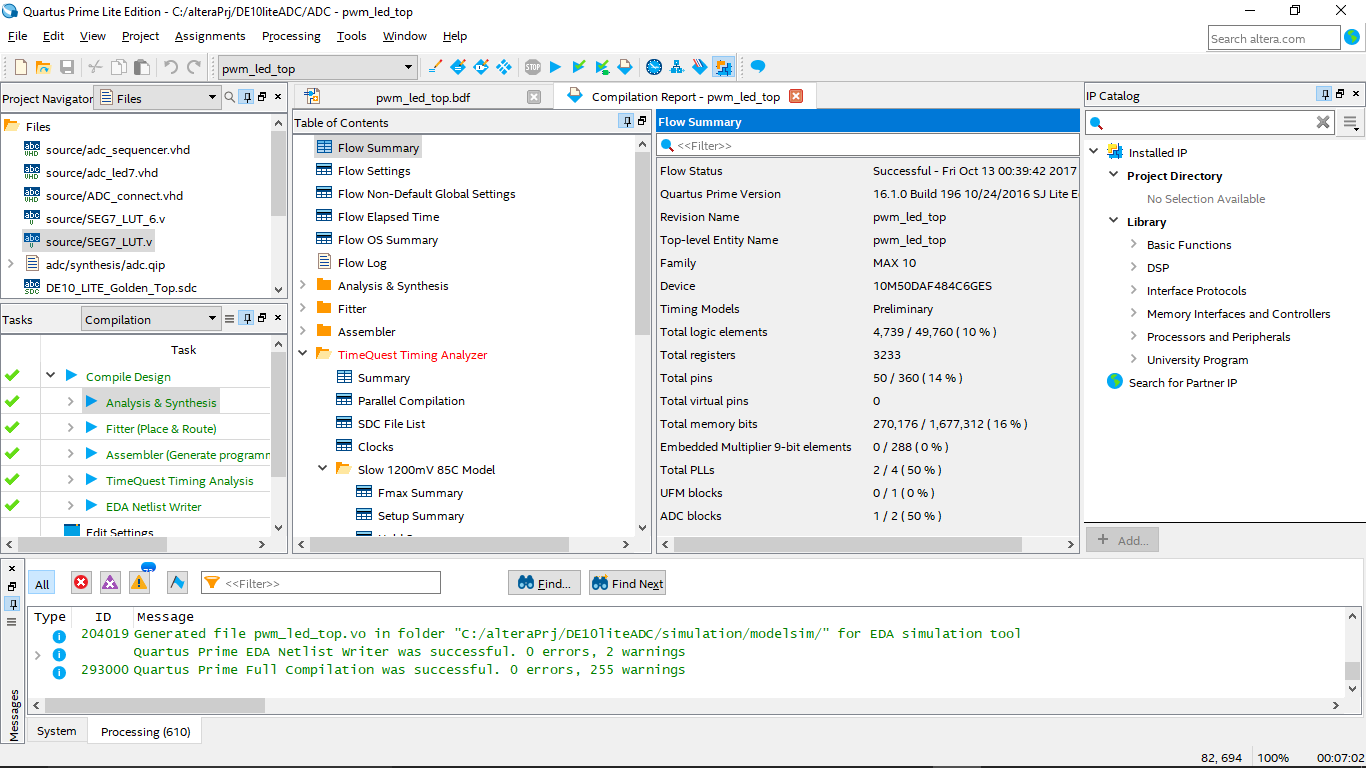


Figure , ADC Compiled Flow Summary

The compiled project creates the Flow Summary. This summary shows the design metrics. This design uses 10% of the logic elements available.

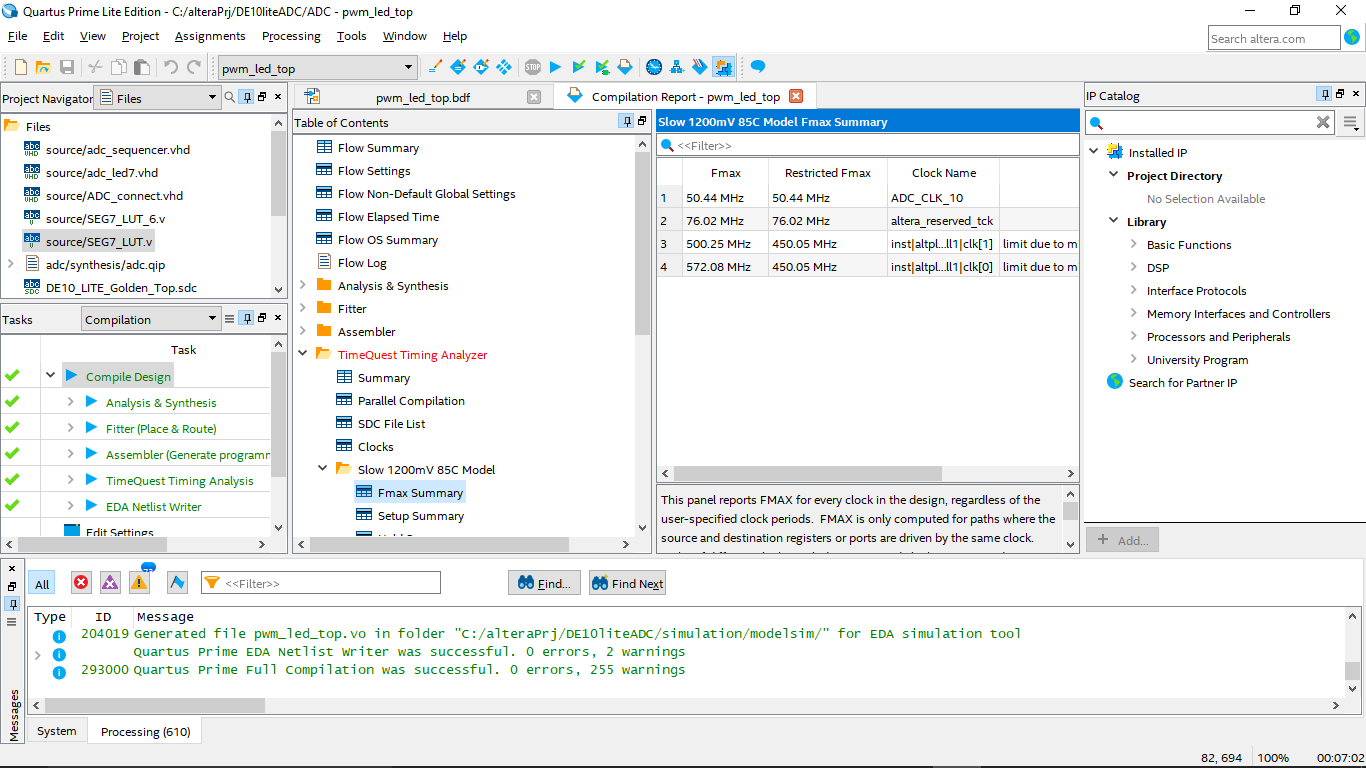


Figure , ADC Fmax Summary

Figure 4 show the Fmax Summary for the 1200mV 85C model.

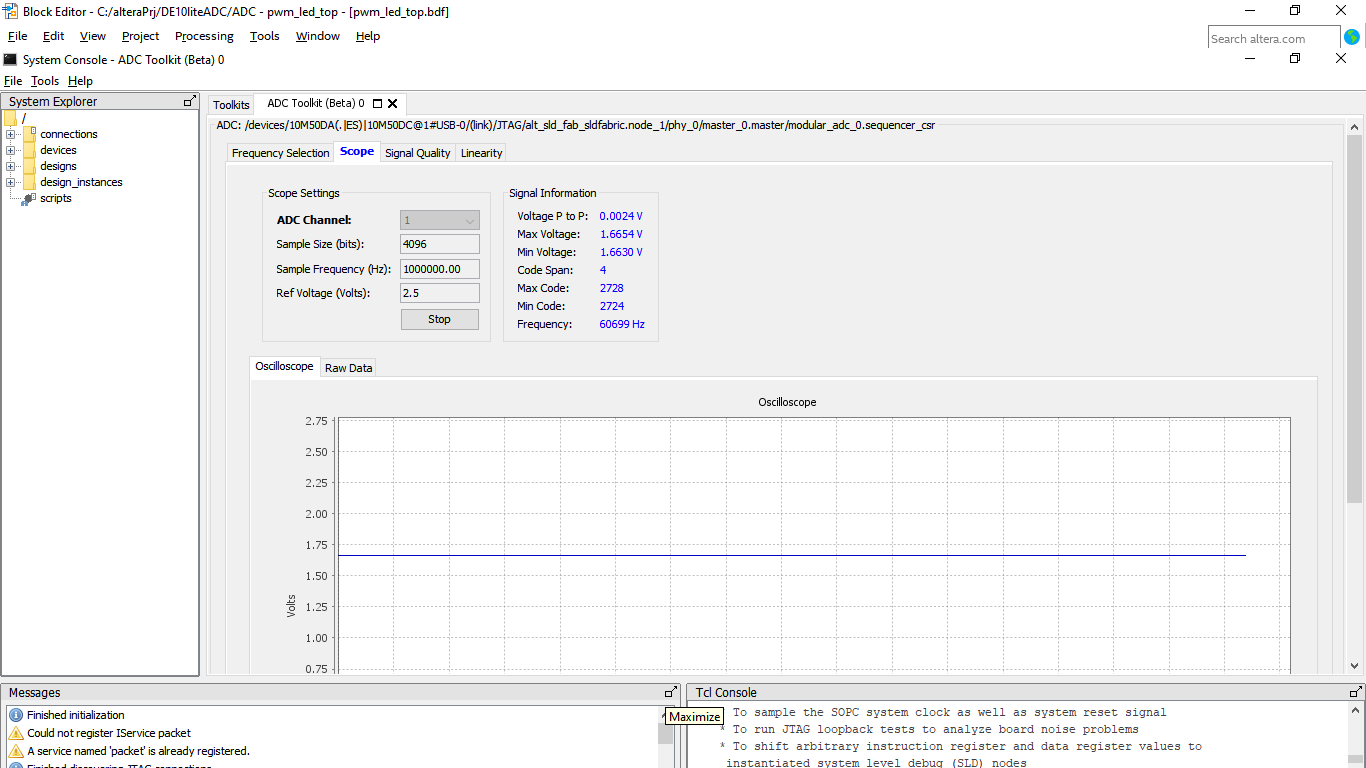


Figure , ADC System Console

The System Console is a Quartus tool for system debugging. This view show voltage characteristics of the ADC channel 1.

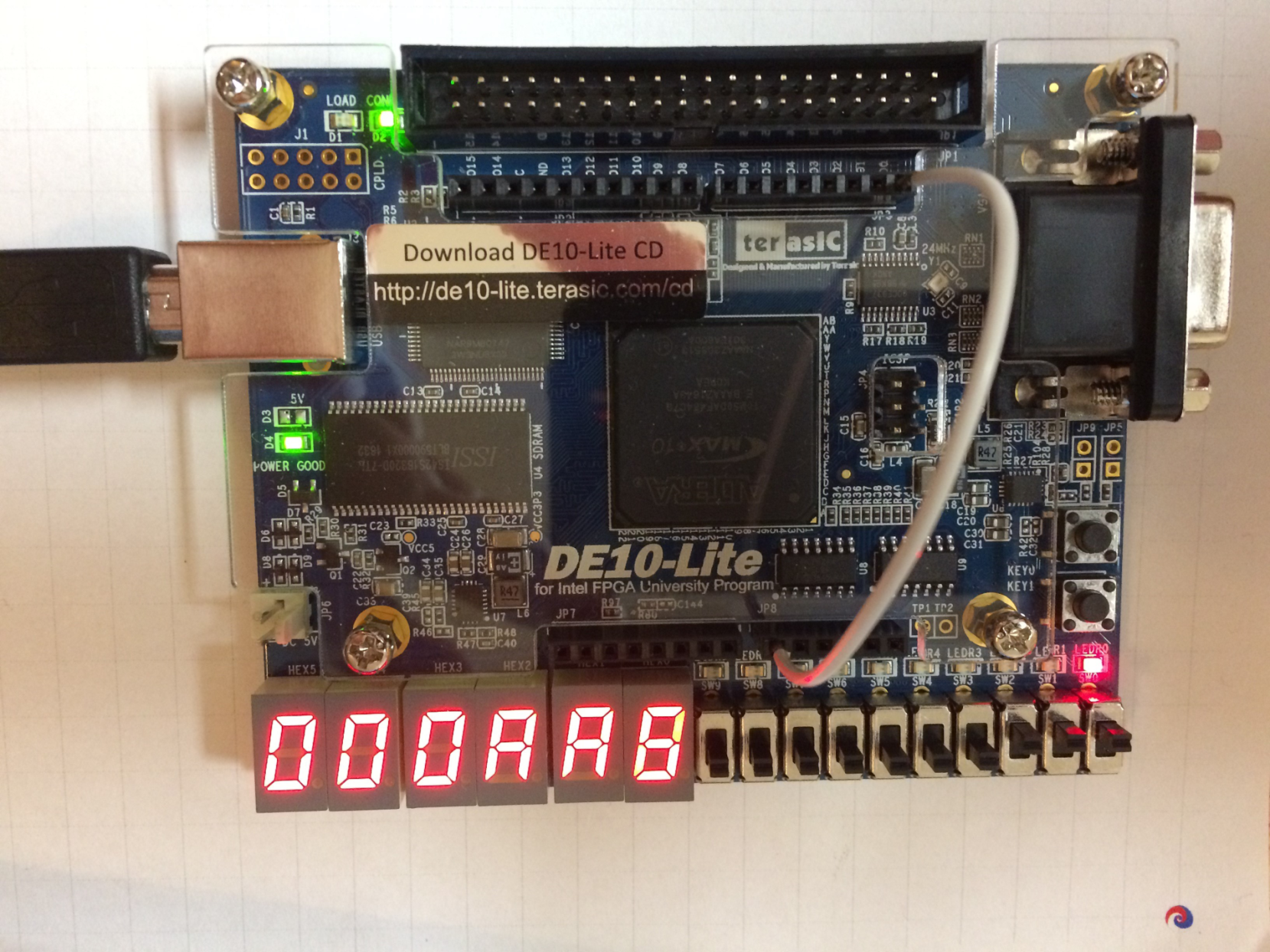


Figure , ADC Demostration

Figure 6 demonstrates the ADC design. This image show the 7 segment display conversion of SW[0..2]=111.