**Module 2**

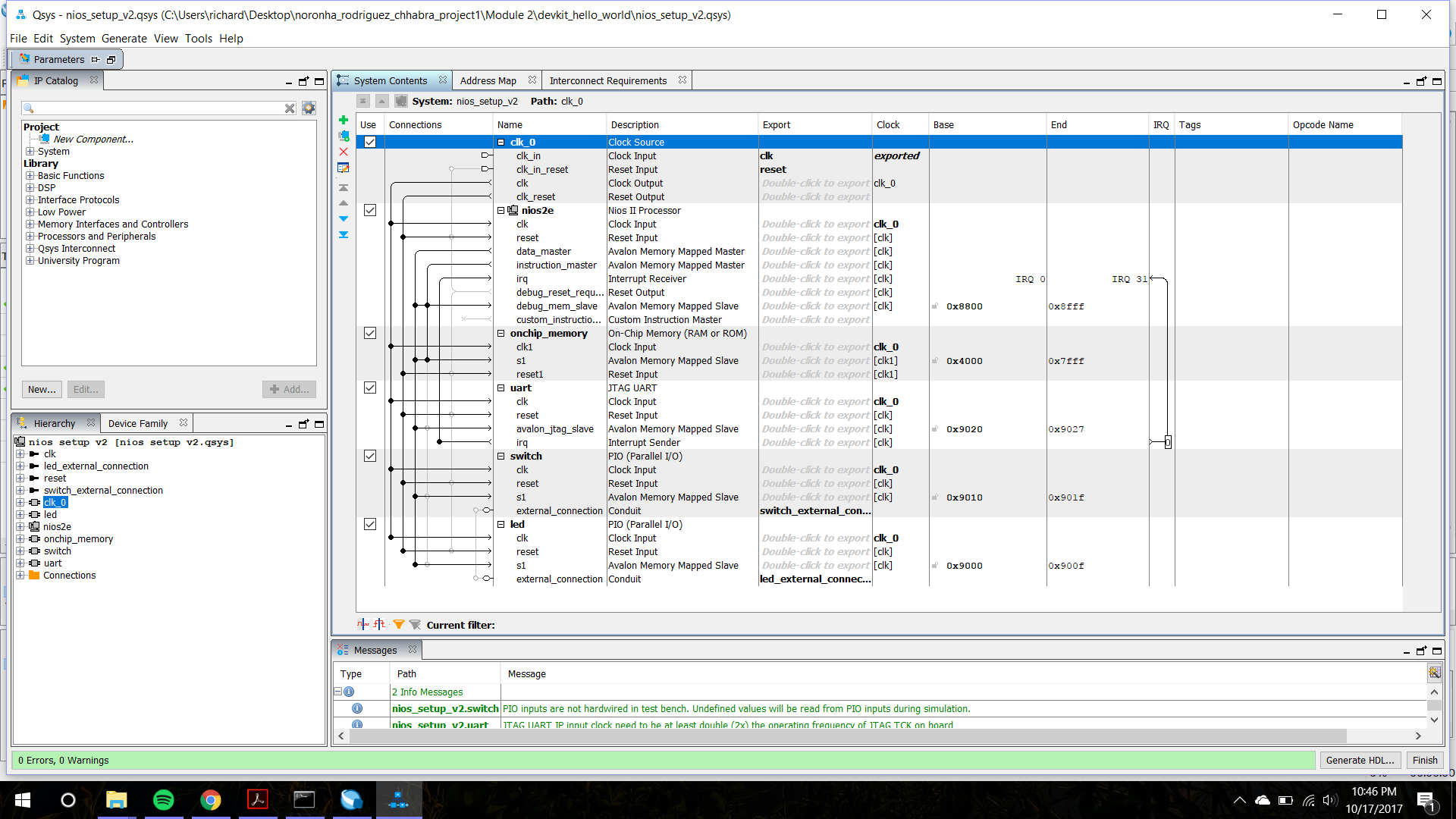


Fig 1. Qsys connections



Fig 2. Successful generation of the HDL code

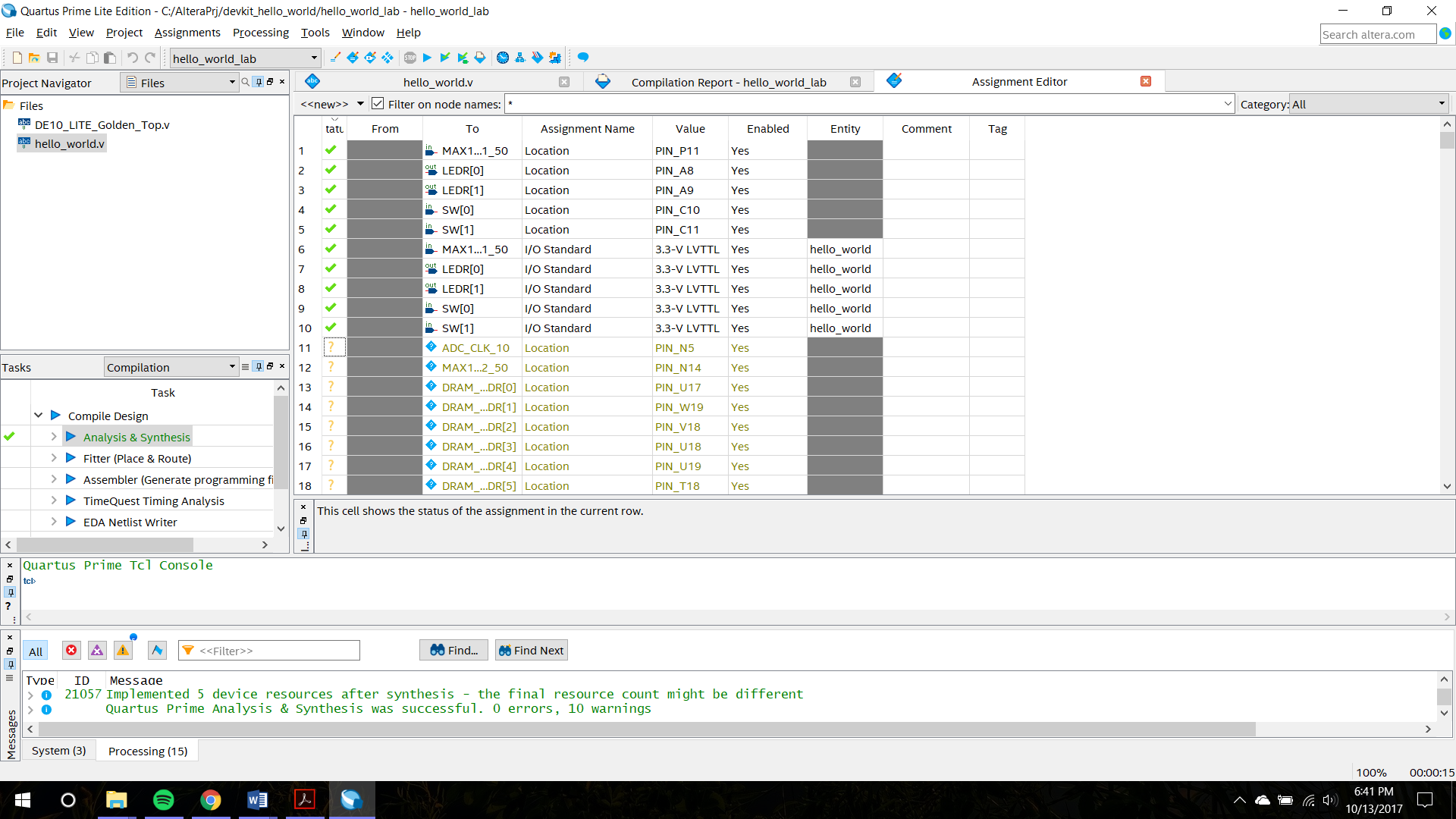


Fig 3. The assignment of the various pins in the module

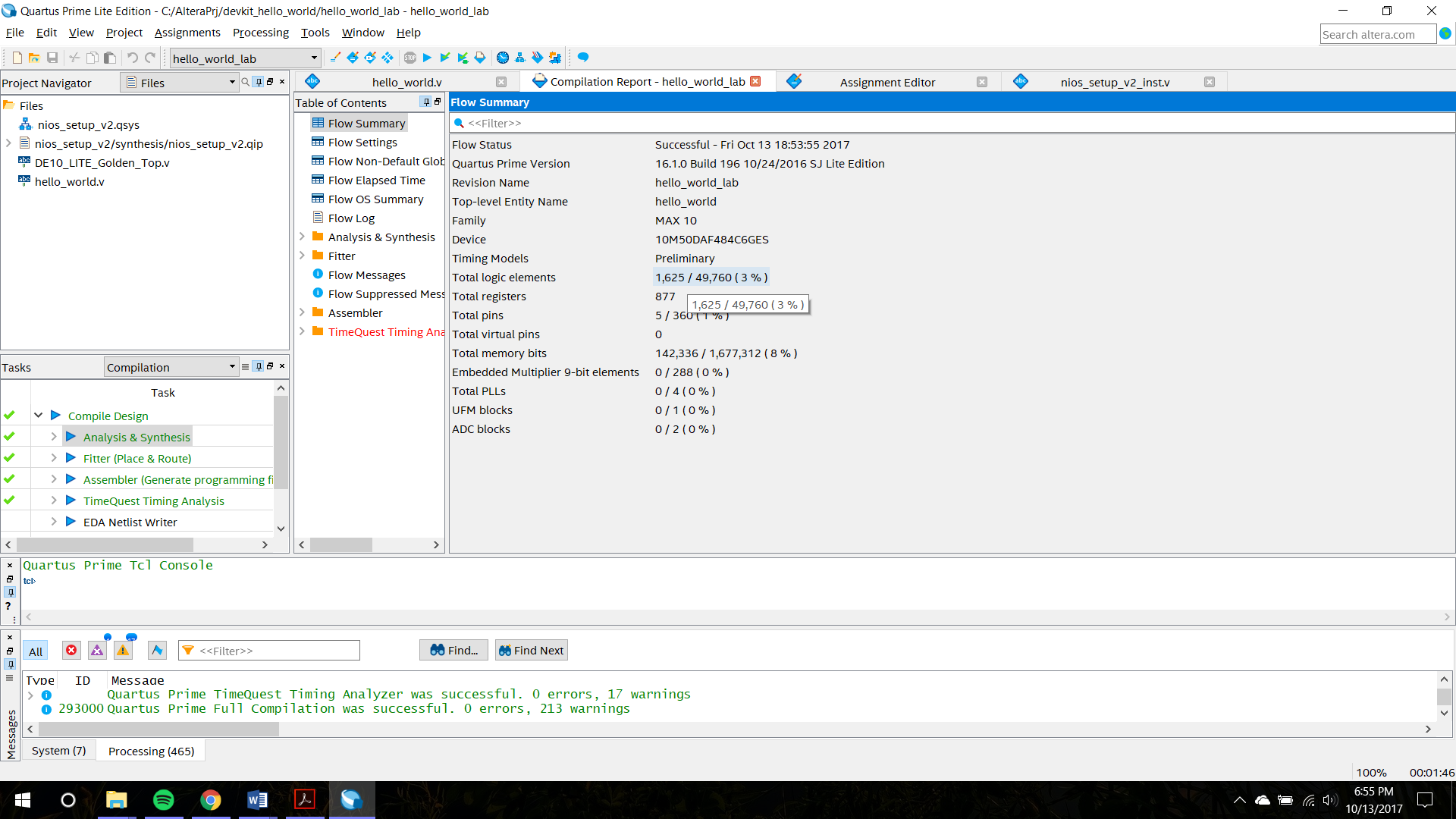


Fig 4. Successful compilation report

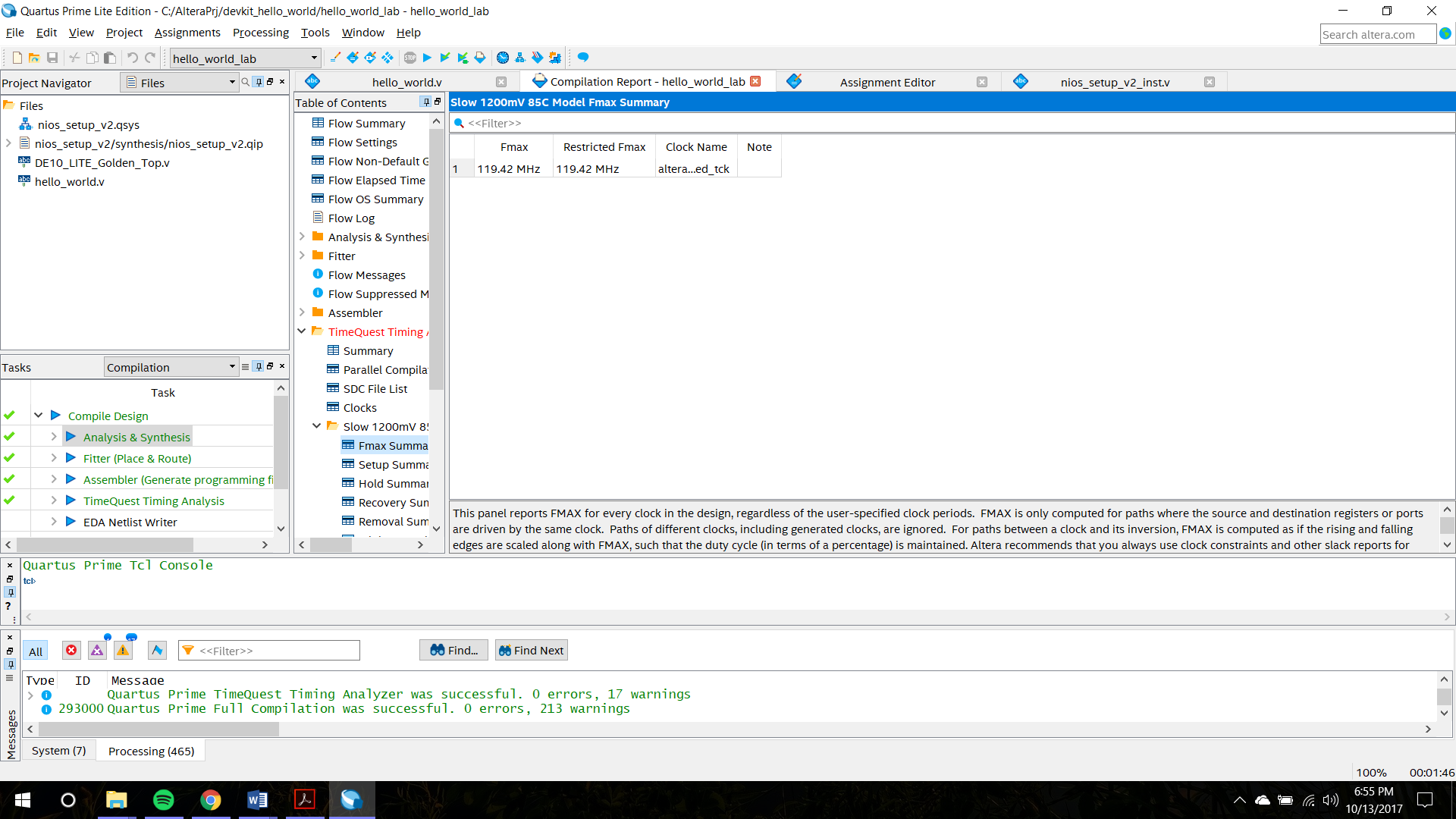


Fig 5. Fmax

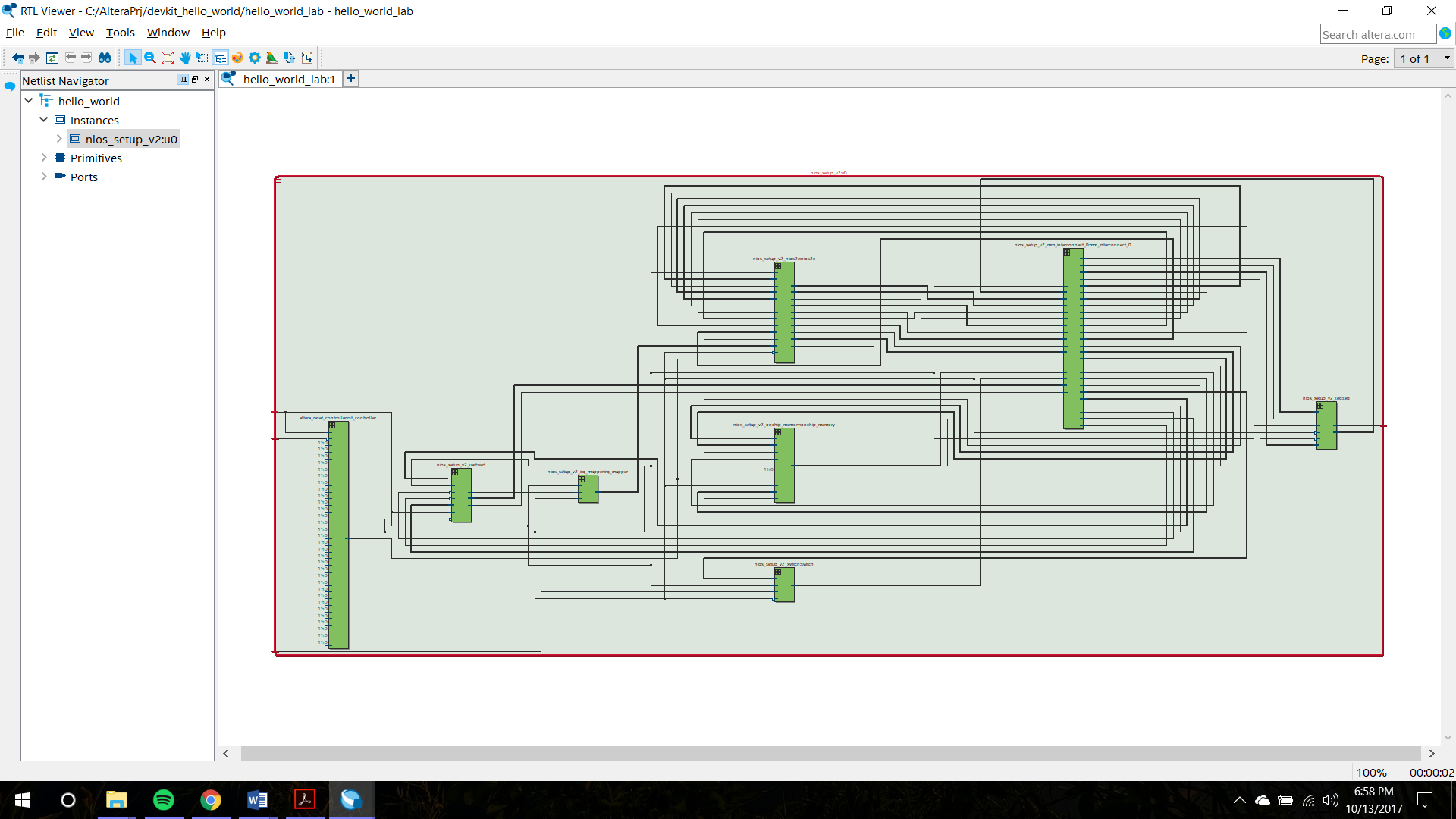


Fig 6 RTL for module 2

**Software design**

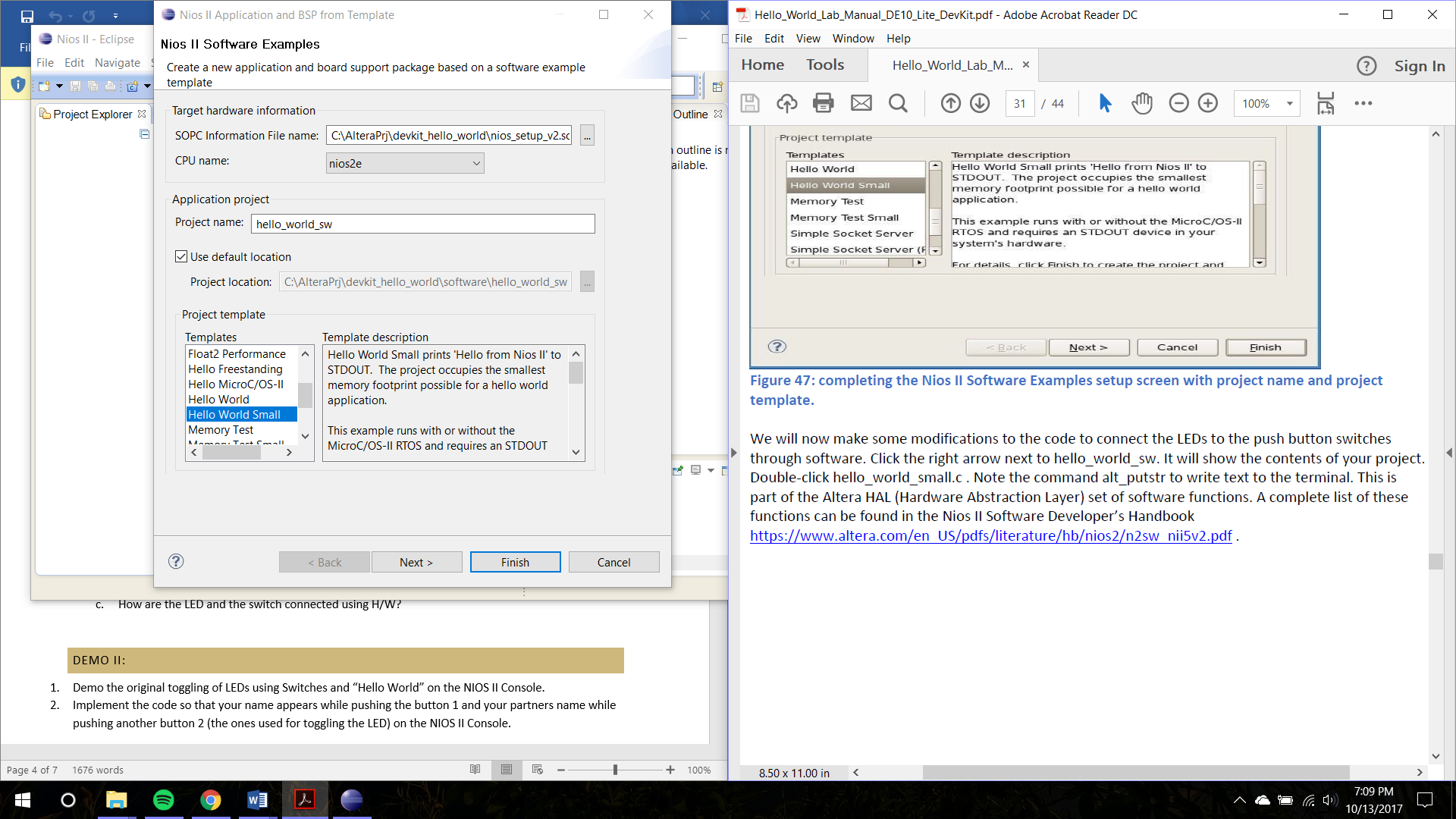


Fig 7. Setting up the software

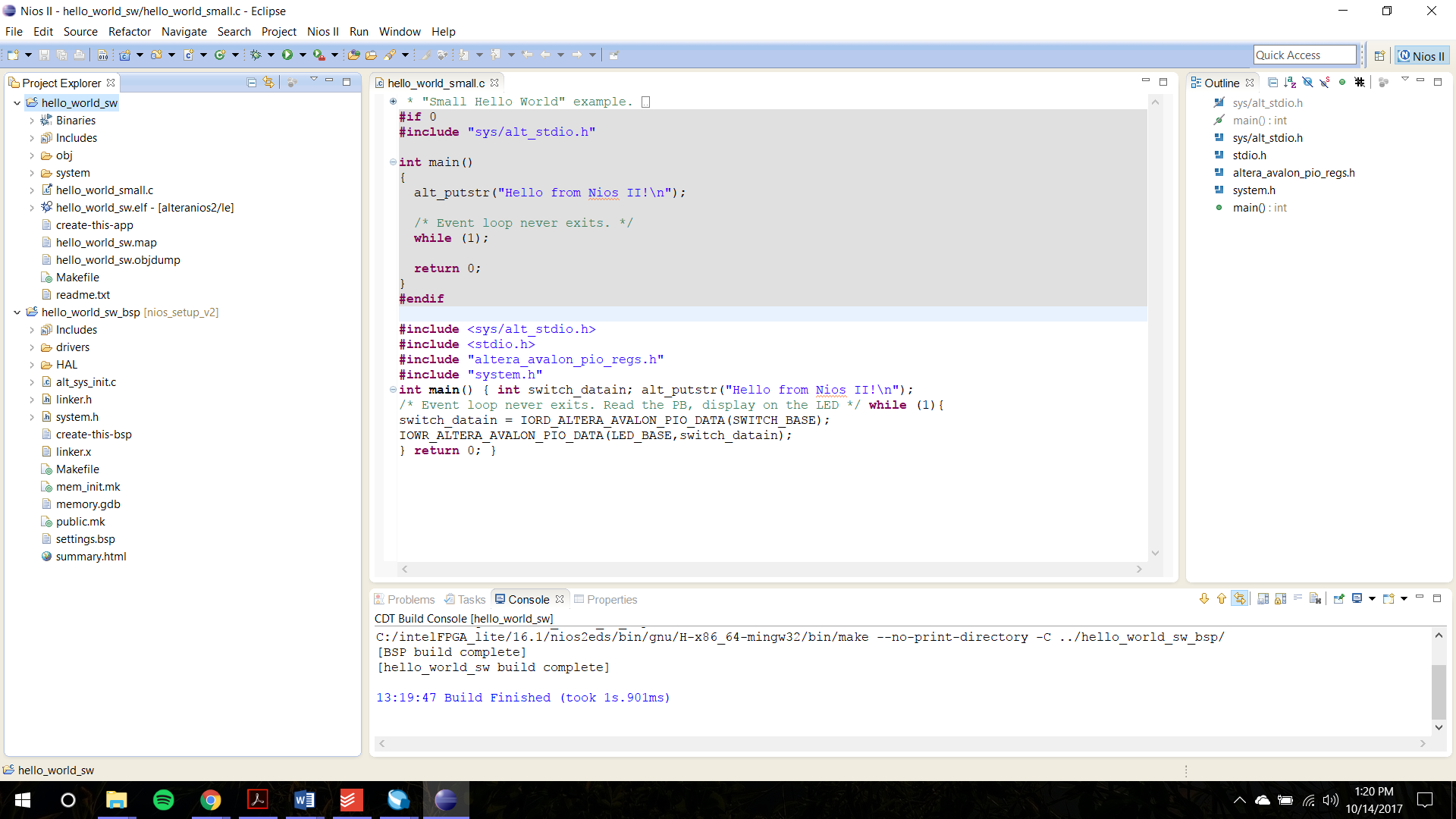


Fig 8. Successful build of the C Code

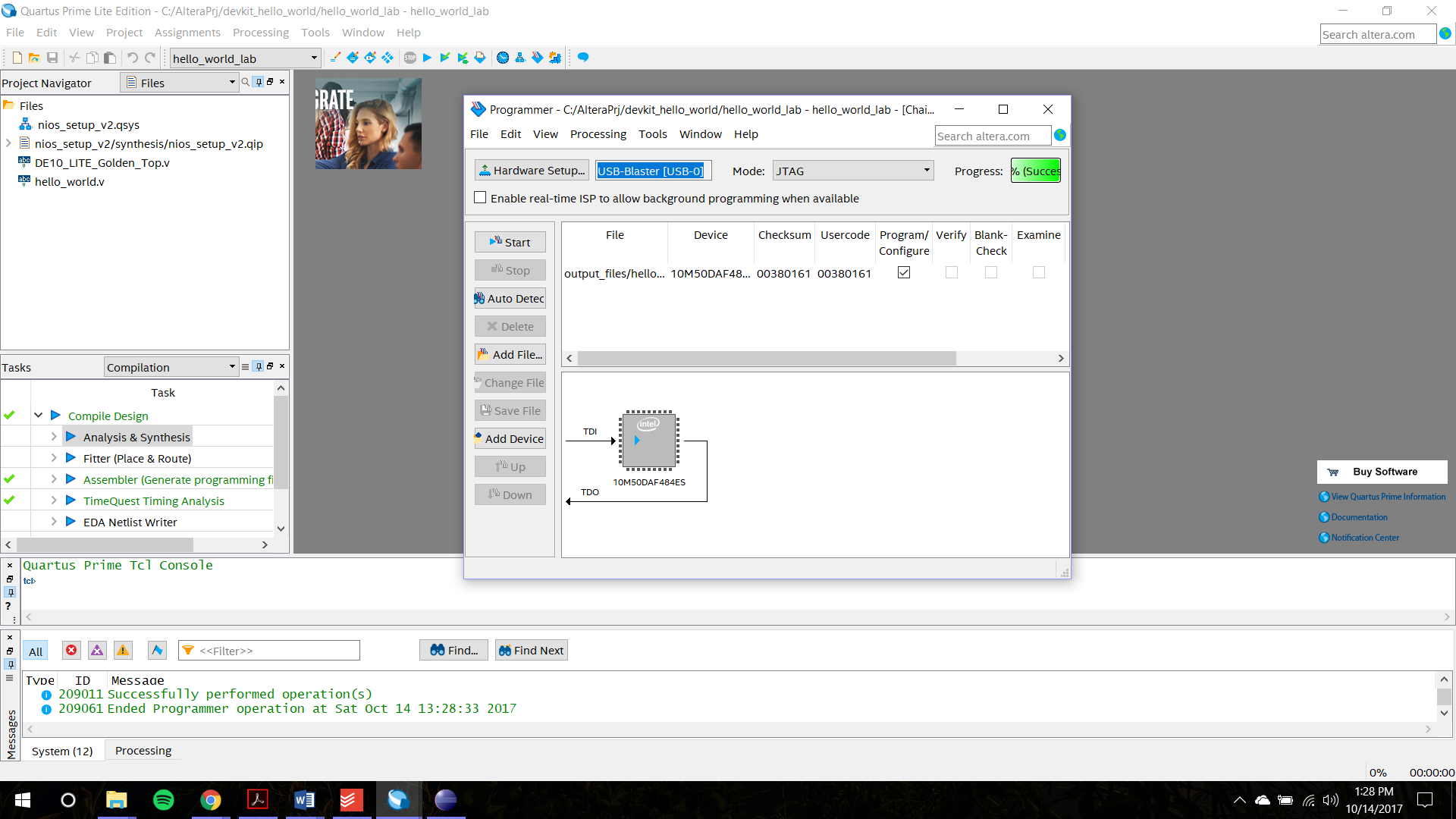


Fig 9. Programming the De10Lite

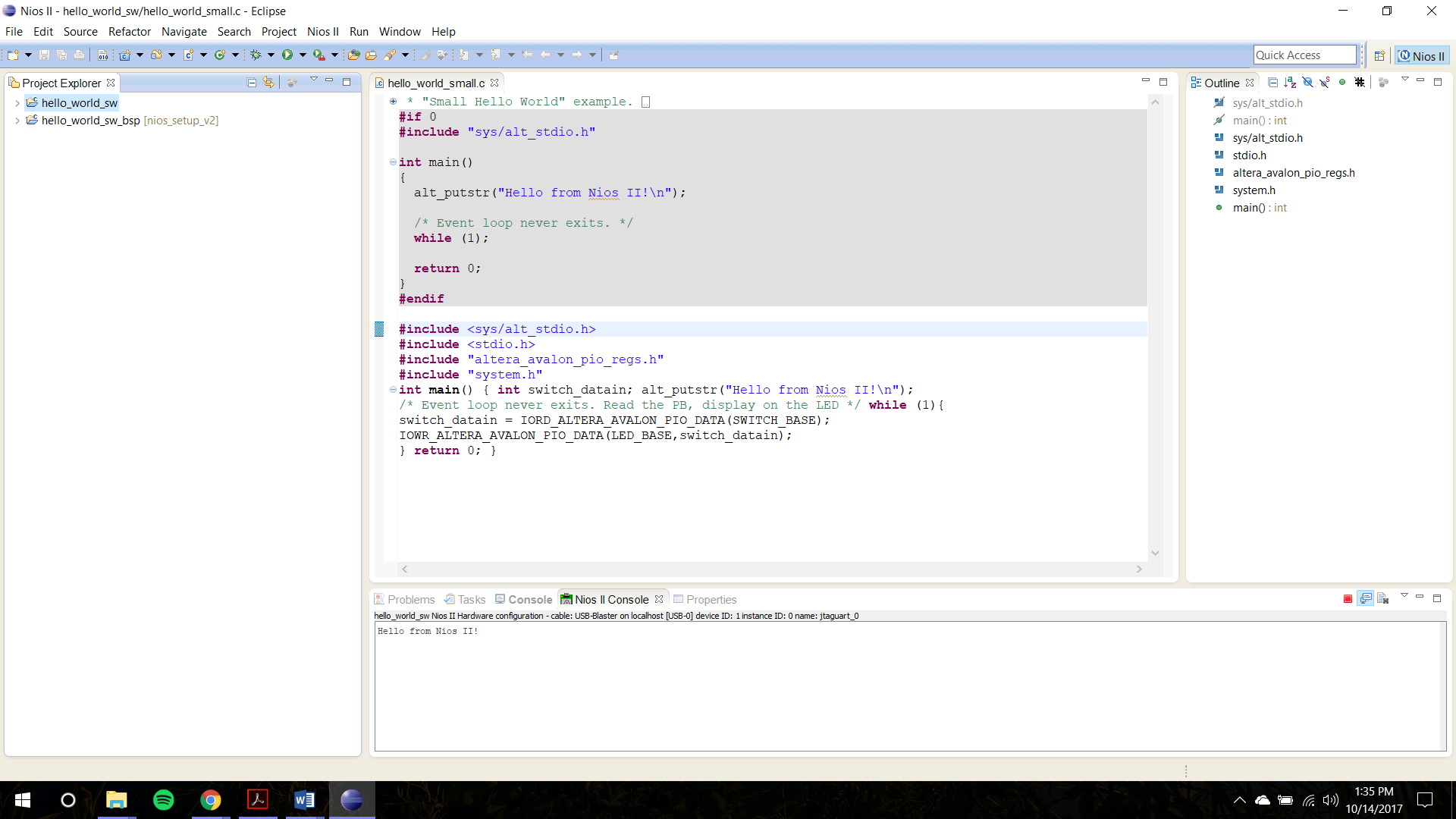


Fig 10. Successful output displayed in the console

**Demo part:**

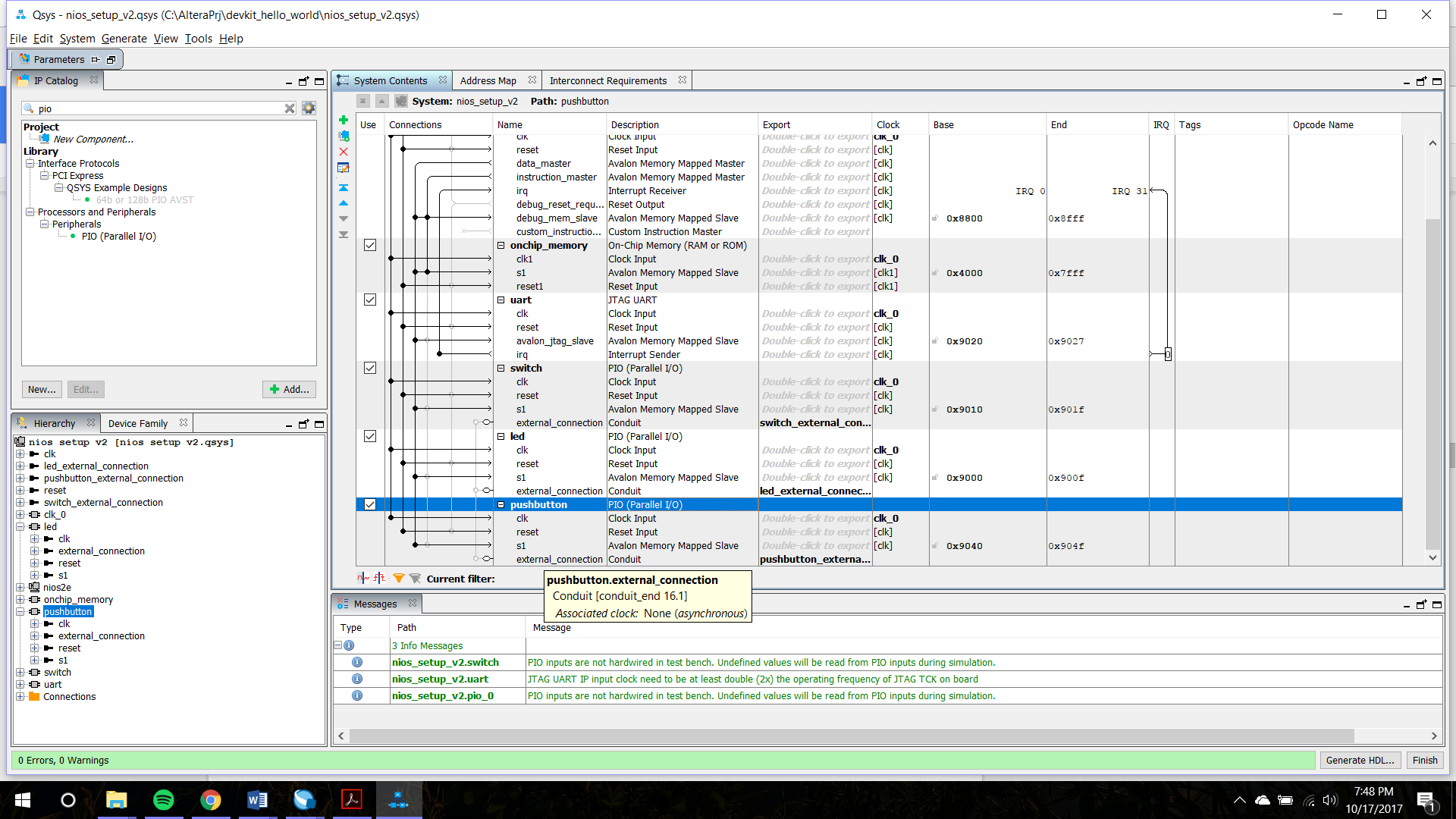


Fig 11. Qsys for the Demo

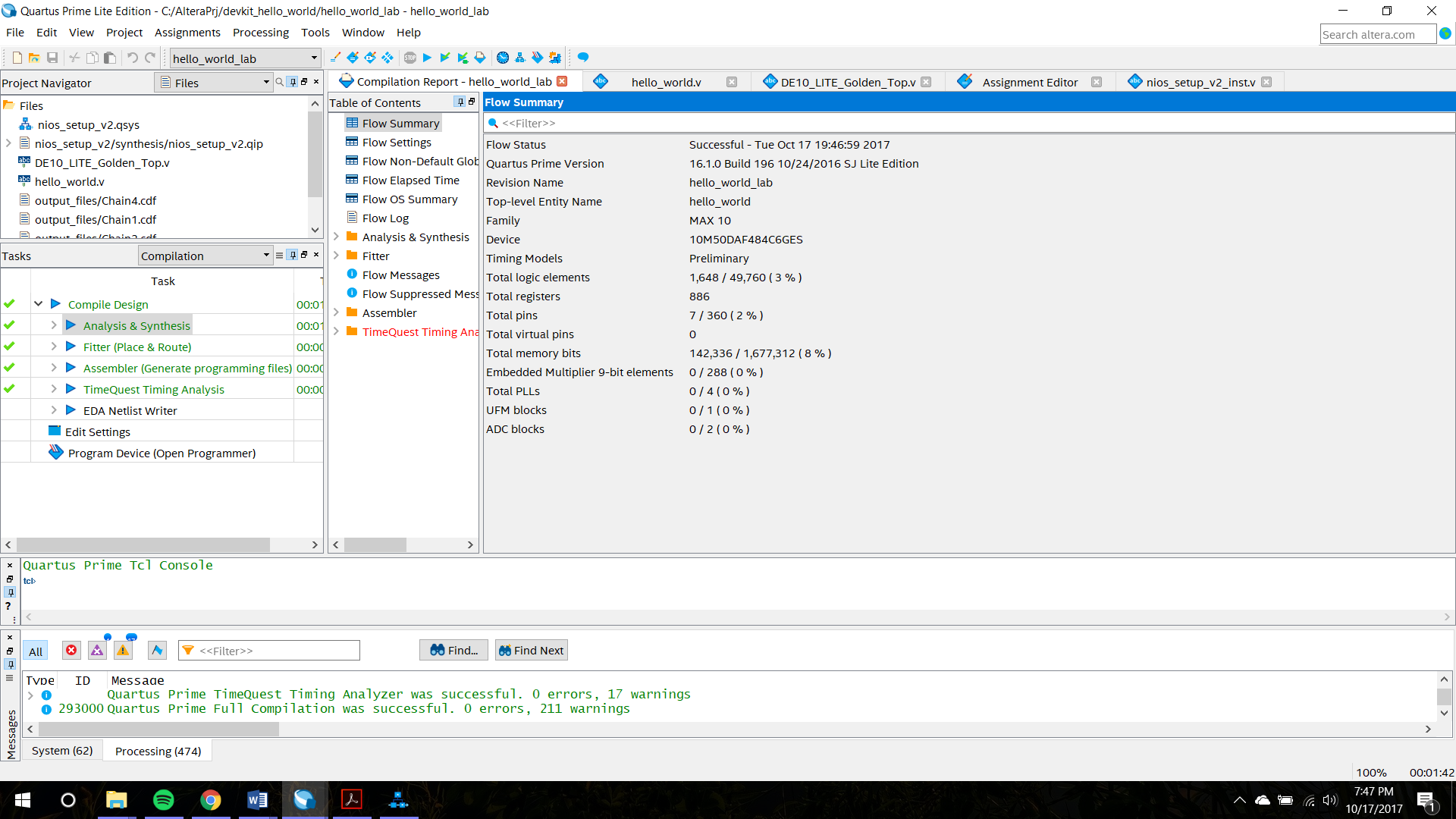


Fig 12 Compilation report for the demo

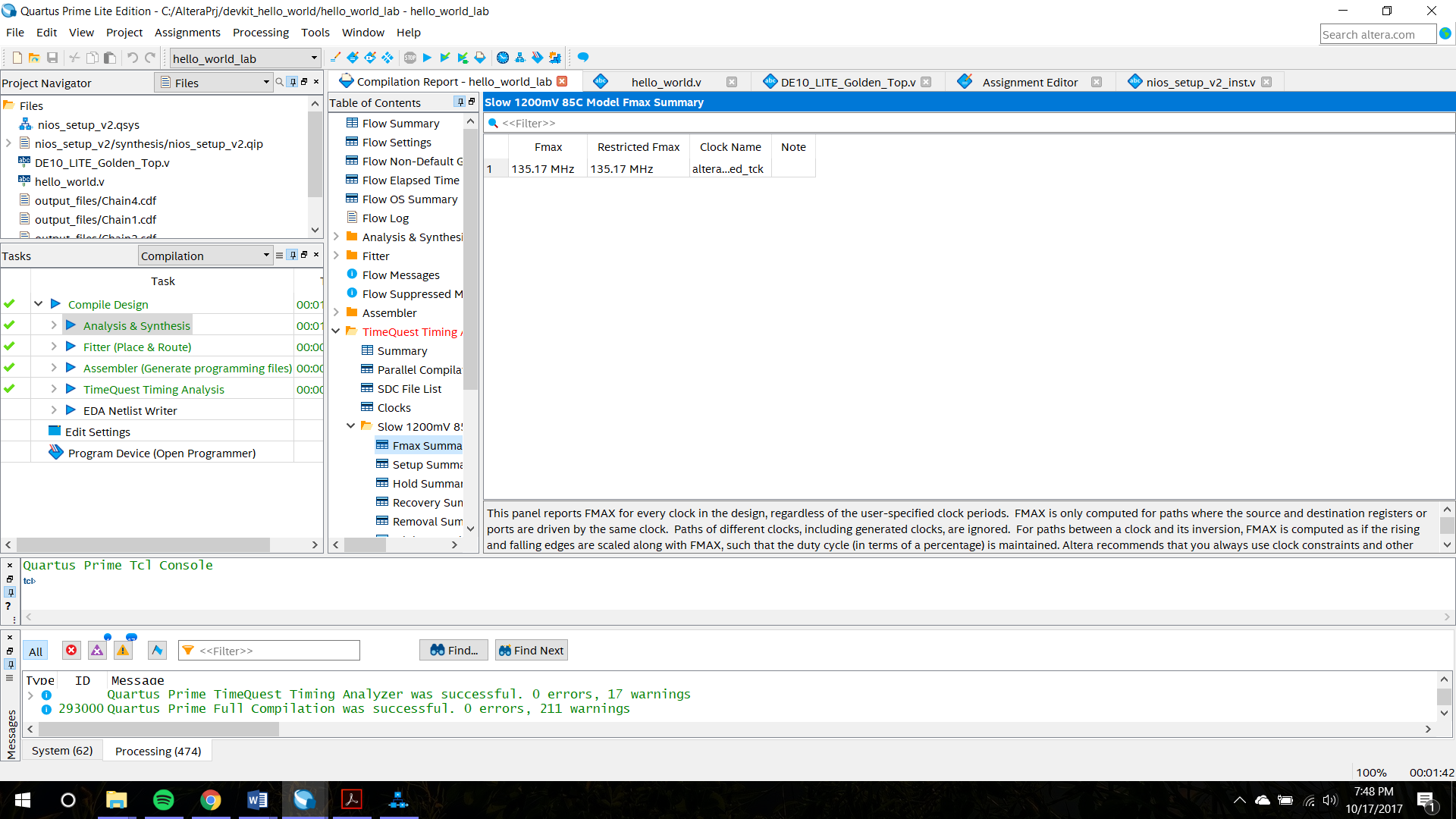


Fig 13 Fmax of the demo

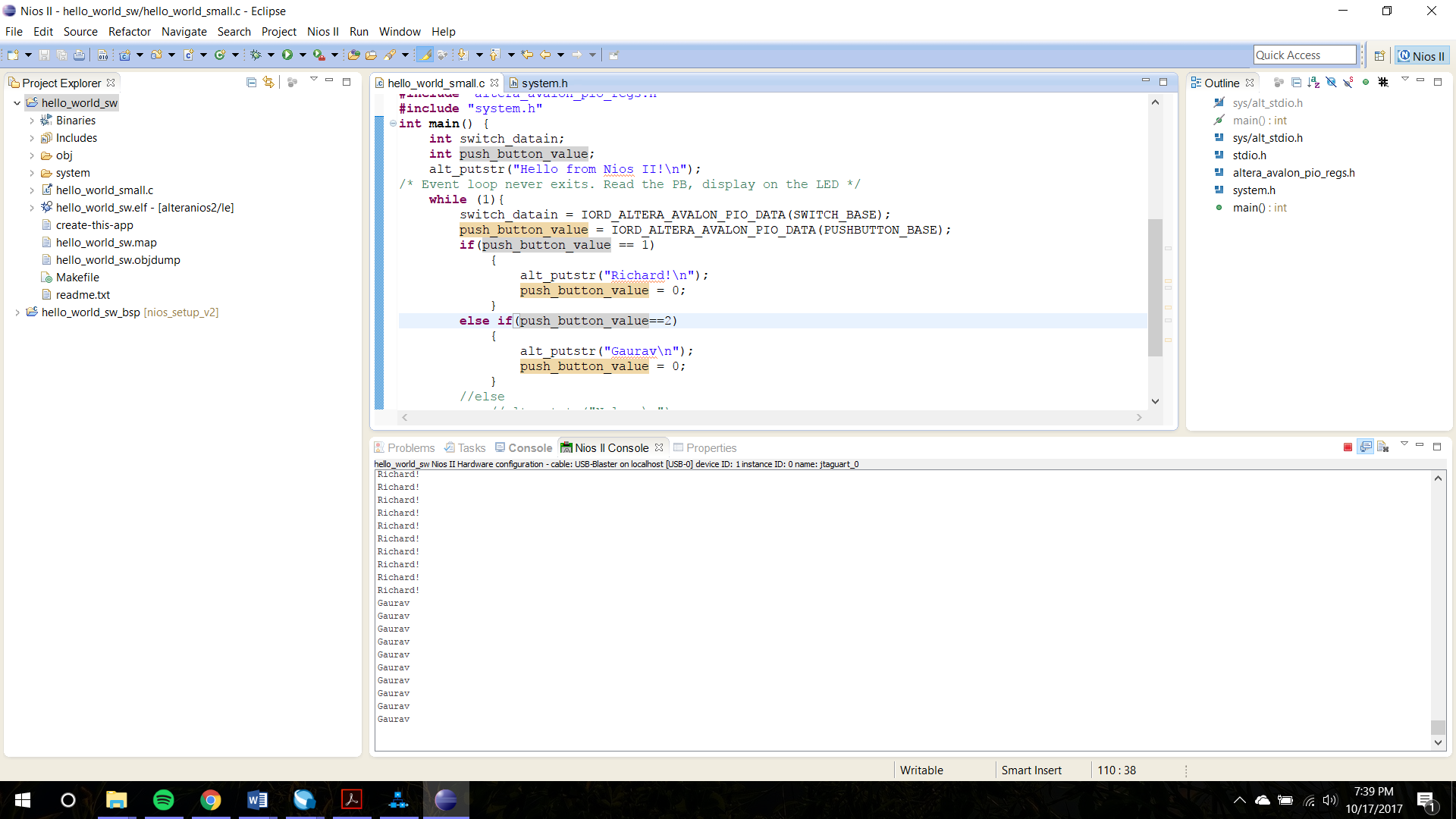


Fig 14. Successful output of the demo

**Module 3**

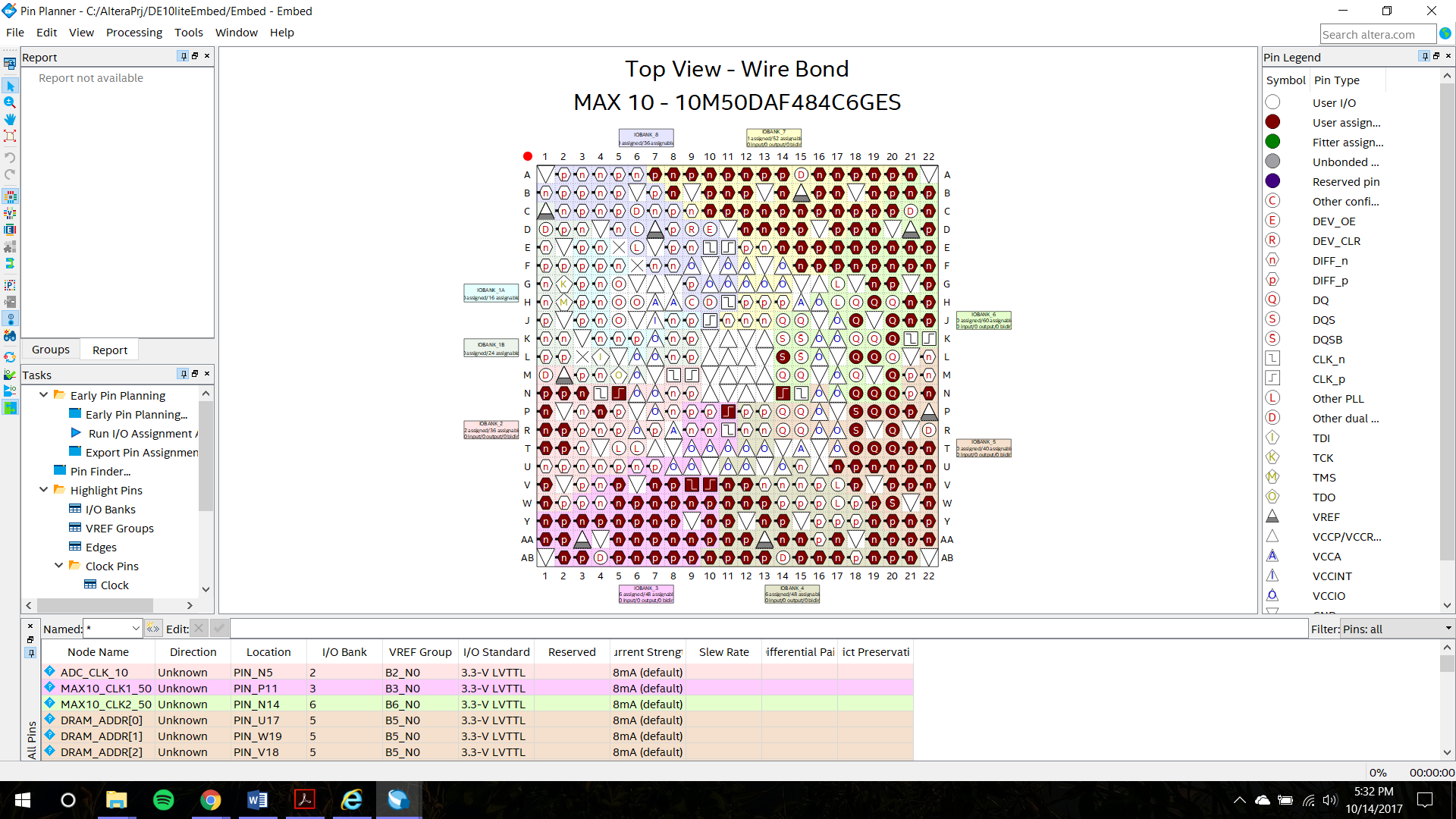


Fig 1. Wire bond view of the DE10Lite

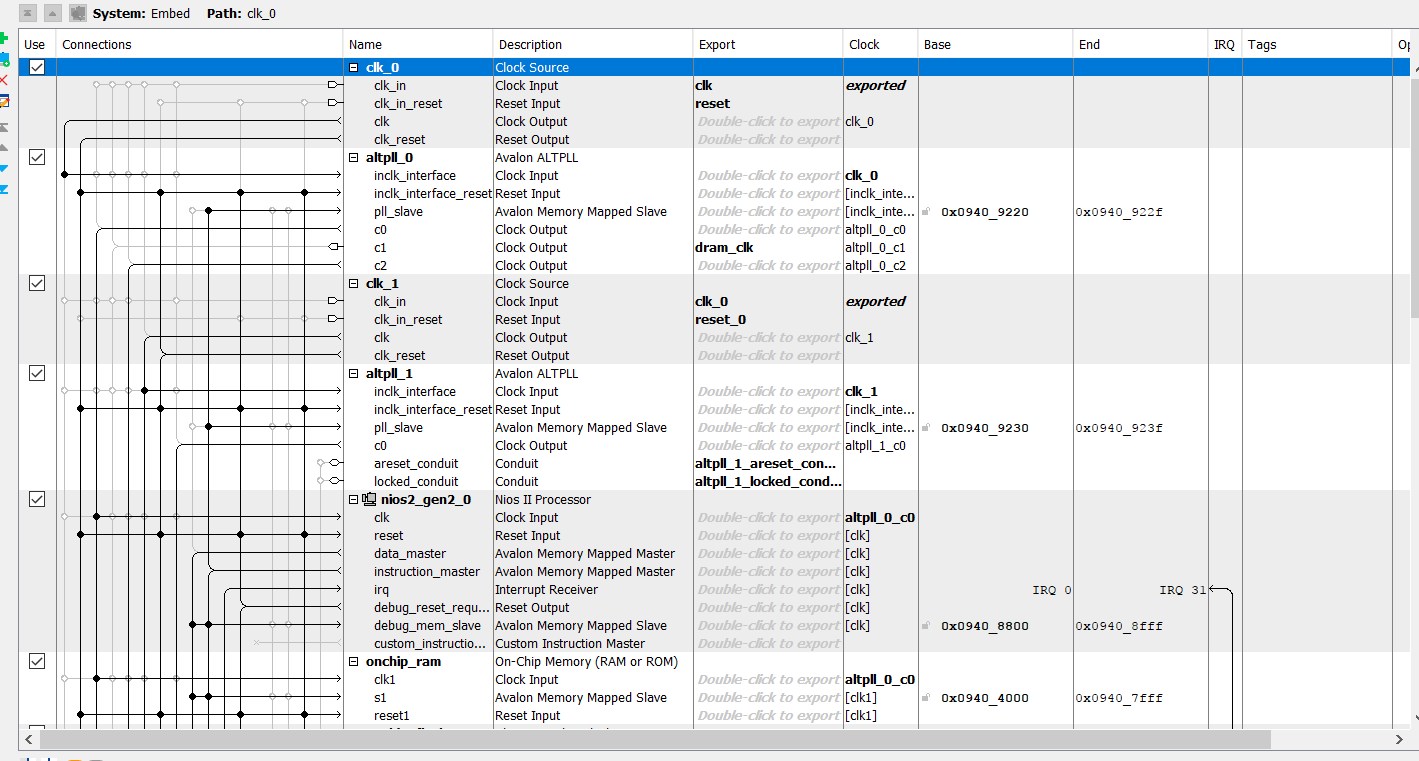


Fig 2. QSys for module 3

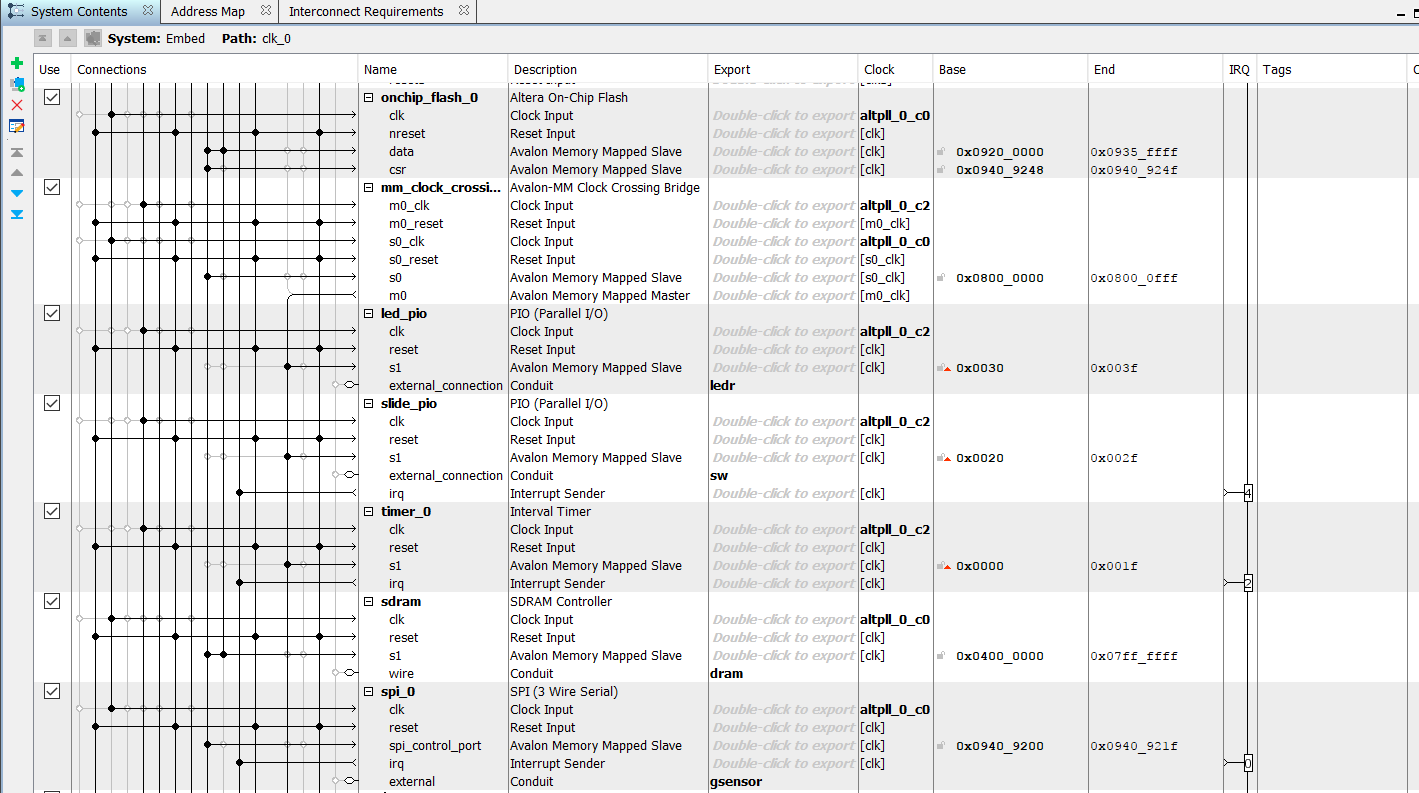


Fig 3. Qsys for module 3

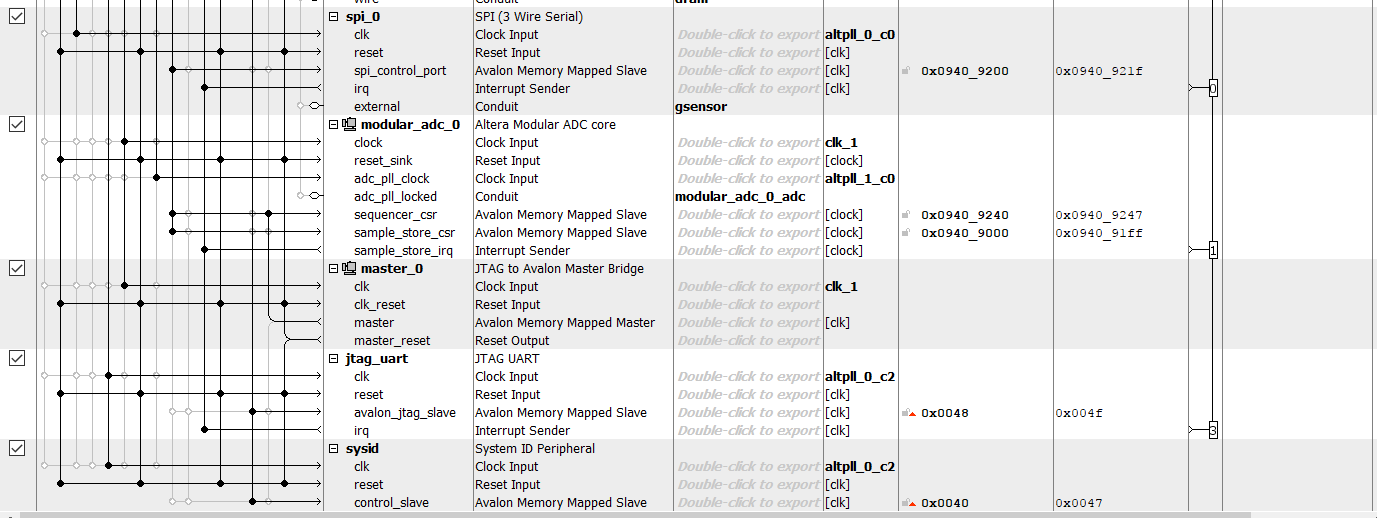


Fig 4 Qsys for module 3

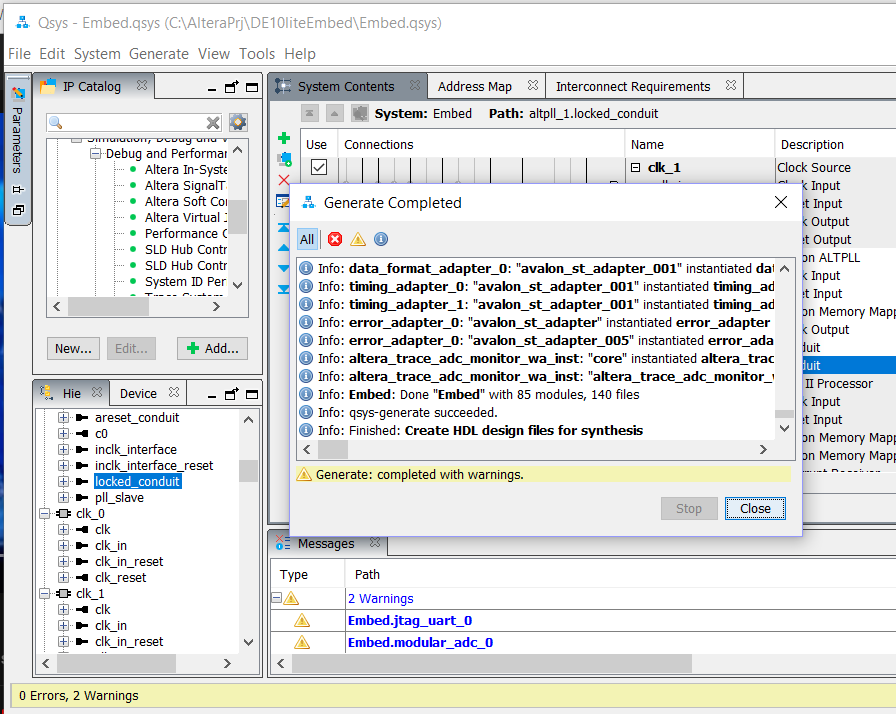


Fig 5. Successful generation of the HDL from Qsys

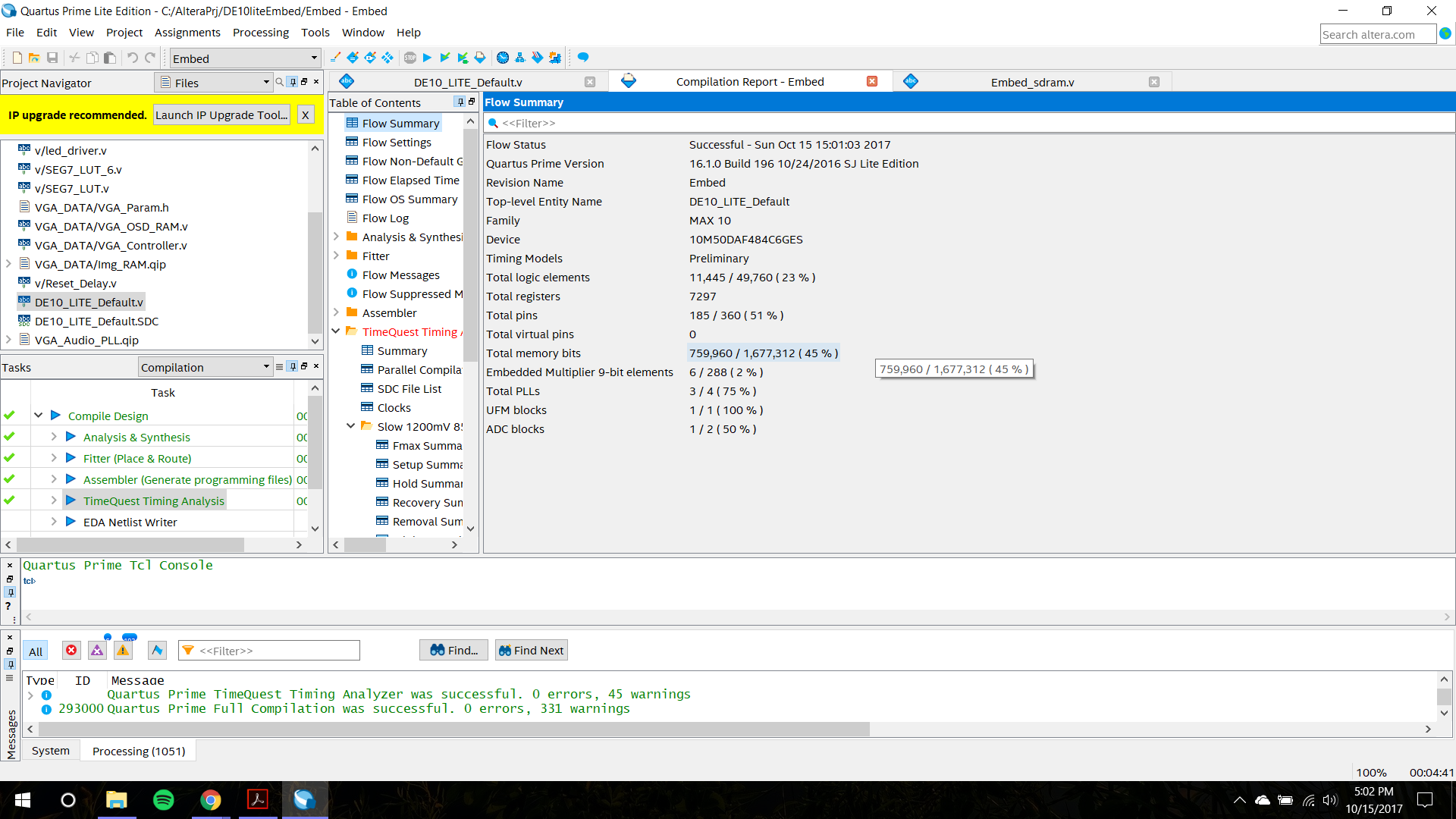


Fig 6. Compilation report for Module 3

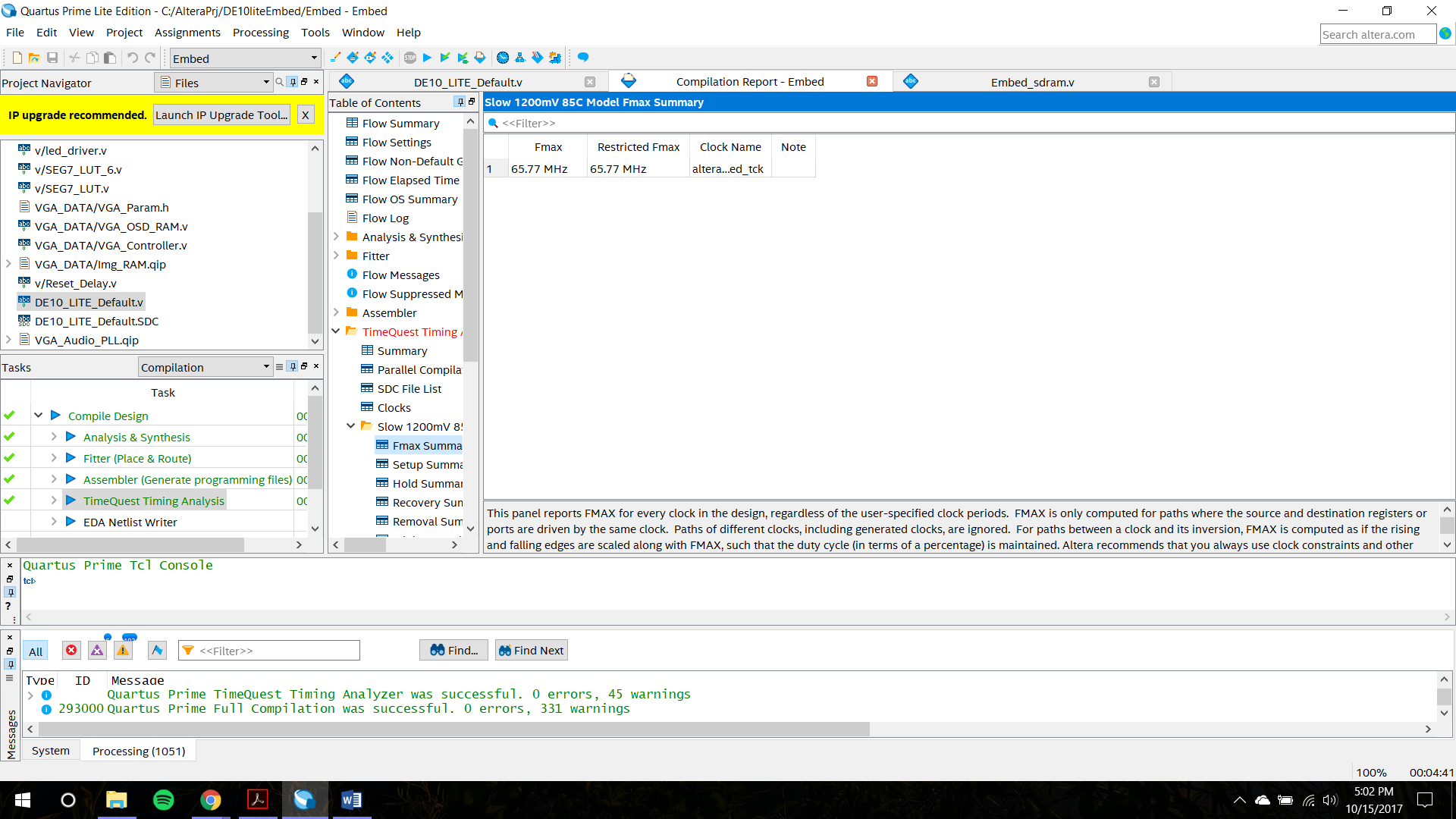


Fig 7. Compilation report for Module 3

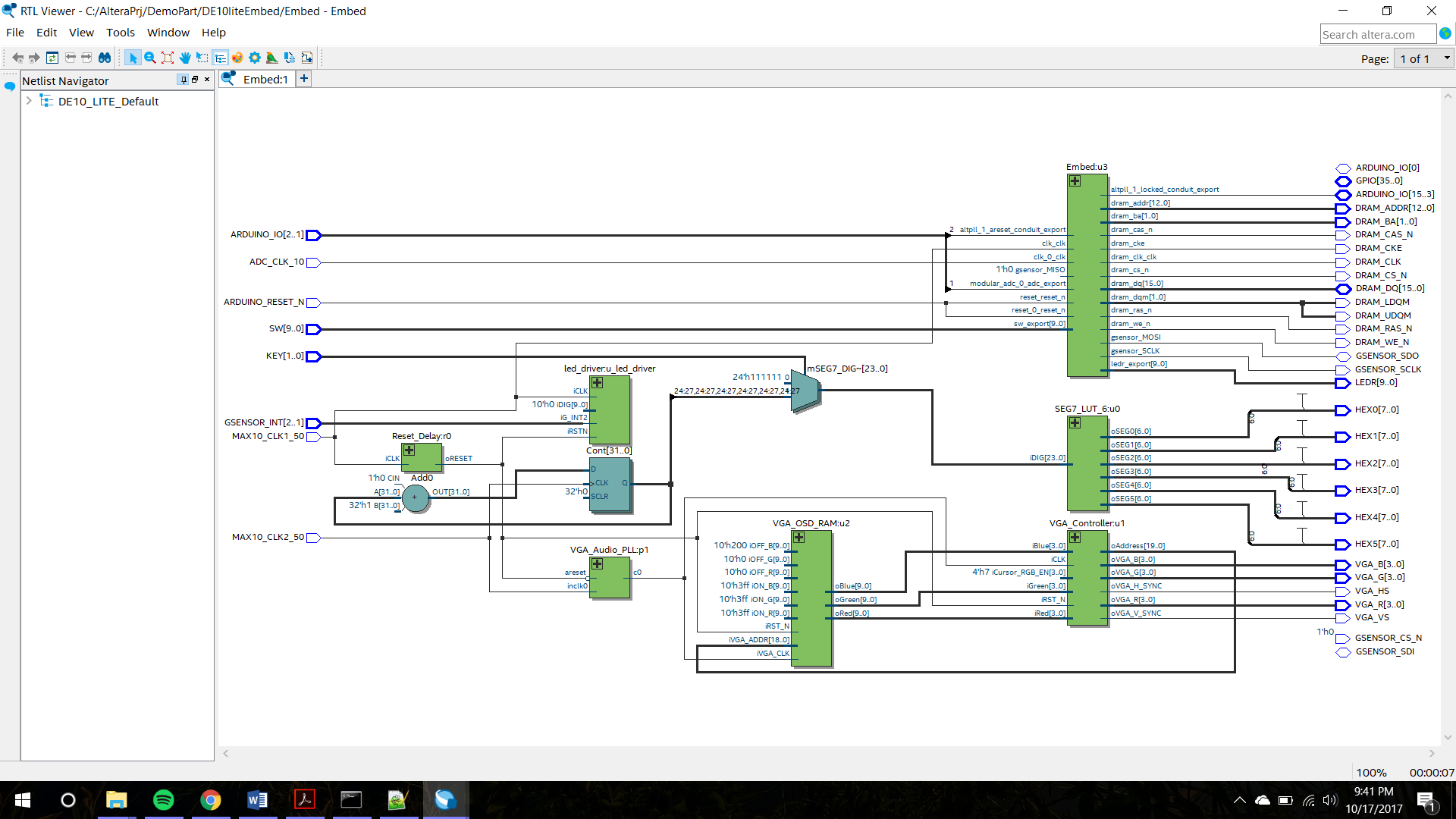


Fig 8. RTL of the system

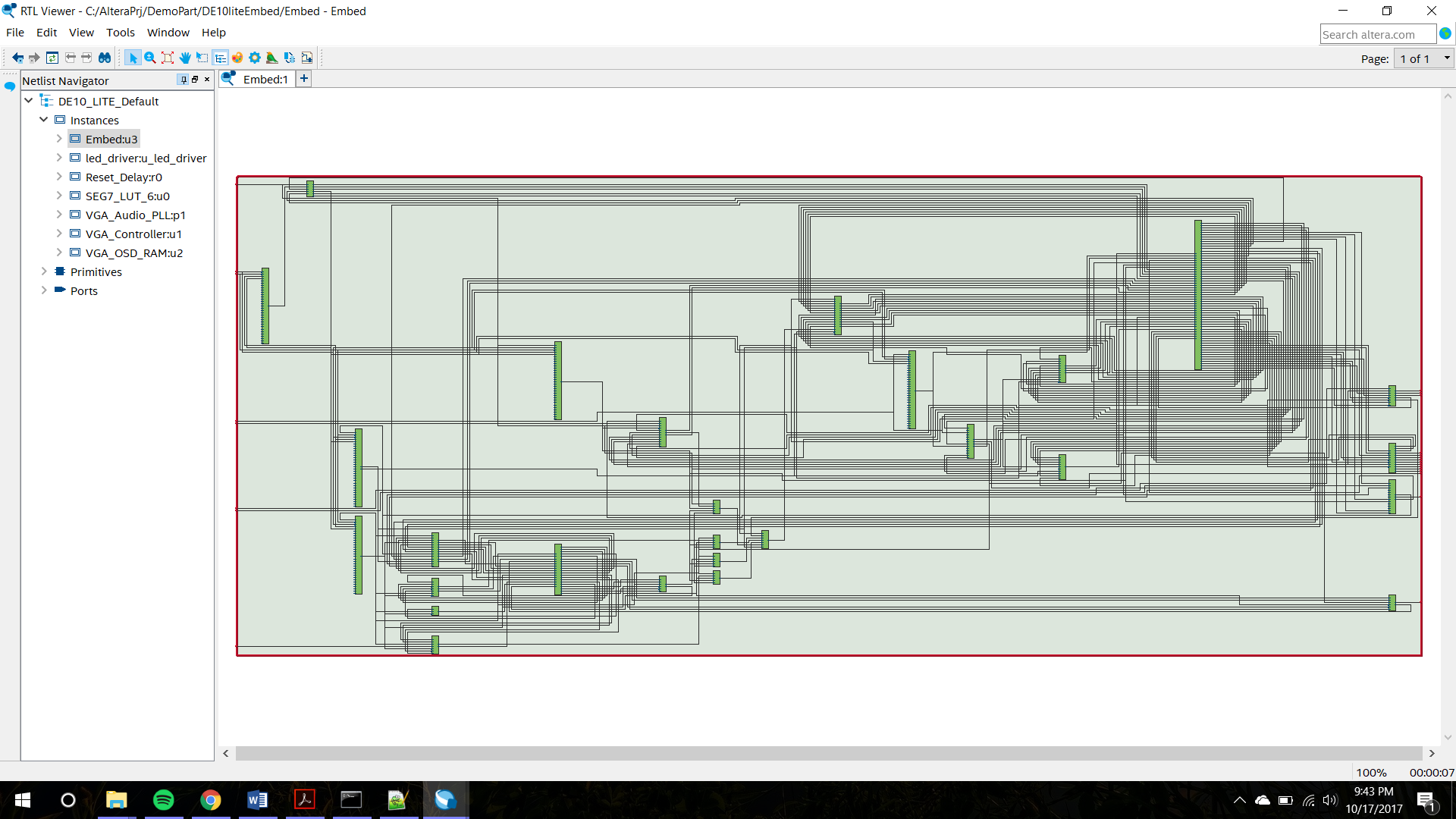


Fig 9. The NIOS II soft processor

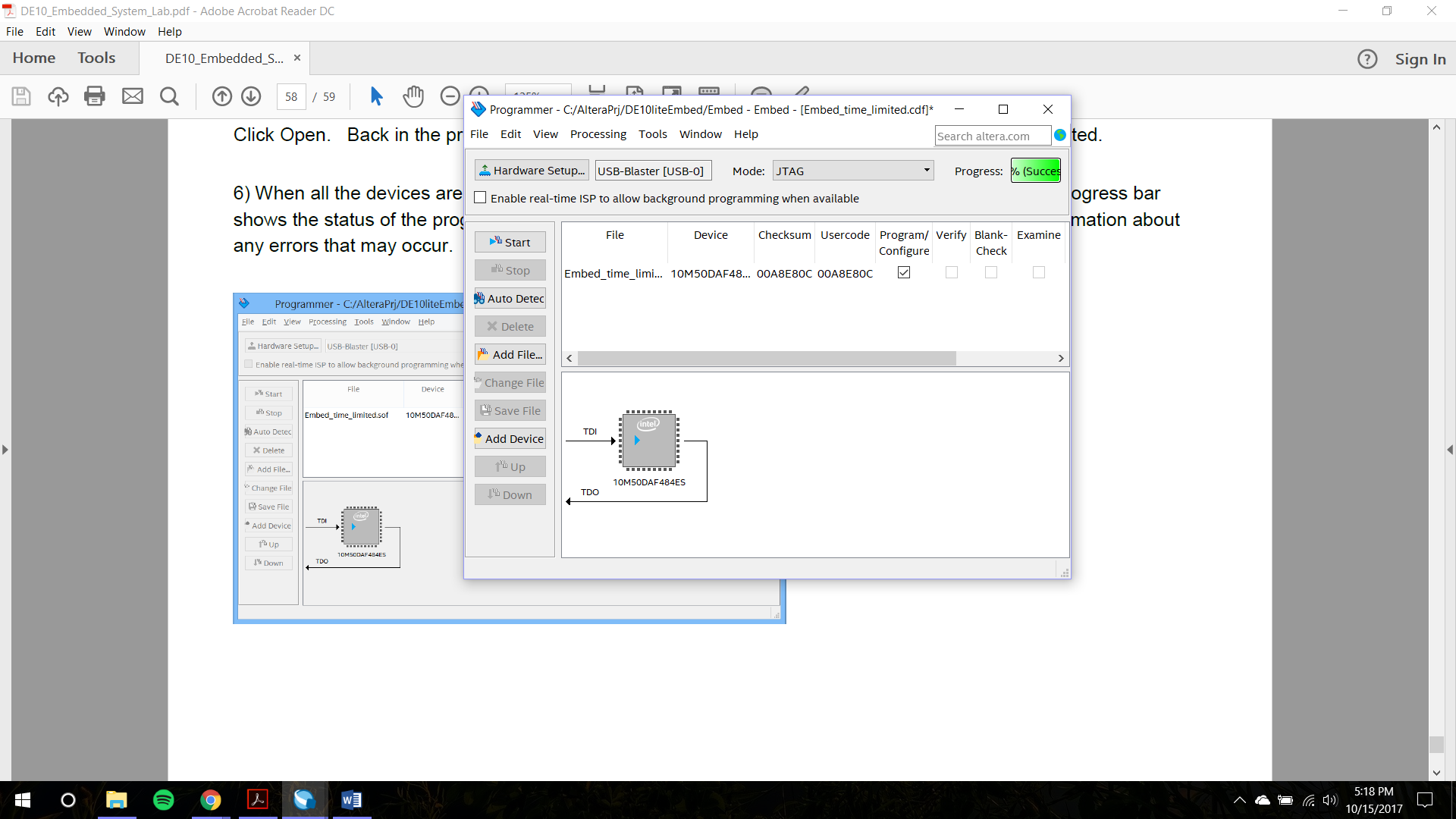


Fig 10. Successful programming of the De10Lite

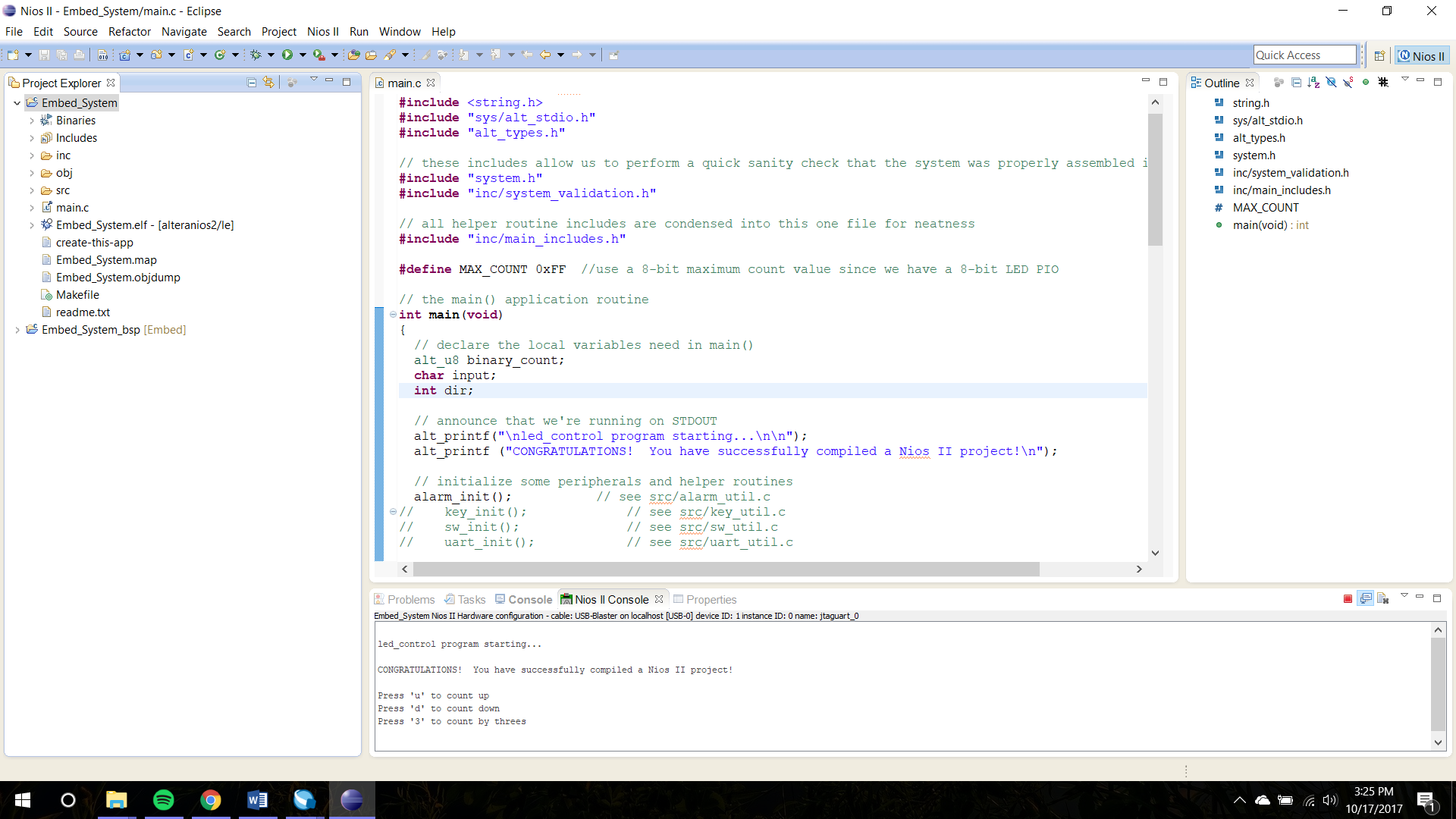


Fig 11. Successful output observed in the console

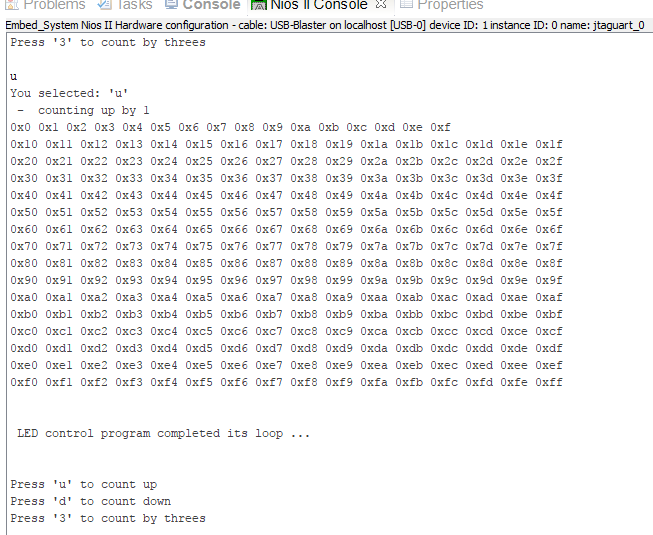


Fig 12. Output for the up counter

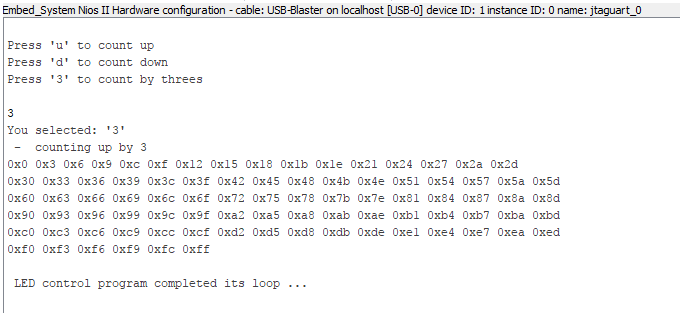


Fig 13. Counting by threes

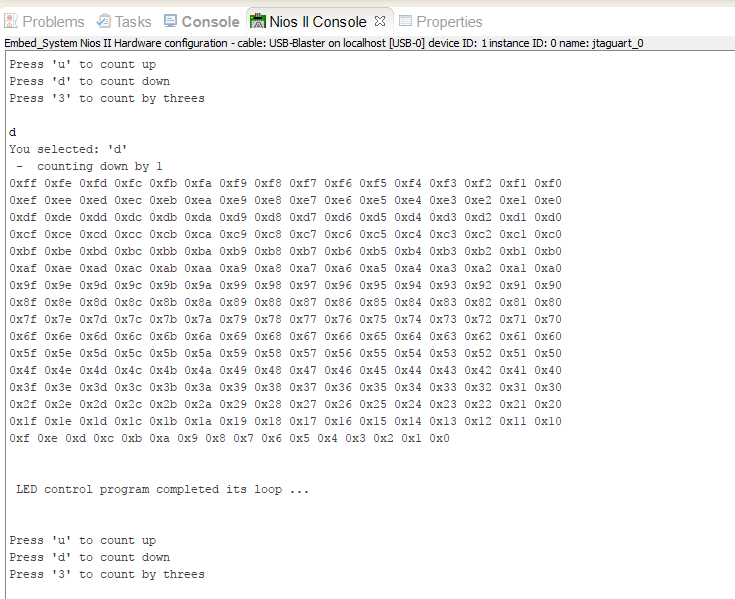


Fig 14. Downcounter

**Demo module 3**

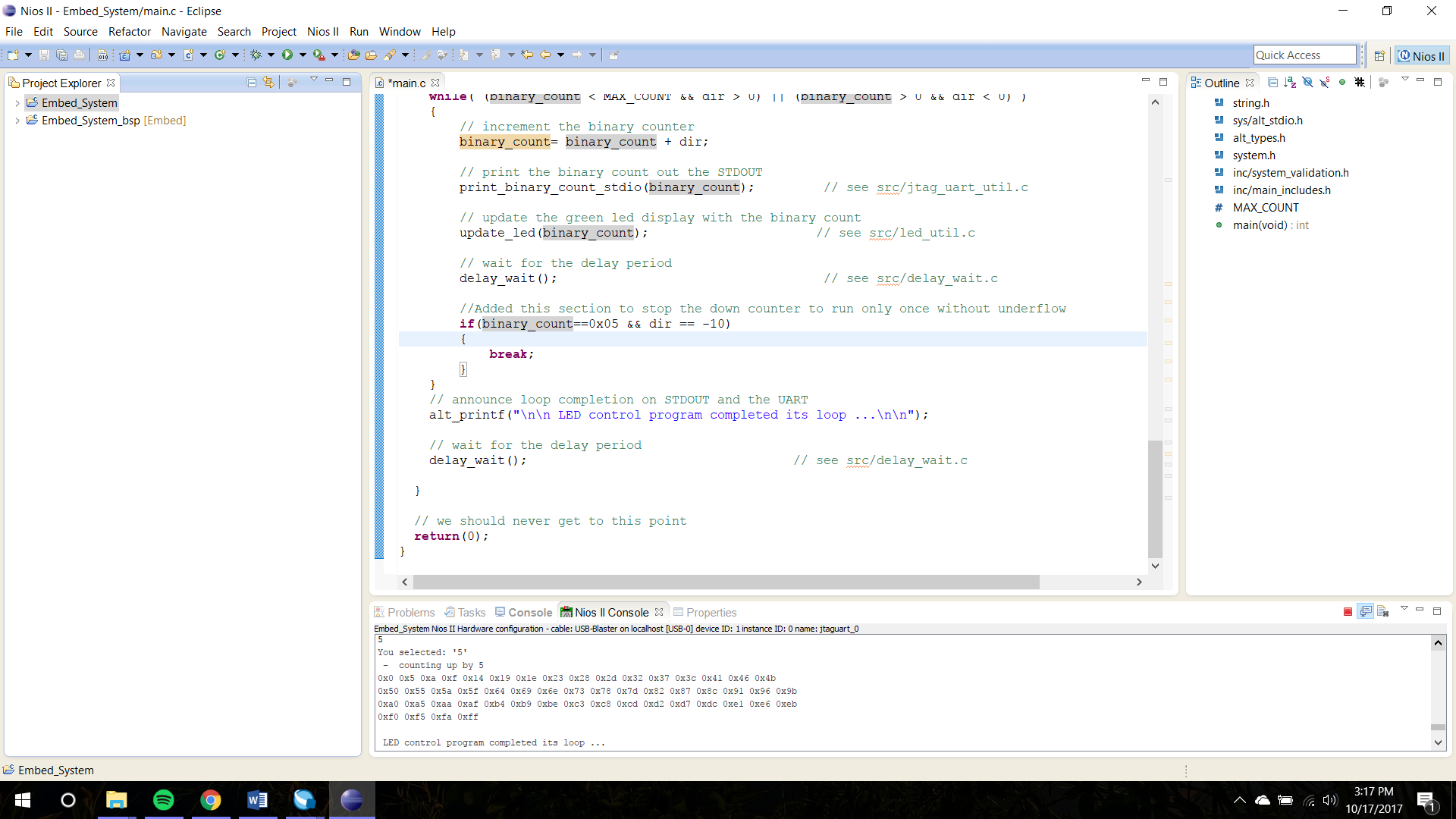


Fig 15 Up count by 5

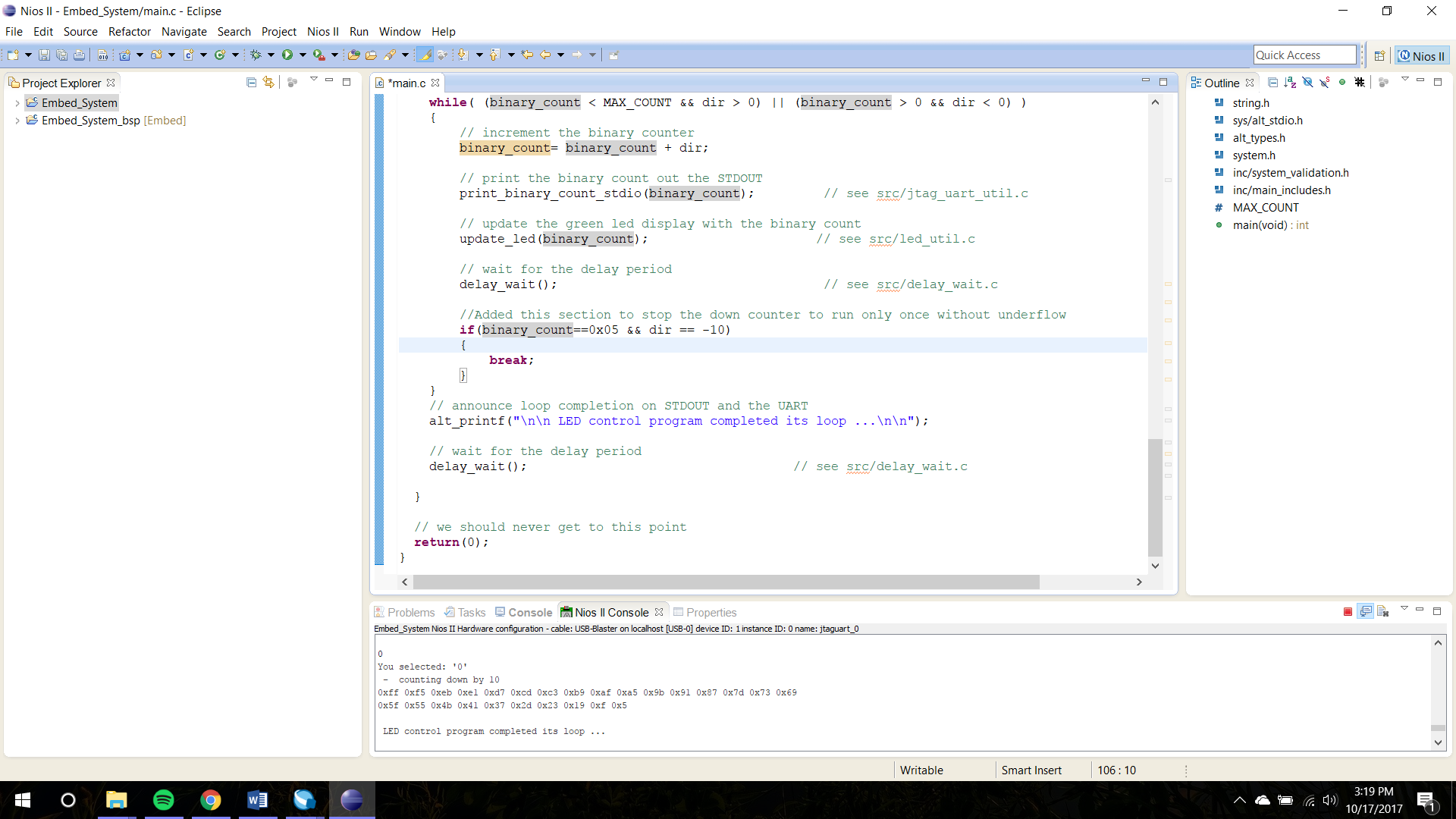


Fig 16. Down count by 10