

Figure , Pulse Width Modulation Block Diagram

Figure 1, shows the completed block diagram for the PWM. The PLL was created using Qsys and converted to block symbol. The debouncer and PWM generator were converted to block symbols using “Create Symbol File from Current File” in Quartus.

Connecting the circuits required using bus and node tool, and interfacing with the development kit required inserting input and output pins for the switch (SW), the LED (LEDR) and Arduino connector.

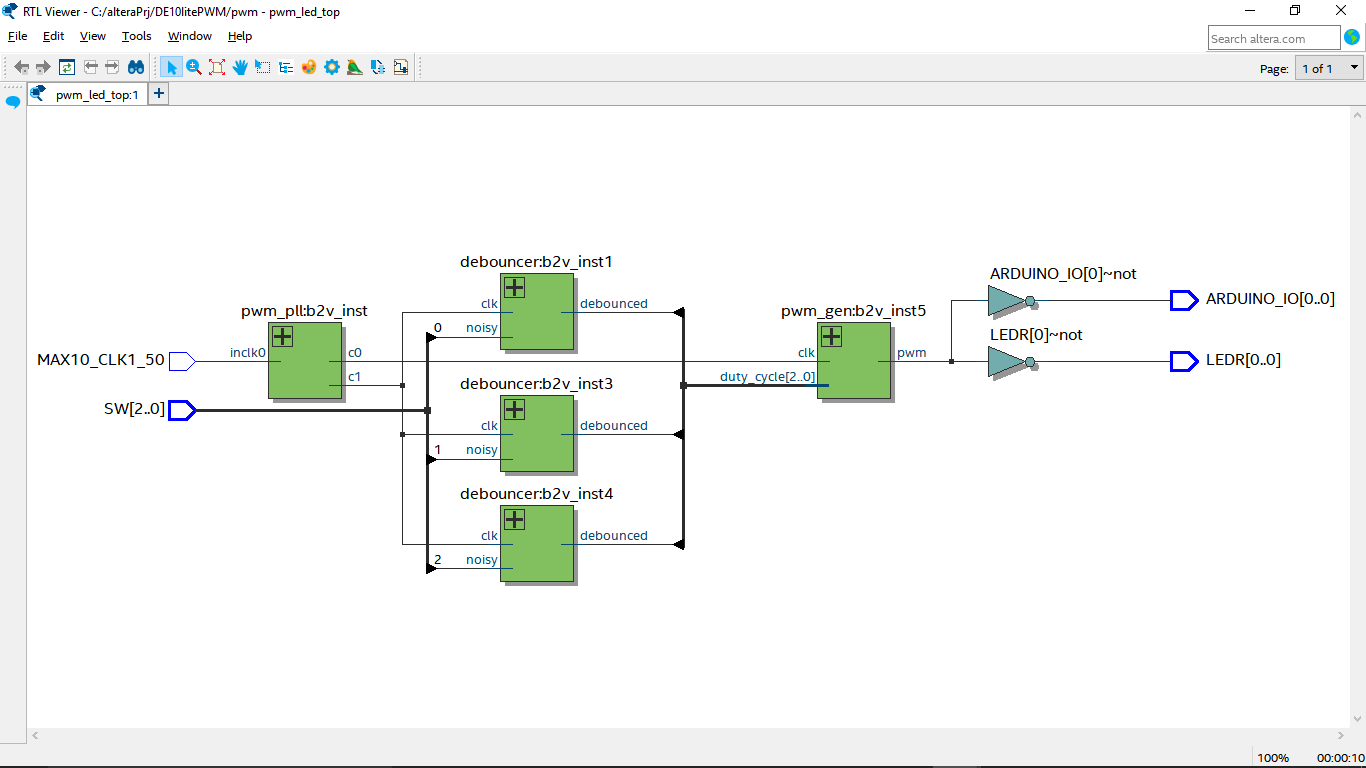


Figure , RTL of PWM circuit

The RTL schematic matches the block diagram.

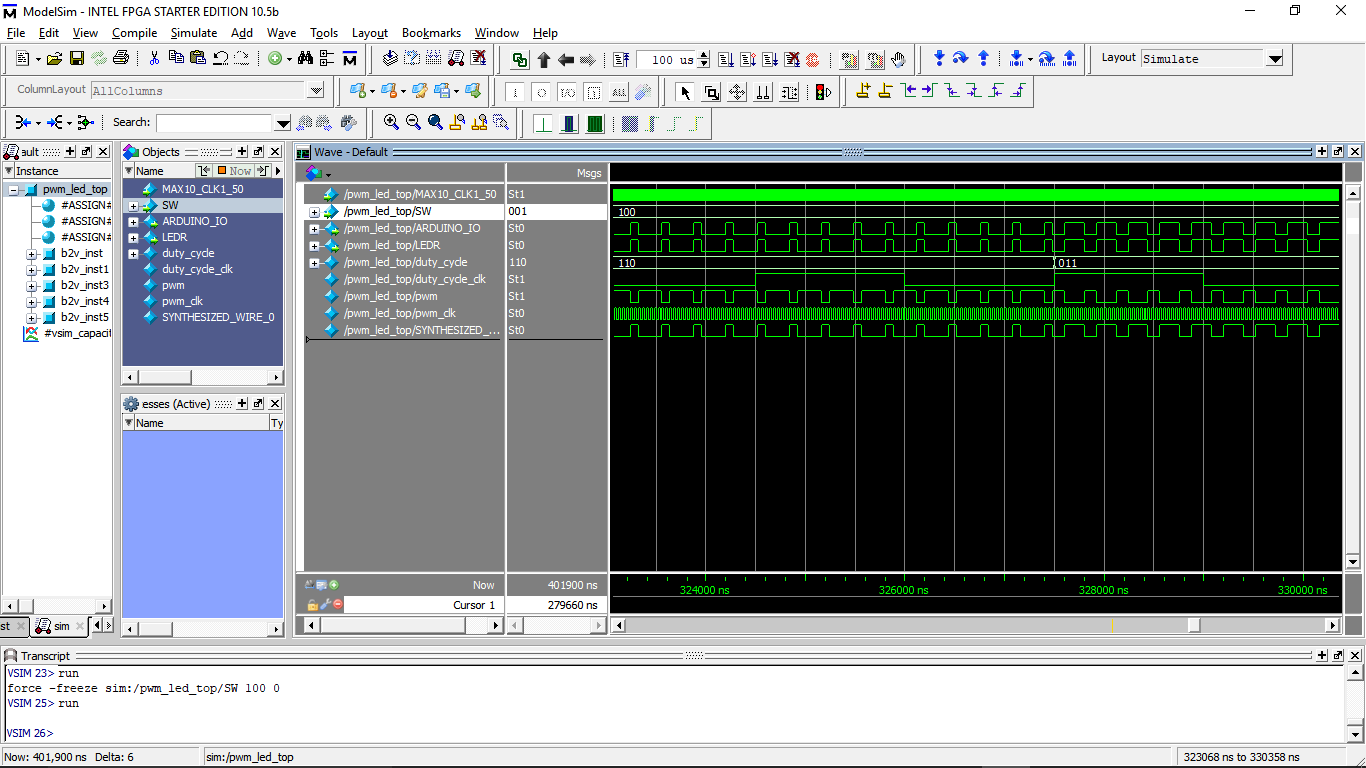


Figure , PWM simulation

This is a transition from switch settings (110 to 011). The new setting cause pulse width change.

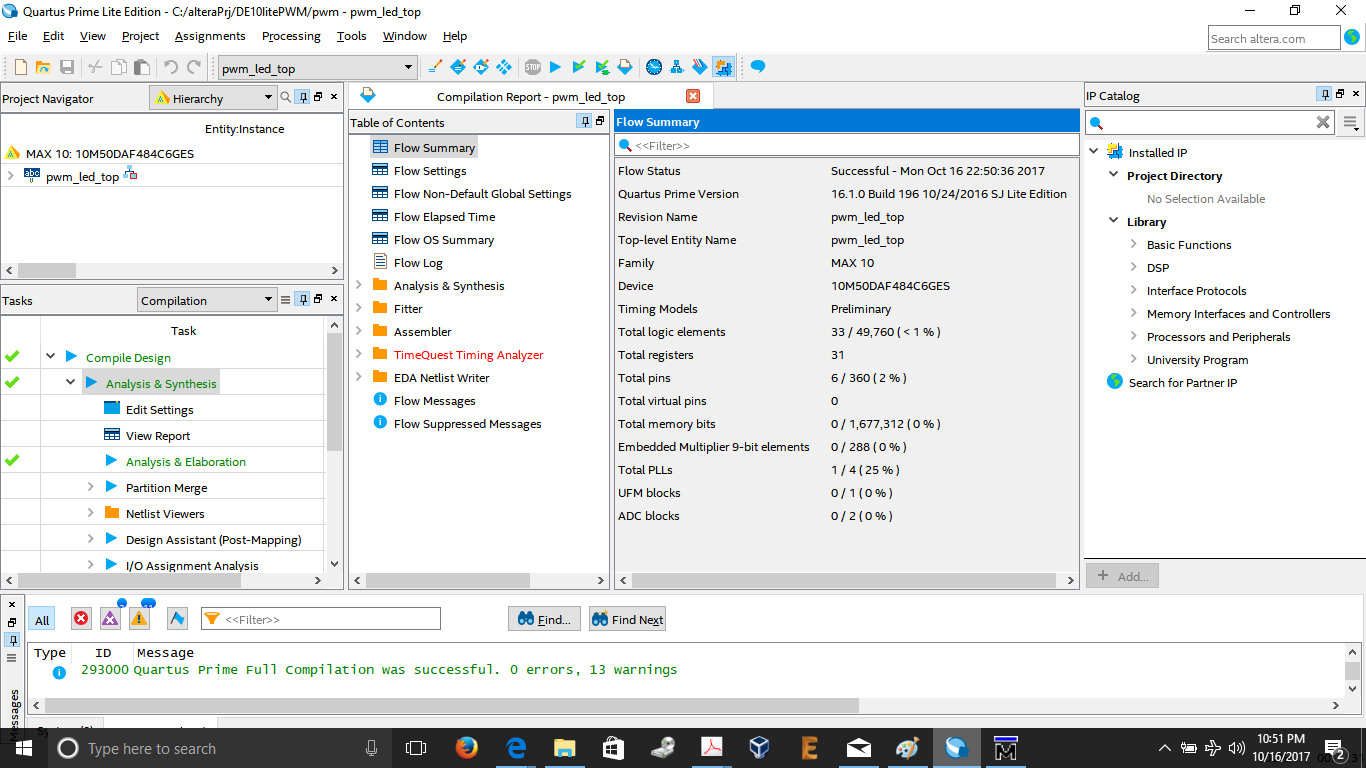


Figure , Compilation Complete

Figure 4, show the Flow Summary after the design was compiled. The Flow Summary shows the total logic elements used (<1%).

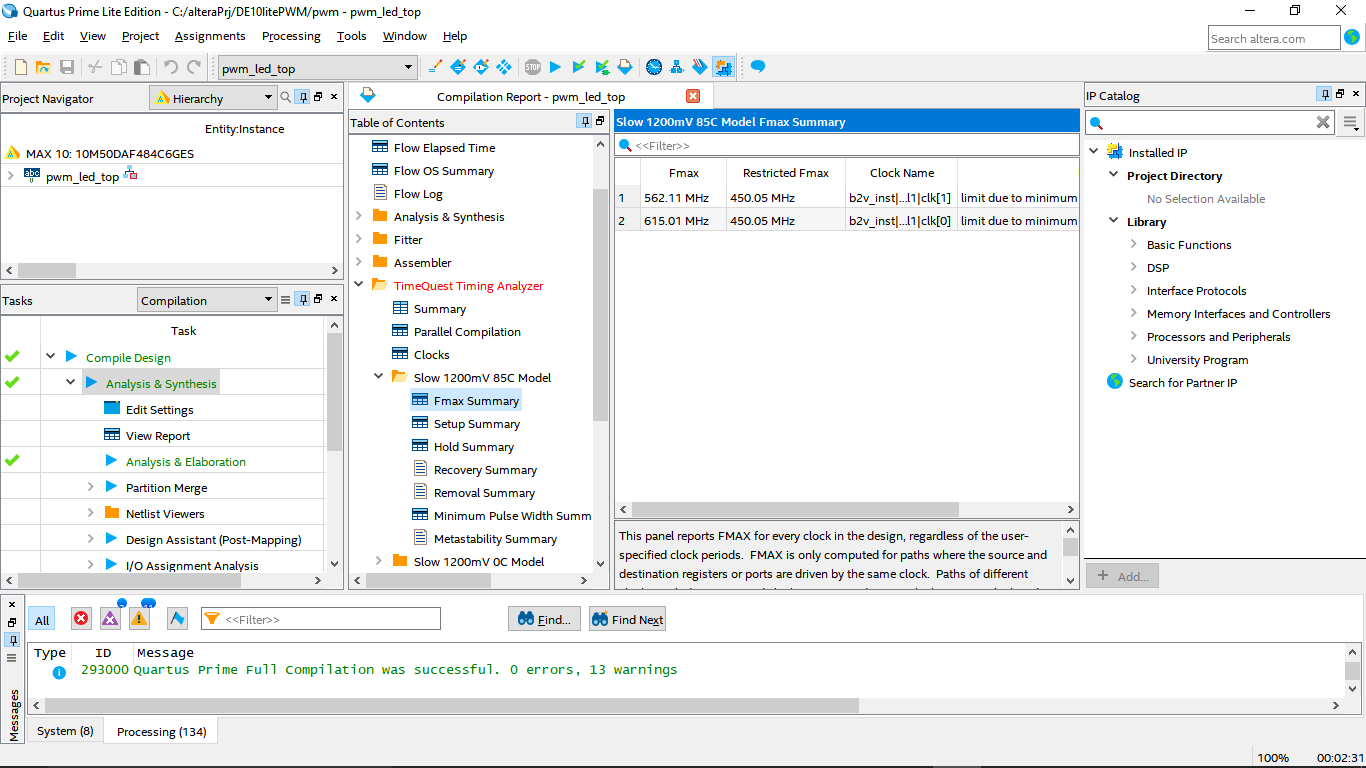


Figure , Slow 1200mV 85C Model Fmax Summary

Figure 5 shows the Fmax summary for the Slow 1200mV 85C model. For this design FMax is limited to 450.05 MHz.