Instituto Superior Técnico, University of Lisbon

Integrated Master in Aerospace Engineering

Circuit Theory and Electronics Fundamentals

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Fourth Laboratory Report

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Contents

1 Introduction

The objective of this laboratory assignment is to simulate a Band Pass Filter (BPF) using OPAMP as shown in Figure 1. We should have a central frequency of 1KHz and a 40 dB gain at the central frequency.

This way, we should choose its the architecture, considering the limitations imposed as well as the cost of the components in the circuit. Its diagram is shown in Figure 1.

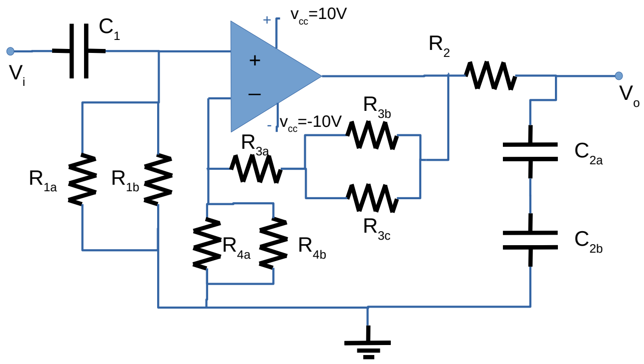


Figure 1: Band Pass Filter Circuit

This circuit is composed by 6 resistors, 3 capacitors and a 741 OPAMP. The values of the components are exhibited in the table below.

Name	Value
R_{1a}	1.000000e+03 Ohm
R_{1b}	1.000000e+04 Ohm
R_1	9.090909e+02 Ohm
R_2	1.000000e+03 Ohm
R_{3a}	1.000000e+05 Ohm
R_{3b}	1.000000e+05 Ohm
R_{3c}	1.000000e+05 Ohm
R_3	1.500000e+05 Ohm
R_{4a}	1.000000e+03 Ohm
R_{4b}	1.000000e+04 Ohm
R_4	9.090909e+02 Ohm
C_1	2.200000e-07 F
C_{2a}	2.200000e-07 Ohm
C_{2b}	2.200000e-07 Ohm
C_2	1.100000e-07 F

Table 1: Components Values

Notice that some components have been simplified by its equivalent (R_1, R_3, R_4 and C_2).

In Section 2, a theoretical analysis of the circuit, performed on Octave, is presented. In Section 3, the circuit is analysed by simulation, using NGSpice, and the results are compared to the theoretical results obtained in Section 2. The conclusions of this study are outlined in Section 4.

2 Theoretical Analysis

In this section, the circuit shown in Figure 1 is analysed theoretically. It is important to notice that the purpose is to build a band pass filter circuit using an OPAMP. This way, the considered circuit has a high pass filter, a signal amplifier (OPAMP) and a low pass filter in series, where the capacitor C1 and the resistor R1 act as a high pass filter, while the capacitor C2 and the resistor R2 function as a low pass filter.

Thus, We will begin by computing the gain, input and output impedances at the central frequency. Then, we will compute the frequency response Vo(f)/Vi(f) , using the incremental circuit, solving the circuit for a frequency vector in log scale with 10 points per decade, from 10Hz to 100MHz.

2.1 Gain, Input and Output Impedances at central frequency

In this subsection, we will compute the gain, input and output impedances at the central frequency.

First, we will calculate low and high cutoff frequencies, w_L and w_H, respectively, as well as central frequency, w_O, which are given by:

$$w_L = \frac{1}{R_1 \cdot C_1} \tag{1}$$

$$w_H = \frac{1}{R_2 \cdot C_2} \tag{2}$$

$$w_O = \frac{1}{\sqrt{w_L \cdot w_H}} \tag{3}$$

Their values are presented in the table below:

Name	Value
w_L	5.000000e+03 rad/s
w_H	9.090909e+03 rad/s
w_O	6.741999e+03 rad/s
f_O	1.073022e+03 Hz

Table 2: Frequencies

As we can see, our central frequency is very close to 1KHz, as requested.

Now we can determine the gain at central frequency, wich is given by the following equation:

$$T_{w_O} = \frac{R_1 \cdot C_1 \cdot jw_O}{1 + R_1 * C_1 * jw_O} \cdot (1 + \frac{R_3}{R_4}) \cdot \frac{1}{1 + R_2 \cdot C_2 \cdot jw_O} \tag{4}$$

As well as Z_{in} and Z_{out}, at the central frequency, are determined by:

$$Z_{in} = R_1 + \frac{1}{jw_O * C_1} \tag{5}$$

$$Z_{out} = R_2 \cdot \frac{\frac{1}{jw_O * C_2}}{R2 + \frac{1}{jw_O * C_2}} \tag{6}$$

The results are shown in tables 3 and 4:

Name	Value
Z_{in}	9.090909e+02 + j-6.741999e+02 Ohm
Z_{out}	6.451613e+02 + j-4.784644e+02Ohm
$\lvert Z_{in}\rvert$	1.131809e+03 Ohm
$\lvert Z_{out}\rvert$	8.032193e+02 Ohm

Table 3: Impedances at central frequency

Name	Value
AV_{HP}	-1.903317e+00 dB
AV_{OPAMP}	4.440216e+01 dB
AV_{LP}	-1.903317e+00 dB
AV	4.059553e+01 dB

Table 4: Gain at central frequency

,where AV_{HP}, AV_{OPAMP}, AV_{LP}, AV correspond to the high pass, OPAMP, low pass and final gain.

It is important to remember that the input impedance should be higher as possible to have a minimum input signal degradation, and output impedance should be close to null. This target became hard to achieve because of the limitations imposed on the circuit components. That's why our output impedance presents a too high value.

As also requested, we can observe that the circuit has a gain close to 40 dB.

Table 5 presents the same gain results, but considering, this time, a central frequency of 1KHz.

Name	Value
AV_{HP}	-2.130546e+00 dB
AV_{OPAMP}	4.440216e+01 dB
AV_{LP}	-1.695830e+00 dB
AV	4.057579e+01 dB

Table 5: Gain at 1KHz

As we can notice, these results are very similar to the ones in the previous table.

2.2 Frequency response Vo(f)/Vi(f)

Now, considering the transfer function $T(s)$, it is given by:

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = 1 + \frac{Z_{in}(s)}{Z_{out}(s)} = \frac{R_1 \cdot C_1 \cdot s}{1 + R_1 * C_1 * s} \cdot (1 + \frac{R_3}{R_4}) \cdot \frac{1}{1 + R_2 \cdot C_2 \cdot s} \quad (7)$$

, where $\frac{R_1 \cdot C_1 \cdot s}{1+R_1*C_1*s}$, $1+\frac{R_3}{R_4}$ and $\frac{1}{1+R_2 \cdot C_2 \cdot s}$ represent the gain at high pass filter, OP-AMP and low pass filter, respectively.

This way, the gain frequency response is plotted in the figure below.

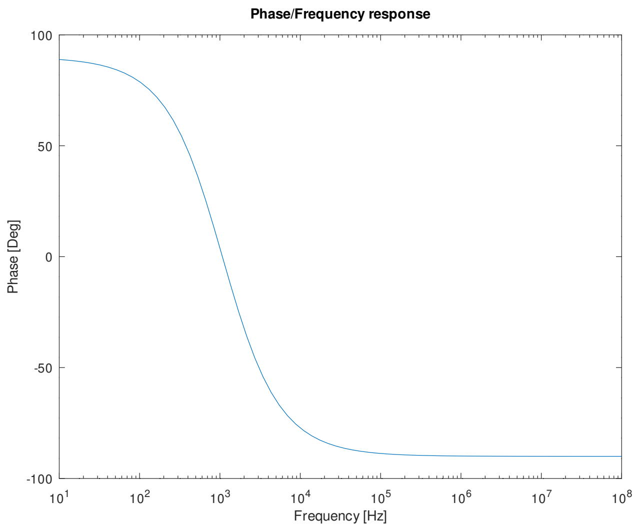


Figure 2: Phase Frequency Response

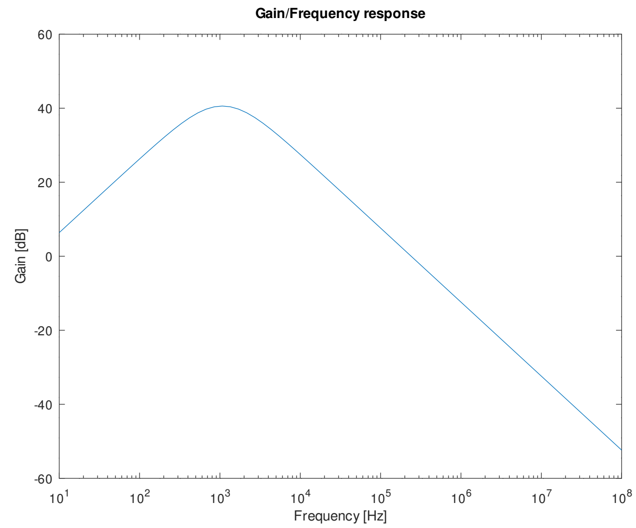


Figure 3: Gain Frequency Response

As we can see there is a maximum for the frequencies in the central frequency, wich is near to 1KHz, otherwise low and high frequencies have a low gain. That was expected because both low and high frequencies were blocked by high and low pass filters.

3 Simulation Analysis and Comparison with Theoretical Values

3.1 Frequency Analysis

3.1.1 Magnitude Response

Figure 4 shows the frequency magnitude response of the circuit, for the voltage gain, which is expressed in dB. Comparing to the theoretical graphic, we notice that the curves are very similar. We only notice the differences by taking a closer look to both curves, and see that the maximum voltage gain is not the same for the theoretical and simulated results. Both results approach very well the reference value, 40dB, and the differences between these two results might rely on the fact that NGSpice uses a real OPAMP model.

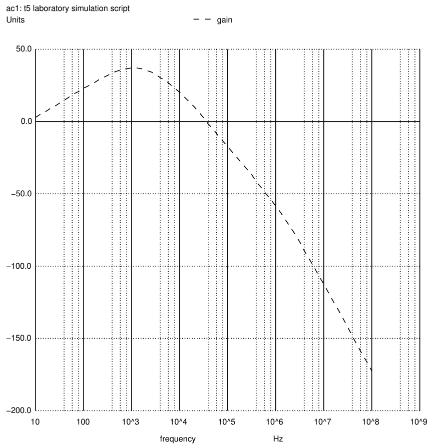


Figure 4: Magnitude response for the voltage gain V_{out}/V_{in}, in dB.

3.1.2 Phase Response

Figure 5 shows the frequency phase response of the circuit, for the voltage gain, which is expressed in degrees. Comparing to the theoretical graphic, we notice that the curves are very similar. We only notice the differences by taking a closer look to both curves, and see that the maximum voltage gain is not the same for the theoretical and simulated results. Both results approach very well the reference value, 40dB, and the differences between these two results might rely on the fact that NGSpice uses a real OPAMP model.

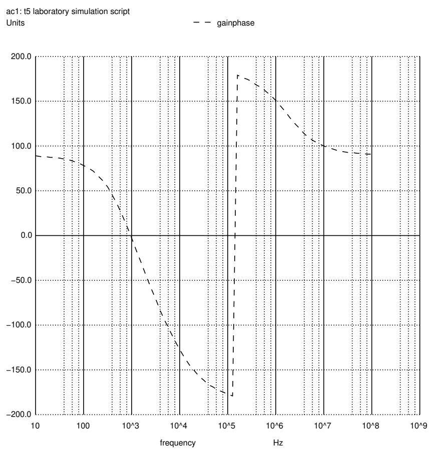


Figure 5: Phase response for the voltage gain V_{out}/V_{in}, in degrees.

3.2 Simulation Results

Table 6 shows the simulated results, using NGSPICE, for the input and output impedances, at the central frequency. Remind that the values on the right are the theoretical ones obtained by Octave, which are reproduced in this section to help compare them to the simulated resuls. Comparing both the values, we conclude that the results are very close, some differences resulting on the fact that, on NGSpice, we used an aproximate value of the central frequency to calculate the impedances and because in this simulating tool, it considers the components real (the OPAMP, most importantly).

Input impedance	**Ohms**
zin	1.161859e+03

Output impedance	**Ohms**
zout	8.251525e+02

Table 6: Input and Output impedances

Finally, Table 7 shows the values obtained for the gain and central frequency of the circuit under analysis. The table shows also the merit result and the values used for the calculation of the merit figure, which are the cost, the central frequency deviation (which should be ideally 1kHz) and the linearly voltage gain deviation (which should be ideally 100).

Name	**Values**
Gain(dB)	37.0419
Gain	71.1371
Central Frequency(Hz)	1051.2
Gain deviation	28.8629
Central frequency deviation(Hz)	51.2041
Cost(MU)	13446.7
Merit	9.28821E-07

Table 7: Values for the calculation of the Merit.

As one can notice, we achieved a very low merit value. However, if we analyse the restrictions imposed on the uses of certain components and the results for the gain and the central frequency, which are quite close to the reference values, we conclude that, despite the low merit value, we achieved a very efficient circuit whose quality would degrade significantly if we changed randomly the values of the components to achieve the highest merit figure possibly.

3.3 Side by Side Comparison

Name	**Value**
zin	1.161859e+03

Name	**Value**
zout	8.251525e+02

Name	**Value**
Z_{in}	9.090909e+02 + j-6.741999e+02 Ohm
Z_{out}	6.451613e+02 + j-4.784644e+02Ohm
$\lvert Z_{in}\rvert$	1.131809e+03 Ohm
$\lvert Z_{out}\rvert$	8.032193e+02 Ohm

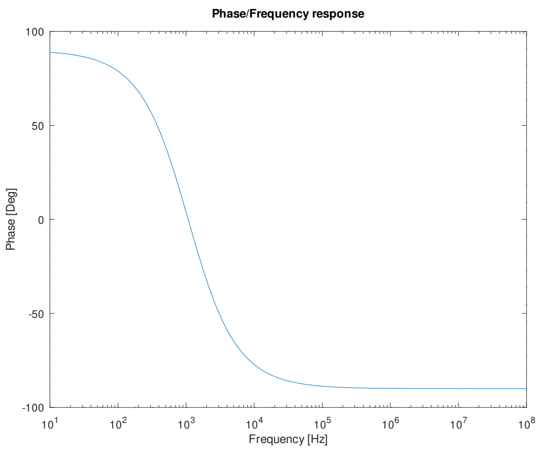
Table 8: Comparison of Input and Output Impendances (Left - Simulation Values, Right - Theoretical Values)

Name	Value
AV_{HP}	-1.903317e+00 dB
AV_{OPAMP}	4.440216e+01 dB
AV_{LP}	-1.903317e+00 dB
AV	4.059553e+01 dB

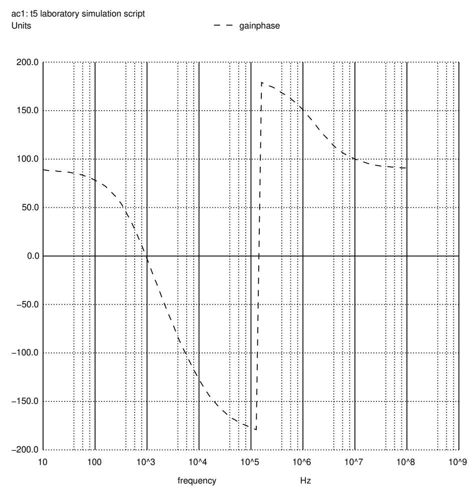
Name	Value
w_L	5.000000e+03 rad/s
w_H	9.090909e+03 rad/s
w_O	6.741999e+03 rad/s
f_O	1.073022e+03 Hz

Name	Value
Gain(dB)	37.0419
Gain	71.1371
Central Frequency(Hz)	1051.2
Gain deviation	28.8629
Central frequency deviation(Hz)	51.2041
Cost(MU)	13446.7
Merit	9.28821E-07

Table 9: Comparison of Gain (Left - Theoretical Values, Right - Simulation Values)

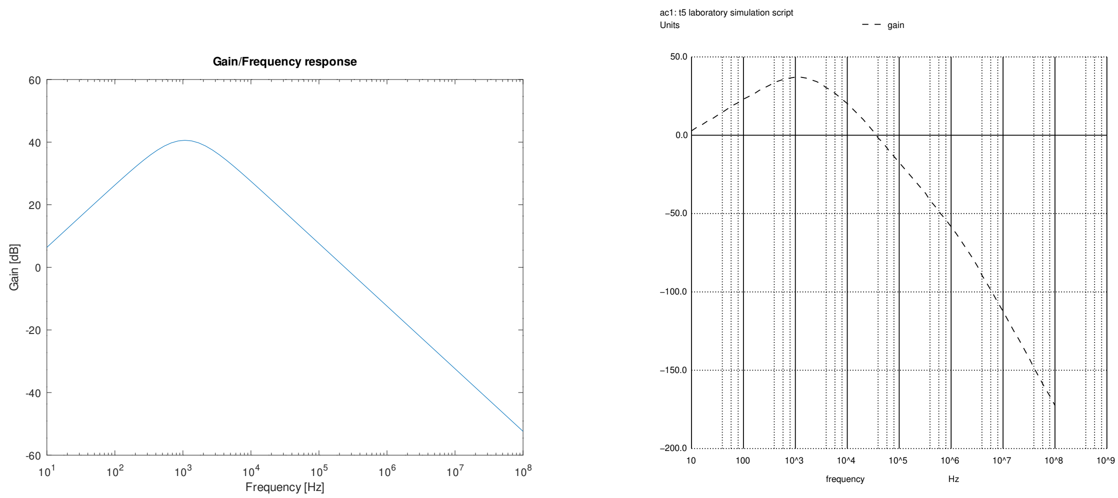


(a) Theoretical Phase Response



(b) Simulation Phase Response

Figure 6: Phase Response



(a) Theoretical Phase Response

(b) Simulation Phase Response

Figure 7: Gain Response

4 Conclusion

In this laboratory assignment the objective of building and analysing an Audio Amplifier Circuit, made of a gain stage and an output stage, has been achieved. The theoretical analysis was performed with the help of the Octave math tool and the circuit simulation using the Ngspice tool. For both analysis, we determined the gain and input and output voltages of the circuit, as well as, lower cut-off frequency. We also plotted the frequency responce Vo(f)/Vi(f). At the end, we calculate the merit of our work.

This way, in theoretical analysis, we explained why the two stages could be connected without significant signal loss. And, in simulation analysis, we also explaneid the purpose of the coupling capacitors and their effect on the bandwidth, the purpose of the bypass capacitor and its effect on the gain and the effect of resistor RC on the gain.

As previously mentioned, the simulation results had slight differences from the theoretical ones. However, we designed an acceptable Audio Amplifier Circuit - furthermore, we obtained a decent figure of merit, despite the cost being too high.