TÉCNICO LISBOA

Instituto Superior Técnico, University of Lisbon

Integrated Master in Aerospace Engineering

Circuit Theory and Electronics Fundamentals

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Fourth Laboratory Report

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1 Introduction

The objective of this laboratory assignment is to simulate a AC/DC converter circuit, which output voltage must be ideally 12 Volts. This converter must have an envelope detector and a voltage regulator. We are free to choose the architecture of both circuits, however we must consider the cost of the components in the circuit, the ripple voltage and the voltage difference between the output voltage and 12 Volts.

After multiple simulations, we have decided to simulate the following circuit. The envelope detector is composed by a full rectifier brigde and a resistor R_1 in parallel with a capacitor C, while the voltage regulator has a resistor R_2 in series with 20 diodes. The values of the components are exhibited in the table below. We have also taken advantage of the fact that, in this assignment, the number of turns n of the transformer will not influence the merit of our work. Therefore, as you can see below, we used an unusual value for n.

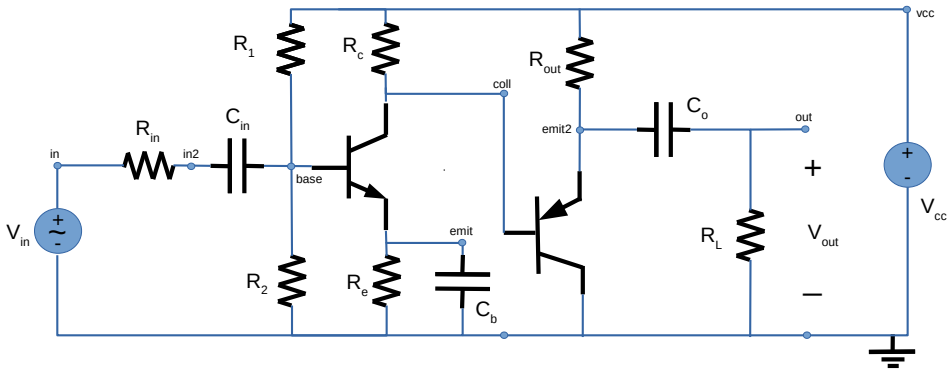

Figure 1: AC/DC converter circuit.

GAIN STAGE Here we have a npn transistor.

Name	Value
V_{CC}	1.200000e+01 V
R_{in}	1.000000e+02 Ohm
R_1	8.000000e+04 Ohm
R_2	2.000000e+04 Ohm
R_c	1.000000e+03 Ohm
R_e	1.000000e+02 Ohm
C_{in}	1.000000e-02 F
C_b	1.000000e-02 F

Table 1: Gain Stage Data

In Section **??**, a theoretical analysis of the circuit, performed on Octave, is presented. In Section **??**, the circuit is analysed by simulation, using NGSpice, and the results are compared to the theoretical results obtained in Section **??**. The conclusions of this study are outlined in Section **??**.

2 Theoretical Analysis

In this section, the circuit shown in Figure **??** is analysed theoretically. We will begin by analyzing the Gain Stage circuit and, after that, the Output Stage circuit.

Thus, we will start by computing the Operating Point using the theoretical DC model studied and comparing it to Ngspice's OP.

Then, we will compute the gain and input and output impedances separately for the 2 stages.

Finally, we will compute the frequency response Vo(f)/Vi(f).

2.1 Gain Stage

In this subsection, we will analyze the Gain Stage circuit.

In order to make this task easier, we used Thévenin's equivalent of bias circuit. Its diagram is represented in Figure **??** as well as the NPN BC547A model used in this assignment is shown in table **??**.

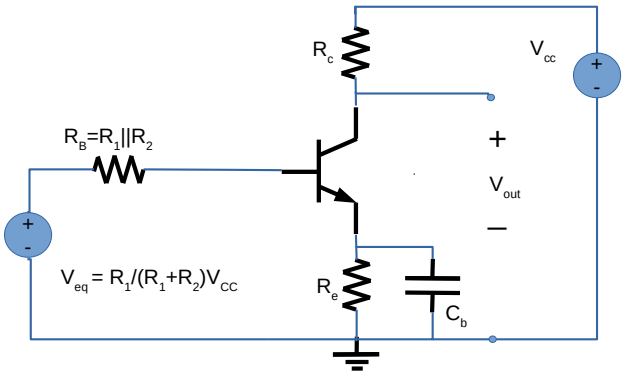

Figure 2: Gain Stage Circuit

Name	Value
V_T	0.025000 V
$beta$	178.700000
V_A	69.700000 V
V_{BEON}	0.700000 V

Table 2: BC547A model

2.1.1 Operating Point

Considering the equations of the lecture 17 and the theoretical DC model studied , we compute the OP. The table **??** presents the results obtained.

Name	Value
R_B	1.600000e+04 Ohm
V_{eq}	2.400000e+00 V
I_{B1}	5.004416e-05 A
I_{C1}	8.942891e-03 A
I_{E1}	8.992935e-03 A
V_{E1}	8.992935e-01 V
V_{O1}	3.057109e+00 V
V_{CE}	2.157816e+00 V

Table 3: OP - Gain Stage

2.1.2 Gain and Input and Output Impedances

Then, we will compute the gain and input and output impedances. In order to do that, we will use the incremental circuit, whose diagram is represented in Figure **??**.

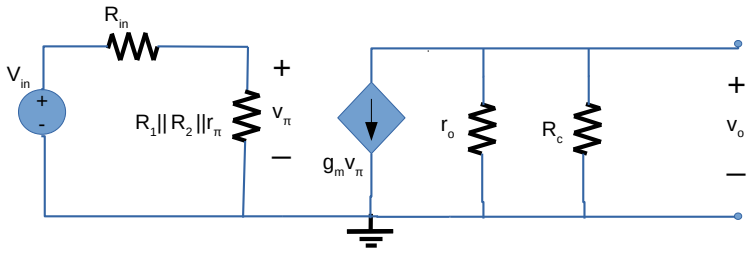

Figure 3: Incremental Gain Stage Circuit

Starting by calculating the gain, after analyzing the circuit, we obtain the following equation, with $R_E = 0$:

$$A_v = \frac{v_o}{v_{in}} = -g_m(r_o||R_C)\frac{R_B||r_\pi}{R_B||r_\pi + R_{in}} \tag{1}$$

Notice that the capacitor C_b was used to bypass R_E. Otherwise, the gain will be lower and the lower cutoff frequency too high. This way, CE is an open-circuit for low frequency (DC) and a short-circuit fot higher frequencies (AC).

Table **??** presents the results.

Name	Value
A_{V1}	4.839221e+01 dB
$A_{VIsimple}$	5.101664e+01 dB

Table 4: Gain - Gain Stage

In order to obtain the impedances, we used the following equations:

$$Z_{I1} = R_1||R_2||r_\pi \tag{2}$$

$$Z_{O1} = R_C||R_o \tag{3}$$

The results are presented in Table **??**

Name	Value
Z_{I1}	4.844336e+02 Ohm
Z_{O1}	8.862848e+02 Ohm

Table 5: Input and Output Impedances - Gain Stage

2.2 Output Stage

In this subsection, we will analyze the Output Stage circuit. Its diagram is represented in Figure **??** as well as the PNP BC547A model used in this assignment is shown in table **??**.

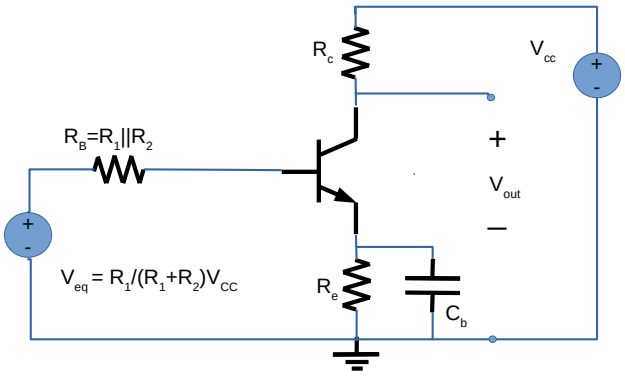

Figure 4: Output Stage Circuit

Name	Value
$beta$	227.300000
V_{AFP}	37.200000 V
V_{BEON}	0.700000 V

Table 6: BC557A model

2.2.1 Operating Point

Considering the equations of the lecture 17, we compute the OP. The table **??** presents the results obtained.

Name	Value
V_{I2}	3.057109e+00 V
I_{E2}	8.242891e-02 A
I_{C2}	8.206785e-02 A
V_{O2}	3.757109e+00 V

Table 7: Operating Point - Output Stage

It is important to notice that output current I_E is much stronger than in Gain Stage and that part pf this current will feed the Load.

2.2.2 Gain and Input and Output Impedances

Then, we will compute the gain and input and output impedances. In order to do that, we will use the incremental circuit, whose diagram is represented in Figure **??**.

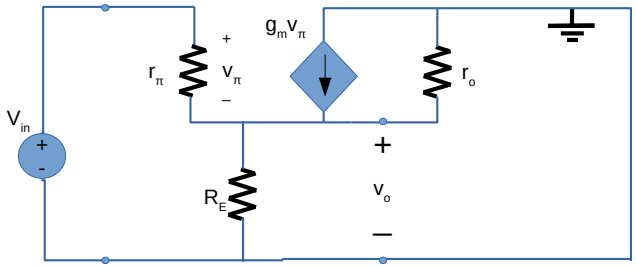

Figure 5: Output Stage Circuit

Starting by calculating the gain, after analyzing the circuit, we obtain the following equation:

$$A_v = \frac{v_o}{v_{in}} = \frac{g_m}{g_\pi + g_E + g_o + g_m} \tag{4}$$

, where g_π, g_E and g_o are the admittances of the respective resistors.

Table **??** presents the results and, as predicted, we obtained almost unitary gain.

Name	Value
A_{V2}	9.919476e-01 dB

Table 8: Gain

In order to obtain the impedances, we used the following equations:

$$Z_{I2} = \frac{g_\pi + g_E + g_o + g_m}{g_\pi(g_\pi + g_E + g_o)} \tag{5}$$

$$Z_{O2} = \frac{1}{g_\pi + g_E + g_o + g_m} \tag{6}$$

The results are presented in Table **??**

Name	Value
Z_{I2}	8.598855e+03 Ohm
Z_{O2}	3.021730e-01 Ohm

Table 9: Input and Output Impedances

2.3 Final

For the final output, it is important to mention that was used another coupling capacitor between the Output stage and the load. So, these outputs are in Table **??**.

Name	Value
A_V	4.795943e+01 dB
Z_I	4.844336e+02 Ohm
Z_O	3.981969e+00 Ohm

Table 10: Output Values

3 Simulation Analysis and Comparison with Theoretical Results

3.1 Transient Analysis

Figure **??** shows the simulated transient analysis results for input voltage of the secondary circuit, the envelope detector output voltage, V_3, the voltage regulator output voltage, V_4 and the average voltage difference, V_4-12 Volts.

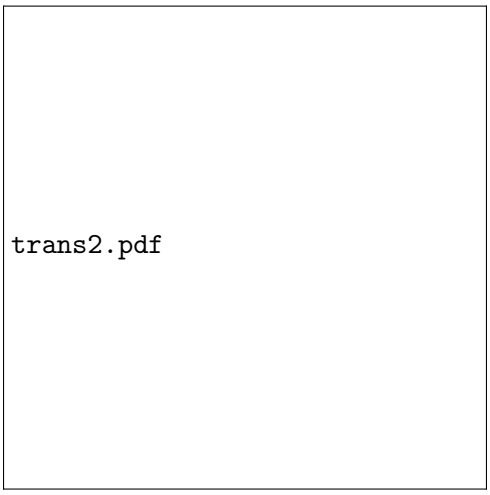

Figure 6: Transient input voltage of the secondary circuit and transient output voltage of both the envelope detector and voltage regulator and the average voltage difference.

By analysing the result of the simulation we notice that the output solution resulted in an aproximated sinusoidal fuction: in fact, because of the average voltage is not ideal, the curve has an upward sinusoidal motion and a downward motion described by a negative exponential. The input voltage is described by a sinusoidal fuction, as expected. As far as the result is concerned, the form of the theoretical solution match the one obtained by NGSpice. Note that, because of the scale, we can not see the wave form of the ripple voltage and voltage difference because they are very small, which means that we obtained a decent result for 2 of the 3 parameters that influence the merit.

Table **??** shows the measured results for the maximum, minimum and average output voltage of the circuit V_4. Notice that the values on the right were obtained by Octave, therefore they are the theoretical values, which we already mentioned previously but, to facilitate the comparison between the simulation and theoretical values, we mentioned them again.

Name	Voltage[V]	Node	Voltage[V]

Table 11: Measured maximum, minimum and average output voltage of the circuit. The values on the right are the theoretical values for the same voltages in the circuit.

Compared to the theoretical analysis results, we noticed that the values are slightly different, this happens mainly because in order to do the theoretical analysis we assumed that the diodes were ideal, something that it is not verified in the simulation since a real diode model was used. Despite that, we realise that the error obtained is minimal making us conclude that, not only was this assignment objective achieved but we can also verify that the ideal diode model is indeed a good approximation.

Table **??** shows the ripple voltage of the circuit and the average voltage difference between the output voltage and 12 Volts. Again, we show the theoretical values obtained for this step, to make it easier to compare between simulation and theoretical values. It is also worth noticing

that, for the reasons mentioned previously, the results vary slightly between the theoretical and the simulation analysis.

Name	Voltage[V]	Name	Voltage[V]

Table 12: Ripple voltage maxV_4 - minV_4 and the average voltage difference V_4 - 12. The values on the right are the theoretical values for the same voltages in the circuit.

Table **??** shows the total cost of the circuit and the figure of merit of the circuit. Note that we used the simulated voltage results to calculate the value of merit.

	Monetary Units [MU]

Table 13: Total cost

Formula	Merit

Table 14: Figure of merit with a cost of 222.4 monetary units (MU).

By analising the figure of merit, we note that its value, considering the multiple results obtained for different values of the components and layots of the circuit, is reasonable. Nevertheless, we consider the result not satisfying, since we obtained a merit of around 900 when we eliminated resistor R_1 and added 15 more diodes to the series (reducing considerably the cost, the ripple and the average voltage difference). However, the AC/DC converter obtained would not be an efficient one, since it would have an enourmous stabilization time and no resistor connected in parallel with the capacitor.

4 Conclusion

In this laboratory assignment the objective of analysing an AC/DC converter, made of an envelope detector and a voltage regulator, has been achieved. The theoretical analysis was performed with the help of the Octave math tool and the circuit simulation using the Ngspice tool. For both analysis, we plotted the output voltages of both the envelope detector and voltage regulator and, in the case of the regulator, we also determine the maximum, minimum and average output voltage, so we could measure the voltage ripple and difference between the output and 12V, to calculate the figure of merit. As previously mentioned, the simulation results had slight differences from the theoretical ones. However, we designed an acceptable AC/DC converter - furthermore, we obtained a low stabilization time and a decent figure of merit, despite the cost being too high.