ELECTRICAL PARAMETERS CMOS 0.7 µm - C07MA AND C07MD

Owner : Technology Engineering CMOS

Location : NA

REVISION STATUS SUMMARY

Revision	Requestor	Date	Request Number	Pages	Description
01	MT	04-12-1992	8747	01-22	New document.
02	MT	22-11-1993	11131	01-72	Complete revision. Addition of analog parameters.
03	MT	05-04-1994	11916	01-79	Update of electrical parameters and design models at R1. Review of methodology for defining M2-M1 capacitances. Addition of C07M-P parameters.
04	TC	02-09-1994	12712	50,53,56	Type error=> channel length >= 2 um.
05	GG	20-07-1995	14214	67	Correction of typing error in hot carrier formula
06	JW	05-02-1996	14991	All	Update parameters and models for R2 release.
07	HVH	25-09-1997	17478	All	Line up with BSim 3 models + Add poly zap structure.
08	HVH	09-04-1999	20313	41, 62-64	Include Ndmos device.
09	TC	02-02-2001	23934	13	Change Weff for Nmos.
10	PC	07-06-2001	24598	31,32,37 38,40,43 46,49,52 53	Adding data for TLM option, forbid combination TLM-polyzaps, relax rules about matching (metal2 cross-over can be allowed)
11	TV	04-03-2002	25938	42	Include Zener Diode for OTP applications
12	TC	23-07-2002	26790	33	Add contact resistances for 0.8 um contacts

TABLE OF CONTENTS

1.0 INTRODUCTION

The AMI Semiconductor 0.7 µm CMOS technology family C07M contains the following technology routes:

- C07M-SDCF-D* (short code: C07M-D):
  The core digital, 0.7 µm, single level poly, double level metal, CMOS technology designed for 5V operation.

- C07M-TDCF-A* (short code: C07M-A):
  The mixed digital/analog, 0.7 µm, single level poly, double level metal, CMOS technology designed for 5V operation. It is obtained from the core C07M-D technology by adding the following analog modules:
  a. low Vt PMOS option
  b. implanted capacitors
  c. high ohmic polysilicon resistors

- C07M-SDCF-P* (short code: C07M-P):
  The polycide digital 0.7 µm, single level poly, double level metal, CMOS technology designed for 5V operation. It is obtained from the core C07M-D technology by adding a low ohmic polycide module.

The layout rules for the C07M technology family are given in the AMI Semiconductor Specification 13290.

The electrical design rule set for the C07M-P is given in the AMI Semiconductor Specification DS 13295.

This document provides the electrical design rule set for the C07M-A and C07M-D technology family.

LIST OF CHARACTERIZED DEVICES:

The following active and passive devices are available in C07MA and C07M-D, and are characterized in this document:

1. TRANSISTORS :
   1A - MOS : NMOS, PMOS and low-Vtp PMOS (˚)
   1B - BIPOLAR: Vertical PNP

2. RESISTORS:
   N+, P+ and NWELL diffusion
   Poly
   High Ohmic Poly (HIPO) (˚)

3. CAPACITORS:
   Gate oxide capacitors & interconnect capacitors
   Junction capacitances
   Implanted capacitor (˚)

   (˚) These devices are available only in the C07M-A route

2.0 DEFINITION OF MEASUREMENT CONDITIONS, STRUCTURES AND CHARACTERIZATION PARAMETERS

This section briefly describes the measurement conditions of the electrical parameters and gives a definition of the basic devices and definitions of some additional characteristic parameters.

All dimensions are as-drawn.

All values of the parameters are measured at 300K. Temperature coefficients are specified from -55˚C to150˚C.

All values of the parameters are valid for all device dimensions except where these dimensions are specified.

Only the absolute values of the voltages and the currents for the PMOS and PMOS low VT transistors are given.

2.1 Definition of the Measurement Conditions of Active and Parasitic MOS Transistors

NMOS

Vdnom	nominal operating drain voltage	5 V
Vdmax	maximum operating drain voltage	5.5 V
Vdlin	drain voltage for operation in linear regime	0.1 V
Vdsat	drain voltage for operation in saturation	5 V
Vdana	characteristics analog drain voltage	3 V
Vg_isubmax	approximate gate voltage at which the substrate current reaches maximum value Isubmax at Vdmax	2 V
Vb_gamma	bulk biasing for measurement of Gamma start value 0 V step value 1 V Nbr of steps 6	
Vd_field	Drain voltage for measuring Vgsat of field transistor	10 V
Id_noise	Drain current for measuring noise	

PMOS and low-Vt PMOS

Vdnom	nominal operating drain voltage	5 V
Vdmax	maximum operating drain voltage	5.5 V
Vdlin	drain voltage for operation in linear regime	0.1 V
Vdsat	drain voltage for operation in saturation	5 V
Vdana	characteristics analog drain voltage	3 V
Vb_gamma	bulk biasing for measurement of Gamma start value 0 V step value 1 V Nbr of steps 6	
Vd_field	Drain voltage for measuring Vgsat of field transistor	10 V
Id_noise	Drain current for measuring noise	

2.2 Definition of the Characterisation Structures of Active Transistors

NMOS

Wide/long device	W= 20 µmL= 20 µm
Wide/short device	W= 20 µmL= 0.7 µm
Narrow/short device	W= 1µm L= 0.7 µm
Narrow/long device	W= 1 µmL= 20 µm
Wide/moderate device	W= 20 µmL= 5 µm

PMOS

Wide/long device	W= 20 µmL= 20 µm
Wide/short device	W= 20 µmL= 0.7 µm
Narrow/short device	W= 1µm L= 0.7 µm
Narrow/long device	W= 1 µmL= 20 µm
Wide/moderate device	W= 20 µmL= 5 µm

PMOS low Vt

Wide/long device	W= 20 µmL= 20 µm
Wide/short device	W= 20 µm L= 1.2 µm
Narrow/short device	W= 1µm L= 1.2 µm
Narrow/long device	W= 1 µmL= 20 µm
Wide/moderate device	W= 20 µmL= 5 µm

VERTICAL PNP

Device Ae = 460 µm^2

2.3 Definition of Additional Characterisation Parameters

2.3.1 Matching

Matching between two identically designed devices is the standard deviation (1sigma) of the relative differences of P1 and P2, where P1 and P2 are characteristic parameters of these devices, and the mean value of P1/P2 ratios is one.
The values given in the electrical rules are valid only for devices designed following special rules given in paragraph 5.

2.3.2 Voltage linearity of drain current and transconductance of MOS transistors

Vli[V] is the drain voltage at which the drain current deviates by 0.1% from the linearly extrapolated value.

Rim is the ratio between the drain current at Vdmax and the extrapolated value at Vdmax.

Vgi[V] is the drain voltage at which the output conductance becomes twice the output conductance at Vdana.

Rgm is the ratio between the output conductance at Vdmax and the output conductance at Vdana.

2.3.3 Drain and bulk current symmetry of MOS transistors

Drain and bulk current symmetry factors characterise the asymmetry between the drain and source terminals. These factors are measured using the difference between forward (f) and reverse (r) currents on MOS transistors with identically designed source and drain terminals.

Idsym[%] = 200*(Idsatf - Idsatr)/(Idsatf + Idsatr)

Isubsym[%] = 200*(Isubmaxf - Isubmaxr)/(Isubmaxf+Isubmaxr)

2.3.4 Temperature coefficients measured over the range -55˚C to 155˚C

MOS Threshold voltage
VT0=VT030 + TCvt0*(t[˚C]-30)

MOS Betalin
LOG(BetalinT*L/W)=Abetalin + TCbetalin*LOG(T[K])

MOS Drain saturation current
Idsat[µA]=Idsat30[µA].(1 + TC1*(t[˚C]-30) +TC2*(t[˚C]-30)^2)

Diode Ileak
Ileak = $i_a A + i_p P$
A: area of the diode; P: perimeter of the diode

Sheet resistance (Rsh)
Rsh[Ohm/sq]=Rsh30[Ohm/sq] *
(1+ TCL*(t[˚C]-30) +TCQ*(t[˚C]-30)^2)

Vbe Vertical PNP
VbeT [V] = Vbe294 + TCL*(t[˚C]-21)

2.3.5 Voltage coefficients

Resistance
Rv[Ohm]=R0*(1 +VCL *V+VCQ*V^2)
where one pin of the resistor is connected to the bulk and the other pin is biased V volt higher

Capacitance
C(V)[pF]=C(0)[pF]*(1 +VCL *V)

3.0 ELECTRICAL PARAMETERS

3.1 NMOS Active Transistors

Wide/long NMOS transistor - digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.65	0.77	0.89	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	86.8	96.3	107	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Slin	86	93	100	mV/dec	Vdlin2.5,5,7.5 nA fit
Vtsat	0.60	0.73	0.84	V	Vdsat
Idsat/w	24.1	27.8	31.8	µA/µm	Vdnom; Vg=Vdnom
Gamma	0.65	0.78	0.85	SQR(V)	Vb_gamma Vdlin
Bvds	10			V	Vg=0V; Id sweep 1µA
Idleak/w			10	pA/µm	Vg=0V; Vd=7V

Remark: 6 σ approach

Wide/long NMOS transistor -analog parameters

	Min	Nom	Max	Unit	Meas. cond.
Parameters					
Temperature coefficients					
TCvt0 of VT0		-1.4		mV/˚C	Vdlin
TCbetalin of Betalin		-1.74		Log(µA/V^2) /Log(K)	Vdlin
Abetalin of Betalin		6.29		Log(µA/V^2)	Vdsat; Vg_isubmax
TC1 of Idsat					
TC2 of Idsat					
Voltage linearity					
Vli	4.0	4.5	5.0	V	Vg_isubmax; Vd sweep
Rim	1.00	1.01	1.02	/	Vg_isubmax
Vgi	3.7	4.2	4.7	V	Vg_isubmax; Vd sweep
Rgm	6.5	10.5	14.5	/	Vg_isubmax
Current symmetry					
Idsym	-5	0	5	%	Vdsat; Vg_isubmax
Isubsym	-15	0	15	%	Vdsat; Vg_isubmax
Current matching $(\sigma_{\Delta}Id/Id)^2=$ $\sigma_{VT0})^2*4/(Vg-VT0)^2 +$ $(\sigma_{\Delta}ß/ß)^2$					
σVT0		0.7		mV	Vbs=0V Vg=VT0+0.2/2V
σ_{Δ}ß/ß		0.13		%	Vbs=0V Vg=VT0+0.2/2V
Noise Equivalent input 1/f noise				V/Sqr(Hz)	Vdana; Id noise; f=1KHz

Wide/short NMOS transistor- digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.60	0.74	0.88	V	Vdlin, max.slope ΔId/ΔVg X intcp-Vd/2
Betalin	1880	2550	3310	µA/V2	Vdlin; max.slope ΔId/ΔVg
Slin	88	94	100	mV/dec	Vdlin 2.5,5,7.5 nA fit
Vtsat	0.56	0.67	0.77	V	Vdsat
Ssat	85	95	105	mV/dec	Vdmax 2.5,5,7.5 nA fit
Idsat/W	288	358	432	µA/µm	Vdnom; Vg=Vdnom
Gamma	0.40	0.6	0.75	SQR(V)	Vb_gamma Vdlin
Bvds	7			V	Vg=0V; Id sweep 1µA
Idleak/w			10	pA/µm	Vd=7V; Vg=0V
Isubmax/w	0.6	1.1	1.6	µA/µm	Vdmax; Vg_isubmax
Vsnapback	7			V	Vg_isubmax, Id sweep to 10Ma
Leff	0.535	0.70	0.865	µm	Leff calculated from Betalin of wide/long and wide/short transistor

Remark: 6 σ approach

Wide/short NMOS transistor- analog parameters

	Min	Nom	Max	Unit	Meas. cond.
Parameters					
Temperature coefficients					
TCvt0 of VT0		-1.5		MV/˚C	Vdlin
TCbetalin of Betalin		-1.83		Log(µA/V^2) /Log(K)	Vdlin
Abetalin of Betalin		6.53		Log(µA/V^2)	Vdsat; Vg_isubmax
TC1 of Idsat		-13.8		µA/˚C	
TC2 of Idsat		0		µA/˚C^2	
Voltage linearity					
Vli	4.5	5.0	5.5	V	Vg_isubmax; Vd sweep
Rim	0.98	1.0	1.02	/	Vg_isubmax
Vgi	4.8	5.3	5.8	V	Vg_isubmax; Vd sweep
Rgm	1.5	2.0	2.5	/	Vg_isubmax
Current symmetry					
Idsym	-5	0	5	%	Vdsat; Vg_isubmax
Isubsym	-15	0	15	%	Vdsat; Vg_isubmax
Current matching $(\sigma_{\Delta}Id/Id)^2=$ $\sigma_{VT0)}^2*4/(Vg-VT0)^2$ + $(\sigma_{\Delta}ß/ß)^2$					
σ_{VT0}		3.55		mV	Vbs=0V Vg=VT0+0.2/2V
$\sigma_{\Delta}ß/ß$		0.64		%	Vbs=0V Vg=VT0+0.2/2V
Noise Equivalent input 1/fnoise				V/Sqr(Hz)	Vdana Id_noise; f=1KHz

Narrow/short NMOS transistor- digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.65	0.81	0.97	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	82	131	196	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Vtsat	0.56	0.70	0.85	V	Vdsat
Idsat/W	266	389	538	µA/µm	Vdsat; Vg=Vdsat
Gamma	0.50	0.70	0.90	SQRT(V)	Vb_gamma Vdlin
Bvds	7			V	Vg=0V; Id sweep 1µA
Idleak/W			10	pA/µm	Vd=7V; Vg=0V
Isubmax/W	0.5	1.3	2	µA/µm	Vdmax; Vg_isubmax

Remark: 6 σ approach

Narrow/Long NMOS transistor- digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.71	0.85	0.99	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	3.16	4.31	5.66	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Idsat/W	19	26.2	35.3	µA/µm	Vdsat;Vg=Vdsat
Gamma	0.7	0.8	0.9	SQR(V)	Vb_gamma Vdlin
Bvds	10			V	Vg=0V; Id sweep 1µA
Idleak/W			10	pA/µm	Vd=7V;Vg=0V
Weff	0.66	0.90	1.19	µm	Weff calculated from Betalin of wide/long and narrow/long transistor

Remark: 6 σ approach

Wide/moderate NMOS transistor- digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.65	0.77	0.90	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	335	381	431	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Idsat/W	83.5	98	112	µA/µm	Vdsat;Vg=Vdsat

Remark: 6 σ approach

Wide/moderate NMOS transistor- analog parameters

	Min	Nom	Max	Unit	Meas. cond.
Parameters					
Temperature coefficients					
TCvt0 of VT0		-1.4		MV/˚C	Vdlin
TCbetalin of Betalin		-1.78		Log(µA/V^2) /Log(K)	Vdlin
Abetalin of Betalin		6.40		Log(µA/V^2)	Vdsat; Vg_isubmax
TC1 of Idsat				µA/˚C	
TC2 of Idsat				µA/˚C^2	
Voltage linearity					
Vli	4.1	4.7	5.3	V	Vg_isubmax; Vd sweep
Rim	0.995	1.01	1.01	/	Vg_isubmax
Vgi				V	Vg_isubmax; Vd sweep
Rgm				/	Vg_isubmax
Current symmetry					
Idsym	-5	0	5	%	Vdsat; Vg_isubmax
Isubsym	-15	0	15	%	Vdsat; Vg_isubmax
Current matching $(\sigma_{\Delta}Id/Id)^2 = \sigma VT0)^2 * 4/(Vg-VT0)^2 + (\sigma_{\Delta}ß/ß)^2$					
σVT0		1.35		mV	Vbs=0V Vg=VT0+0.2/2V
$\sigma_{\Delta}ß/ß$		0.24		%	Vbs=0V Vg=VT0+0.2/2V
Noise equivalent input 1/f noise				V/Sqr(Hz)	Vdana; Id_noise; f=1KHz

3.2 PMOS Active Transistors

Wide/long PMOS transistor - digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.88	1.01	1.13	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	26	30	33	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Slin	76	81	86	mV/dec	Vdlin2.5,5,7.5 nA fit
Vtsat	0.83	0.95	1.08	V	Vdsat
Idsat/W	6.57	7.42	8.41	µA/µm	Vdsat; Vg=Vdsat
Gamma	0.51	0.565	0.62	SQRT(V)	Vb_gamma Vdlin
Bvds	10			V	Vg=0V; Id sweep 1µA
Idleak/W			10	pA/µm	Vd=7V; Vg=0V

Remark: 6 σ approach

Wide/long PMOS transistor -analog parameters

	Min	Nom	Max	Unit	Meas. cond.
Parameters					
Temperature coefficients					
TCvt0 of VT0		-1.8		MV/˚C	Vdlin
TCbetalin of Betalin		-1.41		Log(µA/V^2) /Log(K)	Vdlin
Abetalin of Betalin		4.99		Log(µA/V^2)	Vdsat; Vg_isubmax
TC1 of Idsat					µA/˚C
TC2 of Idsat					µA/˚C^2
Current symmetry					
Idsym	-3	0	3	%	Vdsat; Vg_isubmax
Current matching $(\sigma_{\Delta}Id/Id)^2=$ $\sigma VT0)^2*4/(Vg-VT0)^2 +$ $(\sigma_{\Delta}ß/ß)^2$					
σVT0		1.1		mV	Vbs=0V Vg=VT0+0.2/2V
$\sigma_{\Delta}ß/ß$		0.12		%	Vbs=0V Vg=VT0+0.2/2V
Noise equivalent input 1/f noise				V/Sqr(Hz)	Vdana; Id_noise; f=1KHz

Wide/short PMOS transistor- digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.78	0.95	1.12	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	620	850	1160	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Slin	76	86	96	mV/dec	Vdlin 2.5,5,7.5 nA fit
Vtsat	0.65	0.85	1.05	V	Vdsat
Ssat	80	92.5	105	mV/dec	Vdmax 2.5,5,7.5 nA fit
Idsat/W	130	176	226	µA/µm	Vdnom; Vg=Vdnom
Gamma	0.35	0.425	0.5	SQRT(V)	Vb_gamma Vdlin
Bvds	7			V	Vg=0V; Id sweep 1µA
Idleak/W			10	pA/µm	Vd=7V; Vg=0V
Leff	0.53	0.715	0.90	µm	Leff calculated from Betalin of wide/long and wide/short transistor

Remark: 6 σ approach

Wide/short PMOS transistor- analog parameters

	Min	Nom	Max	Unit	Meas. cond.
Parameters					
Temperature coefficients					
TCvt0 of VT0		-1.8		MV/˚C	Vdlin
TCbetalin of Betalin		-1.39		Log(µA/V^2) /Log(K)	Vdlin
Abetalin of Betalin		4.92		Log(µA/V^2)	Vdsat; Vg_isubmax
TC1 of Idsat		-4.5		µA/˚C	
TC2 of Idsat				µA/˚C^2	
Current symmetry					
Idsym	-3	0	3	%	Vdsat; Vg_isubmax
Current matching Current matching $(\sigma_{\Delta Id/Id})^2 = \sigma_{VT0})^2 * 4/(Vg-VT0)^2 + (\sigma_{\Delta ß/ß})^2$					
σ_{VT0}		5.5		mV	Vbs=0V Vg=VT0+0.2/2V
$\sigma_{\Delta ß/ß}$		0.61		%	Vbs=0V Vg=VT0+0.2/2V
Noise equivalent input 1/f noise				V/Sqr(Hz)	Vdana;Id_noise; f=1KHz

Narrow/short PMOS transistor- digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.85	1.05	1.25	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	21.6	33.7	58.9	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Slin	75	90	105	mV/dec	Vdlin2.5,5,7.5 nA fit
Vtsat	0.60	0.80	1.00	V	Vdsat
Ssat	75	90	105	mV/dec	Vdmax 2.5,5,7.5 nA fit
Idsat/W	98	150	245	µA/µm	Vdnom; Vg=Vdnom
Gamma	0.35	0.45	0.55	SQR(V)	Vb_gamma Vdlin
Bvds	7			V	Vg=0V; Id sweep 1µA
Idleak/W			10	pA/µm	Vd=7V; Vg=0V

Remark: 6 σ approach

Narrow/Long PMOS transistor- digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.94	1.12	1.26	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	0.86	1.19	1.61	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Idsat/W	4.51	6.29	8.65	µA/µm	Vdnom; Vg=Vdnom
Gamma	0.45	0.6	0.75	SQR(V)	Vb_gamma Vdlin
Bvds	10			V	Vg=0V; Id sweep 1µA
Idleak/W			10	pA/µm	Vd=7V; Vg=0V
Weff	0.58	0.88	1.18	µm	Weff calculated from Betalin of wide/long and narrow/ long transistor

Remark: 6 σ approach

Wide/moderate PMOS transistor- digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.88	1.02	1.14	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	106	121	137	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Idsat/W	25.1	29.1	33.3	µA/µm	Vdnom; Vg=Vdnom

Remark: 6 σ approach

Wide/moderate PMOS transistor- analog parameters

	Min	Nom	Max	Unit	Meas. cond.
Parameters					
Temperature coefficients					
TCvt0 of VT0		-1.8		MV/˚C	Vdlin
TCbetalin of Betalin		-1.40		Log(µA/V^2) /Log(K)	Vdlin
Abetalin of Betalin		4.95		Log(µA/V^2)	Vdsat; Vg_isubmax
TC1 of Idsat				µA/˚C	
TC2 of Idsat				µA/˚C^2	
Current symmetry					
Idsym	-3	0	3	%	Vdsat; Vg_isubmax
Current matching $(\sigma_{\Delta}Id/Id)^2=$ $\sigma VT0)^2*4/(Vg-VT0)^2$ + $(\sigma_{\Delta}ß/ß)^2$					
σVT0		2.1		mV	Vbs=0V Vg=VT0+0.2/2V
$\sigma_{\Delta}ß/ß$		0.25		%	Vbs=0V Vg=VT0+0.2/2V
Noise equivalent input 1/f noise				V/Sqr(Hz)	Vdana; Id_noise; f=1KHz

3.3 PMOS LOW VT Active Transistors

Wide/long PMOS LOW VT transistor - digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.63	0.76	0.90	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	29.0	32.4	36.4	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Slin	78	88	96	mV/dec	Vdlin 2.5,5,7.5 nA fit
Vtsat	0.58	0.71	0.84	V	Vdsat
Idsat/W	7.64	8.7	9.8	µA/µm	Vdnom; Vg=Vdnom
Gamma	0.52	0.56	0.60	SQRT(V)	Vb_gamma Vdlin
Bvds	10			V	Vg=0V; Id sweep 1µA
Idleak/W			10	pA/µm	Vd=7V; Vg=0V

Remark: 6 σ approach

Wide/long PMOS LOW VT transistor -analog parameters

	Min	Nom	Max	Unit	Meas. cond.
Parameters					
Temperature coefficients					
TCvt0 of VT0		-1.9		MV/˚C	Vdlin
TCbetalin of Betalin		-1.49		Log(µA/V^2) /Log(K)	Vdlin
Abetalin of Betalin		5.21		Log(µA/V^2)	Vdsat; Vg_isubmax
TC1 of Idsat				µA/˚C	
TC2 of Idsat		-4.5		µA/˚C^2	
Current symmetry	-3	0	3	%	Vdsat; Vg_isubmax
Idsym					
Current matching $(\sigma_{\Delta}Id/Id)^2=$ $\sigma VT0)^2*4/(Vg-VT0)^2$ + $(\sigma_{\Delta}ß/ß)^2$					
σVT0		1.5		mV	Vbs=0V Vg=VT0+0.2/2V
$\sigma_{\Delta}ß/ß$		0.17		%	Vbs=0V Vg=VT0+0.2/2V
Noise equivalent input 1/f noise				V/Sqr(Hz)	Vdana;Id_noise; f=1KHz

Wide/short PMOS LOW VT transistor- digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.63	0.78	0.92	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	400	514	640	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Slin	80	90	100	mV/dec	Vdlin 2.5,5,7.5 nA fit
Vtsat	0.55	0.70	0.85	V	Vdsat
Ssat	80	90	100	mV/dec	Vdmax 2.5,5,7.5 nA fit
Idsat/W	95.5	121	149	µA/µm	Vdnom; Vg=Vdnom
Gamma	0.45	0.50	0.55	SQR(V)	Vb_gamma Vdlin
Bvds	7			V	Vg=0V; Id sweep 1µA
Idleak/W			10	pA/µm	Vd=7V; Vg=0V
Leff	1.13	1.325	1.52	µm	Leff calculated from Betalin of wide/long and wide/short transistor

Remark: 6 σ approach

Wide/short PMOS LOW VT transistor- analog parameters

	Min	Nom	Max	Unit	Meas. cond.
Parameters					
Temperature coefficients					
TCvt0 of VT0		-1.9		MV/˚C	Vdlin
TCbetalin of Betalin		-1.47		Log(µA/V^2) /Log(K)	Vdlin
Abetalin of Betalin		5.13		Log(µA/V^2)	Vdsat; Vg_isubmax
TC1 of Idsat					µA/˚C
TC2 of Idsat					µA/˚C^2
Current symmetry					
Idsym	-3	0	3	%	Vdsat; Vg_isubmax
Current matching $(\sigma_{\Delta}Id/Id)^2=$ $\sigma VT0)^2*4/(Vg-VT0)^2 +$ $(\sigma_{\Delta}ß/ß)^2$					
σVT0		5.5		mV	Vbs=0V Vg=VT0+0.2/2V
$\sigma_{\Delta}ß/ß$		0.65		%	Vbs=0V Vg=VT0+0.2/2V
Noise equivalent input 1/f noise				V/Sqr(Hz)	Vdana; Id_noise; f=1KHz

Narrow/short PMOS LOW VT transistor- digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.71	0.88	1.04	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	13.9	19.6	30.3	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Slin	70	90	115	mV/dec	Vdlin 2.5,5,7.5 nA fit
Vtsat	0.45	0.65	0.85	V	Vdsat
Ssat	70	90	115	mV/dec	Vdmax 2.5,5,7.5 nA fit
Idsat/W	74.9	105	156	µA/µm	Vdnom; Vg=Vdnom
Gamma	0.4	0.5	0.6	SQR(V)	Vb_gamma Vdlin
Bvds	7			V	Vg=0V; Id sweep 1µA
Idleak/W			10	pA/µm	Vd=7V; Vg=0V

Remark: 6 σ approach

Narrow/Long PMOS LOW VT transistor- digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.71	0.86	1.02	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	0.93	1.24	1.63	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Idsat/W	5.65	7.62	9.9	µA/µm	Vdnom; Vg=Vdnom
Gamma	0.5	0.6	0.7	SQR(V)	Vb_gamma Vdlin
Bvds	10			V	Vg=0V; Id sweep 1µA
Idleak/W			10	pA/µm	Vd=7V; Vg=0V
Weff	0.58	0.88	1.18	µm	Weff calculated from Betalin of wide/long and narrow/long transistor

Remark: 6 σ approach

Wide/moderate PMOS LOW VT transistor- digital parameters

	Min	Nom	Max	Unit	Meas. cond.
VT0	0.64	0.77	0.91	V	Vdlin, max.slope ∆Id/∆Vg X intcp-Vd/2
Betalin	112	128	146	µA/V2	Vdlin; max.slope ∆Id/∆Vg
Idsat/W	28.7	33.5	38	µA/µm	Vdsat; Vg=Vdsat

Remark: 6 σ approach

Wide/moderate PMOS LOW VT transistor- analog parameters

	Min	Nom	Max	Unit	Meas. cond.
Parameters Temperature coefficients					
TCvt0 of VT0		-1.9		mV/˚C	Vdlin
TCbetalin of Betalin		-1.47		Log(µA/V^2) /Log(K)	Vdlin
Abetalin of Betalin		5.15		Log(µA/V^2)	Vdsat; Vg_isubmax
TC1 of Idsat		-4.5		µA/˚C	
TC2 of Idsat				µA/˚C^2	
Current symmetry Idsym	-3	0	3	%	Vdsat; Vg_isubmax
Current matching $(\sigma_{\Delta}Id/Id)^2=$ $\sigma VT0)^2*4/(Vg-VT0)^2 +$ $(\sigma_{\Delta}ß/ß)^2$					
σVT0		2.6		mV	Vbs=0V Vg=VT0+0.2/2V
$\sigma_{\Delta}ß/ß$		0.35		%	Vbs=0V Vg=VT0+0.2/2V
Noise equivalent input 1/f noise				V/Sqr(Hz)	Vdana; Id_noise; f=1KHz

3.4 Parasitic Transistors

Parasitic transistors (finger structure, minimum spacing)

	Min	Nom	Max	Unit	Meas. cond.
N poly field Vgsat	8.0	12.0		V	Vdfield; Vg sweep until 1 µA Id
P poly field Vgsat	8.0	12.0		V	
N metal field Vgsat	10.0	15.0		V	
P metal field Vgsat	10.0	15.0		V	

3.5 Resistances

Sheet resistances

	Min	Nom	Max	Unit	Meas. cond.
Nwell (resistor)	1200	1300	1400	Ohm/sq	L/W=76/15.2
P+ (VDP)	82	96	110	Ohm/sq	
N+ (VDP)	60	67.5	75	Ohm/sq	
Poly(VDP)	20	27	34	Ohm/sq	
Metal 1	37.5	50	62.5	mOhm/sq	
Metal 2 (DLM)	30	35	40	mOhm/sq	
Metal 2 (TLM)	40	45	50	mOhm/sq	
Metal 3 (TLM)	30	35	40	mOhm/sq	
High Ohmic poly resistor W≥2µm	1600	2000	2400	Ohm/sq	Vm=2.5V L/W=50/10 = dummies
High Ohmic poly resistor W=2µm	1700	2150	2600	Ohm/sq	Vm=2.5V
N+ CAPA(VDP)	14.8	17	19.2	Ohm/sq	

Electrical width

	Min	Nom	Max	Unit	Meas. cond.
Nwell				µm	Wdesign=3µm
N+	0.6	0.9	1.2	µm	Wdesign=1µm
P+	0.55	0.9	1.25	µm	Wdesign=1µm
Poly	0.6	0.80	1.0	µm	Wdesign=0.7µm
HIPO	2.0	2.2	2.4	µm	Wdesign=2.2µm

Contact resistances

	Min	Nom	Max	Unit	Meas. cond.
N+ (1 μm)	14 41	20 48	26 55	Ohm/ct Ohm/ct	Kelvin structure Contact chain
P+ (1 μm)	28 75	40 95	52 115	Ohm/ct Ohm/ct	Kelvin structure Contact chain
Poly (1 μm)	4 13	7 19	10 25	Ohm/ct Ohm/ct	Kelvin structure Contact chain
N+ (0.8 μm)	55	70	85	Ohm/ct	Contact chain
P+ (0.8 μm)	100	135	170	Ohm/ct	Contact chain
Poly (0.8 μm)	20	26	32	Ohm/ct	Contact chain
High Ohmic poly (1 μm)	80 90	110 230	140 370	Ohm/ct Ohm/ct	Kelvin structure Contact chain
N+ CAPA(1 μm)	14.8	17	19.2	Ohm/ct	Kelvin structure
Via 1 / Via 2(1 -0.8 μm)	0.05	0.15	1	Ohm/via	Contact chain

Temperature coefficients- linear (TCL) and quadratic (TCQ) of resistors

	Min	Nom	Max	Unit	Meas. cond.
Nwell (resistor)		4900 14		ppm/˚C ppm/˚C^2	L/W=76/15.2
P+		1300 1.1		ppm/˚C ppm/˚C^2	
N+		1400 1.2		ppm/˚C ppm/˚C^2	
High ohmic poly	-1600 -4	-2100 5	-2600 14	ppm/˚C ppm/˚C^2	V=2.5 L/W=100/10
Low ohmic poly		620 1.1		ppm/˚C ppm/˚C^2	V= L/W=

Voltage coefficients-linear (VCL), quadratic (VCQ) of resistors

	Min	Nom	Max	Unit	Meas. cond.
High ohmic poly	0	-70	-140	ppm/V	Vstart-10 V
L/W=100/10	-40	-52.5	-65	ppm/V^2	Vstop 10 V Nbr steps 51 Vbulk=0V
Low ohmic poly				ppm/V ppm/V^2	Vstart step Nbr steps Vbulk=
NWELL				ppm/V ppm/V^2	Vstart step Nbr steps

Matching of resistors

	Min	Nom	Max	Unit	Meas. cond.
High ohmic poly L/W=100/10		0.1		%	V=2.5V
n+ doped low ohmic Poly L/W=100/10		0.5		%	V=
p+ doped low ohmic Poly L/W=				%	V=
NWELL L/W=76/15.2				%	I=

3.6 Capacitances

Gate oxide capacitors

	Min	Nom	Max	Unit	Meas. cond.
Nchannel					
Tox	15.5	17.0	18.5	nm	Cmax (Vdnom)
Cplate				F/m2	calc. or meas
Vbd	12	20		V	I=1mA/cm2
CGDO	2.3e-10	3.1e-10	3.9e-10	F/m	TBD
CGSO	2.3e-10	3.1e-10	3.9e-10	F/m	TBD
Pchannel					
Tox	15.5	17.0	18.5	m	Cmax (Vdnom)
Cplate				F/m2	calc. or meas
Vbd	12	20		V	I=1mA/cm2
CGDO	1.9e-10	2.2e-10	2.6e-10	F/m	TBD
CGSO	1.9e-10	2.2e-10	2.6e-10	F/m	TBD

Precision analog capacitor (CAPA)

	Min	Nom	Max	Unit	Meas. cond.
Tox	40	45	50	nm	Cmax(Vnom)
Cplate	0.65	0.75	0.85	fF/µm2	calculated
Vbd	15			V	
VCL	1	25	50	ppm/V	Vstart=-5V step=0.2V Nbr steps=51
Matching of LxL=20x20		0.11		%	

Junction capacitances

	Min	Nom	Max	Unit	Meas. cond.
N+ with LDD to Pwell with field perimeter					
Cj	4.0E-4	5.0E-4	6.0E-4	F/m2	0V
Mj		0.32		-	fitted
Cjsw	1.6E-10	2.8E-10	4.0E-10	F/m	0V
Mjsw		0.23		-	fitted
Pb		0.68		V	fitted
P+ with LDD to Nwell with field perimeter					
Cj	4.8E-4	6.0E-4	7.2E-4	F/m2	0V
Mj		0.51		-	fitted
Cjsw	2.0E-10	3.6E-10	5.2E-10	F/m	0V
Mjsw		0.35		-	fitted
Pb		0.90		V	fitted
Junction n+CAPA/PWELL					
Cj	2.4E-4	2.7E-4	3.2E-4	F/m2	0V
Mj		0.812		-	fitted
Cjsw				F/m	0V
Mjsw				-	fitted
Pb		0.8		V	fitted
Nwell to substrate					
Cj	0.54E-4	0.74E-4	0.94E-4	F/m2	0V
Mj		0.274		-	fitted
Cjsw	6.3E-10	7.0E-10	7.7E-10	F/m	0V
Mjsw		0.247		-	fitted
Pb		0.439		V	fitted

Interconnect capacitances (for single line to ground)

Sakurai for single line to ground capacitances

$C = [1.15 (W/H) + 2.8 (T/H)^{0.222}]$ Eox in F/µ length

Cgnd = L * (W * Cplane + 2 * Cside)
where Cplane = 1.15/H in F/Um2

$Cside = 1.4 (T/H)^{0.222}$ in F/µ

T : Poly, Metal1, Metal2 or Metal 3 line thickness
H : Oxide thickness between Poly, M1, M2 and underlying layer

Other parameters:
W : Poly, Metal1, Metal2 or Metal 3 line width
L : Poly, Metal1,Metal2 or Metal 3 line length
Eox : 8.85e-14*3.9 [F/cm]

Nominal values are calculated using nominal H and T
Minimum values max H and min T
Maximum values min H and max T

C07M: nominal cap

Comment	H (Um)	T (Um)	Cplane (F/Um2)	Cside (F/Um)
POLY-WELL	0.5	0.425	7.94E-17	4.66E-17
M1-ACTIVE	0.75	0.8	5.29E-17	4.90E-17
M1-WELL	1.25	0.8	3.18E-17	4.38E-17
M1-POLY	0.75	0.8	5.29E-17	4.90E-17
M2-ACTIVE	1.8	0.9	2.21E-17	4.14E-17
M2-WELL	2.3	0.9	1.73E-17	3.92E-17
M2-POLY	1.8	0.9	2.21E-17	4.14E-17
M2-M1	1.05	0.9	3.78E-17	4.67E-17
M3-ACTIVE	2.85	1.0	1.39E-17	3.83E-17
M3-WELL	3.35	1.0	1.18E-17	3.69E-17
M3-POLY	2.85	1.0	1.39E-17	3.83E-17
M3-M1	2.1	1.0	1.89E-17	4.10E-17
M3-M2	1.05	1.0	3.78E-17	4.78E-17

C07M: maximum cap

Comment	H (Um)	T (Um)	Cplane (F/Um2)	Cside (F/Um)
POLY-WELL	0.45	0.45	8.82E-17	4.83E-17
M1-ACTIVE	0.65	0.86	6.11E-17	5.14E-17
M1-WELL	1.1	0.86	3.61E-17	4.58E-17
M1-POLY	0.65	0.86	5.14E-17	5.14E-17
M2-ACTIVE	1.55	0.95	2.56E-17	4.33E-17
M2-WELL	2. 0	0.95	1.98E-17	4.10E-17
M2-POLY	1.55	0.95	2.56E-17	4.33E-17
M2-M1	0.9	0.95	4.41E-17	4.89E-17
M3-ACTIVE	2.5	1.05	1.59E-17	3.99E-17
M3-WELL	2.95	1.05	1.35E-17	3.84E-17
M3-POLY	2.5	1.05	1.59E-17	3.99E-17
M3-M1	1.75	1.05	2.27E-17	4.31E-17
M3-M2	0.9	1.05	4.41E-17	5.00E-17

C07M: minimum cap

Comment	H (Um)	T (Um)	Cplane (F/Um2)	Cside (F/Um)
POLY-WELL	0.55	0.4	7.22E-17	4.50E-17
M1-ACTIVE	0.85	0.74	4.67E-17	4.69E-17
M1-WELL	1.4	0.74	2.84E-17	4.19E-17
M1-POLY	0.85	0.74	4.67E-17	4.69E-17
M2-ACTIVE	2.05	0.85	1.94E-17	3.97E-17
M2-WELL	2.6	0.85	1.53E-17	3.77E-17
M2-POLY	2.05	0.85	1.94E-17	3.97E-17
M2-M1	1.2	0.85	3.31E-17	4.48E-17
M3-ACTIVE	3.2	0.95	1.24E-17	3.69E-17
M3-WELL	3.75	0.95	1.06E-17	3.56E-17
M3-POLY	3.2	0.95	1.24E-17	3.69E-17
M3-M1	2.45	0.95	1.62E-17	3.92E-17
M3-M2	1.2	0.95	3.31E-17	4.59E-17

3.7 Diodes

Junction diodes

	Min	Nom	Max	Unit	Meas. cond.
N+ with LDD to Pwell					
Xj				µm	process
VBD		14		V	I=
ia at T = 20˚C T = 80˚C T = 140˚C		0.13 1.9 120		fA/µm^2 fA/µm^2 fA/µm^2	Vdmax
ipf at T = 20˚C T = 80˚C T = 140˚C		0.37 15 150		fA/µm fA/µm fA/µm	
P+ to Nwell					
Xj				µm	process
VBD		13.3		V	I=
i_a at T = 20˚C T = 80˚C T = 140˚C		1.1 1.5 78		fA/µm^2 fA/µm^2 fA/µm^2	Vdmax
ipf at T = 20˚C T = 80˚C T = 140˚C		0.04 5.0 160		fA/µm fA/µm fA/µm	
N+ CAPA to Pwell					
Xj				µm	process
VBD				V	I=
Ileak				pA/cm2	Vdmax

	Min	Nom	Max	Unit	Meas. cond.
Nwell to substrate					
Xj				µm	process
VBD		59		V	I=
i_a at T = 20˚C T = 80˚C T = 140˚C		1.1 2.0 50		fA/µm^2 fA/µm^2 fA/µm^2	Vdmax
ipf at T = 20˚C T = 80˚C T = 140˚C		4.1 6.9 400		fA/µm fA/µm fA/µm	

3.8 Poly Zap Structures **(are not allowed in combination with TLM)**

The layout of the poly diodes is fixed. See design rules.

Specifications for non zapped diodes

* Maximum leakage at 5.5V < 1 µA
* Zener diode Vbd > 5.5 V
* Maximum current in reverse bias < 50 µA

Specifications for zapped diodes

* Maximum Ron after zapping < 1 kOhm
* Maximum current after zapping < 50 µA

Zapping specifications

The diodes can be zapped with a voltage pulse
* Pulse voltage 14 - 17 V
* Pulse duration 5 - 15 ms
* Compliance current 30 - 60 mA

3.9 Zener zap diode for OTP (TLM compatible)

The layout of the Zener zap diode ZD224 is fixed : see DS-13297.

- Characteristics of the unzapped diode in reverse bias ($\pm 6\sigma$ limits) :

  VZ@1μA = 1.6 - 2.3 V
  VZ@50μA = 3.5 - 4.2 V
  Rdiff@1mA = 10-230 Ω

- Obligatory zapping window :

  Vzap = 9.5 ± 0.5 V
  tzap = 2.0 ± 1.0 μs
  VDD = 5.0 ± 0.5 V

- Characteristics of the zapped diode (-40°C<Tzap<+125°C) :

  VZ@50μA < 0.9 V
  Rzapped@50μA < 20 kΩ

The zapping window is only valid in conjunction with :

the PMOS top switch : W/L = 800/0.7 μm

the NMOS selection transistor :W/L = 182/0.7 μm

or equivalent devices.

3.10 Bipolar Transistors

Vertical PNP transistor Ae=460 μm^2

	Min	Nom	Max	Unit	Meas. cond.
Hfe _Ic	11	22	35	-	Ibstart=-10pA Ibstop=-100µA VCE=Vdmax Ic=1µA
Ikf_Hfe				µA	Ibstart=-10pA Ibstop=-100µA VCE=Vdmax Hfe=1/2Hfe_Ic
V Early		370		V	Ib=-100nA VCEsweep 0 to.Vdmax fit, X-intercept
BVCEO		30		V	Vce @Ic=1µA
Vbe	0.553	0.566	0.579	V	Ie = 1µA,T=294K
TCL Vbe		-2.35		mV/K	

3.11 NDmos transistors

NDMOS (NDMOS)
Lmain = 4.0 µ fixed see layout rules Ndmos as High voltage device.

Parameter	**Min**	**Nom**	**Max**	**Units**
Vt(0)	0.55	0.675	0.80	V
ß(lin) (W=40µ)	500	680	860	µA/V2
Slin	90.0	94.0	98.0	mV/decade
Ron (W=40µ)	664	794	1192	Ω
Ron.µ width (W>500µ)	-	-	-	kΩ.µ
|Vbd| (=Vmax)	40.0	-	-	V
Vgsmax	-	-	8	V
Ids@Vgs=1.5,Vds=20	167	238	315	µA
W=40µ				
Ids@Vgs=5,Vds=20	3488	4675	5340	µA
	W=40µ			
|VBS|			5	V
TCvt0	-	-	-1.47	mV/K
TCRon	-		+0.0054	%/K

This is a not-self-aligned device, the characteristics are orientation dependent. To obtain good matching, the devices should therefore be oriented in the same direction in the layout.

For this device the Vt0 is depending on the width. This is only partially covered by the model (which is only valid for W>20µ).

4.0 CHARACTERISATION MODELS

4.1 NMOS Current Matching

The dependence on the dimension of the current matching given in the figure is valid only for:
- 2 transistors designed in common centroid
- identical surrounding (equal distance to field, to capacitor plates, to metal lines)

The model for the gate voltage dependence of the current matching is:

$$(\sigma_{\Delta}Id/Id)^2=(\sigma_{VT0})^2*4/(Vg-VT0)^2 + (\sigma_{\Delta}ß/ß)^2$$

where

$$(\sigma_{VT0})^2=A^2\ VT0/WL + C^2\ VT0$$

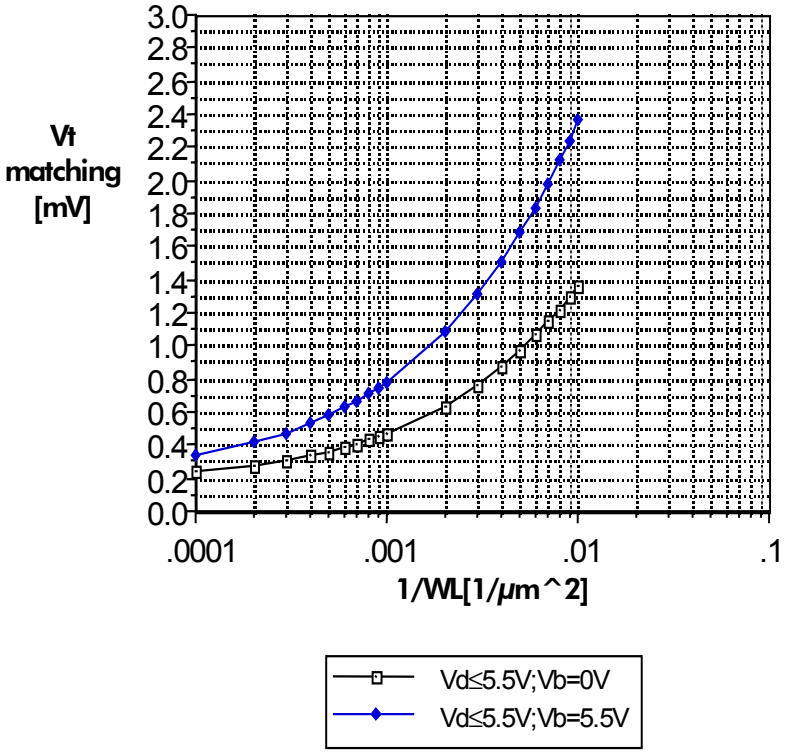
$$(\sigma_{\Delta}ß/ß)^2=A^2\ ß/WL + C^2\ ß$$

This model is valid only for transistors with $20 \le WxL \le 6500$, for transistors with channel length ≥ 2µm if $Vt0+0.2 \le Vg \le Vt0+2V$, and for all lengths if $Vt0+0.2 \le Vg \le Vt0+1V$.

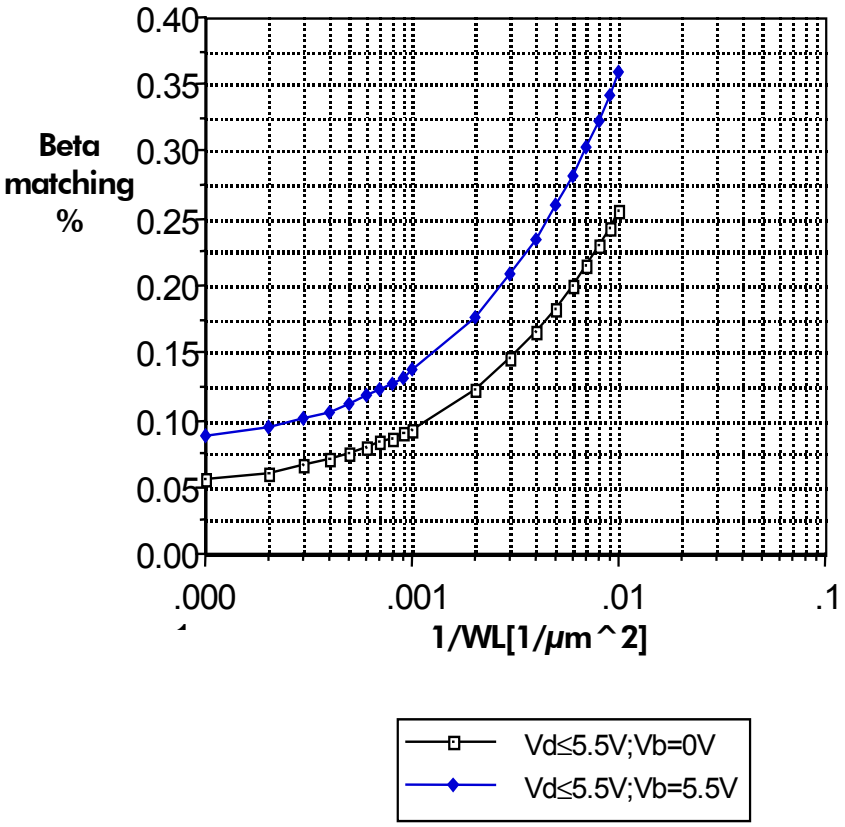
The fit constants A and C are given in the table for different Vd, Vbulk voltages.

	Vd3Vb0	**Vd5.5Vb0**	**Vd3Vb5.5**
Avt0 [mV*µm]	11.5	13.5	23.5
Cvt0 [mV]	0.2	0.2	0.25
Ab [%*µm]	2.5	2.5	3.5
Cb [%]	0.05	0.05	0.08

NMOS Threshold Voltage Matching (sVt0) vs Channel Dimensions



NMOS Beta Matching (sb/b) vs Channel Dimensions



4.2 PMOS Current Matching

The dependence on the dimension of the current matching given in the figure is valid only for:
- 2 transistors designed in cross-couple
- identical surrounding (equal distance to field, to capacitor plates, to metal lines)

The model for the gate voltage dependence of the current matching is:

$$(\sigma_{\Delta Id/Id})^2=(\sigma_{VT0})^2*4/(Vg-VT0)^2 + (\sigma_{\Delta ß/ß})^2$$

where

$$(\sigma_{VT0})^2=A^2\ VT0/WL + C^2\ VT0$$

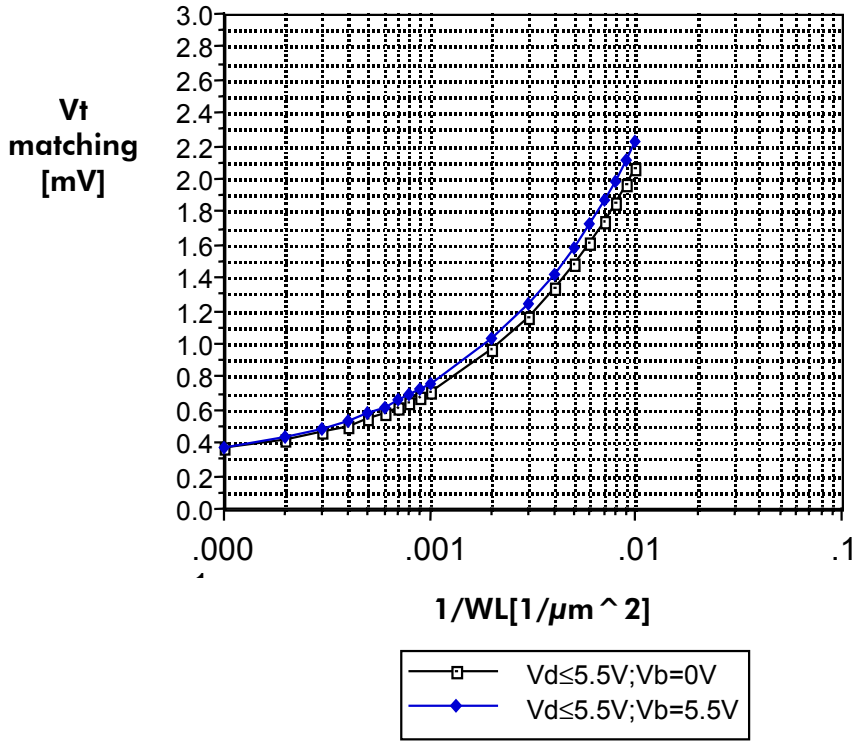
$$(\sigma_{\Delta ß/ß})^2=A^2\ ß/WL + C^2\ ß$$

This model is valid only for transistors with 20 ≤ WxL ≤ 6500, for transistors with channel length ≥ 2µm if Vt0+0.2≤Vg≤Vt0+2V, and for all lengths if Vt0+0.2≤Vg≤Vt0+1V.

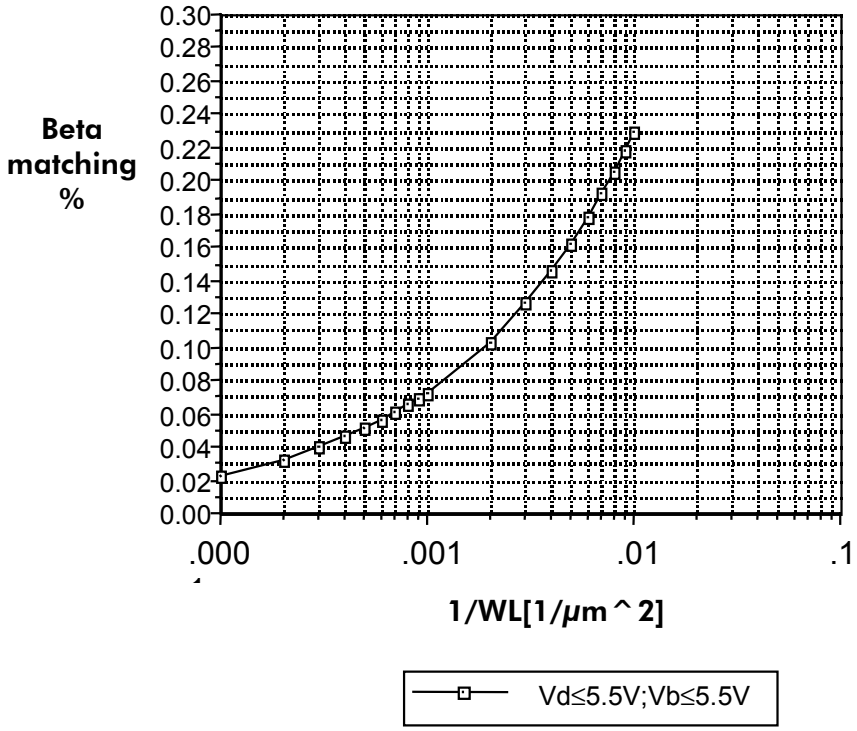
The fit constants A and C are given in the table for different Vd, Vbulk voltages

	Vd3Vb0	**Vd5.5Vb0**	**Vd3Vb5.5**
Avt0 [mV*µm]	19	20.5	22
Cvt0 [mV]	0.4	0.3	0.3
Ab [%*µm]	2.3	2.3	2.3
Cb [%]	0	0	0

PMOS Threshold Matching (sVt0) vs Channel Dimensions



PMOS Beta Matching (sb/b) vs Channel Dimensions



4.3 PMOS Low VT Current Matching

The dependence on the dimension of the current matching given in the figure is valid only for:
- 2 transistors designed in cross-couple
- identical surrounding (equal distance to field, to capacitor plates, to metal lines)

The model for the gate voltage dependence of the current matching is:

$$(\sigma_{\Delta Id/Id})^2=(\sigma_{VT0})^2*4/(Vg-VT0)^2 + (\sigma_{\Delta ß/ß})^2$$

where

$$(\sigma_{VT0})^2=A^2\ VT0/WL + C^2\ VT0$$

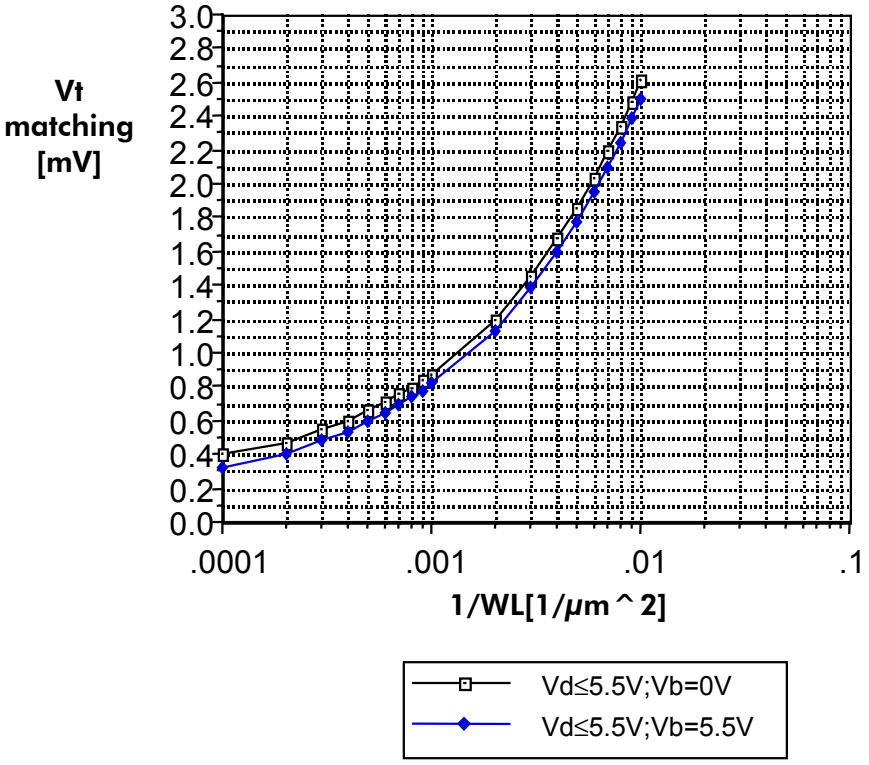
$$(\sigma_{\Delta ß/ß})^2=A^2\ ß/WL + C^2\ ß$$

This model is valid only for transistors with 20 ≤ WxL ≤ 6500, for transistors with channel length ≥ 2µm if Vt0+0.2≤Vg≤Vt0+2V, and for all lengths if Vt0+0.2≤Vg≤Vt0+1V.

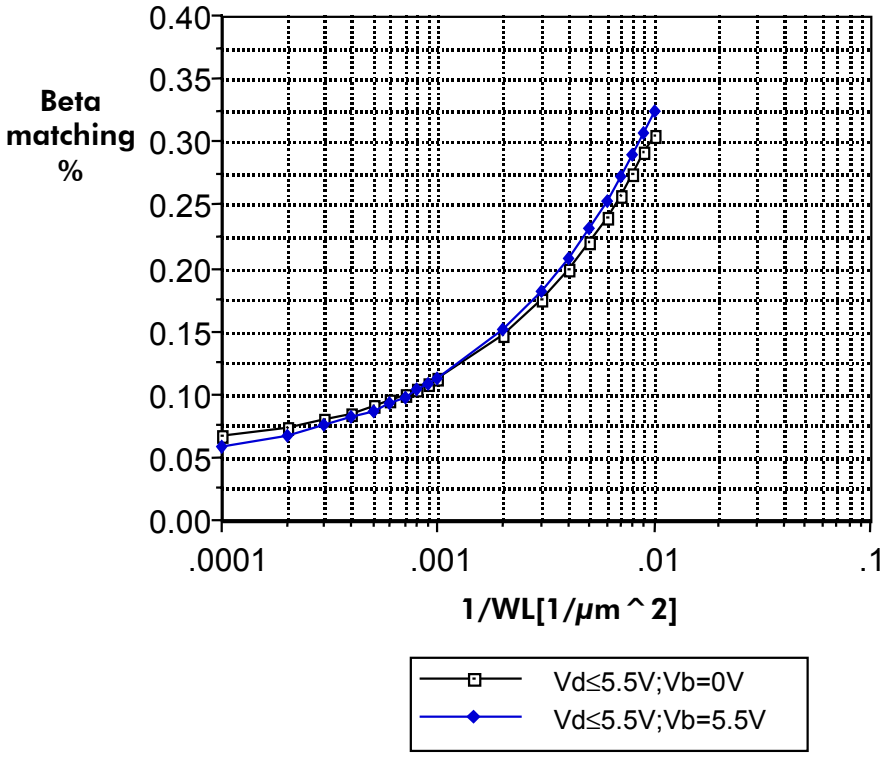
The fit constants A and C are given in the table for different Vd, Vbulk voltages

	Vd3Vb0	**Vd5.5Vb0**	**Vd3Vb5.5**
Avt0 [mV*µm]	23	26	25
Cvt0 [mV]	0.4	0.3	0.2
Ab [%*µm]	2.7	3	3.2
Cb [%]	0.04	0.06	0.05

PMOS Low VT Threshold Matching vs Channel Dimensions



PMOS Low Vt Beta Matching (sb/b) vs Channel Dimensions



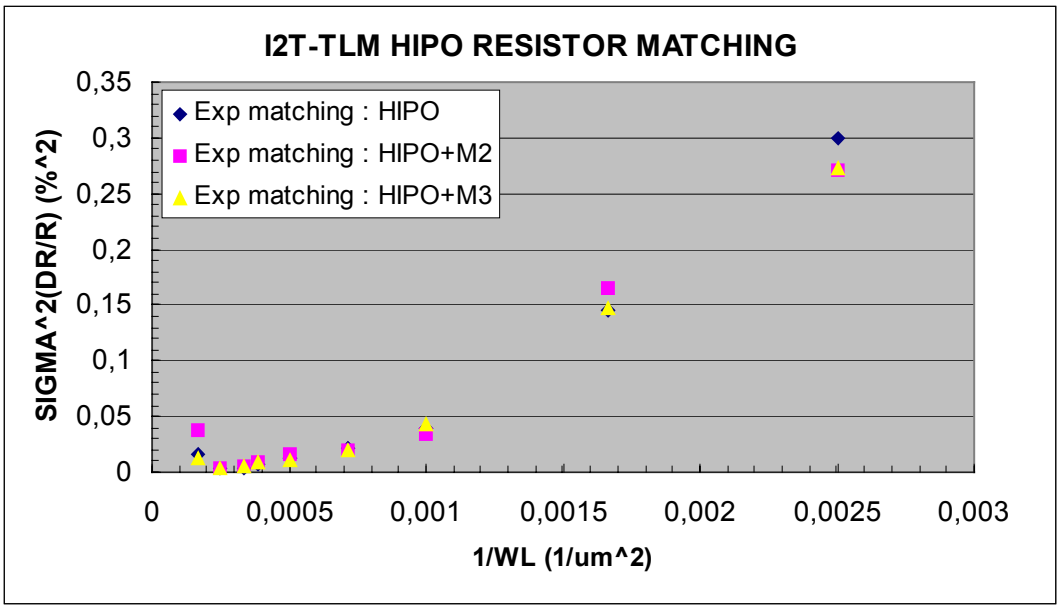
4.4 Resistor Matching

HIPO resistor matching vs resistor dimensions

The dependence on the dimension of the resistor matching given in the figure is valid only for:
- 2 parallel resistor bars placed on field on NWELL with equal lengths and widths
- placed on maximum distance D=10µm
- design with dummy resistors
- identical surrounding (equal distance to field, to capacitor plates, to metal lines)
- no metal 1 cross-over

HIPO Resistor Matching as a Function of 1/WL

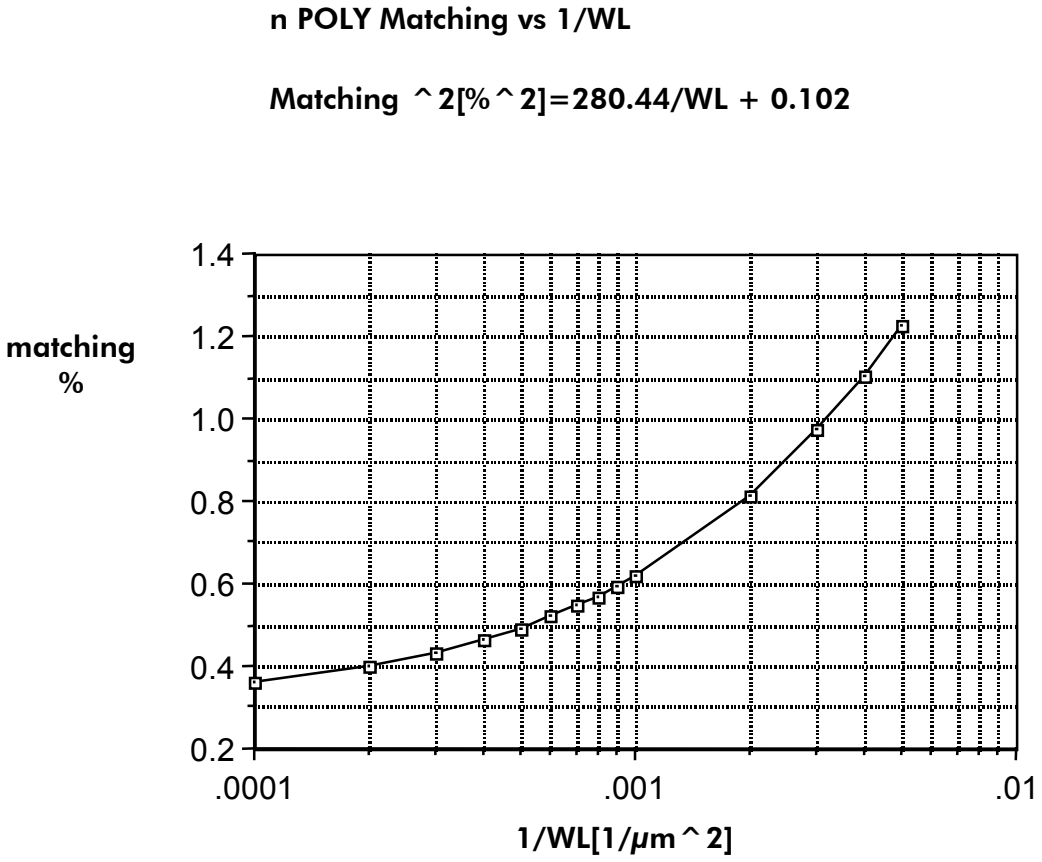
Matching ^2[%^2]=95.26/WL+0.00



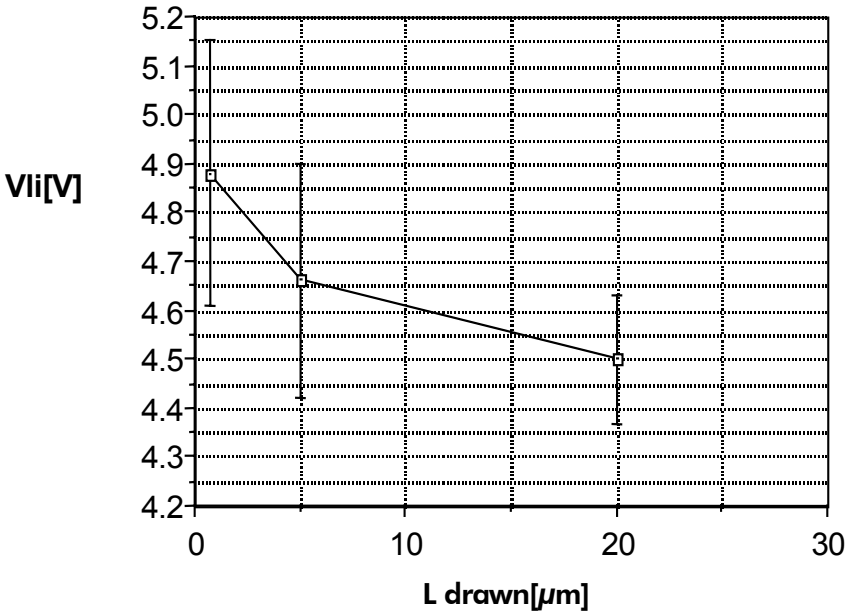
POLY resistor matching vs resistor dimensions

The dependence on the dimension of the resistor matching given in the figure is valid only for:

- 2 parallel resistor bars placed on field on NWELL, designed with minimum distance to active 0.9µm, with equal lengths and widths
- placed on maximum distance D=10µm
- design with dummy resistors
- identical surrounding (equal distance to field, to capacitor plates, to metal lines)

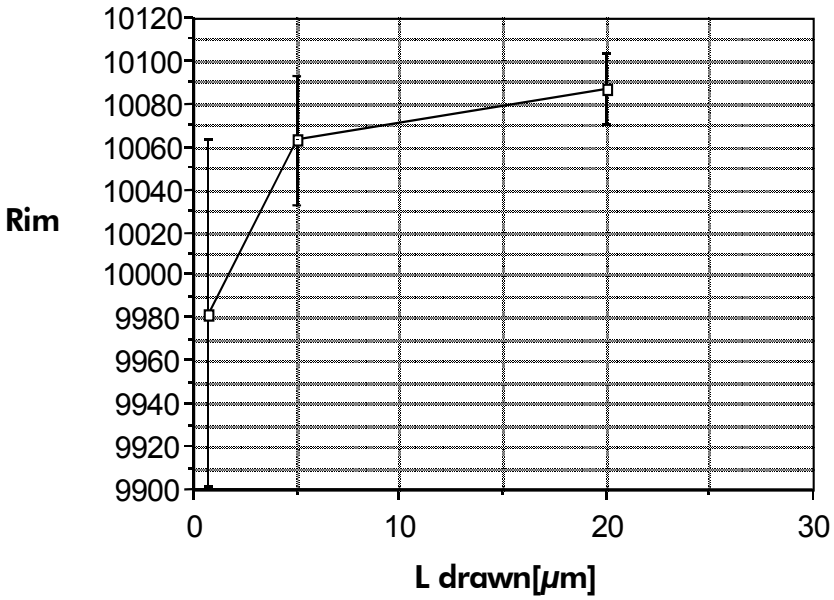


Drain Voltage Vli for 0.1% Deviation of the Drain Current at Vgisubmax; Vb=0V



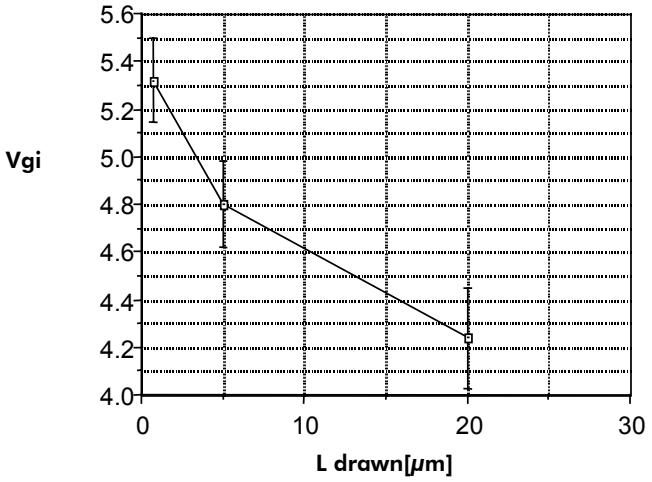
Rim=Id@Vd=5.5V/Id@Vd=5.5V fitted * 10000

- Ratio between Measured and Fitted Drain Current at Vd=5.5V

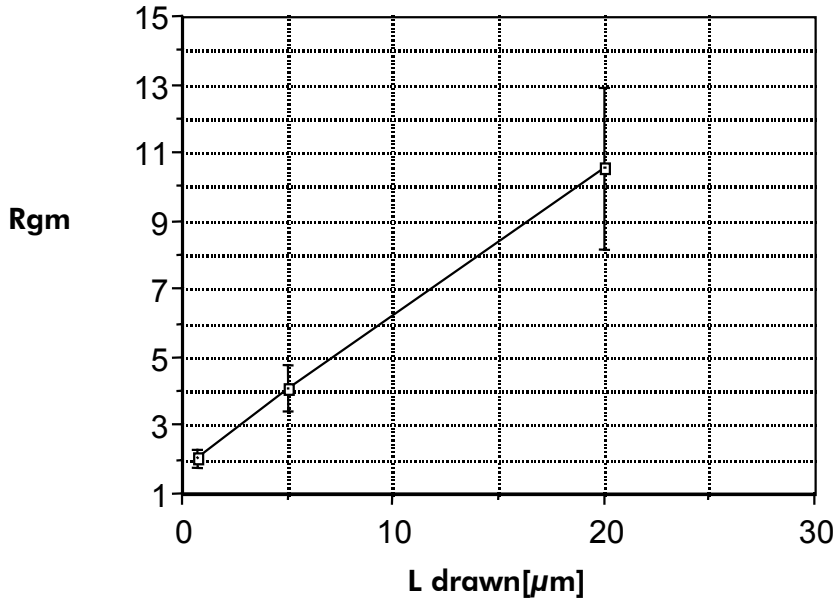


Rim

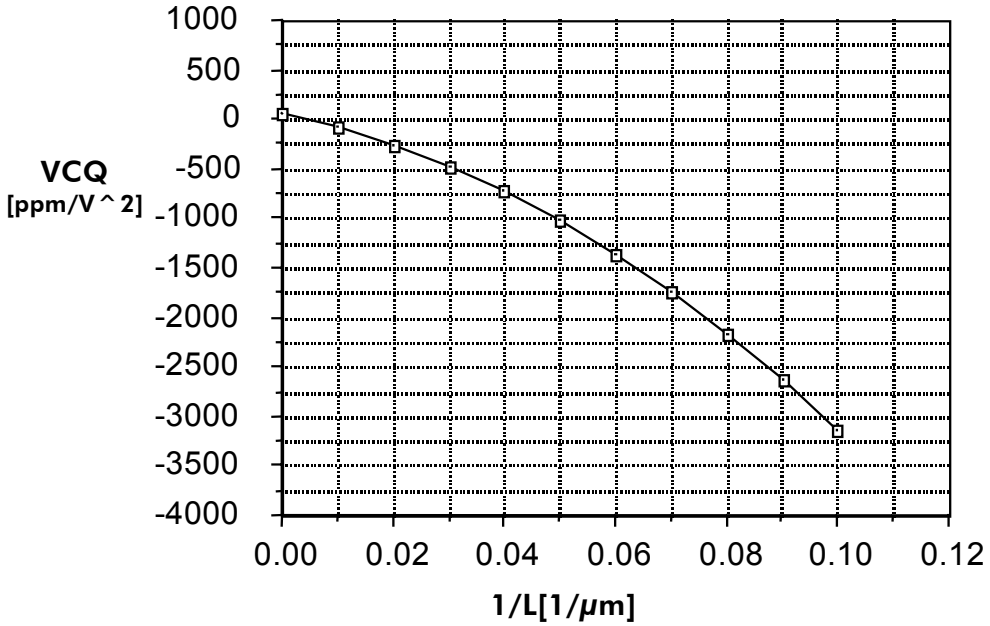
Vgi - Drain Voltage for Gds=2*Gds@Vd=3V



Rgm=Gds@Vd=5.5V/Gds@Vd=3V



Worst Case Quadratic Voltage Coefficient of HIPO at 300K vs Resistor Length



5.0 RELIABILITY GUIDE LINES

5.1 Life time of Nmos devices

Introduction

When nmos transistors operate in deep saturation, impact ionisation becomes important. This impact ionisation causes hot carrier injection in the gateoxide close to the drain. As a result Vt is increasing and gm is decreasing.

The waffab route qualification specification GP15502 guarantees that these parameter changes remain within certain limits during 25 years of continuous operation in worst case degradation conditions i.e.

- Vd = Vdd_maximal and
- Vg at maximum impact ionisation = at Isub max (close to Vd/2-0.5V)

In these conditions the nmos parameter changes are limited to:

- gm degradation < 10%
- Vt increase < 100mV

However for the C07M technology, the 25 year lifetime is only garanteed for continuous operation at Vdd_nominal (5V), in stead of Vdd_maximal (5.5V).

Design restrictions for continuous operation at Vdd_maximal

For continuous operation at Vdd_maximal, being 5.5V and maximal degradation conditions the gm degradation cannot be kept below 10% after 25 years.

In these particular case longer gate lengths will have to be used in order to keep the gm shift below the specified limits.

The gate length that has to be chosen for gm degradation <10% is given in figure 1. This figure takes into account the worst case processing conditions with respect to hot carrier performance.

The Vt shift remains below 10mV by the time 10% gm is reached and hence this parameter shift in not important for the choice of the gate length.

Design restrictions for less degradation

When a designer is interested in less gm degradation, figures 2 and 3 can be used in order to determine the gate length depending on drain voltage.

The Vt shift remains below 1mV by the time 2.5% gm is reached and hence this parameter shift is not important for the choice of the gate length.

AC lifetime calculation

For transistors which are not operating continuously in worst case degradation conditions, the real lifetime (AC lifetime) can be calculated from the DC lifetime according to the following formula:

AC lifetime = DC lifetime x (Time current≠0)/Total period

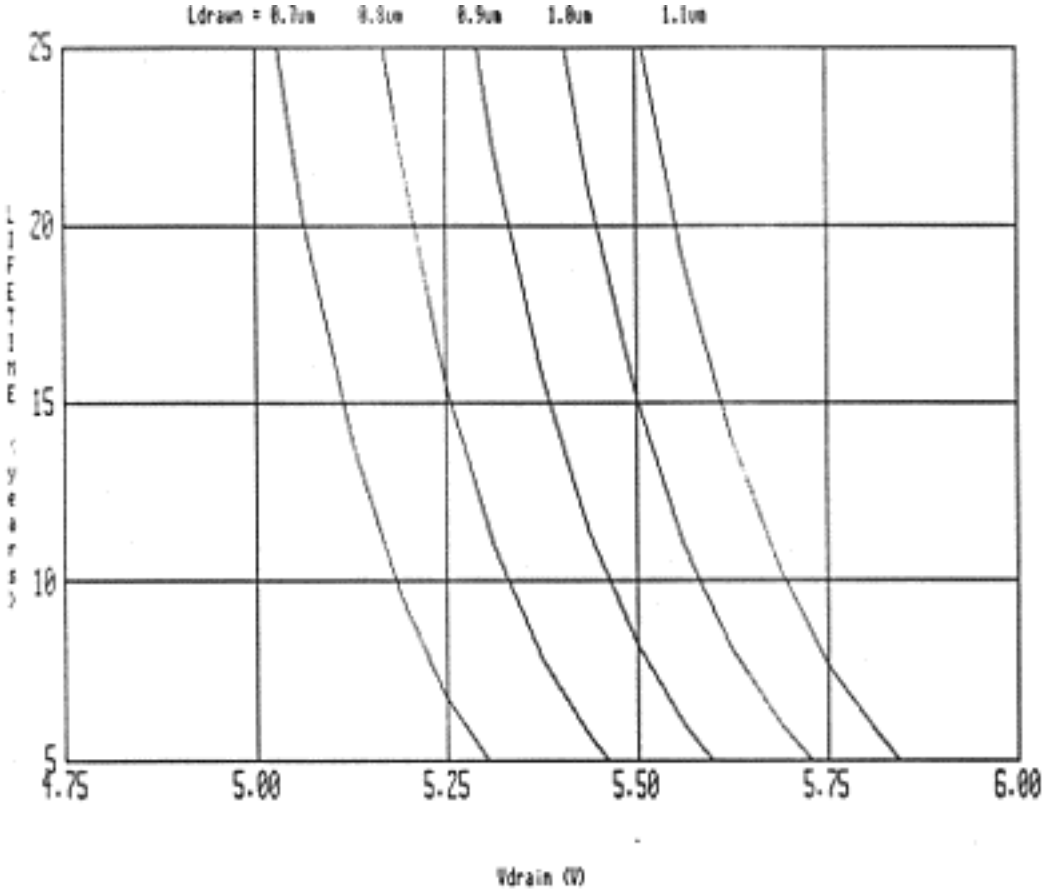
assuming that there is no voltage overshoot above 5.5V

For digital CMOS circuitry, this formula becomes:

AC lifetime = DC lifetime x (Trise + Tfall)/Total period

Figure 1: DC lifetime in function of Vdrain for different gate lengths for 10% gm degradation

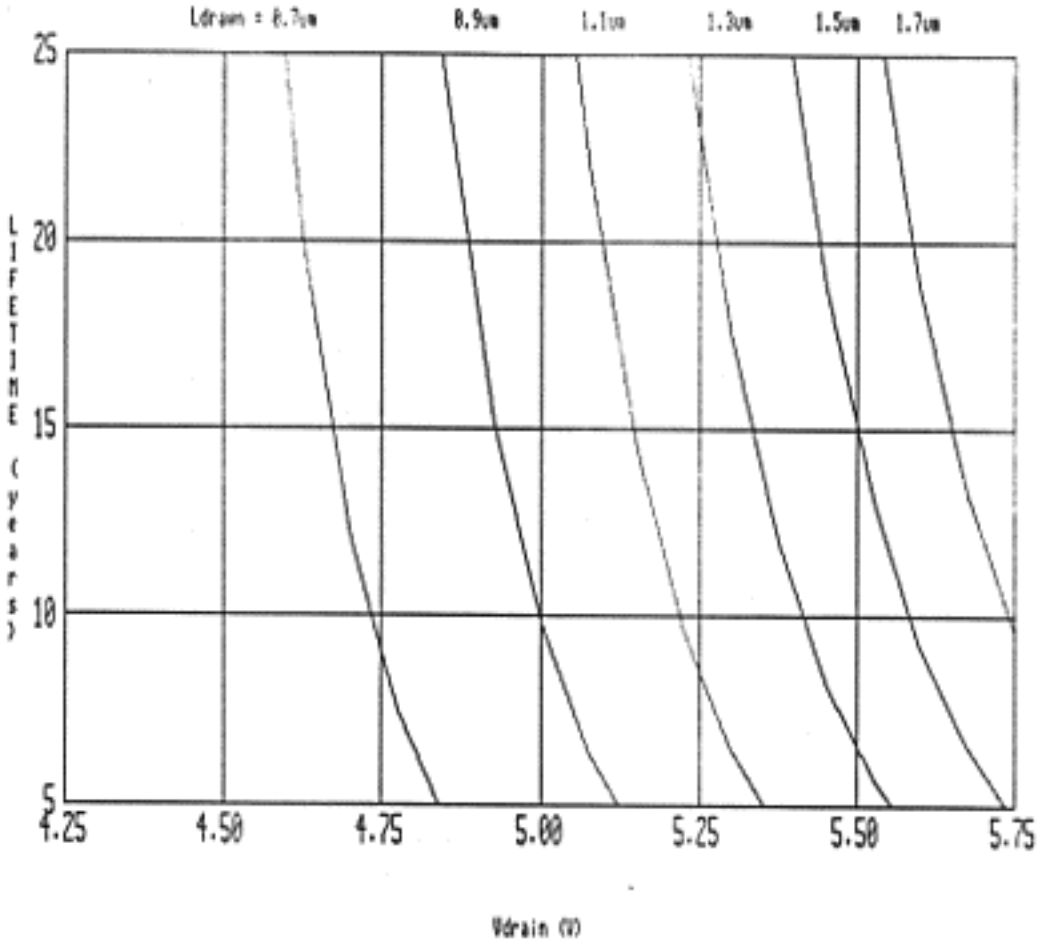
(Assuming worst case processing conditions and worst case degradation conditions)



Log10 (lifetime) = 67.30/Vdrain + 4.727xlog10 (Ldrawn-0.18) - 10.65

Figure 2: DC lifetime in function of Vdrain for different gate lengths for 5% gm degradation.

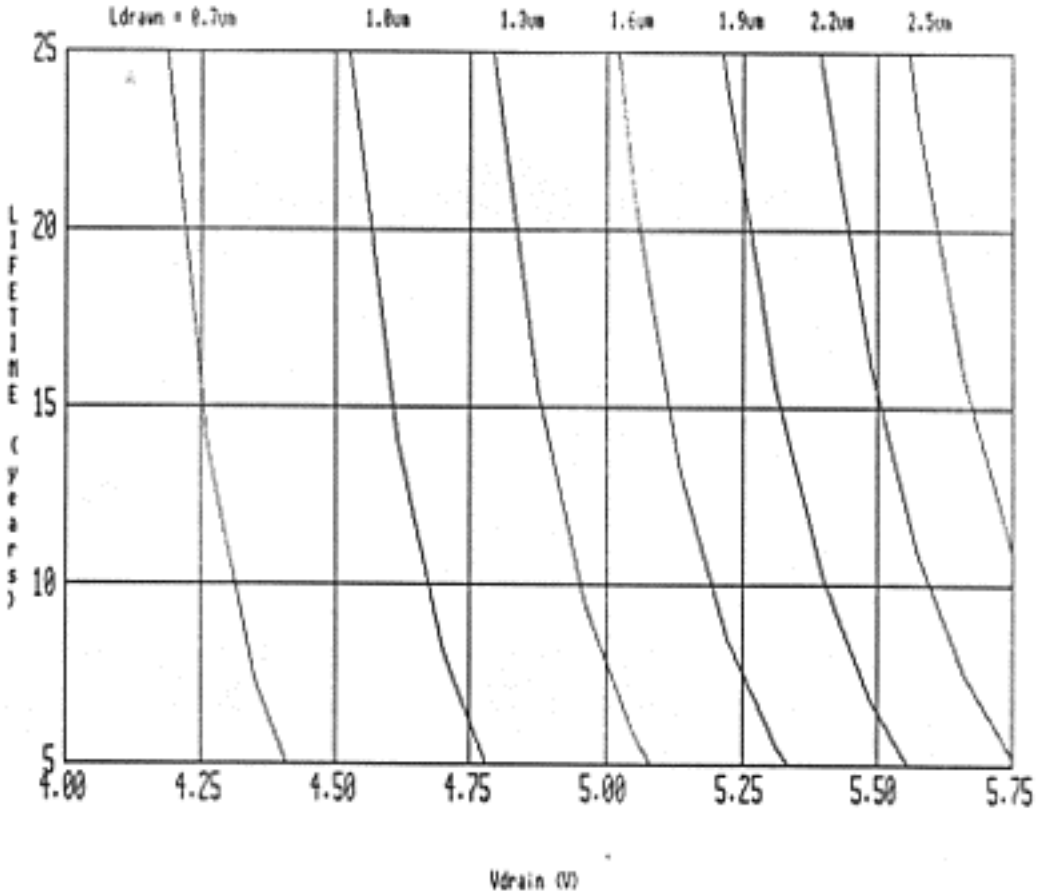
(Assuming worst case processing conditions and worst case degradation conditions)



Log10 (lifetime) = 63.37/Vdrain + 5.063xlog10 (Ldrawn-0.18) - 10.96

Figure 3: DC lifetime in function of Vdrain for different gate lengths for 2.5% gm degradation

(Assuming worst case processing conditions and worst case degradation conditions)



Log10 (lifetime) = 59.46/Vdrain + 5.400xlog10 (Ldrawn-0.18) - 11.28

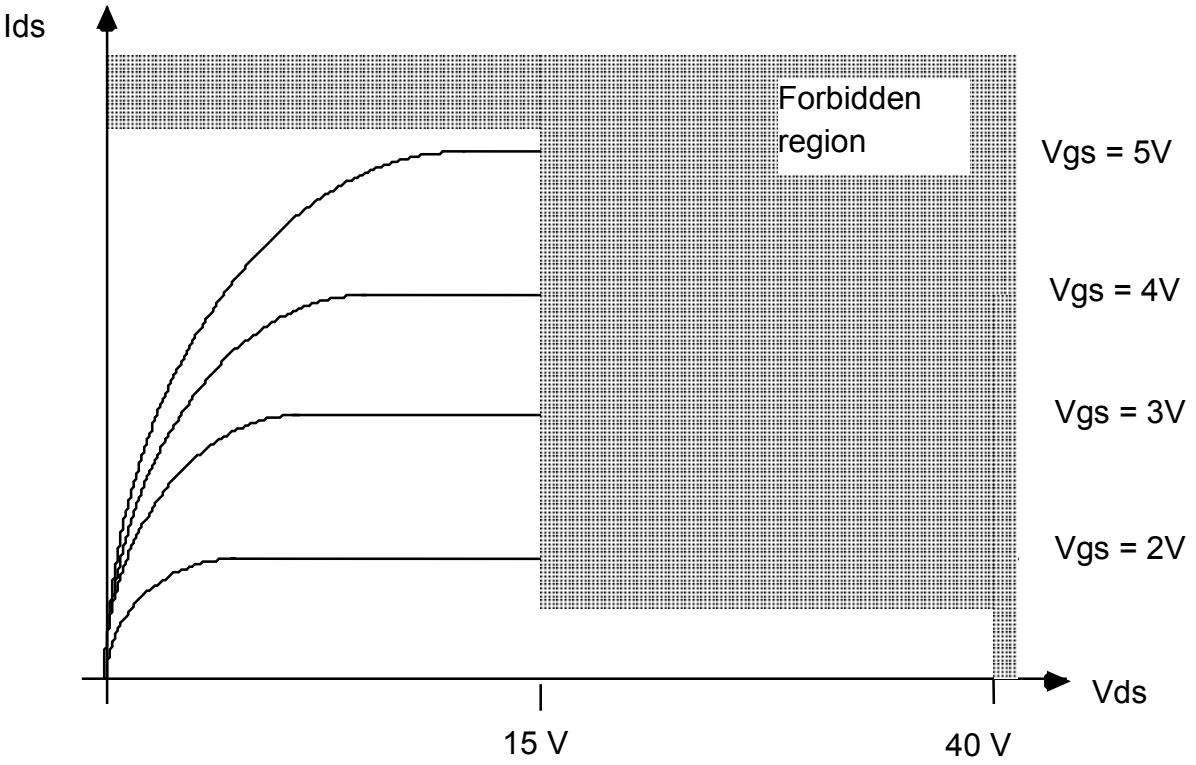
5.2 DMOS Devices

For DMOS devices, two phenomena limit the safe operating area.

The first is the turn-on (and subsequent breakdown) of the parasitic bipolar (NPN for the NDMOS devices). The turn on of the parasitic bipolar is triggered by the DMOS substrate current that biases the Emitter/Base junction of the parasitic bipolar forwards. This phenomenon is thus dependent on the currents that flow in the device. The turn on of the bipolar happens immediately and subsequently the DMOS device is destroyed. Operating the DMOS device in the region where this can happen is therefore strictly forbidden.

A second phenomenon is the degradation of the DMOS characteristics with time, as the device is operated at high voltages or currents. This can be compared with the classic hot carrier degradation of conventional MOS transistors. Operating the devices in this region does not induce immediate destruction of the device; continuous operation of the transistor in this region can induce shifts in the electrical parameters which are very large. The border of the safe operating region for this phenomenon is defined by a maximal degradation of 10% of any prime electrical characteristic (Vt0, Betalin, Ron, Idsat at Vgsmax) after 25 years of continuous operation at this condition.

An example of the Safe Operating Area is given in the figure below.



Safe Operating are imposed by hot carrier degradation.

5.2.1 Safe Operating Area imposed by bipolar turn on

NDMOS

Vgs<5.5V and Vds<40V

The minimum lifetime over the whole operating region is 1E4 seconds

5.2.2 Safe Operating Area imposed by degradation

NDMOS

Vgs<5.5V and Vds<15V and
Vgs< 0.5V and Vds<40V

The lifetime in this region is guaranteed over more than 25 years