LAYOUT RULES CMOS 0.7 µm ENHANCED

Owner : Technology Engineering Cmos

Location : N.A.

REVISION STATUS SUMMARY

Revision	Requestor	Date	Request Number	Pages	Description
01	TC	01-06-1999	20583	01-61	New document.
02	TC	24-11-1999	21576	35-56 27,31 23,29,25	Update for TLm rules Allow 1 um contacts & Vias for Old circuitry Allow smaller poly to active, remove wider M1 spacing for longer tracks. & P+ overlap -> 0.5 µm
03	TC	07-04-2000	22372	24	Change Hipo dope protect overlap from 3 to 5 to be compatible with maskgen. prog.
04	HVH	14-12-2000	23662	19, 24, 40, 51	Line up layout rules with maskgeneration Add poly diode - change bondpadrules
05	AL	11-05-2001	24450	51-65	Addition of zener diode for use in OTP cell ("zener zapp" approach)
06	EDB	19-11-2001	25413	1,58, 59,60	Refer to assembly rules for scribewidth. Update die seal ring rules.
7.0	DB, AL,ADM	22-04-2002	26247	1,2,4,11, 15,43,55 ,56	References to EEPROM route + updated bondpad rules. + Transfer to new template
8.0	ADM	09-01-2003	27575	46, 50,51,52	Update for new Die Seal Ring + update p.46.
9.0	ADM	03-06-2003	28296	50,51,52	Update of Scribe Lane
10.0	ADM	13-10-2003	28970	1,7,13, 27,29	Update for nlddprot, nplusprot and pldd layers.
11.0	PC	12-07-2004	30229	31, 34, 36	Use of wider metal lines in open areas of more than 10 µm.

TABLE OF CONTENTS

1.0 SCOPE & INTRODUCTION

This document provides the AMI Semiconductor Belgium Specification for Layout rules for 0.7 µm CMOS Enhanced.
The 0.7 µm CMOS Enhanced uses the same technology as for the Multi-purpose 0.7 µm CMOS but differs from the fact that more aggressive layout rules for e.g. interconnections, contacts are used. The dimensions of the core transistors (Width and Length) however remains the same. Also no change is done in layout rules for the analogue part.
The Enhanced 0.7 µm CMOS technology family C07E consists of different technology routes: next to the core digital route (single poly, double metal CMOS flow for digital applications), the following options are available :

- Analogue options : - low Vt PMOS transistors
  - Poly to n+ diffusion analogue capacitors
  - High Ohmic poly resistors.
- Route with enhanced PMOS Vt matching.
- OTP option
- Triple metal process.
- Process with polyimide passivation (in case of plastic assembly and when the chip area exceeds 120 mm^2).
- EEPROM route.

Please note that not all the combinations of options are released. Please contact the owner of this Spec for more details.

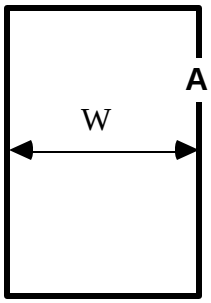
> Refer to AMI Semiconductor Belgium specifications DS13291 (=>core digital and mixed digital/analog for electrical design rules.
> Refer to AMI Semiconductor specification Belgium DES-0021 “Appendix to CMOS 0.7 µm and I2T100 Layout Rules manuals for NVM module”.

2.0 TERMS AND DEFINITIONS

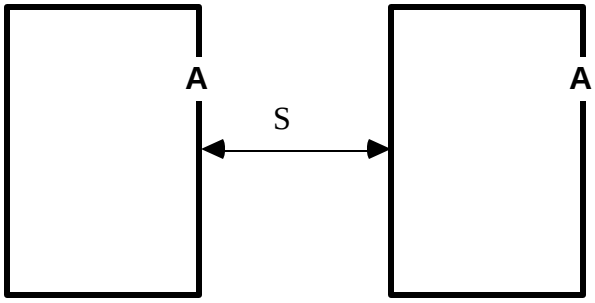
2.1 Convention for Specifying Layout Rules

The following conventions are used to specify the layout rules in this document:

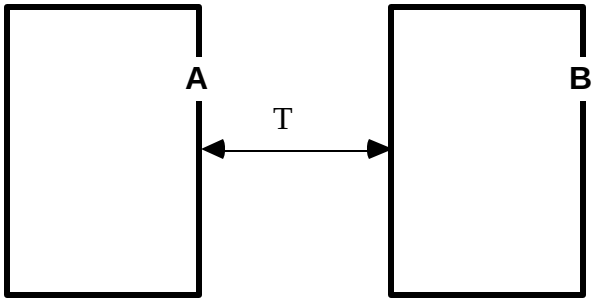
a. Width "W" of level A is defined as:



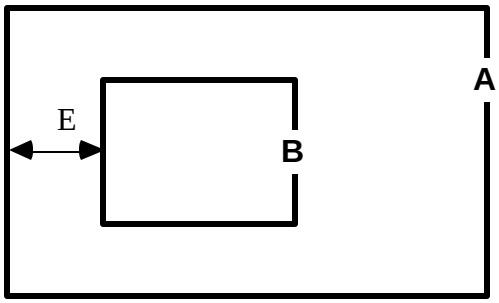
b. Spacing "S" of level A is defined as:



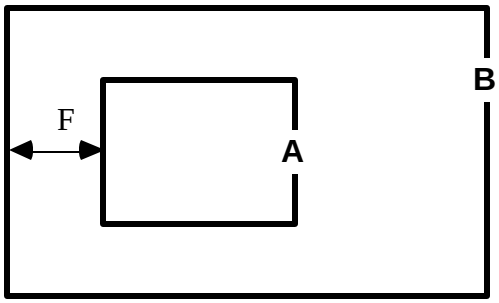
c. Spacing "T" between level A and level B is defined as:



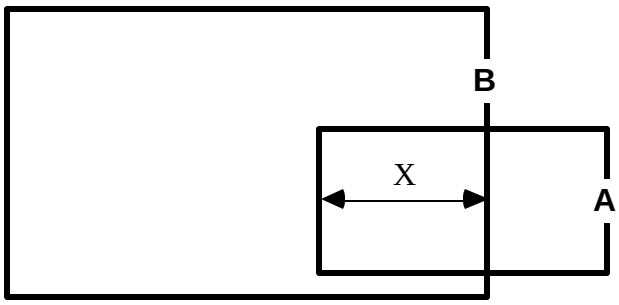
d. Level A enclosure "E" of level B is defined as:



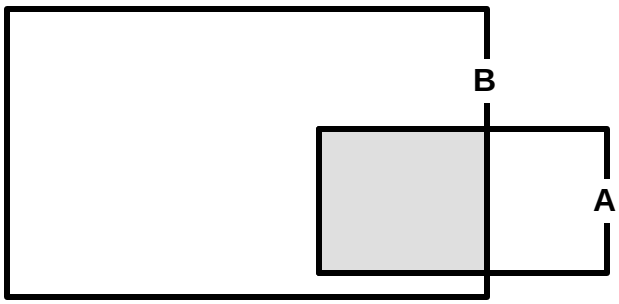
e. Level A enclosure "F" by level B is defined as:



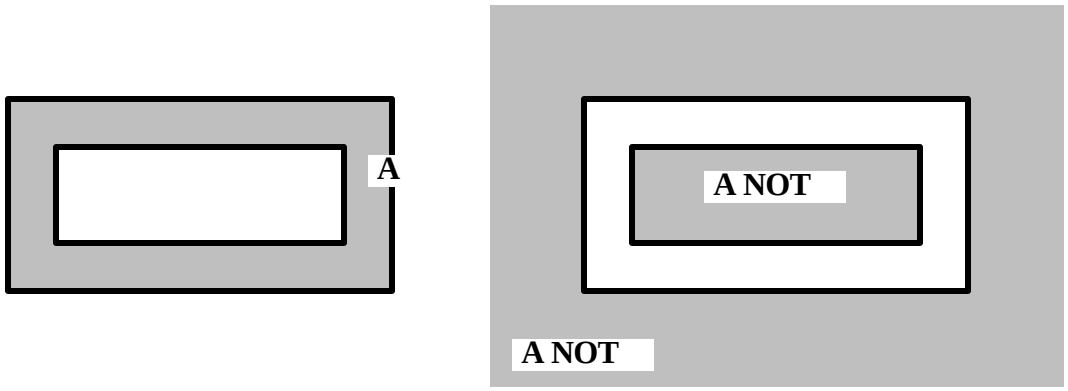
f. Level A intersection "X" with level B is defined as:



g. Level A "AND" level B is defined as the area common to both:



h. Level "A NOT" is defined as the complement of level A:



2.2 Logical Description of Derived Geometries

This section describes the geometries of the CMOS 0.7 µm processes as a logical operation between drawn layers:

P+_DIFFUSION	=	(P+_IMPLANT) OR (NOGEN AND P+_IMPLANT AND PLDD)
N+ ACTIVE AREA	=	ACTIVE AREA AND (NOT P+_DIFFUSION) AND (NOT POLYSILICON) AND (NOT NPLUSPROT) AND (NOT NLDDPROT)
P+ ACTIVE AREA	=	ACTIVE AREA AND P+_DIFFUSION AND (NOT POLYSILICON)
FIELD	=	NOT ACTIVE AREA
NMOS_FIELD	=	(NOT ACTIVE AREA) AND (NOT N-WELL)
N+ SOURCE/DRAIN	=	N+ ACTIVE AREA AND (NOT N-WELL)
P+ SOURCE/DRAIN	=	P+ ACTIVE AREA AND N-WELL
SOURCE/DRAIN	=	N+ SOURCE/DRAIN OR P+ SOURCE/DRAIN
N-WELL STRAP	=	N+ ACTIVE AREA AND N-WELL
SUBSTRATE STRAP	=	P+ ACTIVE AREA AND (NOT N-WELL)
GATE	=	ACTIVE AREA AND POLYSILICON

N-CHANNEL GATE	=	GATE AND N+ AND (NOT N-WELL)
P-CHANNEL GATE	=	GATE AND P+ AND N-WELL
POLYSILICON INTERCONNECT	=	POLYSILICON AND (NOT GATE) AND (NOT HIPO_DOPEPROTECT)
ENDCAP	=	POLYSILICON EXTENSION OF THE TRANSISTOR GATE IN THE WIDTH DIRECTION
HIPO RESISTOR	=	POLYSILICON AND HIPO_DOPEPROTECT AND (NOT DSP)
POLYSILICON OF HIPO RESISTOR	=	POLYSILICON AND HIPO_DOPEPROTECT
LOW VT PMOS TRANSISTOR	=	P-CHANNEL GATE AND LOW_VTP_IMPLANT
IMPLANTED CAPACITOR	=	ACTIVE AREA AND ACTIVE AREA CAPA_IMPLANT AND POLY
IMPLANTED CAPACITOR POLYSILICON	=	(ACTIVE AREA AND CAPA_IMPLANT) AND POLYSILICON
BOND PAD VIA	=	VIA CUTTING OVERLAY

3.0 MASK IDENTIFICATION

3.1 General Requirements for IGS Layer Numbering

AMI Semiconductor Belgium will only accept data tapes if they meet the requirements listed below:

3.1.1 Layout data must be present on the correct IGS layers as given in the sections 3.3, 3.4 and 3.5 below.

3.1.2 No layout data must be present on other IGS layers than those indicated in this document.

3.1.3 IGS layer 3 (Not_FIELD) and IGS layer 16 (Not_N+_IMPLANT) are automatically generated, unless in these areas covered by IGS layer 61 (NO_GEN).
On these IGS layers, all data that is not covered by IGS layer 61 will be ignored during mask preparation.

3.1.4 The Hipo resistors and CAPA resistors are protected from the N+/P+ implant.
Layer DSP is used to add P+ implant to contacts on HIPO resistors, and is added to data used for the P+ mask generation.
IGS layer 9 (DSP) has to be drawn (NO AUTOMATIC GENERATION) for C07M-A products, using the design rules given in this document (refer to § 4.5)

3.1.5 In principle, non-layout data such as CD-structures, layer identifications and/or revision numbers, logo's, test structures etc., must not introduce any layout rule violations; when layout rule violations can not be avoided, the customer shall always notify AMI Semiconductor Belgium prior to tape delivery, about the cell-names of the structures not complying with this layout rule document.

3.1.6 For ESD protection purposes, larger contacts and vias might be present in I/O circuitry.

3.1.7 To allow use of the AMI Semiconductor Belgium Bonding- (or Probecard) Diagram Editor, all bondpads should be labeled using layer 'dractext' (IGS layer 15). Labels must have an unique name per pad. Labels must have the origin inside the bondpad passivation.

3.2 Mask Identification C07E-D

Mask	IGS layer	Description
10	1	N-WELL
20	2	ACTIVE_AREA
30	3 (†)	Not_FIELD_IMPLANT
90	13	POLYSILICON
110	16 (†)	Not_N+_IMPLANT
120	17	P+_IMPLANT
130	19	CONTACTS
140	23	METAL 1
150	25	VIAS
160	27	METAL 2
170	31	OVERLAY

(†) These layers must not be drawn and will be generated automatically (refer to 3.1.3 for exceptions). Refer to AMI Semiconductor Belgium specification 13299 "Mask Generation CMOS 0.7 µm Enhanced" for mask generation details.

3.3 Mask Identification C07E-A

Mask	IGS layer	Description
10	1	N-WELL
20	2	ACTIVE_AREA
30	3 (†)	Not_FIELD_IMPLANT
60	22	LOW_VTP_IMPLANT
70	20	CAPA_IMPLANT
80	21	HIPO_DOPEPROTECT
	52	LOWACC
90	13	POLYSILICON
110	16 (†)	Not_N+_IMPLANT
120	17	P+_IMPLANT
	9	DSP
130	19	CONTACTS
140	23	METAL 1
150	25	VIAS
160	27	METAL 2
170	31	OVERLAY

(†)These layers must not be drawn and will be generated automatically (refer to 3.1.3 for exceptions). Refer to AMI Semiconductor Belgium specification 13299 "Mask Generation CMOS 0.7 µm Enhanced" for mask generation details.

3.4 Mask Identification C07E-T

Mask	IGS layer	Description
10	1	N-WELL
20	2	ACTIVE_AREA
30	3 (†)	Not_FIELD_IMPLANT
90	13	POLYSILICON
110	16 (†)	Not_N+_IMPLANT
120	17	P+_IMPLANT
130	19	CONTACTS
140	23	METAL 1
150	25	VIA1
160	27	METAL 2
180	32	VIA2
190	34	METAL 3
170	31	OVERLAY

3.5 Mask Identification NV7M_A

Mask	IGS layer	Description
10	1	N-WELL
20	2	ACTIVE_AREA
30	3 (†)	Not_FIELD_IMPLANT
75	43	TUNNEL WINDOW
90	13	POLYSILICON
105	55 (*)	PLDD_IMPLANT
110	16 (†)	Not_N+_IMPLANT
115	54 (†)	Not NLDD_IMPLANT
120	17	P+_IMPLANT
130	19	CONTACTS
140	23	METAL 1
150	25	VIA1
160	27	METAL 2
180	32	VIA2
190	34	METAL 3
170	31	OVERLAY

(†)These layers must not be drawn and will be generated automatically.
(*) These layers can be Drawn or Generated.

Here an overview of the layers and masks and a comparison with the similar technologies.

Mask	IGS Layer	Layer Name	Layer Function Description	I2T	C07	NVM
10	1	nwell	MASK, substrate of 5V pMOS	D	D	D
20	2	active	Mask,active area	G	D	D
30	3	nofield	Mask,not field implant	D+G	G	G
-	4	Field	Inhibit generation of nofield	D	-	-
5	5	ntub	Mask, N-diffusion	D	-	-
55	6	pbody	Mask,channel of nDMOS, base of NPN	D+G	-	-
-	7	boundry	Help layer for isolation	D	-	-
-	8	L8	Not used	-	-	-
-	9	dsp	Hipo contact heads	-	D	D
-	10	nvtpoly0	Eliminate vtpoly0/ only optional for redesigns in i2t	D	-	-
-	11	hvmet1	Helping layer for isolation	D	-	-
-	12	hvmet2	Helping layer for isolation	D	-	-
90	13	poly	Mask, 5V poly gate	D	D	D
-	14	ppoly	P+ doped poly used as resisor head	D	-	-
-	15	dractxt	Helping layer for bonding labels	D	D	D
110	16	ndiff	Mask, not N+diffusion	G	G	G
120	17	pdiff	Mask, P+ diffusion	G	D	D
-	18	npoly	Help layer (Hipo + N+ implant	D	-	-
130	19	contact	Mask, contact	D	D	D
70	20	capimpl	Mask,bottom N+ diffision for capacitors	D	D	D
80	21	hipoprt	Mask, protect poly from gate poly doping	G	D	D
60	22	lowvtp	Mask,Vt implant for 5V low vt pmos	D	D	D
140	23	metal1	Mask, 1st interconnect layer	D	D	D
-	24	pdifres	P+ dif. Resistor / Help layer for LVS	D	D	D
150	25	via	Mask, to connect metal1 and metal2	D	D	D
-	26	polyres	Defines poly res 20 Ohm for LVS	D	D	D
160	27	metal2	Mask, 2nd interconnect layer	D	D	D
-	28	mrkpnp	Defines PNP for LVS	D	D	D
-	29	nwellres	Defines Nwell res for LVS	D	D	D
-	30	mrkdio	Defines diodes for LVS	D	D	D
170	31	overlay	Mask, passivation openings	D	D	D
180	32	via2	Mask, to connect M2 to M3	-	D	D
-	33	met1res	Defines M1 resistors for LVS	D	D	D
190	34	metal3	Mask, 3rd interconnect layer	-	D	D
-	35	met2res	Defines M2 resistor for LVS	D	D	D
-	36	pwell	Drawn pwell	D	-	-
-	37	dtunimp	Old NVM concept	-	-	-
15	38	nopwell	Mask, inhibit pwell implant	D+G	-	-
40 *	39	vtpoly0	Mask, Vt impl for old Pdmos Only optional for redesigns	-	-	-
50	40	poly0	Mask, 12V poly gate	D	-	-
-	41	imid	Polyimide for big dies	-	D	D
-	42	nwell40	Nwell at higher voltages	D	-	-
75	43	dtunwin	Mask, drawn tunnel window	-	-	D

Mask	IGS Layer	Layer Name	Layer Function Description	I2T	C07	NVM
-	44	nopdiff	Do not use	-	-	-
-	45	dracula	DRC flags	D	D	D
-	46	naa	All active area n-type	D	-	-
-	47	paa	All active area p-type	D	-	-
2	48	bln	Mask, N+ buried layer	G	-	-
-	49	nomos	Helping layer for LVS	D	D	D
-	50	hvcover	Mask, process related Only optional for redesigns	-	-	-
-	51	boord	Border	D	D	D
-	52	low-acc	Low accurecy resistors for LVS	D	D	D
-	53	mopores	Medium ohmic poly resistor P+	D	-	-
115	54	nnldd	Mask, no nldd implant	D+G#+	D+G#+	D+G#+
105	55	pldd	Mask, pldd implant	D+G##+	D+G##+	D+G##+
-	56	hipores	High ohmic poly resistor body	D	-	-
-	57	lopores	Low ohmic poly resistor body	D	-	-
-	58	nobln	Eliminates BLN generation	D	-	-
-	59	NVM	Old NVM concept	-	-	-
-	60	L60	Metal disable	-	D	D
-	61	Nogen	No generation/ drawn is taken over	D	D	D
-	62	MTC 22000	Marker for C07M layout in i2t	D	-	-
-	63	nores	Helping layer for LVS	D	D	D
-	82	nplusprot	N+ protect= only NLDD implant	D	D	D
-	83	nlddprot	Nldd protect = only N+ implant	D	D	D
-	101	m1bndry	Help layer for place and route	-	D	D
-	102	m2bndry	Help layer for place and route	-	D	D
-	103	viabndry	Help layer for place and route	-	D	D
-	104	v2bndry	Help layer for place and route	-	D	D

D = data is drawn
G = data is generated
- = forbidden to draw any data
Mask 40 (vtpoly0) is optional and only available for redesigns of existing product WFCA
+ The layers NLDD and PLDD under NOGEN (IGS=GDS #61) have to be drawn as the exact copy of respectively NOT_N^+_implant and P^+_implant.
# This layer can only be drawn under NOGEN.
This layer can only be drawn under NOGEN and under MTC22K.

4.0 LAYOUT RULES

Introduction

4.0.1 All dimensions are as drawn on the Interactive Graphical System (IGS).

4.0.2 All dimensions are given in microns (µm), unless specified otherwise.

4.0.3 for 'fixed rules'); wherever possible, if chip size is not significantly increased and/or circuit electrical performance is altered, the minimum dimensions should not be used.

4.0.4 All drawings are for illustrative purposes only. They are not drawn to scale.

4.0.5 The minimum layout grid size is 0.1 µm with the exception of poly and Metal2. For Poly and Metal2 a layout grid size of 0.05 µm is used in order to insure that the center of a minimum size line is on grid. The edges of all polygons must be on grid.

4.0.6 This document has to be read in conjunction with AMI Semiconductor Belgium specification DS13600 "Assembly Layout Rules", which contains additional rules which must be regarded as part of the total layout rule set. In case of discrepancy between the documents, the highest number must always be used.

4.0.7 This document has to be read in conjunction with AMI Semiconductor Belgium specification DS13291 which contains additional rules describing the impact of layout dimensions on electrical behaviour. This is especially important with respect to obtaining good analog performance (matching etc.) in the C07E-A technology.

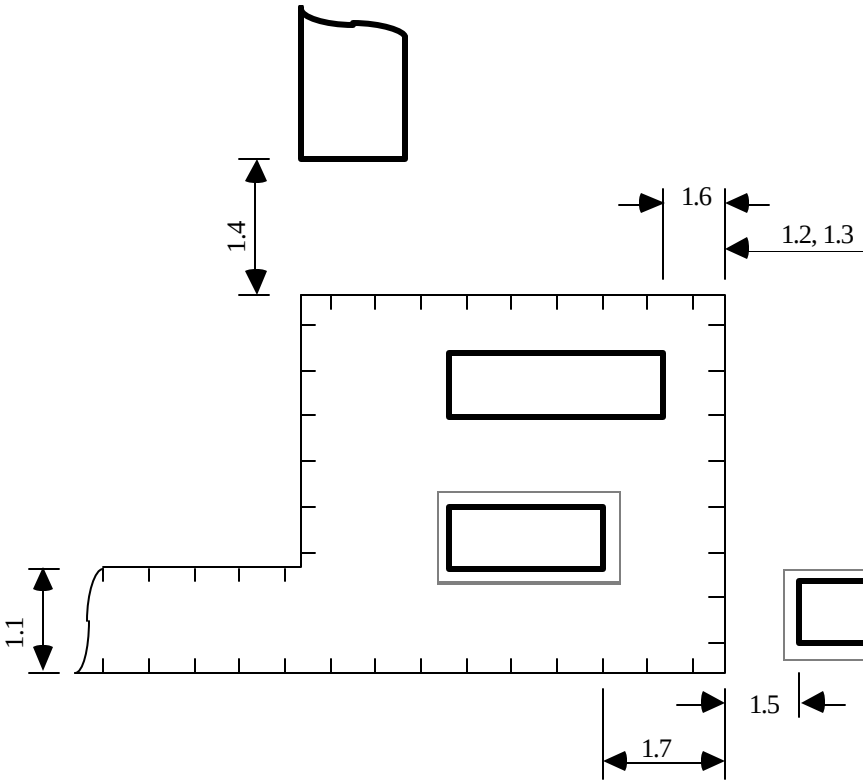
4.0.8 For the performance of the devices and cells used in NVM-EEPROM, see DES-0021 "Appendix to CMOS 0.7µm and I2T100 Layout Rules manuals for NVM module " (notice that PolyZap diodes cannot be manufactured in combination with EEPROM).

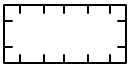
4.0.9 Refer to § 6.0 for more general layout requirements.

4.1 N-WELL (IGS LAYER 1)

Defines all n-well areas.

4.1.1	Minimum n-well width	2.00	
4.1.2	Minimum n-well spacing at different potential	5.00	
4.1.3	Minimum n-well spacing at same potential (merge if less)	3.00	
4.1.4	Minimum n-well spacing to N+ active area	2.20	
4.1.5	Minimum n-well spacing to P+ active area (strap)	1.00	
4.1.6	Minimum n-well enclosure of N+ active area (strap)	0.60	
4.1.7	Minimum n-well enclosure of P+ active area	2.00	





N-well

Active Area

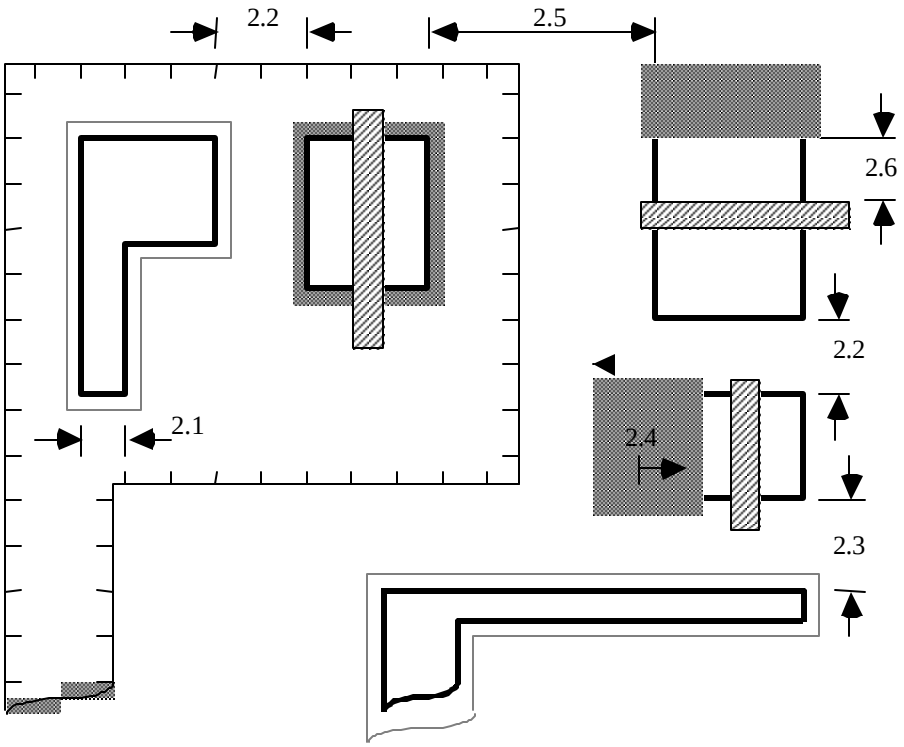
P+_Diffusion

4.2 ACTIVE AREA (IGS LAYER 2)

Defines MOS source and drain areas and diffused areas for interconnect or substrate - and n-well contacts.

4.2.1 Minimum active area width	1.00	
4.2.2 Minimum spacing between same type of active areas at different potential in the same substrate	1.40	
4.2.3 Minimum spacing between opposite type of active areas at different potential in the same substrate	1.60	
4.2.4 Minimum spacing between same or opposite type of active areas at the same potential in the same substrate (merge if less)	1.40	
4.2.5 Minimum spacing between opposite type of active areas in different substrate - transistors/diffusions (4.1.4 + 4.1.7) - straps (4.1.5 + 4.1.6)	 4.20 1.60	
4.2.6 Minimum source & drain length	1.40	

ACTIVE AREA (IGS LAYER 2)



N-well

Active Area

Polysilicon

P+_Diffusion

4.3 Not_Field_Implant (IGS Layer 3)

Defines areas which will not be implanted by the Boron Field implant. It is used to enhance the NMOS field doping and is automatically generated from the N-WELL data. This layer must not be drawn.

Refer to AMI Semiconductor Belgium specification DS13299 "Mask Generation CMOS 0.7 µm Enhanced" for mask generation details.

4.4 Low_VTP_Implant (IGS Layer 22)

Optional for C07E-A.

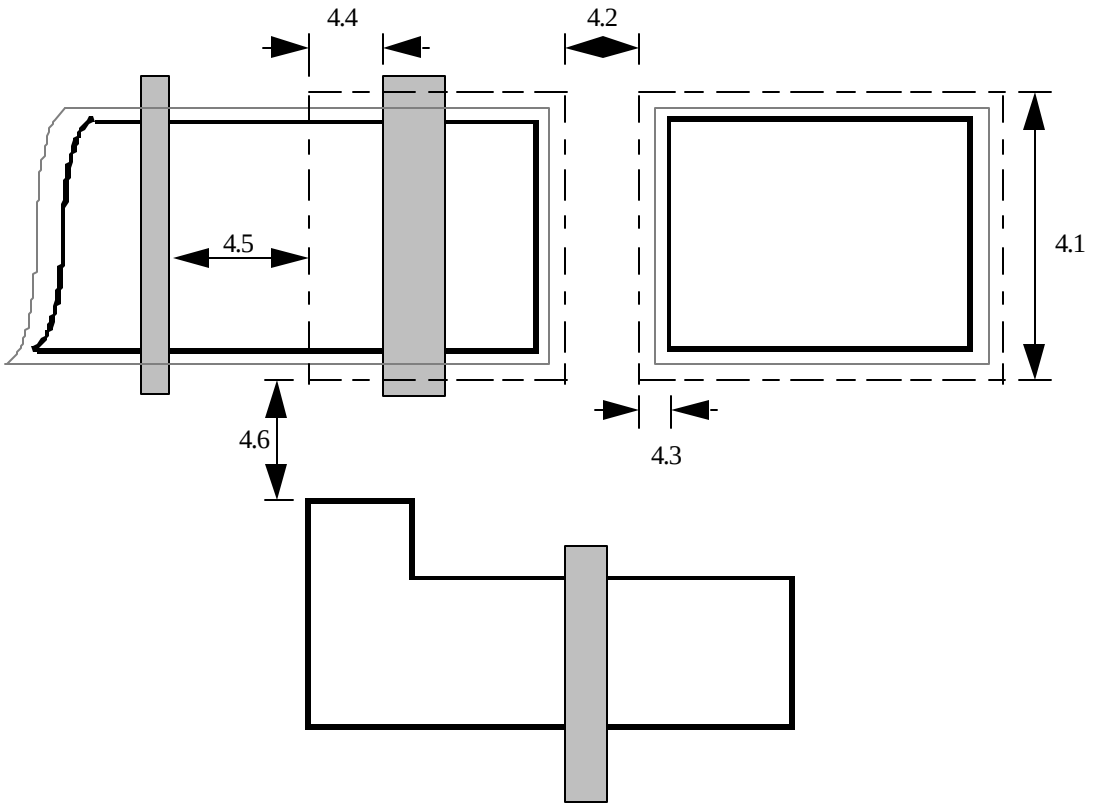
Defines the boron implanted PMOS active areas. It is used to provide the low threshold voltage for the analog PMOS transistors in C07E-A.

The LOW_VTP_IMPLANT mask is defined as an aperture around low threshold voltage PMOS transistors.

Refer to AMI Semiconductor Belgium specification DS13291 "Electrical Parameters CMOS 0.7 µm - C07M" for minimum dimensions and electrical characteristics of low threshold PMOS transistors.

4.4.1 Minimum LOW_VTP_IMPLANT width	1.0	
4.4.2 Minimum LOW_VTP_IMPLANT spacing	1.0	
4.4.3 Minimum LOW_VTP_IMPLANT enclosure of active area on field oxide	0.5	
4.4.4 Minimum LOW_VTP_IMPLANT enclosure of polysilicon on active area	1.0	
4.4.5 Minimum LOW_VTP_IMPLANT spacing to unrelated polysilicon on active area	1.0	
4.4.6 Minimum LOW_VTP_IMPLANT spacing to unrelated active area	0.7	

LOW_VTP_IMPLANT (IGS LAYER 22)




Active Area


LOW_VTP


Polysilicon


P+_Diffusion

4.5 CAPA_Implant (IGS Layer 20)

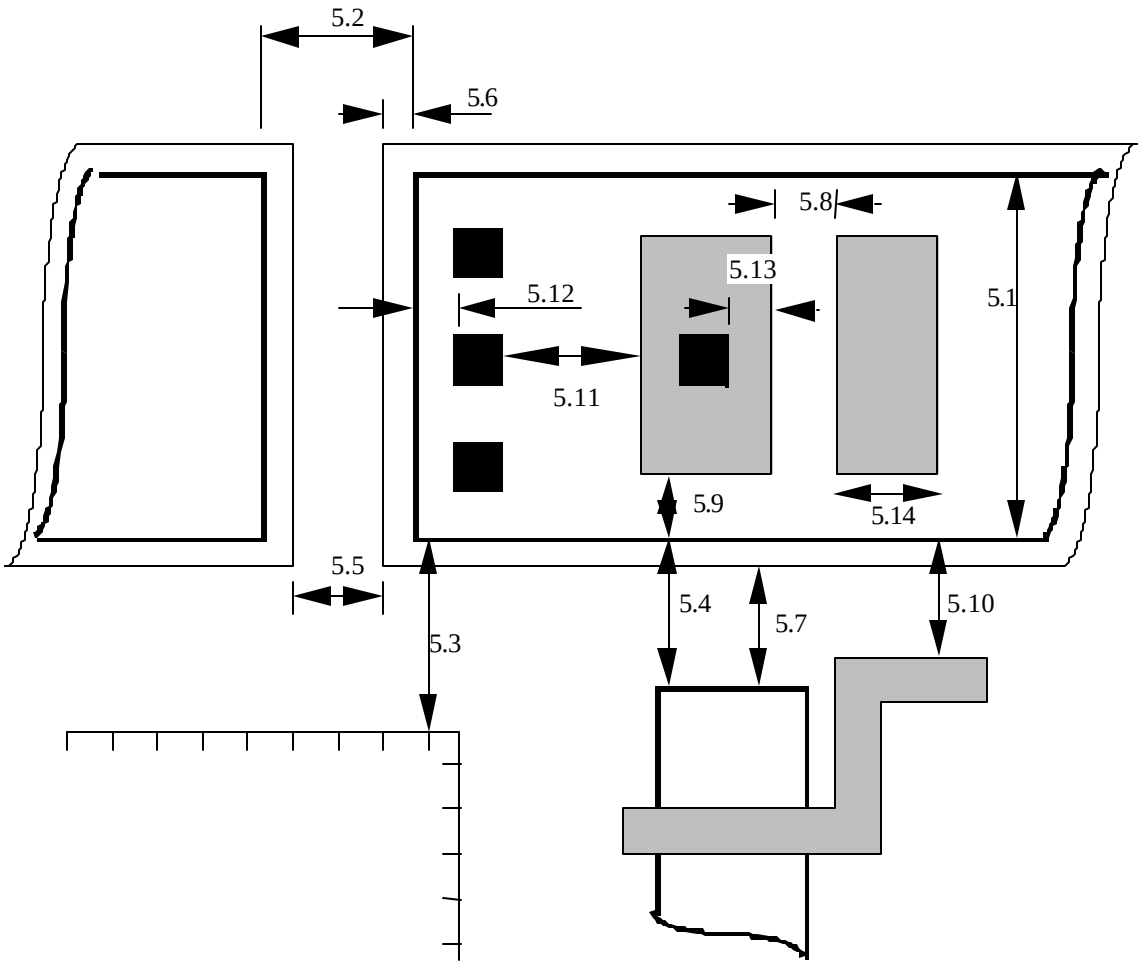
Optional for C07E-A.

Defines the photoresist opening through which N-type dopants are implanted to form the bottom plate of the capacitors.
The topplate of the capacitors is defined by the polysilicon mask over active area with CAPA_IMPLANT mask. The capacitors are masked both at N+ & P+ implants.

Refer to AMI Semiconductor Belgium specification DS13291 "Electrical Parameters CMOS 0.7 µm - C07M" for electrical characteristics of implanted capacitors. This specification also contains additional layout rules to be fulfilled to obtain good analog performance.

4.5.1	Minimum width of capacitor active area	1.0	
4.5.2	Minimum capacitor active area spacing	4.0	
4.5.3	Minimum capacitor active area spacing to n-well	5.0	
4.5.4	Minimum capacitor active area spacing to unrelated active areas	3.0	
4.5.5	Minimum CAPA_IMPLANT spacing	2.0	
4.5.6	Fixed CAPA_IMPLANT enclosure of capacitor active area	1.0	
4.5.7	Minimum CAPA_IMPLANT spacing to unrelated active areas	2.0	
4.5.8	Minimum polysilicon spacing for capacitors	1.5	
4.5.9	Minimum capacitor active area enclosure of polysilicon for capacitors	1.5	
4.5.10	Minimum capacitor active area spacing to unrelated polysilicon	1.5	
4.5.11	Minimum capacitor polysilicon spacing to capacitor active area contact	2.0	
4.5.12	Minimum capacitor active area enclosure of contact	0.6	
4.5.13	Minimum capacitor polysilicon enclosure of contact	1.0	
4.5.14	Minimum capacitor polysilicon width	5	

CAPA_IMPLANT (IGS LAYER 20)



N-well

CAPA_IMPLANT

Active Area

Polysilicon

Contact

P+_Diffusion

Metal 2

4.6 HIPO_Dopeprotect (IGS Layer 21) & DSP (IGS Layer 9)

Optional for C07E-A.

The HIPO_DOPEPROTECT mask defines the poly-silicon regions which will be lowly doped in order to achieve high Ohmic poly-silicon sheet resistance. The HIPO_DOPEPROTECT mask protects the HIPO resistors from N+ poly-doping.

A HIPO resistor is determined by the intersection of polysilicon (IGS layer 13) and hipo_dopeprotect (IGS layer 21) and not covered by DSP.
The width is defined by the polysilicon width (IGS layer 13); the length is defined by the distance between DSP (IGS layer 9) (see L on drawing).
Low accuracy Hipo resistors are defined by a LOWACC layer (IGS layer 52).
A Low Accuracy Hipo resistor is a Hipo resistor for which the Hipo Sheet resistance specification can not be guaranteed.
A 'dummy HIPO resistor' is defined as a HIPO resistor that is not having contacts on both sides.
Dummy HIPO resistors and Low accuracy resistors have the same rules as normal HIPO resistors except when stated otherwise.

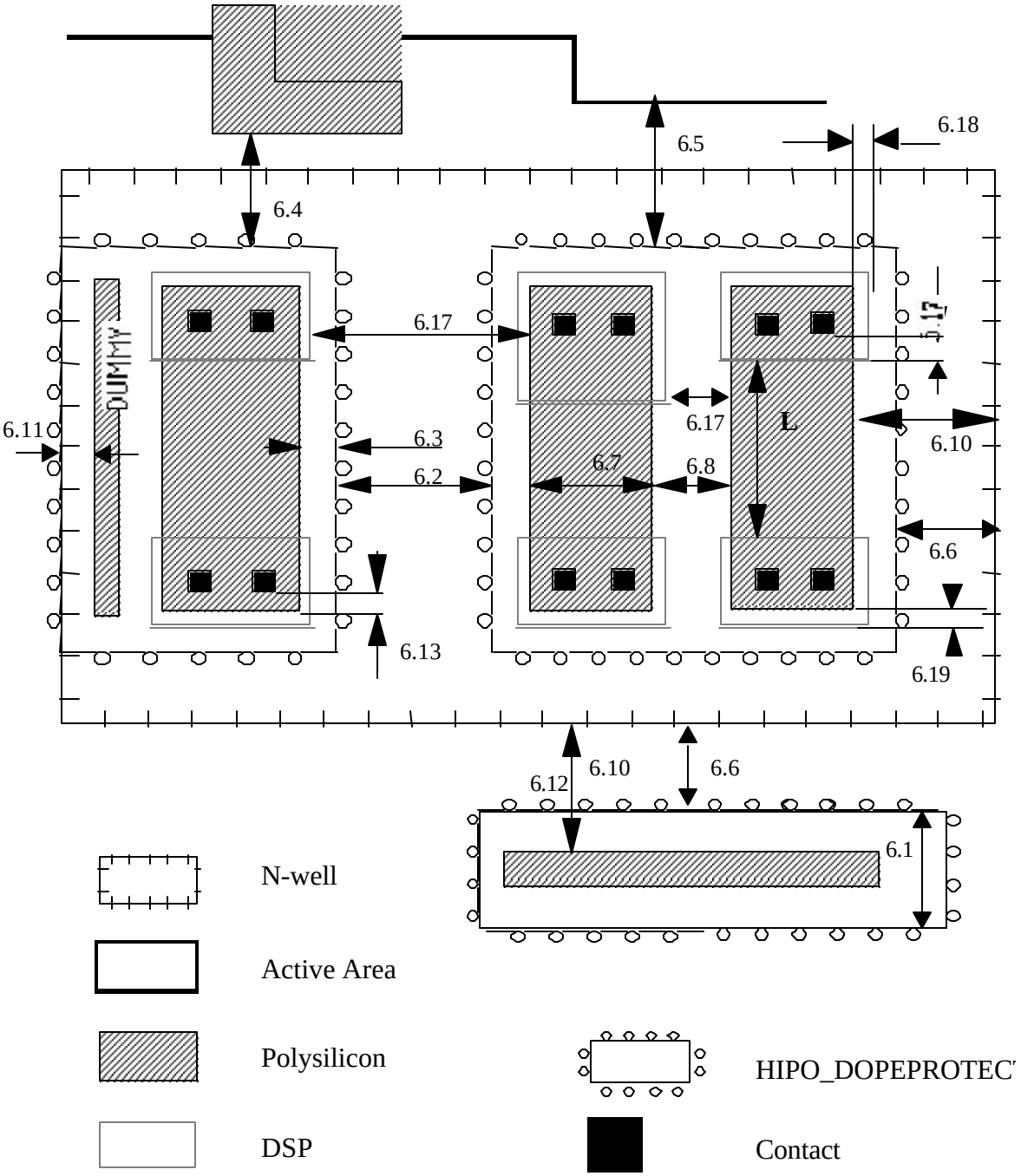
HIPO resistors are protected against N+ & P+ implants.

- Contacts to HIPO resistors must be surrounded by IGS layer 9 (DSP).
  When the overlap of DSP on contacts is larger than the minimum value, these extra overlap regions will cause an additional series resistance (see spec DS13291). The overlap is the same in all directions.
- HIPO resistors must be on field oxide.
- HIPO resistors are allowed on Nwell and on Pwell, but are not allowed to cross the Nwell/Pwell border. It is advised to put the resistors on Nwell when matching performance is critical. Matching is only guaranteed for HIPO on Nwell (see spec DS13291).
- Metal1 and Metal2 on top of HIPO resistors is forbidden
  (except for - the fixed enclosure of Metal1 around contact
  - Dummy & Low Accuracy hipo resistors).

Refer to AMI Semiconductor Belgium specification DS13291 "Electrical Parameters CMOS 0.7 µm - C07M" for electrical characteristics of HIPO resistors. This specification also contains additional layout rules to be fulfilled to obtain good analog performance.

4.6.1	Minimum HIPO_DOPEPROTECT width	2.0
4.6.2	Minimum HIPO_DOPEPROTECT spacing	2.0
4.6.3	Minimum HIPO_DOPEPROTECT enclosure of HIPO resistor	3.0
4.6.4	Minimum HIPO_DOPEPROTECT spacing to unrelated poly-silicon	2.0
4.6.5	Minimum HIPO_DOPEPROTECT spacing to active area	0.0
4.6.6	Minimum HIPO_DOPEPROTECT spacing to n-well (no crossing allowed)	0.0
4.6.7	Minimum HIPO resistor width	2.0
4.6.8	Minimum HIPO resistor spacing	2.0
4.6.9	Minimum n-well enclosure of HIPO resistor	5.0
4.6.10	Minimum HIPO resistor spacing to n-well	5.0
4.6.11	Minimum n-well enclosure of dummy & Low Accuracy HIPO resistor	1.0
4.6.12	Minimum dummy & Low Accuracy HIPO resistor spacing to n-well	1.0
4.6.13	Minimum HIPO resistor enclosure of contact	0.6
4.6.14	Minimum HIPO resistor space to Metal1, 2, 3 (except for metal 1 contacting HIPO, dummy's and Low accuracy Hipo resistors)	5.0
4.6.15	Maximum Metal1 enclosure of HIPO contact	0.9
DSP (IGS layer 9)		
4.6.16	Fixed DSP enclosure of contact in the direction to the HIPO resistor (min=max)	0.5
4.6.17	Minimum DSP spacing to unrelated HIPO resistor	1.5
4.6.18	Minimum DSP enclosure on poly on three sides	0.8

HIPO_DOPEPROTECT (IGS LAYER 21) AND DSP (IGS LAYER 9)

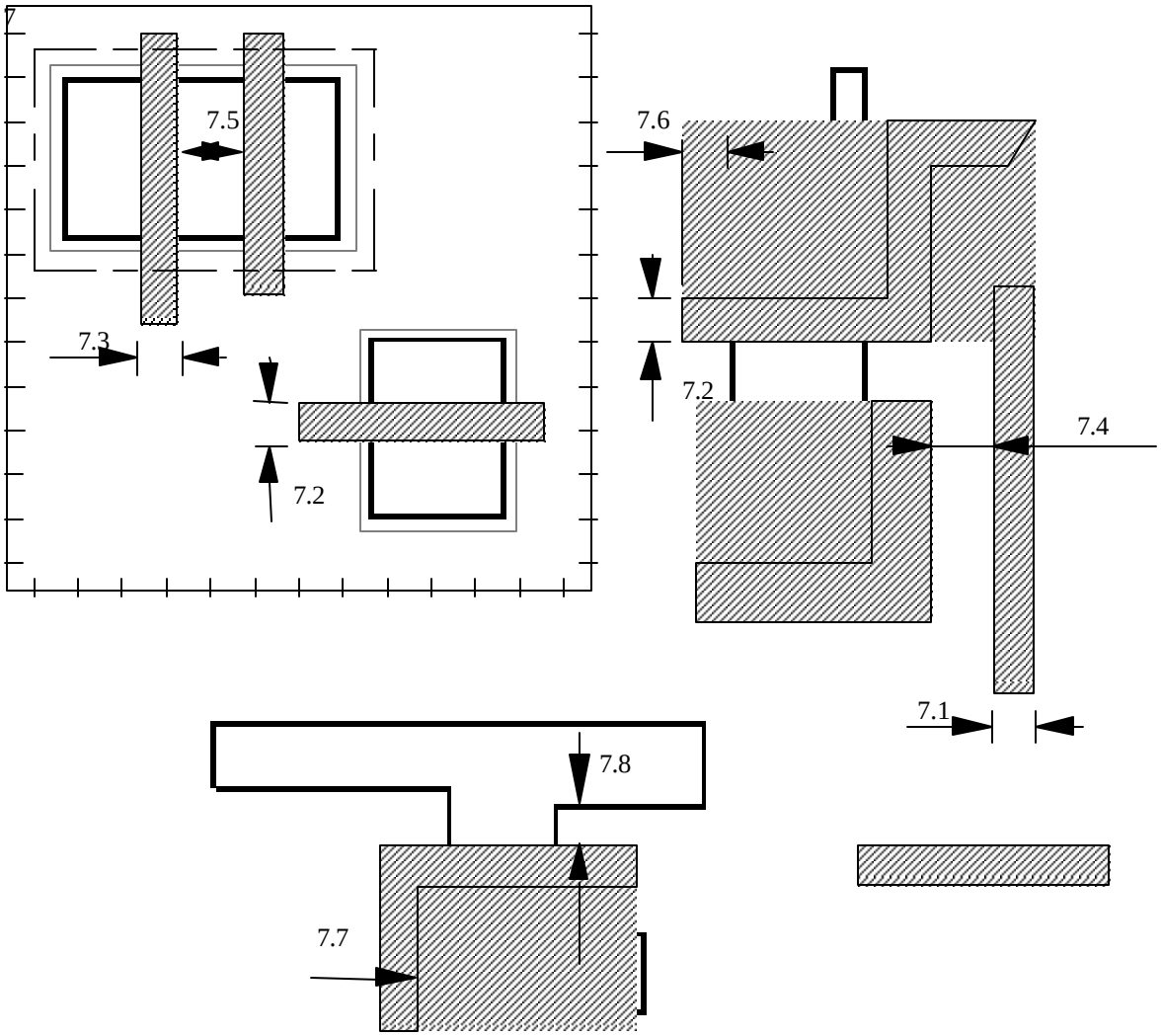


4.7 Polysilicon (IGS Layer 13)

Defines the gate areas, low ohmic poly-silicon interconnect and HIPO resistors (C07E-A only). The HIPO resistor rules are given in § 4.6. "HIPO_DOPEPROTECT".
The layout-grid used is 0.05µm.

4.7.1	Minimum polysilicon width for interconnect	0.7	
4.7.2	Minimum polysilicon width for transistors	0.7	
4.7.3	Minimum polysilicon width for low Vt PMOS transistors (C07M-A only)	1.2	
4.7.4	Minimum polysilicon spacing on field oxide	0.8	
4.7.5	Minimum polysilicon spacing on thin oxide	0.8	
4.7.6	Minimum polysilicon extension beyond gate, on field oxide (endcap)	0.7	
4.7.7	Minimum polysilicon spacing to unrelated active area (used as INTERCONNECT) Minimum polysilicon spacing to unrelated active area and contact to active spacing is >=0.6 µm	0.9 0.3	
4.7.8	Minimum polysilicon spacing to related active area (used as ENDCAP) Minimum polysilicon spacing to related active area and contact to active spacing is >=0.6 µm	0.9 0.3	

POLYSILICON (IGS LAYER 13)



N-well

LOW_VTP

Active Area

P+_Diffusion

Polysilicon

4.8 Not_N+_Implant (IGS Layer 16)

The Not_N+ IMPLANT mask defines the areas which will NOT receive the N+ source & drain implants.

This layer must not be drawn and is generated automatically from the other layers containing layout-data.

Refer to AMI Semiconductor Belgium specification DS13299 "Mask Generation CMOS 0.7 µm Enhanced" for mask generation details.

As this is a light field mask this mask in fact defines the regions which are not implanted.

4.9 NLDDPROT (IGS=GDS layer 83) and NPLUSPROT (IGS=GDS layer 82)

The NLDDPROT mask defines the areas which will NOT receive the NLDD implant; the NPLUSPROT mask defines the areas which will NOT receive the NPLUS implant.
These layers are only used for special layouts (ESD, EEPROM).

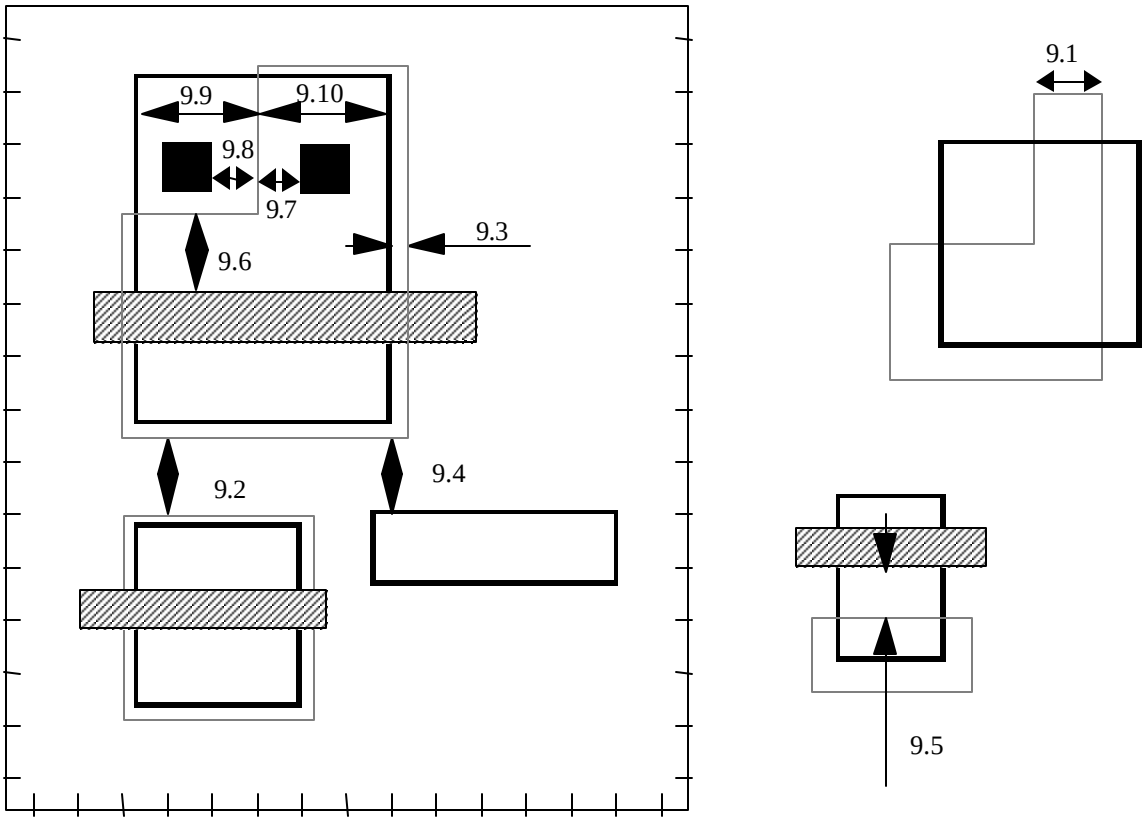
For the layout rules, see the Not_N+IMPLANT table (4.8).

4.10 P+_Implant (IGS Layer 17)

Defines the areas which will receive the P+ source & drain implant, except for the HIPO resistor contact areas which are defined on layer DSP.

4.9.1	Minimum P+_Implant width	0.8	
4.9.2	Minimum P+_Implant spacing (merge if less)	0.8	
4.9.3	Minimum P+_Implant enclosure of P+ active area	0.5	
4.9.4	Minimum P+_Implant spacing to N+ active area	0.5	
4.9.5	Minimum P+_Implant spacing to NMOS poly gate when the n-channel source/drain length is defined by the P+_Implant mask (N+/P+ split region)	1.4	
4.9.6	Minimum P+_Implant enclosure of PMOS poly gate when the p-channel source/drain length is defined by the P+_Implant mask (N+/P+ split region)	1.4	
4.9.7	Minimum P+ enclosure of P+ contact on active	0.5	
4.9.8	Minimum P+ spacing to N+ contact on active	0.5	
4.9.9	Minimum active area extension beyond P+_Implant at N+/P+ split region	1.0	
4.9.10	Minimum P+ extension in AA at N+/P+ split region	1.0	

P+_IMPLANT (IGS LAYER 17)



Contact

N-well

Polysilicon

Active Area

P+_Diffusion

4.11 PLDD (IGS=GDS layer 55).

The PLDD mask defines the areas which will receive the PLDD implant.
This layer is only used for special layouts.

For the layout rules, see the P+_IMPLANT table (4.10).

4.12 Contacts (IGS Layer 19)

Defines the areas where contact is made from metal 1 to polysilicon and N+ & P+ active area.

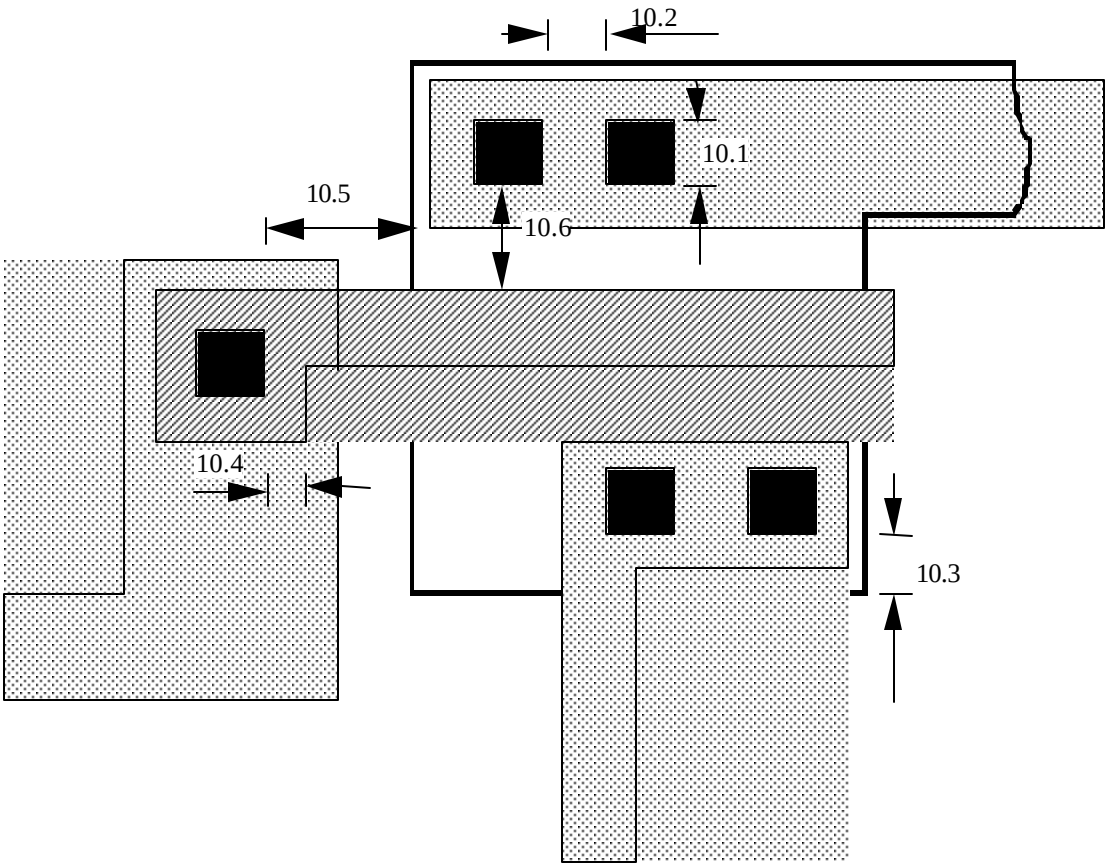
Contacts on polysilicon over active area are not allowed except for capacitors (C07M-A only).

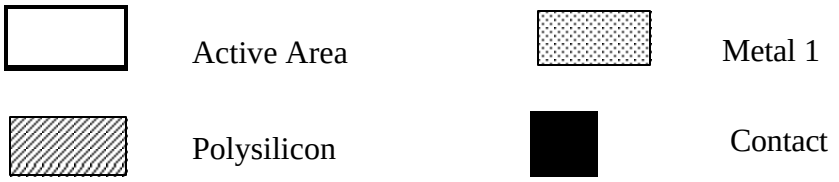
No butted contacts (poly to active, or N+active to P+active) allowed.

Refer to section 6.0 of this document for electromigration rules.

4.10.1	Fixed contact window dimensions (W & L) For OLD circuitry (e.g I/O cells) layouted accordingly to the spec DS13290, 1 µm contacts are allowed.	0.80	
4.10.2	Minimum contact window spacing	0.90	
4.10.3	Minimum active area enclosure of contact window	0.40	
4.10.4	Minimum polysilicon enclosure of contact window	0.50	
4.10.5	Minimum polysilicon contact window spacing to active area	0.60	
4.10.6	Minimum diffusion contact window spacing to gate polysilicon	0.70	

MASK 130: CONTACTS (IGS LAYER 19)

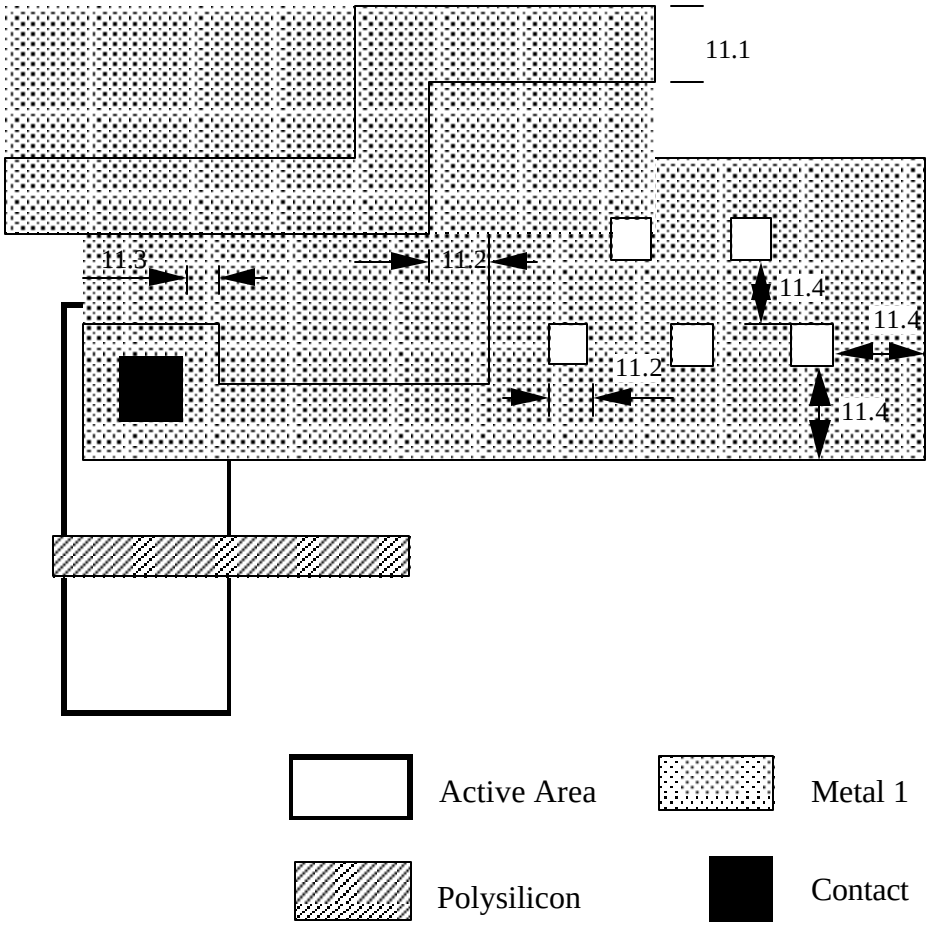




4.13 Metal 1(IGS Layer 23)

Defines the interconnect to all contacts and vias. Every contact must be covered by metal 1; each via must have underlying metal 1.
See section 6.0 of this document for electro-migration rules.

4.11.1	Minimum metal 1 width	0.80	
4.11.2	Minimum metal 1 spacing Note: recommendations for yield improvement only to be used when it not inflicts the cell density. 1 - for wide tracks (>10µm) use larger spacing (>2.0µm) 2 - For parallel tracks < 2 µm (=metal heads for contacts and Via's) a spacing of 0.9 µm can be used.	1.00	
4.11.3	Minimum metal 1 enclosure of contact window	0.50	
4.11.4	Maximum metal 1 width simultaneously in both directions Note: if the linewidth as determined by the electromigration rule (refer to section 5.0 of this document) is larger than 25 µm, introduce holes in the layout of the metal line. The holes should be staggered as shown in the figure. The holes may have minimum layout rule dimensions.	25.00	
4.11.5	Minimum metal1 width with an open space of 10 µm at one (or two) sides	2.50	



4.14 VIA 1 (IGS Layer 25)

Defines all contacts to be made from metal 1 to metal 2 only.

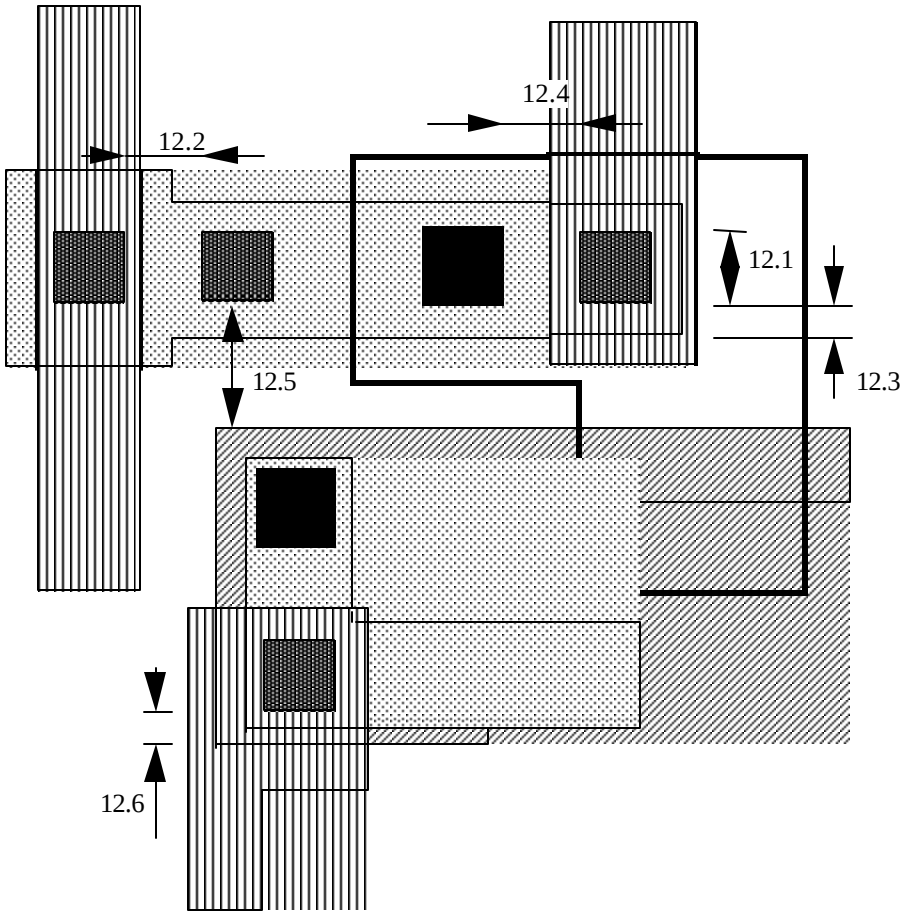
Stacked contacts (vias over contacts) are not allowed.

There will be one size via only, except for bonding pads and test pads.

Refer to section 6.0 of this document for electro-migration rules.

4.12.1	Fixed via window dimensions (W & L)… For OLD (e.g I/O) circuitry layouted accordingly DS13290 we allow 1 µm Via's …	0.80 1 µm	
4.12.2	Minimum via window spacing	1.00	
4.12.3	Minimum metal 1 enclosure of via window	0.40	
4.12.4	Minimum via window spacing to contact window	0.80	
4.12.5	Minimum via window spacing to polysilicon	No rule	
4.12.6	Minimum polysilicon enclosure of via window	No rule	

VIAS (IGS LAYER 25)



Active Area

Metal 1

Polysilicon

Via

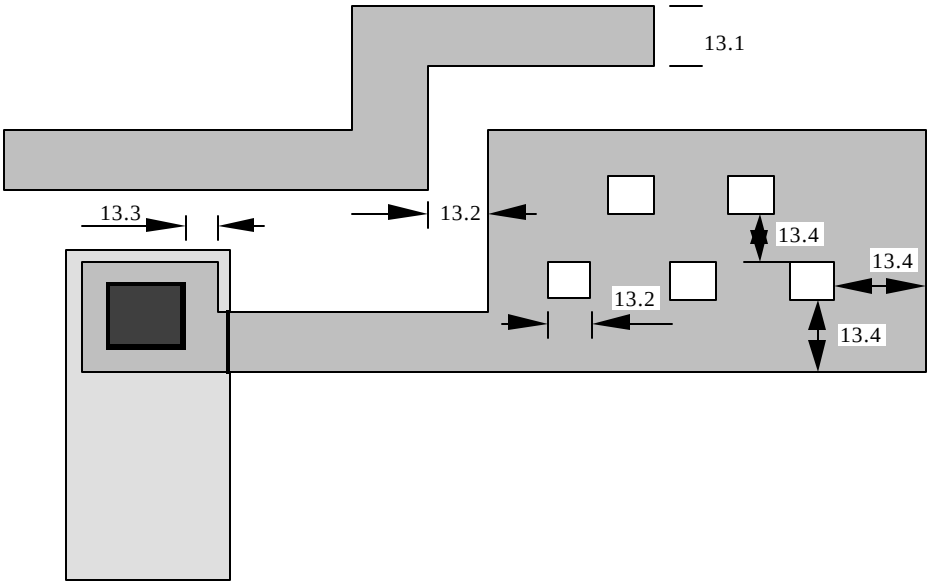
Contact

Metal 2

4.15 Metal 2 (IGS Layer 27)

Defines the interconnect to all vias and bonding pads. Each via must be covered by metal 2.
The layoutgrid used is 0.05 µm.
Metal 2 structures on top of implanted capacitors are not allowed.
See section 6.0 of this document for electromigration rules.

4.13.1	Minimum metal 2 width	1.00	
4.13.2	Minimum metal 2 spacing	1.20	
4.13.3	Minimum metal 2 enclosure of via window	0.50	
4.13.4	Maximum metal 2 width simultaneously in both directions Note: if the linewidth as determined by the electromigration rule (refer to section 5.0 of this document) is larger than 25 µm, introduce holes in the layout of the metal line. The holes should be staggered as shown in the figure. The holes may have minimum layout rule dimensions.	25.00	
4.13.5	Minimum metal2 width with an open space of 10 µm at one (or two) sides	2.50	



Metal 1

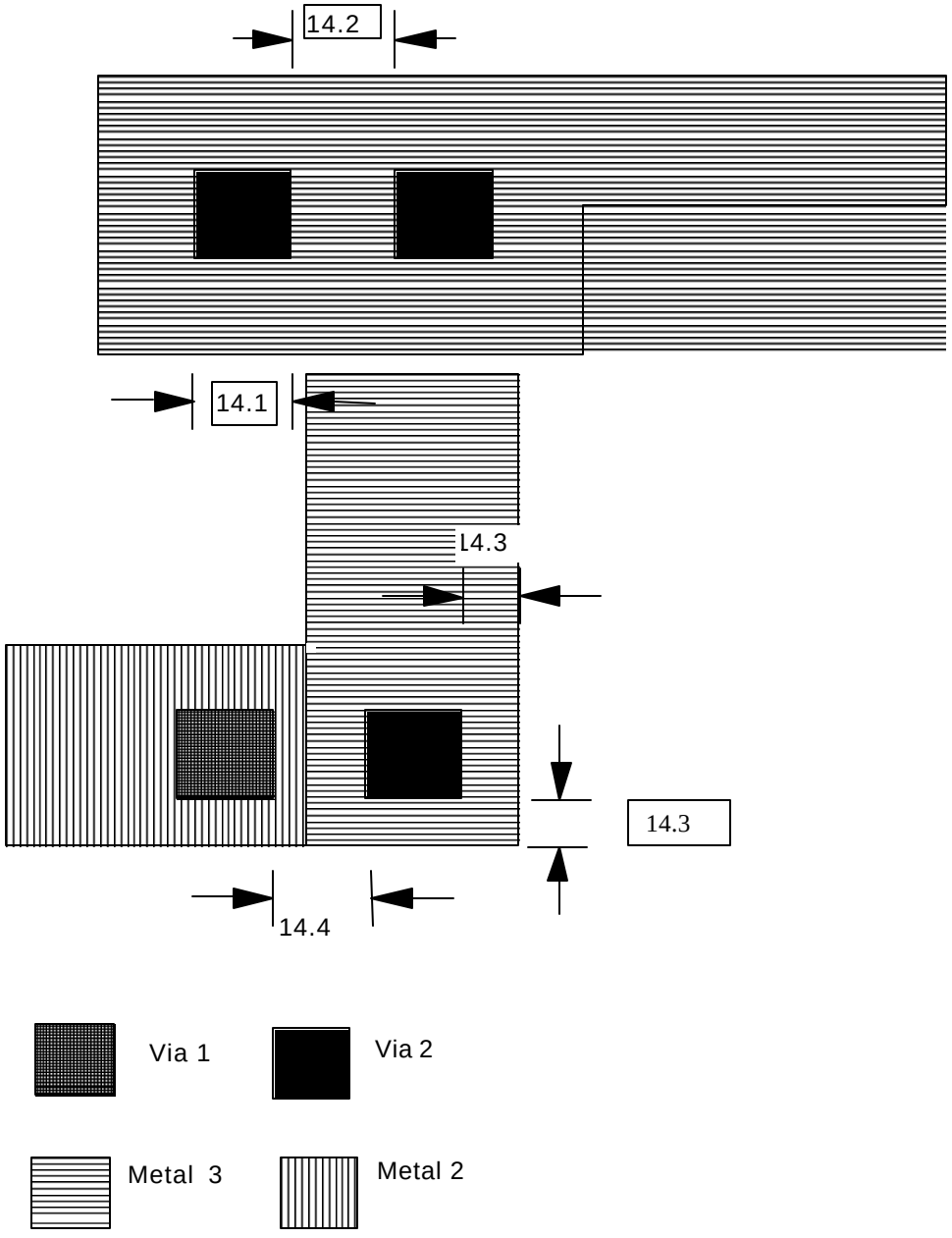
Metal 2

Via

4.16 VIA 2 (IGS Layer 32)

Defines all contacts to be made from metal 2 to metal 3 only. Stacked vias (via 2 on via 1) are not allowed. There will be one size via only, except for bonding pads and test pads.
Refer to section 6.0 of this document for electro-migration rules.

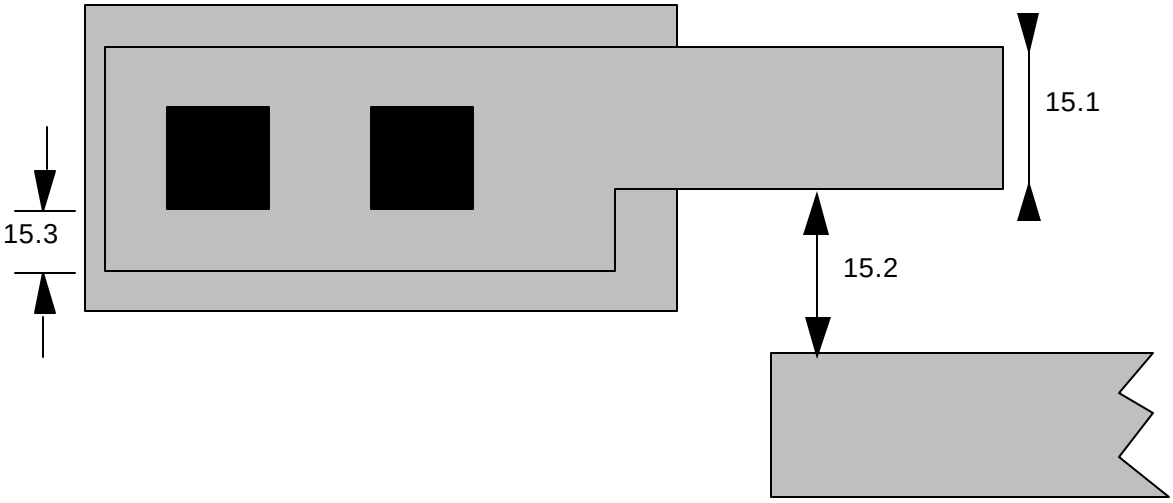
4.14.1	Minimum Via 2 width	1.0 µm
4.14.2	Minimum spacing between Via 2	1.4 µm
4.14.3	Minimum enclosure by Metal 2	0.7 µm
4.14.4	Minimum spacing to Via 1	0.8 µm

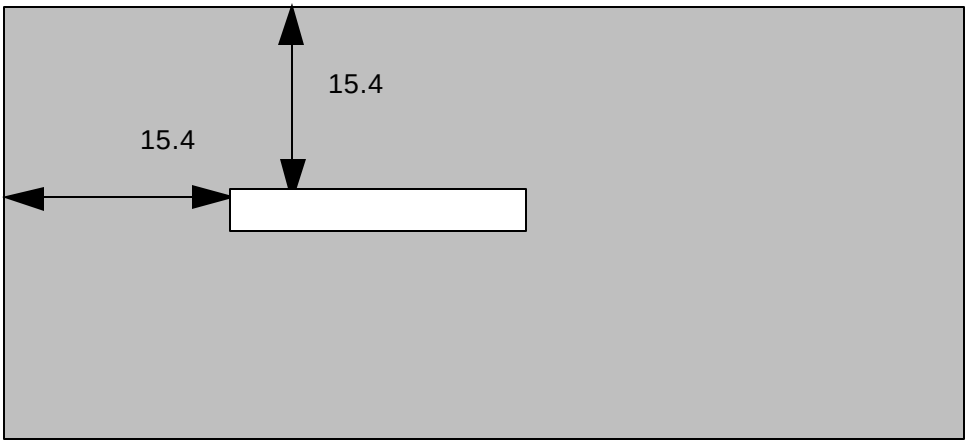


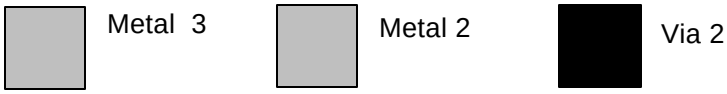
4.17 Metal 3 (IGS Layer 34)

Defines the interconnect to all via 2 and bonding pads. Each via must be covered by Metal 3. See section 6.0 of this document for electro-migration rules.

4.15.1	Minimum Metal 3 width	1.4 µm
4.15.2	Minimum space between Metal 3	1.6 µm
4.15.3	Minimum enclosure of Metal 3 on Via 2	0.7 µm
4.15.4	Maximum Metal 3 width simultaneously in two directions.	25 µm
4.15.5	Minimum Metal3 width with an open space of 10 µm at one (or two) sides	2.5 µm



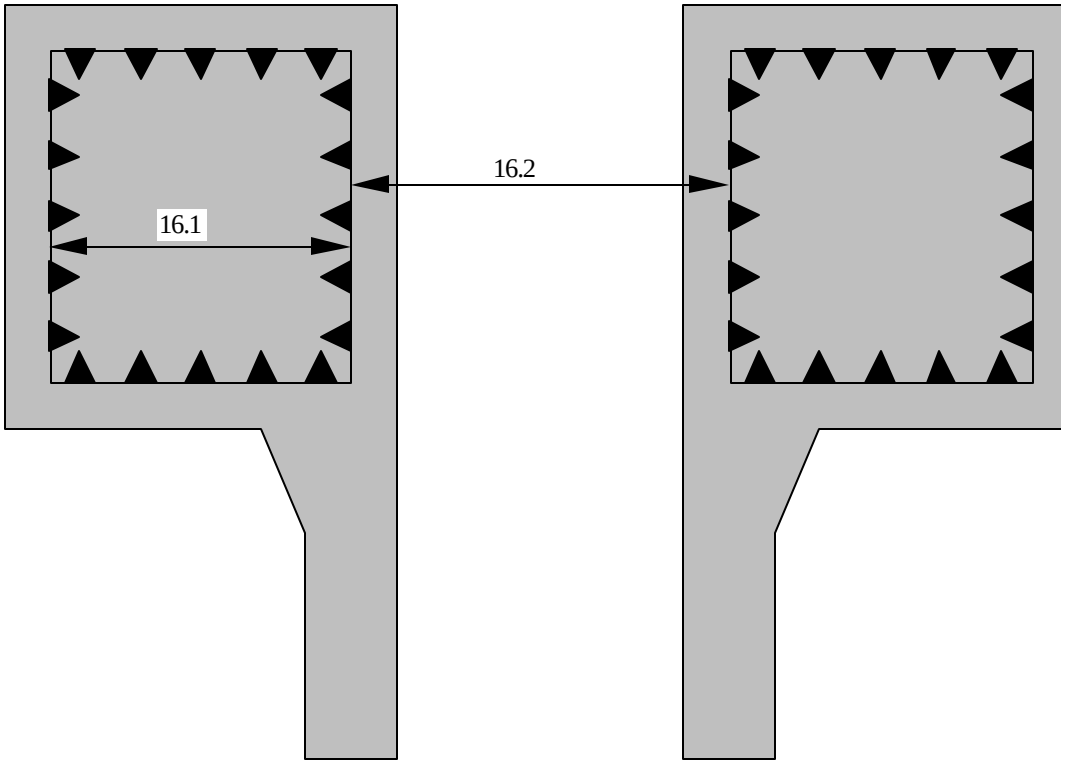




4.18 Overlay (IGS Layer 31)

Defines the area of the bondingpads and test pads where the passivation layer is not present.
No overlay openings are allowed except over bonding pads.
Refer to § 5.0 for a whole table of bonding pad rules and to AMI Semiconductor Belgium Spec DS13600 “Assembly/probe related layout rules” for the complete overview of the bonding requirements.

4.16.1 Minimum overlay window opening	See DS13600
4.16.2 Minimum overlay window spacing	See DS13600




Metal 2


Overlay

4.19 Polyimide

Defines the openings in the Polyimide top protective coating. This is an optinional layer.The use of polyimide as top protective coating has to be used when the chip area exceeds 120 mm2.
This layer must not be drawn and is automatically generated from the overlay data.

Refer to AMI Semiconductor Belgium Spec DS13299 "Maskgeneration CMOS 0.7 µm Enhanced": for generation details.

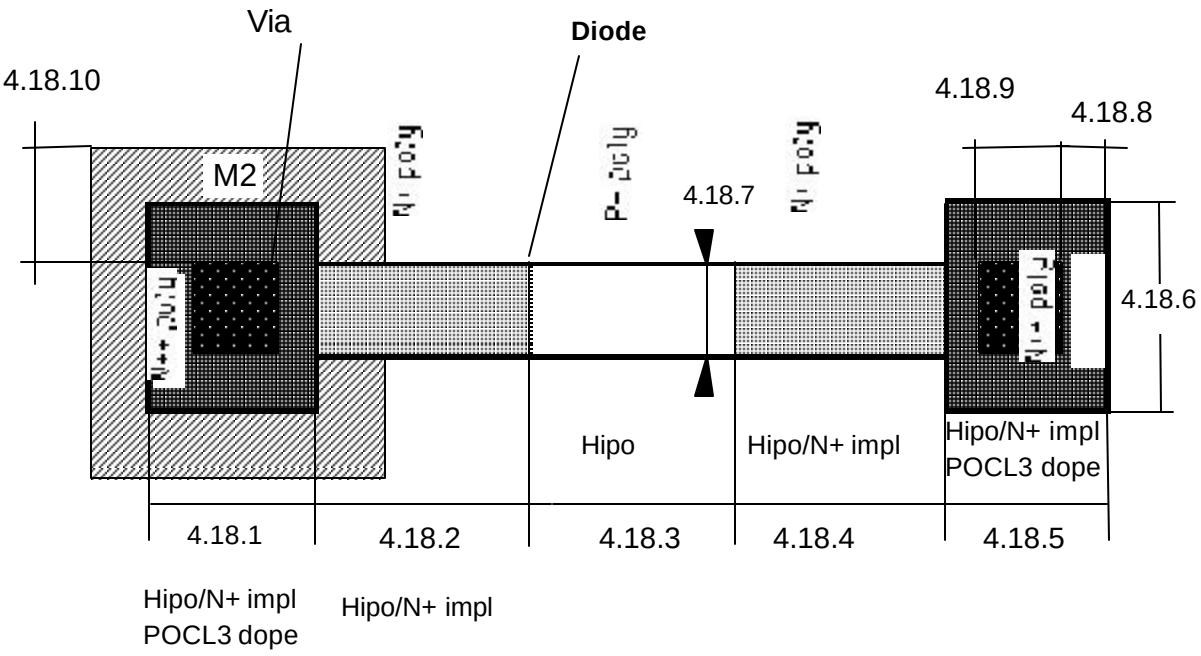
4.20 Poly Zap Structure

The poly zap structure is a device which make simple programming possible. In normal condition this device is a double diode back to back with a breakdown of minimum 5.5 V. After a programming pulse defined in the electrical rules the diode will be zapped and will react as a low ohmic resistor.

The diode has a fixed layout and must be copied from the standard cell library. Name: ‘M_ZAP’. Therefor the rules are not mixed within the normal layout rules but will be handled separately. To avoid false drc errors for rules only valid on the zap structure, this cells will be excluded from the DRC.

* The diode must be always on top of field oxide in Pwell.
* The poly is directly connected to the M2 with a standard via.

Layout of the structure:



Special rules for poly zap

For internal AMI Semiconductor Belgium usage only !!!

4.18.1	Size poly head including contact	2.2
4.18.5	Same as 4.18.1	2.2
4.18.6	Same as 4.18.1	2.2
4.18.2	Distance Poly head to Hipo (= Hipo_Dopeprotect including Not N+win)	3.0
4.18.4	Same as 4.16.2	3.0
4.18.3	Fixed width Not N+win	3.0
4.18.7	HIPO resistor width (Body of the structure)	1.0
4.18.8	Overlap of poly on poly via	0.6
4.18.9	Fixed Via size on top of poly	1.0
4.18.10	Fixed overlap M2 on top of poly via	2.0
4.18.11	Minimum distance polyzap structure to any other structure	5.0

4.21 NDmos as Switch for Polyzap
Ndmos as high voltage device.

The Ndmos used as a switch for the polyzap will not be guaranteed for long life times. It will only be used ones during programming. So, the channel length and the overlap of the gate on fieldox are chosen more critical than the ones of the high voltage device.
The life time of the Ndmos used as a high voltage device is specified in the electrical rules DS13191.
The transistor has a fixed layout in L direction and must use the standard cell library.
Name "M_NDMOSC07Z": as a switch for the polyzap
"M_NDMOSC07": as a HV device.
The direction can be chosen according to the necessary current flowing through the device. Therefore the rules are not mixed within the normal layoutrules but will be handled separately. To avoid false drc errors for rules only valid on the zap structure, these cells will be excluded from the DRC.

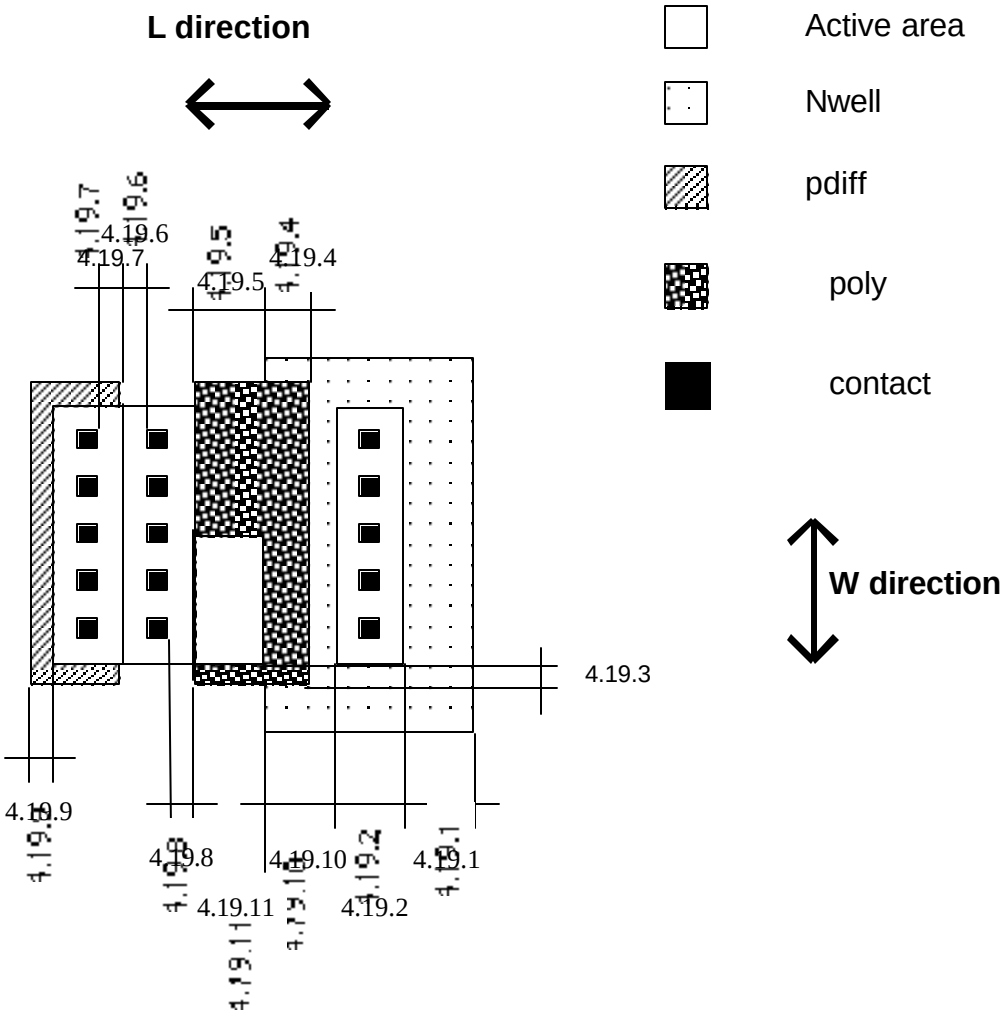
Special rules for NDmos.
For internal AMI Semiconductor Belgium use only!!!

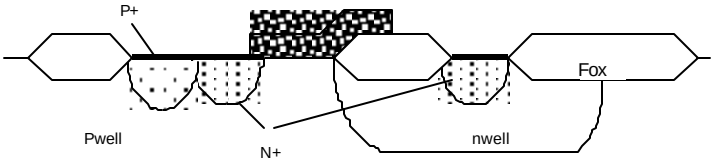
		Zap structure	HV device
4.19.1	Overlap Nwell on active area	3.0	
4.19.2	Active area width	2.2	
4.19.3	Overlap poly gate on Active area W side	0.9	
4.19.4	Overlap poly on Nwell drain =z	1.5	2
4.19.5	Enclosure Poly on Nwell source side = Channel length	2.5	4
4.19.6	Spacing contact to pdiff	0.6	
4.19.7	Overlap Pdiff on contact	0.6	
4.19.8	Spacing contact to poly gate	0.9	
4.19.9	Overlap Pdiff on Active area	0.8	
4.19.10	Overlap Nwell on Active are towards the channel	2.5	
4.19.11	Spacing Active area to Nwell	0.0	

* In addition one has to take care that none of the high voltage metal lines (> 8V) cross 2 different Nwell or N active area regions. In case of crossing an extra PAA isolation line with a width of 2.2 µm has to be inserted in between the Ntype area's.
The distance NAA to PAA is specified in rule 4.2.3.
The distance between Nwell to PAA 5 µm.

HVM1: layer 11
HVM2: layer 12

Layout of the structure





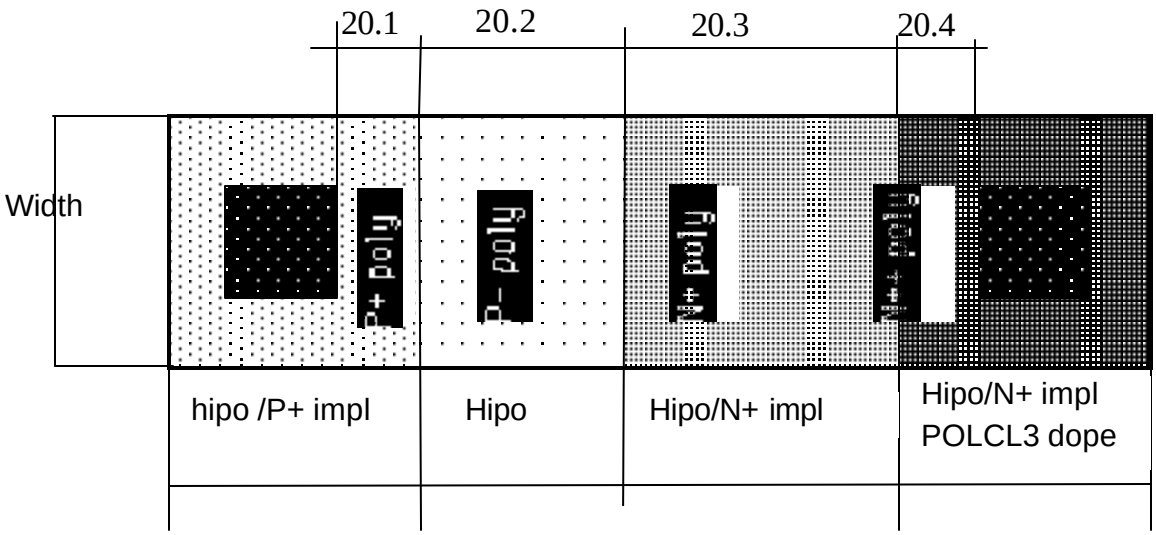
4.22 Poly Diode Structure

The poly diode is a full floating device towards the substrate up till 100 V.

The diode has a fixed layout in the length direction, the width can be chosen according max on resistance, or max current in forward mode. The cell must be copied from the standard cell library.
Name: 'PC_Polydiode'

* The diode must be always on top of field oxide.
* The poly is connected with M1.

Layout of the structure:



Special rules for poly diode

4.20.1	Fixed enclosure PDIFF on CONTACT, towards the inner side (= Hipo_Dopeprotect and Not N+win)	1.2
4.20.2	Fixed overlap NDIFF on PDIFF	1.4
4.20.3	Fixed enclosure HIPO_DOPEPROTECT on NDIFF	3.8
4.20.4	Spacing Poly contact to HIPO_DOPEPROTECT (= Hipo_Dopeprotect not Not N+win)	0.6

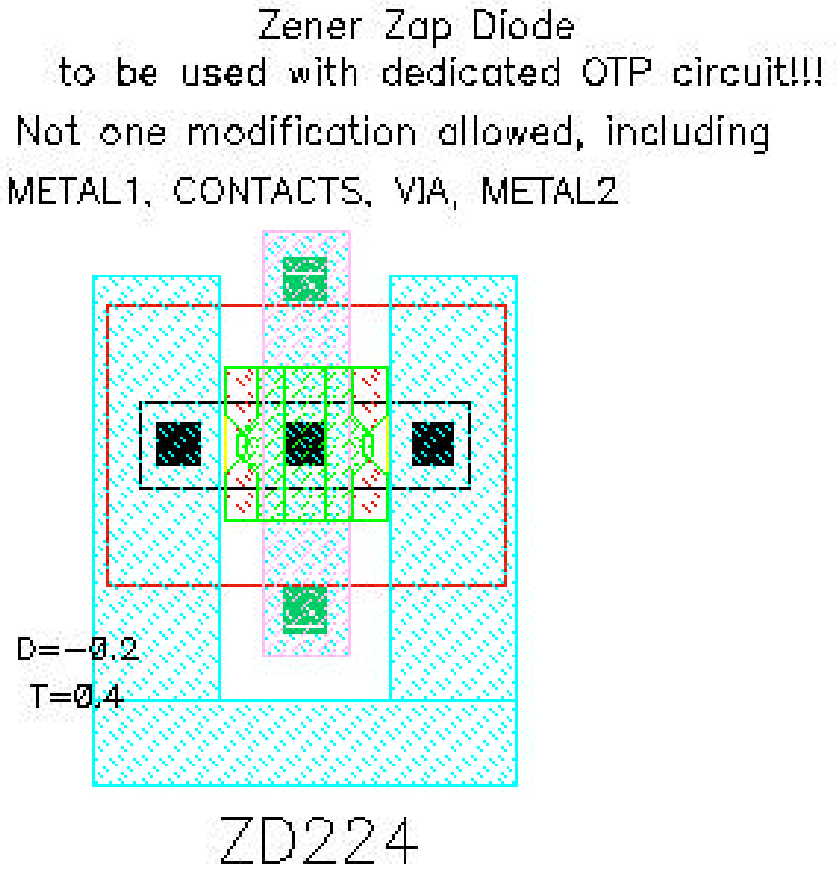
4.23 Zener Diode for OTP Applications

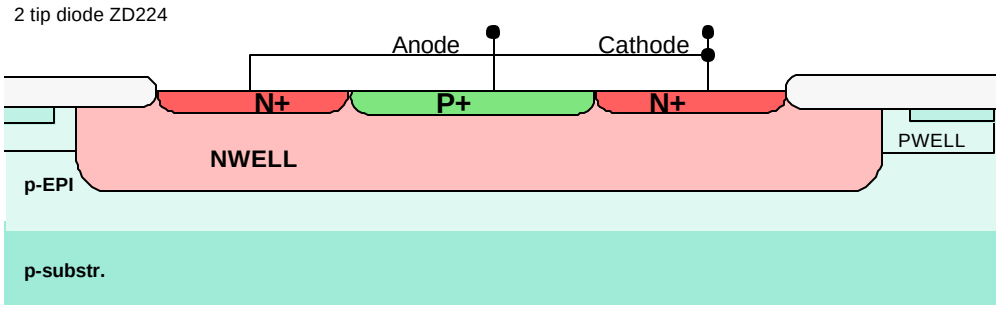
The N+P+ Zener diode zap structure is a device which makes simple and fast one time programming (OTP) possible. In normal condition this device is a reverse biased diode with a breakdown of around 3.85 V @ I=50 µA. After a programming pulse defined in the electrical rules (DS13291) the diode will be zapped and will react as a non-linear ohmic resistor in the appropriate read current range.

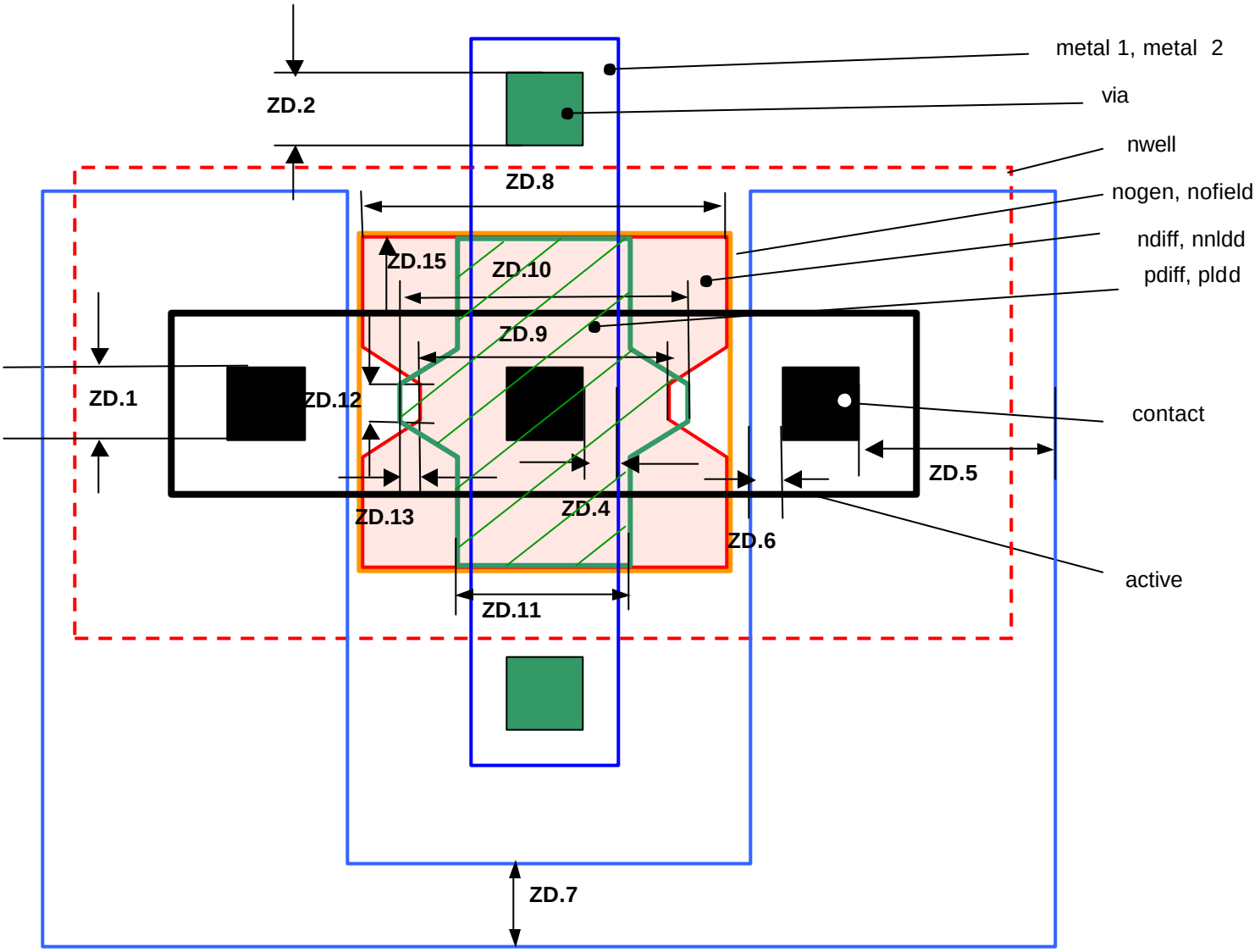
The diode has a fixed layout and must be copied from the standard cell library.

Cell Name: ZD224.

USE OF THIS DEVICE IS ONLY AUTHORISED AS PART OF A QUALIFIED ZAPPING CIRCUIT. FURTHER DETAILS OF SUCH CIRCUITS ARE AVAILABLE ON REQUEST.




2 tip diode ZD224
Anode
Cathode
N+
P+
N+
NWELL
PWELL
p-EPI
p-substr.


metal 1, metal 2
via
nwell
nogen, nofield
ndiff, nnldd
pdiff, pldd
contact
active
ZD.1
ZD.2
ZD.4
ZD.5
ZD.6
ZD.7
ZD.8
ZD.9
ZD.10
ZD.11
ZD.12
ZD.13
ZD.15

Layout rules. The following layout rules are for internal use only. No change is permitted.

ZD.1 Fixed contact size	1.0 x 1.0
ZD.2 Fixed via size	1.0 x 1.0
ZD.3 Fixed active area size	2.0 x 7.8
ZD.4 Fixed metal 1 enclosure of anode (p+) contact one side	0.5
ZD.5 Minimum metal 1 enclosure of cathode (n+) three sides*	1.5
ZD.6 Fixed metal 1 enclosure of cathode (n+) contact one side	0.5
ZD.7 Minimum metal 1 connection width of both n+ areas	2.0
ZD.8 Fixed long side NDIFF extension	3.8
ZD.9 Fixed small side NDIFF extension	2.8
ZD.10 Fixed long side PDIFF extension	3.2
ZD.11 Fixed small side PDIFF extension	2.2
ZD.12 Fixed tip width	0.4
ZD.13 Fixed overlap of NDIFF and PDIFF	0.2
ZD.14 Fixed NWELL size	9.4 x 6.6
ZD.15 Fixed vertical NOGEN enclosure of active area	0.8

* standard cell uses larger value in one direction although 1.5µm is sufficient

5.0 BONDING PADS AND SCRIBE LANE

5.1 BONDING PADS

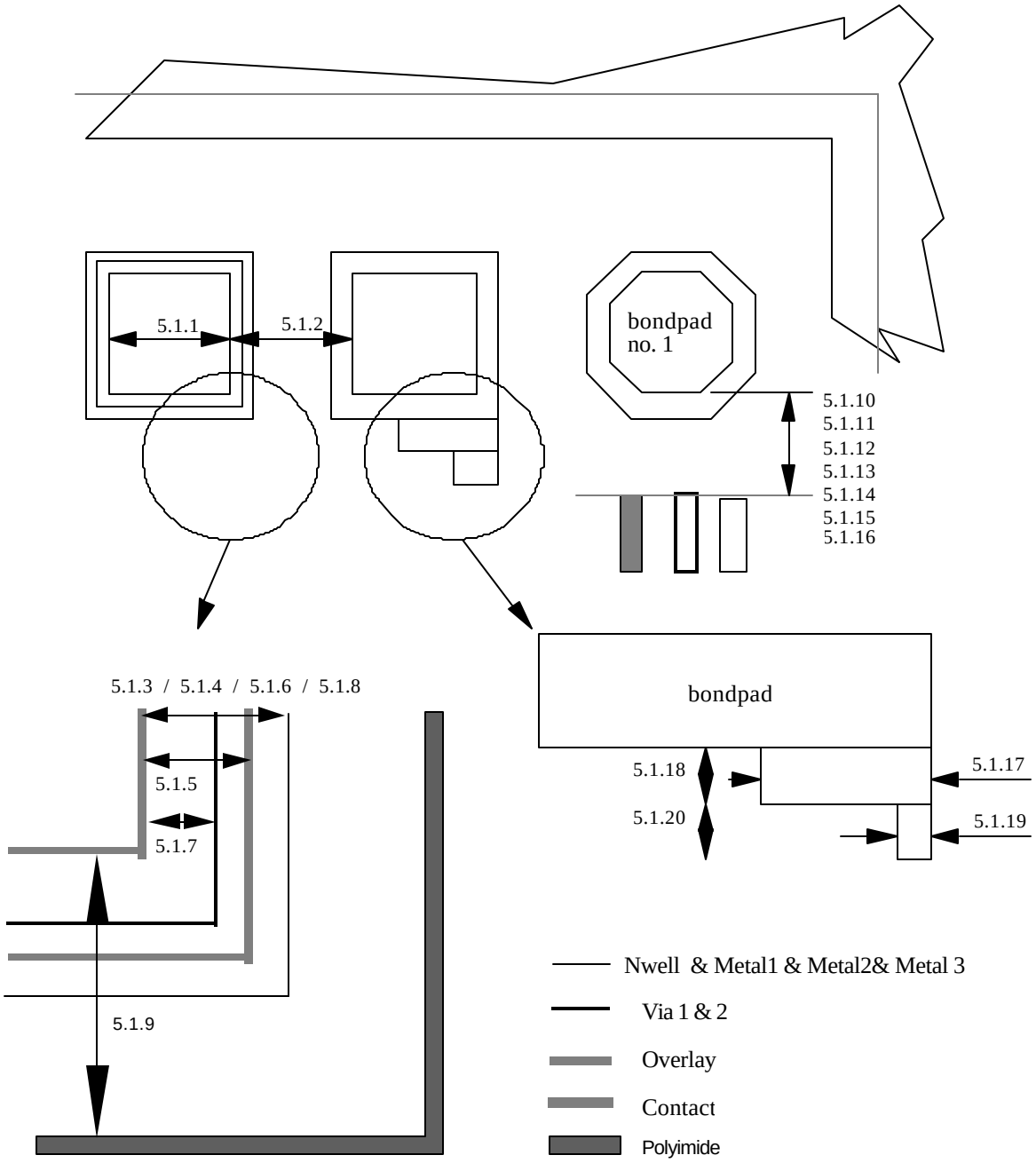
A bonding pad (or a test pad) is defined as the area of the overlay opening over the Top Metal layer (either Metal 2 or Metal 3) areas of the pad.
A bonding pad (or testpad) consists of an isolated metal 1 pad, a via 1 & 2 window, a metal 2 & 3 pad and an overlay opening, sometimes also a NWELL underneath. Active area, Poly and Contact are not allowed under bonding pads.

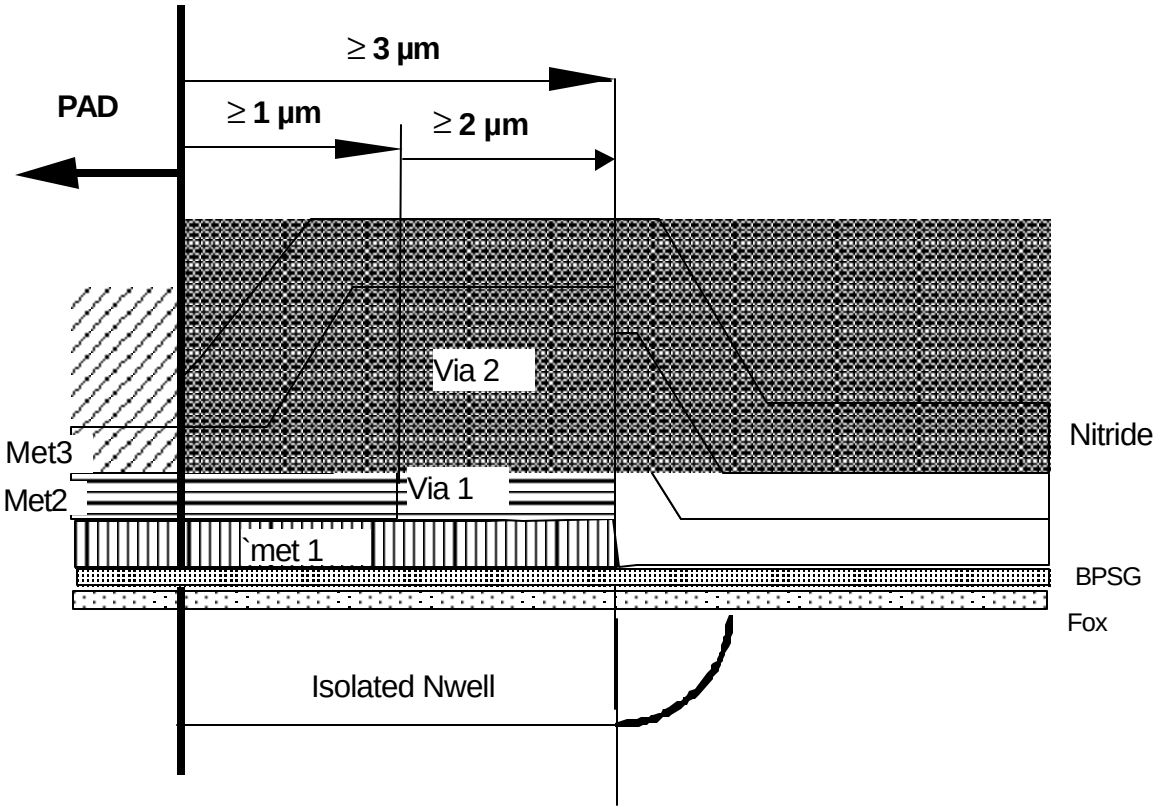
The minimum pad opening and the minimum pad spacing are defined according to the rules set by the Assembly and Probing groups : refer to AMI Semiconductor Belgium Spec DS13600 “Assembly/probe related layout rules”. The layout rules for bonding pads are package dependent.
Bonding pad no. 1 will be angled at all four corners.
Refer to AMI Semiconductor Belgium Spec DS13299 "Maskgeneration CMOS 0.7 µm Enhanced" :

It is recommended that metallization to a bonding pad will be through a metal fillet and leadaway. The rules 5.1.17, 5.1.18, 5.1.19, and 5.1.20 are recommended rules.

			Codes DS13600
5.1.1	Minimum bonding pad size (overlay window): L = W	See DS13600	H
5.1.2a	Minimum bonding pad spacing	See DS13600	P2-H
5.1.2b	Minimum bonding pad spacing (valid for the 5 pads most closed to the corners of the die, in some packages)	See DS13600	P1-H
5.1.3	Minimum Nwell enclosure of bondpad (if drawn)	5.0	-
5.1.4	No POLY allowed underneath the pad		-
5.1.5	No contact allowed underneath the pad		-
5.1.6	Minimum metal1 enclosure of bondpad	3.0	K
5.1.7a	Minimum Via1-2 enclosure of bondpad (Via2 is generated)	1.0	-
5.1.7b	Minimum of Metal2/Metal3 over Via1-2 (Metal3 is generated)	2.0	-
5.1.8	Minimum Metal2-3 enclosure of bondpad (MTL3 generated)	3.0	K
5.1.9	Polyimide opening enclosure of pad	25.0	-
5.1.10	Minimum bonding pad to Nwell spacing	13.0	-
5.1.11	Minimum bonding pad to active area spacing	11.0	-
5.1.12	Minimum bonding pad to polysilicon spacing	13.0	F+K
5.1.13	Minimum bonding pad to contact window spacing	13.0	F+K
5.1.14	Minimum bonding pad to Metal 1 spacing	13.0	F+K
5.1.15	Minimum bonding pad to Via1 & 2 spacing	13.0	F+K
5.1.16	Minimum bonding pad to Metal2 & 3 spacing	13.0	F+K
5.1.17	Minimum metal2 & 3 fillet width along the bond pad	30.0	
5.1.18	Minimum metal2 & 3 fillet length	15.0	
5.1.19	Minimum metal2 & 3 leadaway width	10.0	
5.1.20	Minimum metal2 & 3 leadway length	20.0	

BONDING PADS

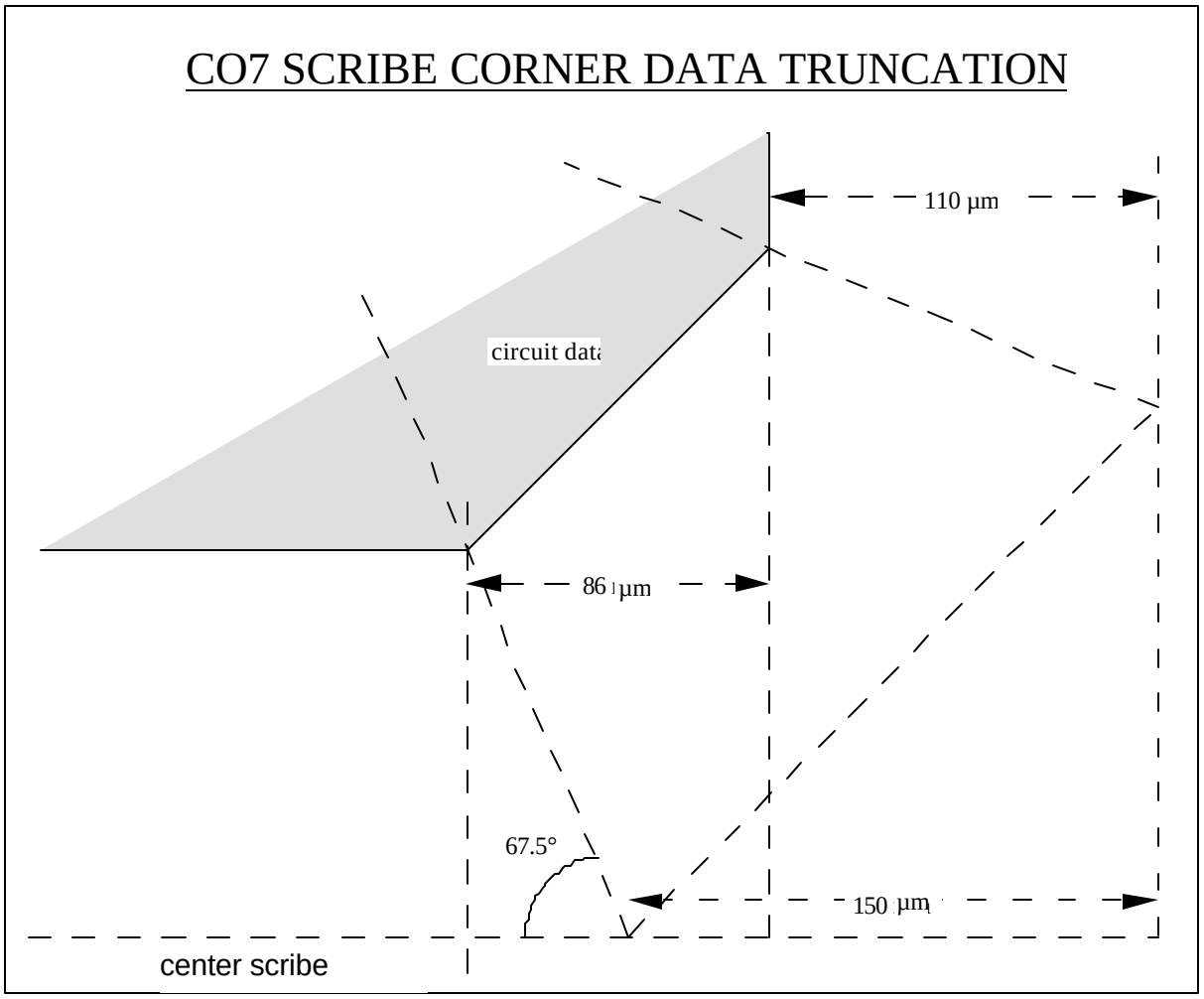




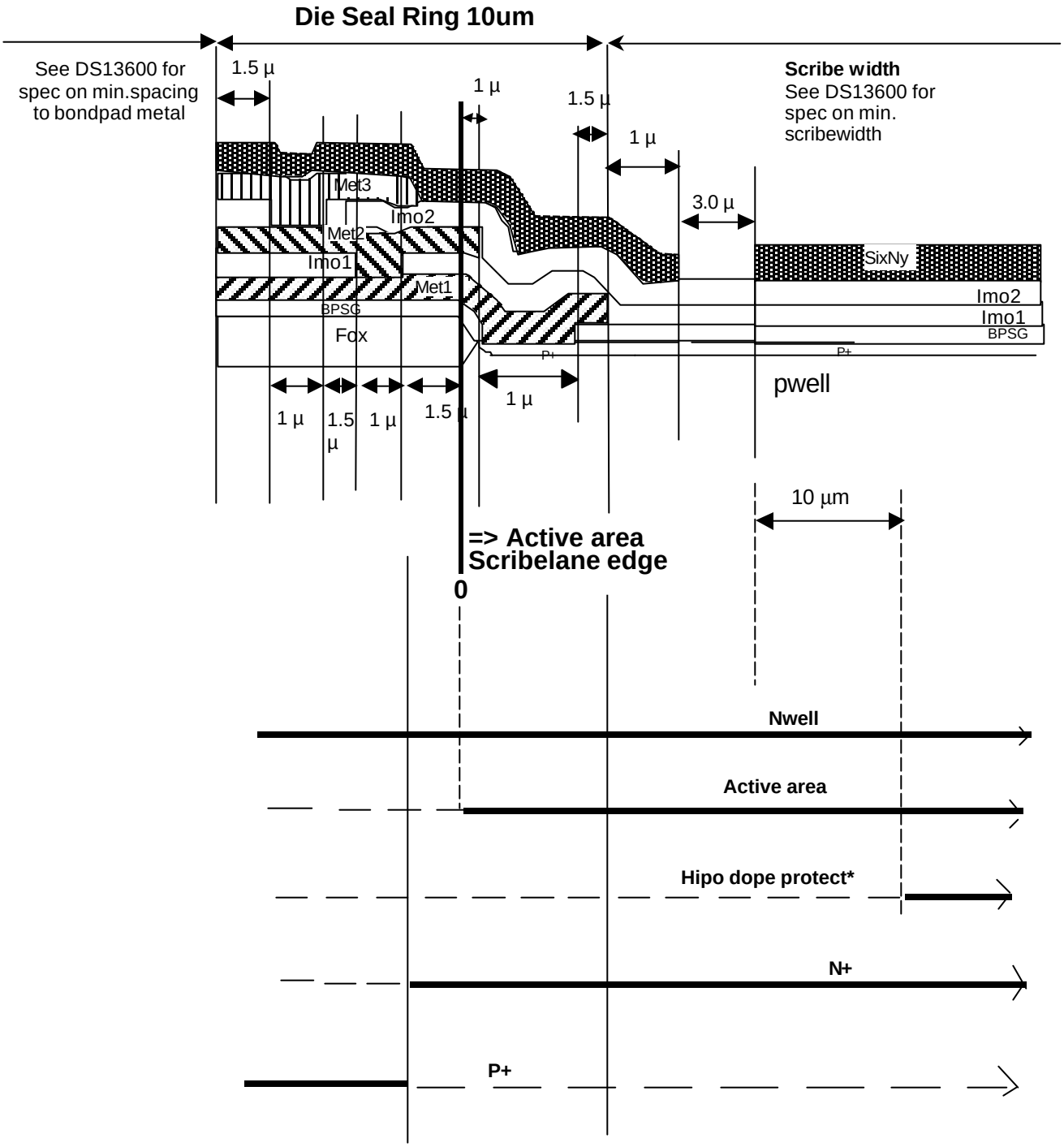
BONDING PAD CROSS-SECTION

EDGE-OF-DIE

The corners of the die will be angled as illustrated in the figure below.



5.2 Scribe Lane & Edge-of-Die without TEG



All the drawn data are mask data without bias.

* HIPO_DOPEPROTECT in the middle of the scribe insert without TEG structures, increases the lowly doped poly area to be able to control the poly etch more accurately.

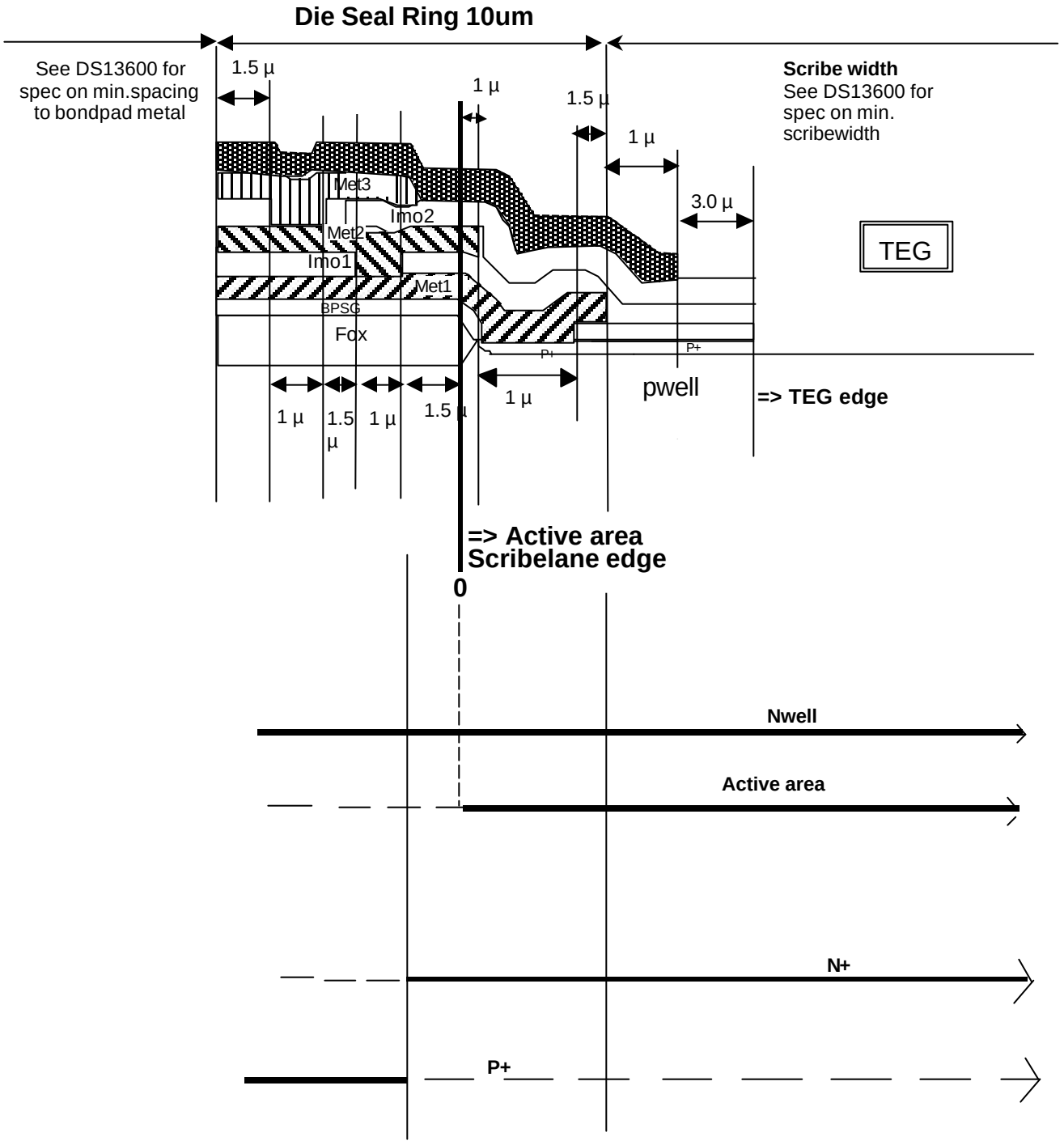
5.2.1 Overview table for scribe lane & edge of die finishing

Underlaying table is a summary of the spacing for the different layers towards the active area scribe lane edge.

Layer	From	To
ACTIVE	0	Center scribe
HIPO_DOPEPROTECT	17.5 µm	Center scribe
P+	-1.5 µm	Center scribe
N+ (not)	-1.5 µm	Center scribe
Contact	1 µm	2 µm
Metal 1	-6.5 µm	3.5 µm
Via1	-2.5 µm	-1.5 µm
Metal 2	-6.5 µm	1 µm
Via 2	–5 µm	-4 µm
Metal 3	-6.5 µm	-1 µm
Overlay opening	4.5 µm	7.5 µm

For the minimum spacing circuit to active area scribe lane edge, see DS13600.
If there is a Vss bus present on the circuit data the Vss bus can be as close as 5 µm to the metal of the scribe lane finishing ring.
So starting at -11.5 µm referring to the active area scribe lane edge.
Note that this is only applicable for a Vss bus. The minimum width of the Vss ring is 10 µm.

5.3 Scribe Lane & Edge-of-Die with TEG



All the drawn data are mask data without bias.

6.0 GENERAL LAYOUT REQUIREMENTS

6.1 General

6.1.1 Apart from 0° and 90° layout, only 45° angles are allowed.

6.1.2 A n-well cannot be used as a cross-under for Vdd connections.

6.1.3 Resistors in input protection circuitry must not be used as cross-unders. Minimum spacing to unrelated metal shall be 19 µm.

6.1.4 Corners of bends of input protection resistors must be at 45° angles.

6.1.5 All input protection diodes must be hard wired to the Vdd and Vss pads via metal. Cross-unders or substrate contacts to these devices are not allowed.

6.1.6 The chip size as defined by the scribe lane center must be a multiple of 10.0 µm to allow compatibility with testing and scribing equipment.

6.1.7 Transistor length is measured from drain to source as defined by the polysilicon mask. Device width is equal to the width center line of the gate with one half the device channel length subtracted for each 90° bend.

6.1.8 Resistor length is measured by counting the numbers of squares from contact edge to contact edge; a 90° bend is counted as one half square.

6.2 Product Identification

6.2.1 Chip name

6.2.1.1 Every chip must be identified. The chip identification must be placed according to the following rules:

6.2.1.2 The chip name must always be present in the circuit. It must appear only once in the circuit.

6.2.1.3 The chip name must be written on the metal layers only.

6.2.1.4 The chip name should be designed according to the layout rules; only 45° angles can be used.

6.2.1.5 If the chip name is not placed, an empty space of 250 µm x 50 µm must be preserved for this purpose.

6.2.2 AMI Semiconductor Belgium logo

6.2.2.1 The AMI Semiconductor Belgium logo must always be present in the circuit, unless clearly forbidden.

6.2.2.2 The AMI Semiconductor Belgium logo shall preferably be placed near the chip name.

6.2.2.3 If the AMI Semiconductor Belgium logo is not placed, an empty space of 125 µm x 75 µm must be preserved for this purpose.

6.2.3 Layer and iteration numbering

6.2.3.1 Every circuit must contain Layer and Iteration Numbering. This can be combined with the CD structures.
6.2.3.2 All layer iterations on a completely new chip will be "A".
6.2.3.3 They should not introduce layout rule errors; only 45° angles are allowed.
6.2.3.4 The overlay mask should have no Layer and Iteration Numbering at all.

6.3 Latch-up and ESD Protection Rules

6.3.1 I/O cells

Only standard I/O cells are allowed for latch-up and ESD protection. For deviations of the standard I/O cells, please contact AMI Semiconductor Belgium.

6.3.2 Latch-up guidelines for core cell design.

6.3.2.1 It is advised to use as many as possible Nwell straps and Psubstrate straps.
6.3.2.2 Active Area should be covered with as much as possible contacts and metal straps.

6.4 Electromigration Design Rules

6.4.1 Contacts and vias

6.4.1.1 Only minimum dimension contact windows can be used.
6.4.1.2 Whenever the current exceeds the calculated values, multiple contacts must be used. The minimum number N of contacts or vias required for an equivalent current level is;

$$N = Kc * Ieq * f(T)$$

where;

Kc = 1/ (maximum current through a single contact or via at 142°C)
f(T) = exp { 7.0 *(1- 415/T) }
T = the absolute temperature (Kelvin) determined for worst case application of each design.
Ieq is the equivalent current determined as specified in 6.5.1.4

6.4.1.3 The appropriate values for Kc can be found from the following table;

Contact	Contact	Via1	Via 2
Size (nominal)	0.8	0.8	1.0
Max current/contact at 1428C { f(T)=1 }	0.24	0.28	0.35
Kc	3.33	2.85	2.85

6.4.1.4 Determination of the equivalent current

LOW FREQUENCIES (period > 200 nsec)

a) Repetition frequencies less than 5 MHz
The equivalent current is equal to the RMS current.

b) DC current
The equivalent current is equal to the direct current.

c) Pulse DC and AC (Bi-directional)
The equivalent current is equal to the RMS current.
The RMS current should be calculated as
Ieq = {Integral (i(t)^2 dt) / Tc} ^ 0.5
where the limits of the integral are T0 to T0 +Tc, with T0 the start temperature, and Tc the final temperature after Joule heating

HIGH FREQUENCIES (period = 200 nsec)

a) Repetition frequencies greater than 5 MHz
The equivalent current is equal to the average of the absolute value of the current.

b) Pulse current
For DC pulse current, irregular waveforms in one direction, and each direction component of AC current, the equivalent current is the current averaged over the worst case operating cycle.

PEAK CURRENT
For both low and high frequency pulse, D.C. and A.C. currents, the peak current shall be limited to 25 times the DC current.
That is;
Ieq >= 0.04 * Ipeak

6.4.2 Metal electromigration

6.4.2.1 The minimum metal 1 linewidth to be used is calculated from the formula:

W = K* Ieq*f(T) + ?W

where;

K = 1/{minimum Al thickness * Al stepcoverage * Imax}
Imax = 2 mA/ µm^2 at 142°C { f(T)=1 }
f(T) = exp { 7.0 *(1- 415/T) }
Ieq is the equivalent current as specified in 6.4.1.4

T is the absolute operating temperature (in Kelvin) determined for the worst case application (and package type) of each design.
?W is the CD variation

6.4.2.2 Values for metal conductor thickness

Values for the minimum aluminium thicknesses, step coverage and ?W are provided in the following table;

Conductor	Metal 1	Metal 2 DLM Metal 3 TLM	Metal 2 TLM	Unit
Max ?W	0.15	0.2	0.2	µm
Min Al thickness	5400	7600	5800	Angstrom
1. Flatregions				
Al stepcoverage	100	100	100	
K	0.92	0.66	0.86	µm/mA
2. Rough topography				
Al stepcoverage	90	90	90	
K	1.03	0.73	0.96	µm/mA
3. Contacts & Vias				
Al stepcoverage	25	25	25	
K	3.7	2.6	3.4	µm/m