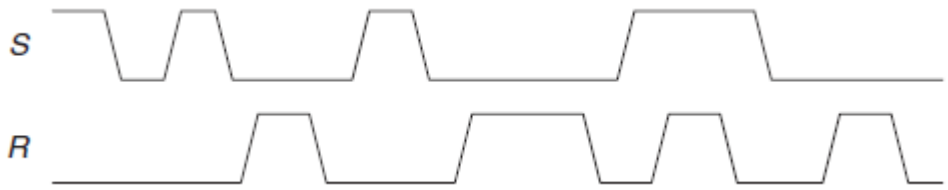
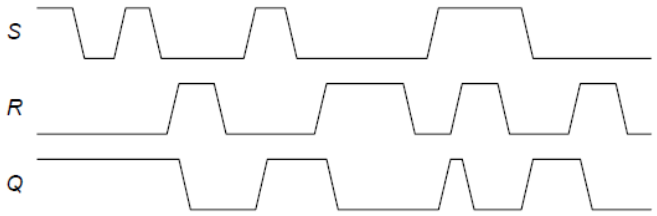
Latch and Flip-Flop

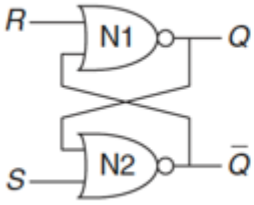
Exercise 1 – Given the input waveforms below, sketch the output, Q, of an SR latch.



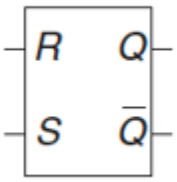
Solution:



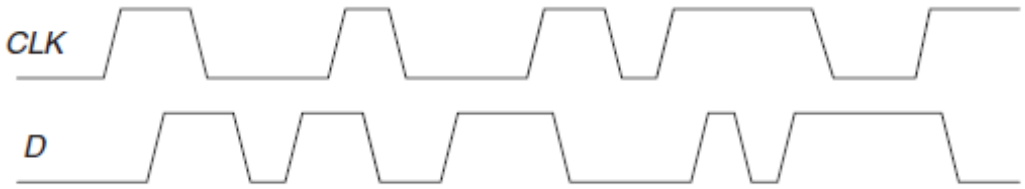
Design a SR latch on DEEDS and simulate it to check that the circuit is working properly.
Use the timing diagram simulation to check the correctness of your answer.



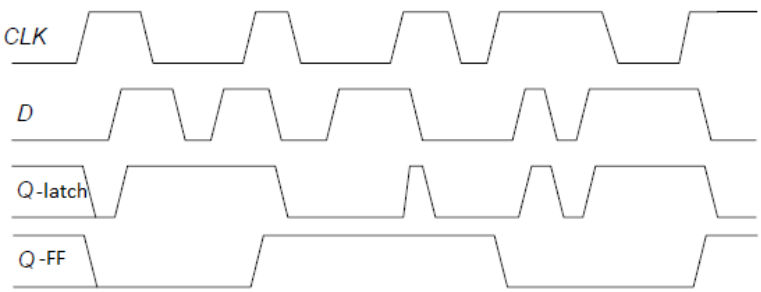
Case	S	R	Q	$\bar{Q}$
IV	0	0	Q_{prev}	$\bar{Q}_{prev}$
I	0	1	0	1
II	1	0	1	0
III	1	1	0	0



Exercise 2 – Given the input waveforms below, sketch the output, Q-latch, of a D latch and the output Q-FF of a D flip-flop.

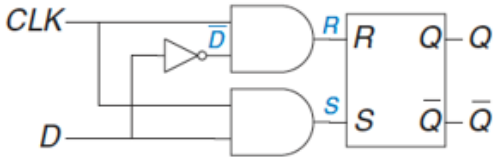


Solution:

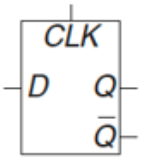


Design a D latch and a D flip-flop on DEEDS and simulate it to check that the circuit is working properly. Use the timing diagram simulation to check the correctness of your answer.

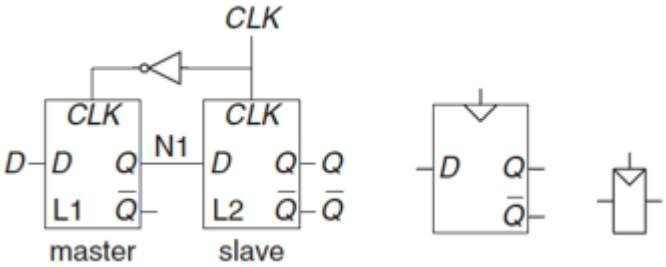
D Latch:



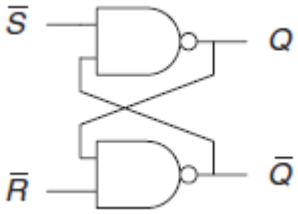
CLK	D	$\overline{D}$	S	R	Q	$\overline{Q}$
0	X	$\overline{X}$	0	0	Q_{prev}	$\overline{Q}_{prev}$
1	0	1	0	1	0	1
1	1	0	1	0	1	0



D Flip-Flop:



Exercise 3 – Is the circuit in figure below combinational logic or sequential logic? Explain in a simple fashion what the relationship is between the inputs and outputs. What would you call this circuit?



Solution:

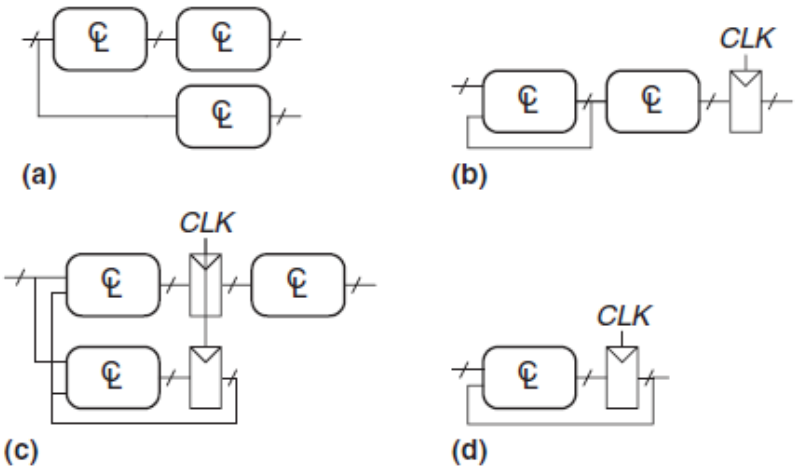
The circuit is sequential because it involves feedback and the output depends on previous values of the inputs. This is a SR latch. When $\overline{S} = 0$ and $\overline{R} = 1$, the circuit sets Q to 1. When $\overline{S} = 1$ and $\overline{R} = 0$, the circuit resets Q to 0. When both $\overline{S}$ and $\overline{R}$ are 1, the circuit remembers the old value. And when both $\overline{S}$ and $\overline{R}$ are 0, the circuit drives both outputs to 1.

Exercise 4 – Which of the circuits in figure below are synchronous sequential circuits? Explain.

(Remind the **rules of synchronous sequential circuit composition:**

- every circuit element is either a register or a combinational circuit
- at least one circuit element is a register
- all registers receive the same clock signal
- every cyclic path contains at least one register

)



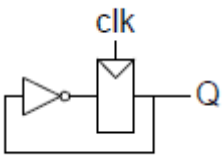
Solution:

(a) No: no register. (b) No: feedback without passing through a register.

(c)Yes. Satisfies the definition. (d) Yes. Satisfies the definition.

Exercise 5 – The toggle (T) flip-flop has one input, CLK, and one output, Q. On each rising edge of CLK, Q toggles to the complement of its previous value. Draw a schematic for a T flip-flop using a D flip-flop and an inverter.

Solution:

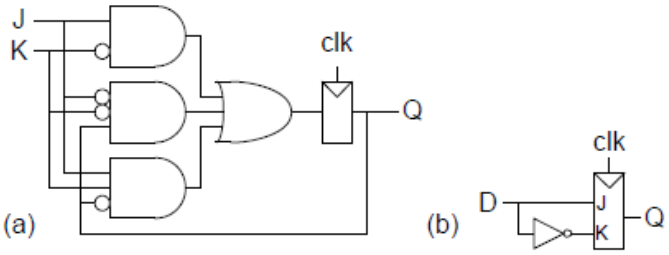


Exercise 6 – A JK flip-flop receives a clock and two inputs, J and K. On the rising edge of the clock, it updates the output, Q. If J and K are both 0, Q retains its old value. If only J is 1, Q becomes 1. If only K is 1, Q becomes 0. If both J and K are 1, Q becomes the opposite of its present state.

(a) Construct a JK flip-flop, using a D flip-flop and some combinational logic.

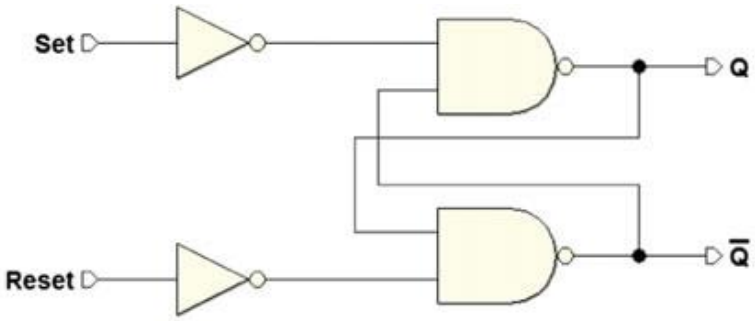
(b) Construct a D flip-flop, using a JK flip-flop and some combinational logic.

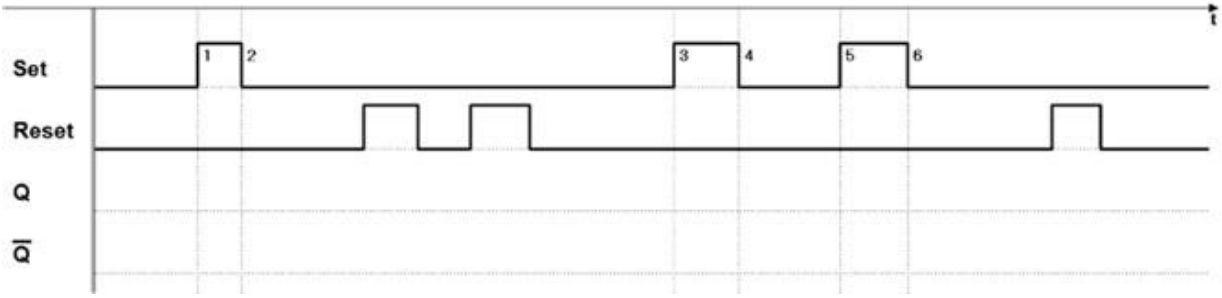
Solution:



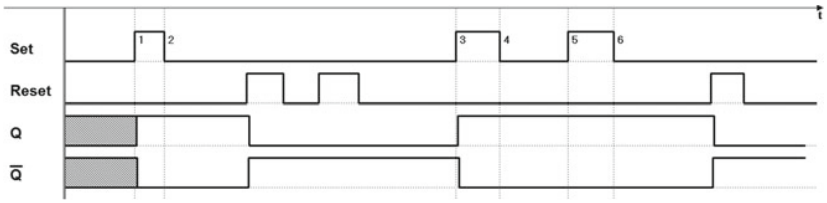
Exercise 7 – For each network below, complete the timing diagram. We suggest drawing first the diagrams without using the simulator and then check your answers with it.

1 - Set-Reset flip-flop (direct command)

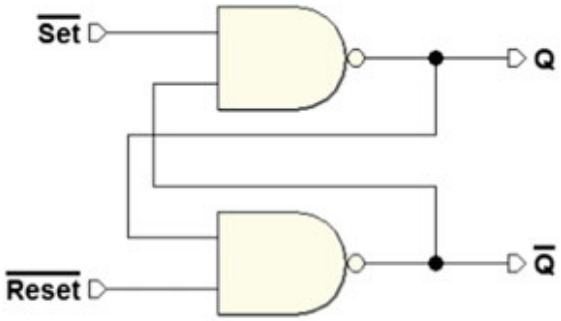


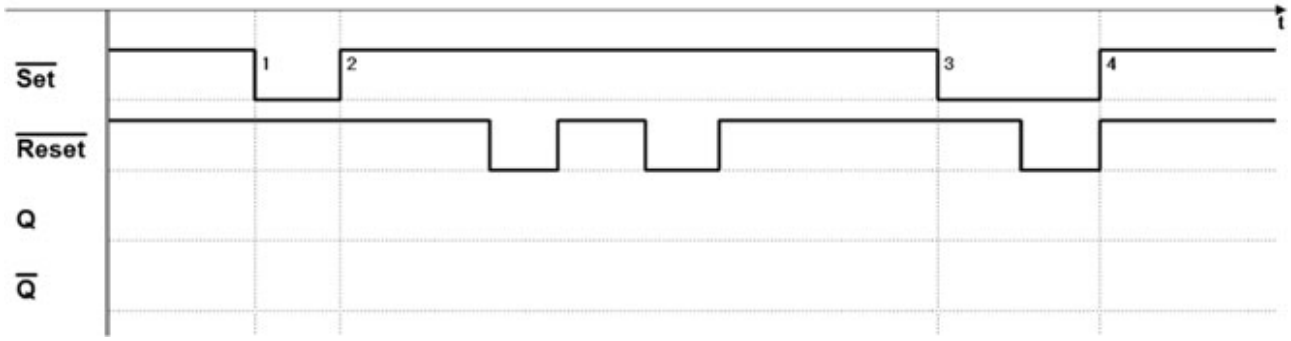


Solution:

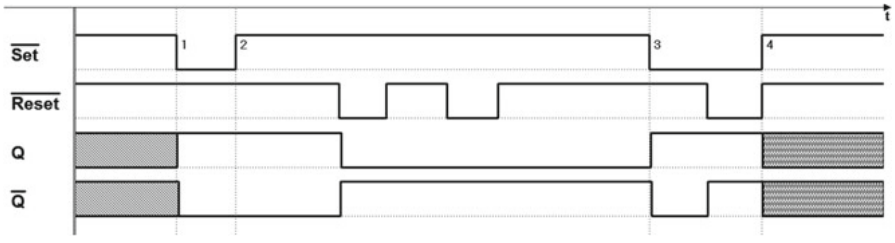


2 - Set-Reset flip-flop (direct command, NAND base cell)

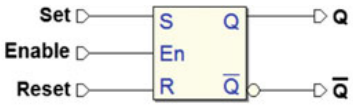


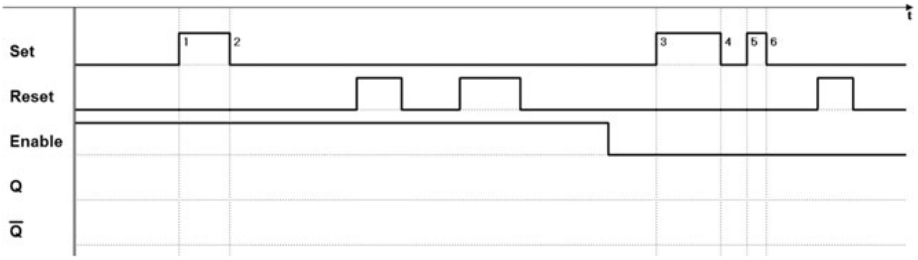


Solution:

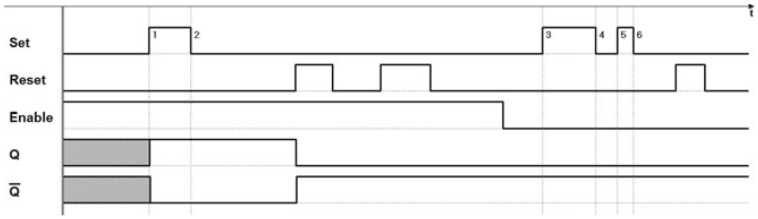


3 - Set-Reset flip-flop (with Enable)

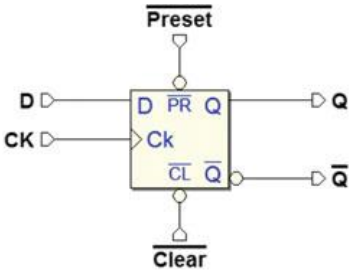


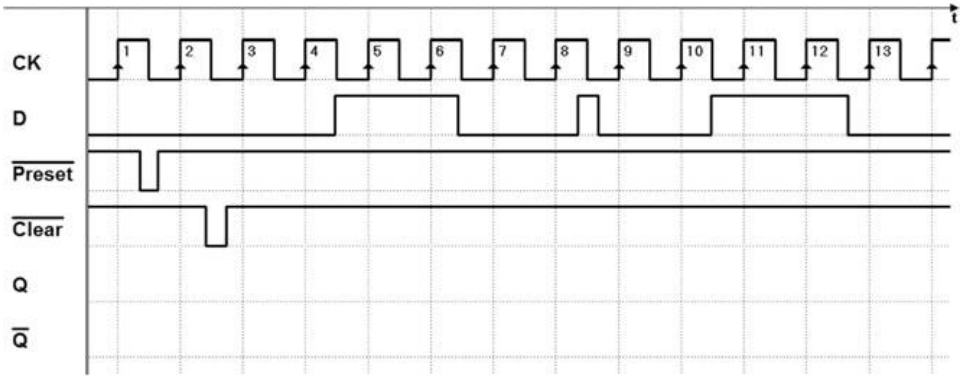


Solution:

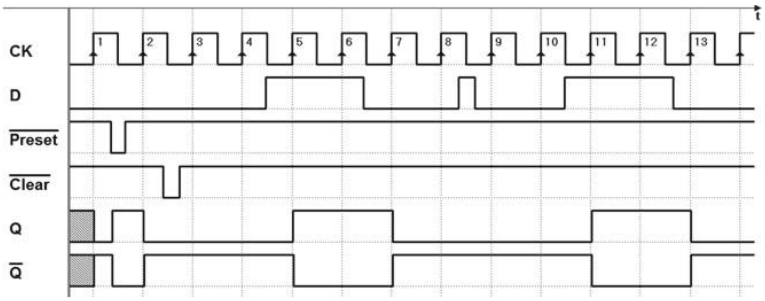


4 - D-PET flip-flop (with Preset and Clear) (PET = Positive-Edge-Triggered: If the active edge is the rising one the structure is called Positive-Edge-Triggered (PET); if the falling edge is active, it is called Negative-Edge-Triggered (NET).)

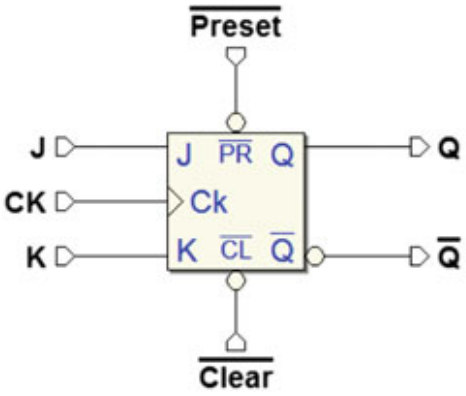


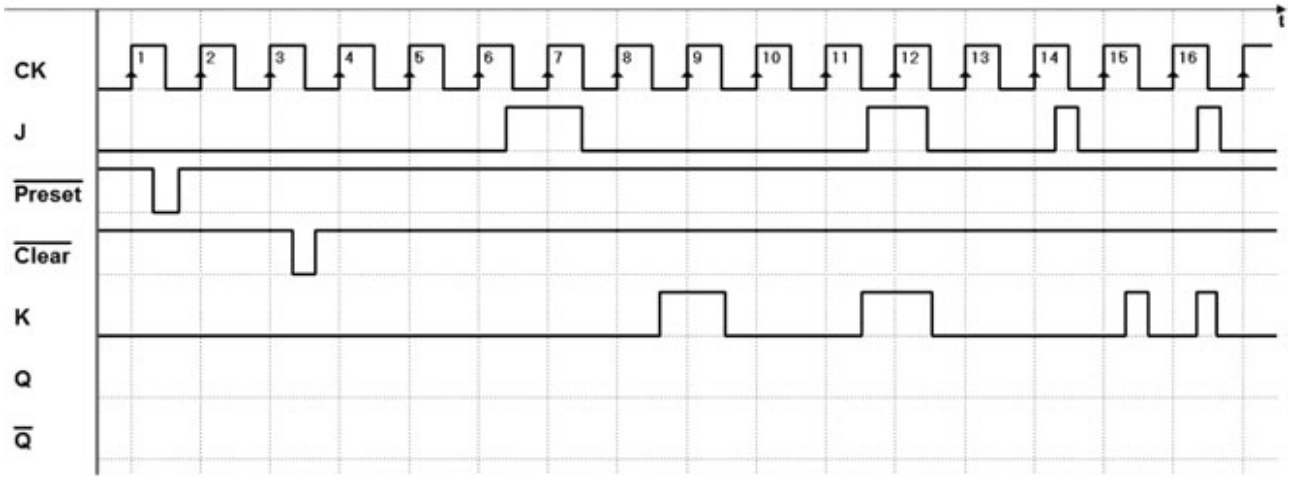


Solution:

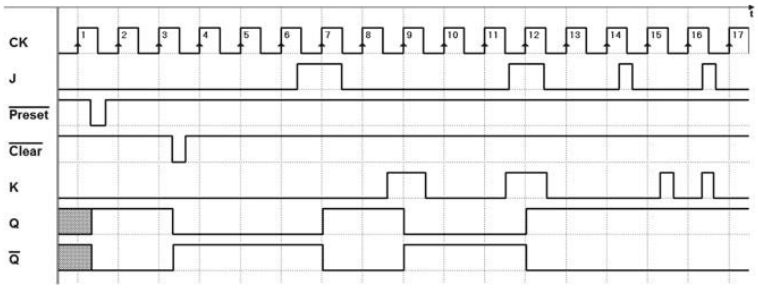


5 - JK-PET flip-flop (with Preset and Clear)

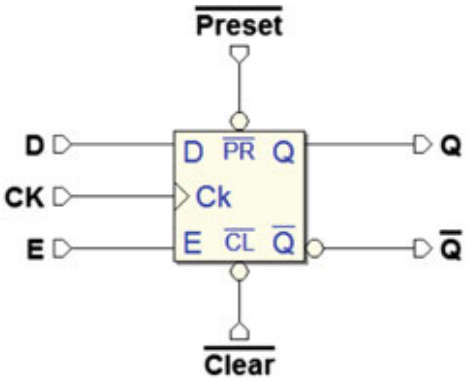


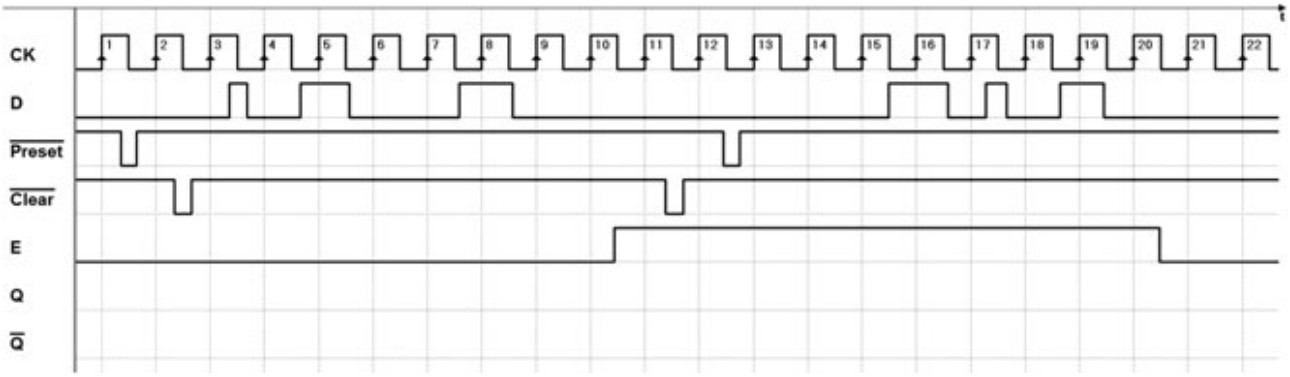


Solution:

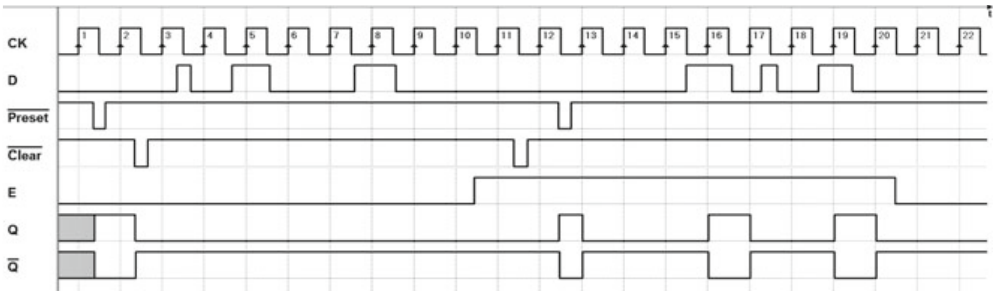


6 - E-PET flip-flop (with Preset and Clear)

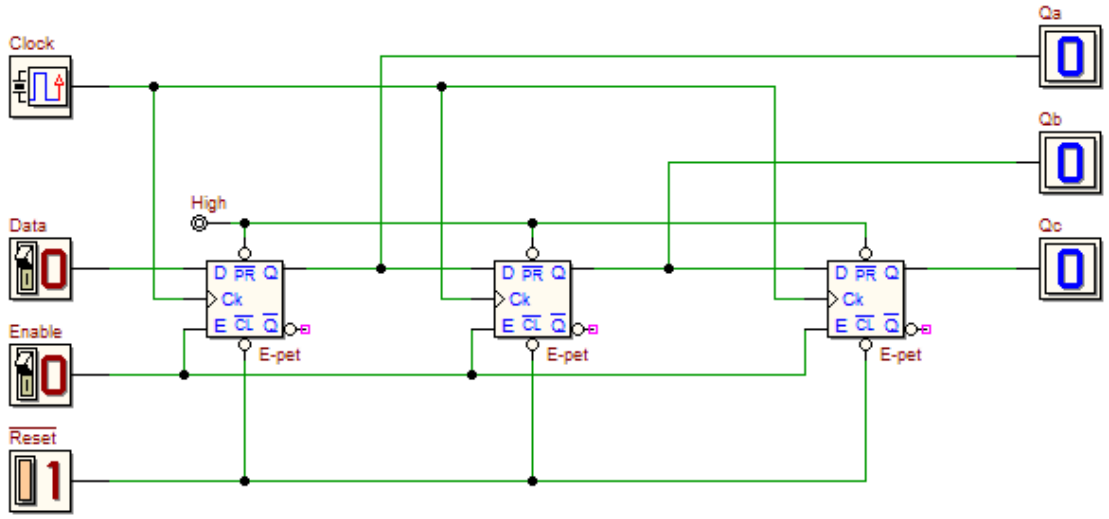




Solution:



Exercise 8 – Analysis of a 3-bits shift-register (E-PET). The following circuit is a 3-bits "shift-register", based on 'E-PET' flip-flops.



Once completed the schematic, using the timing simulation, verify the correct flow of the information through the register, given a suitable data input waveform.

Next, consider the 3 bits **QaQbQc** as a signed two's complement coded number (Qa = sign) and define a Data input sequence such that the circuit produces the sequence below (represented in decimal):

0, **-4**, **-2**, **+3**, **+1**, **0**.

Write the Data input sequence in a table and specify the Data input values (on the left hand side) and the resulting values (expressed in binary and decimal format) on the output Qa, Qb and Qc on the right side, after the symbol representing the clock event.

!Reset	Enable	Data	Clock	Qa	Qb	Qc	Dec
0	1	**0**	-	0	0	0	**0**
1	1		↑				**0**
1	1		↑				**-4**
1	1		↑				**-2**
1	1		↑				**+3**
1	1		↑				**+1**
1	1		↑				**0**

Verify all the operations with the timing simulator.