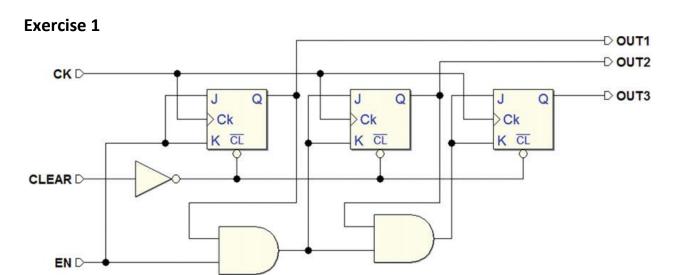
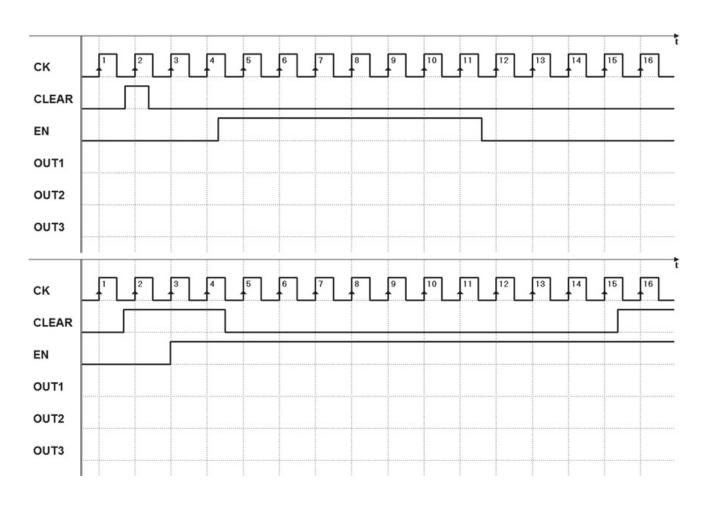
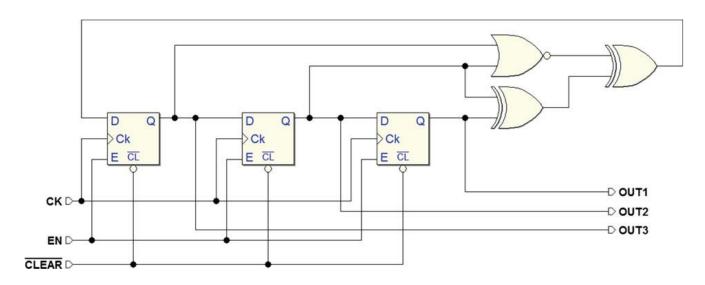
### **Time analysis**

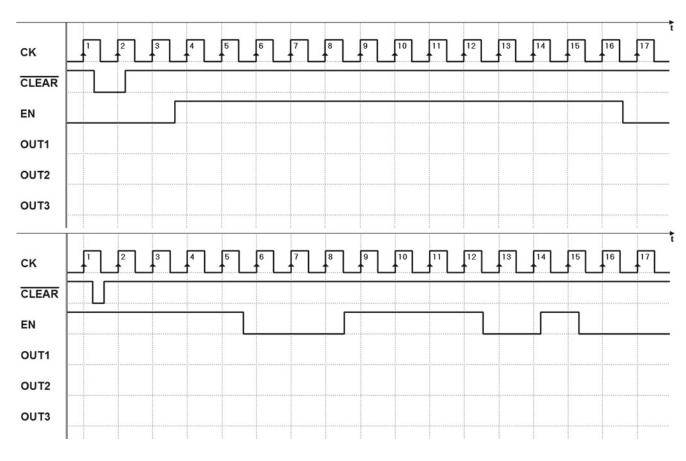
Analyze the following synchronous sequential networks by completing the timing diagrams on the side page. It is recommended to manually complete these diagrams on paper first, using Deeds only to verifying your solutions.



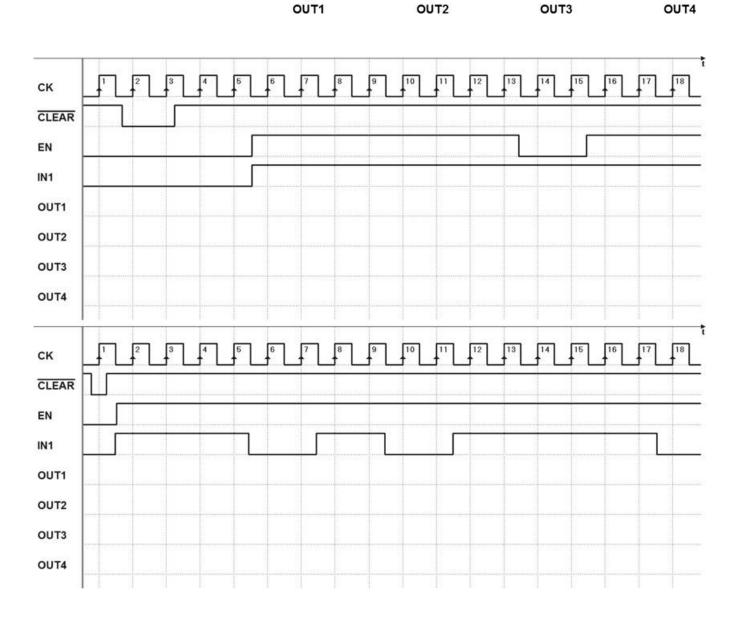


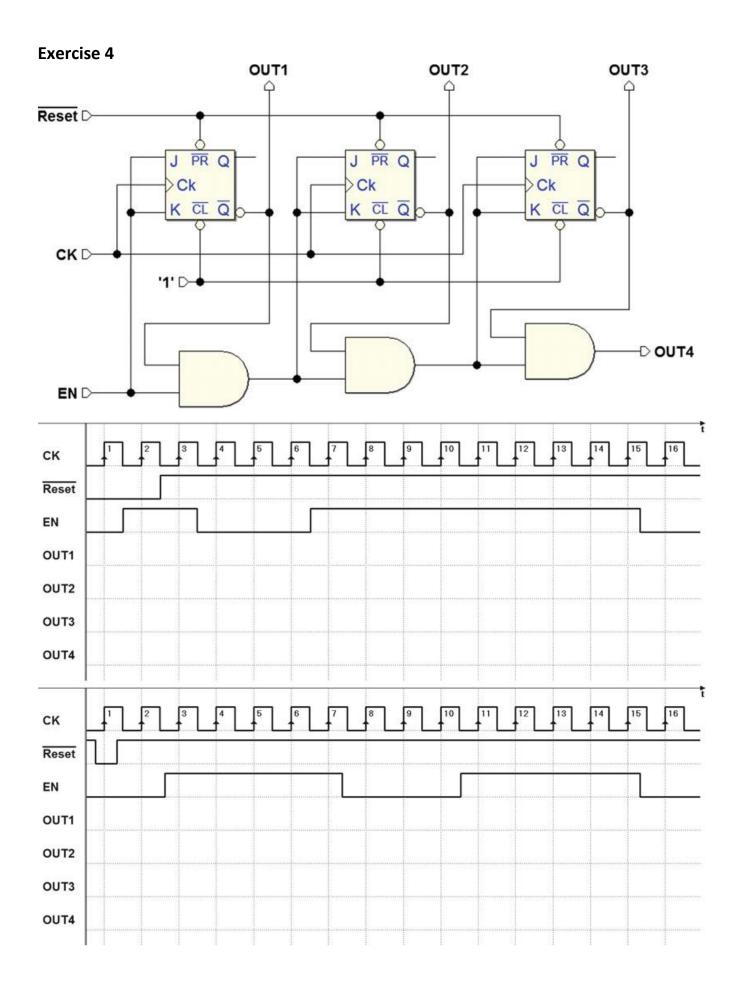
### **Exercise 2**

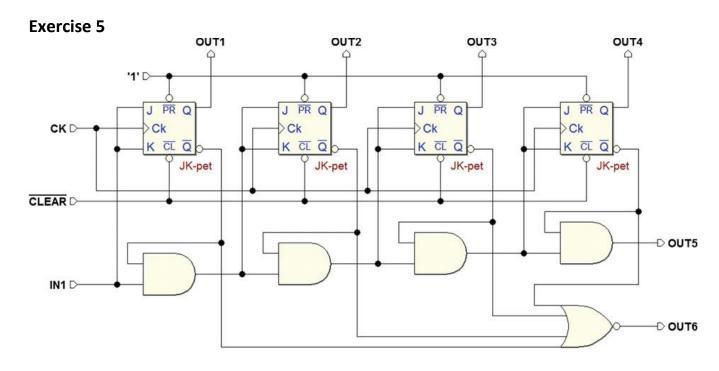


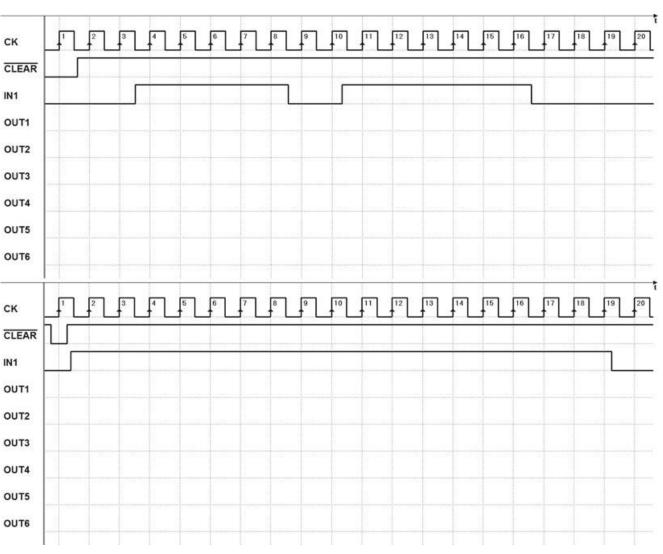


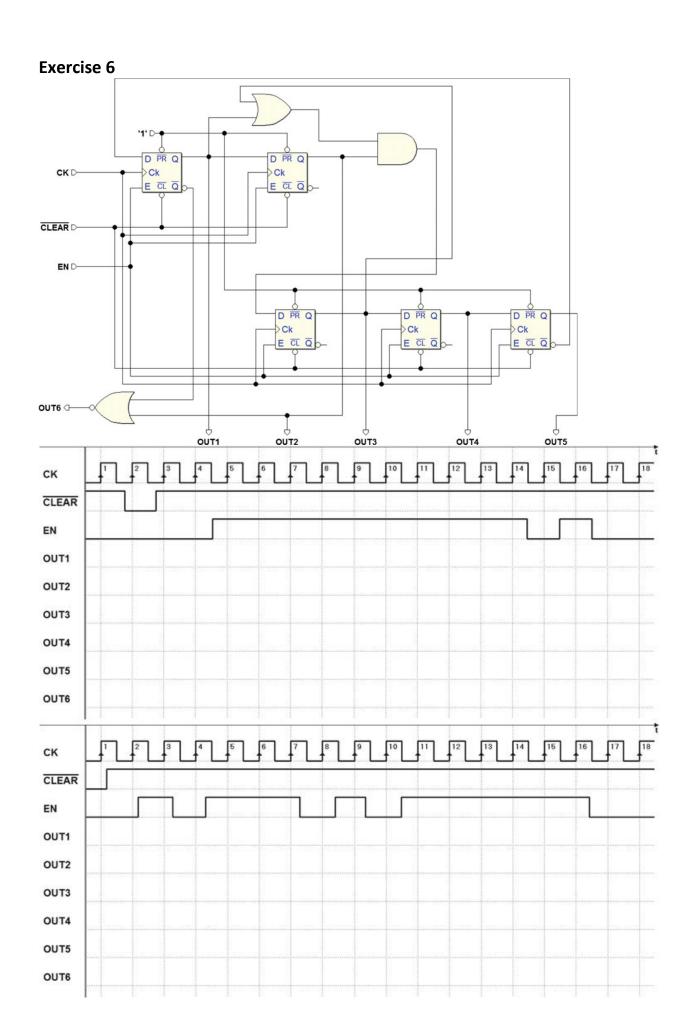
#### **Exercise 3** '1' D D PR Q D PR Q D PR Q D PR Q IN1 D Ck Ck Ck Ck E CL Q E CL Q E CL Q E CL Q CK D-CLEAR D EN D

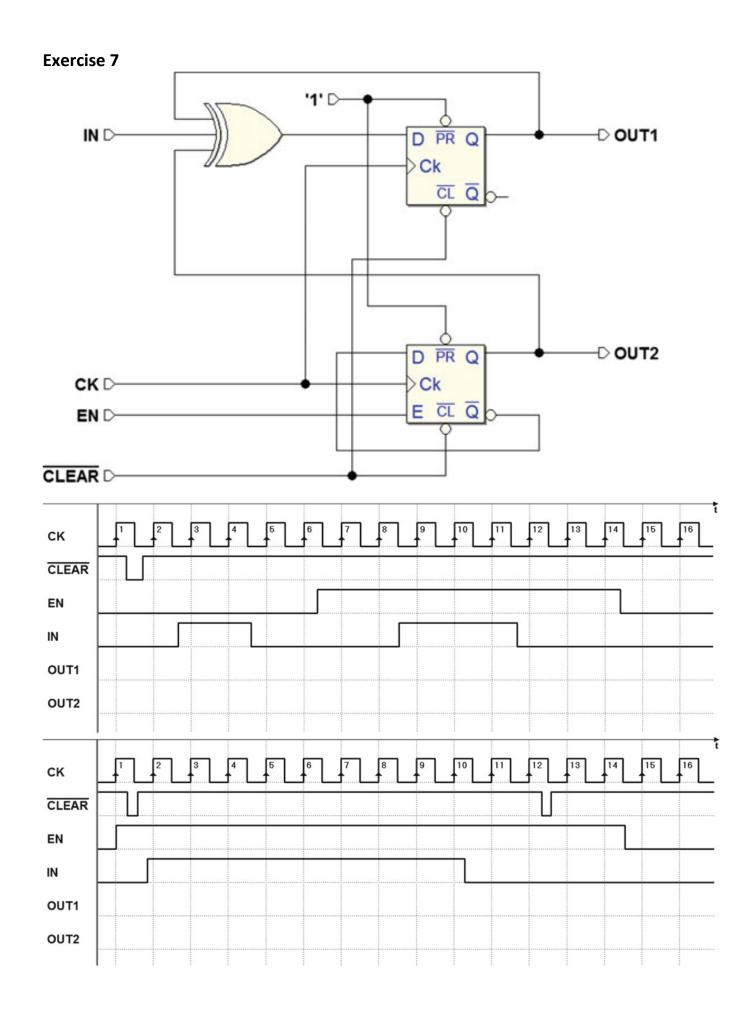


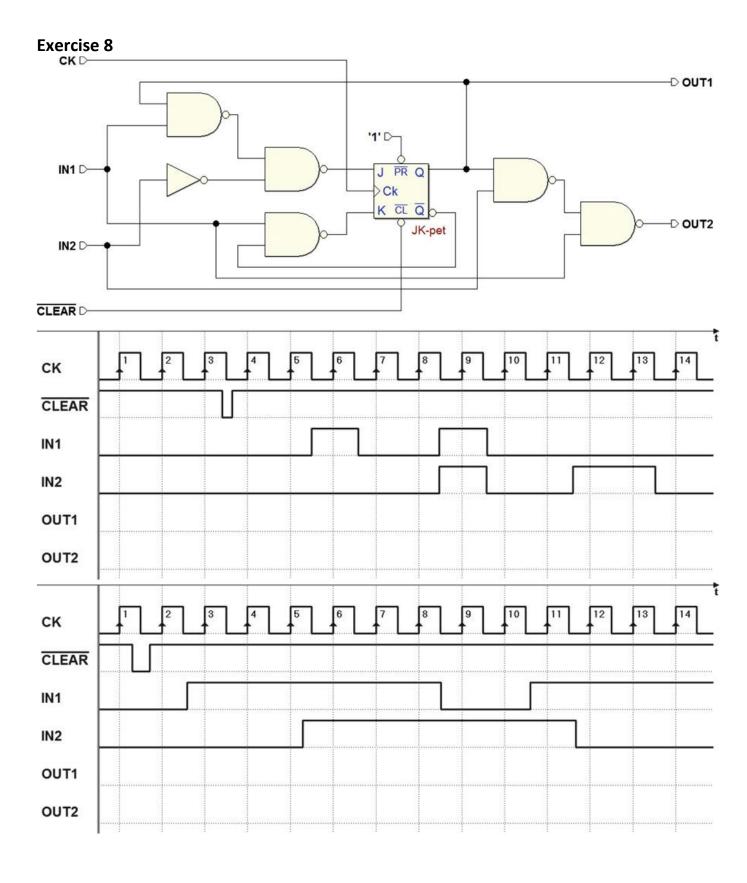


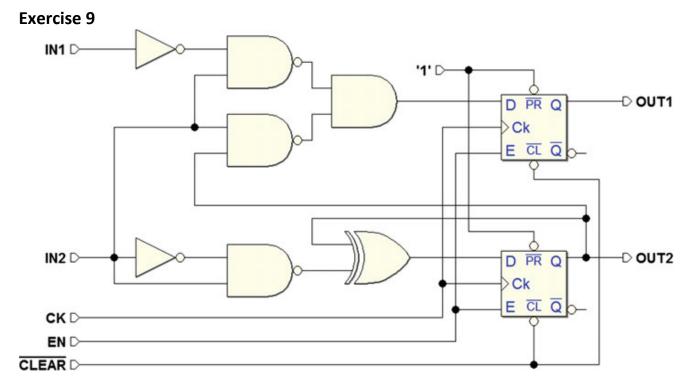


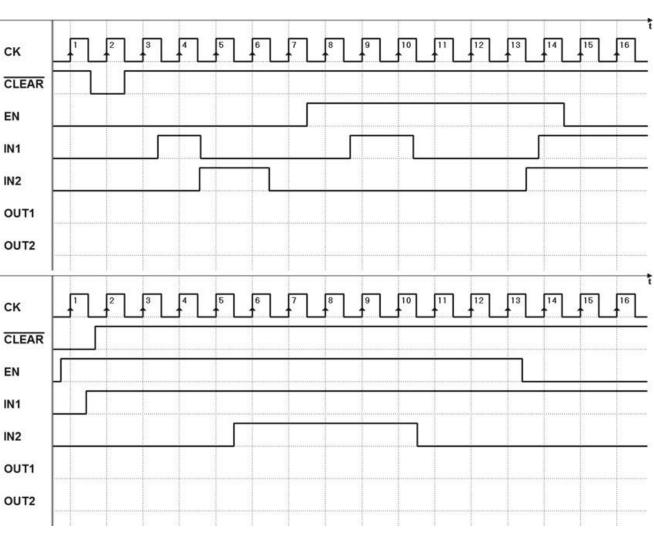












## **Exercise 10** -D OUT1 '1' D J PR Q D OUT2 Ck K CL Q JK-pet -D OUT3 -D OUT4 '1' D IN2 D D PR Q Ck E CL Q E-pet CK D-EN D CLEAR D CK CLEAR ΕN IN1 IN2 OUT1 OUT2 OUT3 OUT4 CK CLEAR EN IN1 IN2 OUT1 OUT2 OUT3 OUT4

# **Solutions**

