
ESD - Elettronica dei Sistemi Digitali

Solutions on Logic Gates and Circuits

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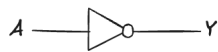
1 Logic gates and circuits Exercises

1.1 Exercise 1

Complete the truth tables of the following gates and use the DEEDS simulator to verify their correctness:

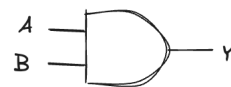
1.1.1 (a) NOT, AND, NAND

NOT



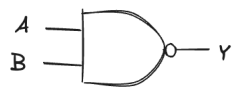
A	Y
0	1
1	0

AND



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

NAND



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

1.1.2 (b) OR, NOR, XOR

OR



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

NOR



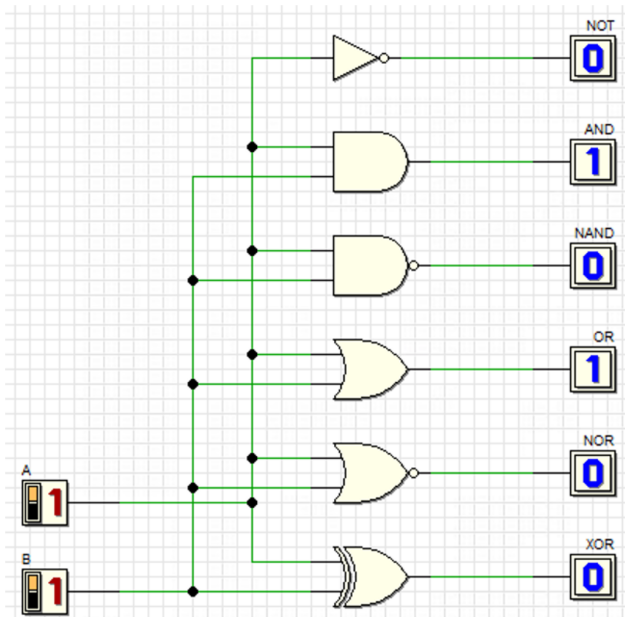
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

XOR



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

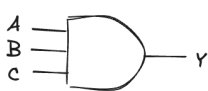
1.1.3 (c) DEEDS simulation



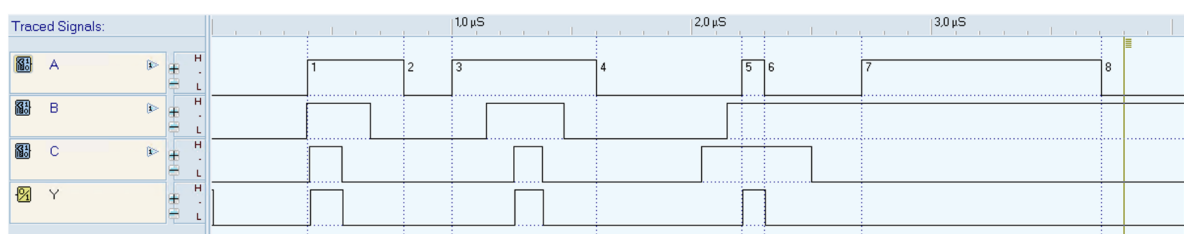
1.2 Exercise 2

Complete the truth table and the timing diagram of the following 3-inputs digital circuits, and use the DEEDS simulator to verify their correctness:

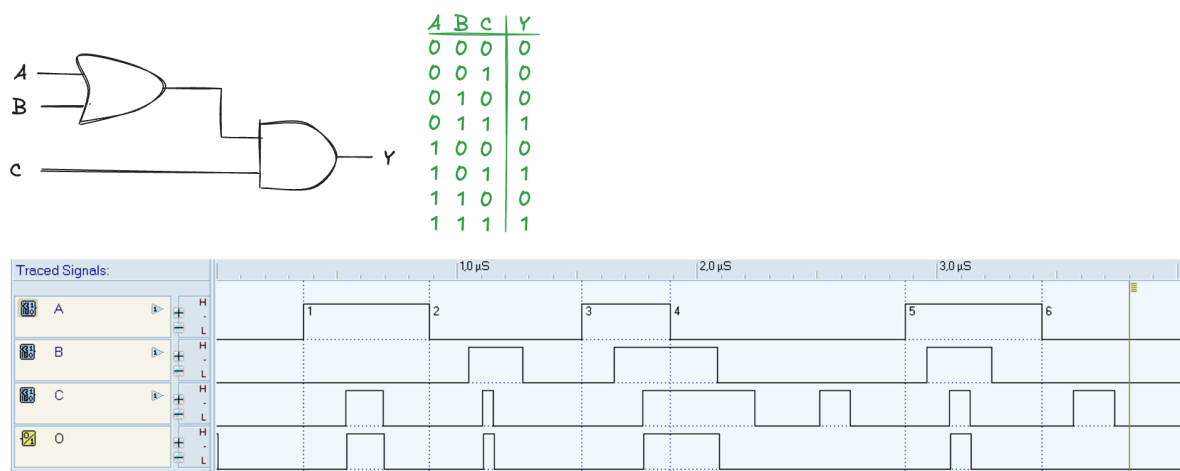
1.2.1 (a)



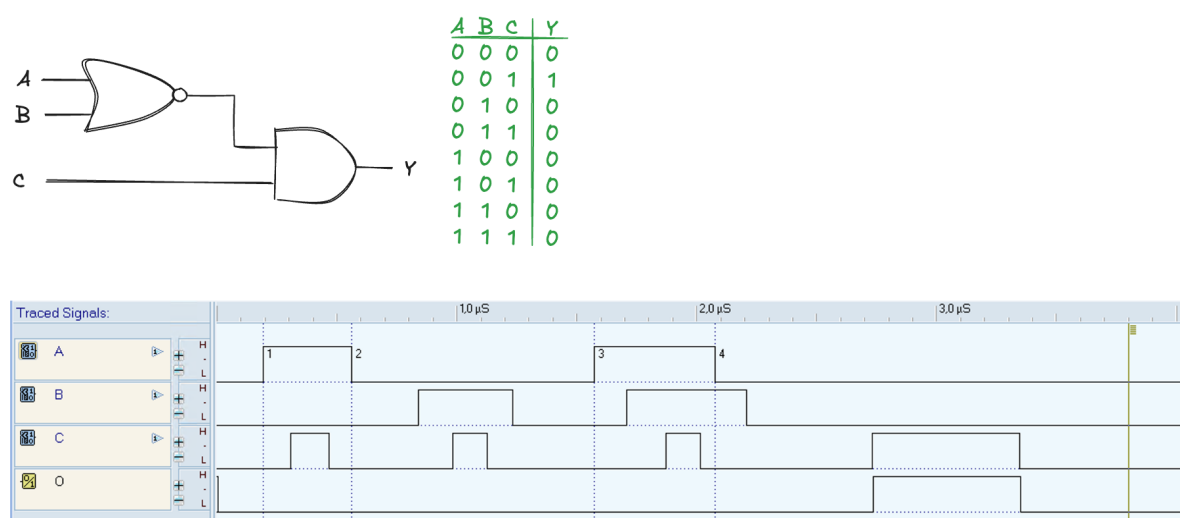
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



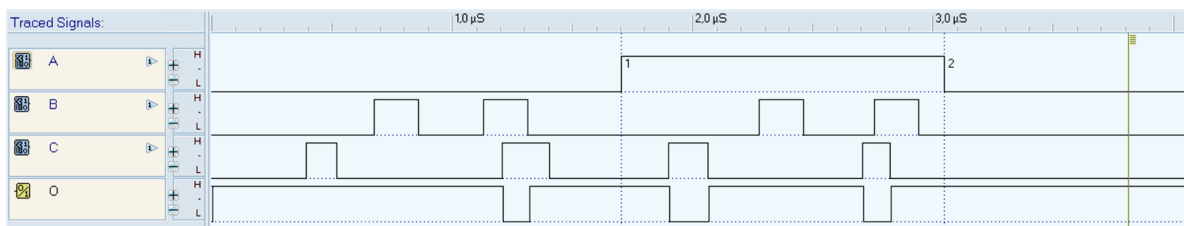
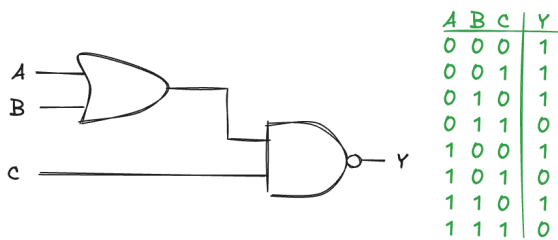
1.2.2 (b)



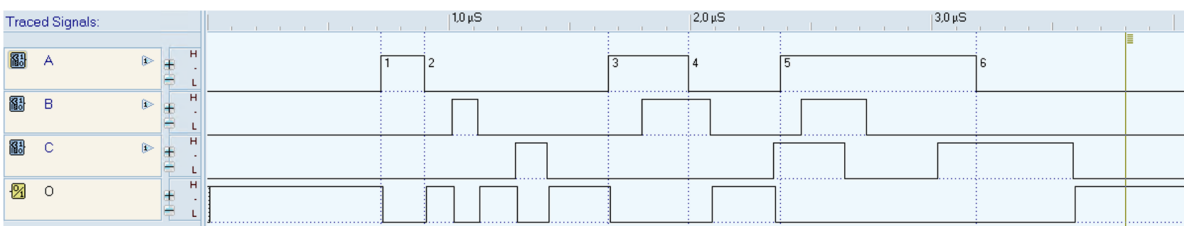
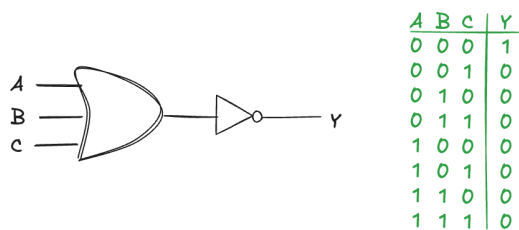
1.2.3 (c)



1.2.4 (d)



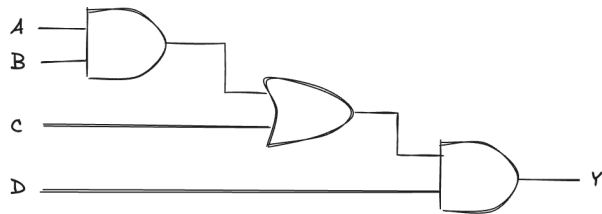
1.2.5 (e)



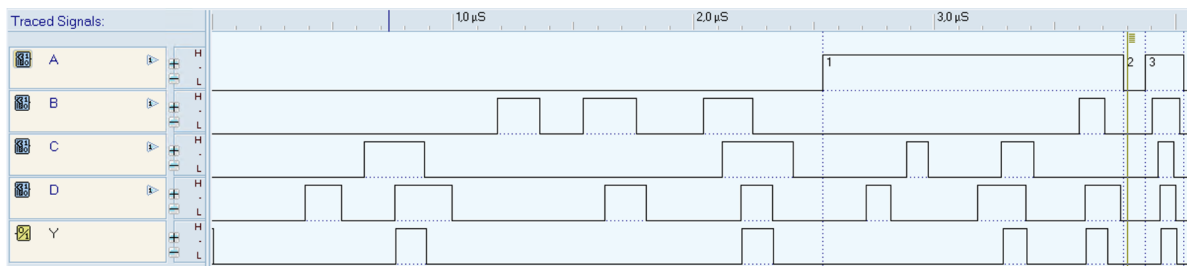
1.3 Exercise 3

Complete the truth table and the timing diagram of the following 4-inputs digital circuits, and use the DEEDS simulator to verify their correctness:

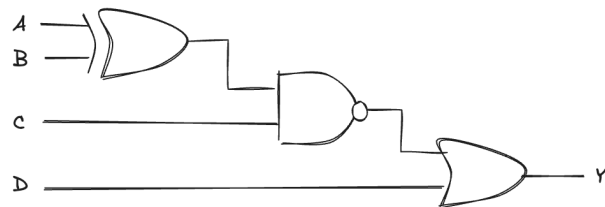
1.3.1 (a)



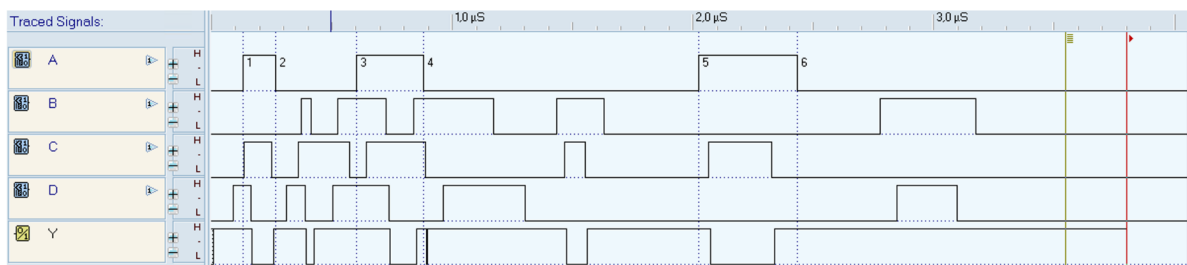
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1



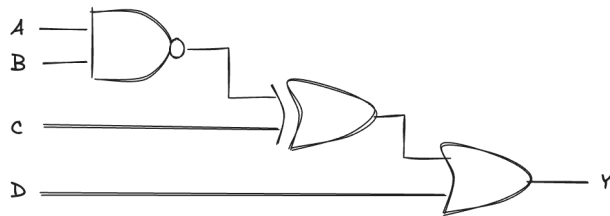
1.3.2 (b)



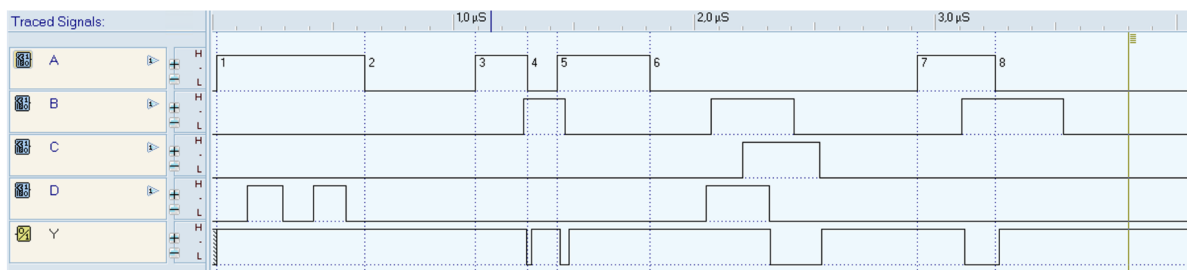
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



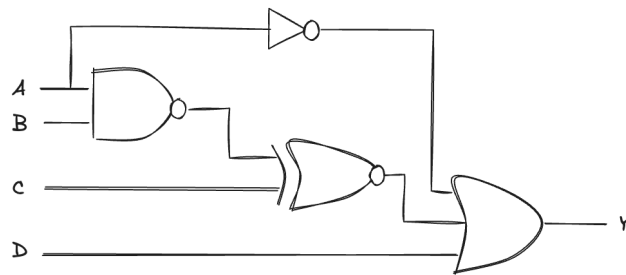
1.3.3 (c)



A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



1.3.4 (d)



A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

