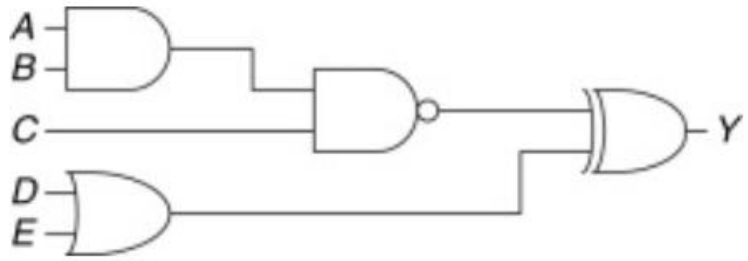
Timing

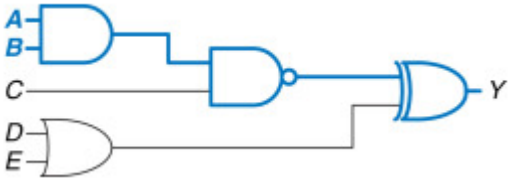
Exercise 1 – You would like to find the propagation delay and contamination delay of the circuit shown in figure Below. According to his data book, each gate has a propagation delay of 100 picoseconds (ps) and a contamination delay of 60 ps.



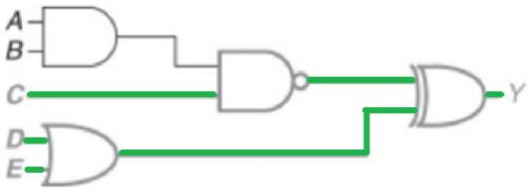
Solution:

Start finding the critical path and the shortest path through the circuit.

In the critical path tpd is three times the propagation delay of a single gate, or 300 ps.

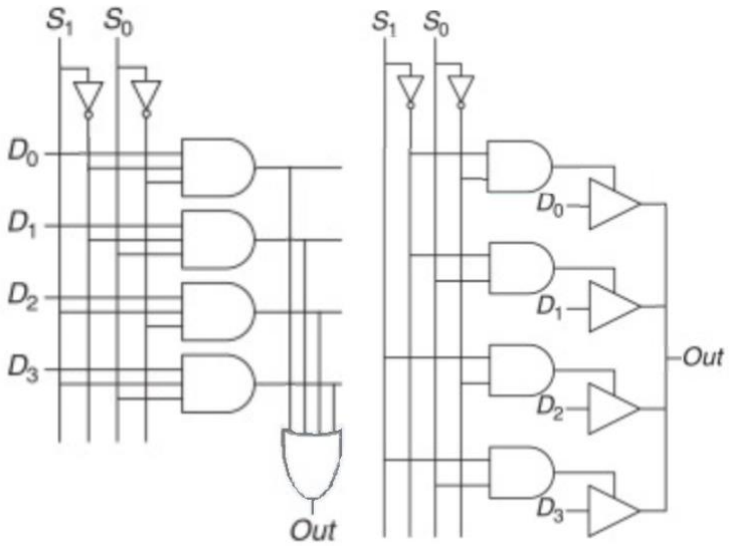


The shortest path are only two gates in the shortest path, so tcd is 120 ps.

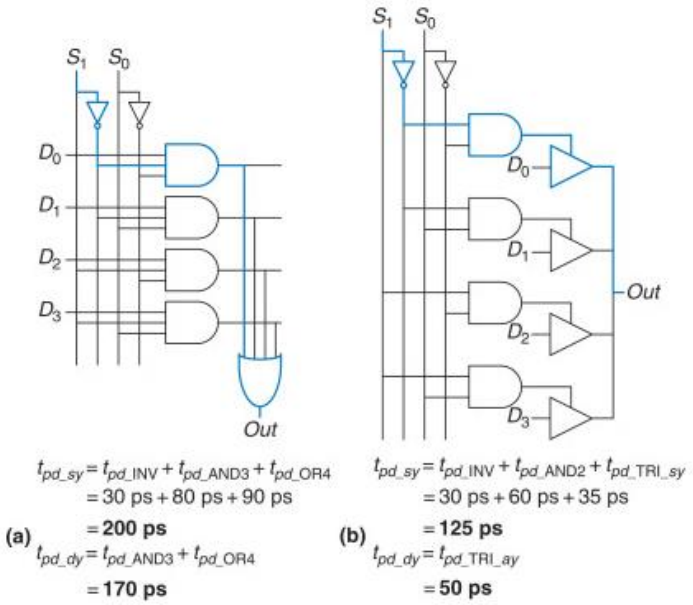


Exercise 2 – Compare the worst-case timing of the three four-input multiplexer designs shown in the two figure below. The table lists the propagation delays for the components. What is the critical path for each design (from control signals to output and from data signals to output)? Given your timing analysis, why might you choose one design over the other?

Gate	t_{pd} (ps)
NOT	30
2-input AND	60
3-input AND	80
4-input OR	90
tristate (*A* to *Y*)	50
tristate (enable to *Y*)	35



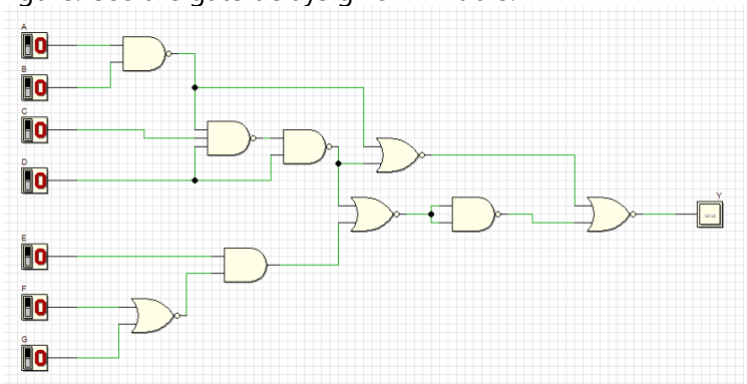
Solution:
One of the critical paths for each of the three design options is highlighted in blue.
tpd_sy indicates the propagation delay from input S to output Y;
tpd_dy indicates the propagation delay from input D to output Y;
tpd for the circuit is the worst of the two: max(tpd_sy, tpd_dy).



For both the two-level logic and tristate implementations in figures, the critical path is from one of the control signals S to the output Y: tpd = tpd_sy. These circuits are control critical, because the critical path is from the control signals to the output. Any additional delay in the control signals will add directly to the worst-case delay. The delay from D to Y in Figure (b) is only 50 ps, compared with the delay from S to Y of 125 ps.

The best choice depends not only on the critical path through the circuit and the input arrival times but also on the power, cost, and availability of parts.

Exercise 3 – Determine the propagation delay and contamination delay of the circuit in the following figure. Use the gate delays given in Table.



Gate	tpd(ps)	tcd(ps)
NOT	15	10
2-input-NAND	20	15
2-input-NOR	30	25
3-input-NAND	30	25
3-input-NOR	45	35
2-input-AND	30	25
2-input-OR	40	30

Solution:

Start finding the critical path and the shortest path through the circuit.

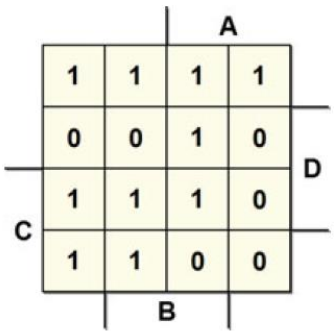
In the critical path tpd is the sum of the propagation delays from A to Y passing for 6 gates, so tpd is 150 ps.

The shortest path are only two gates in the shortest path from A to Y, so tcd is 65 ps.

Exercise 4 –

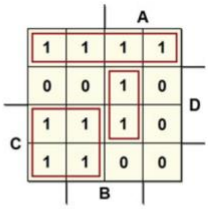
Derive the minimal synthesis from the following map:

(a) Ignoring the hazards;
(b) Eliminating the hazards.

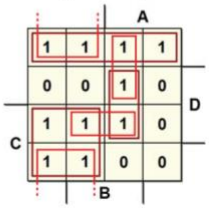


Synthesis of a function considering the hazards issue:

a) With hazards:
$\overline{C}\,\overline{D} + \overline{A}\,C + A\,B\,D$:

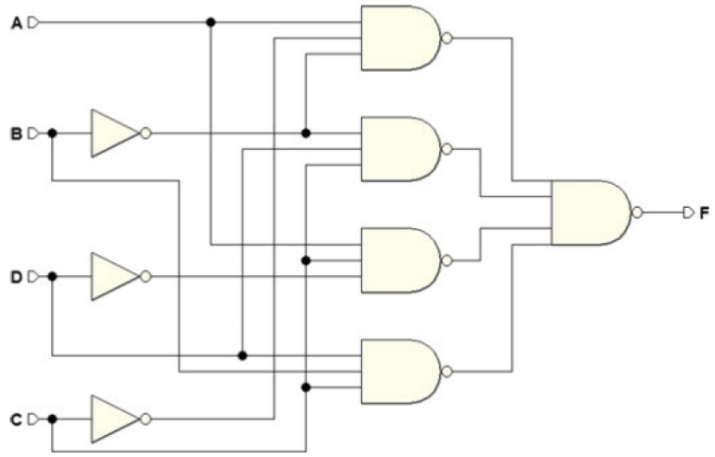


b) With hazards "*covered*":
$\overline{C}\,\overline{D} + \overline{A}\,C + A\,B\,D +$
$\overline{A}\,\overline{D} + B\,C\,D + A\,B\,\overline{C}$:



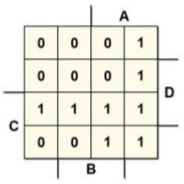
Exercise 5 –

Identify the hazards in the circuit and eliminate them.

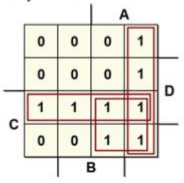


Keeping NAND-NAND network equivalence in mind, we derive the expression of the AND-OR network, and from this, we get the map.

$$F = A\,\overline{B}\,\overline{C} + \overline{B}\,C\,D + A\,C\,\overline{D} + B\,C\,D$$

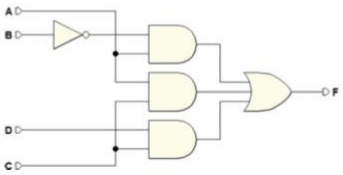


We group the map for minimal synthesis.



On the map, all the adjacent 1s are masked, so the minimal synthesis is already free of hazards. See its expression and the logical network below.

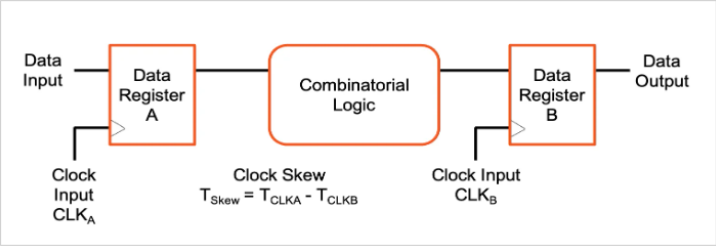
$$F = A\,\overline{B} + C\,D + A\,C$$

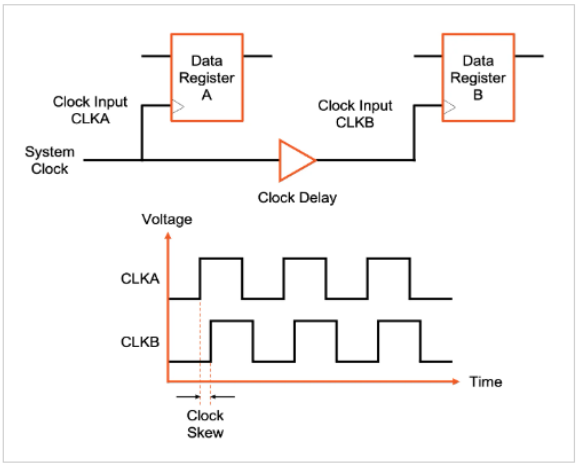


Exercise 6 –A gate has propagation and contamination delays of 0.61 ns and 0.30 ns, respectively. It also contains flip-flops with propagation and contamination delays of 0.72 and 0.50 ns, and setup and hold times of 0.53 ns and 0 ns, respectively.

(a) If you are building a system that needs to run at 40 MHz, how many consecutive gates can you use between two flip-flops? Assume that there is no clock skew and no delay through wires between gates.

(b) Suppose that all paths between flip-flops pass through at least one gate. How much clock skew can the circuit have without violating the hold time?





Solution:

(a) T_c = 1 / 40 MHz = 25 ns

$T_c \geq t_{pcq} + Nt_{CLB} + t_{setup}$

25 ns ≥ [0.72 + N(0.61) + 0.53] ns

Thus, N < 38.9

N = 38

(b)

$t_{skew} < (t_{ccq} + t_{cd\_CLB}) - t_{hold}$

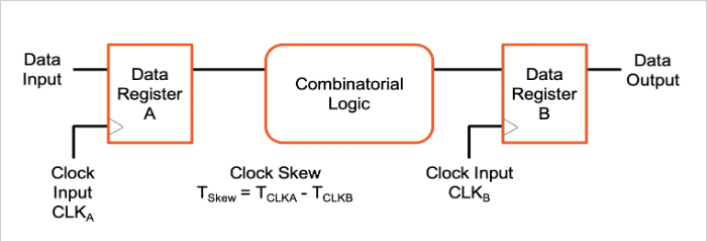
< [(0.5 + 0.3) - 0] ns

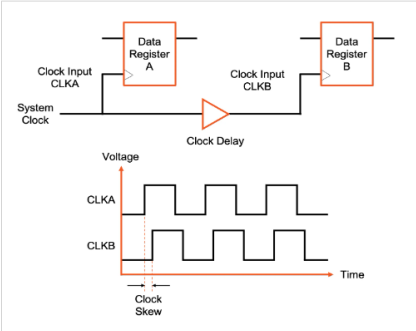
< 0.8 ns = 800 ps

Exercise 7 –A gate has propagation and contamination delays of 0.50 ns and 0.20 ns, respectively. It also contains flip-flops with propagation and contamination delays of 0.80 and 0.40 ns, and setup and hold times of 0.60 ns and 0.10 ns, respectively.

(a) If you are building a system that needs to run at 100 MHz, how many consecutive gates can you use between two flip-flops? Assume that there is no clock skew and no delay through wires between gates.

(b) Suppose that all paths between flip-flops pass through at least one gate. How much clock skew can the circuit have without violating the hold time?





Solution:

(a) T_c = 1 / 100 MHz = 10 ns

$T_c \geq t_{pcq} + Nt_{CLB} + t_{setup}$

10 ns ≥ [0.80 + N(0.50) + 0.60] ns

Thus, N < 17.2

N = 17

(b)

$t_{skew} < (t_{ccq} + t_{cd\_CLB}) - t_{hold}$

< [(0.4 + 0.2) – 0.1] ns

< 0.5 ns = 500 ps

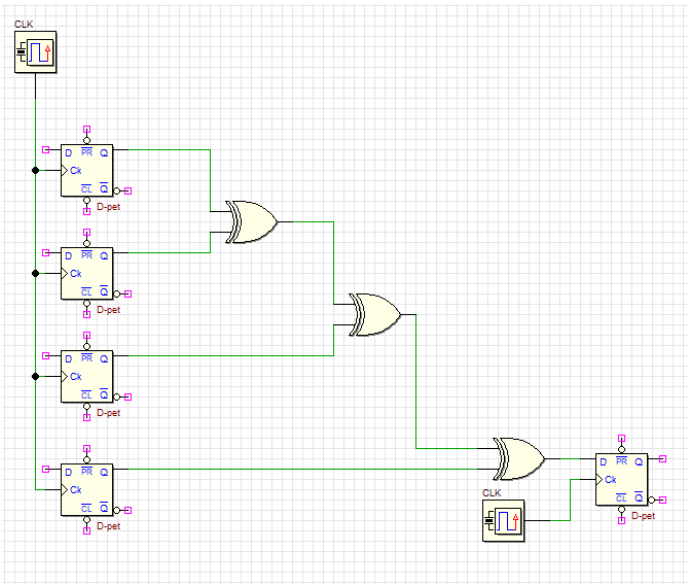
Exercise 8 – For the clocked registered circuit shown in Figure.

a. If there is no clock skew, what is the maximum operating frequency of the circuit?

b. Does the circuit meet the register hold time constraint?

c. How much clock skew can the circuit tolerate before it might experience a hold time violation?

Each XOR gate has a propagation delay of 100ps and a contamination delay of 55ps. Each flip-flop has a setup time of 60ps, a hold time of 20ps, a clock-to-Q maximum delay of 70ps, and a clock-to-Q minimum delay of 50ps.



Solution:

(a)

$Tc \geq t_{pcq} + 3*t_{CLB} + t_{setup}$

Longest path:

$Tc \geq [70 + 3*(100) + 60]$ ps

$Tc \geq 430$ ps

Thus, $F <= 1 / Tc$

$F <= 2.3Ghz$

(b)

$t_{skew} <= (t_{ccq} + t_{cd\_XOR}) - t_{hold}$

$0 < [(50 + 55) – 20]$ ps

$0 <= 85$ ps

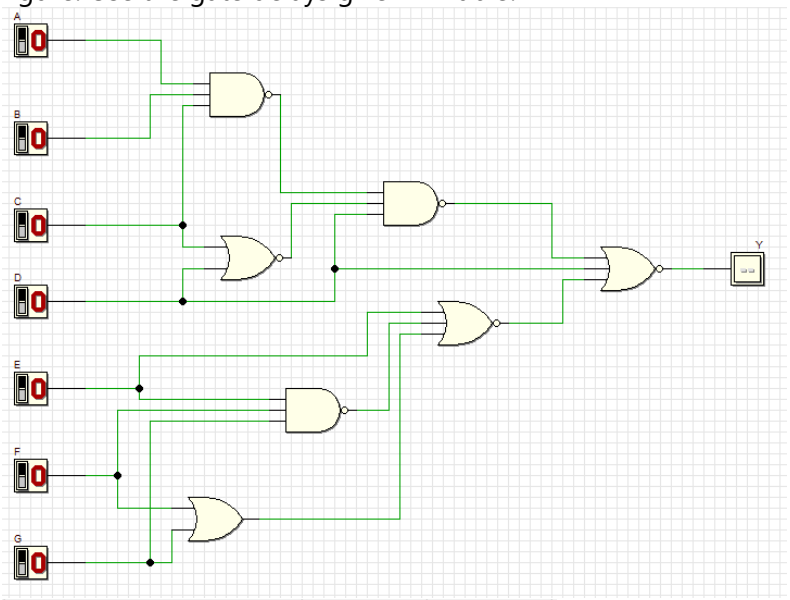
It meets the register hold time constraint.

(c)

Same as b

$t_{skew} <= $**85 ps**

Exercise 9 – Determine the propagation delay and contamination delay of the circuit in the following figure. Use the gate delays given in Table.



Gate	tpd(ps)	tcd(ps)
NOT	15	10
2-input-NAND	20	15
2-input-NOR	30	25
3-input-NAND	30	25
3-input-NOR	45	35
2-input-AND	30	25
2-input-OR	40	30

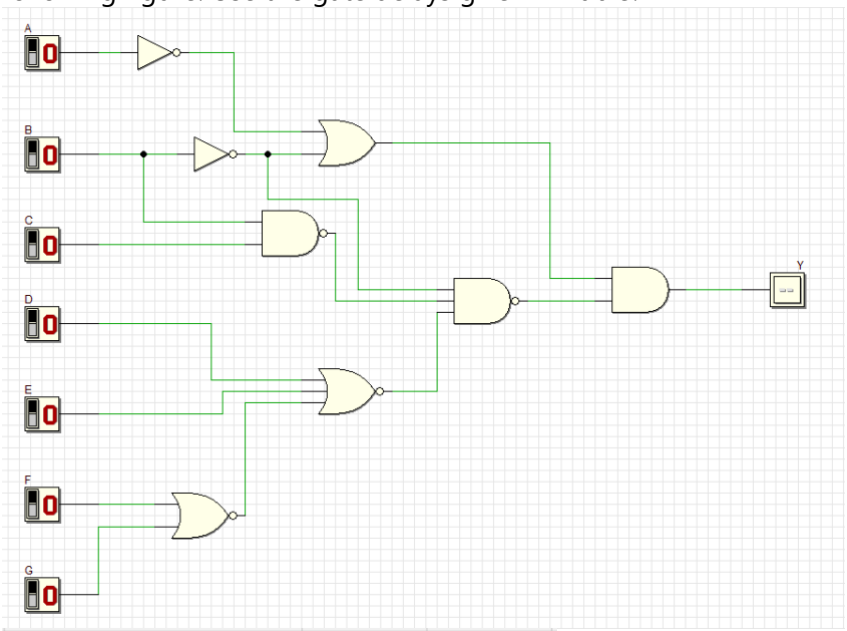
Solution:

Start finding the critical path and the shortest path through the circuit.

In the critical path tpd is the sum of the propagation delays from G to Y passing for 3 gates, so tpd is 130 ps.

The shortest path are only two gates in the shortest path from E to Y, so tcd is 70 ps.

Exercise 10 – Determine the propagation delay and contamination delay of the circuit in the following figure. Use the gate delays given in Table.



Gate	tpd(ps)	tcd(ps)
NOT	15	10
2-input-NAND	20	15
2-input-NOR	30	25
3-input-NAND	30	25
3-input-NOR	45	35
2-input-AND	30	25
2-input-OR	40	30

Solution:

Start finding the critical path and the shortest path through the circuit.

In the critical path tpd is the sum of the propagation delays from G to Y passing for 4 gates, so tpd is 135 ps.

The shortest path are only 3 gates in the shortest path from B to Y, so tcd is 60 ps.

Exercise 11 – You would like to build a synchronizer that can receive asynchronous inputs with an MTBF (mean time between failures) of 50 years. Your system is running at 1 GHz, and you use sampling flip-flops with τ = 100 ps, T0 = 110 ps, and tsetup = 70 ps. The synchronizer receives a new asynchronous input on average 0.5 times per second (i.e., once every 2 seconds). What is the required probability of failure to satisfy this MTBF? How many clock cycles would you have to wait before reading the sampled input signal to give that probability of error?

Solution:

P(failure)/sec = 1/MTBF = 1/(50 years * 3.15 x 10^7 sec/year) = **6.34×10^{-10}**

P(failure)/sec waiting for one clock cycle: $N*(T0/Tc)*e^{-(Tc-tsetup)/Tau}$

= 0.5 * (110/1000) * $e^{-(1000-70)/100}$ = 5.0 x 10^{-6}

P(failure)/sec waiting for two clock cycles: $N*(T0/Tc)*[e^{-(Tc-tsetup)/Tau}]^2$

= 0.5 * (110/1000) * $[e^{-(1000-70)/100}]^2$ = 4.6 x 10^{-10}

This is just less than the required probability of failure (6.34 x 10^{-10}).

Thus, **2 cycles** of waiting is just adequate to meet the MTBF.