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## **Solutions 03 - Logic Gates and Circuits**

Prof. Riccardo Berta

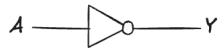
2025-09-15

**0.0.1 Logic gates and circuits Exercises**

**Exercise 1** – Complete the truth tables of the following gates and use the DEEDS simulator to verify their correctness:

(a) NOT, AND, NAND

**NOT**



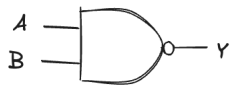
A	Y
0	1
1	0

**AND**



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

**NAND**



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(b) OR, NOR, XOR

**OR**



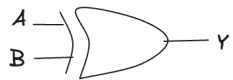
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

**NOR**



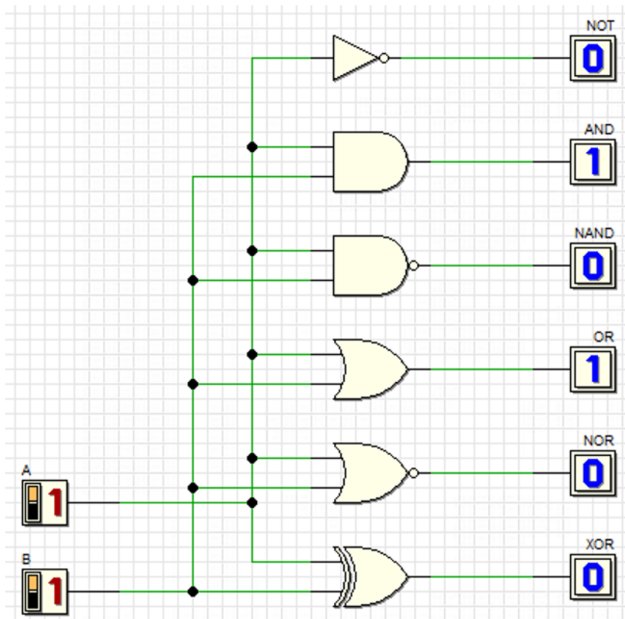
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

**XOR**



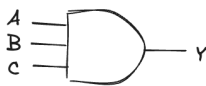
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(c) DEEDS simulation

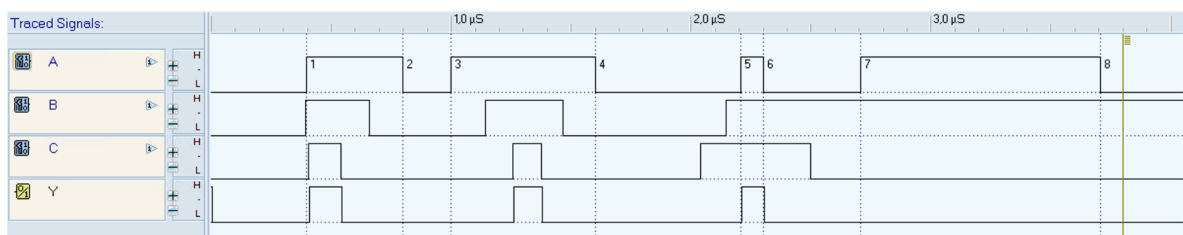


**Exercise 2** - Complete the truth table and the timing diagram of the following 3-inputs digital circuits, and use the DEEDS simulator to verify their correctness:

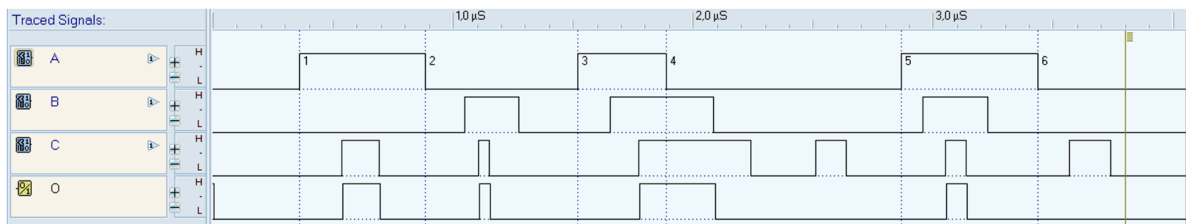
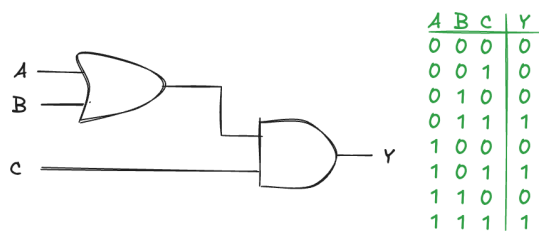
(a)



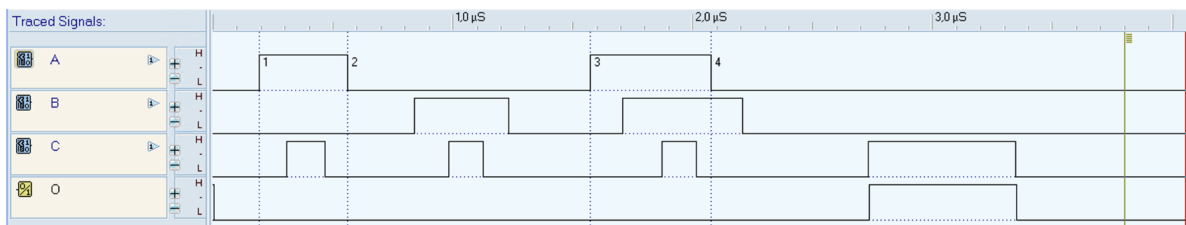
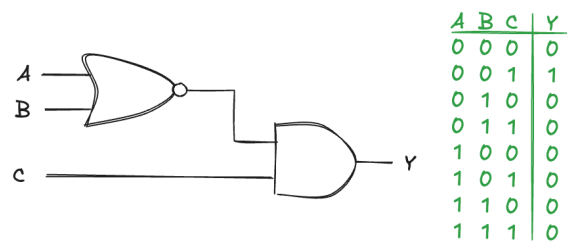
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



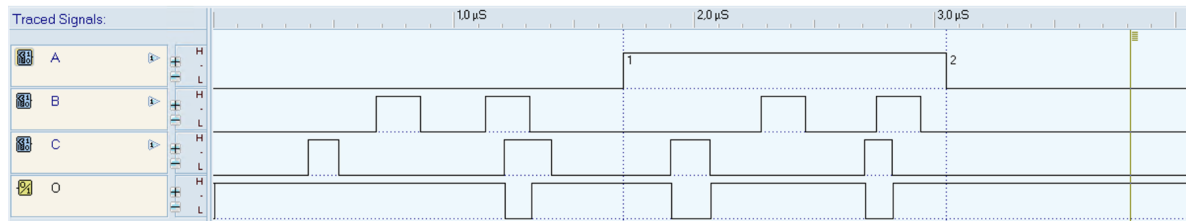
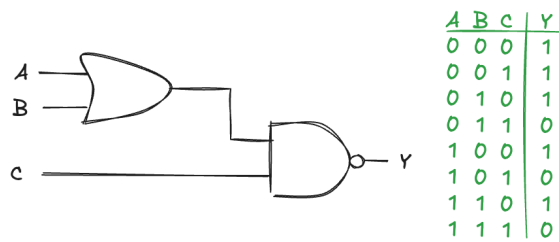
(b)



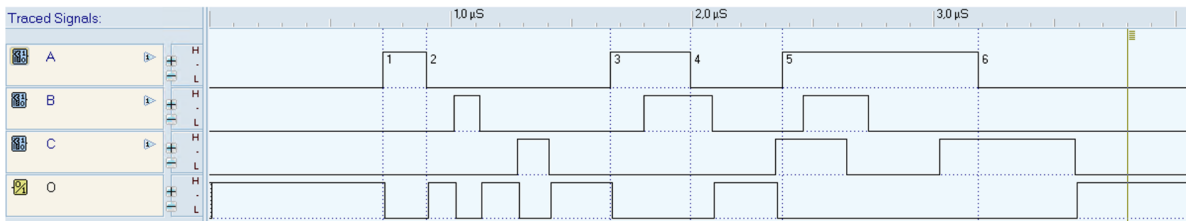
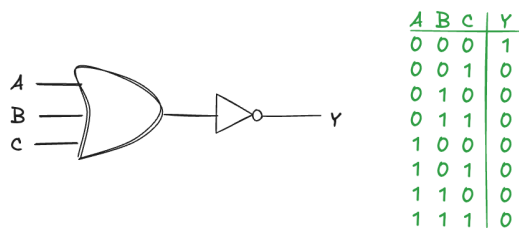
(c)



(d)

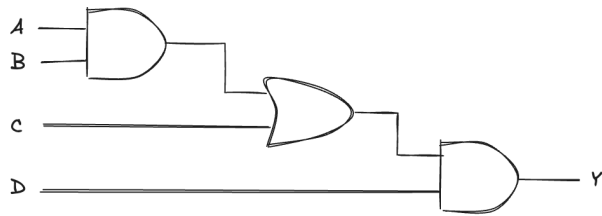


(e)

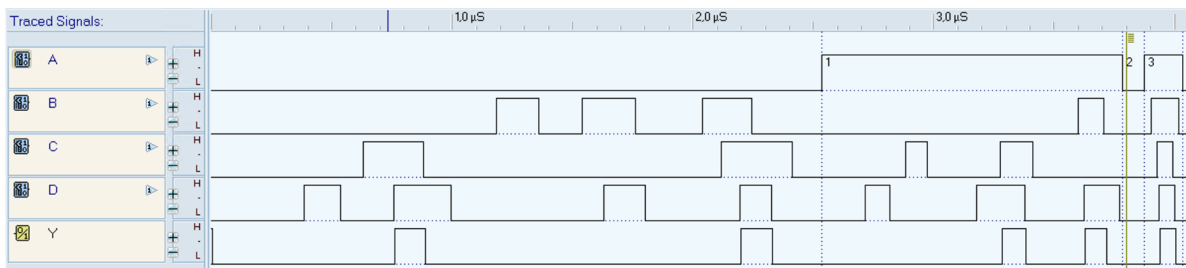


**Exercise 3** - Complete the truth table and the timing diagram of the following 4-inputs digital circuits, and use the DEEDS simulator to verify their correctness:

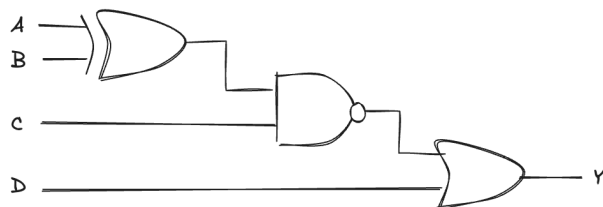
(a)



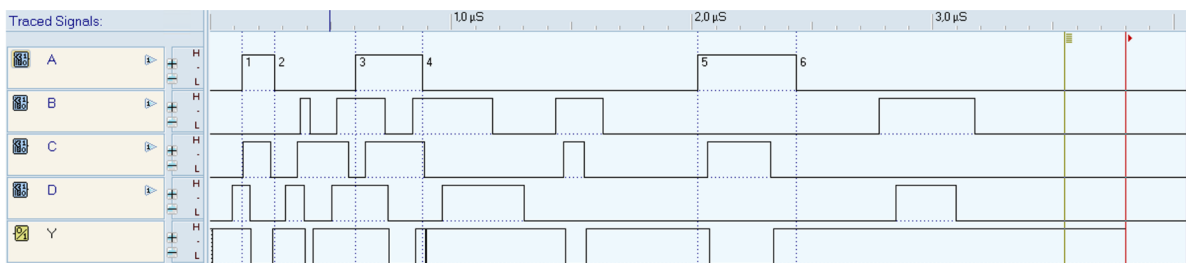
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1



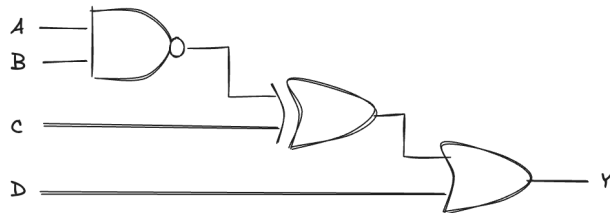
(b)



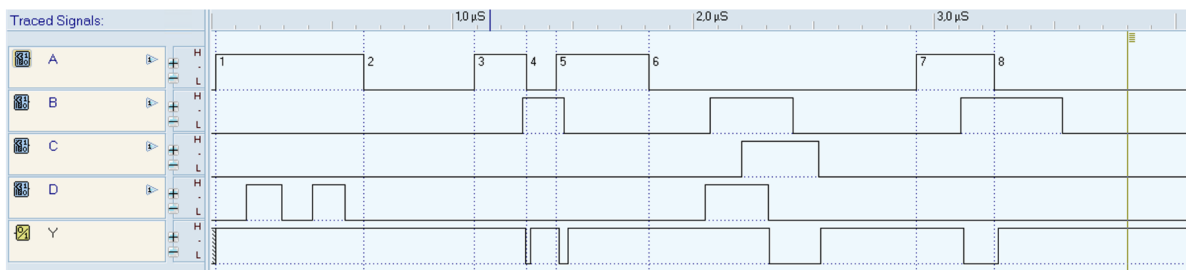
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



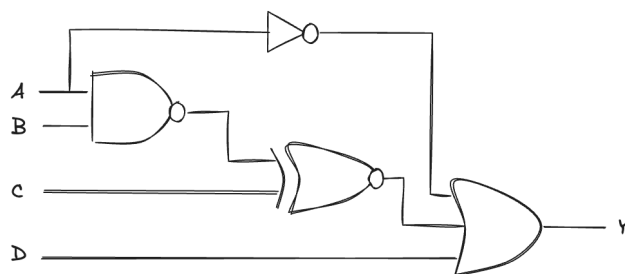
(c)



A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



(d)



A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

