ESD - Elettronica dei Sistemi Digitali

Exercises on Graphical Minimization Methods

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1 Graphical minimization methods Exercises

1.1 Exercise 1

Design the following circuits by proceeding through these steps: define the truth table based on the textual description, construct the corresponding Karnaugh map, minimize the Boolean function, draw the circuit schematic, and finally verify the correctness of the truth table using Deeds.

1.1.1 (a) Majority Detector

Design a circuit with three inputs A, B, C and one output Y, which is 1 whenever at least two inputs are 1.

1.1.2 (b) Odd Parity Detector

Design a circuit with three inputs A, B, C and output Y = 1 if the number of 1s is odd

1.1.3 (c) Code Detector

Design a circuit with three inputs A, B, C. The output Y = 1 only when the input pattern is 101.

1.1.4 (d) Greater Than 9

Design a circuit that takes a 4-bit input A3 A2 A1 A0 and outputs Y=1 if the unsigned decimal number represented by the binary input is greater than 9 (decimal 10–15).

1.1.5 (e) 2-bit Comparator

Design a circuit with two 2-bit binary numbers A1 A0 and B1 B0. The output Y = 1 if the unsigned decimal number represented by A is greater than the unsigned decimal number represented by B.

1.1.6 (f) Binary-to-Gray Code Converter

Design a circuit that converts a 3-bit binary input (A2 A1 A0) to its Gray code (G2 G1 G0)

1.2 Exercise 2

Simplify the following Boolean expressions using two different approaches: using Boolean algebra theorems and Karnaugh maps.

1.2.1 (a)

$G = ABC + B\overline{C}$

1.2.2 (b)

$H = (A + \overline{B})(B + \overline{C})$

1.2.3 (c)

$Y = BC\overline{D} + CD + A\overline{B}C\overline{D} + \overline{A}\,\overline{B}C$

1.2.4 (d)

$Y = AB + A\overline{B}\,\overline{C}\,\overline{D}$