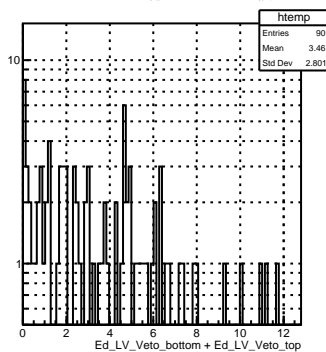
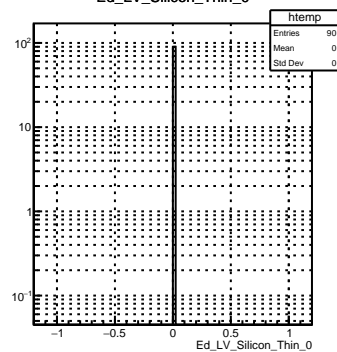


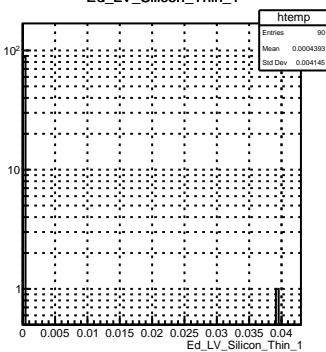
Ed_LV_Veto_bottom + Ed_LV_Veto_top (Ed_LV_Veto_bottom + Ed_LV_Veto_top > 0)



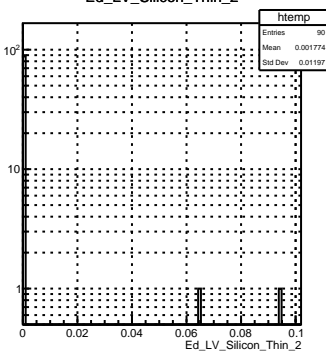
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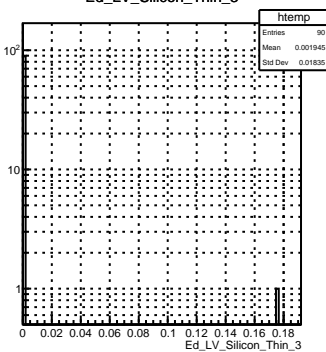
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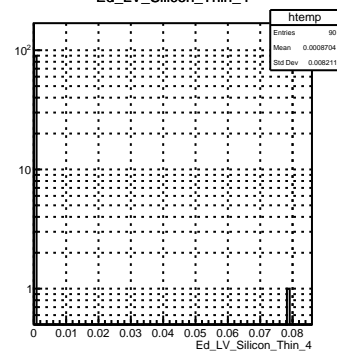
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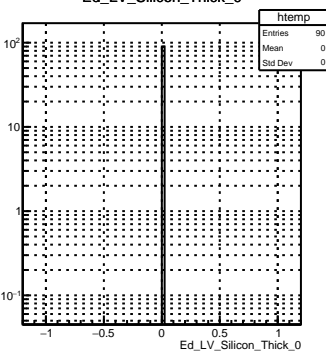
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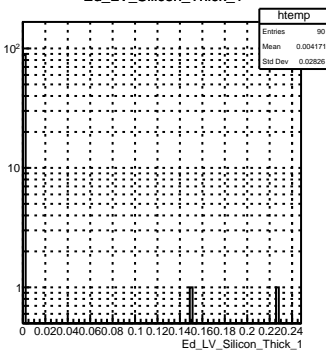
Ed_LV_Silicon_Thin_4



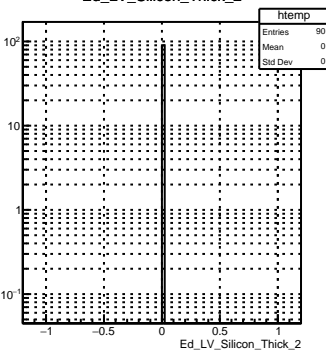
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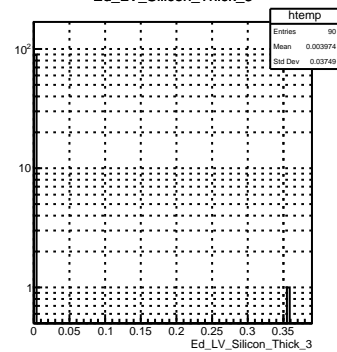
Ed_LV_Silicon_Thick_1



Ed_LV_Silicon_Thick_2



Ed_LV_Silicon_Thick_3



Ed_LV_Silicon_Thick_4

