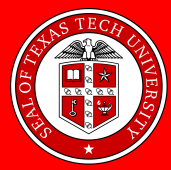


Modeling the MSP430 in Verilog

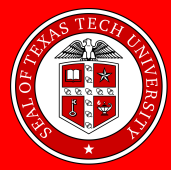
Week 2

Victoria Rodriguez

Texas Tech University

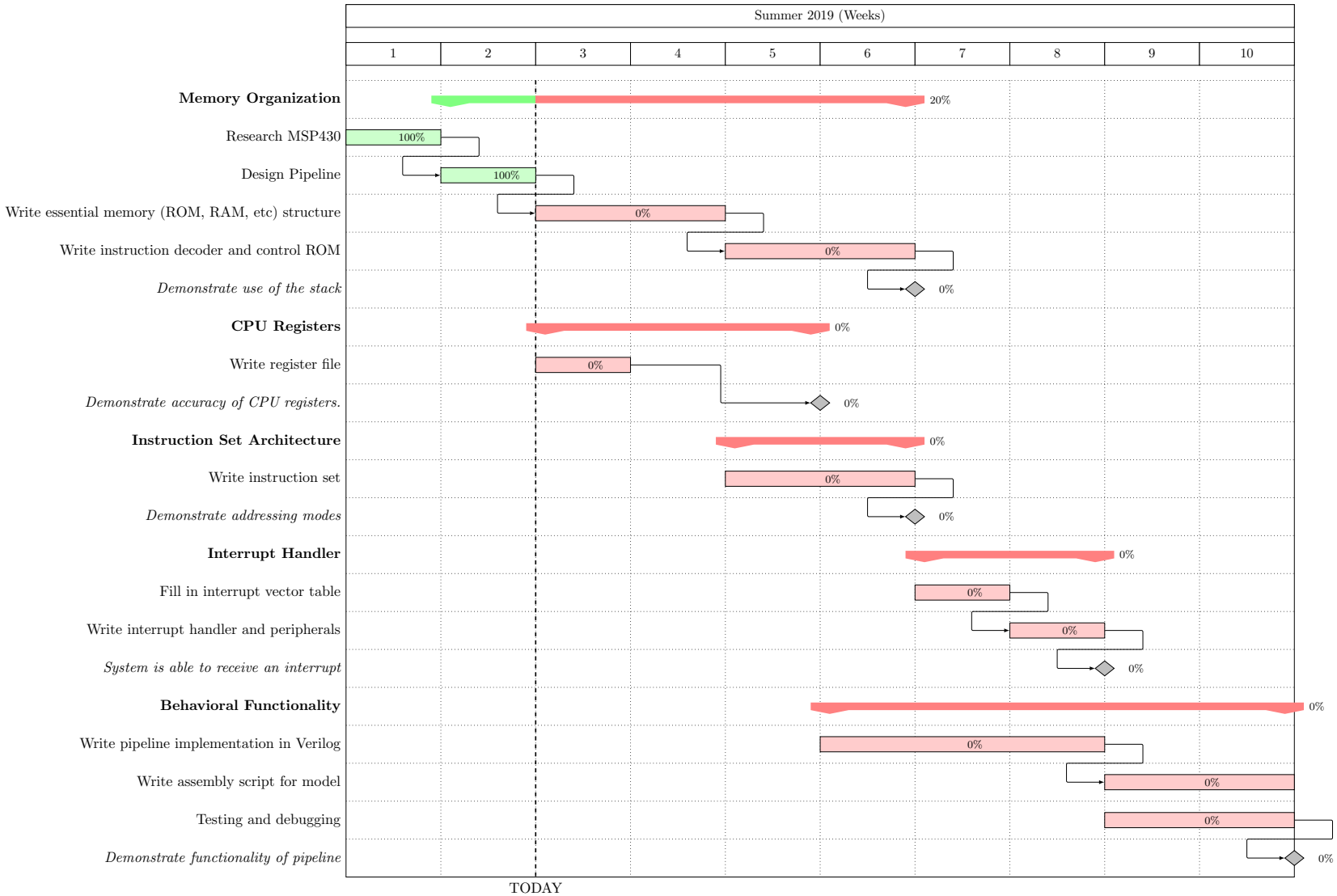
Wednesday 19$^{\text{th}}$ June, 2019

Overview

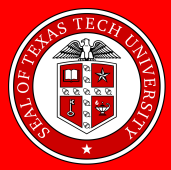


Logistics

Gantt Chart



Last week's deliverable was to design the pipeline.



Designing the Pipeline

MSP430 Instruction Formats

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Double-Operand (Format I)															
Op-code				S-Reg				Ad	B/W	As		D-Reg			
Single-Operand (Format II)															
Op-code									B/W	Ad		D/S-Reg			
Jumps															
Op-code			C				10-bit PC Offset								

[1]

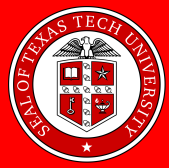
- There doesn't appear to be a way to identify that an instruction is of a certain format, so the instruction decoder will need to identify the instruction in its entirety to correctly categorize it to the correct format
- Ad/As identify addressing modes, and there's only 1 bit for dst [1]

Addressing Modes

As/Ad	Addressing Mode	Syntax	Description
00/0	Register mode	Rn	Register contents are operand
01/1	Indexed mode	X(Rn)	(Rn + X) points to operand. X is stored in next word.
	Symbolic mode	ADDR	(PC + X) points to operand. X is stored in next word.
	Absolute mode	&ADDR	(SR + X) points to operand. X is stored in next word.
10/-	Indirect register mode	@Rn	Rn points to operand
11/-	Indirect autoincrement	@Rn+	Rn points to operand and is incremented by 1 for .B and 2 for .W
	Immediate mode	#N	N is stored in next word. @PC+ is used.

[1]

Instruction Cycle Lengths



Src	Dst	Cycles
Rn	Rm	1
	PC	2
	x(Rm)	4
	EDE	4
	&EDE	4

[1]

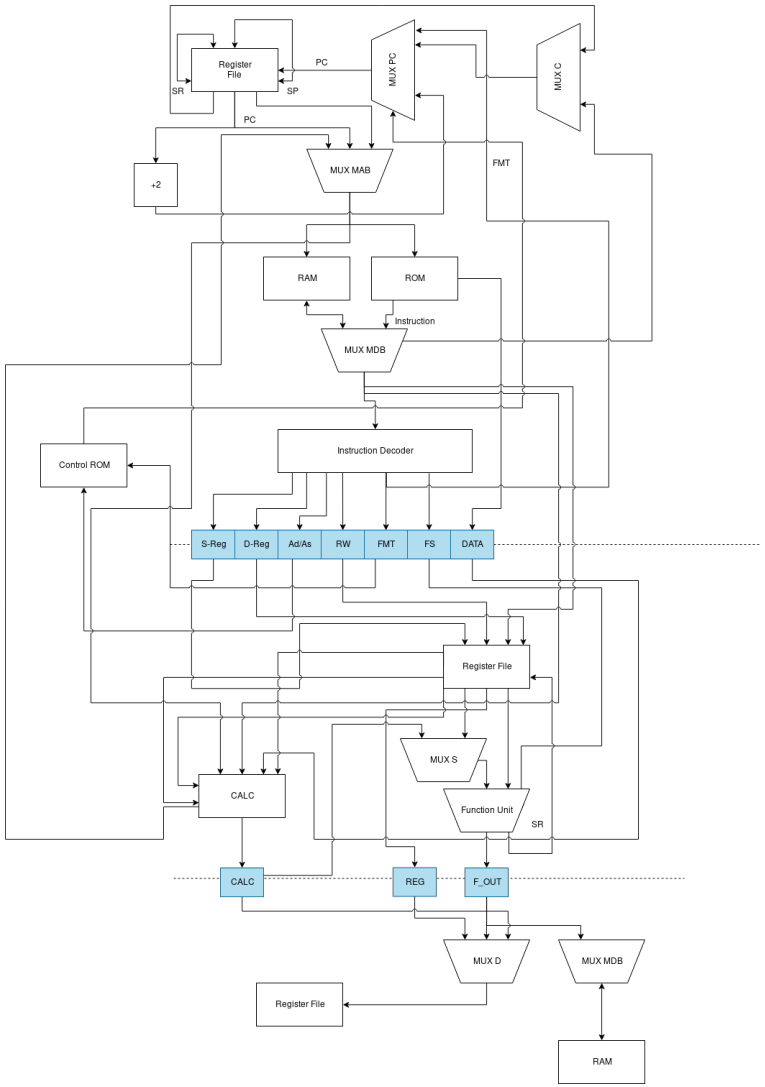
- Single cycle register-to-register instructions
- Accessing memory requires more clock cycles

Relation to Pipeline

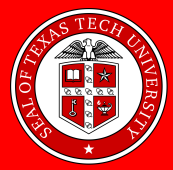
Crossing Guard Program — City of Cuyahoga Falls

- Addressing modes require access to memory
- Address into memory is not necessarily from the instruction itself
- Control ROM is needed to direct flow of traffic

Pipeline

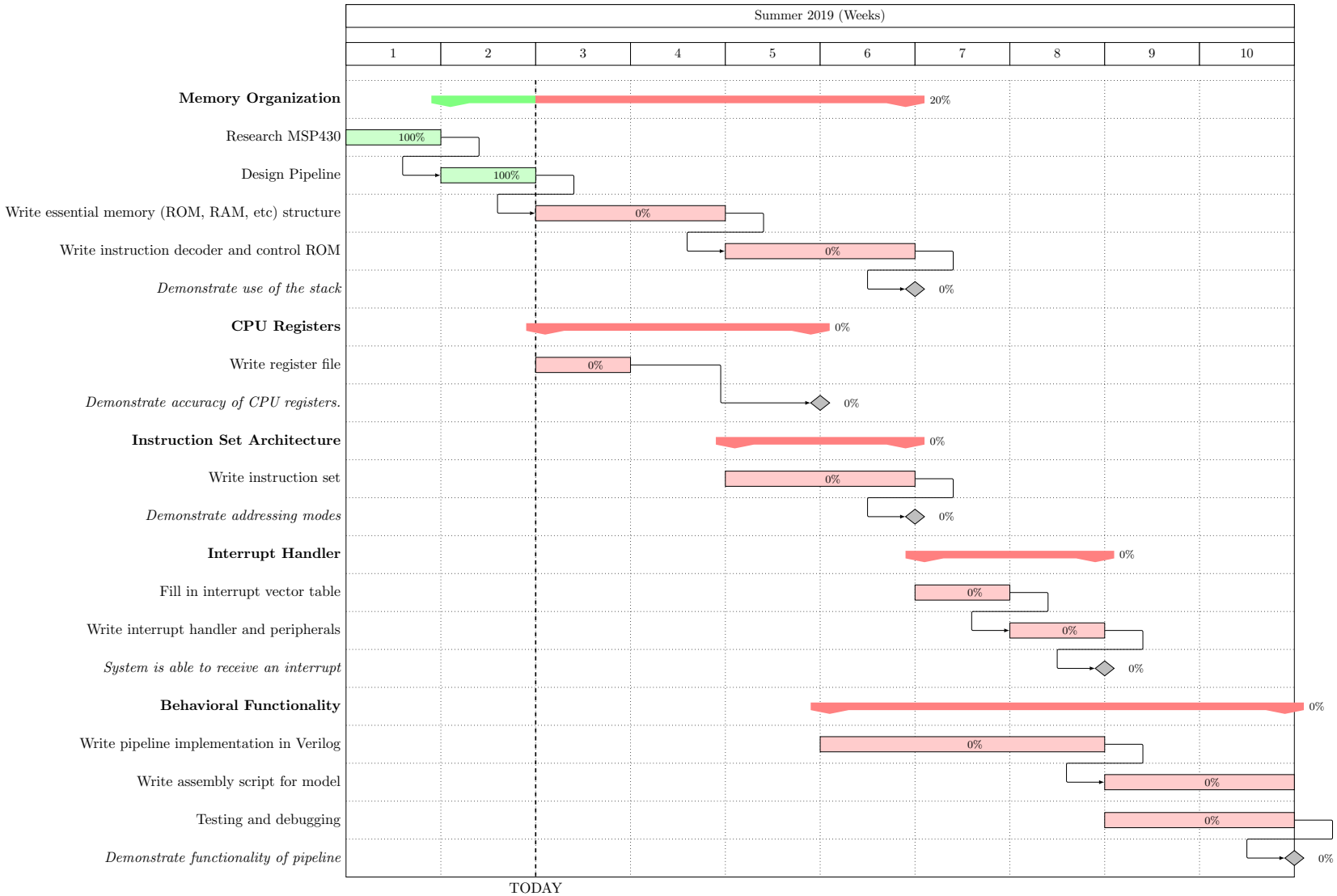

Register File
SR
SP
PC
PC
MUX PC
MUX C
+2
MUX MAB
FMT
RAM
ROM
Instruction
MUX MDB
Instruction Decoder
Control ROM
S-Reg
D-Reg
Ad/As
RW
FMT
FS
DATA
Register File
MUX S
CALC
Function Unit
SR
CALC
REG
F_OUT
MUX D
MUX MDB
Register File
RAM

Pipeline Concerns



- Memory is receiving inputs from different stages of pipeline and needs to keep track of this
- Instructions should generally match cycle length as described in TI's family guide

Next Week's Deliverable(s)



Next week's deliverable is to write the register file and begin writing the essential memory structure.

Review

1. Logistics
   - Gantt Chart
2. Designing the Pipeline
   - Pipeline Considerations
   - Instruction Cycle Lengths
   - Reverse Engineered Draft Pipeline

References

 *MSP430x2xx Family User's Guide*, Texas Instruments.