Application Note

DP83867 Troubleshooting Guide

Evan Mayhew, Patrick O'Farrell, Hillman Lin

Table of Contents

1 Introduction......2
2 Troubleshooting the Application......3
  2.1 Read and Check Register Values for Basic Health Check......3
  2.2 Schematic and Layout Checklist......4
  2.3 Component Checklist......4
  2.4 Peripheral Pin Checks......5
  2.5 Link Quality Check......10
  2.6 Built-in Self Test With Various Loopback Modes......11
  2.7 Debugging MAC Interface......14
3 Application Specific Debugs......18
  3.1 Improving Link-up Margins for Short Cables......18
  3.2 Improving Link Margins across Different Channels......19
  3.3 Link up in 100Mbps Full Duplex Force Mode......19
  3.4 Unstable Link Up Debug in 1Gbps communication......19
  3.5 DP83867PHY and DP83867PHY Cannot Link Up in 1Gbps......20
  3.6 Compliance Debug......21
  3.7 EMC Debug......22
  3.8 Tools and References......23
4 Conclusion......25
5 References......25
6 Revision History......25

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The DP83867 is a robust, low power, fully featured Physical Layer transceiver with integrated PMD sublayers to support the 10BASE-Te, 100BASE-TX, and 1000BASE-T Ethernet protocols.

Figure 1-1 is a high-level system block diagram of a typical DP83867 application.

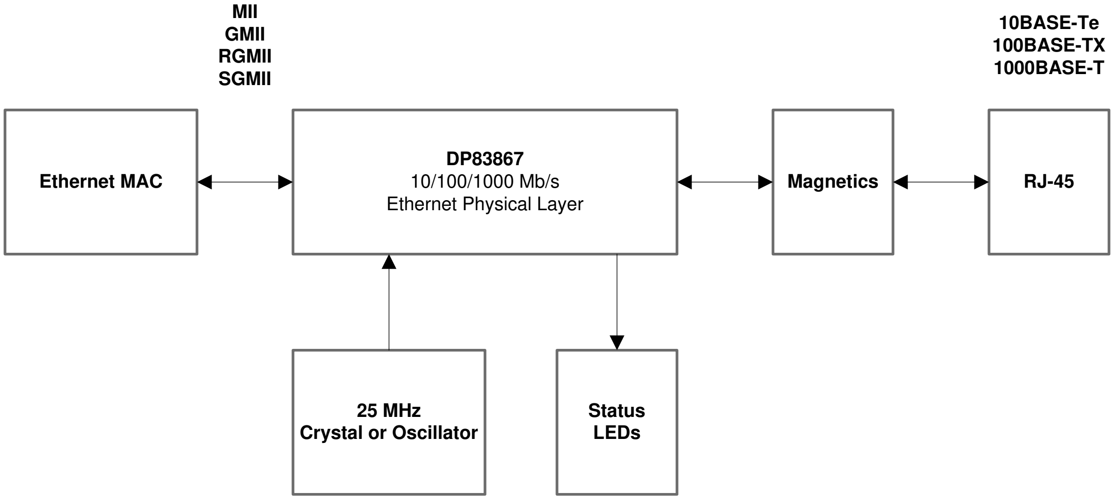

MII
GMII
RGMII
SGMII
10BASE-Te
100BASE-TX
1000BASE-T
Ethernet MAC
DP83867
10/100/1000 Mb/s
Ethernet Physical Layer
Magnetics
RJ-45
25 MHz
Crystal or Oscillator
Status
LEDs

Figure 1-1. DP83867 Block Diagram

The DP83867 can connect to an Ethernet MAC and to a media. The connection to the media is via a transformer and a connector.

Table 1-1. DP83867 Configurations

DP83867 Version	MAC interface	Pin number/ package
DP83867IR/CR	RGMII	48 pins / QFN package
DP83867IS/CS/DP83867E	SGMII	48 pins/ QFNpackage
DP83867IRPAPR	MII/GMII/RGMII	64 pins / QFP package

Note

This Debug application note mainly focuses on RGMII and SGMII interface debug

2 Troubleshooting the Application

The following sections approach the debug from a high level, attempting to start with application characteristics that have a broad impact and then zeroing in on more focused aspects of the design.

2.1 Read and Check Register Values for Basic Health Check

Read the registers and verify the default values shown in the data sheet. Note that the initial values of some registers can vary based on strap options.

The expected register values for PHY operation and link in 1000 Mbps with auto-negotiation enabled are shown in Table 2-1.

Table 2-1. DP83867 Register Value References

Register Address (h)	Register Value (h)	Comments
0x0000	0x1140	MII loopback; Auto-negotiation enable and disable
0x0001	0x769D	Link Status
0x0003	0xA231	PHY revision
0x0004 (1)	0x0061	DUT 10/100Mbps advertisement
0x0005 (2)	0xC1E1	LP 10/100Mbps advertisement
0x0009	0x0300	Compliance test mode; DUT 1000Base speed advertisement
0x000A	0x3C00	LP 1000Base speed advertisement
0x0010	0x5048	Enable SGMII; Enable Power-Saving Mode; Manual MDI or MDIX configuration
0x0011	0xBF02	PHY Status
0x0012	0x0000	Interrupt status
0x0013	0x1C42	Interrupt status 2
0x0014	0x29C7	Enable Speed optimization
0x0015	0x0000	RX_ER counter
0x0016	0x0000	Enable PRBS generator and checker; Enable Loopback
0x0017	0x0040	PRBS status
0x0018	0x6150	LED configuration
0x0019	0x4444	LED configuration 2
0x001E	0x0002	TDR register; Enable Auto-MDIX
0x006E (3)	Based on strap resistors	Strap status register
0x006F (3)	Based on strap resistors	Strap status register2

With the PHY linked in a given speed, use these values as a reference to identify any variance from the expected operation.

Example: After powering and linking the PHY in 10 Mbps, register 0x0001 is read at hex value 7969. Noting the difference in this value from the expected value of 796D, the equivalent binary values are used to identify which bits are distinct. In this case, bit[2] is low, while the expected value is high. Referencing the data sheet register map, bit[2] of register 0x0001 corresponds to link status. From this, it is known that the PHY is not linked.

Repeating this process for any values distinct from the expected values shown in Table 2-1 help diagnose the exact state of the PHY for any encountered issues.

For information about reading and writing registers using the USB-2-MDIO interface, refer to the Section 3.8.

2.2 Schematic and Layout Checklist

Reference and verify all of the noted schematic and layout recommendations in the following spreadsheet:

DP83867 Schematic Checklist

DP83867 Layout Checklist

2.3 Component Checklist

2.3.1 Magnetics

The following guidelines are the main specifications to reference for compatible magnetics:

Table 2-2. Magnetic Isolation Requirements

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turns Ratio	±2% Tolerance	1:1	-
Open Circuit Inductance	-	320 to 350	µH
Insertion Loss	1-100MHz	-1	dB
Return Loss	1-30MHz	-16	dB
	30-60MHz	-12	dB
	60-100MHz	-10	dB
Differential to Common Mode Rejection Ratio	1-50MHz	-30	dB
	50-150MHz	-20	dB
Crosstalk	30MHz	-35	dB
	60MHz	-30	dB
Isolation	HPOT	1500	Vrms

If these exact requirements cannot be met, the following allowances can be made:

- Turns ratio
  - 2% preferred, but 3% is tolerable.
- Inductance
  - High inductance is preferred. Usual numbers seen are around 350µH.
- Insertion loss
  - As close to 0dB as possible compared to specified value for each range stated in data sheet. If specification gives -1dB as typical. finding a component with -1dB, -0.9dB, … is recommended.
- Return loss
  - At or lower than the magnitude specified in data sheet. If specification gives -16dB as typical, finding a component with -16dB, -17dB, … is recommended.

2.3.2 Crystal / Oscillator

The following guidelines are the main specifications to reference for compatible crystals.

Table 2-3. 25-MHz Crystal Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	1 year aging			±50	ppm

If opting for an oscillator:

Table 2-4. 25-MHz Oscillator Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	1 year aging			±50	ppm
Rise / Fall Time	20% - 80%			5	ns
Symmetry	Duty Cycle	40%		60%	
Jitter RMS	Integration Band: 12kHz to 5MHz			11	ps
Input voltage for 25MHz Oscillator		1.5		1.9	Vpp

2.4 Peripheral Pin Checks

The following section details the expected values of various peripheral output pins of the PHY during operation - measure and compare the noted pin outputs to verify PHY operation.

2.4.1 Power Supplies

The power supplies are the first key item to check. Power up the device and perform DC measurement of the supplies as close to the pin as possible. Confirm that each measurement is within the limits defined in the *Recommended Operating Conditions* section of the data sheet.

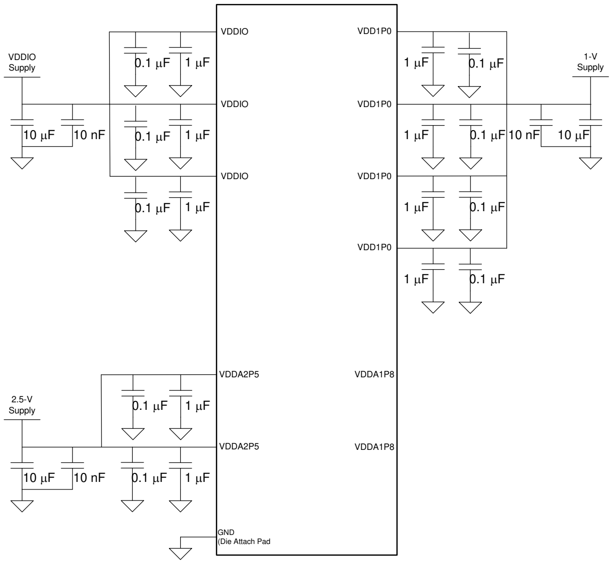

VDDIO Supply
10 µF
10 nF
0.1 µF
1 µF
VDDIO
VDDIO
VDDIO
VDD1P0
VDD1P0
VDD1P0
VDD1P0
1-V Supply
10 nF
10 µF
2.5-V Supply
VDDA2P5
VDDA2P5
VDDA1P8
VDDA1P8
GND
(Die Attach Pad

Figure 2-1. Two Supply Configuration

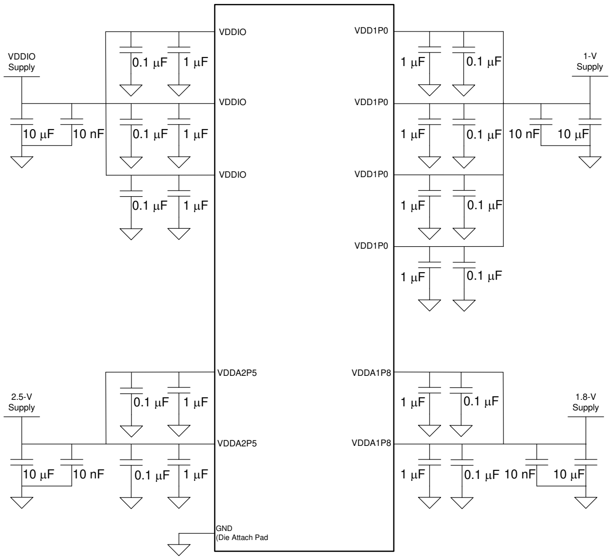

VDDIO Supply
10 µF
10 nF
0.1 µF
1 µF
VDDIO
VDDIO
VDDIO
VDD1P0
VDD1P0
VDD1P0
VDD1P0
1-V Supply
2.5-V Supply
VDDA2P5
VDDA2P5
VDDA1P8
VDDA1P8
1.8-V Supply
GND
(Die Attach Pad

Figure 2-2. Three Supply Configuration

The DP83867 supports two configurations for power supplies as shown in Figure 2-1 and Figure 2-2. DP83867 can operate with as few as two supplies. When operating in the three-supply configuration, the VDDA1P8 supply must be stable within 25ms of the VDDA2P5 supply ramping up. There is no sequencing requirement for other supplies when operating in three supply mode. When powering down the DP83867, the VDDA1P8 supply needs to be brought down before the VDDA2P5 supply. Power up the board and verify the sequence of these supplies with an oscilloscope.

Note

Make sure to supply VDDIO1P8 after VDDA2V5

2.4.2 RBIAS Voltage and Resistance

The RBIAS resistor is used to develop the internal bias currents and voltages in the PHY. It is specified for 1% tolerance so that the PHY can meet the tightest IEEE 802.3 specifications.

Measure the DC value of the voltage across the RBIAS resistor and confirm that the voltage is 1 V.

Power down the board and verify that the RBIAS resistor value is 11 kΩ ±1%.

2.4.3 Probe the XI Clock

Verify the frequency and signal integrity. For link integrity the clock must be 25 MHz ±50 ppm.

If using a crystal as the clock source, probe the CLK_OUT signal. Probing the crystal can change the capacitive loading and therefore change the operational frequency. The default signal on CLK_OUT is a buffered version of the XI reference and will provide a representative measurement.

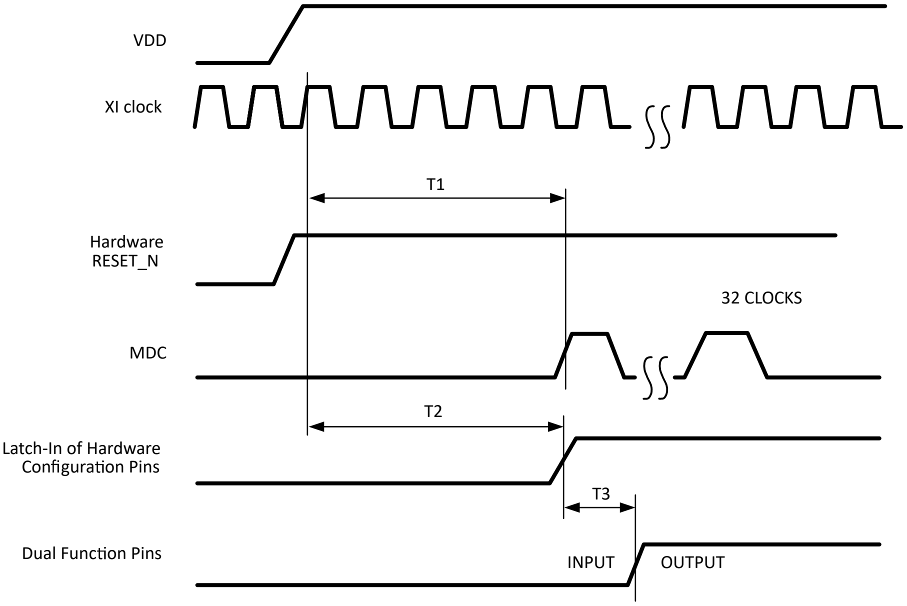
2.4.4 Probe the RESET_N Signal

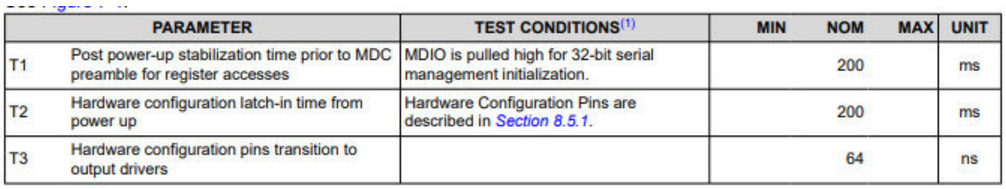
The reset input is active low. It is important to confirm that the controller is not driving the RESET_N signal low. Otherwise, the device will be held in reset and will not respond.

2.4.5 Probe the Strap Pins During Initialization

In some cases, other devices on the board (for example, the MAC) can pull or drive these pins unexpectedly. Confirm that these signals are in the range of the target voltages described in the data sheet. Measurements can be made during power up and after power up when the RESET_N signal is asserted.

Strap Latch-in process occurs during power up process. Latch-in event normally occurs within 200ms after VDD pull up.


VDD
XI clock
T1
Hardware RESET_N
32 CLOCKS
MDC
T2
Latch-In of Hardware Configuration Pins
T3
Dual Function Pins
INPUT
OUTPUT



	PARAMETER	TEST CONDITIONS(1)	MIN	NOM	MAX	UNIT
T1	Post power-up stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32-bit serial management initialization.		200		ms
T2	Hardware configuration latch-in time from power up	Hardware Configuration Pins are described in *Section 8.5.1*.		200		ms
T3	Hardware configuration pins transition to output drivers			64		ns

Figure 2-3. Strap Latch-in Process

For further confirmation, the strap values can be read from the registers. The values are available in register 0x006E (STRAP_STS1) and register 0x006F (STRAP_STS2). Section 3.8.2

2.4.6 Probe the Serial Management Interface Signals (MDC, MDIO)

1. MDIO should pull up to the I/O supply when undriven. Probe MDIO to confirm the default voltage.
2. Confirm processor and PHY have the same VDDIO voltage.
3. MDC should not have any pull up or pull down resistor.
4. Attempt to read the registers. Probe the MDC/MDIO signals during read and write operations, referencing the expected waveforms in the following images.

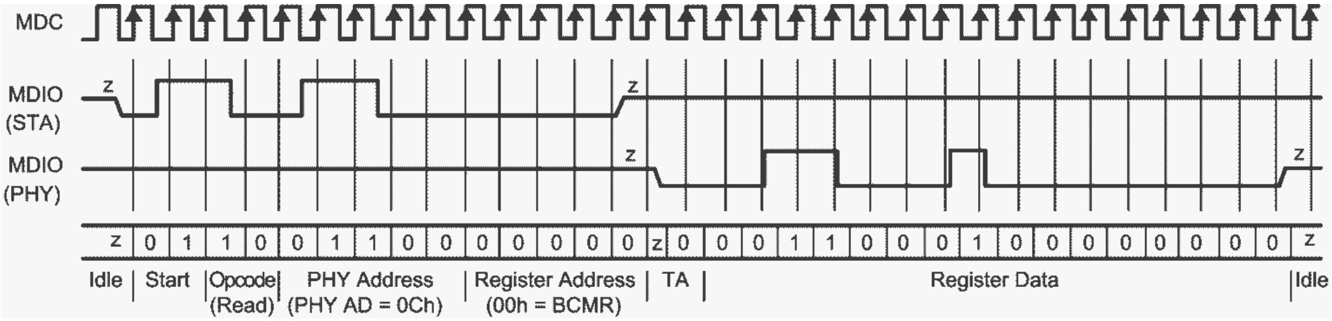

MDC
MDIO (STA)
MDIO (PHY)
z
z 0 1 1 0 0 1 1 0 0 0 0 0 0 0 z 0 0 0 1 1 0 0 0 1 0 0 0 0 0 0 0 0 z
Idle
Start
Opcode (Read)
PHY Address (PHY AD = 0Ch)
Register Address (00h = BCMR)
TA
Register Data
Idle

Figure 2-4. Typical MDC/MDIO Read Operation

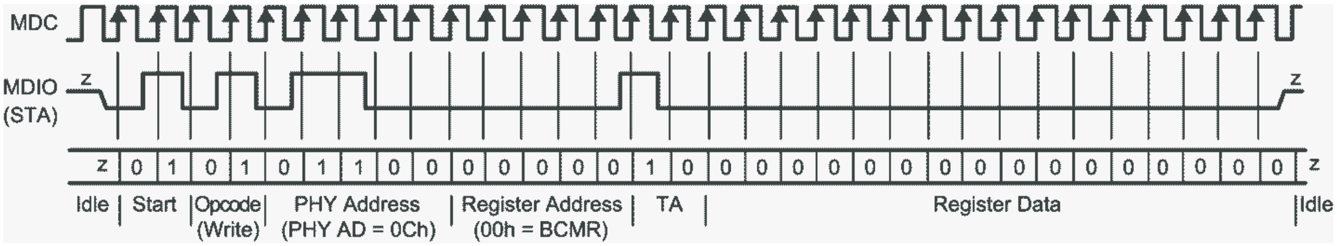

MDC
MDIO (STA)
z
z 0 1 0 1 0 1 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 z
Idle
Start
Opcode (Write)
PHY Address (PHY AD = 0Ch)
Register Address (00h = BCMR)
TA
Register Data
Idle

Figure 2-5. Typical MDC/MDIO Write Operation

Note

Recommend using Logic Analyzer to debug MDIO communication.

2.4.7 Probe the MDI Signals

When Auto-negotiation enable, A link pulse should be visible on the channel A transmit and receive differential pairs (TD_P_A and TD_M_A).

A short Ethernet cable with 100 Ohm terminations can be used for measuring the MDI signals. A terminated cable is shown in Figure 2-6. A connection diagram for making measurements with the terminated cable is shown in Figure 2-7.

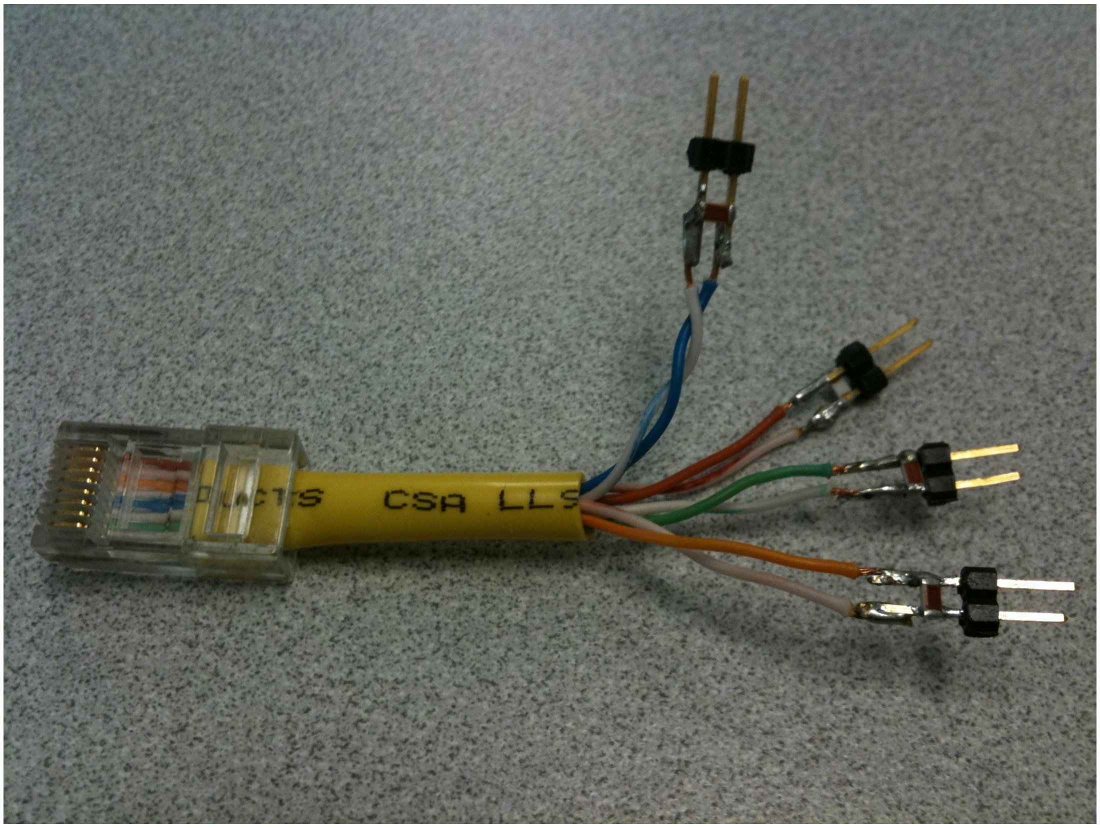


Figure 2-6. 100 Ohm Terminated Cable for MDI Signal Measurement

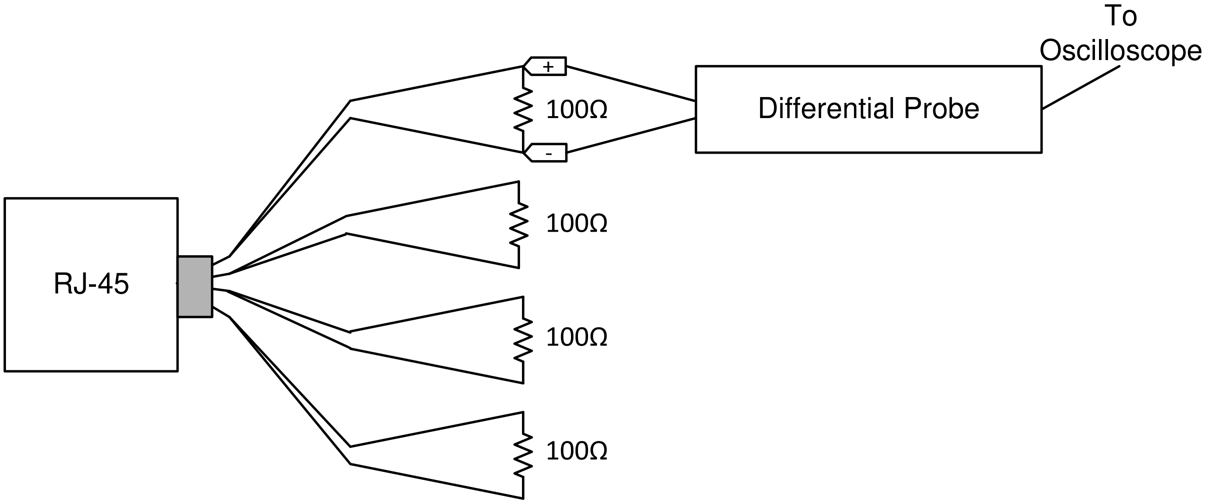


Figure 2-7. Connection Diagram for 100M Terminated Cable

Auto-Negotation link pulses are nominally 100ns wide. Pulses are spaced by 62µs or 125µs and are transmitted in bursts. The bursts are nominally 2ms in duration and occur every 16ms. An example link pulse is shown below in Figure 2-8.

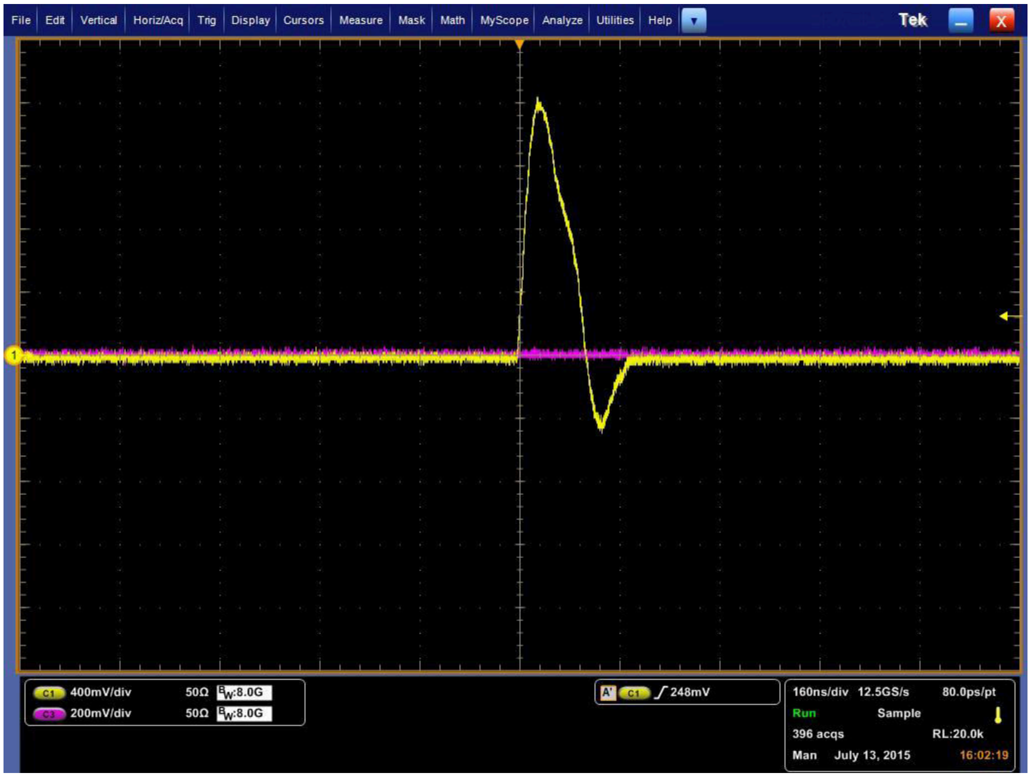

File
Edit
Vertical
Horiz/Acq
Trig
Display
Cursors
Measure
Mask
Math
MyScope
Analyze
Utilities
Help
Tek
1
C1 400mV/div 50Ω BW:8.0G
C3 200mV/div 50Ω BW:8.0G
A' C1 248mV
160ns/div 12.5GS/s 80.0ps/pt
Run Sample
396 acqs RL:20.0k
Man July 13, 2015 16:02:19

Figure 2-8. DP83867 Link Pulse

Observing this pulse confirms the PHY is on and attempting to link.

2.5 Link Quality Check

With the PHY powered and connected to a link partner, the following registers can be read from to determine the health of the link for 1000Mbps and 100Mbps:

Table 2-5. Link Quality MSE Registers for 1000Mbps

Channel	Register Address
A	0x225
B	0x265
C	0x2A5
D	0x2E5

Note

In 100Mbps communication, please refer for channel A for accurate measurement.

In 10Mbps communication, please do not refer to the table for accurate measurement.

For a given channel, read the register value to determine the MSE (Mean Square Error), convert to decimal, and refer to the following table to determine link quality:

Table 2-6. MSE Link Quality Ranges

Link Quality	MSE Range
Excellent	< 522
Good	522 - 827
Poor	> 827

For information on how to read and write registers in the extended register space, please refer to Section 3.8.

2.6 Built-in Self Test With Various Loopback Modes

Loopback feature for debug:

Loopback mode could determine the communication issue occur on MAC < -- > PHY or PHY < -- > PHY. MII loopack, PCS loopback, Digital Loopback, and Analog Loopback could isolate the PHY < -- > PHY communication. Reverse Loopback could isolate the MAC < -- > PHY communication. The following diagrams illustrate the various loopback mode that DP83867 have:

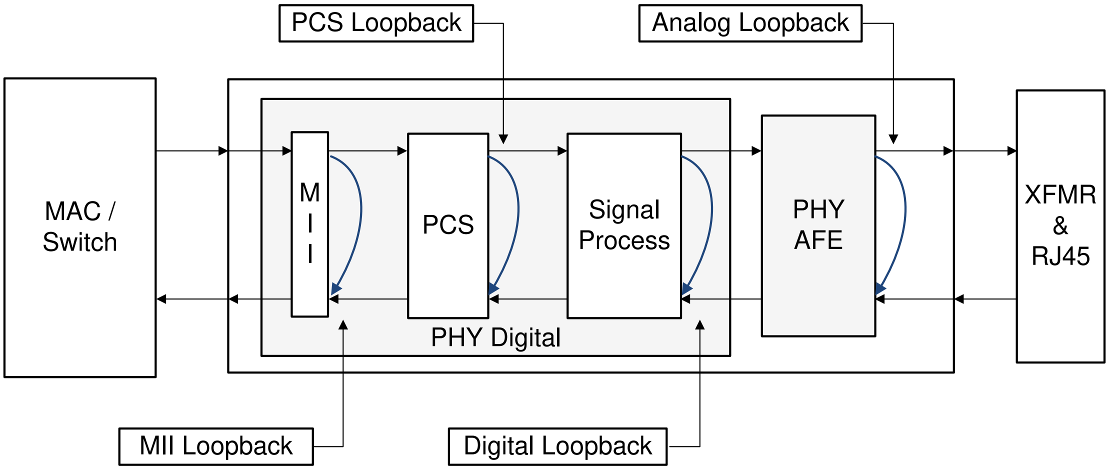

PCS Loopback
Analog Loopback
MAC / Switch
M I I
PCS
Signal Process
PHY AFE
XFMR & RJ45
PHY Digital
MII Loopback
Digital Loopback

Figure 2-9. Block Diagram, Loopback Modes

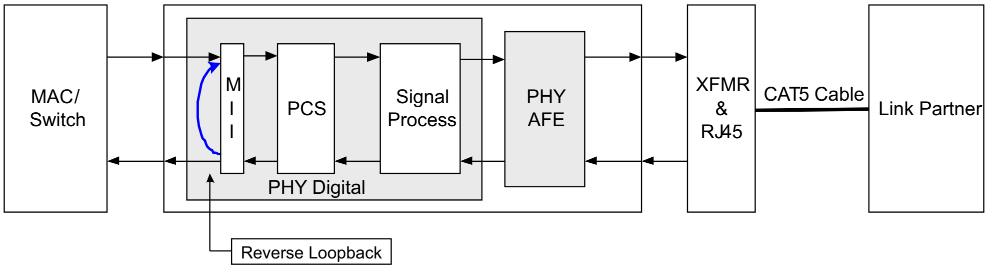

MAC/ Switch
M I I
PCS
Signal Process
PHY AFE
XFMR & RJ45
CAT5 Cable
Link Partner
PHY Digital
Reverse Loopback

Figure 2-10. Block Diagram, Reverse Loopback Mode

Analog loopback is typically used to verify the PHY's full internal data path, while reverse loopback is used with a link partner to verify the data path along the MDI.

Transmitting and Receiving Packets with the MAC:
If generating and checking packets with the MAC is possible, and the PHY has a working link partner with reverse loopback capability, verify the full data path as follows:

1. Power and connect the PHY to the MAC and a working link partner.
2. Enable reverse loopback on the link partner (for DP83867 link partner, write 0x16 to 0020).
3. Transmit test packets from the MAC to the PHY.
4. Verify the MAC receives the same test packets.

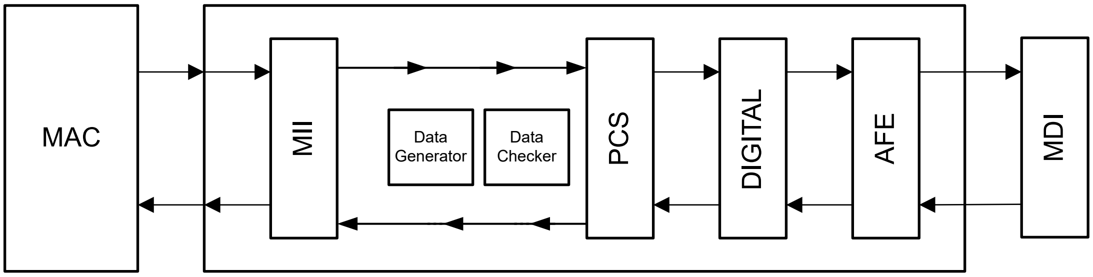
If the MAC receives the same test packets transmitted without issue, the full data path through MAC → PHY → MDI is valid. If this test does not pass, perform analog loopback to isolate the issue along the data path:

1. Power and connect the PHY to the MAC.
2. Enable analog loopback on the PHY (write 0x16 to 0008).
3. Transmit test packets from the MAC to the PHY.
4. Verify the MAC receives the same test packets.

If the MAC receives the same test packets, the data path through MAC → PHY is valid, and the issue has been isolated to the MDI data path. If this test does not pass, the issue could be on the MAC interface or the internal data path. To verify the MAC interface, refer to Debugging MAC Interface. To verify the internal data path, perform PRBS with analog loopback using the following script.

Transmitting and Receiving Packets with BIST:

This device incorporates an internal PRBS Built-in Self Test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be used to test the integrity of the transmit and receive data paths. BIST can be performed using various loopback modes to isolate any issues to specific parts of the data path. The BIST generates packetized data with variable content and IPG.



If generating and checking packets with the MAC is not possible, use PRBS packet generation and checking functionalities to verify the data path. Perform reverse loopback with PRBS and a working link partner as follows:

1. Power and connect the PHY to a link partner.
2. Enable PRBS packet generation on the PHY (write 0x16 to 5000).
3. Enable reverse loopback on the link partner (for DP83867 link partner, write 0x16 to 0020).
4. Wait at least one second, then check PRBS lock status on the PHY (read register 0x17[11:10]).

If register 0x17[11] is high, the data path through PHY → MDI is valid. If this test does not pass, the issue could be on the PHY's internal data path or the MDI. To verify the internal data path, perform PRBS with analog loopback using the following script. If the internal data path is valid, then the issue is isolated to the MDI (assuming the link partner is working).

The following is an example sequence of register reads and writes to perform BIST with analog loopback in 10Mbps:

```
// This is how you make a comment. All scripts must start with 'begin'
begin
// hard reset
001F 8000
// disable auto-neg, force 10Mbps (1)
0000 0100
// enable analog loopback (2)
0016 0008
// force mdi mode for 10/100 Mbps (not relevant for 1000Mbps)
0010 5008
// loopback configuration register required
00FE E720
// enable packet gen, keep analog loopback (3)
0016 5008

// (1)
// for 100Mbps, write 0000 to 2100
// for 1000Mbps, write 0000 to 0140
// (2)
// for digital loopback, write 0016 to 0004
// for PCS loopback, write 0016 to 0003
// (3)
// for packet generation with digital loopback, write 0016 to 5004
// for packet generation with PCS loopback, write 0016 to 5003
end
```

Reference the annotated (1-3) register writes if testing in different loopback modes or speeds. Wait at least one second before the following reads/writes to allow for PRBS to transmit packets.

```
begin
// lock byte count
0072 0201
// check lock status, # of packets received, and # of errors
0017
0071
0072
// enable continuous mode packet counting
0016 D004
// update packet counter with current value (4)
0072 0201
// read packet counter (5)
0071
// soft reset
001F 4000
// Repeat (4) and (5) as desired to verify packet count changing for each counter update
end
```

Register 0x17[11] indicates whether PRBS was able to successfully receive the same transmitted data through the given data path.

2.7 Debugging MAC Interface

2.7.1 RGMII Debug

Reference the waveforms in this section verify the expected MAC data and clock signals for RGMII in shift and align modes. To capture data and clock signals, measure close to the receiver end. Note the following requirements for selecting the correct delay mode:

Table 2-7. Selecting the Correct RGMII Delay Mode

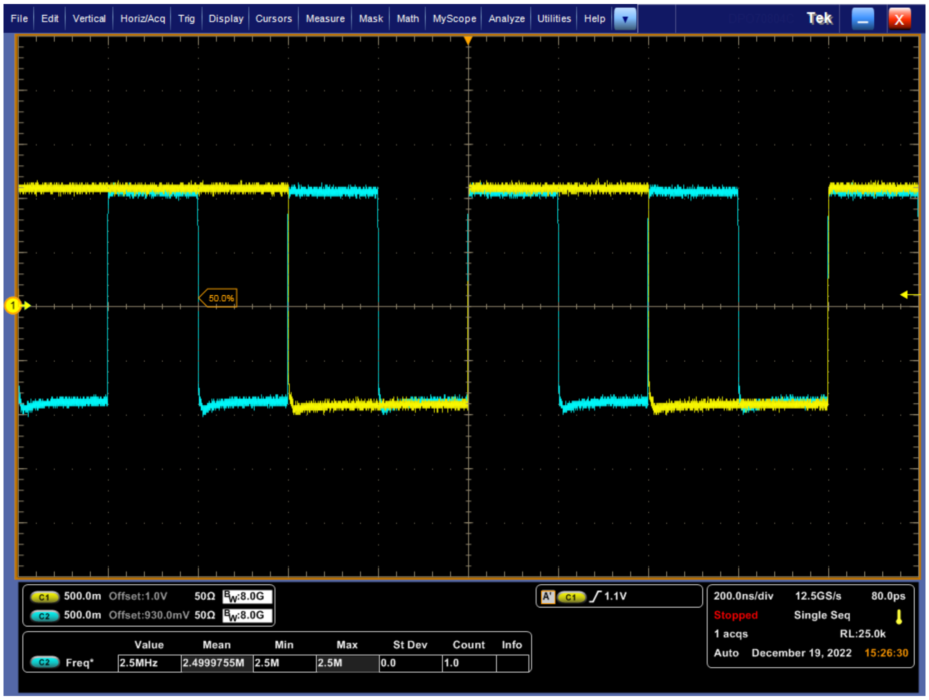
If MAC's Configuration is	Required PHY Configuration
RGMII Align Mode on TX side	RGMII Shift Mode on TX side
RGMII Align Mode on RX side	RGMII Shift Mode on RX side
RGMII Shift Mode on TX side	RGMII Align Mode on TX side
RGMII Shift Mode on RX side	RGMII Align Mode on RX side

Note

In Shift mode, the clock skew can be adjusted using the RGMII Delay Control Register (RGMIIDCTL), address 0x0086.

RX_D[3:0] Data Aligned with RX_CLK

For the PHY set in RX align mode in 10/100Mbps, probe the clock and data signals on the MAC end and compare to the reference waveforms shown below:



C1 500.0m Offset:1.0V 50Ω BW:8.0G
C2 500.0m Offset:930.0mV 50Ω BW:8.0G

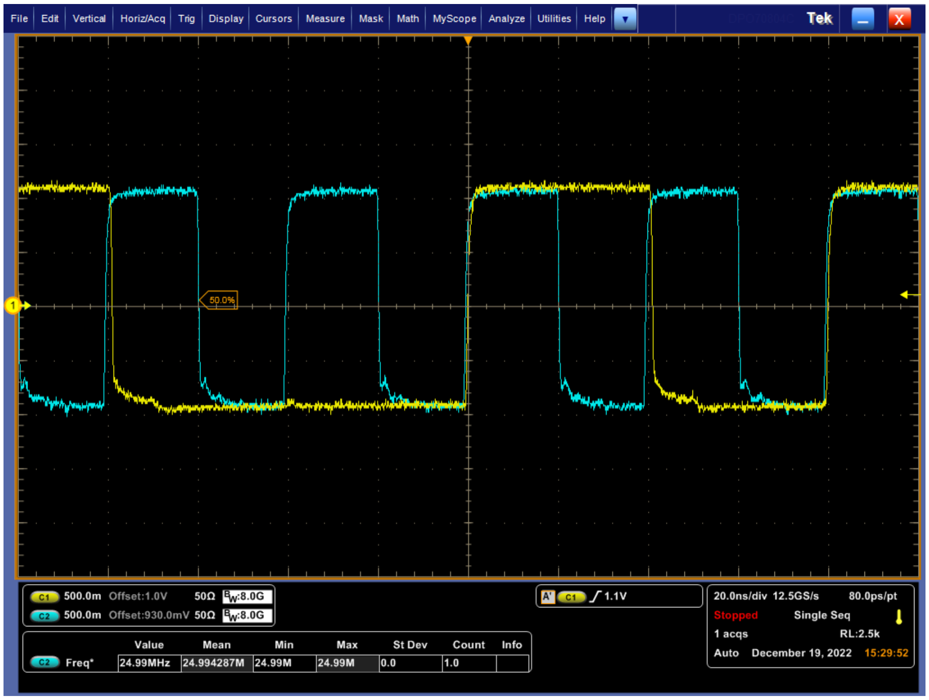
A' C1 ∫ 1.1V

200.0ns/div 12.5GS/s 80.0ps
Stopped Single Seq
1 acqs RL:25.0k
Auto December 19, 2022 15:26:30

	Value	Mean	Min	Max	St Dev	Count	Info
C2 Freq*	2.5MHz	2.4999755M	2.5M	2.5M	0.0	1.0	

Figure 2-11. 10 Mbps Data Aligned with RX_CLK

Verify the frequency of the clock (C2) as 2.5MHz, and the data (C1) being sampled at the rising edge of the clock.

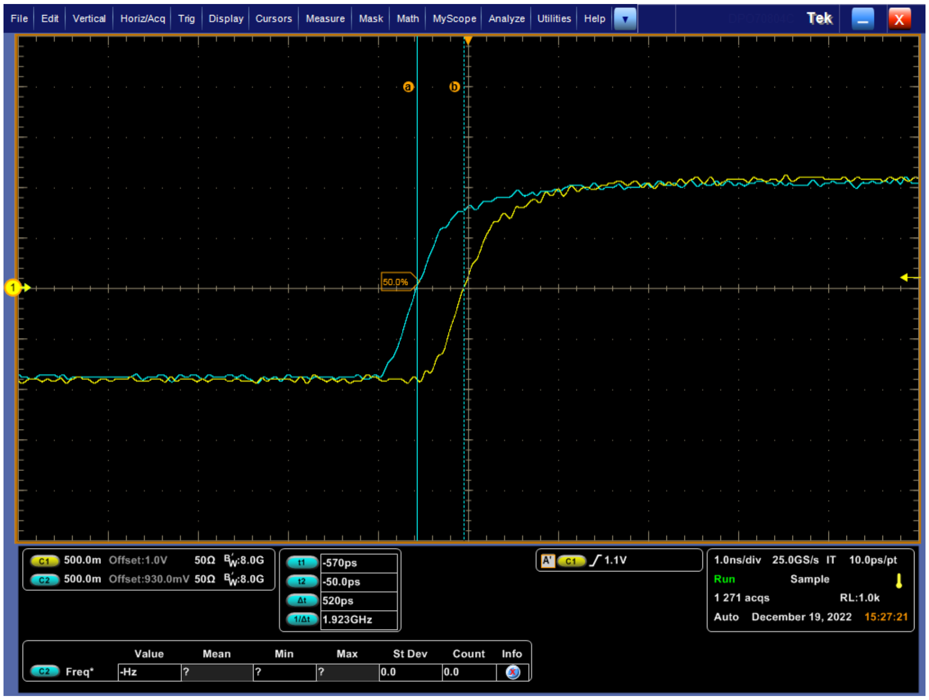

File
Edit
Vertical
Horiz/Acq
Trig
Display
Cursors
Measure
Mask
Math
MyScope
Analyze
Utilities
Help
Tek
50.0%
1

C1 500.0m Offset:1.0V 50Ω BW:8.0G
C2 500.0m Offset:930.0mV 50Ω BW:8.0G
A' C1 ∫ 1.1V
20.0ns/div 12.5GS/s 80.0ps/pt
Stopped Single Seq
1 acqs RL:2.5k
Auto December 19, 2022 15:29:52

	Value	Mean	Min	Max	St Dev	Count	Info
C2 Freq*	24.99MHz	24.994287M	24.99M	24.99M	0.0	1.0	

Figure 2-12. 100 Mbps Data Aligned with RX_CLK

Verify the frequency of the clock (C2) as 25MHz, and the data (C1) being sampled at the rising edge of the clock.


File
Edit
Vertical
Horiz/Acq
Trig
Display
Cursors
Measure
Mask
Math
MyScope
Analyze
Utilities
Help
Tek
a
b
50.0%
1

C1 500.0m Offset:1.0V 50Ω BW:8.0G
C2 500.0m Offset:930.0mV 50Ω BW:8.0G
t1 -570ps
t2 -50.0ps
Δt 520ps
1/Δt 1.923GHz
A' C1 ∫ 1.1V
1.0ns/div 25.0GS/s IT 10.0ps/pt
Run Sample
1 271 acqs RL:1.0k
Auto December 19, 2022 15:27:21

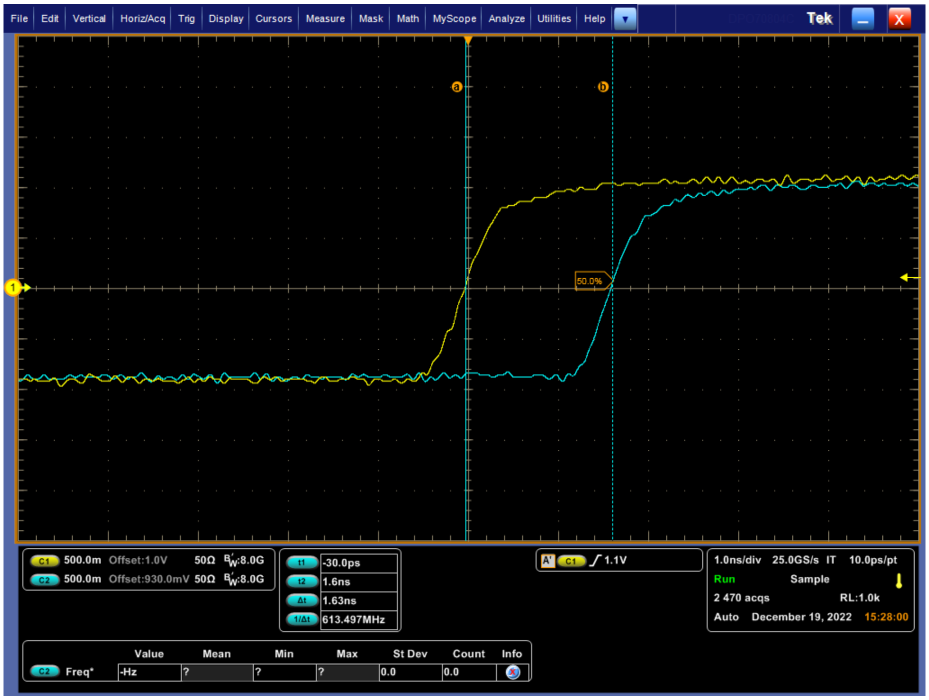
	Value	Mean	Min	Max	St Dev	Count	Info
C2 Freq*	-Hz	?	?	?	0.0	0.0	

Figure 2-13. 10Mbps Data and Clock Delay in Align Mode

Verify the delay between clock and data is <500ps in align mode.

RX_D[3:0] Data and RX_CLK in Shift Mode

For the PHY set in RX shift mode (0x32) in 10/100Mbps, probe the clock and data signals on the MAC end and compare to the following reference waveforms.


File
Edit
Vertical
Horiz/Acq
Trig
Display
Cursors
Measure
Mask
Math
MyScope
Analyze
Utilities
Help
Tek
a
b
1
50.0%

C1 500.0m Offset:1.0V 50Ω BW:8.0G
C2 500.0m Offset:930.0mV 50Ω BW:8.0G

t1 -30.0ps
t2 1.6ns
Δt 1.63ns
1/Δt 613.497MHz

A' C1 1.1V

1.0ns/div 25.0GS/s IT 10.0ps/pt
Run Sample
2 470 acqs RL:1.0k
Auto December 19, 2022 15:28:00

	Value	Mean	Min	Max	St Dev	Count	Info
C2 Freq*	-Hz	?	?	?	0.0	0.0	

Figure 2-14. 10 Mbps Data and RX_CLK in Shift Mode (4ns Programmed Delay)

Verify the delay between clock and data is >1ns in shift mode. The programmed delay is relative to the clock's initial position in aligned mode. Measuring the difference in the clock's position before and after setting shift mode yields a value closer to the programmed delay.

TX_D[3:0] and TX_CLK in Shift and Align Mode

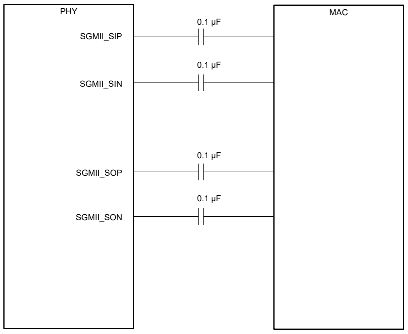
For the PHY set in TX shift or align mode, probe the data and clock signals on the PHY end and verify the timing requirements below are met:

For the PHY set in TX shift or align mode, probe the data and clock signals on the PHY end and verify the timing requirements following are met:

PARAMETER		MIN	NOM	MAX	UNIT
T_{skewT}	Data to Clock output Skew (at Transmitter)	–500	0	500	ps
T_{skewR}	Data to Clock input Skew (at Receiver)	1	1.8	2.6	ns
T_{setupT}	Data to Clock output Setup (at Transmitter – internal delay)	1.2	2		ns
T_{holdT}	Clock to Data output Hold (at Transmitter – internal delay)	1.2	2		ns
T_{setupR}	Data to Clock input Setup (at Receiver – internal delay)	1	2		ns
T_{holdR}	Clock to Data input Hold (at Receiver – internal delay)	1	2		ns
T_{cyc}	Clock Cycle Duration	7.2	8	8.8	ns
Duty_G	Duty Cycle for Gigabit	45	50	55%	
Duty_T	Duty Cycle for 10/100T	40	50	60%	
T_R	Rise Time (20% to 80%)			0.75	ns
T_F	Fall Time (20% to 80%)			0.75	ns

2.7.2 SGMII Debug

1. Check register 0x0037 bit[1:0] for link up status of SGMII interface.
2. Check schematic on SGMII lines make sure there is 0.1uF DC blocking caps.



3. Probe the lines on all SOP/SON and SIP/SIN signals to make sure the lines have the peak to peak voltage around 800mV.
4. Take a look on the trace length and impedance on the SGMII lines and make sure it follows the DP83867 Layout Checklist.
5. Write software reset 0x001F to 4000 or restarting SGMII auto-negotiation by register 0x0014 bit[7].

3 Application Specific Debugs

3.1 Improving Link-up Margins for Short Cables

If you are encountering an issue with packet loss or CRC errors while using the DP83867, please consider some of these items for debug when using short cables.

Short cables at 1m or less in length for your device can experience signal quality issues. One reason could be that the digital signal processing internally can take too long to converge or can converge to suboptimal filter values at shorter lengths which can result to a bad SNR - Signal to Noise Ratio. This then creates link dropping or potential packet losses which can require you to reset your device before beginning packet transfer again.

We have a register configuration below that can improve the SNR in applications where this marginality is observed. This script allows for a change in the timing bandwidths to make sure the DSP converges correctly:

```
begin
// Hard Reset
001F 8000
// Threshold for consecutive amount of Idle symbols for Viterbi Idle detector to assert Idle Mode
set to 5
0053 2054
// CAGC DC Compensation Disable
00EF 3840
// Master Training Timers - increasing time in different training states
0102 7477
// Master Training Timers - increasing time in different training states
0103 7777
// Master Training Timers - increasing time in different training states
0104 4577
// Timing Loop Bandwidth
010C 7777
// Timing Loop Bandwidth
01C2 7FDE
// Slave Timers - increasing time in different training states
0115 5555
// Slave Timers - increasing time in different training states
0118 0771
// Timing Loop Bandwidth
011D 6DB2
// Timing Loop Bandwidth
011E 3FFB
// Timing Loop Bandwidth
01C3 FFC6
// Timing Loop Bandwidth
01C4 0FC2
// Timing Loop Bandwidth
01C5 0FF0
// FFE Fix
012C 0E81
// Soft Reset
001F 4000
end
```

3.2 Improving Link Margins across Different Channels

The DP83867 uses an AGC gain convergence circuit (automatic gain control of MDI receiver) to provide faster linkup. There is a tradeoff between the linkup time and gain mismatch between pairs. In applications where packet errors are observed, gain matching can be improved for more optimal link by increasing the gain convergence time with the following register writes:

```
begin
// Hard reset
001F 8000
// Increase time for AGC
0102 7477
// No AGC Re-train
00E4 0080
// Soft reset
001F 4000
end
```

3.3 Link up in 100Mbps Full Duplex Force Mode

If DP83867 is configure in force 100Mbps full duplex force mode through register 0x0000 bit[12] and bit[6,13] and wasn't able to link up, please check the following process:

- Check the link partner PHY and see if auto-negotiation is enable on the link partner PHY.
- If the link partner PHY's auto-negotiation is on and able to advertise 100Mbps full duplex and half duplex, enable register 0x001E[11] for the link up
- If the link partner PHY's auto-negotiation is disable, make sure the link partner PHY is also program in force 100Mbps full duplex mode in register 0x0000.

3.4 Unstable Link Up Debug in 1Gbps communication

If repeating link up and link down between Dp83867 and another Link Partner behavior occur, please follow this session for debug:

1. Write register 0x001F to 4000 (software reset) and see if you are able to link up.
2. Check if DP83867 is able to link up with another TI giga-bit PHY.
3. Check the Schematic and Layout Checklist session to make sure the board design follow the recommendation.
4. Read register 0x0013 bit[12] and register 0x0011 bit[12]. If both registers indicate page received in 1Gbps communication. Write register 0x01D5 = F508 to change DP83867PHY from low power mode to normal operational mode.

```
begin
// Check page recieved in 1Gbps communication
0012
0013
// changing from lower power mode to normal operational mode
01D5 F508
end
```

3.5 DP83867PHY and DP83867PHY Cannot Link Up in 1Gbps

If two DP83867PHYs are able to link up at 10Mbps and 100Mbps but not able to link up at 1Gbps, please refer to the following debug process:

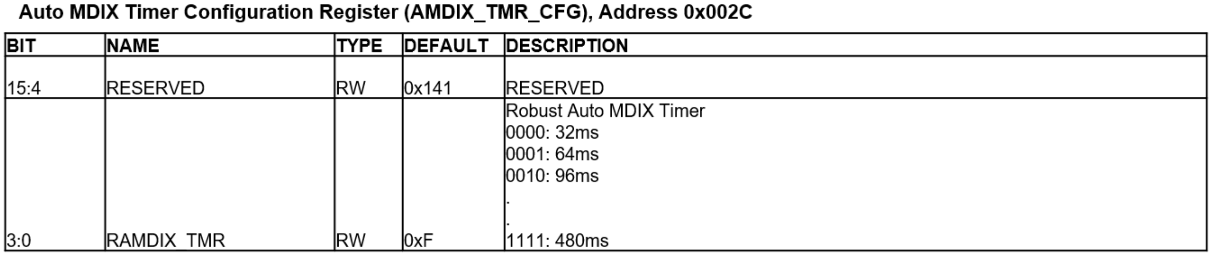
Note

This errata only occur in old revision of the DP83867PHY (Register 0x0003 = A0F1)

- Try software reset by writing register 0x001F = 4000 on one of the DP83867PHY and see if that resolve the issue.
- Read register 0x0005[15] and If 0x0005 bit[15] = 0,
  - Auto-MDIX is most likely not complete. Both of the PHY is sending Auto-MDIX FLP_Brust in the same channel at the same time and result in deadlock situation.

  Solution:

  - Change Auto MDIX timer on one of the PHY can prevent the deadlock situation.
  - Change register 0x002C bit[32] = 0 on one of the DP83867PHY



Auto MDIX Timer Configuration Register (AMDIX_TMR_CFG), Address 0x002C

BIT	NAME	TYPE	DEFAULT	DESCRIPTION
15:4	RESERVED	RW	0x141	RESERVED
3:0	RAMDIX_TMR	RW	0xF	Robust Auto MDIX Timer 0000: 32ms 0001: 64ms 0010: 96ms . . 1111: 480ms

  - write 0x001F to 4000 to software reset the PHY

- Read register 0x0005[15] and If 0x0005 bit[15] = 1
  - Auto-MDIX is complete and Auto-negotiation pseudo random number (PRN) is most likely be the issue. Pseudo random number (PRN) sending *random number* to determine which PHY is Master PHY (clocked from a local source) and which one is the slave PHY (clocked from the recovered clock on the received data stream) when both PHY are communicate in 1000Base-T. This can be check through register 0x000A bit[14].
  - However, the PRN is not exactly random and if both DP83867 start auto-negotiation at the same time, there is a possibility both DP83867 send out the exact same random seed (PRN) and result in dead lock.

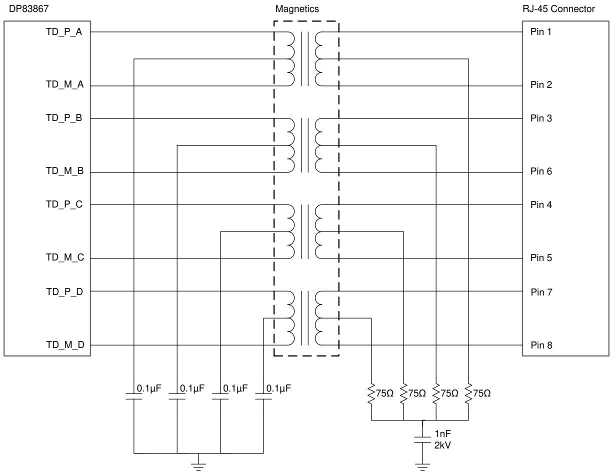
  Solution:

  - Write 0x0009 bit[12:11] to 11 on one of the DP83867PHY and write 0x0009 bit[12 :11] to 10 on another DP83867PHY. This register can force one of the PHY to always be MASTER in 1000Base-T communication to prevent the Pseudo random number (PRN) process.
  - Write 0x001F to 4000 to software reset the PHY or write 0x0000[9] =1 to restart the auto-negotiation

3.6 Compliance Debug

The following section mainly go over the general guideline on how to debug compliance issue on DP83867PHY.

- Check the schematic
  - Make sure the Transformer follow data sheet specification in Section 2.3.1.
  - No shorted center taps on transformer
  - Double check on the capacitors on the center taps of transformer


DP83867
Magnetics
RJ-45 Connector
TD_P_A
TD_M_A
TD_P_B
TD_M_B
TD_P_C
TD_M_C
TD_P_D
TD_M_D
Pin 1
Pin 2
Pin 3
Pin 6
Pin 4
Pin 5
Pin 7
Pin 8
0.1µF
0.1µF
0.1µF
0.1µF
75Ω
75Ω
75Ω
75Ω
1nF
2kV

  - Remove ESD diodes on MDI lines for compliance test
  - Check Rbias value and make sure the value falls in the 1% range
  - Follow the schematic check list recommendation in Section 2.2
- Check the layout
  - Make sure no clock signal and data signal near the MDI lines
  - Check length matching and impedance matching (100ohms) for MDI lines
  - No vias around the MDI lines
  - Follow the layout checklist in Section 2.2
- Check the compliance test *How to Configure DP8386x for Ethernet Compliance Testing* application note. Follow the procedure on the compliance test application note.
- If all schematic, layout checklist, and compliance test application note do not help, adjusting register 0x00A0, 0x00A1, 0x00A2, 0x00A3 can help with compliance test.

Note

Default values of 0x00A1 and 0x00A2 registers are trimmed.

3.7 EMC Debug

The following section mainly go over the general guideline on how to debug EMC issue on DP83867PHY.

- Check the test setup:

  EMC test:

  - No loop cable

  - Place the cable away from the emission source or Antenna (mainly on RE test)
  - Shielded cable is preferred
  - Make sure the test board and test equipment match (mainly on CE test)
    - Cable type needs to match the CDN test equipment
  - Turn off CLK_OUT when it is open or not used
  - EMI test:
    - Check the ground path of both test board and test equipment
    - Shielded cable is preferred
    - Make sure the cable type match with test equipment (mainly on CI test)
      - Cable type needs to match the CDN test equipment
- Check the schematic
  - Make sure there is a ground isolation

    Make sure there is a ground isolation path (R//C) between connector ground and earth ground

    Make sure the Transformer follow data sheet specification

    No shorted center taps on transformer

    Double check on the capacitors on the center taps of transformer

    Remove ESD diodes on MDI lines for compliance test

    Check Rbias value and make sure the value falls in the 1% range

    Follow the schematic check list recommendation in Section 2.2
- Check the layout
  - Make sure no clock signal and data signal near the MDI lines
  - Check length matching and impedance matching for MDI lines
  - No vias around the MDI lines
  - Follow the layout checklist in Section 2.2
- If customer is struggling on conducted immunity IEC61000 4-6 on DP83867 PHY, please program the following script:
  -
    ```
    begin
    008A 010F
    00C0 0000
    00B3 000C
    0100 1027
    001F 4000
    end
    ```

These registers tune the filter inside the PHY to further optimize and filter out high frequency noise and improve the Signal to Noise ratio.

3.8 Tools and References

The following section contains additional tools and references relevant for debugs.

3.8.1 DP83867 Register Access

If register access is not readily available in the application, USB-2-MDIO GUI is available from TI and can be used with an MSP430 Launchpad, and purchased through TI.com. The GUI supports reading and writing registers as well as running script files. USB-2-MDIO GUI can be used with the DP83867 and the other devices in TI's Ethernet portfolio. The USB-2-MDIO User's Guide and GUI are available for download at: USB-2-MDIO serial management tool.

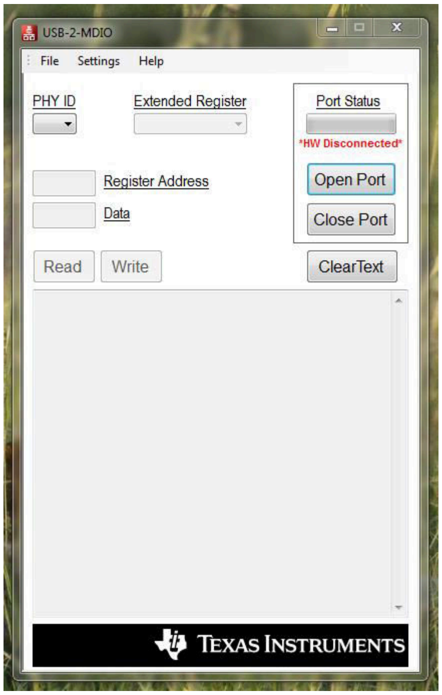

USB-2-MDIO
File
Settings
Help
PHY ID
Extended Register
Port Status
HW Disconnected
Register Address
Data
Open Port
Close Port
Read
Write
ClearText
TEXAS INSTRUMENTS

Figure 3-1. USB-2-MDIO GUI

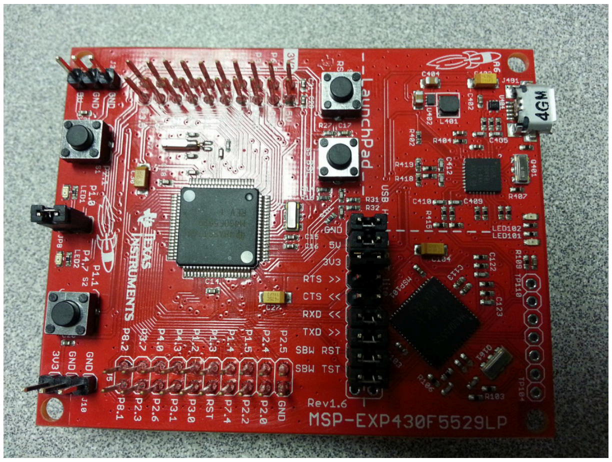

LaunchPad
TEXAS INSTRUMENTS
Rev1.6
MSP-EXP430F5529LP

Figure 3-2. MSP430 LaunchPad

Following is an example script that can also be found in the USB-2-MDIO GUI in the Help menu:

```
// This is how you make a comment. All scripts must start with 'begin'
begin
// To read a register, all you need to do is put down the 4 digit
// HEX value of the registers (from 0000 to FFFF)
// Example to read registers 0001, 000A, and 0017
0001
000A
0017
// To write a register, all you need to do is put down the 4 digit
// HEX value of the register (from 0000 to FFFF) followed by the
// HEX you desire to configure the register to (from 0000 to FFFF)
// Example to write 2100 to register 0000 and
// Example to write 0110 to register 0016
0000 2100
0016 0110
// You must end the script by adding 'end' once you are finished
end
```

The Serial Management Interface defined by IEEE 802.3 is a single master bus. The MDC clock is generated by the bus master, typically an Ethernet MAC. To use the USB-2-MDIO GUI, connections must be made directly between the MSP430 Launchpad and the DP83867 MDIO and MDC pins. Specifically, pins 4.1 to MDC, 4.2 to MDIO, and any GND to the ground of the PHY will allow the MSP to read and write the PHY's registers via USB-2-MDIO.

3.8.2 Extended Register Access

To read and write registers in extended register space, refer to the following procedure:

Write procedure for MMD "1F" registers:

write reg<000D> = 0x001F

write reg<000E> = <address>

write reg<000D> = 0x401F

write reg<000E> = <value>

Read procedure for MMD "1F" registers:

write reg<000D> = 0x001F

write reg<000E> = <address>

write reg<000D> = 0x401F

read reg<000E>

Note

- To read or write MMD "1" registers, replace 1F with 01.
- Above write and read procedure is normally used for registers with address greater than 0x001F. But the procedure can also be used for any address in general.

4 Conclusion

This application note provides a suggested flow for evaluating a new application and confirming the expected functionality. The step-by-step recommendations will help ease board bring up and initial evaluation of DP83867 designs.

5 References

1. Texas Instruments, *How to Pass IEEE Ethernet Compliance Tests*, application note.
2. Texas Instruments, *How to Configure DP838xx for Ethernet Compliance Testing*, application note.

6 Revision History

Changes from Revision B (December 2022) to Revision C (April 2024)	Page
• Updated DP83867 Configurations table	2
• Updated the register table	3
• Updated the schematic and layout checklist hyperlink	4
• Added power up sequence note	5
• Added timing diagram on when the strapping event occurs	6
• Added steps for debug of MDIO/MDC lines	8
• Updated Link Quality test	10
• Added a section on loopback and diagram on BIST	11
• Added section for debugging SGMII interface	14
• Added Link up in 100Mbps full duplex Force mode	19
• Added unstable link up debug	19
• Added errata debug on old revision silicon of DP83867	20
• Added compliance debug section	21
• Added EMC debug session	22

Changes from Revision A (April 2016) to Revision B (December 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	2
• Added reference register values for PHY linked in 1000 Mbps	3
• Deleted list of key configuration and status registers	3
• Added section for schematic and layout checklist	4
• Added section for component checklist	4
• Added section for peripheral pin checks	5
• Updated loopback and BIST sections with testing procedure and corresponding scripts	11
• Added section for debugging MAC interface	14
• Added section for application specific debugs	18
• Added section for tools and references	23

Changes from Revision * (October 2015) to Revision A (April 2016)	Page
• Added Auto-Negotiation status registers to list of key configuration and status registers	3
• Changed phrasing of descriptions for two and three supply configurations	5
• Changed description of three supply power sequencing	5
• Changed order of RBIAS measurements in *Section 2.4.2*	6
• Added recommendation to confirm strap values in strap status registers	6
• Added cable connection diagram for termination cable	9
• Added section on register access	23
• Changed images for USB-2-MDIO GUI and MSP430 LaunchPad in *Section 3.8.1*	23
• Changed format of USB-2-MDIO link	23
• Added example script for USB-2-MDIO	23

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265