Gigabit Ethernet – IEEE 802.3z
The Choice of a New Generation
Final Report

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Introduction

In the last few years the world of communications has known a series of revolutions, the most important of which was the Internet. It revolutionized the way people communicate not only within the United States but also all around the world. Almost every American household is now connected to the Internet. In addition, in countries less industrialized, Cyber Cafes have flourished in every street corner. This increased usage has created a constant craving for faster connections with an increased bandwidth for all types of new applications. Both these needs have fostered the emergence of new technologies such as the Ethernet, the Fast Ethernet, than the Gigabit Ethernet. The important place of the Gigabit Ethernet in today's world of telecommunications in general and electrical engineering in particular has made it a topic of choice for a design capstone for prospective electrical engineers.

The goal of this project is therefore to design implement and test the transmitter module of a Gigabit Ethernet Intel Network card. The first step towards achieving this goal was to gain some background knowledge about the topic.

Evolution of the Ethernet

In general, the Ethernet brought many advantages including simpler networks, larger capacity, lower cost and increase in efficiency. With the growing usage of this technology, there was soon a need for standards for the convenience of both manufacturers and consumers. In order to fulfill this need, a task force was created by the Institute of Electrical and Electronics Engineers (IEEE) to put the 802 standard together. For the concerns of the project, the part of the standard that we are interested in is the 802.3, which covers the physical layer of the Ethernet for Local Area Networks or LANs. Figure 1 shows a drawing of the first Ethernet system.
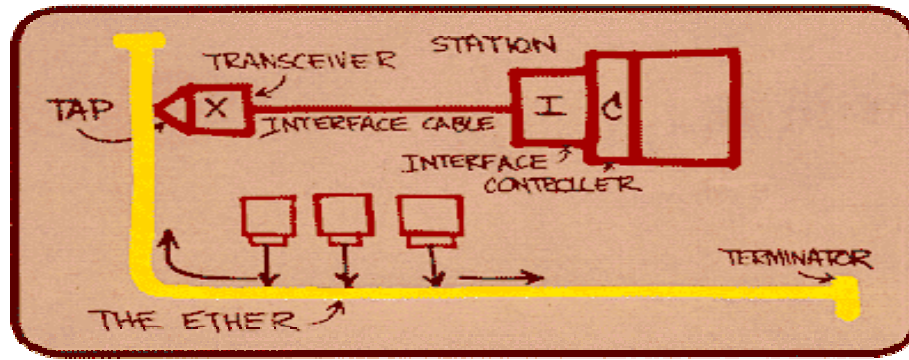
Figure 1- Drawing of the First Ethernet System [1].

From the simple structure illustrated in Figure 1 on the previous page, the Ethernet evolved to a much more complex entity and a much faster means of data transmission. In fact it has steadily evolved to reach speeds of transmission of 1Mbps then 10, 100 and 1000Mbps as illustrated in Figure 2 on the next page.
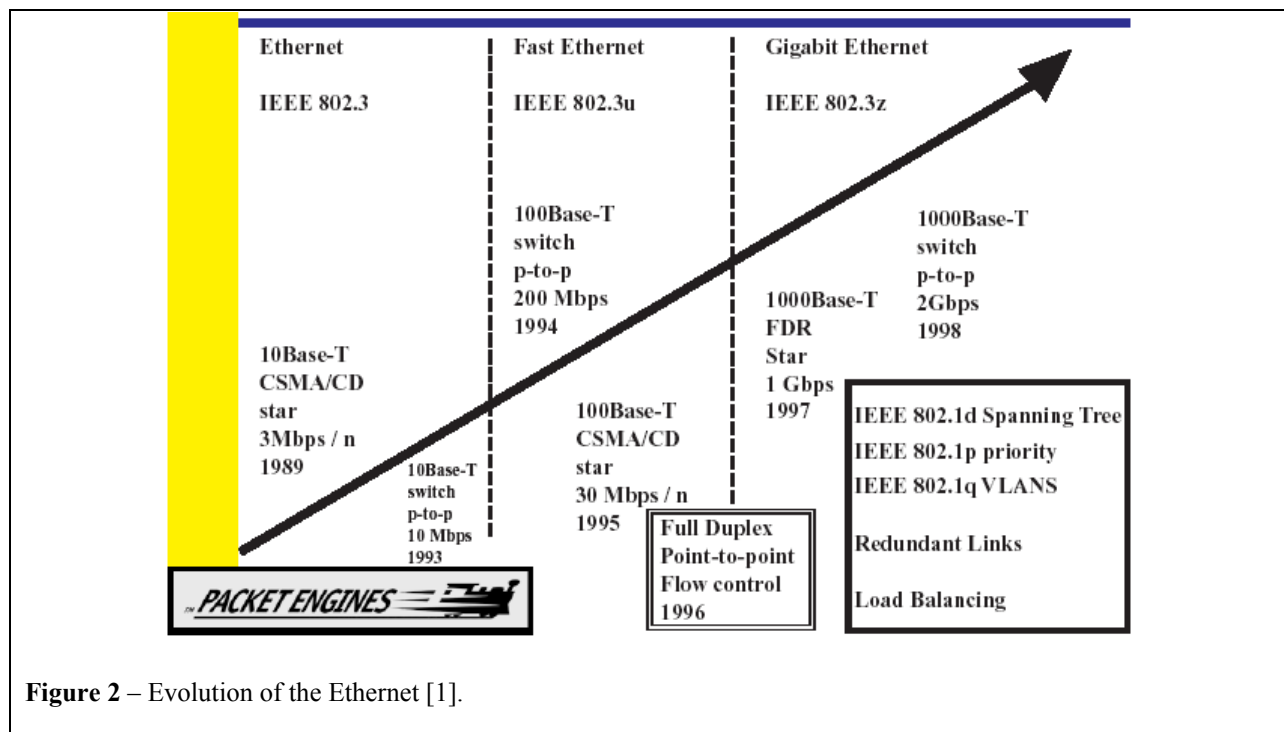

Figure 2 – Evolution of the Ethernet [1].

From this figure, it can easily be inferred the reason why the terminology Gigabit Ethernet is now in use instead of the name "Ethernet" by itself. The constant improvements of the Ethernet

along with the many advantages it brought made it earn a very important place in the market. In an attempt to better understand the technology behind the Ethernet, the next part of the discussion will cover the 802.3 standards.

The Ethernet Standards: 802.3

In researching the IEEE standards, four parts seemed relevant to the Ethernet: 802.3ab, 802.3u, 802.3ae and 802.3z. The 802.3ab standard is for the 1000BASE-T, which is the twisted-pair for the Gigabit Ethernet's physical layer i.e. the actual wiring of physical connections. 802.3u represents the standard for the Fast Ethernet with speeds around 100Mbps. In addition, the 802.3ae sets the standard for the 10-Gigabit Ethernet while the 802.3z is for the 1-Gigabit Ethernet with fiber-optic cables [1]. The latter is the only standard needed for the accomplishment of the task assigned in this project. Since the specified medium of transfer for the 802.3z standard is fiber optic cables, the choice was still to be made between Single-Mode and Multi-Mode fiber.

Single-Mode Fiber (SMF) vs. Multi-Mode Fiber (MMF)

The ever-emerging world of the telecommunication industry is always seeking more bandwidth for information transfer for example wired or wireless communications. Until recently, about 80 percent of all network traffic were for professional use. However, times have changed and nowadays, the traffic primarily runs in Local-Area Networks (LANs), Wide-Area Networks (WANs) or the Internet [2]. The great demand for more bandwidth has now made more appealing to adopt new methods of transmission. In fact, traditionally, data has been sent via copper wires in the form of electrons but now a newer and more efficient medium is transmission of data as photons (light) over fiber. The advantages of fiber over wire can easily be understood by looking at Figure 3.
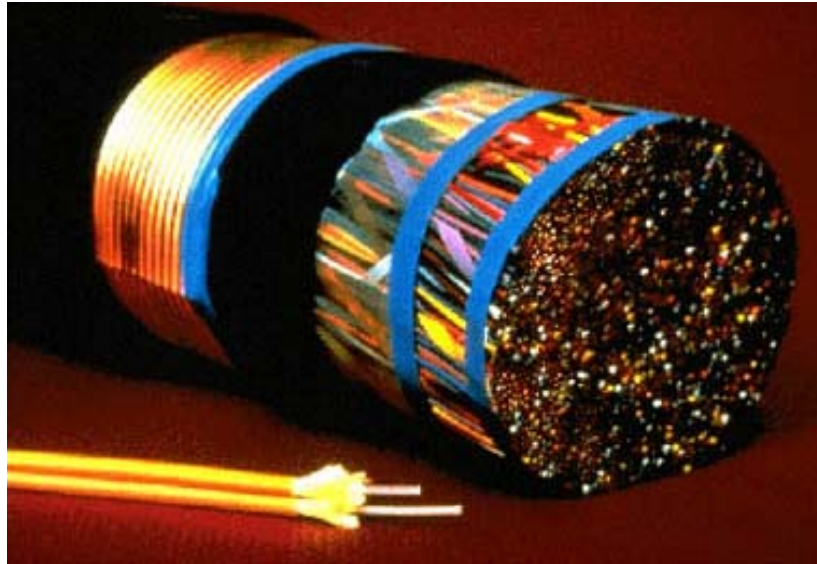
Figure 3. Several copper wires (above) and two fiber cables (below).

The two fibers can transfer the same amount of information as the bundle of wires. Fiber comes in two forms, Single-Mode Fiber and Multi-Mode Fiber. The mode is the grouping of light pulses. Single-mode fiber has very good characteristics. In fact, it conserves signal integrity because the light travels parallel to the center axis and therefore eliminates interference due to trailing edges of pulses [3, 4]. It has a diameter size of about 9 microns or less. Multi-mode fiber comes in different forms, among which, step-index and graded-index. Step Index has a diameter of up to 100 microns and the light moves in zigzag across the fiber channel causing varying arrival times for the signal.

The graded-index multi-mode fiber has a core size between 50 and 62.5 microns and has a higher index of refraction in the center and gradually decreases when moving away from the center. The result is that the part of the signal moving in the center is faster, resulting in more dispersion. Given its advantages, the best choice for the fiber might appear to be SMF but graded index showed to better suited when the cost is taken into consideration.

VCSEL vs. EEL

In order for the signal to be repeated and amplified along the networks of fiber-optic cables, the tool of choice is a laser. The first lasers that were in the market were Edge Emitting Lasers (EELs). Then, Vertical Cavity Surface Emitting Lasers (VCSELs) came into use. The advantages of the VCSEL are multiple. Among these its circular laser beam that makes it easier to couple with fiber. This also makes it cheaper than EELs, which have an elliptical beam that needs corrective optical lenses for coupling. Another advantage of VCSELs over EELs is that VCSELs can be tested in the wafer form because the laser beam is perpendicular to the substrate. This allows the bad chips to be discarded earlier in the manufacturing process, therefore increasing the yield and decreasing the unit price. Because of all its advantages, the best choice for the project is VCSELs.

Specifics of the Project

In addition to our group two other groups are working on the same Intel Network Card. The OE module, which is a transceiver, is the specific part of the PC Network card that the 3 groups will try to implement. The first group will work on the receiver; the second group will test and build the laser and the last group ours, will conceive and build the transmitter. Figure 4 is a representation of the PC card and OE Module.
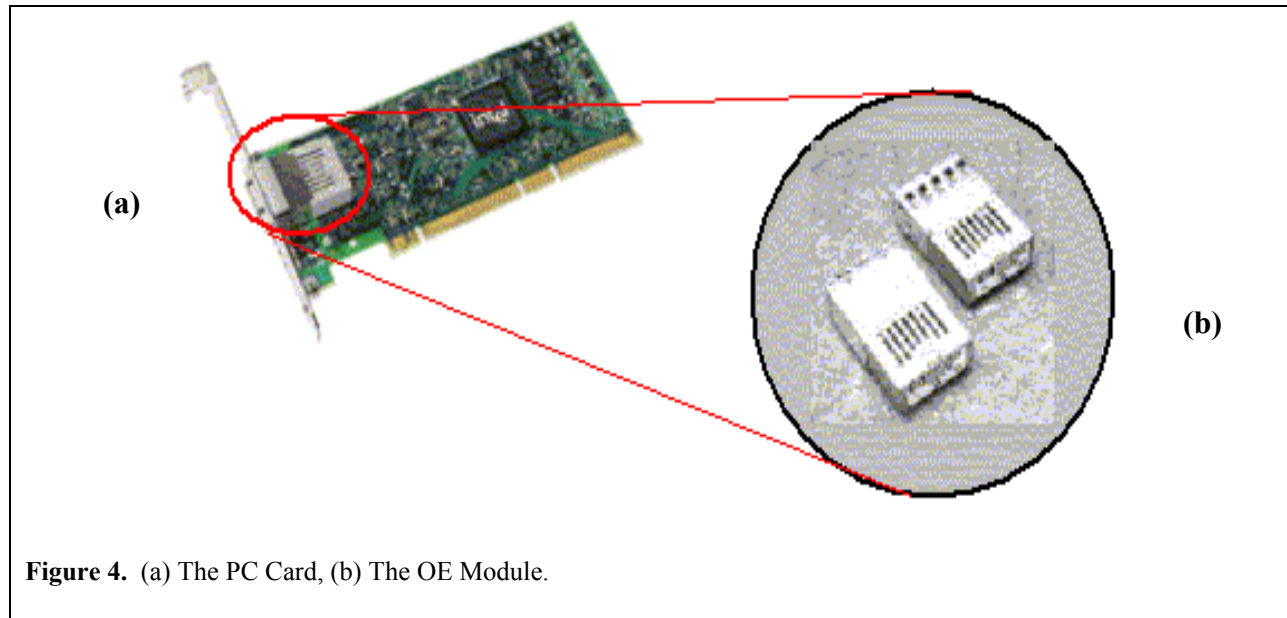
Figure 4. (a) The PC Card, (b) The OE Module.

The network card to be rebuilt is the Intel Pro/1000f Gigabit Ethernet card shown on figure 4a and 4b is the opto-module. In order to make the transmitter of the OE module, the MAX3287 chip will be used. In fact, it is a Transmitter and can be evaluated or tested using the evaluation board (MAX3287SW EV KIT). The chip is usually configured in common cathode configuration and works with an adjustable DC current. It can be pre-biased to a current that is compatible with the VCSEL it is connected to. Additional features include an adjustable photodiode current and an adjustable modulation current. The evaluation is configured for electrical operations, which allows SMA cables to be directly connected to it. The outgoing SMA cable can then be plugged into a pigtailed VCSEL.

Building and Testing

The evaluation kit as well as the board that is to be built will be tested using different methods. One of those is to compare the eye diagram obtained from the evaluation kit or board with the eye mask shown in Figure 5.
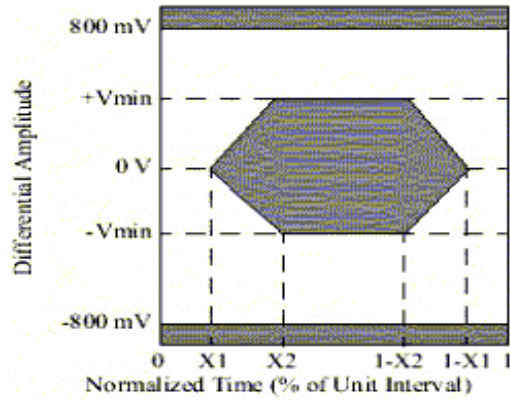
Figure 5. The eye mask used to test the transceiver.

The eye mask is provided by the IEEE 802.3z standard and shows the difference between a logical 0 and a logical one. Other testing methods include measuring the amount of errors that occur during transmission using a Bit Error Rate Tester (BERT). The evaluation board will be replicated using parts chosen and ordered by the group.

In order for the board to be replicated, a certain set of design modifications were made on the evaluation board but before this, a closer look at the Intel Card/ Opto-module and at the Maxim Board/ Maxim 3287 Chip.

Intel Card/ Opto-Module

In order to build a working replica of the transmitter of the Intel Card, it is necessary to gain a better understanding of the opto-module. Figure 6 is a top view of the connection pins of the latter.
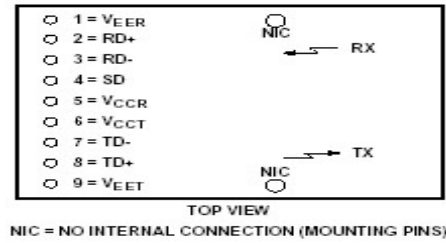
Figure 6. Top View of the Connections of the Opto-module.

The pins on the above figure labeled 1 through 9 have the following functions:

- Pins 1 and 9 are the grounds for respectively the receiver and the transmitter.

- Pins 2 and 3 are the Receiver differential output.

- Pin 4 is the signal detect, which provides the information about the link being off.

- Pins 5 and 6 provide respectively the transmitter and receiver powers.

- Pins 7 and 8 are the differential outputs for the transmitter.

The figure shows how to connect components to the module but a closer look at its circuitry is needed. Figure 7 provides a schematic of the opto-module.
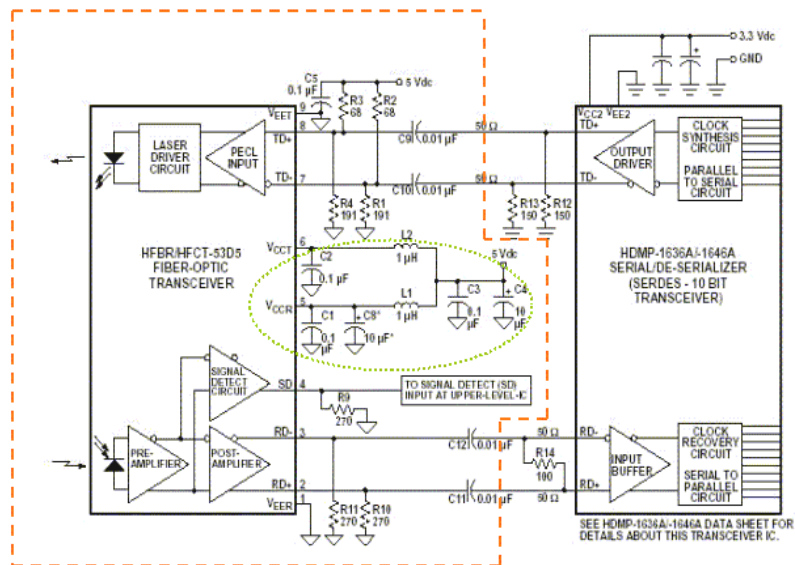

Figure 7. Opto-Module Connected to Intel Card.

The elements in the dashed box are the actual opto-module. The top circuit (with the laser

driver) is the transmitter while the bottom circuit is the receiver. The section of the circuit in the

circle is a filter for the noise originating in the power supply. Resistors 1 through 4 are in parallel

in ac and therefore provide a 50Ω termination to the cables. The capacitors C9, C10, C11 and

C12 provide a dc coupling to the lines they are connected to. Figure 8, below shows how the

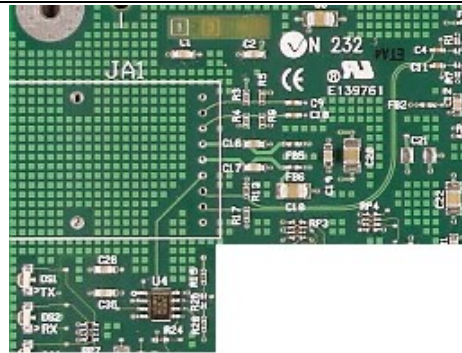opto-module connects with the Intel network card.

Figure 8. The Opto-Module as it Connects to the Intel card [5].

In the white box of the figure, there is the same representation as Figure 6. The parts that

constitute the opto-module will be connected in the following fashion (Figure 9) to rebuild the
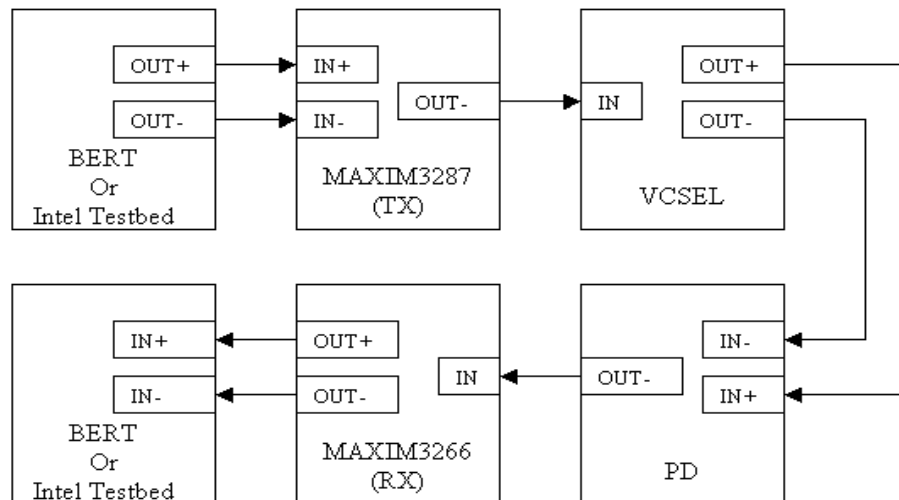
component.

Figure 9. High Level Drawing of the Reconstructed Opto-Module.

Maxim Board Specifications and Maxim 3287 Chip

In order for the group to succeed in rebuilding the transmitter of the Intel card, it is very important to study the Maxim board and its specifications as well as the Maxim 3287 chip. The board is optimized for operation at 1.25Gbps and can support 30 mA of laser modulation current at the specified data rate. In addition, the deterministic jitter (DJ) for the chip is approximately 22ps. The main component on the board to be replicated is the MAX3287, which is the 16-pin chip illustrated in Figure 10.
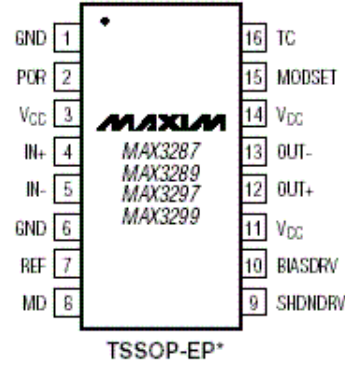

**Figure 10.** MAX3287 Laser Driver Chip [6].

The pins on the figure have the following functions:

- Pins 1 and 6 are ground (GND).

- Pin 2 is the power-on reset (POR). This feature resets the laser when it has been turned off. The signal is low when VCC is within the operating range of 3 to 5V. The POR also contains an internal delay for noise rejection during power-on or hot-plugging.

- Pins 3, 11, and 14 labeled as VCC are connected to a 3 to 5 volt power supply.

- Pins 4 and 5 are the non-inverting (IN+) and inverting (IN-) inputs respectively.

- Pins 12 and 13 are the modulation-current outputs. These differential outputs eliminate the noise that may be generated during transmission.

- Pin 7 is the reference voltage.

- Pin 8 is the monitor diode used for automatic power control of the laser.

- Pin 9 is the shutdown driver output (SHDNDRV) a safety feature that shuts down the laser.

- Pin 10 is the bias controlling transistor driver (BIASDRV). A capacitor is needed to ensure the rejection of the noise from the power supply.

- Pin 15 is the modulation-current set (MODSET) and Pin 16 is the temperature compensation. The amplitude of the modulation current is set with the resistors in the MODSET and TC pins.

Maxim Board Layout Analysis

The following figure shows 2 versions of the evaluation board circuitry.

Figure 11. Maxim Board Layout
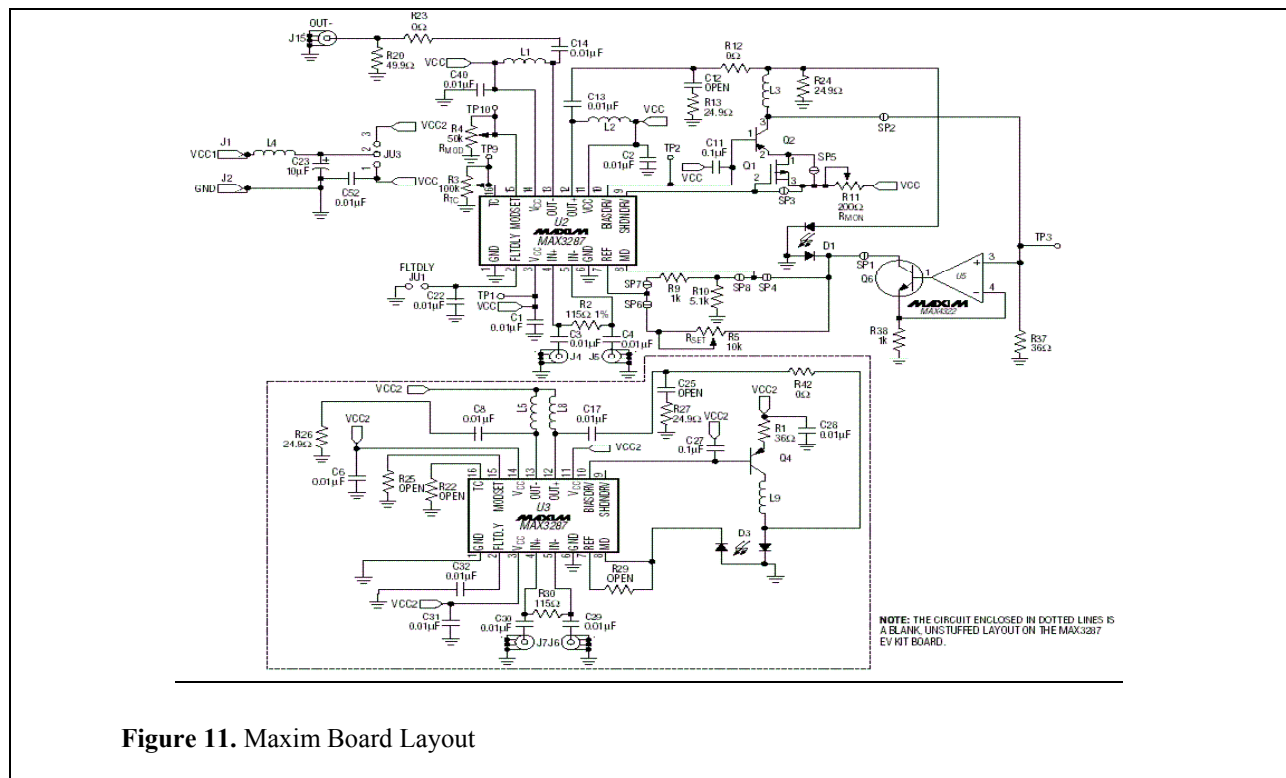
The analysis of the board layout will consider the circuit in the box. In fact, the stuffed layout consists of more components because it utilizes a lot of safety features incorporated in the Maxim chip (U2). These extra features will not be needed in our design. The following are the functions featured on the evaluation board:

- Transistor Q1 is a switch to turn the laser on and off and is not needed.

- The fact that the laser will not be mounted on the chip, components U5, Q6, R5, R9, R10, R24, R37, R38 and D1 are unnecessary.

- Q2, L3 and R11 are used to control the current needed to drive the laser via the SMA cables connected to J15.

- Decoupling capacitors (C1, C2, C3, C4, C11, C12, C13, C14, C22, C23, C40, and C52) are open when a dc bias is applied and short when an ac bias is applied.

- R_{MOD} and R_{TC} are needed to control the current modulation and the temperature coefficient of the laser.

Board Set-Up

Our first task in this project is to set-up the Maxim board for proper operation with the Intel/PRO 1000. The board may be configured in different ways but in this project, the common cathode configuration is to be used. The following 12-step process will be used to configure the board:

1) Set the R4 (RMOD) potentiometer to maximum resistance by turning the screw completely counterclockwise (approximately 50 kΩ). This minimizes the modulation current.

2) Place a jumper between pins 1 and 2 on JU3 to provide power to the main circuit.

3) Remove R24 (24.9 Ω) and replace it with R20 (49.9 Ω).

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4) Attach differential sources to SMA connectors J4 and J5. Each source should have a peak-to-peak amplitude between 100mV and 830mV.

5) Connect an SMA cable from J15 (OUT-) to the laser module. This output will be used to drive the laser. In order for the current to be large enough to drive the laser, the PNP transistor attached to pin 5 (BIASDRV) must be biased correctly.

6) While monitoring the laser output, adjust R4 (RMOD) until the desired laser modulation current is obtained.

7) While monitoring the laser output, adjust R4 (RMOD) until the desired laser modulation current is obtained.

8) Look at the eye output on an oscilloscope capable of supporting frequencies of up to at least 1.25 GHz, such as the Tektronix TDS7154 DPO, 1.5 GHz, 20 GS/sec.

Building our own Board

One of the goals of this project will be to build our own board. The first part involved analyzing the new Maxim board and understanding how it worked. After this careful analysis, the following circuit in Figure 12 was the initial board layout but was modified subsequently.
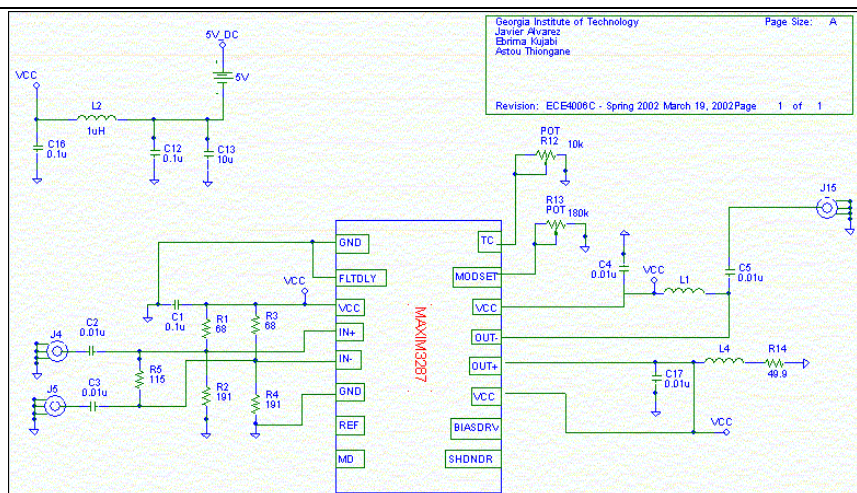

Figure 12. Initial Schematic of Proposed Circuit Design.

As shown on the top left of Figure 12, the power supply is being regulated to supply a steady voltage of 5 Volts, as well as filtering out any noise due to the power supply. Also, all of the safety features and on-board laser biasing components attached to pins 7, 8, 9, and 10 were removed. Since the laser will be driven via the SMA connector (J15), there is no need for the transistors and it's biasing components because they were only used to provide a certain threshold current for a laser mounted on the Maxim board. The following table, Table 1, is a list of components that will needed in order to complete the design of our own board.

Description	Component Value	Quantity
Resistors (1206) (Surface Mount)	68Ω	2
Resistors (1206) (Surface Mount)	191Ω	2
Resistors (1206) (Surface Mount)	115Ω	1
Resistors (1206) (Surface Mount)	49.9Ω	1
Resistors (1206) (Surface Mount)	68Ω	2
Trimmer Potentiometers (3296W)	200kΩ	2
Capacitors (1206) (Ceramic Chip)	0.1μF	3
Capacitors (1206) (Ceramic Chip)	0.01μF	5
Capacitors (1206) (Ceramic Chip)	10μF	1
Ferrite Bead Inductor (BLM11HA102SG)	N/A	2
Inductor (1206)	1μH	1
SMA Connectors	N/A	3
Power Supply Connector	N/A	1
MAXIM3287 Chip	N/A	1

Table 1. Required Component List.

 In order for our board to be built, we also had to make a layout with the Super PCB (Printed Circuit Board) software and here is the resulting schematic as Figure 13.
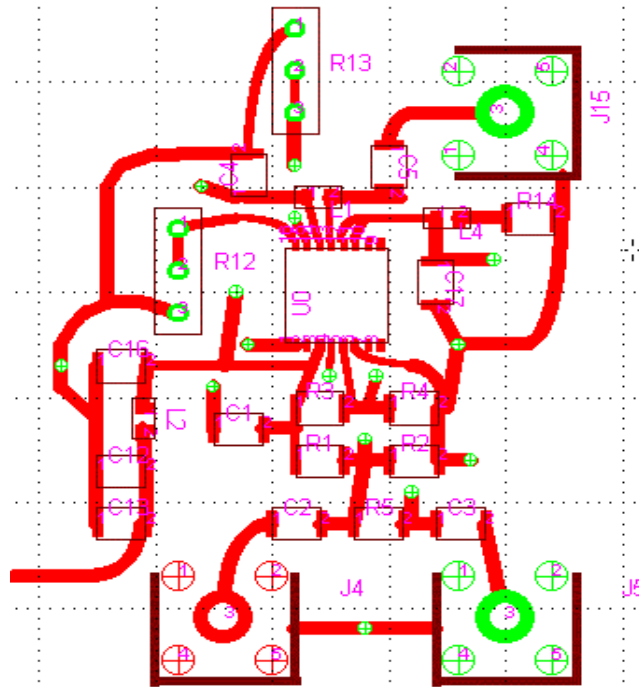
15

Figure 13. Board Layout Using SuperPCB.

The above circuit was drawn taking transmission lines problems into consideration.

RESULTS

The first part of this project involved testing the previous semester's Intel testbed. Once the card was seated into a PCI slot, a loop back test was performed using the Intel diagnostic software that was included with the Intel PRO network card. The test was successfully performed several times. The second part of this project involved testing the Maxim 3287 Evaluation (TX) board. Initially, the board was going to be tested by connecting it to the other OE modules as shown in Figure 9 and testing it with the working Intel testbed. However according to Professor Brooke, since a bit error tester (BERT) had been obtained in the laboratory, there was no need to use the Intel testbed. The bit-error tester would allow us to send random bit patterns to our board in order to obtain an eye diagram. Even though, the BERT in the laboratory was not capable of displaying the number of bit errors, it was still practical for

sending out raw bits. For this reason, the output was fed back into an oscilloscope in order to obtain an eye diagram. The Tektronix DTS 7154 oscilloscope was used for several reasons. First, it was capable of obtaining signals up to 1.5 GHz. This would allow us to obtain an eye diagram for our 1.25 GHz signal. Secondly, the oscilloscope contained a Gigabit Ethernet 802.3z mask, which would allow us to know if the eye was open enough for valid transmission in Gigabit Ethernet networks.

Initial Maxim Board Setup

Once the Maxim boards were received, preliminary tests were performed in order to determine proper functionality. The initial board setup involved connecting the BERT differential TX outputs to the differential inputs of the Maxim board as illustrated in Figure 14. The output of the Maxim board was then fed into channel 1 of the oscilloscope, while the sync output of the BERT was connected to channel 3. The sync output of the BERT was used to achieve the correct triggering on the oscilloscope.
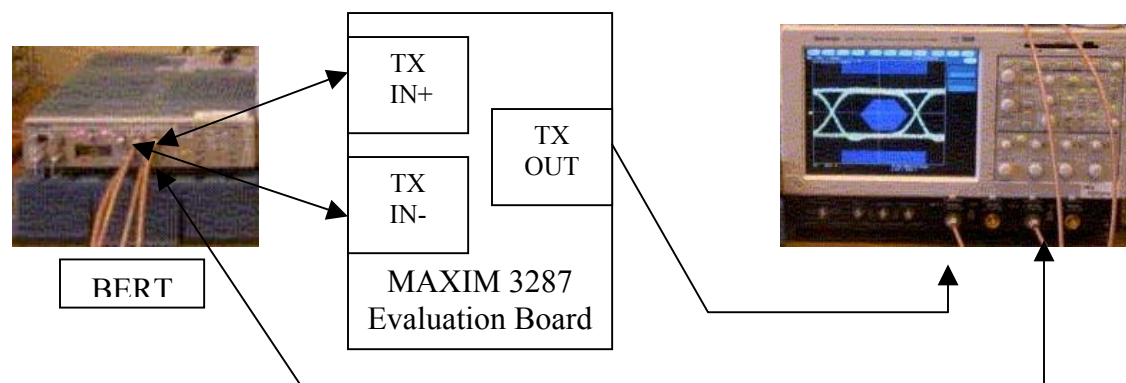

Figure 14. Initial Maxim board setup.

All of the connections were done via SMA connectors. Initially since the Tektronix DTS 7154 oscilloscope shown in Figure 14 was not available, we tried obtaining an eye diagram from the Tektronix TDS 3054 oscilloscope shown in Figure 15a. However, since this oscilloscope could

not fully capture all of the harmonics of a 1.25 GHz sinusoidal signal, we were not able to obtain

an eye diagram. Instead, the signal shown in Figure 15b was captured.

Figure 15. (a) Tektronix TDS 3054 oscilloscope, (b) Signal Obtained.
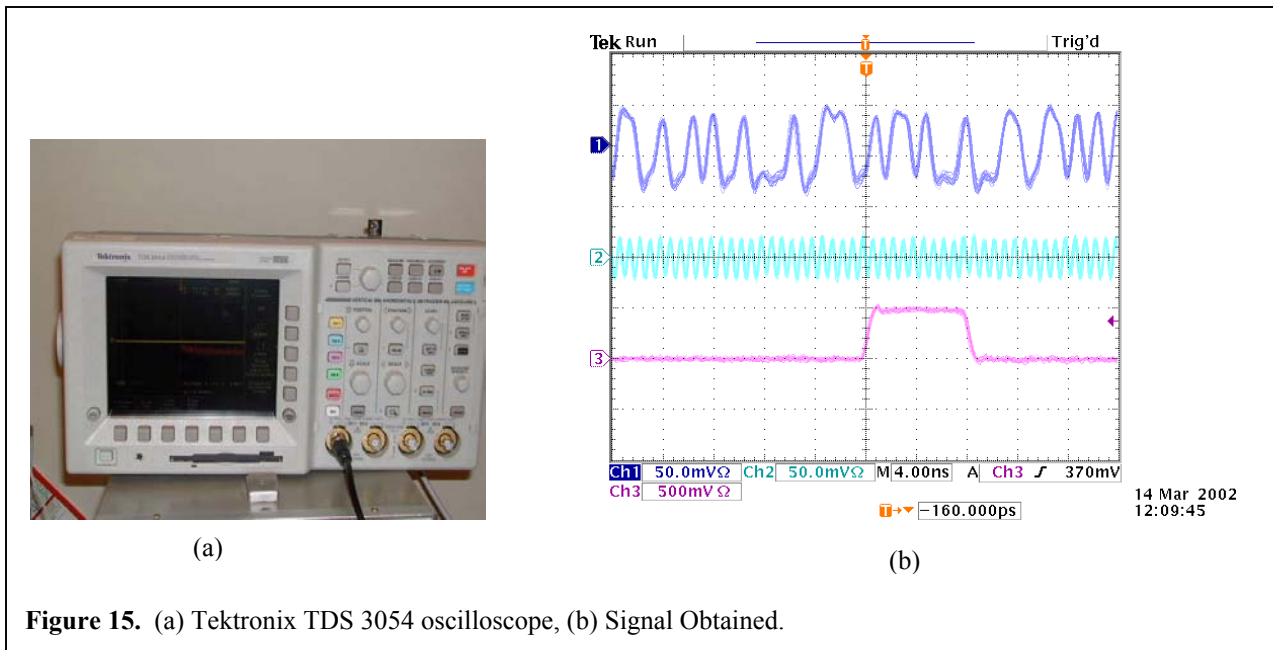
Channel 2 in Figure 15b illustrates the input signal, while channel 1 illustrates the output from

the Maxim board. Channel 3 is a sync pulse from the BERT used to trigger the oscilloscope. At

least, this assured us that the Maxim board was working. Once the Tektronix DTS 7154

oscilloscope was obtained in the laboratory, an eye diagram was obtained. In order to facilitate

obtaining an eye diagram, Professor Brooke conveniently installed the correct setup for the

oscilloscope. This was simply done by selecting "File" from the top menu and clicking on

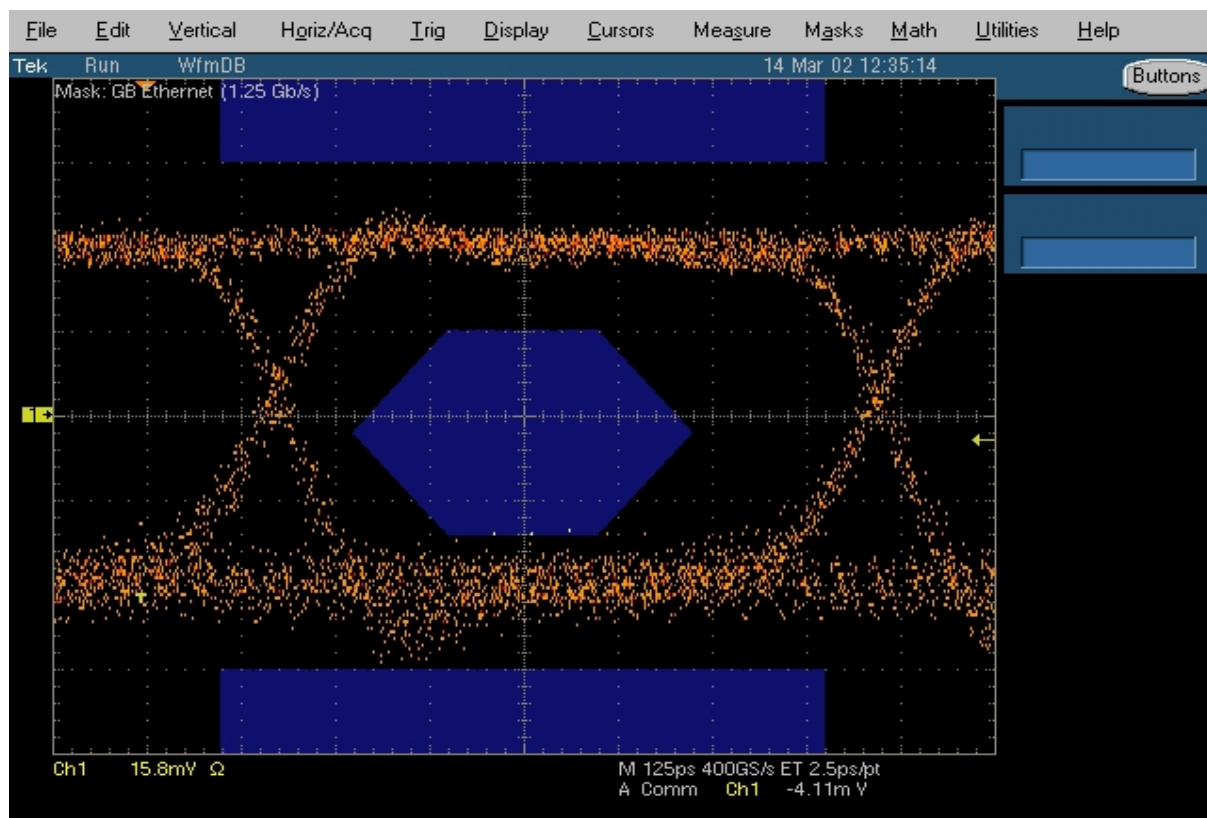"eye". Finally, an open eye was captured as shown in Figure 16.

Figure 16. Initial Maxim board eye diagram.

The only major concern of this eye diagram was the somewhat significant overshoot found at the bottom. After speaking with the professors, it was determined that this could possibly be caused by inductance from the board or noise caused by the power supply.

OE Modules

The next step in this project involved testing the Maxim board with the laser group and verifying proper operation by obtaining an eye diagram. However, we noticed that in order to drive the laser via the SMA connector (J15) on the Maxim board, it would need to be ac-coupled. Figure 17 shows a schematic of the modifications made to the Maxim board.
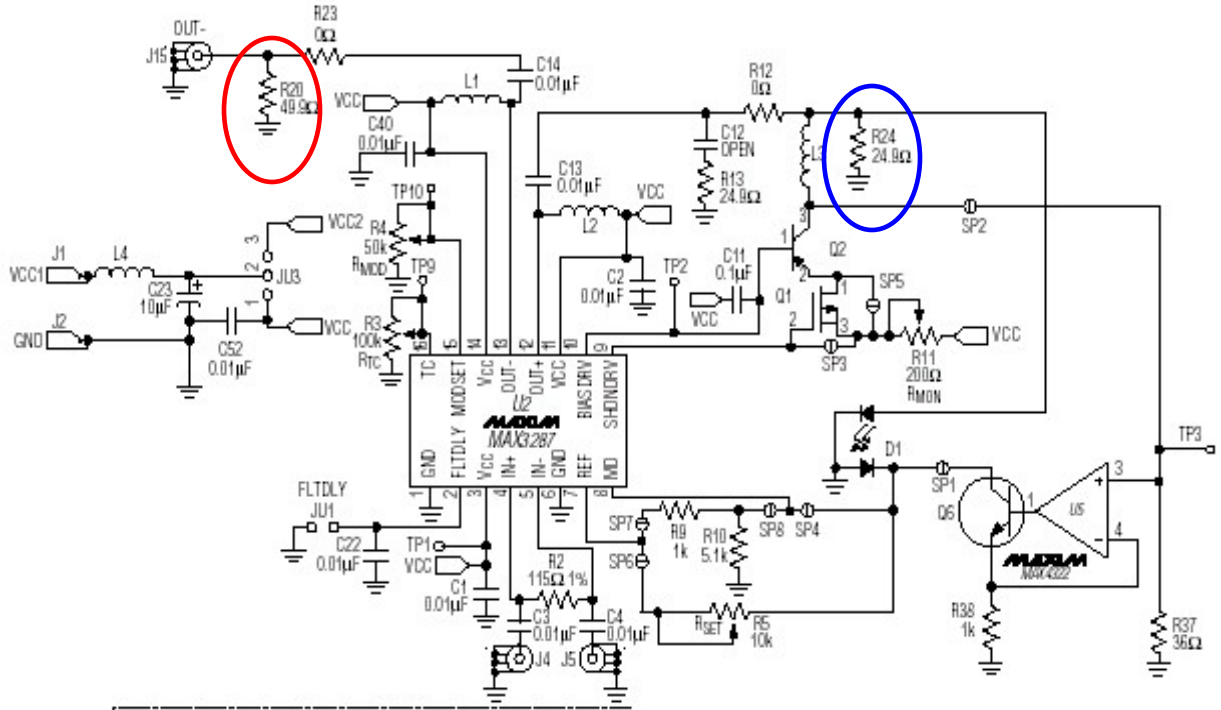
Figure 17. Modifications to original Maxim circuit layout [6].

In order to ac-couple the Maxim board, R24 (24.9Ω - pictured in blue) would need to be replaced

with the 49.9Ω resistor found at R20 (pictured in red). This, in turn, would correctly terminate

pin12 (OUT+) of the Maxim 3287 chip with a 49.9Ω resistor. The laser group, on the other

hand, agreed to provide a 49.9Ω termination on their board; therefore, R20 was removed from

the Maxim board. However, while trying to remove R20, the resistor popped off the board and

was lost. Since there were no 49.9Ω resistors in the laboratory, a 47Ω resistor was used to

terminate pin 12 (OUT+). Once these modifications were made, another eye diagram shown in

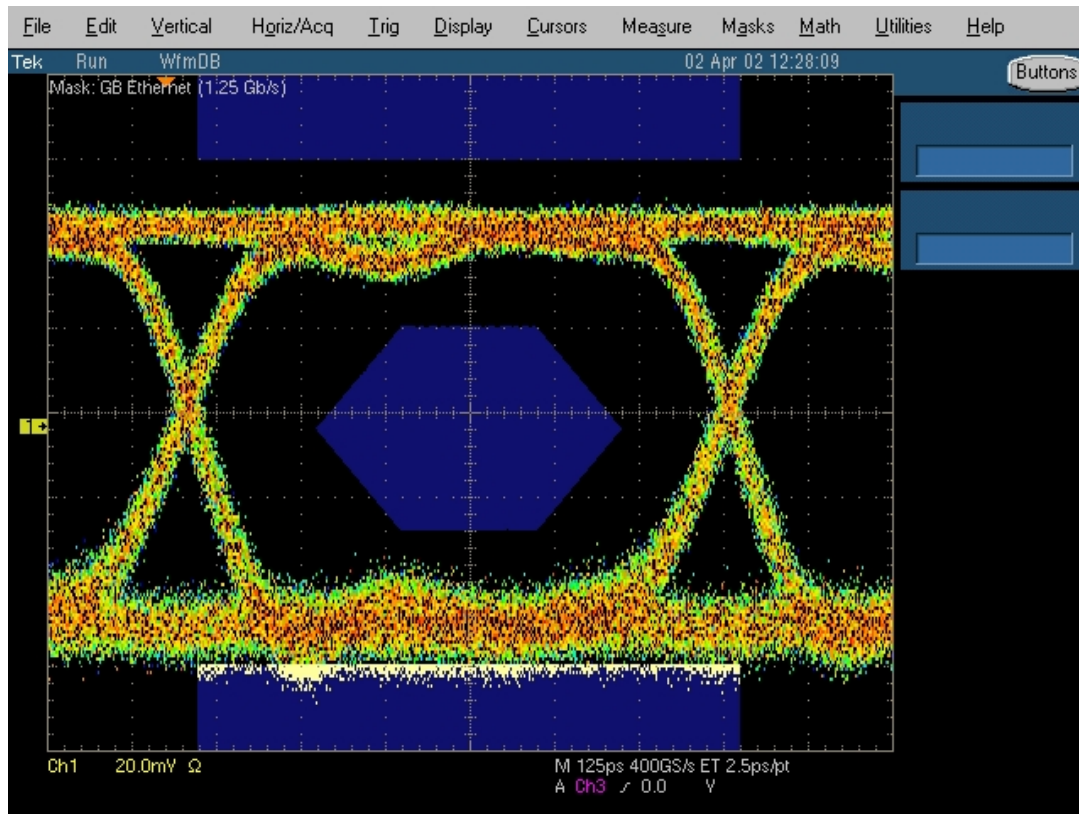Figure 18 was obtained using the same setup shown in Figure 14.

Figure 18. AC-Coupled Maxim board eye diagram.

There are some notable differences between the ac-coupled and dc-coupled eye diagrams. For instance, the overshoot found at the bottom of the dc-coupled eye is much smaller on the ac-coupled eye. However, the ac-coupled eye contains a small undershoot at the top which was not there before. This could possibly be due to using a 47Ω resistor to terminate pin 12 (OUT+), instead of using the required 49.9Ω termination.

The next step would involve connecting the Maxim board with the laser and OE module as shown in Figure 19
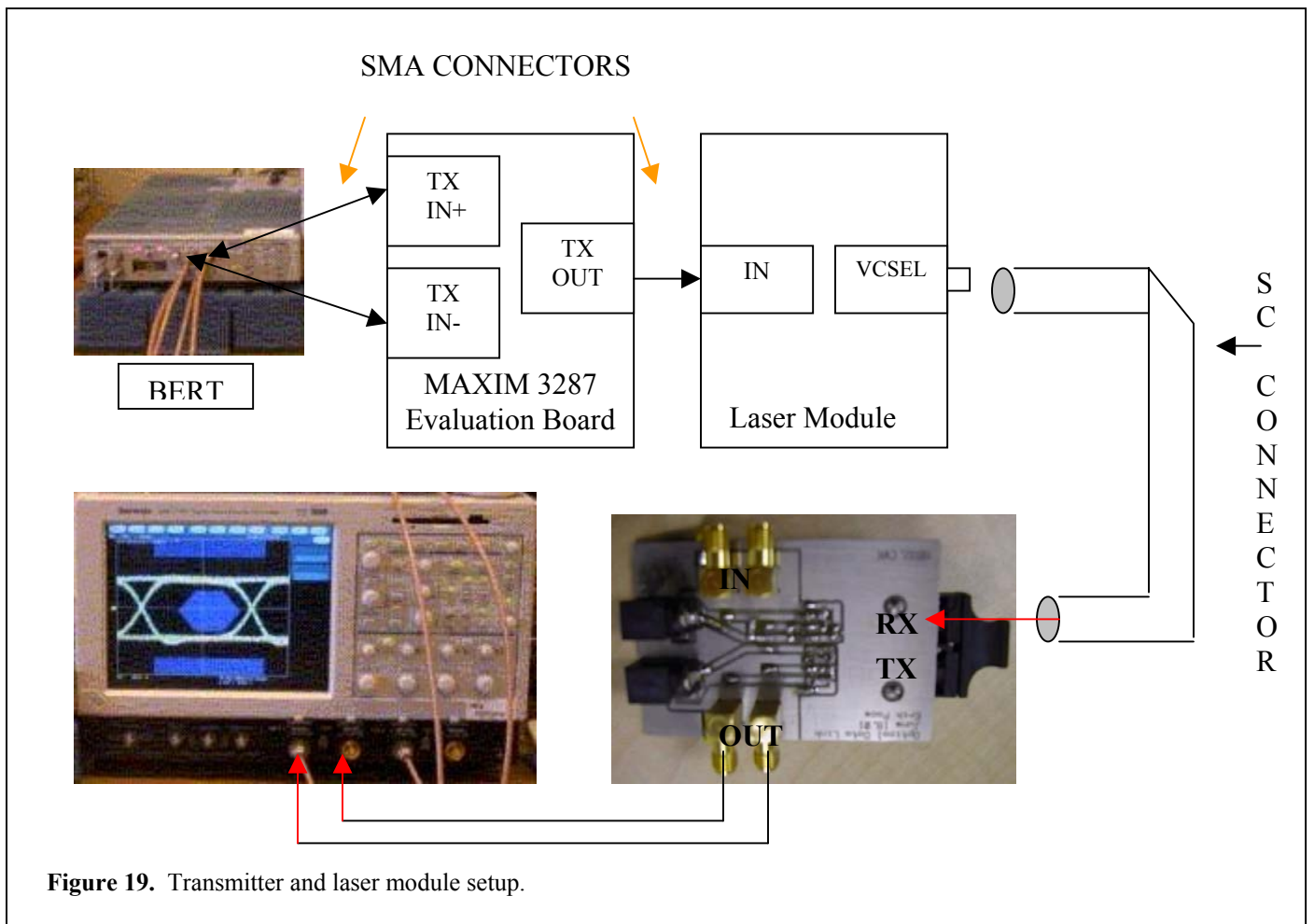
Figure 19. Transmitter and laser module setup.

The connections between the BERT, Maxim board, and laser module are done via SMA

connectors; while, an SC connector is used to connect the VCSEL to the OE module. The

outputs of the OE module are then connected to channels 1 and 2 of the oscilloscope,

respectively. It is not really necessary to connect both outputs unless an eye diagram is desired

on each of the differential outputs. Therefore, one output channel should be enough to obtain an

eye diagram. Again, the sync output of the BERT should be used to set the trigger on the

oscilloscope. Due to some unforeseen circumstances, an eye diagram could not be done because

the laser module was missing from the laboratory. The laser group was not able to construct

another working module; thus, the eye was never obtained. However, we are confident that our

board would have provided an open eye because the previous test with the ac-coupled Maxim

board yielded an open eye.

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Newly Designed Board

Finally, the last part of the project involved building and testing our newly designed board. The greatest difficulty in making our own board involved soldering the MAX3287 chip to the board. The appropriate tools for these types of surface mounts were not available. As a matter of fact, we had one the lab TA's grind a soldering tip and carefully mount the chip on the board. In addition, the soldering iron could only rest on top of each pin for 10 seconds at 550° F. If it were left on for a longer period of time, the chip would have to be discarded. Also, since each of the pins were very close together, a small amount of solder would easily spill over to the next pin, causing an undesirable short circuit. When this occurred, the solder would have to be removed using solder wick. The only problem with this was that the traces on the board began to lift off along with the solder. These pins would then be connected to the traces via a small metallic wire as shown in Figure 20 by the solid red arrows.
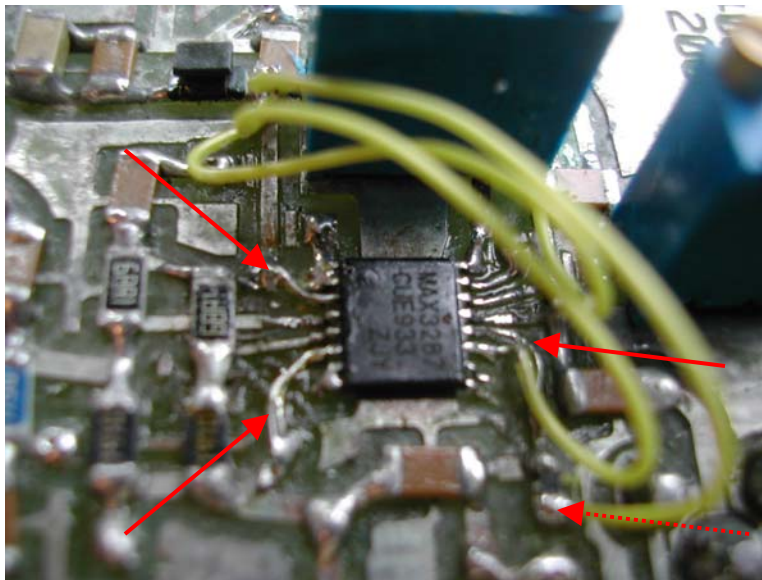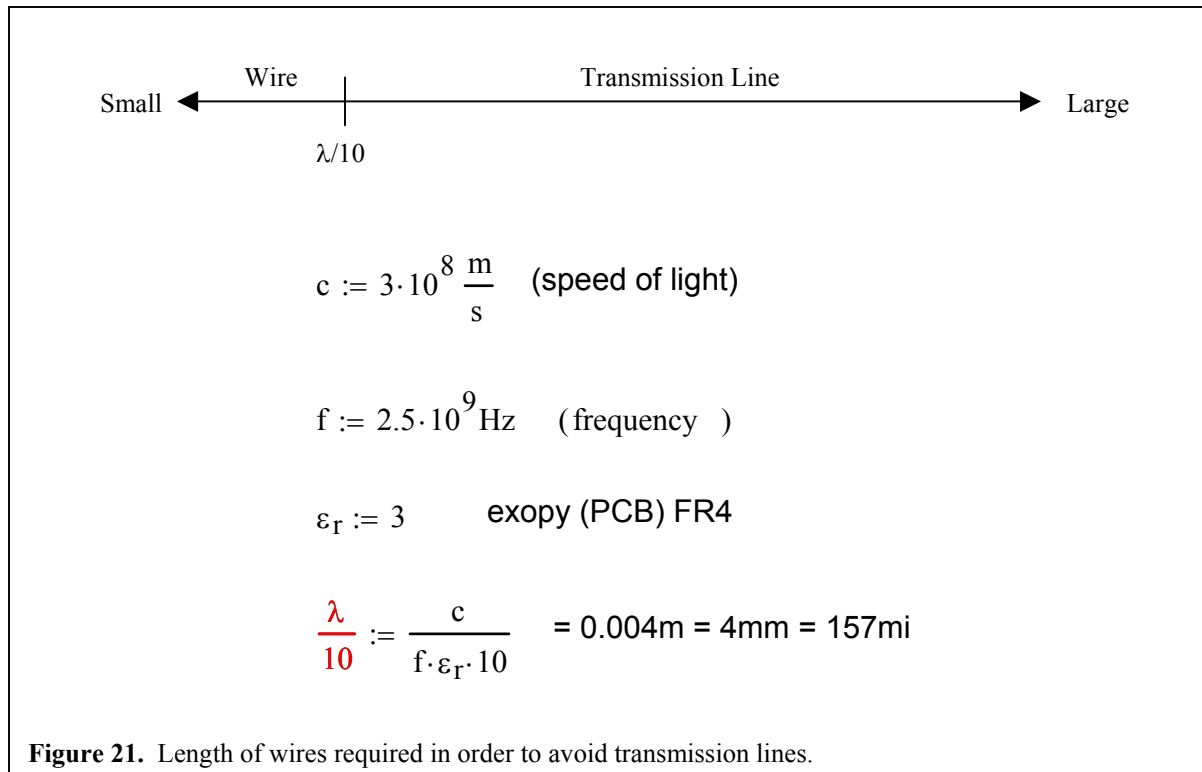

Figure 20. Fixes performed on newly designed board.

In order not to run into transmission line problems, these wires could not be longer than 4mm or 157mi. Figure 21 illustrates how these values were calculated.

Figure 21. Length of wires required in order to avoid transmission lines.

According to Professor Brooke, any wire approximately greater than 1/10 of a wavelength (λ) would act as a transmission line. Therefore for this reason, it was imperative for us to keep our wires less than this distance. Since our transmission rate was 1.25 Gbps, the highest possible frequency of a square wave would be 500 MHz (1.25 Gbps / 2 bits). In order to obtain at least 5 harmonics of a square wave, the frequency must be equal to $2.5*10^9$ Hz (5*500MHz). The index of refraction, ε_r, for an exopy board is approximately equal to 3. Thus, the length of the wire can be no longer than 4mm.

While preparing the board, some errors in our design were pointed out by Professor Brooke. Therefore, some minor modifications had to be made to our board design. Figure 22 illustrates the new modifications.

Figure 22. Circuit layout with slightly new modifications.
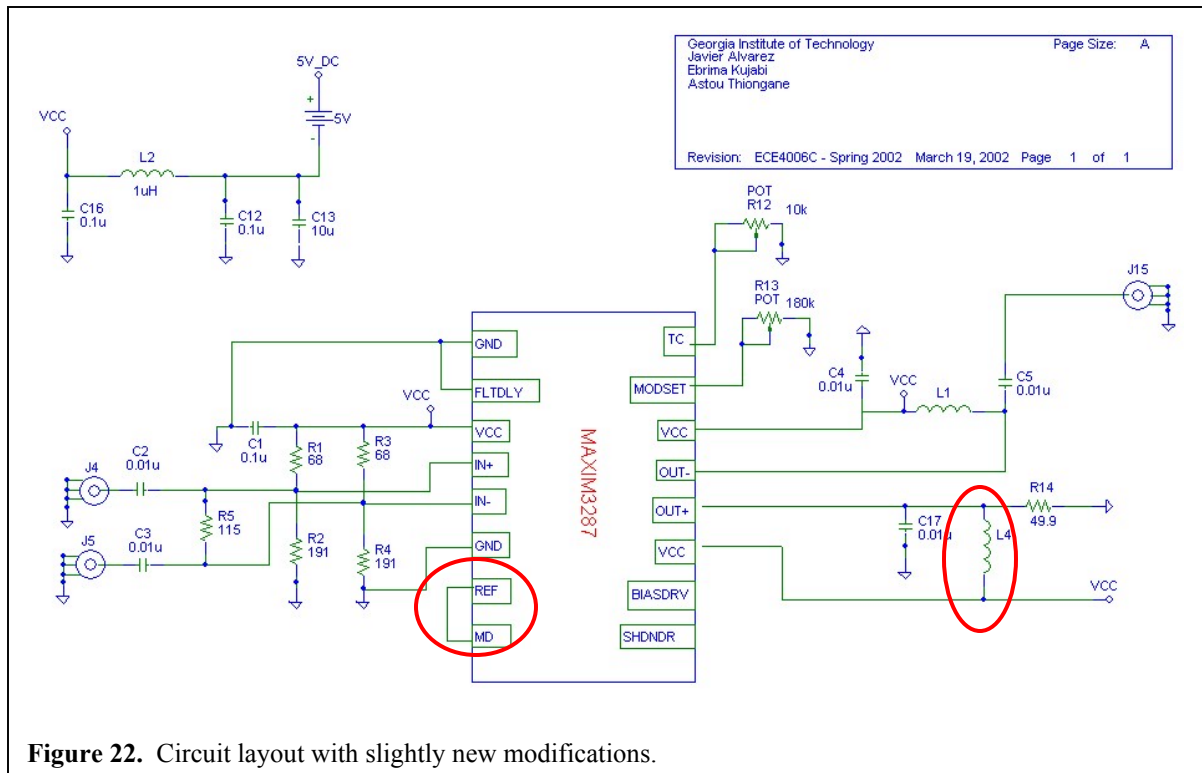
One of the problems was easily fixed by soldering pins 7 and 8 together. According to the

Maxim specification sheets, these pins should be connected if the APC (Automatic Power

Control) was to be disabled. The second modification to the board involved L4 (a ferrite bead).

This inductor was not connected to VCC before. Instead, the other end of the inductor was

connected to the 49.9Ω resistor. In order to fix this, the trace between the inductor and resistor

was removed. Then, the end of the inductor was connected to VCC via a yellow jumper cable as

shown in Figure 6 by the dotted arrow. The 49.9Ω resistor was then attached to the capacitor

(C17) via a small metallic wire. Even though the laser was not going to be driven via pin 12

(OUT+), it was still necessary to keep the same symmetry between pins 11, 12 and pins 13, 14

for proper operation. Once these errors had been fixed, we began testing our board using the

same setup configuration shown in Figure 14. Little to our surprise, we did not get any output

from our board whatsoever. After analyzing the board, we discovered that the bottom traces of

the board were not connected to the top traces. Therefore, we placed a small wire through the

vias on the board and soldered each end to the traces. Again, there was no output from our

board. In order to make sure that everything was connected properly, we began checking our

board for continuity with a Fluke meter. It was determined that the SMA Connectors were not

making any contact with the board. Therefore, we connected the center pin of the SMA

connector from underneath the board to the signal path above via a long insulated cable. This,

however, gave us a problem with transmission lines. After reconsidering this fix, we decided to

flip over the SMA connectors and solder the pins directly to the signal path as shown in Figure
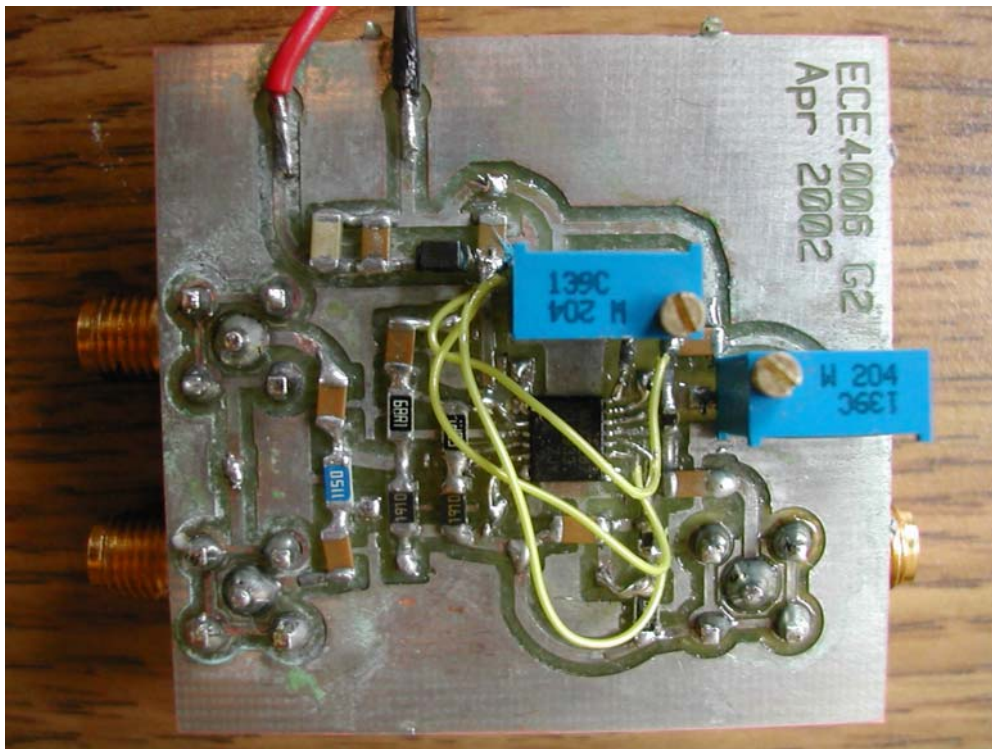
23.

Figure 23. Final board design with all fixes.

Finally, we connected the board to the BERT and the oscilloscope to obtain an eye diagram. The

BERT contains several different bit patterns that it can generate. We began by trying to obtain

an eye diagram with the pseudo-random bit option selected, but the output was not very clear.

However for a simple square wave (D215), we were able to obtain an open eye as shown in Figure 24.

Figure 24. Eye diagram of newly designed board using a square input.
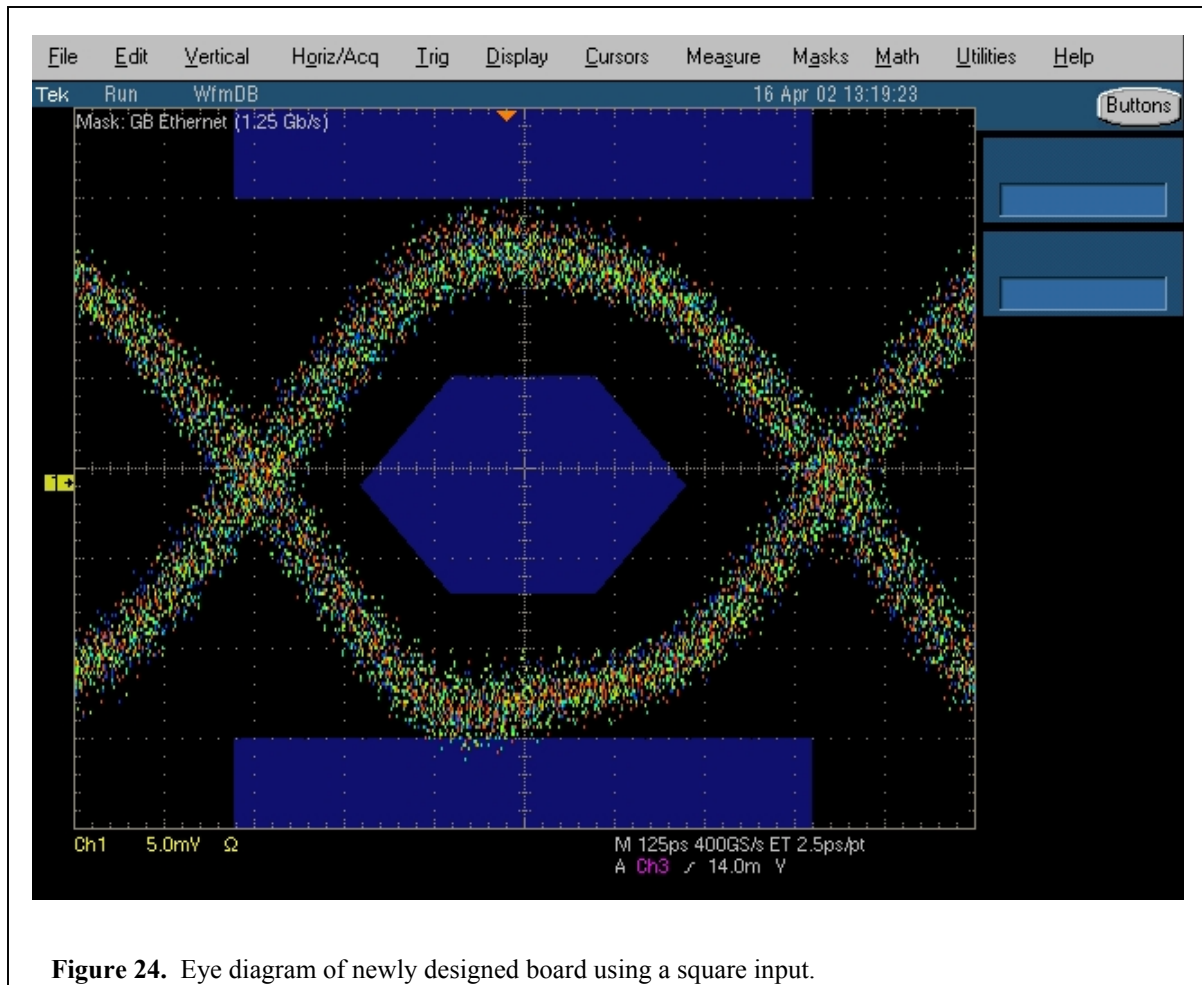
This clearly indicated several things. Most importantly, it indicated that the board was functioning the way it was supposed to. However, it also indicated that the problems with the board were probably attributed to transmission lines. The most suspicious transmission line would have to be the wires connecting the Maxim chip pins to the traces. Since these wires lie in the signal path, we assume that this is the major contributor to noise. Besides these metallic wires, there are some yellow insulated cables running VCC to several different areas on the board. These slight modifications can be easily fixed by redesigning the board to accommodate these fixes.

References

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