AN5020

Interfacing LVDS, LVPECL, CML, HCSL/LPHCSL

1.0 INTRODUCTION

When dealing with high-speed signaling, interconnects between components must be treated as transmission lines. Additionally, line termination must be considered with special care to avoid impedance mismatching and line discontinuities, which can lead to signal reflections and performance degradation.

This application note gives an overview of different transmission line termination techniques to interface between devices with similar or different I/O technologies (LVPECL, LVDS, CML, HCSL, LP-HCSL).

Proper line termination should maintain impedance matching and provide the right signal translation to avoid I/O incompatibilities which can lead to device malfunction, eventual reliability issues, and—in the worst case scenario—devices damage.

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2.0 DC COUPLING VS. AC COUPLING

DC coupling offers the advantage over AC coupling of less components count and less power consumption. However, while DC coupling, devices from different vendors or devices of different technology I/Os compatibility between driver's output signal level and receiver's input signal level range is not always guaranteed and, in some cases, comes with the price of adding more components with increase in power consumption and in many cases DC coupling is not possible at all leaving AC coupling as the only solution.

AC coupling blocks the DC bias between the driver's output and the receiver's input thus eliminating the issue of common mode voltage incompatibility between them. The receiver's input can then be biased at the optimum levels that offers the best performance in terms of jitter, duty cycle distortion, and crossing. While there is no issue with AC coupling clock signals, AC coupling data signals requires that the data be DC-balanced (same overall number of zeros and ones) to avoid signal decay, in the absence of transitions (during long chains of identical bits), at the two ends of the receiver termination to the same level, which will reduce noise margin.

3.0 DRIVER OUTPUT/RECEIVER INPUT VOLTAGE LEVEL

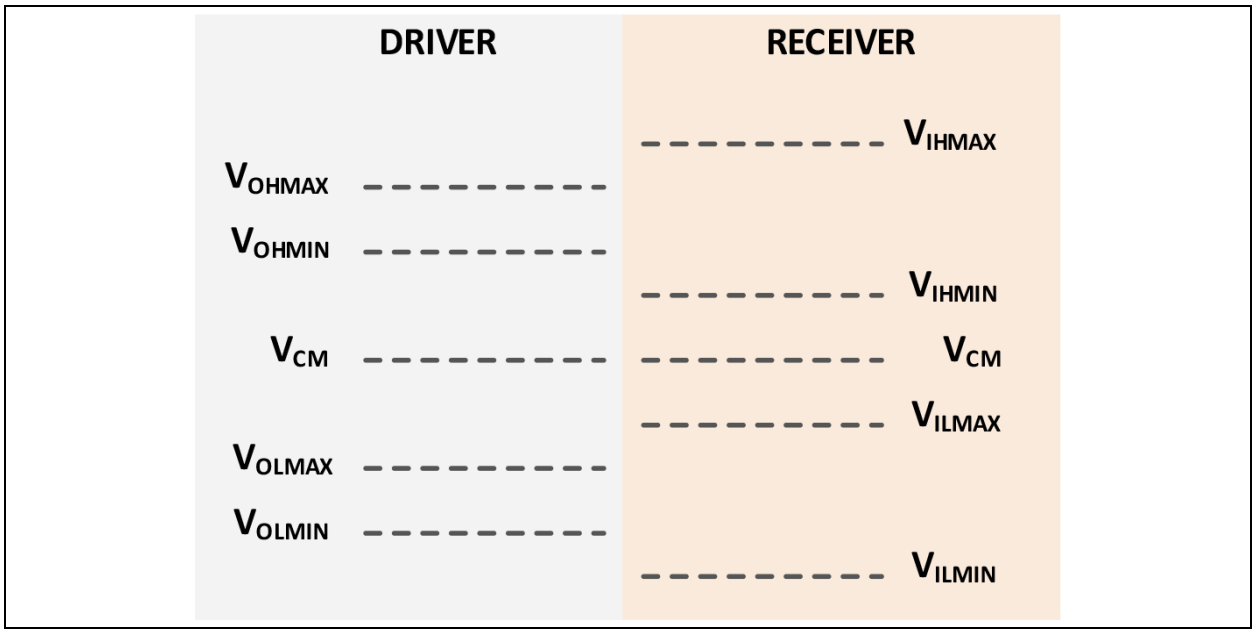

FIGURE 1: DRIVER'S OUTPUT AND RECEIVER'S INPUT VOLTAGE LEVEL.

Figure 1 shows the case where the driver's output and the receiver's input have the same common mode voltage and the driver's output signal levels fall within the receiver's input signal level range. This is the case we face when interfacing devices with the same logic especially when they are from the same manufacturer. It is the ideal case for DC coupling between the two devices.

Unfortunately, that's not always the case and sometimes even interfacing between devices of the same logic from different manufacturers requires special care when DC coupling. When the gap between the common mode voltage of the receiver's input and the common mode of the driver's output is too large, DC coupling becomes impossible, and AC coupling must be used to keep the driver and receiver at their sweet spots of operation. Figure 2 shows operating levels of most Microchip SYxxx products family that we'll be referring to in this application note.

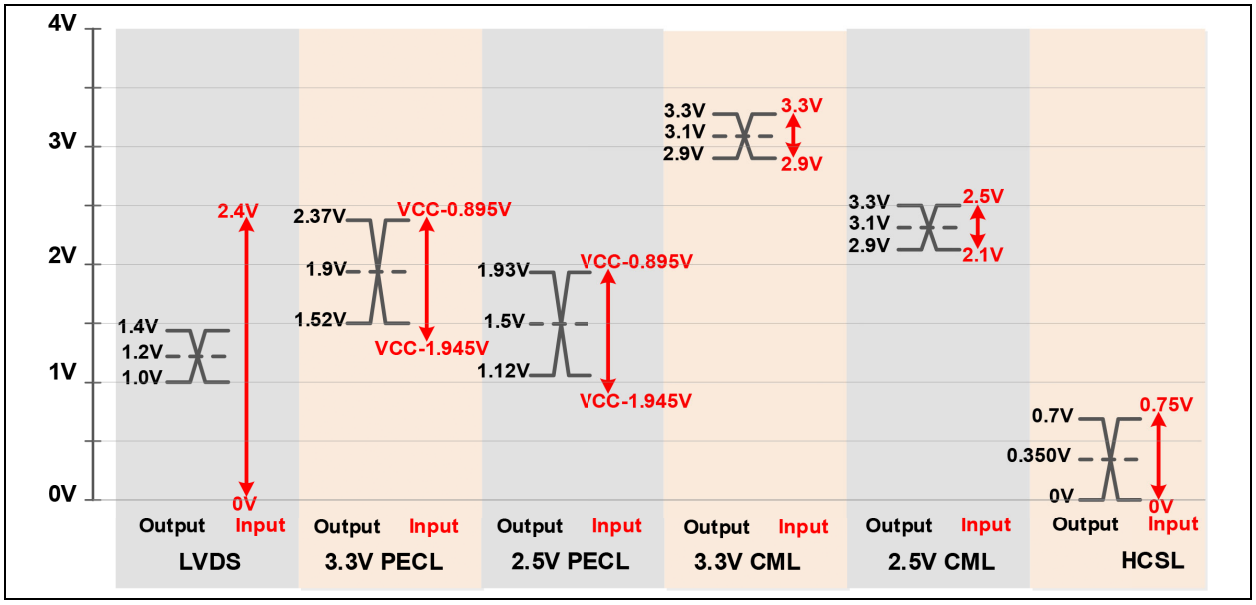

FIGURE 2: DIFFERENT I/O TECHNOLOGY INPUT/OUTPUT LEVELS.

4.0 DC COUPLING

4.1 DC Coupling LVDS Driver

4.1.1 DC COUPLING LVDS DRIVER TO LVDS RECEIVER

Just connect the LVDS output to the LVDS input and if the receiver doesn't have internal termination terminate with external 100Ω differential close to the receiver input.

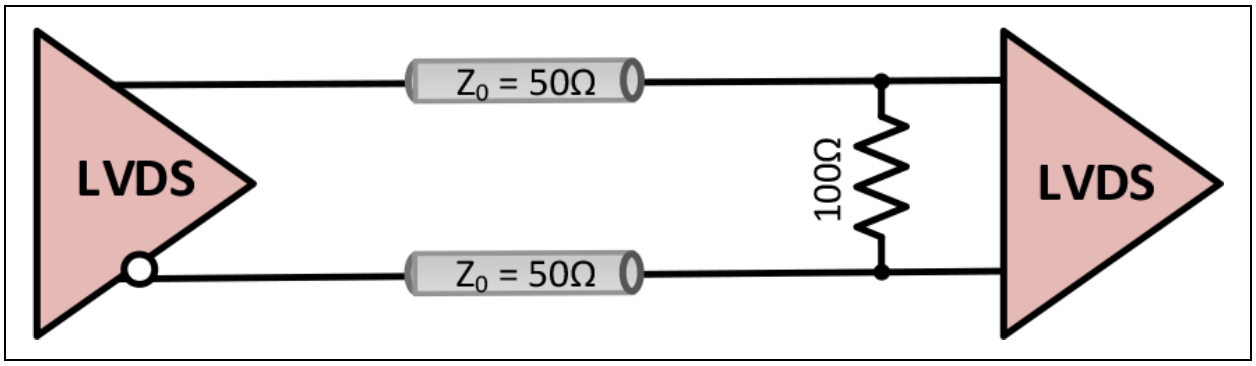

FIGURE 3: RECEIVER WITHOUT INTERNAL TERMINATION.

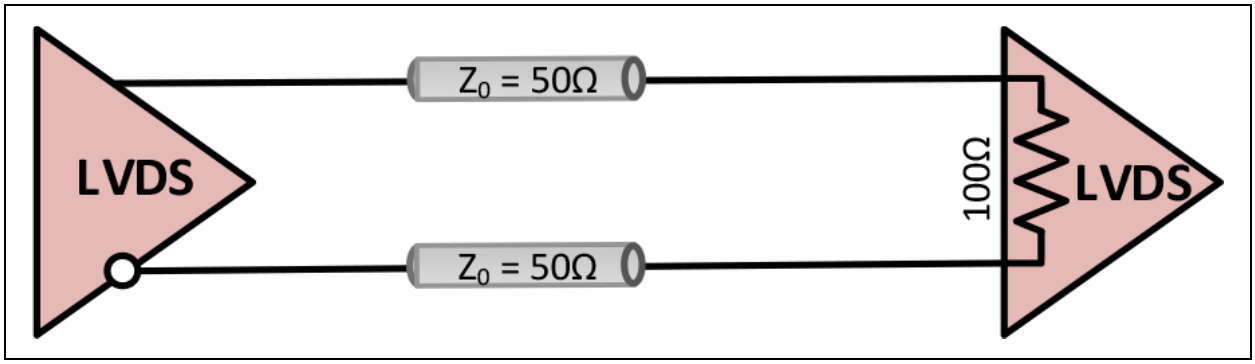

FIGURE 4: RECEIVER WITH INTERNAL TERMINATION.

4.1.2 DC COUPLING LVDS DRIVER TO LVPECL RECEIVER

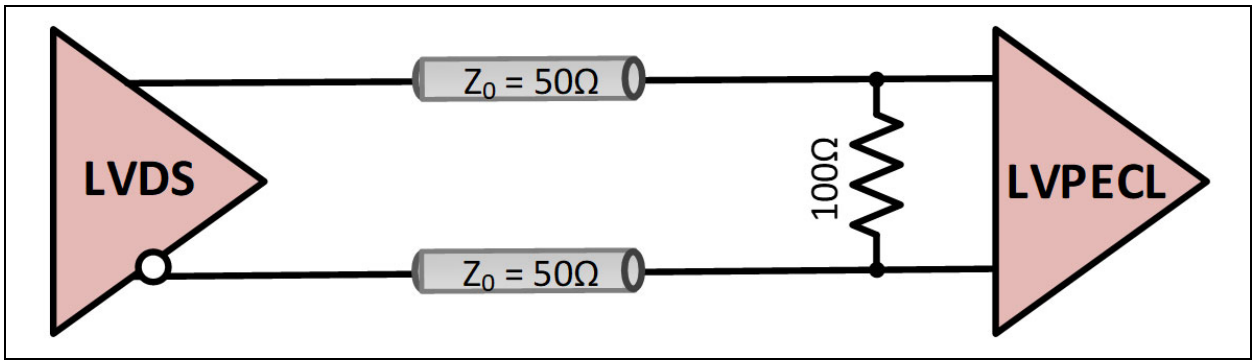

FIGURE 5: DC COUPLING LVDS TO LVPECL.

Even though the difference between the common mode voltage, 1.2V for LVDS vs VCC-1.3V for LVPECL, this circuit will work fine in most cases due to the wide common mode range of the LVPECL input and the relatively small swing of LVDS (400 mV) which will not cause the saturation of the LVPECL input stage current source.

Another solution to DC couple LVDS to LVPECL is to use a resistor network to shift the DC level from LVD common mode voltage (1.2V) to LVPECL common mode voltage (VCC-1.3V). This can be achieved using the circuit in Figure 6. Resistors values can be calculated from the following equations dictated by the circuit constraints:

LVDS common mode voltage at point A:

EQUATION 1:

$$\frac{R1}{R2+R3} \times V_{CC} = 1.2V$$

LVPECL common mode voltage at point B:

EQUATION 2:

$$\frac{R1+R2}{R1+R2+R3} \times V_{CC} = V_{CC} - 1.3V$$

EQUATION 3:

$$\left(\frac{R0}{2}\right) \parallel (R1 \parallel (R2 + R3)) = 50$$

Considering V_{CC} = 3.3V and solving Equation 1 and Equation 2 leads to R2 = 0.615R3 and R1 = 0.571 (R2 + R3). For R2 = 200Ω, R3 = 325Ω (324Ω normalized), and R1 = 299Ω (301Ω normalized). Then, Equation 3 leads to R0 = 136Ω (137Ω normalized).

Selecting high value resistors has the advantage of low power consumption while lower value resistors allow the circuit to perform better at higher frequencies.

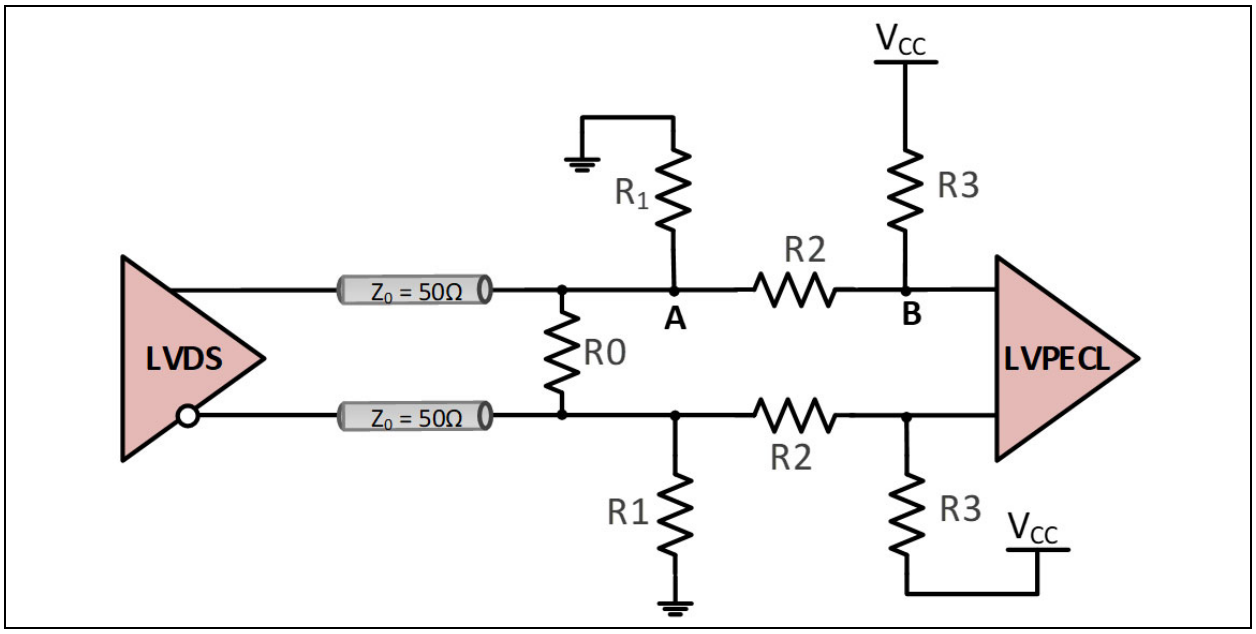

FIGURE 6: DC COUPLING LVDS DRIVER TO CML RECEIVER.

4.1.3 DC COUPLING LVDS DRIVER TO CML RECEIVER

Due to the large gap between the LVDS and CML common mode voltage it's not practical to DC couple LVDS driver to CML receiver and vice versa.

4.2 DC Coupling LVPECL Driver

4.2.1 DC COUPLING LVPECL DRIVER TO LVPECL RECEIVER

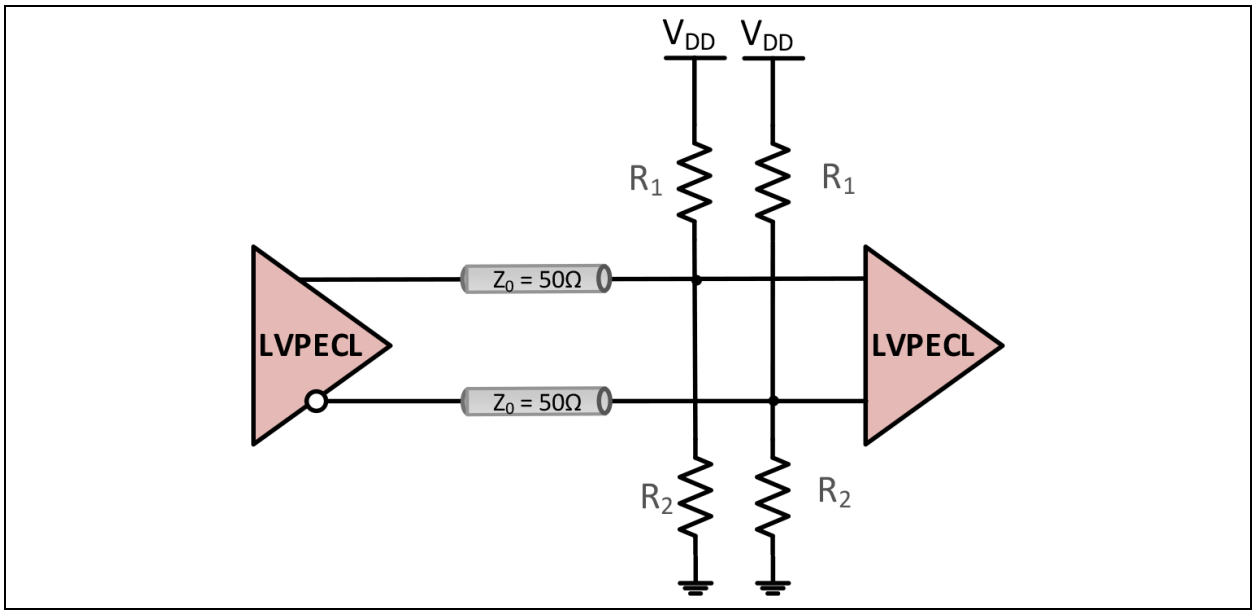

FIGURE 7: DC COUPLING LVPECL TO LVPECL.

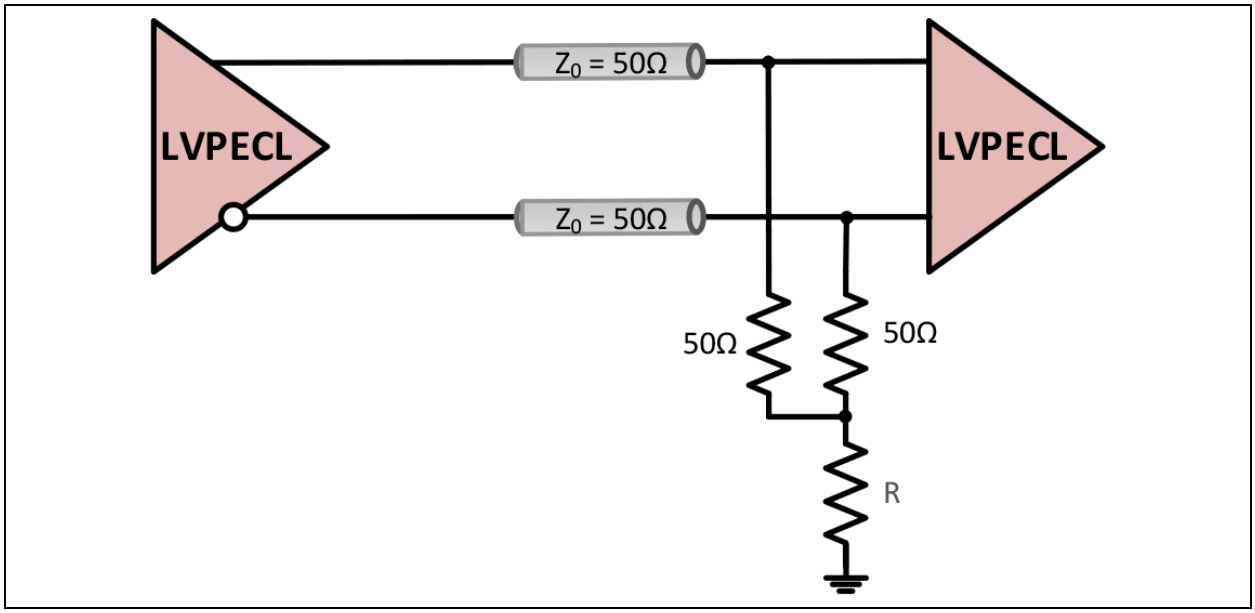

FIGURE 8: DC COUPLING LVPECL TO LVPECL.

In Figure 7, the Thevenin termination is equivalent to the 50Ω to V_{CC} - 2V standard LVPECL termination and satisfy Equation 4 and Equation 5.

EQUATION 4:

$$\frac{R1 \times R2}{R1 + R2} = 50$$

EQUATION 5:

$$\frac{R2}{R1+R2} \times V_{CC} = V_{CC} - 2$$

The R1 and R2 solutions are:

$$R1 = \frac{50 \times V_{CC}}{V_{CC} - 2}$$
$$R2 = 25 \times V_{CC}$$

For V_{CC} = 3.3V: R1 = 127Ω, R2 = 82.5Ω

In Figure 8, the value of R is calculated as follows:

The voltage at the node between R and the 50Ω is V_{CC} − 2V (PECL termination: 50Ω to V_{CC} − 2V) and the current flowing through R is the sum of the currents flowing through the two 50Ω termination resistors.

EQUATION 6:

$$I = \frac{V_{OH} - (V_{CC} - 2)}{50} + \frac{V_{OL} - (V_{CC} - 2)}{50}$$
$$I = \frac{(V_{OH} + V_{OL}) - (2V_{CC} + 4)}{50}$$

EQUATION 7:

$$R = \frac{V_{CC} - 2}{1} = \frac{50 \times (V_{CC} - 2)}{(V_{OH} + V_{OL}) - (2V_{CC} + 4)}$$

If we consider SY58012U as a driver, the following table shows R0 values for V_{CC} = 3.3V and 2.5V.

TABLE 4-1: RO VALUES FOR V_{CC} = 3.3V AND 2.5V

V_{CC}	V_{OH}	V_{OL}	R
3.3V	V_{CC} – 0.895V	V_{CC} – 1.695V	40Ω
2.5V			18Ω

4.2.2 DC COUPLING LVPECL DRIVER TO LVDS RECEIVER

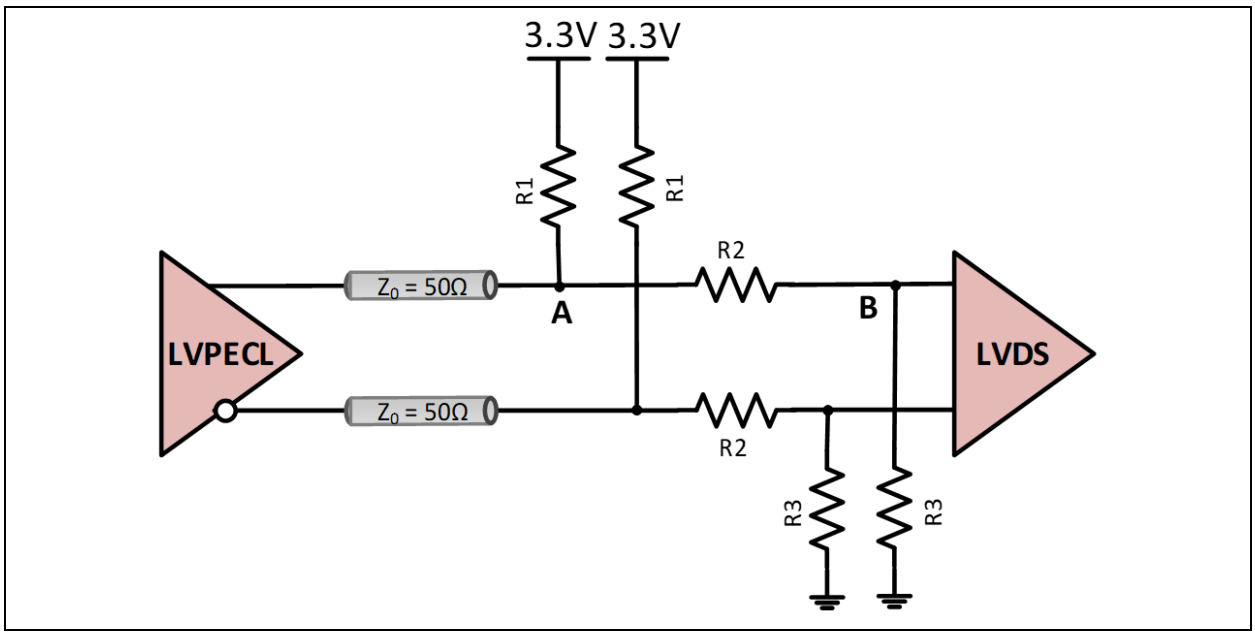

FIGURE 9: DC COUPLING LVPECL TO LVDS.

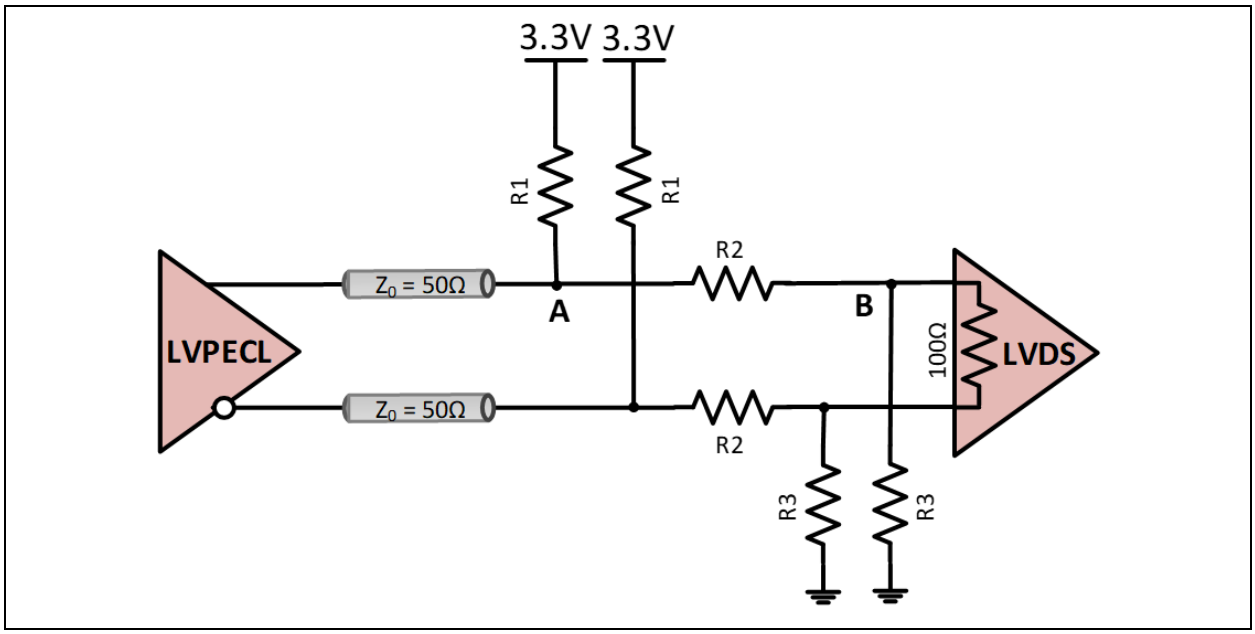

FIGURE 10: DC COUPLING LVPECL TO LVDS WITH INTERNAL DIFFERENTIAL 100Ω TERMINATION.

The voltages at nodes A and B in both Figure 9 and Figure 10 are:

- A: V_{CM} (LVPECL) = V_{CC} – 1.3V = 2V
- B: V_{CM} (LVDS) = 1.2V

In Figure 9, we have the following:

EQUATION 8:

$$(R2 + R3)/(R1 + R2 + R3) \times 3.3 = 2$$

EQUATION 9:

$$R3 \parallel (R1 + R2 + R3) \times 2 = 1.2$$

EQUATION 10:

$$R1 \parallel (R2 + R3) = 50$$

The values of R1, R2, and R3 satisfying Equation 8, Equation 9, and Equation 10 for Figure 9 are:

- R1 = 82.5Ω
- R2 = 51Ω
- R3 = 75.8Ω

In Figure 10, where the receiver has internal differential 100Ω termination, we have:

EQUATION 11:

$$(R2 + R3)/(R1 + R2 + R3) \times 3.3 = 2$$

EQUATION 12:

$$(R3)/(R1 + R2 + R3) \times 2 = 1.2$$

EQUATION 13:

$$R1 \parallel (R2 + R3 \parallel 50) = 50$$

The values of R1, R2, and R3 satisfying Equation 11, Equation 12, and Equation 13 for Figure 10 are:

- R1 = 102Ω
- R2 = 63.4Ω
- R3 = 95.3Ω

4.2.3 DC COUPLING LVPECL DRIVER TO CML RECEIVER

It is not recommended to DC couple LVPECL to CML unless AC coupling cannot be used due, for example, to unbalanced data. In this case, the diagram in Figure 11 can be used. From the LVPECL output, the resistor network is seen as a Thevenin termination with 82.5Ω to GND and 208 // (275 + 50) = 127Ω to VCC. The CML input is biased with the 50Ω to VCC.

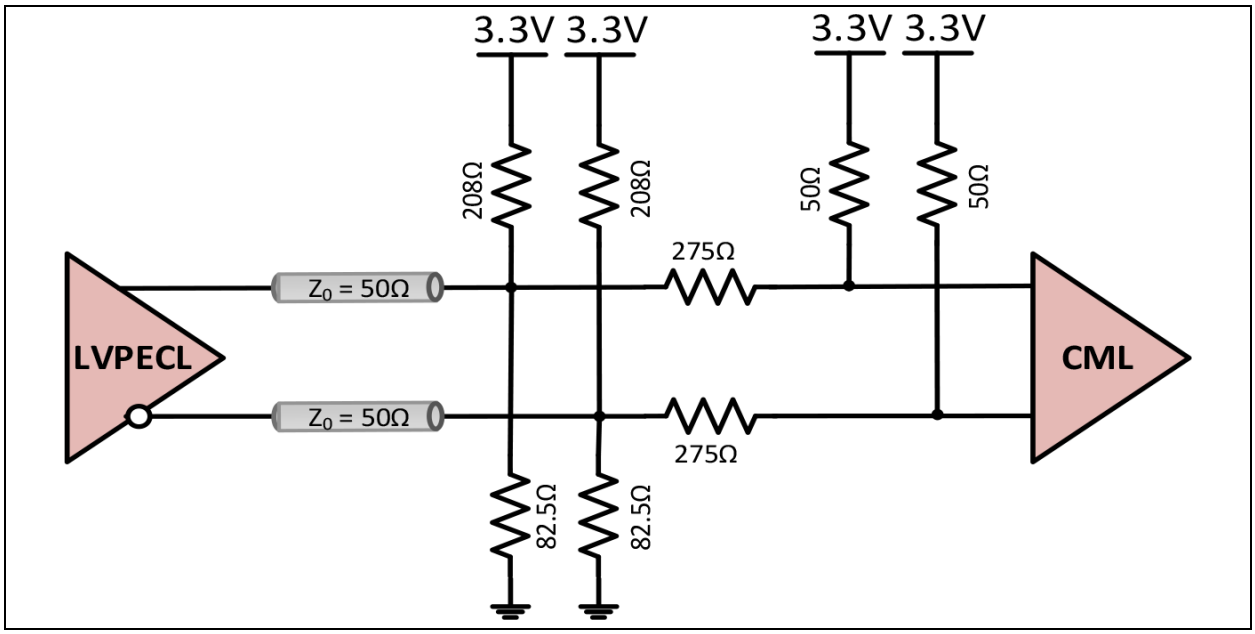

FIGURE 11: DC COUPLING LVPECL TO CML.

4.3 DC Coupling CML Driver

4.3.1 DC COUPLING CML DRIVER TO CML RECEIVER

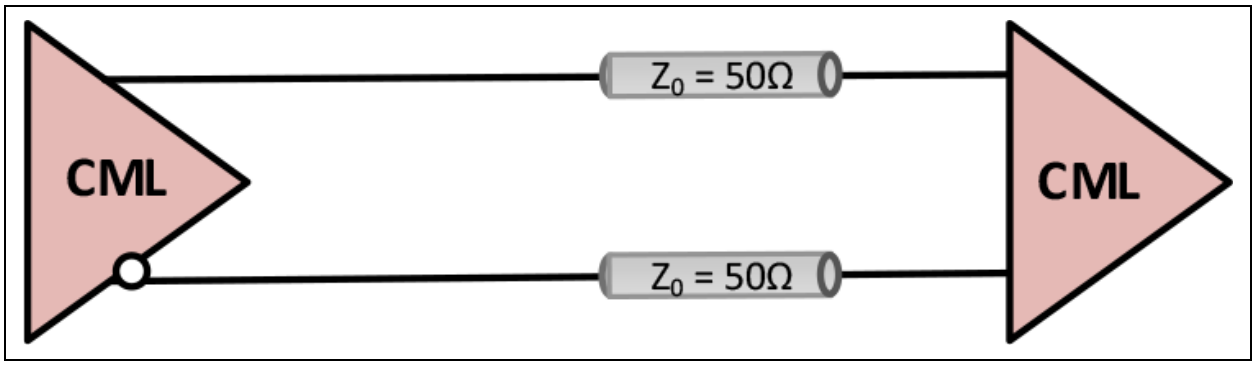

FIGURE 12: DC COUPLING CML TO CML (DRIVER WITH INTERNAL TERMINATION).

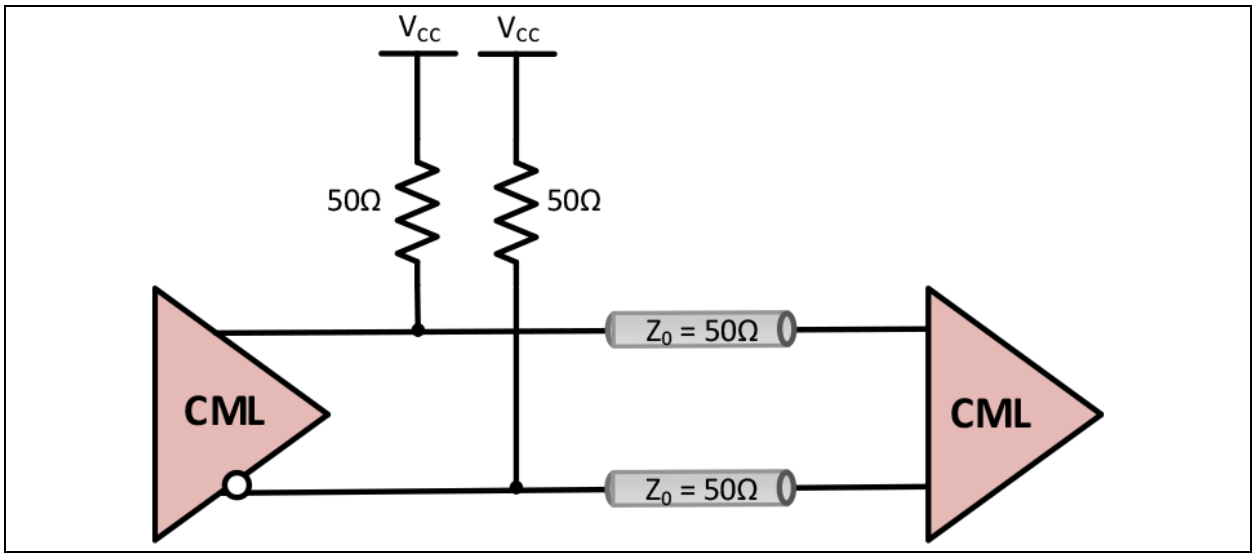

FIGURE 13: DC COUPLING CML TO CML (DRIVER WITHOUT INTERNAL TERMINATION).

Due to the high common mode voltage of the CML driver (V_{CC} – 200 mV), it's difficult if not impossible to DC couple the CML driver to other logics.

4.4 DC Coupling HCSL/LPHCSL Driver

4.4.1 DC COUPLING HCSL/LPHCSL DRIVER TO HCSL RECEIVER

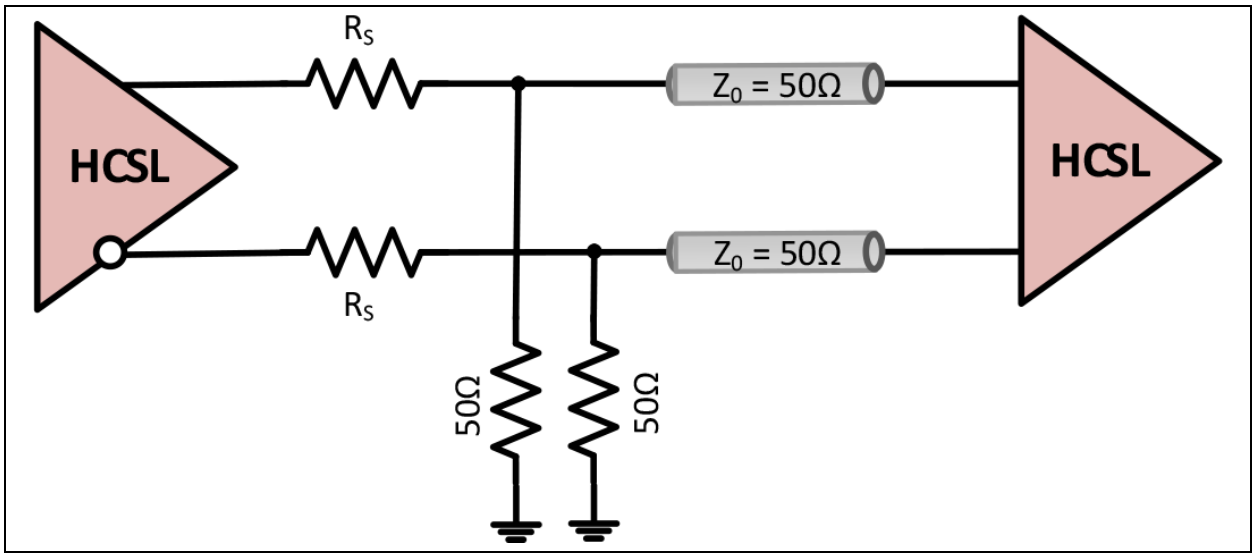

FIGURE 14: DC COUPLING HCSL TO HCSL.

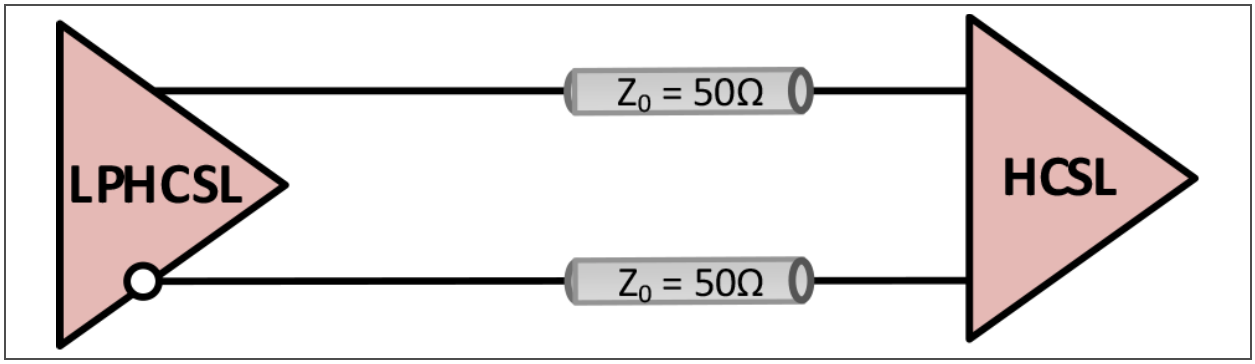

FIGURE 15: DC COUPLING LPHCSL TO HCSL.

LPHCSL doesn't require the 50Ω termination to GND necessary for the HCSL driver, which needs a path to ground.

Due to the low common mode voltage of the HCSL/LPHCS driver (250 mV – 55 mV), it's difficult if not impossible to DC couple the HCSL/LPHCSL driver to other logics.

5.0 AC COUPLING

5.1 AC Coupling LVDS Driver

5.1.1 AC COUPLING LVDS DRIVER TO LVDS RECEIVER

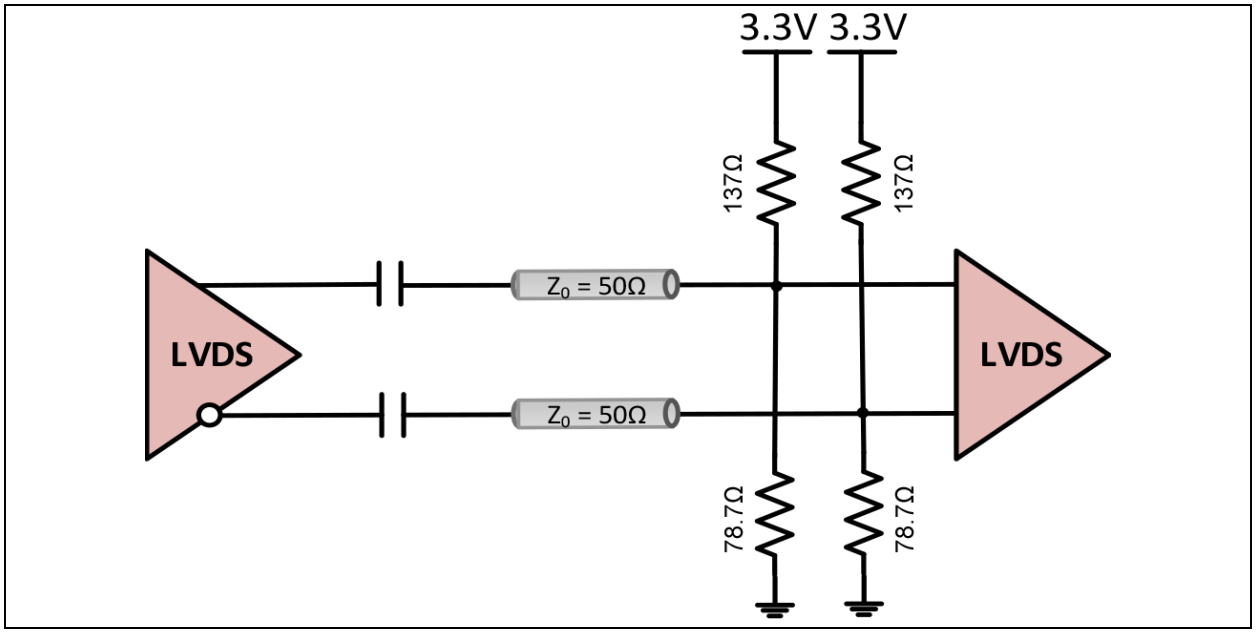

FIGURE 16: AC COUPLING LVDS TO LVDS.

For an LVDS receiver without internal termination, the termination network in Figure 16 sets the appropriate termination at the receiver input and sets the LVDS input common mode voltage (1.2V). If the receiver has internal termination, the external network used to generate the common mode voltage (1.2V) should use high value resistors to preserve the transmission line termination (100Ω differential). In Figure 17, the 5.1KΩ and 9.1KΩ resistor values set the common mode voltage to 1.2V.

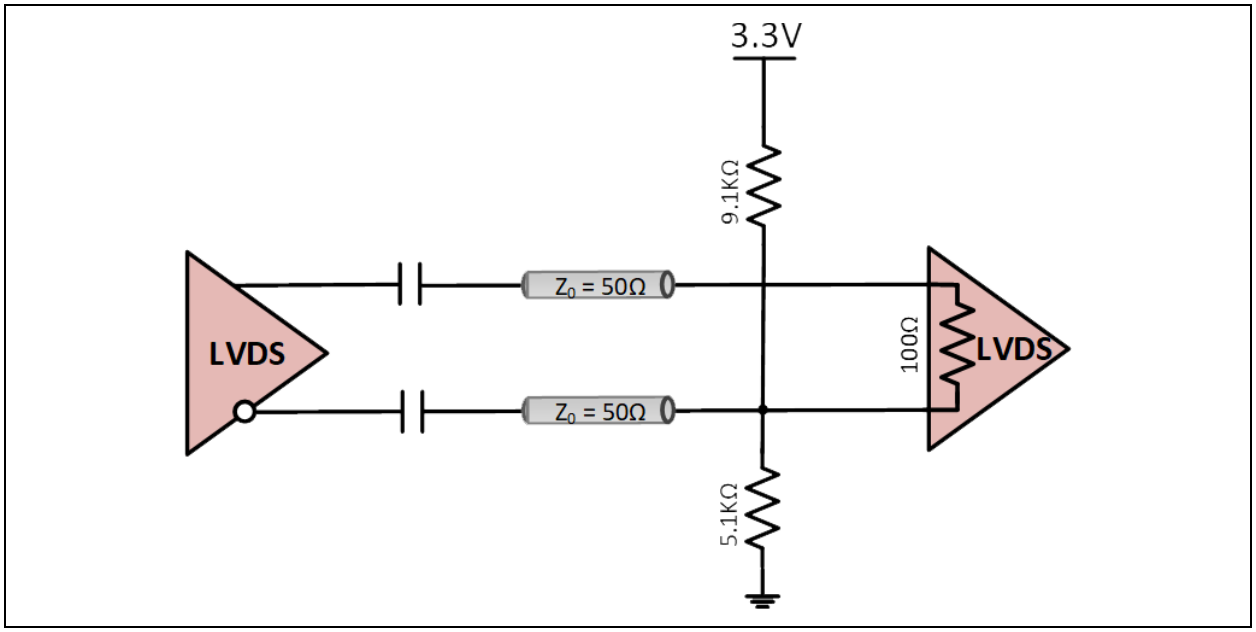

FIGURE 17: AC COUPLING LVDS TO LVDS (RECEIVER WITH INTERNAL TERMINATION).

5.1.2 AC COUPLING LVDS DRIVER TO LVPECL RECEIVER

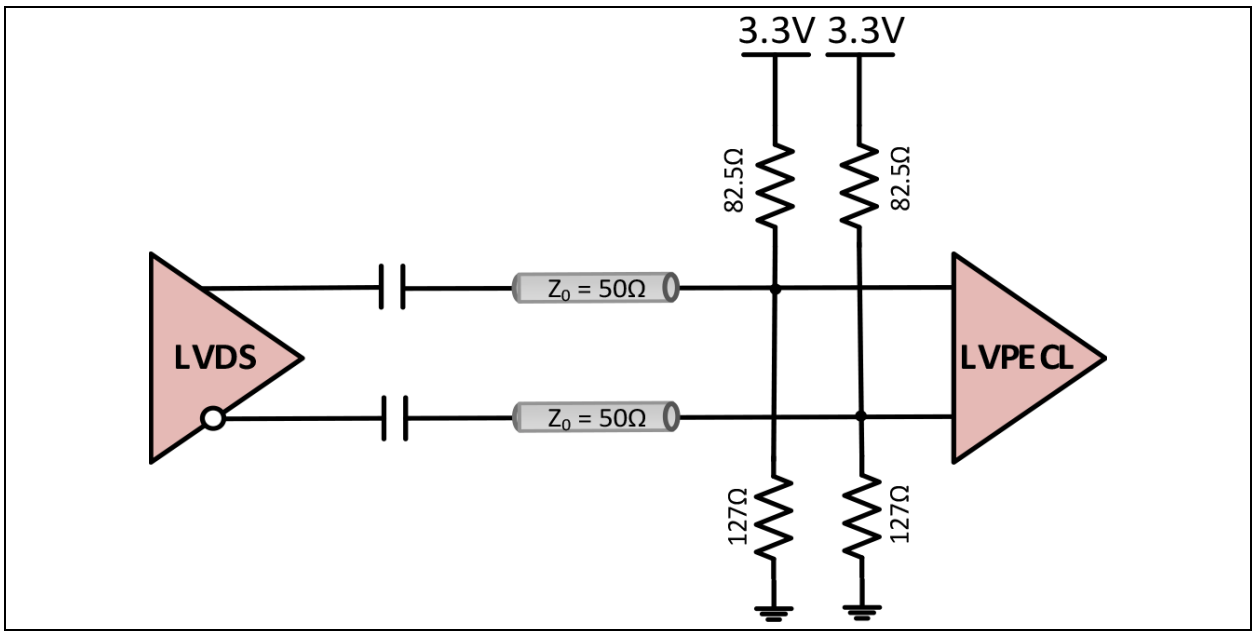

FIGURE 18: AC COUPLING LVDS TO LVPECL.

The termination network in Figure 18 restores the LVPECL input common mode voltage (VCC – 1.3V = 2V) and provide 50Ω line termination (100 differential). If the receiver has a VBB (2V) bias source, just terminate each input with a 50Ω to VBB. To interface to Microchip SYxxx products with “Any IN Input” with internal 50Ω termination to VT and VREF_AC pin, just connect the VT pin to the VREF_AC pin.

5.1.3 AC COUPLING LVDS DRIVER TO CML RECEIVER

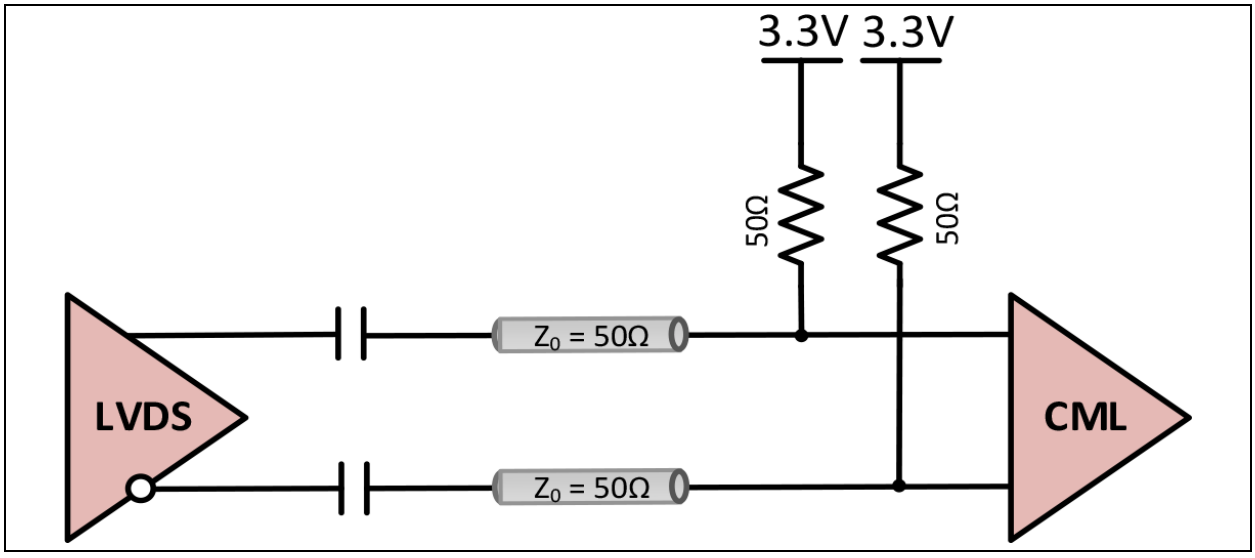

FIGURE 19: AC COUPLING LVDS TO CML.

The 50Ω resistors provide the bias to the CML input and the 100Ω differential termination to the LVDS driver.

5.1.4 AC COUPLING LVDS DRIVER TO HCSL RECEIVER

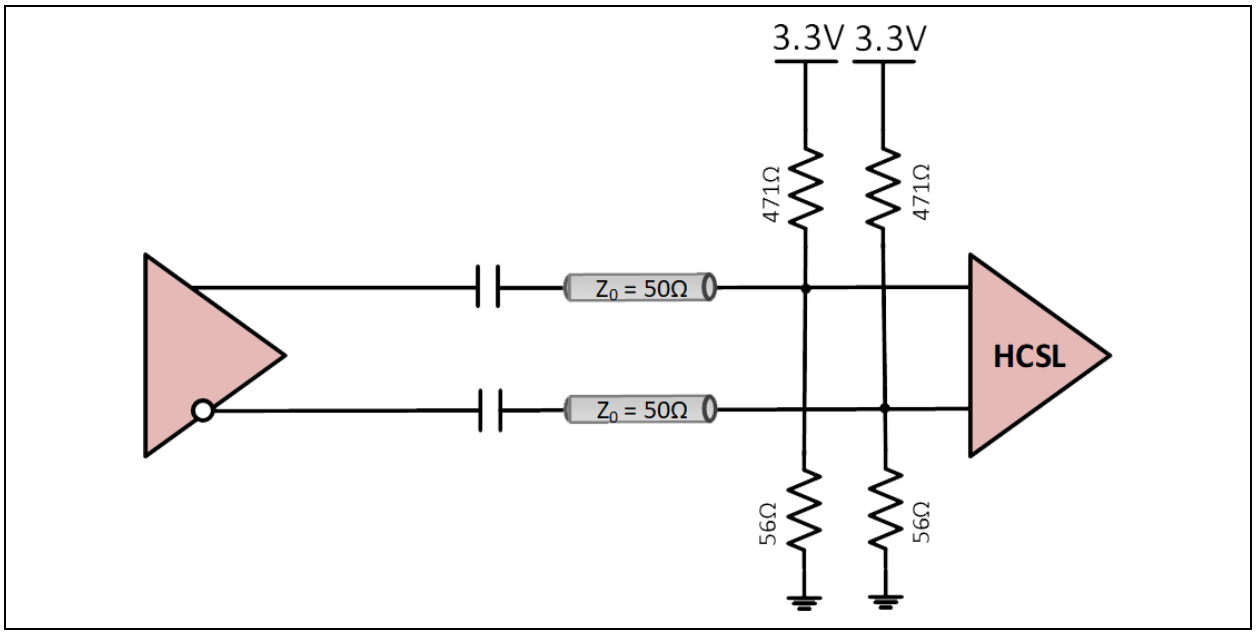

FIGURE 20: AC COUPLING LVDS TO HCSL.

The 471Ω/56Ω network sets the HCSL receiver common mode voltage to about 400 mV.

5.2 AC Coupling LVPECL Driver

5.2.1 AC COUPLING LVPECL DRIVER TO LVPECL RECEIVER

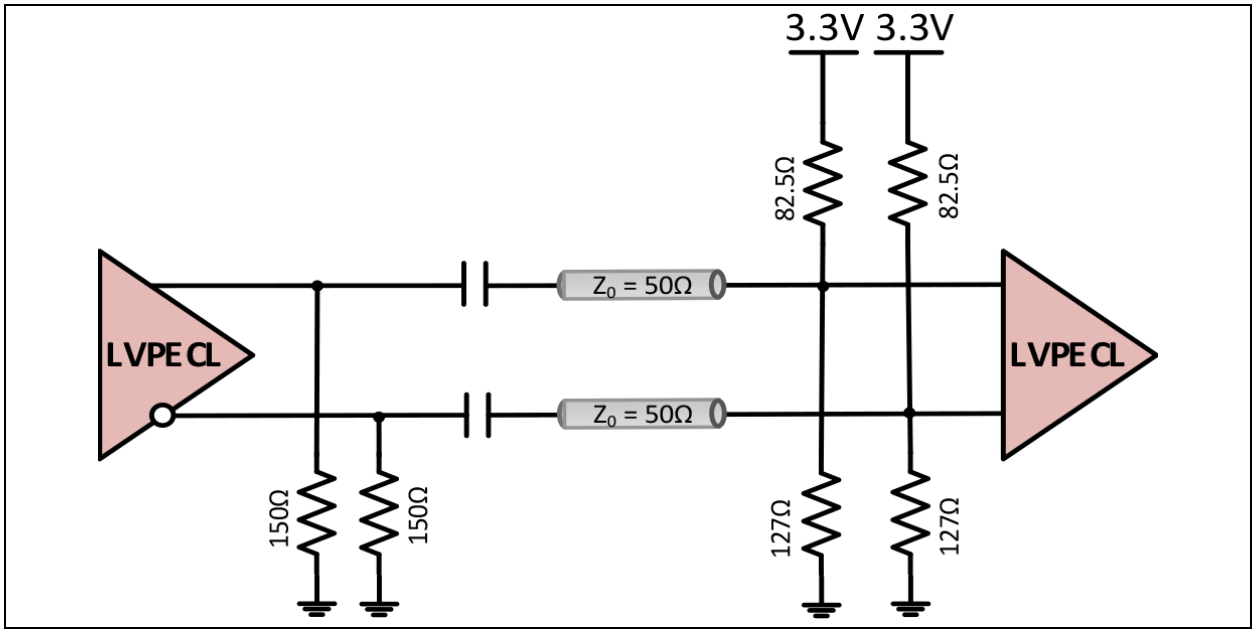

FIGURE 21: AC COUPLING LVPECL TO LVPECL.

The 82.5Ω/127Ω network terminates the line with 50Ω and sets the LVPECL input common mode voltage to V_{CC} – 1.3V (2V).

5.2.2 AC COUPLING LVPECL DRIVER TO LVDS RECEIVER

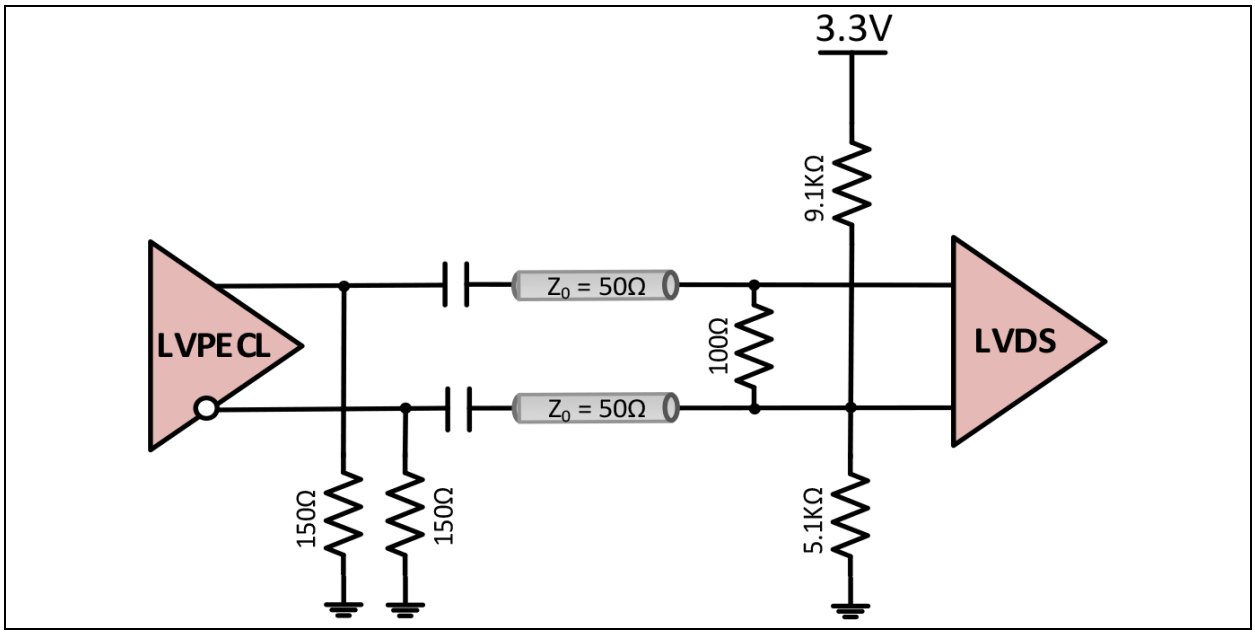

FIGURE 22: AC COUPLING LVPECL TO LVDS.

The 150Ω is the equivalent termination to LVPECL output. The 5.1KΩ/9.1KΩ network sets the LVDS input common mode voltage to 1.2V.

5.2.3 AC COUPLING LVPECL DRIVER TO CML RECEIVER

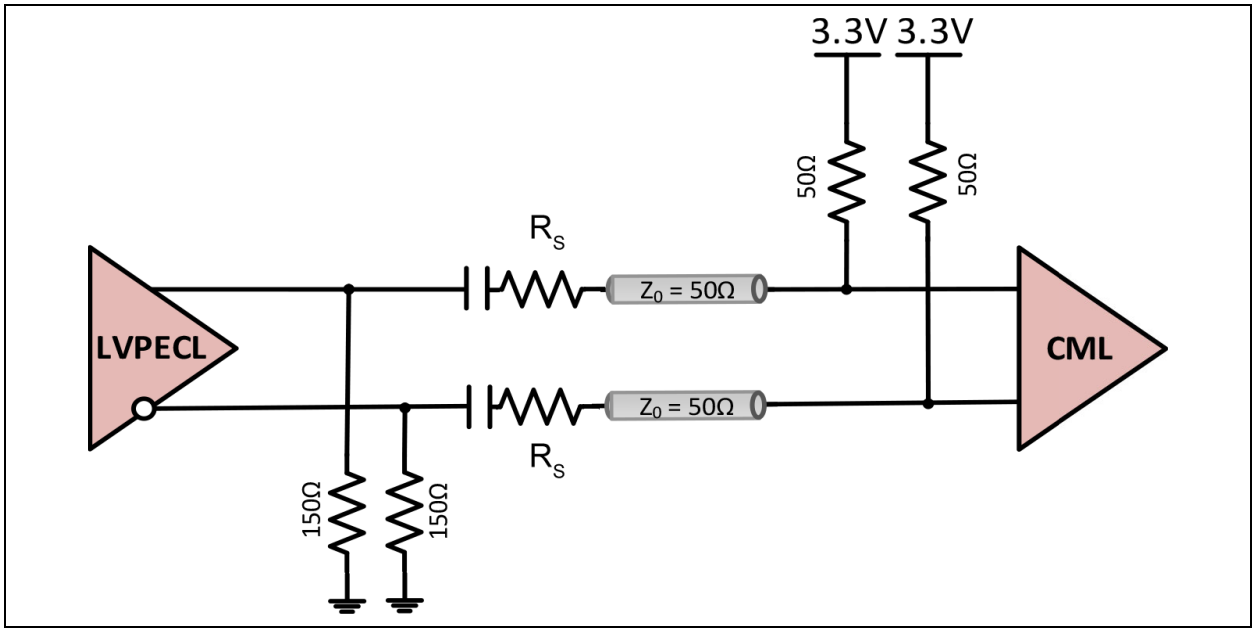

FIGURE 23: AC COUPLING LVPECL TO CML.

The 50Ω resistors terminate the line and bias the CML input while the series resistor attenuates the LVPECL signal to be within range for CML input.

5.2.4 AC COUPLING LVPECL DRIVER TO HCSL RECEIVER

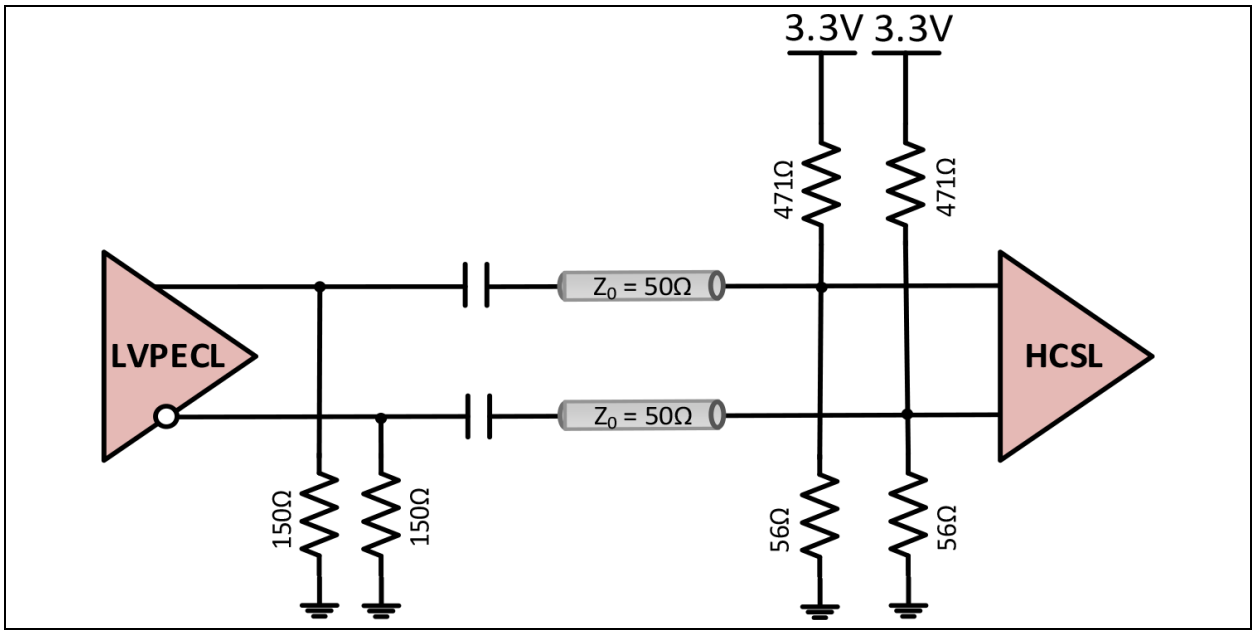

FIGURE 24: AC COUPLING LVPECL TO HCSL.

The 471Ω/56Ω network provide a 50Ω line termination and set the HCSL input common voltage close to 400 mV.

5.3 AC Coupling CML Driver

5.3.1 AC COUPLING CML DRIVER TO CML RECEIVER

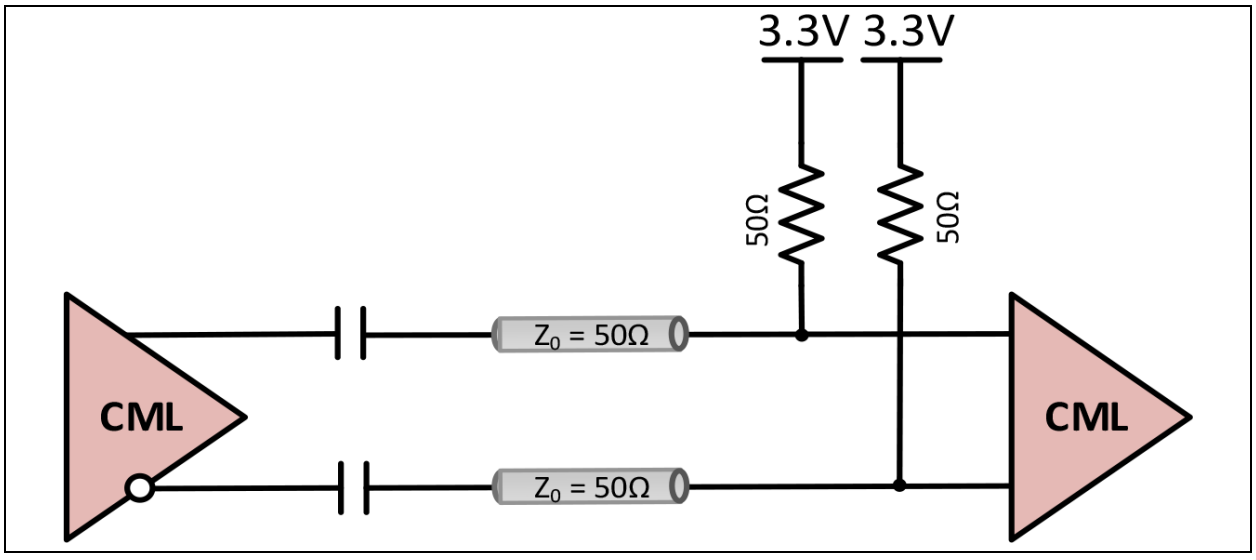

FIGURE 25: AC COUPLING CML TO CML (DRIVER WITH INTEGRATED 50Ω TERMINATION TO VCC).

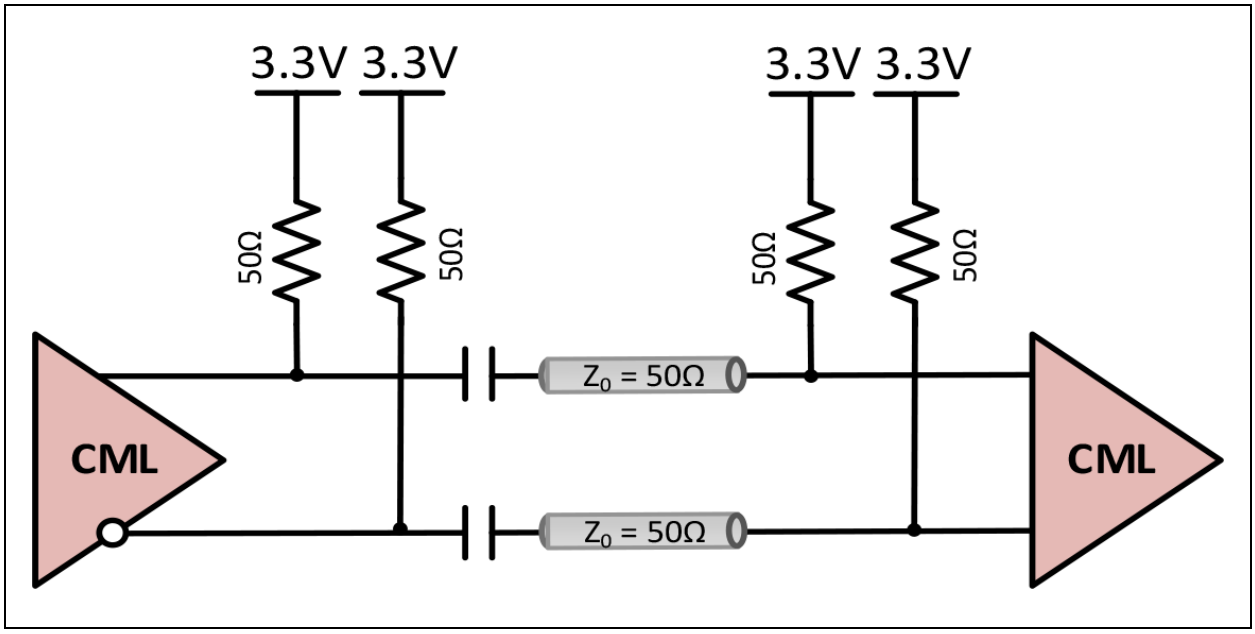

FIGURE 26: AC COUPLING CML TO CML (DRIVER WITHOUT INTEGRATED 50Ω TERMINATION TO VCC).

If the driver doesn't have internal 50Ω termination to VCC, the output must be terminated outside before the coupling cap.

5.3.2 AC COUPLING CML DRIVER TO LVDS RECEIVER

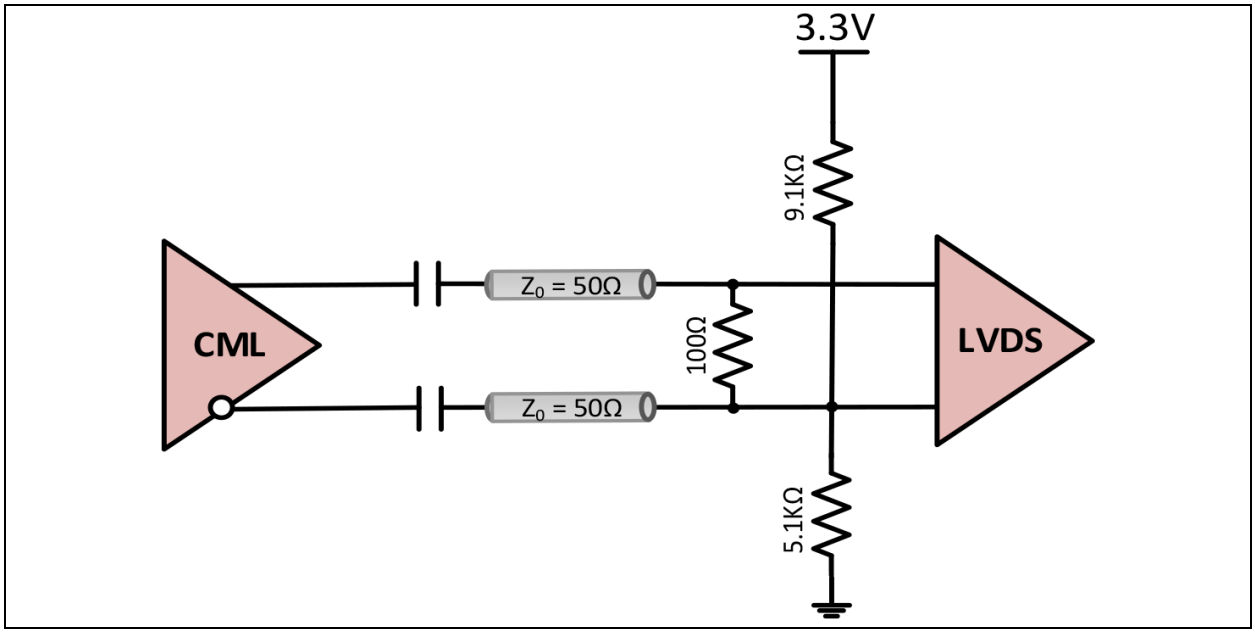

FIGURE 27: AC COUPLING CML TO LVDS.

The CML driver in Figure 27 has internal 50Ω termination to VCC, and the LVDS receiver doesn't have internal termination. The 5.1 KΩ/9.1 KΩ networks set the 1.2V common mode voltage for the LVDS receiver. For CML driver without internal termination, please refer to Figure 26. For an LVDS receiver with internal termination, please refer to Figure 17.

5.3.3 AC COUPLING CML DRIVER TO LVPECL RECEIVER

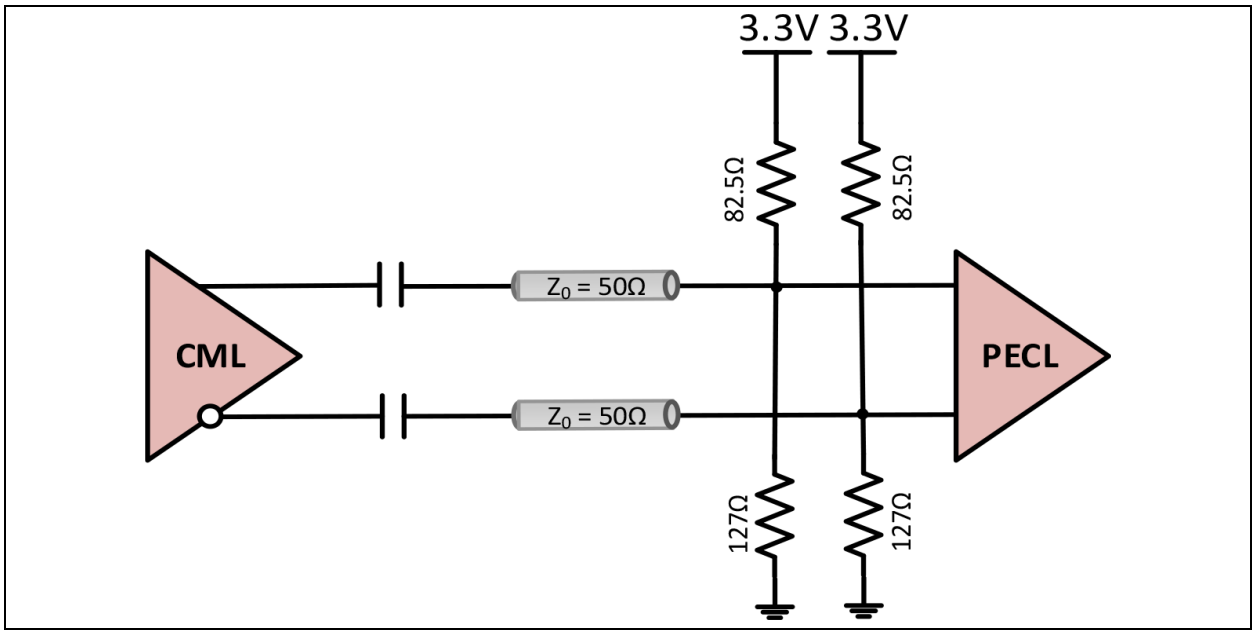

FIGURE 28: AC COUPLING CML TO LVPECL.

5.3.4 AC COUPLING CML DRIVER TO HCSL RECEIVER

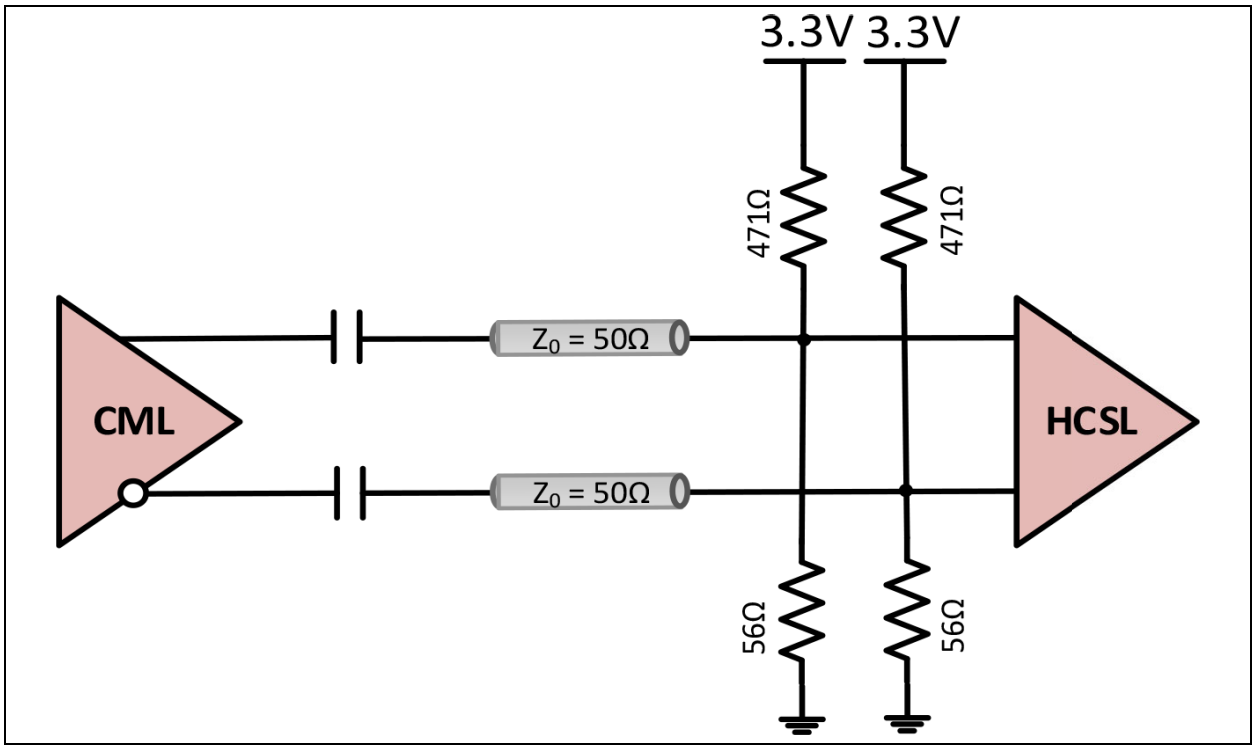

FIGURE 29: AC COUPLING CML TO HCSL.

5.4 AC Coupling HCSL Driver

5.4.1 AC COUPLING HCSL DRIVER TO HCSL RECEIVER

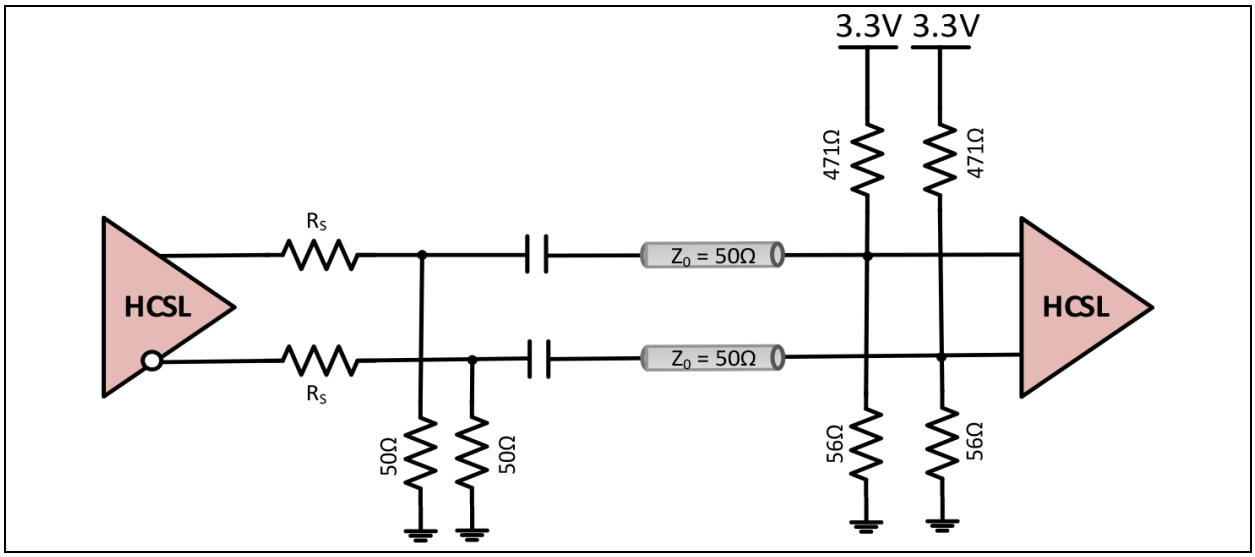

FIGURE 30: AC COUPLING HCSL TO HCSL.

5.4.2 AC COUPLING HCSL DRIVER TO LVDS RECEIVER

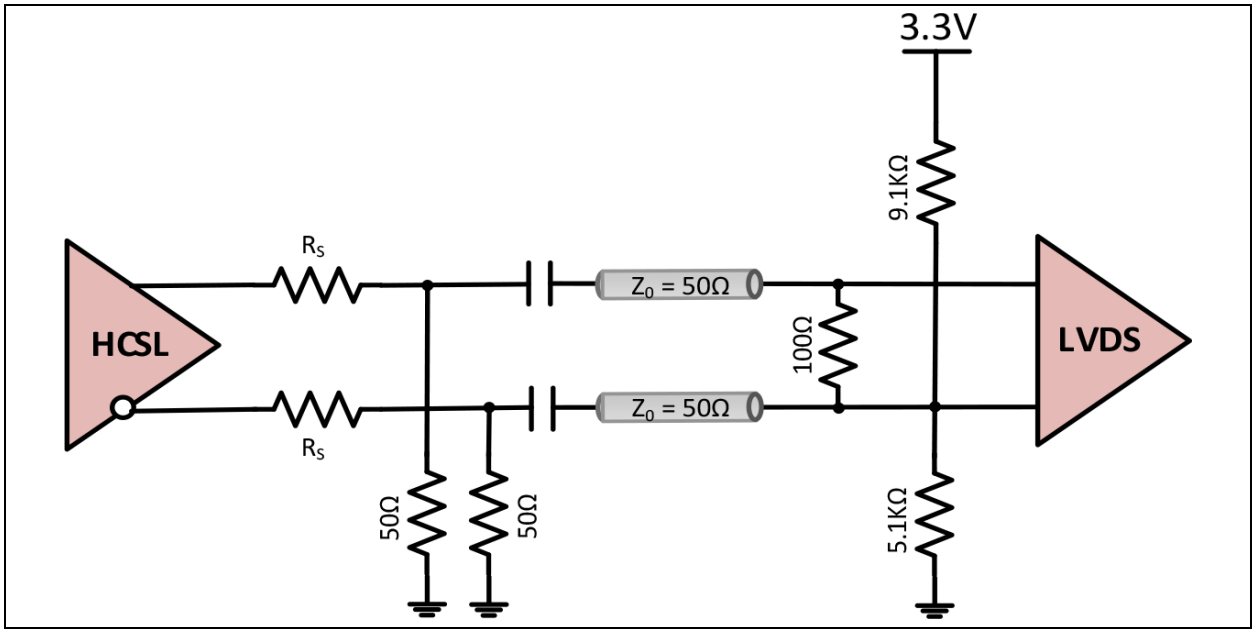

FIGURE 31: AC COUPLING HCSL TO LVDS.

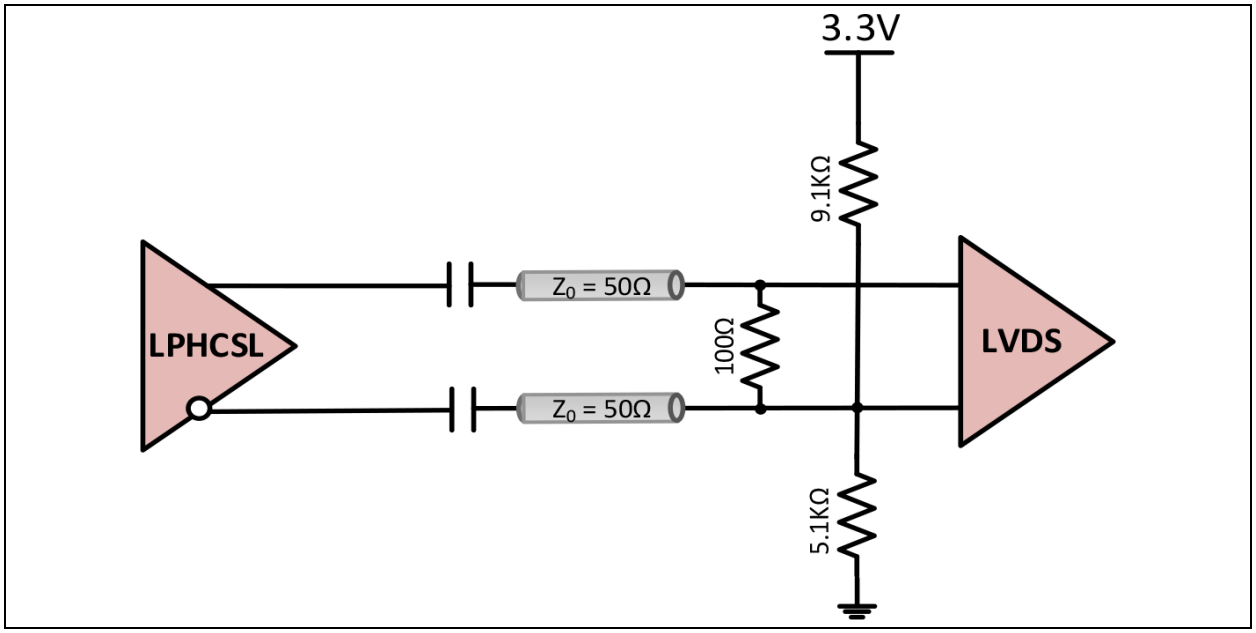

FIGURE 32: AC COUPLING LPHCSL TO LVDS.

5.4.3 AC COUPLING HCSL DRIVER TO LVPECL RECEIVER

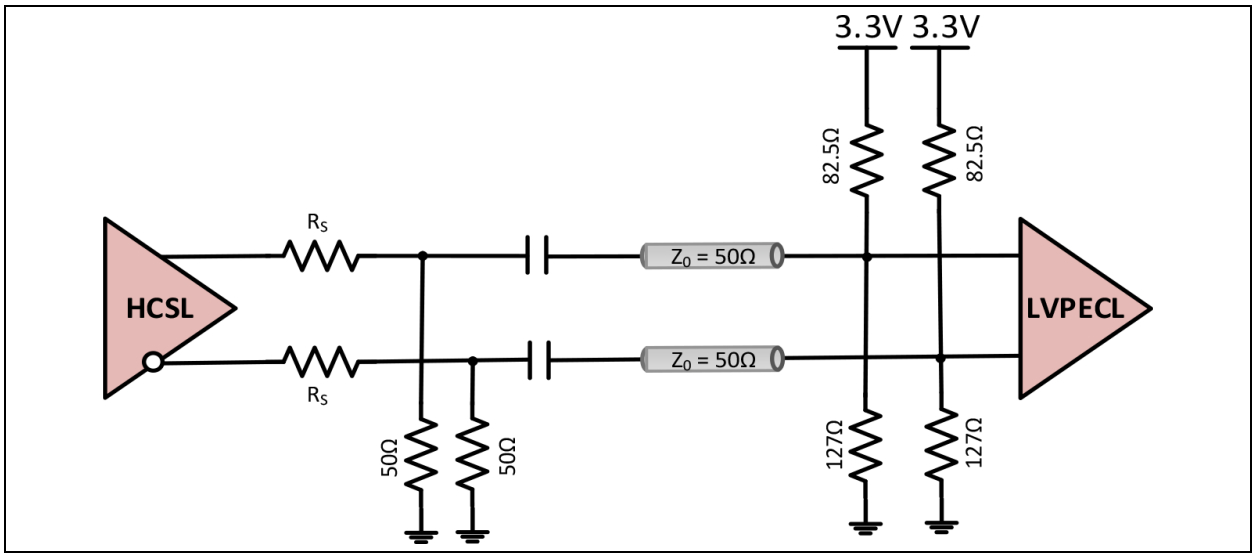

FIGURE 33: AC COUPLING HCSL TO LVPECL.

5.4.4 AC COUPLING HCSL DRIVER TO CML RECEIVER

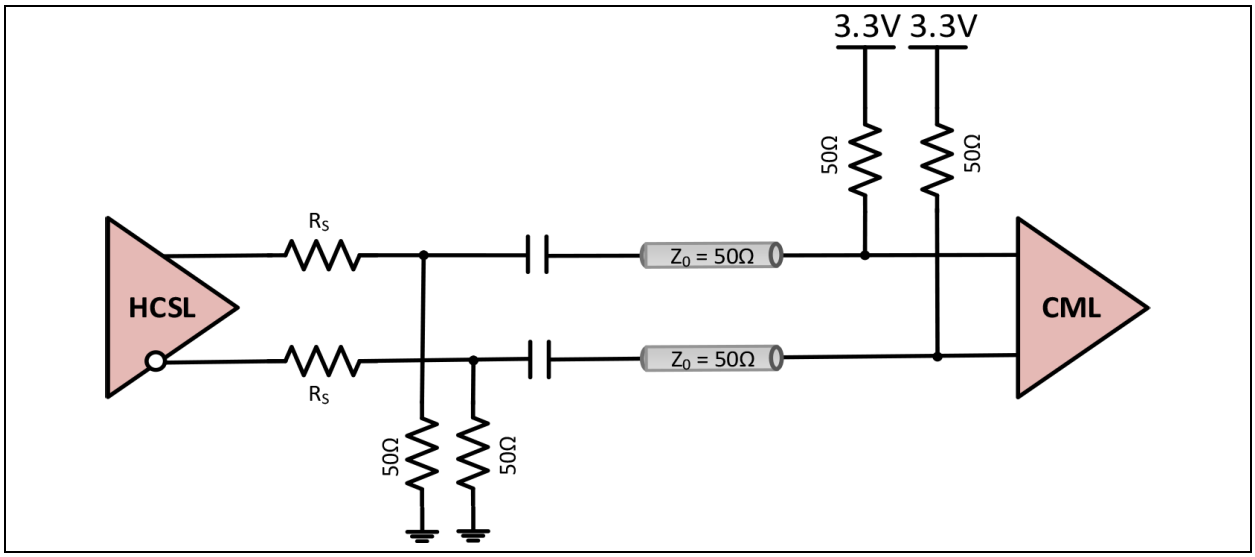

FIGURE 34: AC COUPLING HCSL TO CML.

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