VSC8211
Linking CPUs with R/GMII Interfaces to SGMII-Based Switches

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first release of this document. It was published in April 2005.

2 Introduction

This Application Note will describe design considerations for connecting an embedded microprocessor that contains a GMII or RGMII MAC interface to an SGMII-based Gigabit Ethernet Switch. This document will cover system, hardware, and software considerations as well as advantages and limitations for each.

Systems such as IP DSLAMs, wireless platforms, and enterprise routers often require enhanced security protocol processors to help to perform switching and parsing of packets. However, packet processors' Ethernet interfaces are a generation behind the latest Ethernet switch devices. The latest Gigabit Ethernet switch devices with high port counts of 16-24 ports per chip have migrated towards SGMII interfaces, while processors are only now offering both GMII and RGMII interfaces. For a packet processor to connect to the latest gigabit switch, there will need to be an interface conversion device to get an RGMII processor to link to an SGMII-based Ethernet switch. This document will cover various design considerations for connecting an embedded microprocessor with a GMII or RGMII MAC interface to an SGMII-based Gigabit Ethernet switch. This document will address system, hardware, and software considerations as well as advantages and limitations for each.

2.1 Audience

This document is geared toward system, hardware, and software designers.

2.2 References

2.2.1 Vitesse Documents

- VSC8211 Datasheet (VMDS-10105)
- VSC8224 Datasheet (VMDS-10107)
- VSC7372 Datasheet (PD0031)
- VSC7374 Datasheet (PD0028)
- VSC7376 Datasheet (PD0032)
- VSC8211 Design and Layout Guide (VPPD-01173)
- VSC8224 Design and Layout Guide (VPPD-01145)

2.2.2 IEEE Standards

- CSMA/CD Access Method and Physical Layer Specification (IEEE802.3)

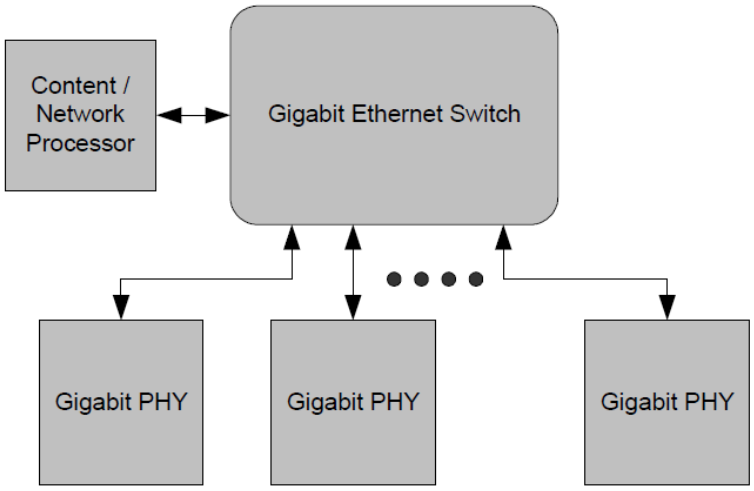
2.2.3 External Documents

- Freescale MPC8548E Fact Sheet (MPC8548FS)
- Intel IXP2325 Product Brief (30367902)
- AMCC PowerPC 440GX Product Brief (PB2000)
- Mindspeed M27481 Product Brief (27481-BRF)

3 A Managed Switch System

A managed switch system is composed of at least an Ethernet switch chip, several physical layer devices (PHYs) that can interface to copper or fiber links, and at least one embedded processor. The system will generally be responsible for managing packets at a level of up to Layer 3 or higher.

Figure 1 • Managed Switch Block Diagram



4 System Considerations

4.1 How Many Interface Ports?

One factor to consider is how many interface ports from the switch will be connected to the embedded processor. For example, the MPC8548E PowerQuicc III has four-gigabit Ethernet MAC interfaces. All four of these ports could be linked to the Ethernet switch.

4.2 Packet Traffic Shaping

Generally a gigabit Ethernet connection requires at least 1 GHz of dedicated CPU processing power. Most embedded processors cannot handle a large continuous burst of packet data of this magnitude. To prevent a processor from being overrun, it is important to consider if traffic shaping will be required. Traffic shaping is useful in that it can limit the amount of egress traffic from being sent out of a switch port into a bandwidth-limited device, such as a CPU.

4.3 RGMII-SGMII PHY Device Link Monitoring

To ensure the link between the processor and switch is active, there are several monitoring methods to consider.

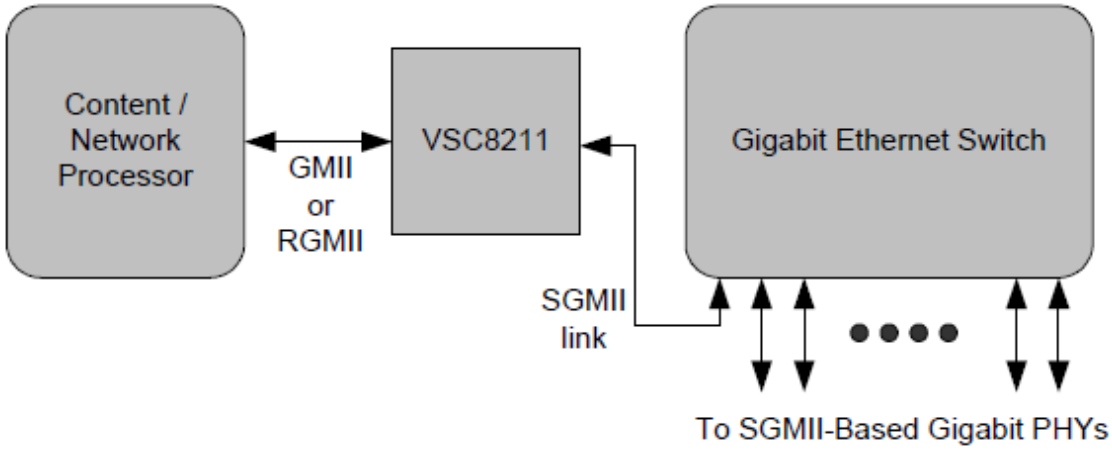
- The PHY's link status register bit can be continuously polled.
- The PHY's interrupt pin is connected to the interrupt controller to monitor change in link status.
- The LINK LED can be connected to a GPIO pin on the processor and then this pin is monitored.

5 Hardware Considerations

Once the number of ports is established, the RGMII-SGMII conversion device must be selected. For 1-2 ports, the VSC8211 single gigabit PHY can be used. For higher ports, the VSC8224 quad gigabit PHY is a better choice due to its compact footprint size and low power.

The following information in this section is a general description. Please consult both the PHY's datasheet or design and layout guide for more specific design information.

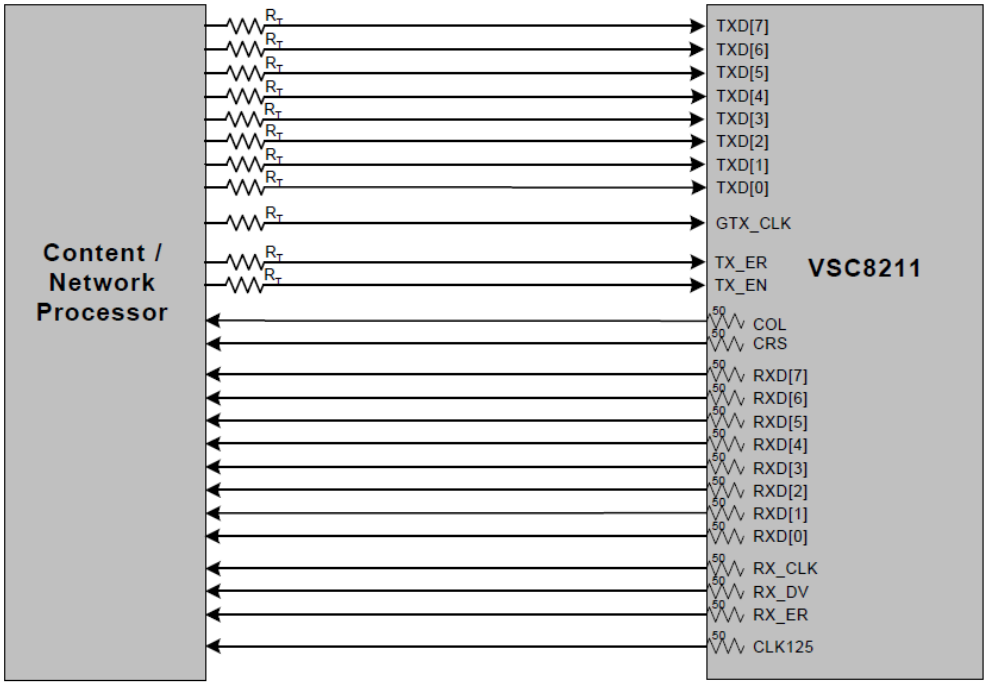
Figure 2 • RGMII-to-SGMII Hardware Connectivity



5.1 Connecting GMII

GMII is a 25-pin per port interface. It has a clock speed of 125 MHz and 8 data bits in both directions. The interface clock is sourced by the PHY.

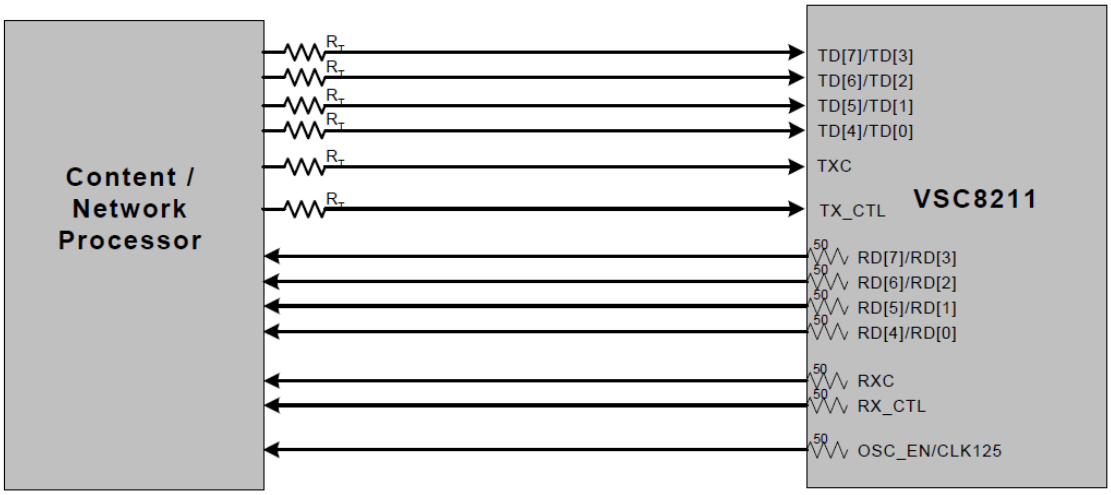
Figure 3 • GMII Connection Diagram



5.2 Connecting RGMII

RGMII is a reduced pin count version of GMII as it only has 12 pins per port. While it uses the same 125 MHz clock speed, the data pin count is reduced to 4 bits and the data is clocked in on both edges of the clock in a double-data rate manner.

Figure 4 • RGMII Connection Diagram



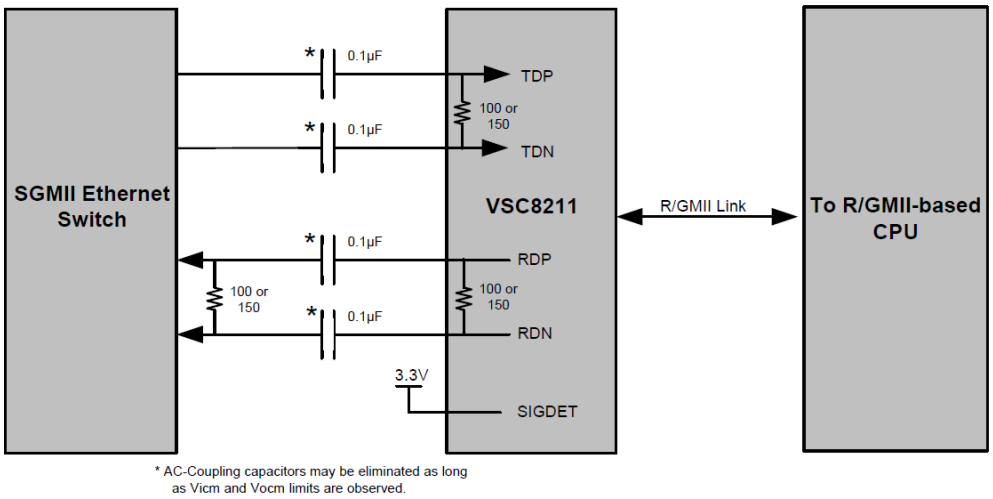
Another aspect of RGMII that is different from GMII is that it requires a clock delay skew of 1.5 ns–1.9 ns to either be placed on the board with a delay trace or the delay is created internally in the MAC and/or PHY. The VSC8211 offers this clock delay skew feature on both TX and RX pairs thereby removing the need for a board trace delay. See the VSC8211 or VSC8224 Design and Layout Guide for more information.

5.3 Connecting SGMII

SGMII is a further pin reduction of GMII as it is only a 4-pin interface. The data and clock are embedded and transmitted on a two pin differential interface in both directions. The latest switch will operate its port interface using the SGMII interface. Both the VSC8211 and VSC8224 cannot perform a full RGMII-to-SGMII conversion. These devices however, can operate as an RGMII-to-1000BASE-X SerDes media converter. 1000BASE-X SerDes is compliant electrically and functionally to SGMII's 1000 Mbps setting. From a permanent link perspective, 1000 Mbps is the only speed that is required in an SGMII-based Ethernet switch system. Therefore the RGMII-to-1000BASE-X mode can be used to link the processor to the SGMII-based Ethernet switch.

For the VSC8211/VSC8224, AC coupling capacitors are needed from the processor to the PHY. The SGMII switches such as the VSC7372/74/76 have a register setting to allow the PHY-to-Switch portion to be electrically compatible. To allow the SerDes on the PHY to link, the SIGDET pin must also be asserted by tying it high.

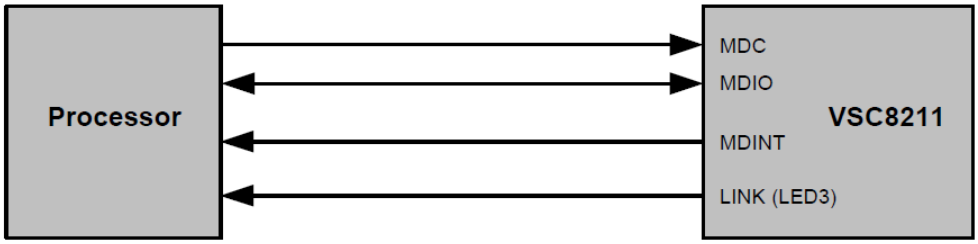
Figure 5 • SGMII Connection Diagram



5.4 Control and Status Connections

In order to setup the PHY the MDC and the MDIO must be connected to the host processor to setup the operating mode and other PHY register settings. Also depending on how the processor will monitor the PHY during normal operation, other pins such as the interrupt pin (MDINT) or the LINK LED pin will need to be connected.

Figure 6 • Control and Status Diagram



The MDC/MDIO pins are required to setup the VSC8211.
The MDINT and LINK LED are optional.

6 Software Considerations

6.1 VSC8211 Register Configuration

For the VSC8211, the following registers must be configured.

- Set the operating mode (see the following table).
- If using RGMII, then set the delay skew setting (register 23[11:8]).
- Set Auto-negotiation Disabled (Register 0.12 = 0).
- Set Speed Selection (Register 0.[6,13] = 10).
- Set Duplex to Full (Register 0.8 = 1).
- If using MDINT pin as a link indication, set Register 25.15 = 1 and Register 25.13 = 1 (Link state change indication).

Table 1 • Setting the VSC8211 Operating Mode (Register 23[15:12, 2:1])

Register Setting	Description
0011 01	GMII-Fiber (1000BASE-X SerDes)
0001 01	RGMII-Fiber (1000BASE-X SerDes)

6.2 SGMII Switch Register Configuration

For the VSC7372/74/76 switch, the following registers must be configured in order to link to the VSC8211. This is in addition to the settings that are required for initialization of the switch. These settings can be found in the Minimum Software Requirements section of the VSC7372/74/76 datasheets.

- Set the SGMII_MACRO_CFGx.TX_ENA (Block 1, 0x1A bit 28 = 1)
- Set the SGMII_MACRO_CFGx.TX_OUTPUT_LEVEL (Block 1, 0x1A bit 26 = 1)
- Set the SGMII_MACRO_CFGx.TX_RESET (Block 1, 0x1A bit 25 = 1)
- Set the SGMII_MACRO_CFGx.RX_IB_AUTO_SQUELCH (Block 1, 0x1A bit 24 = 1)
- Set the SGMII_MACRO_CFGx.TX_COMMONMODE_TERM_ENA (Block 1, 0x1A bit 23 = 1)
- Set the SGMII_MACRO_CFGx.CDR_DISABLE (Block 1, 0x1A bit 22 = 0)
- Set the SGMII_MACRO_CFGx.RX_ENA (Block 1, 0x1A bit 8 = 1)
- Set the SGMII_MACRO_CFGx.RX_RESET (Block 1, 0x1A bit 0 = 1)
- Set the SGMII_INPUT_COMMONMODE_SELx.IB_B (Block 1, 0x1B bit 9 = 1)
- Set the SGMII_INPUT_COMMONMODE_SELx.IB_A (Block 1, 0x1B bit 0 = 1)

Also, if traffic shaping is being employed, this can be found in the following table.

Table 2 • Switch Egress Port Traffic Shaping Control

Register Setting	Register	Description
WS_CONFx.ENABLE	Block 1, 0x28 bit 6	Enables/Disables Shaping
WS_CONFx	Block 1, 0x28 bits 12:7, 5:0	Configures the Shaping
WS_BUCK0	Block 1, 0x29 bits 20:0	Configures Queue 0 Bucket
WS_BUCK1	Block 1, 0x2A bits 20:0	Configures Queue 1 Bucket
WS_BUCK2	Block 1, 0x2B bits 20:0	Configures Queue 2 Bucket
WS_BUCK3	Block 1, 0x2C bits 20:0	Configures Queue 3 Bucket

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