LAN8870/LAN8871/LAN8872

100/1000BASE-T1 Ethernet PHY Transceiver

Highlights

- Single-chip Ethernet physical layer transceiver
- Compliant with IEEE 802.3bp-2016 (1000BASE-T1)
- Compliant with IEEE 802.3bw-2015 (100BASE-T1) (LAN8870 only)
- Media-Independent Interface support
  - LAN8870: RGMII/SGMII MAC interfaces
  - LAN8871: RGMII MAC interface
  - LAN8872: SGMII MAC interface
- Supports RGMII and SGMII MAC interfaces
- 100Mbps/1000Mbps auto-negotiation and force speed mode
- IEEE 1588-2019 and 802.1AS-2020 support
- OPEN Alliance TC10 support / wake-up support
- Ultra low power sleep
- FlexPWR® technology power management
- Advanced Signal Quality Indicator (SQI)
- Over-temperature and under-voltage protection
- Comprehensive status interrupt support
- 1000BASE-T1 Type B support for extended cable reach (LAN8870B only)
- Small footprint 48-pin VQFN (7 x 7 mm) with wettable flanks
- AEC-Q100 automotive product qualification
- Grade 2 Automotive temperature range (-40°C to +105°C)
- Industrial temperature range (-40°C to +85°C)
- Microchip Functional Safety Ready

Target Applications

- Advanced Driver-Assistance Systems (ADAS)
- Infotainment
- Telematics & Smart Antennas
- In-Vehicle Backbone
- Gateways
- Industrial Control
- IIoT

Key Benefits

- High-performance 100BASE-T1/1000BASE-T1 Ethernet PHY (100BASE-T1 LAN8870 only)
  - 100Mbps and 1000Mbps over single balanced twisted pair cable
  - OPEN Alliance TC10 sleep/wake-up support
  - Supports cable lengths up to at least 15m
  - PTP support
  - Fully AVB/TSN compatible
  - Jumbo frame support up to 16KB
  - On-chip termination resistors for balanced UTP cable
  - 25MHz SMI interface for rapid register access
- RGMII (LAN8870/LAN8871) & SGMII (LAN8870/LAN8872) Interfaces
- 25MHz, 50MHz, 125MHz reference clock output
- Low RF Emissions
  - Integrated transmission filtering
  - 125MHz RGMII clock slew rate adjust (LAN8870/LAN8871)
- EtherGREEN™ Energy Efficiency
  - Ultra low-power sleep mode (15µA typical) with local wake-up support (OPEN Alliance TC10)
  - Sleep request recognition
  - IDLE detection on MDI
  - **WAKE_IN** pulse detection wakeup
  - **INH** output for enable/disable of ECU supply
  - Gap free voltage and temperature monitoring
- Resets
  - Pin reset (**RESET_N**)
  - Power-On Reset (POR) with brownout protection
  - Software reset
- Packaging
  - 48-pin (7 x 7 mm) wettable VQFN
- Environmental
  - Grade 2 Automotive temperature range (-40°C to +105°C)
  - Industrial temperature range (-40°C to +85°C)
- Functional Safety
  - For ASIL B and Beyond Applications
  - FMEDA Computation Spreadsheet (Evaluation of Random Hardware Failures Metric)
  - Functional Safety Manual

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
1000BASE-T	1 Gbps Ethernet over twisted pair, IEEE 802.3 compliant
1000BASE-T1	1 Gbps Ethernet over single balanced twisted pair, IEEE 802.3bp compliant
100BASE-T1	100 Mbps Ethernet over single balanced twisted pair, IEEE 802.3bw compliant
AFE	Analog Front End
BYTE	8-bits
CSR	Control and Status Register
DCQ	Dynamic Channel Quality
DSP	Digital Signal Processor
FIFO	First In First Out buffer
FS	Full Speed
FSM	Finite State Machine
GPIO	General Purpose I/O
HOST	External system (Includes processor, application software, etc.)
LDO	Linear Drop-Out Regulator
lsb	Least Significant Bit
LSB	Least Significant Byte
LTC	Local Time Counter
MAC	Media Access Controller
MCH	Microchip Control Header, proprietary extension to PCH
MDI	Medium Dependent Interface
MSE	Mean Square Error
N/A	Not Applicable
PCH	Packet Control Header, standard format
PCS	Physical Coding Sublayer
PLL	Phase Locked Loop
POR	Power on Reset.
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
RGMII	Reduced Gigabit Media Independent Interface
SFD	Start of Frame Delimiter - The 8-bit value indicating the end of the preamble of an Ethernet frame
SGMII	Serial Gigabit Media Independent Interface

TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
SMI	Serial Management Interface
SQI	Signal Quality Indication
SW	Software
TOD	Time of Day

1.2 Buffer Types

TABLE 1-2: LAN887X BUFFER TYPE DESCRIPTIONS

Buffer	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-directional
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
P	Power pin
PU	70K (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	70K (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
VIS-VDDIO	Variable voltage Schmitt-triggered input (**VDDIO** power domain)
VIS-VDD_RGMII	Variable voltage Schmitt-triggered input (**VDD_RGMII** power domain)
VIS-VBAT	Variable voltage Schmitt-triggered input (**VBAT** power domain)
VO-VDDIO	Variable voltage output with 5 mA sink and 5 mA source (**VDDIO** power domain)
VO-VDD_RGMII	Variable voltage output with 5 mA sink and 5 mA source (**VDD_RGMII** power domain)
VO-VBAT	Variable voltage output with 5 mA sink and 5 mA source (**VBAT** power domain)
VOD	Variable open-drain output
LVDS	LVDS input

Note: Digital signals are not 5V tolerant unless specified.

Note: Sink and source capabilities are dependent on the supplied voltage.

1.3 Register Bit Types

Table 1-3 describes the register but attributes used throughout this document.

TABLE 1-3: REGISTER BIT TYPES

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Write:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
W1S	**Write One to Set:** Writing a one sets the value. Writing a zero has no effect.
W1C	**Write One to Clear:** Writing a one clears the value. Writing a zero has no effect.
WAC	**Write Anything to Clear:** Writing anything clears the value.
RC	**Read to Clear:** Contents is cleared after the read. Writes have no effect.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents is self-cleared after being set. Writes of zero have no effect. Contents can be read.
SS	**Self-Setting:** Contents is self-setting after being cleared. Writes of one have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** This mode is used by the Ethernet PHY registers. Bits with this attribute will stay high until the bit is read. After it a read, the bit will remain high, but will change to low if the condition that caused the bit to go high is removed. If the bit has not been read the bit will remain high regardless of if its cause has been removed.
NASR	**Not Affected by Software Reset.** The state of NASR bits does not change on assertion of a software reset.
STKY	This field is “Sticky” in that it is neither initialized nor modified by hot reset or Function Level Reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros, unless otherwise indicated, to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

Many of these register bit notations can be combined. Come examples of this are:

- **R/W**: Can be written. Will return current setting on a read.
- **R/WAC**: Will return current setting on a read. Writing anything clears the bit.

1.4 Reference Documents

1. *IEEE 802.3™-2018 IEEE Standard for Ethernet,*
   https://ieeexplore.ieee.org/document/8457469
2. *IEEE 802.3bp™-2016 IEEE Standard for Ethernet Amendment 4,*
   https://ieeexplore.ieee.org/document/7564011
3. *IEEE 802.3bw™-2015 IEEE Standard for Ethernet Amendment 1,*
   https://ieeexplore.ieee.org/document/7433918
4. *RMII Specification Revision 1.2,*
   http://ebook.pldworld.com/_eBook/-Telecommunications,Networks-/TCPIP/RMII/rmii_rev12.pdf
5. *Reduced Gigabit Media Independent Interface (RGMII) Specification Version 2.0,*
   https://web.archive.org/web/20160303171328/http://www.hp.com/rnd/pdfs/RGMIIv2_0_final_hp.pdf
6. *OPEN Alliance TC1 - Advanced diagnostics features for 100BASE-T1 automotive Ethernet PHYs Version 1.0*
   http://www.opensig.org/download/document/218/Advanced_PHY_features_for_automotive_Ethernet_V1.0.pdf
7. *OPEN Alliance TC10 - Sleep/Wake-up Specification Version 2.0*
   http://www.opensig.org/download/document/220/TC10+Wake-up+and+Sleep+Specification+for+Automotive+Ethernet_11-2017.pdf

2.0 INTRODUCTION

2.1 General Description

The Microchip LAN8870/LAN8871/LAN8872 (LAN887x) family of devices provide a compact, cost-effective, single-port 100BASE-T1/1000BASE-T1 Ethernet physical layer transceiver solution compliant with the IEEE 802.3bw-2015 and IEEE 802.3bp-2016 specifications.

The LAN887x provides transmit and receive capability with cable reaches beyond the IEEE 802.3bp standard:

a) A link segment supporting up to four in-line connectors using a single twisted-pair copper cable for up to at least 15 meters (referred to as link segment type A)

b) A link segment supporting up to four in-line connectors using a single twisted-pair copper cable for up to at least 40 meters (referred to as link segment type B)

The LAN887x is available in both Industrial grade (-40°C to +85°C) and AEC-Q100 Automotive Grade 2 (-40°C to +105°C) temperature ranges and is optimized for applications such as Industrial Automation, IIoT, Automated Driver-Assistance Systems (ADAS), infotainment, telematics, and in-vehicle backbones.

The LAN887x supports communication with an Ethernet MAC via standard RGMII/SGMII interfaces (see Table 2-1 for device specific interface breakdown). An optional 25MHz, 50MHz, or 125MHz reference clock output is provided. An integrated SMI interface provides rapid register access and configuration.

The LAN887x is Time Sensitive Networking (TSN) ready, supporting IEEE802.1AS-2020 and IEEE1588-2019 Precision Clock Synchronization Protocol for real time Ethernet networking.

Microchip's LAN887x EtherGREEN™ energy efficient technology provides low-power 1000BASE-T1/100BASE-T1 PHY operation along with OPEN Alliance TC10 ultra low-power remote sleep and wake-up support. FlexPWR® variable I/O and core power supply voltages provide flexible design options and further power saving opportunities.

Advanced PHY diagnostics provide the user with troubleshooting capabilities such as cable defect detection of shorts or opens, a receiver Signal Quality Indicator (SQI), over-temperature, under-voltage protection, comprehensive status interrupt support, and various loopback and test modes.

The Microchip LAN887x family includes the following devices:

- LAN8870
- LAN8870B
- LAN8871
- LAN8872

Device specific features that do not pertain to the entire LAN887x family are called out independently throughout this document. Table 2-1 provides a summary of the feature differences between family members:

TABLE 2-1: LAN887X FAMILY FEATURE MATRIX

Part Number	Package	1000BASE-T1	100BASE-T1	Auto-Negotiation	RGMII Support	SGMII Support	125MHz Reference Clock Output	Precision Time Protocol (PTP)	Internal Core Voltage Regulator Disable Option	INH Pin Support	WAKE_IN Pin Support	AEC-Q100 -40° To 105°C	Industrial Grade -40° To +85°C	1000BASE-T1 Type B Extended Reach
LAN8870	48-VQFN	X	X	X	X	X	X	X	X	X	X	X	X	
LAN8870B	48-VQFN	X	X	X	X	X	X	X	X	X	X	X	X	X
LAN8871	48-VQFN	X		X	X		X	X	X	X	X	X	X	
LAN8872	48-VQFN	X		X		X	X	X	X	X	X	X	X	

A system-level block diagram is shown in Figure 2-1. An internal block diagram of the LAN887x is shown in Figure 2-2.

FIGURE 2-1: LAN887X FAMILY SYSTEM-LEVEL BLOCK DIAGRAM

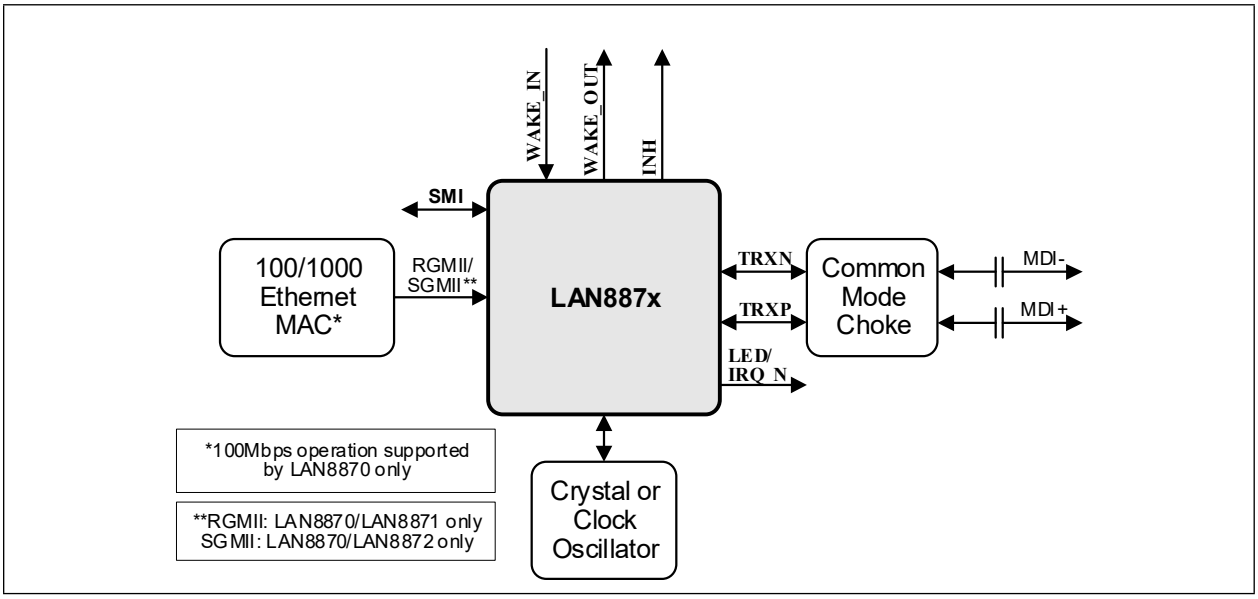
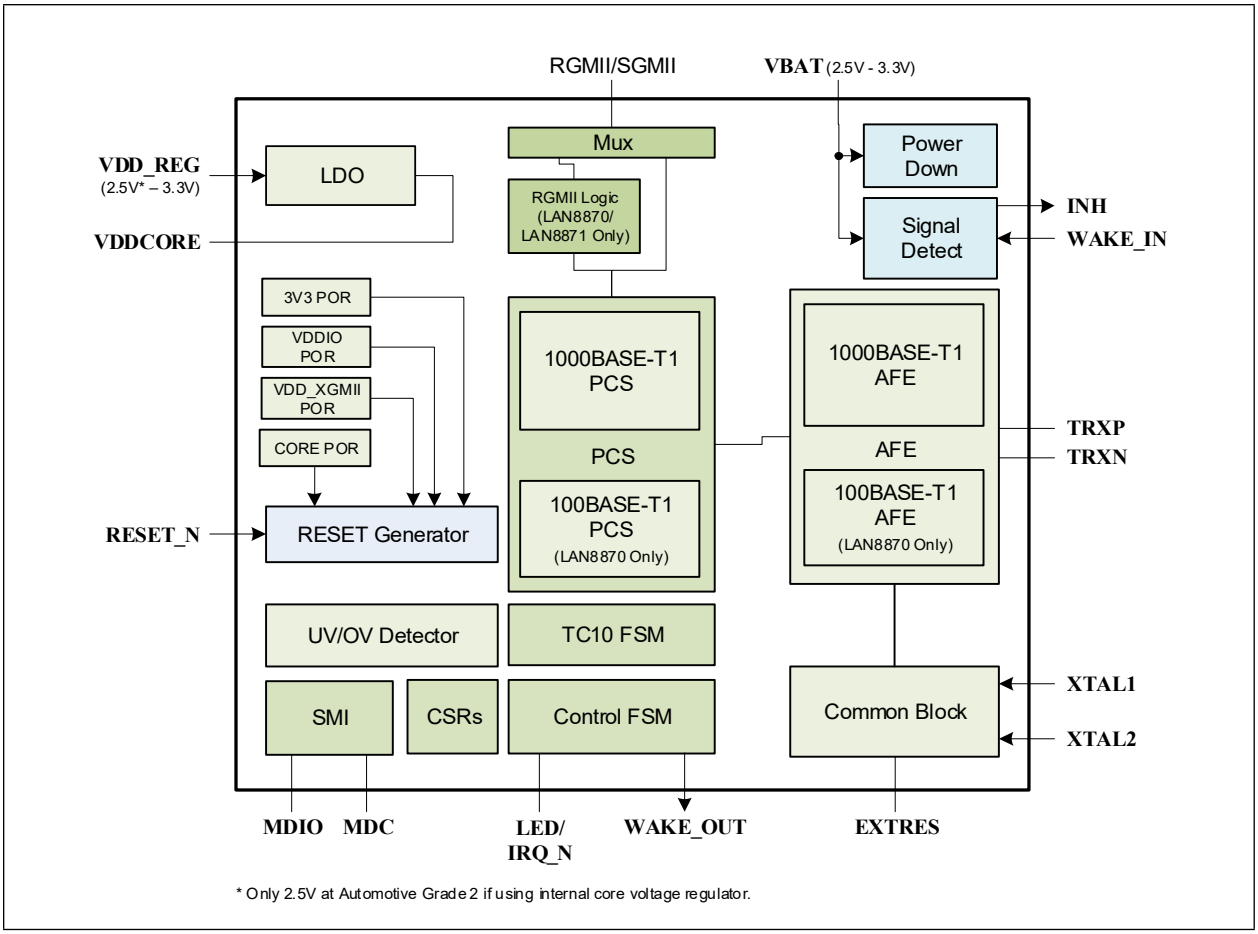


FIGURE 2-2: LAN887X INTERNAL BLOCK DIAGRAM



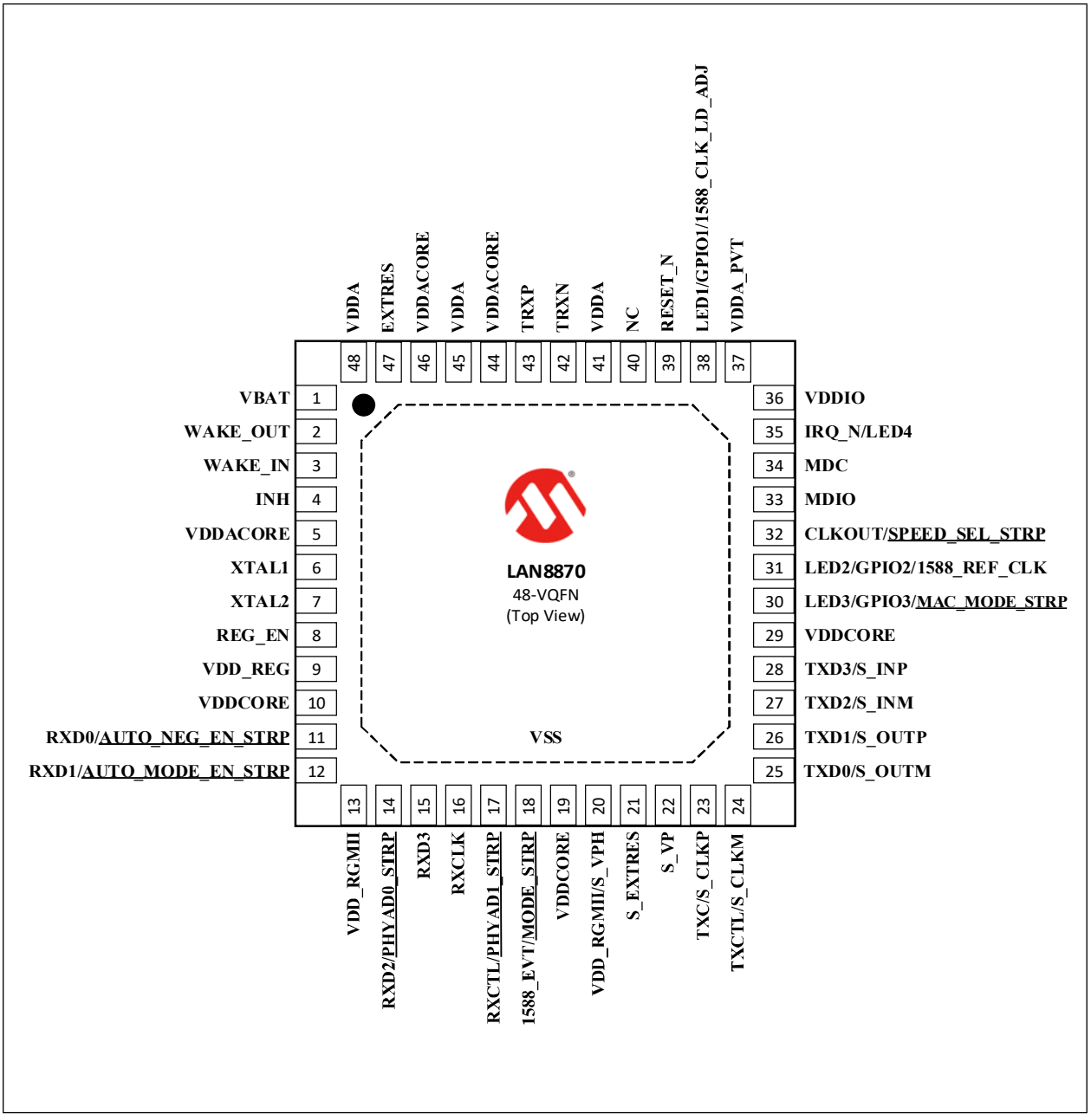
3.0 PIN DESCRIPTIONS

This chapter included the following sections:

- Pin Assignments
- Pin Descriptions
- Configuration Straps

3.1 Pin Assignments

FIGURE 3-1: LAN8870 48-VQFN PIN ASSIGNMENTS

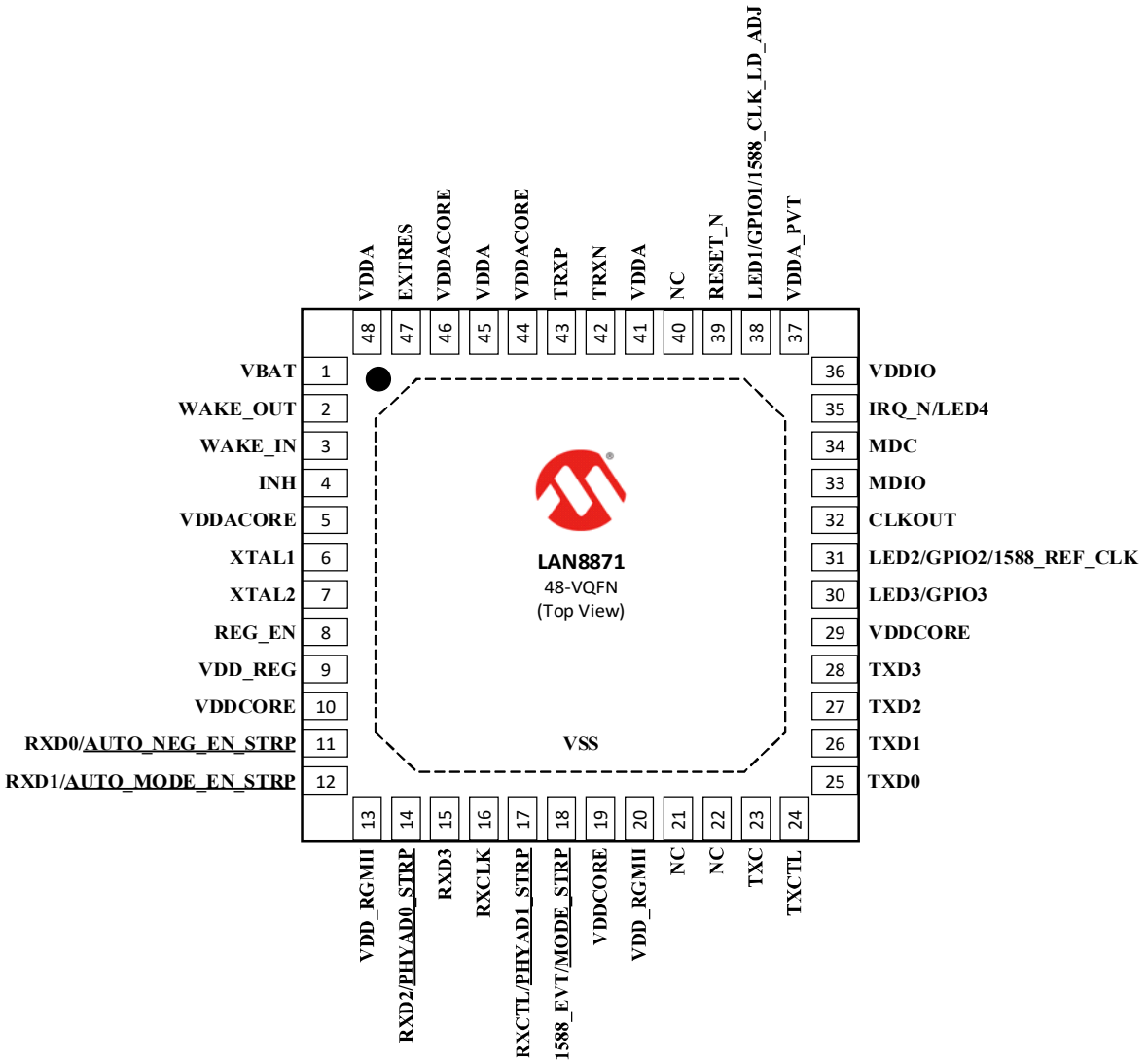


Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

TABLE 3-1: LAN8870 48-VQFN PIN ASSIGNMENTS

Pin Num	Pin Name	Pin Num	Pin Name
1	VBAT	25	TXD0/S_OUTM
2	WAKE_OUT	26	TXD1/S_OUTP
3	WAKE_IN	27	TXD2/S_INM
4	INH	28	TXD3/S_INP
5	VDDACORE	29	VDDCORE
6	XTAL1	30	LED3/GPIO3/MAC_MODE_STRP
7	XTAL2	31	LED2/GPIO2/1588_REF_CLK
8	REG_EN	32	CLKOUT/SPEED_SEL_STRP
9	VDD_REG	33	MDIO
10	VDDCORE	34	MDC
11	RXD0/AUTO_NEG_EN_STRP	35	IRQ_N/LED4
12	RXD1/AUTO_MODE_EN_STRP	36	VDDIO
13	VDD_RGMII	37	VDDA_PVT
14	RXD2/PHYAD0_STRP	38	LED1/GPIO1/1588_CLK_LD_ADJ
15	RXD3	39	RESET_N
16	RXCLK	40	NC
17	RXCTL/PHYAD1_STRP	41	VDDA
18	1588_EVT/MODE_STRP	42	TRXN
19	VDDCORE	43	TRXP
20	VDD_RGMII/S_VPH	44	VDDACORE
21	S_EXTRES	45	VDDA
22	S_VP	46	VDDACORE
23	TXC/S_CLKP	47	EXTRES
24	TXCTL/S_CLKM	48	VDDA
Exposed Pad (VSS) must be connected to ground.			

FIGURE 3-2: LAN8871 48-VQFN PIN ASSIGNMENTS

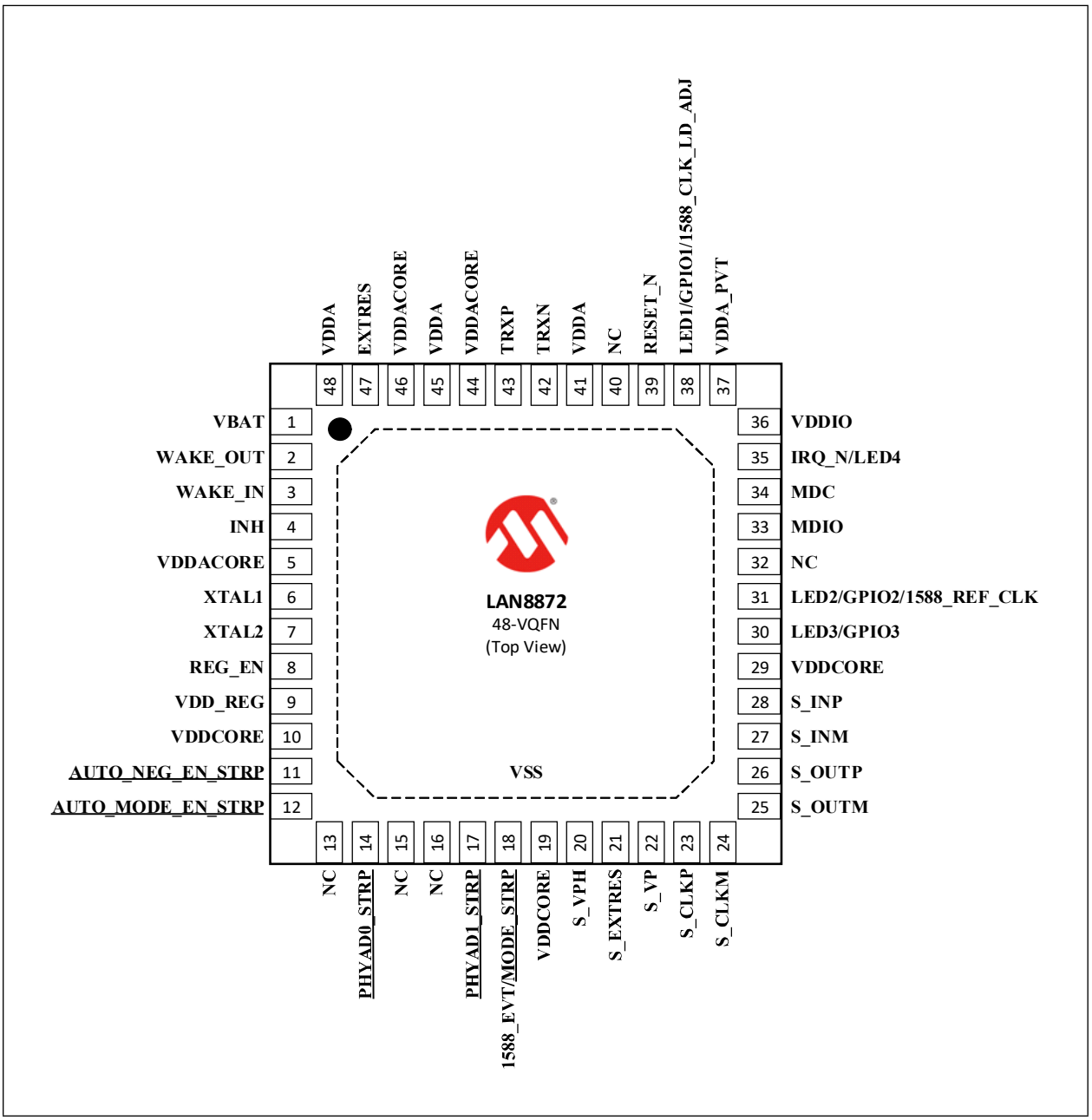


Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

TABLE 3-2: LAN8871 48-VQFN PIN ASSIGNMENTS

Pin Num	Pin Name	Pin Num	Pin Name
1	VBAT	25	TXD0
2	WAKE_OUT	26	TXD1
3	WAKE_IN	27	TXD2
4	INH	28	TXD3
5	VDDACORE	29	VDDCORE
6	XTAL1	30	LED3/GPIO3
7	XTAL2	31	LED2/GPIO2/1588_REF_CLK
8	REG_EN	32	CLKOUT
9	VDD_REG	33	MDIO
10	VDDCORE	34	MDC
11	RXD0/AUTO_NEG_EN_STRP	35	IRQ_N/LED4
12	RXD1/AUTO_MODE_EN_STRP	36	VDDIO
13	VDD_RGMII	37	VDDA_PVT
14	RXD2/PHYAD0_STRP	38	LED1/GPIO1/1588_CLK_LD_ADJ
15	RXD3	39	RESET_N
16	RXCLK	40	NC
17	RXCTL/PHYAD1_STRP	41	VDDA
18	1588_EVT/MODE_STRP	42	TRXN
19	VDDCORE	43	TRXP
20	VDD_RGMII	44	VDDACORE
21	NC	45	VDDA
22	NC	46	VDDACORE
23	TXC	47	EXTRES
24	TXCTL	48	VDDA
Exposed Pad (VSS) must be connected to ground.			

FIGURE 3-3: LAN8872 48-VQFN PIN ASSIGNMENTS



Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

TABLE 3-3: LAN8872 48-VQFN PIN ASSIGNMENTS

Pin Num	Pin Name	Pin Num	Pin Name
1	VBAT	25	S_OUTM
2	WAKE_OUT	26	S_OUTP
3	WAKE_IN	27	S_INM
4	INH	28	S_INP
5	VDDACORE	29	VDDCORE
6	XTAL1	30	LED3/GPIO3
7	XTAL2	31	LED2/GPIO2/1588_REF_CLK
8	REG_EN	32	NC
9	VDD_REG	33	MDIO
10	VDDCORE	34	MDC
11	AUTO_NEG_EN_STRP	35	IRQ_N/LED4
12	AUTO_MODE_EN_STRP	36	VDDIO
13	NC	37	VDDA_PVT
14	PHYAD0_STRP	38	LED1/GPIO1/1588_CLK_LD_ADJ
15	NC	39	RESET_N
16	NC	40	NC
17	PHYAD1_STRP	41	VDDA
18	1588_EVT/MODE_STRP	42	TRXN
19	VDDCORE	43	TRXP
20	S_VPH	44	VDDACORE
21	S_EXTRES	45	VDDA
22	S_VP	46	VDDACORE
23	S_CLKP	47	EXTRES
24	S_CLKM	48	VDDA
Exposed Pad (VSS) must be connected to ground.			

3.2 Pin Descriptions

This section contains descriptions of the various LAN887x pins. The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signal. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

TABLE 3-4: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description
Ethernet			
Ethernet TX/RX Positive Terminal	**TRXP**	AIO	Positive terminal for transmit/receive signal.
Ethernet TX/RX Negative Terminal	**TRXN**	AIO	Negative terminal for transmit/receive signal.
Reference Resistor	**EXTRES**	AI	Reference resistor connection pin for T1 PHY. This pin requires connection of a 12.1KΩ ±1% resistor to ground.
Serial Management Interface			
SMI Data Input/ Output	**MDIO**	VIS-VDDIO/ VO-VDDIO	Serial Management Interface data input/output. **Note:** This pin requires a pull-up resistor with resistance between 1.5KΩ and 10KΩ.
SMI Clock	**MDC**	VIS-VDDIO	Serial Management Interface clock.
RGMII Signals (LAN8870/LAN8871 Only)			
Transmit Data 0	**TXD0**	VIS-VDD_RGMII	Transmit data bus bit 0
Transmit Data 1	**TXD1**	VIS-VDD_RGMII	Transmit data bus bit 1
Transmit Data 2	**TXD2**	VIS-VDD_RGMII	Transmit data bus bit 2
Transmit Data 3	**TXD3**	VIS-VDD_RGMII	Transmit data bus bit 3
Transmit Clock	**TXC**	VIS-VDD_RGMII	Clock used to latch data from the MAC into the transceiver. RGMII: 25/125MHz
Transmit Control	**TXCTL**	VIS-VDD_RGMII	Indicates both the transmit data enable (TXEN) and transmit error (TXER) functions per the RGMII specification. Indicates the presence of valid transmit data and control signals.
Receive Data 0	**RXD0**	VO-VDD_RGMII	Receive data bus bit 0

TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
Receive Data 1	**RXD1**	VO-VDD_RGMII	Receive data bus bit 1
Receive Data 2	**RXD2**	VO-VDD_RGMII	Receive data bus bit 2
Receive Data 3	**RXD3**	VO-VDD_RGMII	Receive data bus bit 3
Receive Clock	**RXCLK**	VO-VDD_RGMII	Receive clock output used to transfer data to the MAC. RGMII: 25/125MHz
Receive Control	**RXCTL**	VO-VDD_RGMII	Indicates both the receive data valid (RXDV) and receive error (RXER) functions per the RGMII specification. Indicates the presence of valid receive data and carrier sense.
Reference Clock Output	**CLKOUT**	VO-VDDIO	Reference clock output to the SoC MAC. Supports crystal clock. 25MHz, 50MHz, and 125MHz. **Note:** This clock is disabled by default.
SGMII Signals (LAN8870/LAN8872 Only)			
SGMII Differential Input Data+	**S_INP**	AI	SGMII differential input data+
SGMII Differential Input Data-	**S_INM**	AI	SGMII differential input data-
SGMII Differential Output Data+	**S_OUTP**	AO	SGMII differential output data+
SGMII Differential Output Data-	**S_OUTM**	AO	SGMII differential input data+
SGMII Differential Clock+	**S_CLKP**	LVDS	SGMII low-swing differential input clock+
SGMII Differential Clock-	**S_CLKM**	LVDS	SGMII low-swing differential input clock-
SGMII Reference Resistor	**S_EXTRES**	AI	SGMII reference resistor. This pin requires connection of a 200Ω ±1% ±100ppm/C resistor to ground. This pin is not connected when LAN8870 is in RGMII mode.
Miscellaneous			
External 25MHz Crystal Input	**XTAL1**	ICLK	External 25MHz crystal input or single-ended clock oscillator.

TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
External 25MHz Crystal Output	**XTAL2**	OCLK	External 25MHz crystal output. **Note:** Do not connect this pin when using a single-ended clock oscillator.
Inhibit	**INH**	VO-VBAT	Inhibit. Used to switch on/off the main external power supply unit. **INH** drives high during normal operation to enable the external power supply. It is high-Z during the sleep state to switch off the external power supply. Inhibit means inhibit shutdown of the external power supply. **Note:** This pin operates off of **VBAT** domain. **Note:** **RESET_N** assertion does not affect the state of this pin. **Note:** This signal is active high. **Note:** This pin is open-source. An external pull-down to ground is required if this pin is used.
Internal Regulator Enable	**REG_EN**	AI	Internal regulator enable. Used to enable the internal voltage regulator for the core voltage domains. When driven high, the regulator is enabled. When driven low, the regulator is disabled.
Wake Input	**WAKE_IN**	VIS-VBAT	Wakeup Input. Asserted to move the part out of sleep. This pin implements the optional wake input described in the TC10 specification. **Note:** This pin operates off of the **VBAT** domain.
Wake Output	**WAKE_OUT**	VO-VBAT	Wake Output. Asserted when the part moves out of sleep. This pin implements the optional wake output described in the TC10 specification. **Note:** This pin operates off of the **VBAT** domain.
LED 1	**LED1**	VOD	LED 1 output. Active low and open-drain.
LED 2	**LED2**	VOD	LED 2 output. Active low and open-drain.
LED 3	**LED3**	VOD	LED 3 output. Active low and open-drain.
LED 4	**LED4**	VOD	LED 4 output. Active low and open-drain. The default function for this pin is **IRQ_N**.
GPIO 1	**GPIO1**	VIS-VDD_RGMII/ VO-VDD_RGMII (PU)	General Purpose Input/Output 1
GPIO 2	**GPIO2**	VIS-VDDIO/ VO-VDDIO (PU)	General Purpose Input/Output 2
GPIO 3	**GPIO3**	VIS-VDDIO/ VO-VDDIO (PU)	General Purpose Input/Output 3
Interrupt	**IRQ_N**	VOD	Device interrupt. Active low and open drain. **Note:** Float pin when unused.

TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
System Reset	**RESET_N**	VIS-VDDIO	System rest. This pin is active low. **Note:** If unused, this pin must be pulled-up to **VDDIO**.
IEEE 1588 Event	**1588_EVT**	VO-VDDIO	IEEE 1588 Event pin
IEEE 1588 Clock Load Adjust	**1588_CLK_LD_ADJ**	VIS-VDD_RGMII	IEEE 1588 Clock Load Adjust pin
IEEE 1588 Reference Clock	**1588_REF_CLK**	VIS-VDDIO	IEEE 1588 Reference Clock pin
No Connect	**NC**	-	No connect. This pin must be left unconnected for proper operation.
Configuration Straps			
Speed Select Configuration Strap	**SPEED_SEL_STRP**	VIS-VDDIO PU	This configuration strap is used to define the default PHY speed. See Section 3.3, Configuration Straps for additional information. (LAN8870 Only)
Auto-Negotiation Enable Configuration Strap	**AUTO_NEG_EN_STRP**	VIS-VDDIO PD	This configuration strap is used to enable auto-negotiation. See Section 3.3, Configuration Straps for additional information.
PHY Address Configuration Strap	**PHYAD[1:0]_STRP**	VIS-VDDIO PD	These configuration straps are used to select the device's default PHY address. See Section 3.3, Configuration Straps for additional information.
Autonomous Mode Enable Configuration Strap	**AUTO_-MODE_EN_STRP**	VIS-VDDIO PD	This configuration strap is used to enable autonomous mode. See Section 3.3, Configuration Straps for additional information.
Autonomous Mode Enable Configuration Strap	**MAC_-MODE_STRP**	VIS-VDDIO PD	This configuration strap is used to enable autonomous mode. See Section 3.3, Configuration Straps for additional information. (LAN8870 Only)
Master/Slave Mode Configuration Strap	**MODE_STRP**	VIS-VDDIO PD	This configuration strap is used to enable autonomous mode. See Section 3.3, Configuration Straps for additional information.
Power/Ground			
Digital Core Power Supply	**VDDCORE**	P	Digital core power supply. All **VDDCORE** pins should be connected together with a 2.2uF capacitor to ground. **Note:** **VDDCORE** is supplied via the internal voltage regulator when **REG_EN** is driven high. When **REG_EN** is low, an external core voltage source is required.

TABLE 3-4: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description
+2.5 SGMII High Power Supply	S_VPH	P	+2.5 SGMII high power supply. This supply must be isolated on the PCB through a ferrite bead. This pin is not connected when LAN8870 is in RGMII mode.
Analog Core Power Supply Input	VDDACORE	P	Analog core power supply input.
SGMII Core/ Transmitter Power Supply Input	S_VP	P	SGMII core/transmitter power supply input. (LAN8870/LAN8872 only) This supply must be isolated on the PCB through a ferrite bead. This pin is not connected when LAN8870 is in RGMII mode.
+1.8V to +3.3V Variable I/O Power Supply Input	VDDIO	P	+1.8V to +3.3V variable I/O power supply input. **Note:** +3.3V is for RGMII operation only
+1.8V to +3.3V Variable RGMII Power Supply Input	VDD_RGMII	P	+1.8V to +3.3V variable RGMII power supply input. (LAN8870/LAN8871 only). This pin is not connected when LAN8870 is in SGMII mode. **Note:** +3.3V is for RGMII operation only
+2.5V to +3.3V Variable Voltage Regulator Power Supply Input	VDD_REG	P	+2.5V to +3.3V variable voltage regulator power supply input. **Note:** +3.3V is for RGMII operation only
+2.5V to +3.3V Variable T1 Power Supply Input	VDDA	P	+2.5V to +3.3V variable T1 power supply input. **Note:** +3.3V is for RGMII operation only
+2.5V to +3.3V Variable VBAT Power Supply Input	VBAT	P	+2.5V to +3.3V variable VBAT power supply input. **Note:** +3.3V is for RGMII operation only
+2.5V to +3.3V Variable PVT Sensor Supply	VDDA_PVT	P	+2.5V to +3.3V variable integrated PVT sensor power supply input. **Note:** +3.3V is for RGMII operation only
Ground	VSS	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

3.3 Configuration Straps

Configuration straps allow various features of the device to be automatically configured to user defined values. Configuration straps are identified by an underlined symbol name and are latched upon the following reset assertions:

- Power-On Reset (POR)
- Pin Reset (**RESET_N**)
- PVT Reset (PVT Sensor)
- Under-Voltage Reset (UV)
- Over-Voltage Reset (OV)
- TC10 Sleep (Indirectly causes POR)

Configuration straps include internal resistors in order to prevent the signal from floating when unconnected. An external pull-up or pull-down resistor must be used to augment the internal resistor to ensure that it reaches the required voltage level prior to latching. The internal resistor can also be overridden by the addition of an external resistor.

3.3.1 SPEED SELECT (SPEED_SEL_STRP)

The **SPEED_SEL_STRP** configuration strap may be used to define the default PHY speed when device is in autonomous mode. When driven high, 1000BASE-T1 is selected. When driven low, 100BASE-T1 is selected. The **SPEED_SEL_STRP** configuration strap applies to LAN8870 only.

When the device is in managed mode, this strap is re-purposed as a **PHYAD[2]** configuration strap and the default speed will be the highest supported speed. The **PHYAD[2]** configuration strap applies to all devices (LAN8870, LAN8871 and LAN8872).

Note:	This strap is ignored when the **AUTONEG_EN_STRP** strap is enabled.

3.3.2 MAC MODE (MAC_MODE_STRP)

This configuration strap sets the MAC_ MODE for the PHY when the device is in autonomous mode, as defined by the **AUTO_MODE_EN_STRP** configuration strap. A value of 1 on this strap selects SGMII; a value of 0 selects RGMII. When the device is in managed mode, this strap is ignored. The **MAC_MODE_STRP** applies to LAN8870 only.

3.3.3 AUTO-NEGOTIATION ENABLE (AUTO_NEG_EN_STRP)

The **AUTO_NEG_EN_STRP** configuration strap may be used to enable auto-negotiation. When driven high, auto-negotiation is enabled. When driven low, negotiation is disabled.

When the device is in managed mode, this strap is re-purposed as a PHYAD[3] configuration strap and the default setting for auto-negotiation will be disabled.

3.3.4 PHY ADDRESS (PHYAD[1:0]_STRP)

The **PHYAD[1:0]** configuration straps are driven high or low to give each PHY a unique address. This address is latched into an internal register at the end of a hardware reset. In a multi transceiver application (such as a repeater), the controller is able to manage each transceiver via the unique address. Each transceiver checks each management data frame for a matching address in the relevant bits. When a match is recognized, the transceiver responds to that particular frame. The PHY address is also used to seed the scrambler. In a multi-transceiver application, this ensures that the scramblers are out of synchronization and disperses the electromagnetic radiation across the frequency spectrum.

When the device is in autonomous mode, only PHYAD[1:0] straps are available and the value of PHYAD[4:2] straps will be ‘000’.

3.3.5 AUTONOMOUS MODE ENABLE (AUTO_MODE_EN_STRP)

The **AUTO_MODE_EN_STRP** configuration strap may be used to enable autonomous mode by default. When driven high, the device is in autonomous mode. When driven low, the device is in managed mode.

When the device is in managed mode, it will not pass traffic until configured appropriately via the SMI interface.

When the device is in autonomous mode, it is capable of passing data without being configured via the SMI interface. This is useful in data converter applications.

Note:	This strap selects alternate functions for the **SPEED_SEL_STRP**, **AUTO_NEG_EN_STRAP**, and **MODE_STRP** configuration straps when the device is in managed mode.

Note:	TC10 and other advanced features are not available in autonomous mode.

3.3.6 MASTER/SLAVE MODE SELECT (MODE_STRP)

The **MODE_STRP** configuration strap may be used to place the PHY in master or slave mode by default. When driven high, the PHY is in master mode. When driven low, the PHY is in slave mode.

Note:	When the device is in managed mode, this strap is re-purposed as a PHYAD[4] configuration strap and the default setting will be slave mode.

4.0 FUNCTIONAL DESCRIPTIONS

This section details various device functions, including:

- Dynamic Channel Quality (DCQ) (TC1/TC12)
- Sleep and Wakeup (TC10)
- Over Temperature Detection
- RGMII (LAN8870/LAN8871 Only)
- SGMII (LAN8870/LAN8872 Only)
- Serial Management Interface (SMI)
- Resets
- Power Management
- LED Operation
- IEEE 1588 (PTP)

4.1 Dynamic Channel Quality (DCQ) (TC1/TC12)

The LAN887x provides dynamic channel quality features that include Mean Square Error (MSE), Signal Quality Indicator (SQI), and peak Mean Square Error (pMSE) values. These features are designed to be compliant with Sections 6.1.1, 6.1.2, and 6.1.3 of both the Open Alliance TC1 - Advanced diagnostics features for 100BASE-T1 automotive Ethernet PHYs Version 1.0 specification and the Open Alliance TC12 - Advanced diagnostics features for 1000BASE-T1 automotive Ethernet PHYs Version 1.0 specification:

- Mean Square Error (MSE)
- Signal Quality Indicator (SQI)
- Peak Mean Square Error (PMSE)

Upon detection of an DCQ error, the DCQ Error Interrupt bit in the Interrupt Source Register asserts. If this interrupt is not masked via the DCQ Error Interrupt Mask bit in the Interrupt Mask Register, the **IRQ_N** pin will assert.

4.1.1 MEAN SQUARE ERROR (MSE)

This section defines the LAN887x implementation of Section 6.1.1 of the TC-1 specification. The LAN887x can provide detailed information on the dynamic signal quality by means of a MSE value.

The MSE value is determined with a refresh rate in the tolerance range of 0.8ms to 2.0ms. The MSE value for 1000/100BASE-T1 is determined across 2^16 (65,536) symbols (summing up and normalization). With a symbol duration of 15ns, this corresponds to a refresh rate of approximately 1.0ms. The resulting MSE value is linearly scaled to a value in the range of [0…511] and the value is placed in the MSE Value bit of the DCQ Mean Square Error Register.

In addition to the current MSE Value, the MSE Worst Case Value since the last read of the speed's MSE Register is stored in the speed's Worst Case MSE Register.

For LAN8870 100BASE-T1, the MSE Measurement Enable bit in the TC1 100BASE-T1 MSE Register must be set to enable 100BASE-T1 MSE Measurement.

For 1000BASE-T1, the 1000BASE-T1 DCQ/SQI Measurement Enable bit in the TC12 1000BASE-T1 DCQ/SQI Measurement Enable Register must be set to enable 1000BASE-T1 MSE measurement.

4.1.2 SIGNAL QUALITY INDICATOR (SQI)

The LAN887x provides two SQI methods:

- SQI Method A: TC-1 Section 6.1.2/TC12-Section 6.1.2 compliant
- SQI Method B: Proprietary method

4.1.2.1 SQI Method A

This section defines the LAN887x implementation of both TC-1 Section 6.1.2 for 100BASE-T1 (LAN8870 only) and TC-12 Section 6.1.2 for 1000BASE-T1.

The SQI value is stored in the speed’s SQI Value field of the speed’s SQI Register in 8 levels (between “000” = worst value and “111” = 7 = best value). In addition to the current SQI value, the lowest SQI value calculated since the last register read access is obtained via the speed’s SQI Register Worst Case Value of the speed’s SQI Register.

For LAN8870 100BASE-T1, both the 100BASE-T1 SQI Measurement Enable bit in the 100BASE-T1 SQI Configuration Register 1 and the 100BASE-T1 MSE and SQI enable bit in the 100BASE-T1 SQI Configuration 2 Register must be set. For 1000BASE-T1, the 1000BASE-T1 DCQ/SQI Measurement Enable bit must be set.

4.1.2.2 SQI Method B

For both 100BASE-T1 (LAN8870 only) and 1000BASE-T1, PAM3 modulation is used for data transmission. In the device, 3 level PAM3 data {-1, 0, +1} is mapped to a slicer reference {-63, 0, +63}. In other words, after proper signal processing in DSP, transmitted data {-1, 0, +1} shall converge to {-63, 0, +63} correspondingly at the slicer input on the RX side under ideal conditions.

However, because of noise and imperfections in real applications, processed RX data may be off from its ideal location, namely {-63, 0, +63}. So based on closest distance, if processed data is above 31.5, it will be decoded as +1; if it is between -31.5~+31.5, it is assigned 0; and if the processed data is smaller than -31.5, it will be decoded as -1.

Slicer error is a measurement of how far the processed data is off from its ideal location. For example, if the slicer error is 29 for a processed data value 34, it is decoded as +1 which corresponds to slicer reference 63, and therefore the slicer error is 63-34=29. A higher absolute slicer error indicates a degraded signal receiving condition.

Slicer error is converted into an absolute value and then filtered by a programmable low pass filter. This is similar to taking the average of absolute slicer error over a long moving time window. For LAN8870 100BASE-T1, the result is in TC1 100BASE-T1 MSE register. For 1000BASE-T1, the result is in TC12 1000BASE-T1 MSE Register.

4.1.3 PEAK MEAN SQUARE ERROR (PMSE)

This section defines the LAN887x implementation of both Section 6.1.3 of the TC-1 Specification and Section 6.1.3 of the TC-12 specification.

The pMSE value is intended to identify transient disturbances which are typically in the micro-second range. The pMSE value is determined from the Mean Square Error of the slicer. The value is determined with a refresh rate of 1 ms.

The pMSE value for 100BASE-T1/1000BASE-T1 is determined by a sliding window over 128 symbols. For each 2^16 (65,536) symbols, the maximum value of this sliding window is stored in the Peak MSE Value field of the DCQ Peak MSE Register. For a symbol duration of 15ns, the sliding window corresponds to a time of approx. 2.0 microseconds. This corresponds to a refresh rate of approximately 1.0ms.

Additionally, the speed's Worst Case Peak MSE Value in the speed's Peak MSE Register contains the highest peak MSE value since the last time this register was read.

For LAN8870 100BASE-T1, the Peak MSE Measurement Enable bit in 100BASE-T1 SQI CONFIGURATION 2 REGISTER must be set to enable 100BASE-T1 pMSE Measurement. For 1000BASE-T1, the 1000BASE-T1 DCQ/SQI Measurement Enable bit in the TC12 1000BASE-T1 DCQ/SQI Measurement Enable Register must be set to enable 1000BASE-T1 pMSE measurement.

4.2 Sleep and Wakeup (TC10)

The TC10 specification defines a mechanism for implementing ultra low power operation while enabling support for partial networking. This section describes the TC10 implementation in this device.

A separate **VBAT** supply is used by the device for wakeup detection when the part is in the SLEEP state. In the SLEEP state **INH** is de-asserted, and as a consequence, the main power supply to the device is cut. The **VBAT** module is responsible for detecting activity on the MDI interface and/or the **WAKE_IN** pin to determine if the part has received wakeup signaling.

4.2.1 MDI WAKEUP

When in SLEEP the device may be awakened via activity on the MDI interface. The wake up signaling monitored is the WUP (Wake-up Packet) defined in the Open Alliance TC10 specification. The WUP consists of 1 ms (+/-300 us) of IDLE signaling.

When the device detects activity on **TRXN/TRXP** it asserts a signal as long as activity is present. A de-bouncing function is used to ensure that false positive wake-ups are not caused by noise, as defined in the TC10 specification. If the debounce is successful, the **INH** pin will assert. Within 1 ms of de-assertion of INH, the main supply to the device will be asserted, as mandated by the TC10 specification. If the debounce fails, the device returns to the IDLE state and continues to monitor for WUP reception.

Note:	In the case of MDI wakeup from the SLEEP state, the device supplies must be externally powered down except for VBAT. This will allow maximum power savings and TC10 power requirements to be met.

4.2.2 WAKE_IN WAKEUP

The **WAKE_IN** pin is monitored for a valid pulse. Per the TC10 specification, pulses with durations of less than 10 ms must be ignored while pulses >40 ms in duration must be recognized. The wake up signaling detected on WAKE_IN may optionally be configured for a pulse of 200 ms in duration.

After determination of a valid pulse, the **INH** pin is asserted. Within 1 ms of de-assertion of **INH** the main supply to the device will be asserted, as mandated by the TC10 specification. After the core voltage is stable and the MDI interface comes up, IDLEs will be transmitted to propagate the wakeup event, if configured.

In the case of **WAKE_IN** wakeup from the SLEEP state, the device supplies will be powered down except for **VBAT**.

The TC10 specification defines a mechanism for implementing ultra low power operation while enabling support for partial networking.

A separate **VBAT** supply is used by the device for wakeup detection when the part is in the SLEEP state. In the SLEEP state, **INH** is de-asserted and as a consequence, the main power supply to the device is cut as shown in Figure 11.6.

This **VBAT** module is responsible for detecting activity on the MDI interface and/or on **WAKE_IN** pin to determine if the part has received wakeup signaling.

4.2.3 INH MODE

The **INH** pin supports two operational modes which are defined by the **INH** Mode bit in the TC10 Configuration Setup Register.

4.2.4 WAKE_IN POLARITY

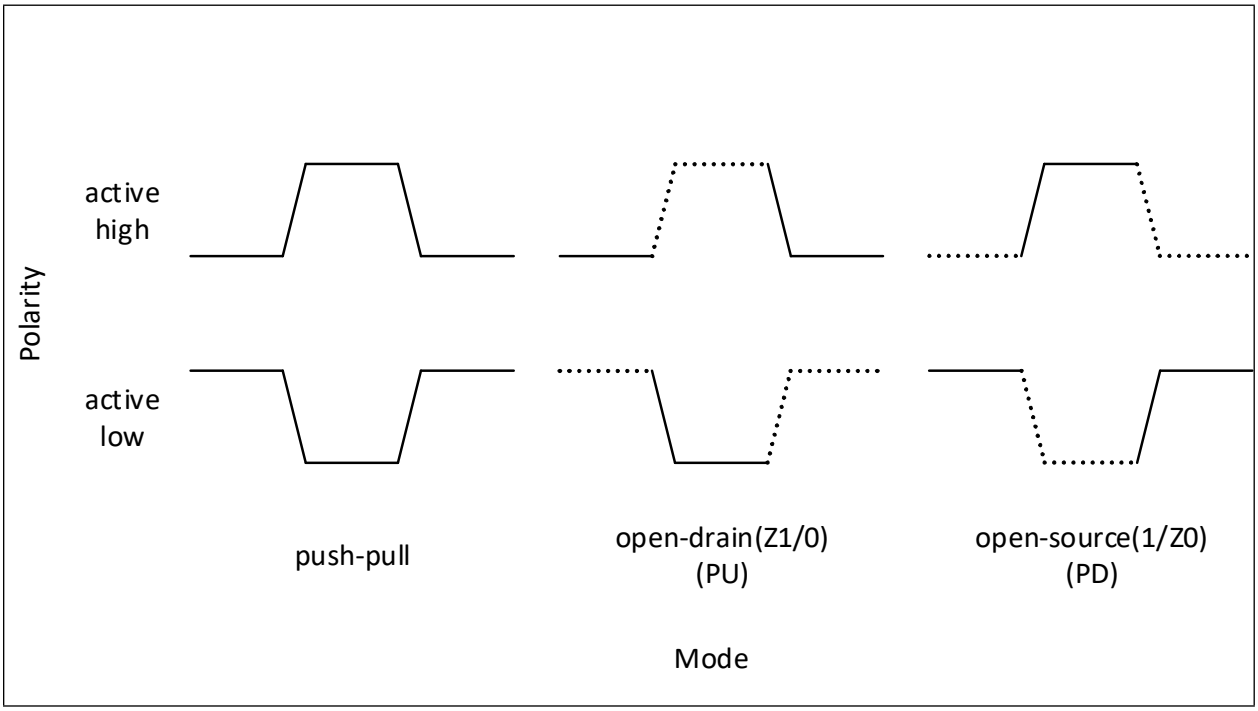
The polarity of the **WAKE_IN** is determined via the **WAKE_IN** Polarity bit in the TC10 Configuration Setup Register.

4.2.5 WAKE_OUT MODE

The polarity of the **WAKE_OUT** is determined via the **WAKE_OUT** Polarity bit in the TC10 Configuration Setup Register.

The mode of operation is determined by the **WAKE_OUT** Mode bit in the TC10 Configuration Setup Register which allows for open-source, open-drain and push-pull operation.

FIGURE 4-1: WAKE_OUT MODES



4.3 Over Temperature Detection

Upon detection of an over temperature condition, the Over-Temperature Error Interrupt bit in the Interrupt Source Register asserts. If this interrupt is not masked via the Over-Temperature Error Interrupt Mask bit in the Interrupt Mask Register, the **IRQ_N** pin will assert.

Regardless of the state of the Over-Temperature Error Interrupt bit, the device disables this function when in the SLEEP, DISABLE, or STANDBY power states.

4.4 RGMII (LAN8870/LAN8871 Only)

The integrated Reduced Gigabit Media Independent Interface (RGMII) provides a common interface between physical layer and MAC layer devices, adhering to the *Reduced Gigabit Media Independent Interface (RGMII) Specification Version 2.0*.

RGMII includes the following interface signals:

- Transmit data - **TXD[3:0]**
- Transmit clock - **TXC**
- Transmit control - **TXCTL**
- Receive data - **RXD[3:0]**
- Receive clock - **RXC**
- Receive control - **RXCTL**

All transmission related signals, **TXC**, **TXD[3:0]** and **TXCTL**, are generated by the MAC device and are inputs to the PHY. The **TXC** transmit clock is used to synchronize the **TXD[3:0]** data and **TXCTL** control signals. All reception related signals, **RXC**, **RXD[3:0]** and **RXCTL**, are generated by the PHY. The **RXC** receive clock is used to synchronize the **RXD[3:0]** data and **RXCTL** control signals.

The RGMII interface supports both Version 1.3 and Version 2.0 of the RGMII specification. Version 1.3 of the RGMII Specification requires a 1.5 to 2ns clock delay via a PCB trace delay. Version 2.0 of the RGMII Specification introduces the option of an on-chip Internal Delay (ID). These distinct RGMII modes of operation are referred to as “Non-ID Mode” and “ID Mode”, respectively, throughout the document.

Refer to the *Reduced Gigabit Media Independent Interface (RGMII) Specification Version 2.0* for additional information.

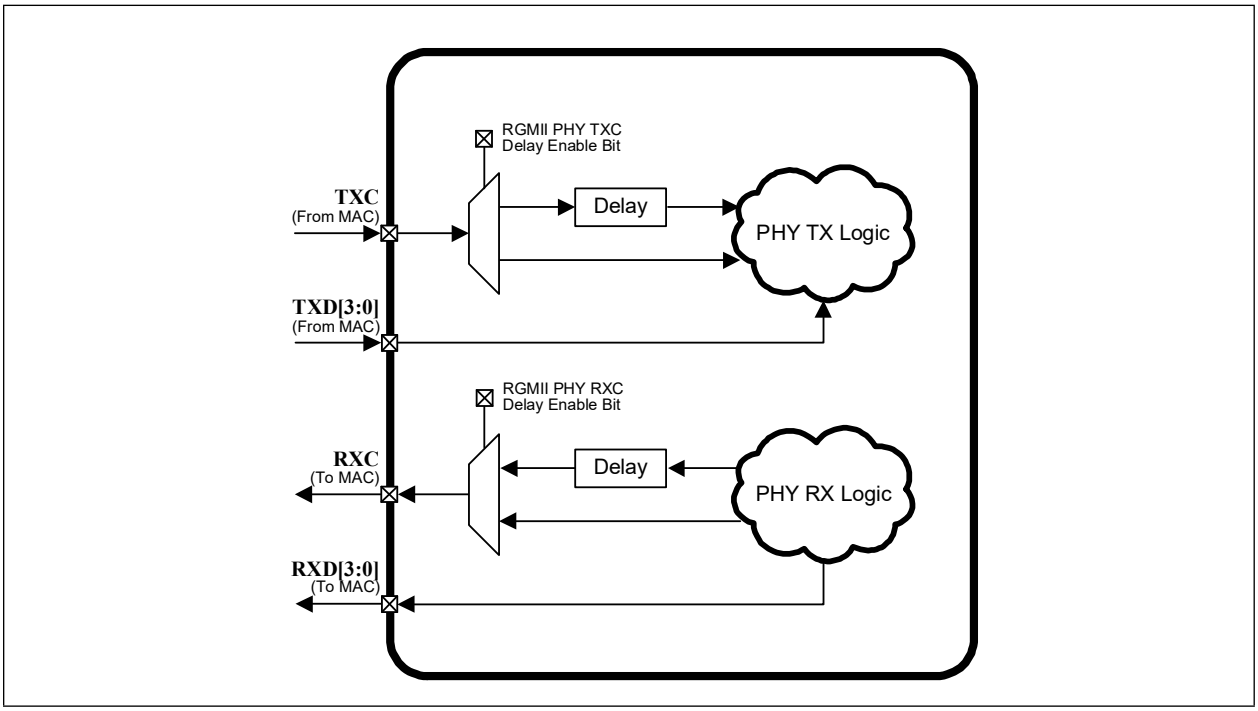
4.4.1 ID MODES

In addition to the standard Non-ID and ID modes of operation, the device supports a hybrid mode of operation, for a total of 3 RGMII modes. The RGMII mode is configured via the RGMII TXC Internal Delay Enable and RGMII RXC Internal Delay Enable bits of the Control 1 Register in the Miscellaneous Registers bank. These modes are summarized below:

- **Non-ID Mode** - Per the RGMII Version 1.3 specification, no internal delay is generated on **TXC** at the MAC, or on **RXC** at this device (PHY). External PCB trace delays are required on **TXC** and **RXC** to meet RGMII timing requirements.
- **ID Mode** - Per the RGMII Version 2.0 specification, an internal delay is generated on **TXC** in the MAC, and an ID is generated on **RXC** in this device (PHY). No PCB trace delay is required.
- **Hybrid Mode** - In this mode, this device (PHY) will generate an ID on both **TXC** and **RXC**. This mode may be used to eliminate the PCB trace delay requirement when utilizing a non-ID MAC. This mode is preferred to Non-ID Mode. Hybrid Mode is achieved by setting both RGMII TXC Internal Delay Enable and RGMII RXC Internal Delay Enable bits.

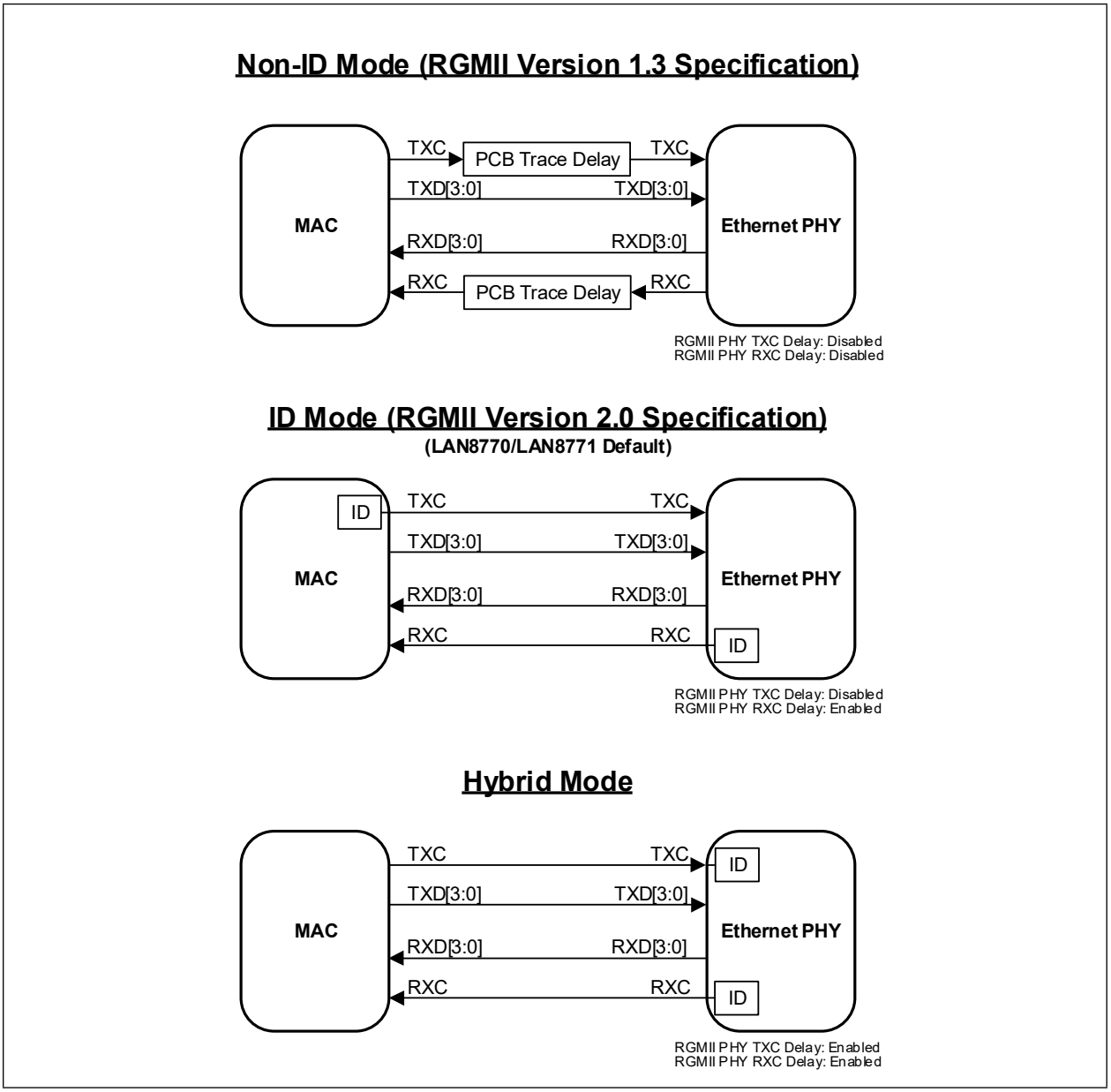
Note:	By default, the TXC internal delay is disabled and the RXC internal delay is enabled.

FIGURE 4-2: RGMII MODE CONFIGURATION LOGIC



The various RGMII modes and their corresponding configuration settings are summarized in Figure 4-3.

FIGURE 4-3: RGMII MODES OF OPERATION



4.5 SGMII (LAN8870/LAN8872 Only)

The integrated Serial Gigabit Media Independent Interface (SGMII) provides a common interface between physical layer and MAC layer devices, adhering to the *Serial-GMII Specification*. SGMII may be used for interfacing the LAN8870/LAN8872 to an external 10/100/1000 BASE-T PHY that supports the SGMII MAC/PHY interface, or to another device with an SGMII interface. This interface also has a SerDes mode for interfacing to 1000BASE-X fiber optic modules or to other modules such as 1000BASE-T which do not support SGMII.

The interface has one receive differential pair and one transmit differential pair for sending and receiving data and control at a serial bit rate of 1.25 G baud. The SGMII block recovers the clock from the incoming data. Therefore, a separate input SGMII clock is not needed. Likewise, no output SGMII clock is provided, with the expectation that the connected device will also recover the clock from the receive data.

SGMII uses auto-negotiation to establish the MAC - PHY connection. The PHY-side device is sometimes referred to as

the leader, and the MAC-side device is referred to as the follower. The PHY-side device relays the following information about the 10/100/1000 BASE-T link to the MAC-side device:

- Speed
- Duplex
- Link up/down status

The switch's SGMII interface defaults to MAC-side mode, with auto-negotiation enabled. The mode can be changed to PHY-side for connection to a MAC-side device. There is also the option to disable auto-negotiation. If auto-negotiation is disabled, it must also be disabled in both devices. Do not confuse "auto-negotiation" across the SGMII interface with auto-negotiation performed between the PHY and its far-end link partner. When the SGMII speed and duplex can be fixed, as when connected to another switch or a processor, auto-negotiation is optional.

100/1000 BASE-T PHYs with SGMII interfaces may be discrete devices or may be housed in SFP modules. Note, however, that not all SFP modules support SGMII.

In SerDes mode, this port uses 1000BASE-X "auto-negotiation". Unlike the SGMII interface where one device acts as a PHY and one acts as a MAC, the SerDes interface is symmetrical between the two connected devices. Besides being compatible with 1000BASE-X fiber modules, it can also interface to a copper 1000BASE-T PHY or module that uses 1000BASE-X auto-negotiation instead of SGMII, and is fixed at 1 Gbps and full duplex. When a PHY is connected to this port, the auto-negotiation is between the switch and the PHY, and this local PHY is known as the link partner. When a 1000BASE-X fiber module is connected to this port, the auto-negotiation is between the PHY and the distant link partner. The fiber module does not participate in the auto-negotiation.

The switch cannot auto-detect the type of SFP module it is attached to, but a management processor can access the SGMII registers and determine whether the received auto-negotiation codeword corresponds to an SGMII device or a SerDes mode device.

AC coupling should be used on the SGMII differential pairs. AC coupling capacitors are included in SFP modules. The SGMII port has internal termination resistors, which eliminates the need for external termination.

4.6 Serial Management Interface (SMI)

The Serial Management Interface is used to control the device and obtain its status. This interface supports the standard PHY registers required by Clause 22 and Clause 45 of the 802.3 standard.

At the system level, SMI provides 2 signals: **MDIO** and **MDC**. The **MDC** signal is an aperiodic clock provided by the station management controller (SMC). **MDIO** is a bi-directional data SMI input/output signal that receives serial data (commands) from the controller SMC and sends serial data (status) to the SMC. There is no maximum time between edges. The minimum cycle time (time between two consecutive rising or two consecutive falling edges) is up to 40 ns. These modest timing requirements allow this interface to be easily driven by the I/O port of a microcontroller.

The data on the **MDIO** line is latched on the rising edge of the **MDC**. The frame structure and timing of the data is shown in Figure 4-4 and Figure 4-5. The timing relationships of the **MDIO** signals are further described in Section 6.6.6, SMI Timing.

FIGURE 4-4: MDIO TIMING AND FRAME STRUCTURE - READ CYCLE

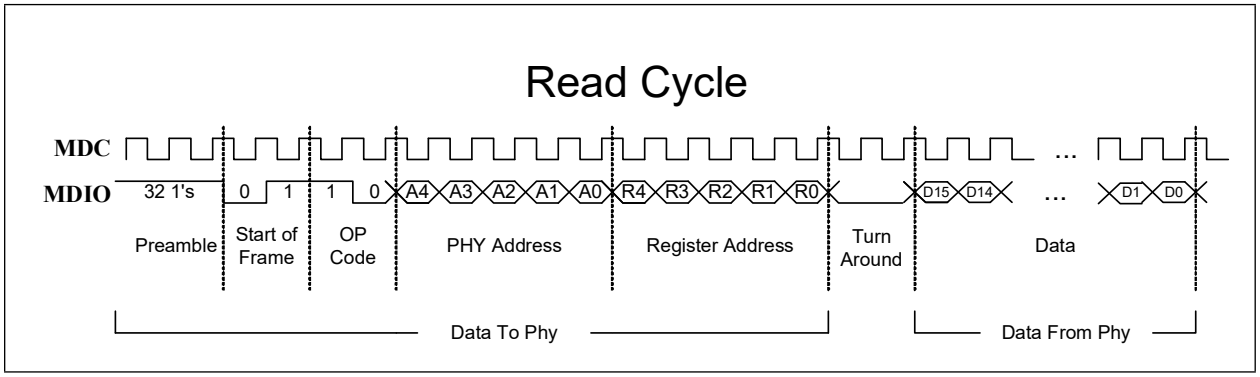
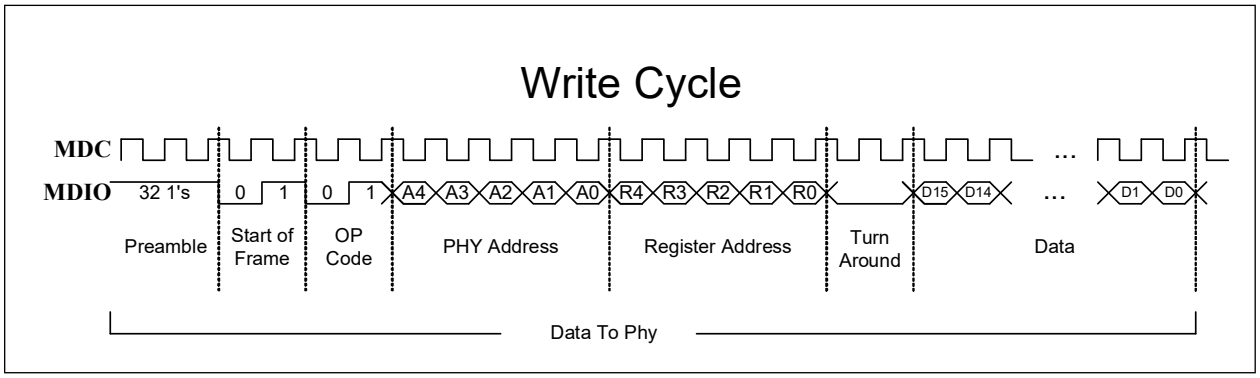


FIGURE 4-5: MDIO TIMING AND FRAME STRUCTURE - WRITE CYCLE



4.7 Resets

The device provides the following chip-level reset sources:

- Power-On Reset (POR)
- External Chip Reset (RESET_N)
- Software Reset
- Under/Over Voltage Reset (UVOV_RESET)
- Over-Temperature Reset
- TC10 Sleep

4.7.1 POWER-ON RESET (POR)

A Power-On reset occurs whenever power is initially applied to the device, or if power is removed and reapplied to the device. A timer within the device will assert the internal reset for approximately 2ms. Configuration straps are loaded by this reset and must adhere to the timing requirements specified in Section , Output timing specifications assume a 25pF equivalent test load, unless otherwise noted, as illustrated in Figure 6-1. when not using the External Chip Reset (RESET_N).

After power-on, the POR initially deasserts after the Rising Threshold is passed. In the event that the supply drops below the Falling Threshold, the POR asserts. The POR stays asserted until the Rising Threshold is once again crossed. The rising and falling thresholds are listed in Table 4-1.

TABLE 4-1: POR THRESHOLDS

POR	Rising Threshold	Falling Threshold
T1 Common (VDDACORE)	0.83 V	0.75 V
T1 Common (VDDA)	2.0 V	1.78 V
VDDIO	1.47 V	1.23 V
RGMII VDDIO	1.47 V	1.23 V
RGMII VDDCORE	0.83 V	0.7 V
VBAT POR (VDDCORE)	0.83 V	0.7 V
VBAT POR (VBAT)	1.92 V	1.64 V

Note: The PORs on **VDDIO** and **VDD_RGMII** are targeted at 1.8 V I/O operation. If a higher voltage is used, an external POR may be required to provide full brown out detection on the I/O domain.

4.7.2 EXTERNAL CHIP RESET (RESET_N)

A hardware reset will occur when the **RESET_N** pin is asserted. The **RESET_N** pin is pulled high internally but must be connected externally to **VDDIO** if unused. If used, the **RESET_N** pin must be driven for a minimum period as defined in Section 6.6.3, RESET_N Configuration Strap Timing. Configuration straps are loaded by the reset.

4.7.3 SOFTWARE RESET

The software reset is available via the PHY Soft Reset (SW_RESET) bit in the Basic Control Register.

4.7.4 UNDER/OVER VOLTAGE RESET (UVOV_RESET)

The device implements under and over voltage protection which may optionally trigger a chip level reset. When configured as a chip level reset there is a reload of the configuration straps. Assertion of this reset shall tune the IO cells.

4.7.5 OVER-TEMPERATURE RESET

This is a chip level reset that occurs from the detecting of an over-temperature event. It can also be configured to force the device into TC10 sleep. This reset does not reload the configuration straps. Threshold2 of the PVT sensor may be configured to trigger an over-temperature reset event.

4.7.6 TC10 SLEEP

A system using TC10 Sleep will typically utilize the INH pin to disabled external power except for the VBAT domain. This will manifest as a POR reset with the exception of the VBAT domain.

4.8 Power Management

A summary of the device's available power states is provided in Table 4-2.

TABLE 4-2: POWER MANAGEMENT SUMMARY

Module	Power-Down/ Standby	Sleep	Active
100Base-T1 PMA/PCS-TX	Off	Note 4-1	On
100Base-T1 PMA/PCS-RX	Off	Note 4-1	On
1000Base-T1 PMA/PCS-TX	Off	Note 4-1	On
1000Base-T1 PMA/PCS-RX	Off	Note 4-1	On
SMI	On	Note 4-1	On
Crystal Oscillator	On	Note 4-1	On
Energy Detection	Off/On	Note 4-1	Off
LDO	On	Note 4-1	On
INH Output	On	Off	On
RESET_N Input	On	Note 4-1	On
WAKE Input	On	On	On
IRQ_N Output	high-ohmic	Note 4-1	On
LED Output	Off	Note 4-1	On/Off
PVT Sensor	Off	Note 4-1	On
MDI Signal Detect	On	On	On

Note: Outputs RXD[3:0], RXER and RXDV are low in POWER-DOWN.

Note 4-1 In the SLEEP state the INH output will assert and turn off external power supplies to the device with the exception of VBAT.

4.9 LED Operation

The device supports the following LED pins:

- LED1
- LED2
- LED3
- LED4

Each LED can be configured for a variety of functions, as detailed in Section 4.9.1, LED Modes.

4.9.1 LED MODES

Table 4-3 lists the supported LED functions.

In addition to static assertion, some LED functions support blink and pulse-stretch operation. Blink is a 50% duty cycle oscillation of asserting and de-asserting the LED pin. Pulse-stretch ensures that the LED pin is asserted and de-asserted for a specific period of time when activity is either present or not present. These rates can also be configured using register settings.

To provide additional power savings, the LEDs (when asserted) can be pulsed at 5 kHz with a programmable duty cycle.

TABLE 4-3: LED MODES

LED Mode	LED State and Description
Activity	1: No RX/TX activity present. 0: RX activity present. Blink or pulse-stretch = Activity present **Note:** Configuration option to support only TX activity present.
Link/Activity	1: No link in any speed on any media interface. 0: Valid link at any speed on any media interface. Blink or pulse-stretch = Valid link at any speed on any media interface with activity present.
Link1000/Activity	1: No link in 1000BASE-T. 0: Valid 1000BASE-T. Blink or pulse-stretch = Valid 1000BASE-T link with activity present.
Link100/Activty	1: No link in 100BASE-T. 0: Valid 100BASE-T. Blink or pulse-stretch = Valid 100BASE-T link with activity present. **Note:** 100BASE-T is LAN8870 only
MODE	1: Master Mode 0: Slave Mode Does not support blink or pulse-stretch.
Force On	De-asserts the LED.
Force Off	Asserts the LED.

4.9.2 LED INTERFACE

The LED interface only supports direct drive. The polarity of the LED output is programmable and can be changed via the appropriate register settings.

The following table summarizes the LED behavior.

TABLE 4-4: LED DRIVE STATE

Setting	Active	NON-active
Default	GND	Tri-State
Alternate Setting	GND	VDD

The LED buffer type is selectable between open-drain/open-source and push-pull and is configured by the LED Buffer Type field in the Output Control Register. If open-drain/open-source is selected, the polarity then determines open-drain (active low) and open-source (active high).

4.10 IEEE 1588 (PTP)

The device provides hardware support for the IEEE 1588-2008 (v2) Precision Time Protocol (PTP), allowing time synchronization with remote Ethernet devices, packet time stamping and time driven event generation.

TABLE 4-5: IEEE-1588 MODES OF OPERATION

Mode	1588 Roles	Notes
Standalone Mode - Full-featured hardware supported time-stamping with standard frame formats	OC Master, OC Slave, E2E TC, P2P TC, BC	Inter-operable with KSZ, LAN and VSC legacy products
Packet Control Header (PCH) Mode - Full-featured hardware supported timestamping with flexible frame formats	OC Master, OC Slave, E2E TC, P2P TC, BC	Inter-operable with VSC switch proprietary MCH mode

Note: Support for the IEEE 1588-2002 (v1) packet format is not provided.

Note on terminology: IEEE 1588 terminology has been updated to align with draft amendment P1588g/D1.2 (March 2022) *Master-Slave Optional Alternative Terminology*. Using this updated terminology, the components of a PTP network are described below:

- **Ordinary Clock (OC):** A PTP instance that has one PTP port, which is operating as either a timeTransmitter or a timeReceiver. A Grandmaster Clock is a special case of an OC/timeTransmitter which is the primary timing source for a given PTP domain.
- **Boundary Clock (BC):** A PTP instance which terminates PTP timing on its timeReceiver port and distributes the recovered PTP timing on one or more timeTransmitter port(s).
- **Transparent Clock (TC):** A PTP instance which passes timing transparently. A TC can be either End to End (E2E TC) or Peer to Peer (P2P TC), and may also be combined with an OC function.

The device may function as a timeTransmitter or a timeReceiver clock per the IEEE 1588-2008 specification. End-to-end and peer-to-peer link delay mechanisms are supported as are one-step and two-step operations.

A 48-bit seconds and 30-bit nanoseconds tunable Local Time Counter is provided that is used as the time source for all PTP timestamp related functions. A 1588 Local Time Events sub-module provides 1588 Local Time Counter comparison based interrupt generation and timestamp-related GPIO event generation. GPIO pins, when configured as an input, can

be used to trigger a timestamp capture or the setting of the tunable Local Time Counter. When configured as an output, the GPIO pins can provide a signal based on a 1588 Local Time Target compare event. All features of the IEEE 1588 unit can be monitored and configured via their respective configuration and status registers.

The device support two basic 1588 operating modes:

- 1588 Standalone Mode Operation, in which the full classification an 1588 processing capabilities are available. This mode is to be used where the host device is not an advanced Microchip switch or other 1588 engine capable of operating with PCH or MCH headers.
- 1588 PCH Mode Operation, in which no classification is available and only limited 1588 processing capabilities are used. This mode is to be used where the host device is an advanced Microchip switch (SparX-5i, etc.) or other 1588 engine capable of operating with PCH or MCH headers.

4.10.1 1588 OPERATION WITH FRAME PREEMPTION

The device supports 1588 timestamping of unfragmented e-frames. Timestamping of 1588 e-frames works in the presence of fragmented or unfragmented p-frames.

4.10.2 1588 STANDALONE MODE OPERATION

4.10.2.1 Standalone Mode RX

In Standalone mode RX, arriving 1588 frames are identified and parsed, and the arrival timestamp is captured and placed into the Timestamp FIFO for use in the RX or TX frame modification block, which modifies PTP Message Timestamps and correctionField (CF).

To interoperate with legacy VSC 1588 PHYs using E2E TC mode, arriving 1588 frames are identified and parsed, and the arrival timestamp is captured and placed in the PTP Message header four-byte Reserved field. The format is 30-bit subseconds with the upper two Reserved bits set to zero, compatible with legacy VSC timestamping PHYs.

UDP checking and updating is as follows:

- UDP/IPv4: verify zero or valid checksum. If invalid, force FCF error. If valid, clear to zero.
- UDP/IPv6: verify non-zero (if enabled) and valid checksum. If invalid, force FCS error. If valid, update checksum pad types (if enabled).

FCS checking and updating is as follows:

- Incrementally update FCS based on all frame modifications. If arriving FCS or UDP checksum fails, ensure departing FCS fails.

4.10.2.2 Standalone Mode TX

In Standalone mode TX, departing 1588 frames are identified and parsed, and the departure timestamp captured and placed into the Timestamp FIFO for use in the TX frame modification block which modifies PTP Message Timestamps and correctionField.

To interoperate with legacy VSC 1588 PHYs using E2E TC mode, departing 1588 frames are identified and parsed. The departure timestamp is captured and the 30-bit subseconds arrival timestamp is extracted from the PTP Message header four-byte Reserved field. The arrival timestamp and departure timestamp are placed into the Timestamp FIFO for use in the TX frame modification block, which updates the PTP Message correctionField as follows:

CF = A (original CF of the frame) + departure timestamp + TX delay – arrival timestamp

TX delay accounts for all known fixed/static plus variable delays from the TX timestamping point to the TX PHY port.

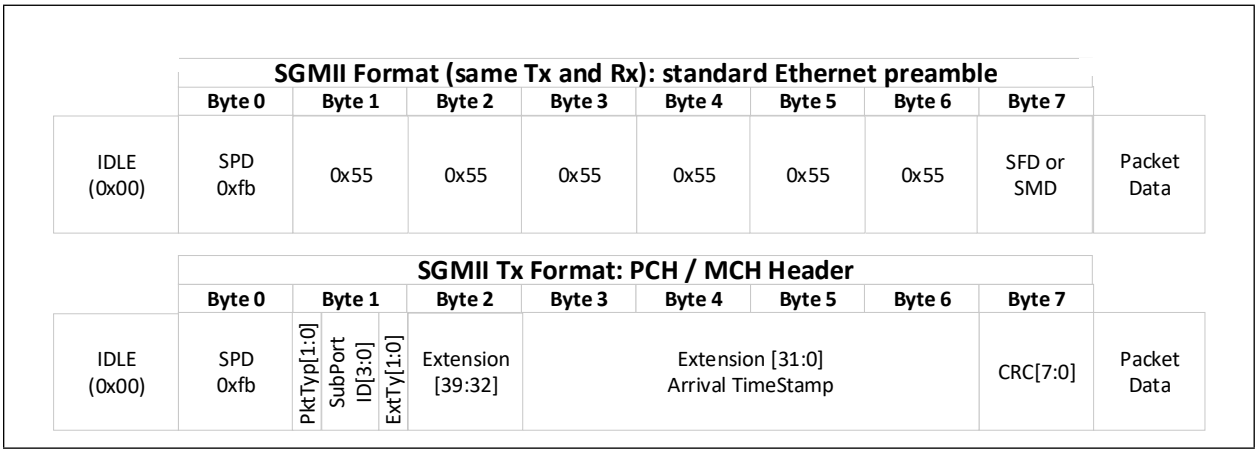
The device also updates the Ethernet FCS and UDP checksum pad bytes (if IPv6 and enabled) accordingly. If IPv4 and enabled, the device clears the UDP checksum field to zeros.

4.10.3 1588 PCH MODE OPERATION

4.10.3.1 PCH Mode RX

In PCH mode RX, arriving 1588 frames are not identified or parsed by the device. All arriving frames are given an arrival timestamp, which is in the ENT RSRV30 format. The preamble is replaced with a PCH/MCH TX header containing the arrival timestamp as shown in Figure 4-6, and this is passed to the SGMII TX functions. Note, SGMII TX and 1588 RX are the same direction, which is PHY to MAC. In this mode, arriving frames must have a minimum of three preamble bytes (e.g., 0x55, 0x55, 0xD5) to be properly handled and passed along toward QSGMII.

FIGURE 4-6: PCH / MCH TX HEADER FORMAT (TOWARD SGMII)



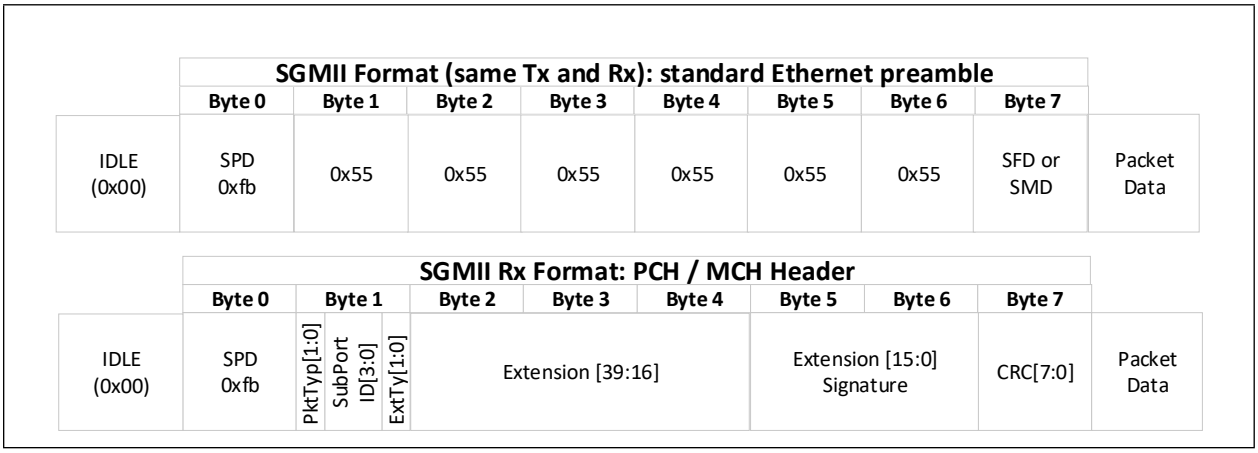
PCH/MCH Bytes 1 and 2 control frame preemption and timestamping. The following values are used:

- PktTyp[1:0]=00 (other values reserved)
- SubPortID[3:0]= Device port number (0, 1, 2, or 3)
- ExtTy[1:0]=01 (preemption disabled on this PHY port) or 10 (preemption enabled on this PHY port). ExtTy will be the same value for all frames on a port.
- Extension[39:32] convey preemption state. Refer to the USGMII specification for details.
  - Preemption Verify and Respond mPackets are passed transparently across the Q-USGMII using Extension values. The device does not generate or respond to these mPackets, it is left to the Q-USGMII link partner to handle Preemption Verification.
- Extension[31:0]=[0,0,30-bit arrival subseconds]
- CRC[7:0]=CRC-8 covering PCH/MCH as per USGMII specification

4.10.3.2 PCH Mode TX

In PCH mode TX, departing frames arrive from the QSGMII RX functions with their preamble replaced with a PCH or MCH RX header. 1588 frames of interest are identified by the device based on PCH or MCH header fields. Note,QSGMII RX and 1588 TX are the same direction, MAC to PHY.

FIGURE 4-7: PCH / MCH TX HEADER FORMAT (TOWARD SGMII)



PCH/MCH Bytes 2-4 control frame preemption and timestamping. The following values are used:

- PktTyp[1:0] = '00'

- SubPortID[3:0] = Device port number (0, 1, 2, or 3)
- Extension[39:32] = convey preemption state. Refer to the SGMII specification for details.
  - Preemption Verify and Respond mPackets are passed transparently across the Q-USGMII using Extension values. The device does not generate or respond to these mPackets, it is left to the Q-USGMII link partner to handle Preemption Verification.
- PCH (preemption enabled, PCH only supports two-step):
  - All frames on the port are expected to have ExtTy[1:0] = '10'.
    - However, frames with ExtTy[1:0] = '00' are treated as valid unfragmented frames. These frames will be passed to the line with valid preambles and will not be counted as Extension Type Mismatch errors.
    - Frames with ExtTy[1:0] = '01' or '11' are treated as invalid frames. They are counted as Extension Type Mismatch errors and discarded by the transmit PHY.
  - Extension[31] = indicates a departure timestamp is to be captured for this frame
  - Extension[15:0] = Signature (two-step Frame Signature)
- PCH (preemption disabled, PCH only supports two-step):
  - All frames on the port are expected to have ExtTy[1:0] = '00' or '01'.
    - ExtTy[1:0] = '00' indicates a frame not needing timestamp functions.
    - ExtTy[1:0] = '01' indicates a frame needing timestamp functions.
    - Frames having ExtTy[1:0] = '10' or '11' are treated as invalid frames. They are counted as Extension Type Mismatch errors and discarded by the transmit PHY.
  - Extension[31] = unused/ignore (ExtTy indicates when a departure timestamp is to be captured for this frame)
  - Extension[15:0] = Signature (two-step Frame Signature)
- MCH: Extension[31] = unused/ignore (DataCmd indicates when a departure timestamp operation is to be performed)
- Extension[30:16] = unused/ignore
- MCH: Extension[15] = indicates one-step or two-step
- MCH (preemption enabled):
  - All frames on the port are expected to have ExtTy[1:0] = '10'.
    - However, frames with ExtTy[1:0] = '00' are treated as valid unfragmented frames. These frames will be passed to the line with valid preambles and will not be counted as Extension Type Mismatch errors.
    - Frames with ExtTy[1:0] = '01' or '11' are treated as invalid frames. They are counted as Extension Type Mismatch errors and discarded by the transmit PHY.
- MCH (preemption disabled):
  - All frames on the port are expected to have ExtTy[1:0] = '01'.
    - However, frames with ExtTy[1:0] = '00' are treated as valid unfragmented frames. These frames will be passed to the line with valid preambles and will not be counted as Extension Type Mismatch errors.
- Frames with ExtTy[1:0] = '10' or '11' are treated as invalid frames. They are counted as Extension Type Mismatch errors and discarded by the transmit PHY. MCH (two-step):
  - Extension[15] = '0'
  - Extension[14:10] = Signature (Frame Signature for two-step operation)
  - Extension[9] = unused/ignore
  - Extension[8:7] = unused/ignore
  - Extension[6:0] = unused/ignore
- MCH (one-step):
  - Extension[15] = '1'
  - Extension[14:10] = unused/ignore
  - Extension[9] = UdpFix.UdpFix = '1' indicates this is a PTP/UDP/IPv6 frame and the two UDP checksum pad bytes are to be incrementally updated.
  - Extension[8:7] = DataCmd[1:0]. DataCmd[1:0] = '10' indicates this is a PTP frame to be timestamped and the correctionField must be updated using the ADD48_CF (48-bit add) operation. Other values of DataCmd[1:0] are unused by the device and must be ignored (these frames are not timestamped).
  - Extension[6:0] = DataOfs[6:0]. For PTP frames where the correctionField must be updated, this provides the sixteen-bit location of the correctionField, starting with the first 16 bits of packet data following MCH CRC(7:0).

- CRC[7:0] = CRC-8 covering PCH/MCH as per SGMII specification

PCH is a standardized header supporting two-step operation using a Frame Signature. Frames with a valid Frame Signature are processed as 1588 frames. For these frames the departure 80-bit timestamp is captured and placed into the Timestamp FIFO along with the Signature [15:0] field to be either read by software over MDIO. Note, the 80-bit timestamp is really only 78 bits, with two bits always set to '00b'.

MCH is a non-standard extension of PCH enabling one-step operation in a PHY without classification capabilities. Frames with MCH DataCmd = '01' = ADD48_CF (48-bit add) are processed as 1588 frames. For these frames, the departure 80-bit timestamp (78 bits plus two bits always set to '00b') is captured and placed into the Timestamp FIFO, along with the following MCH fields:

- For one-step frames, the DataOfs and UdpFix fields are put into the Timestamp FIFO along with the departure timestamp and sent to the Frame Modification block.
- For two-step frames, the Signature[14:0] field is put into the Timestamp FIFO along with the departure timestamp and is either read by software over MDIO or pushed off-chip via the 1588 Serial Timestamp Interface.

PCH/MCH frame signature is read by software via the PTP_TX_MSG_ HEADER2 register. Departure timestamp is read by software via the PTP_TX_SYNC_SEC_HI/MID/LO and PTP_TX_SYNC_NS_HI/LO registers.

The MCH processing essentially implements a TC between the PHY and the switch, where the switch has subtracted an arrival value from CF, and the PHY adds the departure timestamp to CF. All other 1588 operations are performed in the switch.

4.10.4 1588 LOCAL TIME COUNTER

The device contains a single 1588 LTC, shared by the four per-port 1588 Timestamp Engines.

The 1588 LTC is 48 bits of seconds and 30 bits of nanoseconds, plus 32 bits of sub-nanoseconds for precise adjustment. The 1588 LTC runs from a reference clock, which can be either not frequency-locked to any PHY timing (e.g., 250 MHz based on an independent reference), or locked to PHY timing but not at a frequency which is a direct multiple (e.g., 200 MHz based on the same reference clock as PHY timing).

The 1588 LTC is able to be set (initial load) and adjusted using configuration registers, the external **1588_LD_ADJ** pin, and the ePPS. LTC updates from the external **1588_LD_ADJ** pin and ePPS are configurable to be either one-shot or static (repeating).

The following LTC TOD load options are supported:

- Software-based: TOD is loaded from PTP_LTC_SET_x registers when software writes to the PTP_LTC_LOAD register.
- 1PPS: TOD is loaded from PTP_LTC_SET_x registers when a rising edge is detected on the **1588_LD_ADJ** pin.
- 1PPS with TOD: TOD is loaded when a 1PPS rising edge is detected on the **1588_LD_ADJ** pin, and the TOD is also serially encoded on the same pin.

ePPS: TOD is loaded from PTP_LTC_SET_x registers when a PPS is detected on the **1588_REF_CLK** pin.

4.10.5 EXTERNAL 1588 INTERFACE

The device provides the following 1588 I/O pins:

- **1588_REF_CLK**: This input pin can provide an independent reference clock to use with the 1588 LTC functions. Other reference clock options are also supported.
  - This pin also supports Embedded 1 Pulse Per Second (ePPS) capability, where the PPS is coded into the clock signal by moving the falling edge of the clock signal at the appropriate time. ePPS is supported by Microchip Timing products and the SparX-5 at 25 MHz clock.

1588_LD_ADJ: This input pin can be used to synchronize one or more LAN8870/1/2 1588 LTCs with the system 1588 TOD. This pin controls initial setting (load) and incremental update (adjust) of the internal 1588 LTC. It supports the "1PPS" and "1PPS with TOD" modes described in <hyperactive>Section 4.10.4, "1588 Local Time Counter". Note that while this signal is typically a 1PPS, it can also be a non-repeating signal or a signal which repeats at some rate other than 1 Hz.

The 1PPS with TOD format is as follows:

- 1PPS: Rising edge indicates the 1PPS position, the pulse width is 1 µs.
- Waiting: a gap of 20 µs (logic low) between PPS and TOD
- TOD: 16 TOD octets, each occupies 10 µs consisting of a start bit (logic high), eight TOD bits (LSB-first) and a stop bit (logic low).

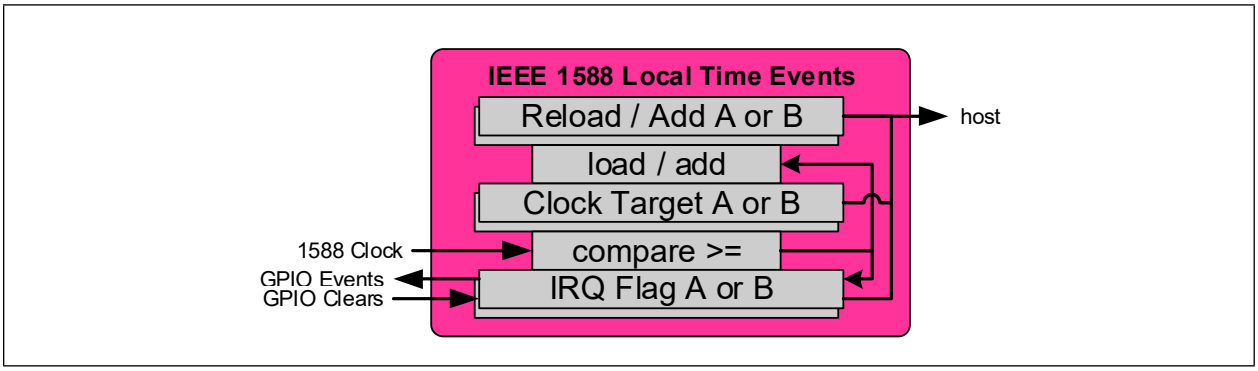
- The first six octets are Seconds in IEEE 1588-2008 format. The device will use these octets to load the LTC.
- The next six octets are Date in 0xYYMMHHMMSS decimal format. These octets are ignored by the device.
- The final four octets are Reserved. These octets are ignored by the device.

• Idle: a gap of 999819 µs (logic low) between TOD and the next PPS rising edge

4.10.6 1588 LOCAL TIME EVENTS

The 1588 Local Time Events block is responsible for generating and controlling all 1588 Local Time related events. Two Local Time event channels, A and B, are available.
A block diagram of the 1588 Local Time Events is shown in Figure 4-8

FIGURE 4-8: 1588 LOCAL TIME EVENTS TARGET BLOCK DIAGRAM



For each Local Time event channel, a comparator compares the 1588 Local Time Counter with a Local Time Target loaded in the PTP LTC Target x Seconds High/Low Registers (PTP_LTC_TARGET_SEC_HI/LO_x) and PTP LTC Target x Nanoseconds High/Low Registers (PTP_LTC_TARGET_NS_HI/LO_x). Only the lower 32 bits of seconds is considered.

The Local Time Target register set requires four 16-bit write cycles, one to each quarter, before the register set is affected. The writes may be in any order. There is a register set for each Local Time event channel (A and B).

The Local Time Target can be read by setting the LTC Target Read (PTP_LTC_TARGET_READ) bit in the PTP Command and Control register (PTP_CMD_CTL). This saves the current value of the both Local Time Targets (A and B) into the PTP LTC Target x Seconds High/Low Registers (PTP_LTC_TARGET_SEC_HI/LO_x) and PTP LTC Target x Nanoseconds High/Low Registers (PTP_LTC_TARGET_NS_HI/LO_x) where they can be read.

When the 1588 Local Time Counter reaches or passes the Local Time Target for a Local Time event channel, a Local Time event occurs, which triggers the following:

• The maskable interrupt for that Local Time event channel (PTP Timer Interrupt A (PTP_TIMER_INT_A) or PTP Timer Interrupt B (PTP_TIMER_INT_B) is set in the PTP Interrupt Status register (PTP_INT_STS).
• The PTP LTC Target x Actual Nanoseconds High/Low Registers is loaded from the nanoseconds portion of the 1588 Local Time Counter.

APPLICATION NOTE: Since the Local Time Target compare is a “greater than equals to” function, it is possible that it triggers with the 1588 Local Time Counter exceeding the Local Time Target value. These registers can be used to account for the variation.

• The Reload/Add A (RELOAD_ADD_A) or Reload/Add B (RELOAD_ADD_B) bit in the PTP General Configuration register (PTP_GENERAL_CONFIG) is checked to determine the new Local Time Target behavior:
  - RELOAD_ADD = ‘1’:
    The new Local Time Target is loaded from the Reload/Add Registers (PTP LTC Target x Reload/Add Seconds High/Low Registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x) and PTP LTC Target x Reload/Add Nanoseconds High/Low Registers (PTP_LTC_TARGET_RELOAD_NS_HI/LO_x)).
  - RELOAD_ADD = ‘0’:
    The Local Time Target is incremented by the Reload/Add Registers (PTP LTC Target x Reload/Add Seconds High/Low Registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x) and PTP LTC Target x Reload/Add Nanoseconds High/Low Registers (PTP_LTC_TARGET_RELOAD_NS_HI/LO_x)). The Local Time Target Nanoseconds rolls over at 10^9 and the carry is added to the Local Time Target Seconds.

The Local Time Target Reload/Add register set requires four 16-bit write cycles, one to each quarter, before the register set is affected. The writes may be in any order. There is a register set for each Local Time event channel (A and B).

Note:	Writing the 1588 Local Time Counter may cause the interrupt event to occur if the new 1588 Local Time Counter value is set equal to or greater than the current Local Time Target.

The Local Time Target reload function (RELOAD_ADD = ‘1’) allows the Host to pre-load the next trigger time in advance. The add function (RELOAD_ADD = ‘0’) allows for a automatic repeatable event.

5.0 APPLICATION DIAGRAMS

This section provides application diagrams for the following:

- RGMII or SGMII Operation
- Remote Wakeup Enabled Configuration
- Power Connectivity

5.1 RGMII or SGMII Operation

Figure 5-1 illustrates device connectivity in RGMII mode. This mode is supported by the LAN8870 and LAN8871.

FIGURE 5-1: RGMII OPERATION

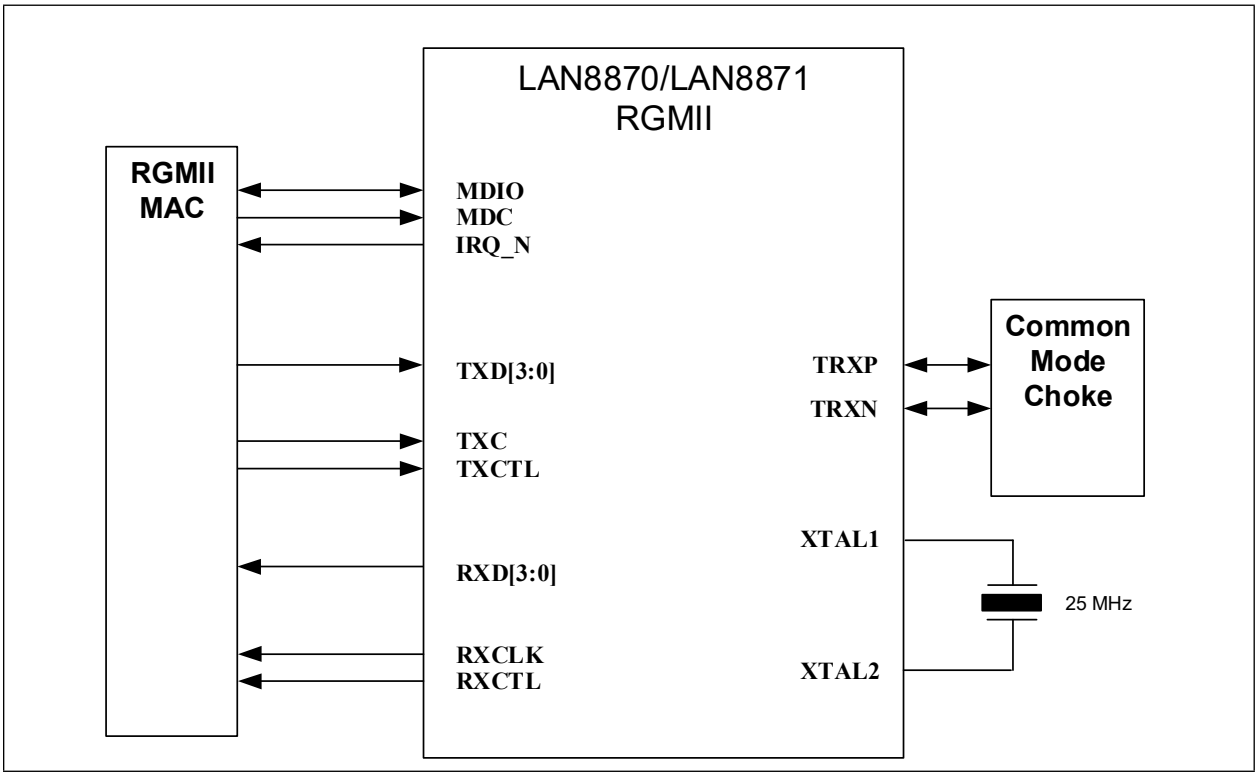


Figure 5-2 illustrates device connectivity in SGMII mode with an internal SGMII reference clock. This mode is supported by the LAN8870 and LAN8872.

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FIGURE 5-2: SGMII OPERATION WITH INTERNAL SGMII REFERENCE CLOCK

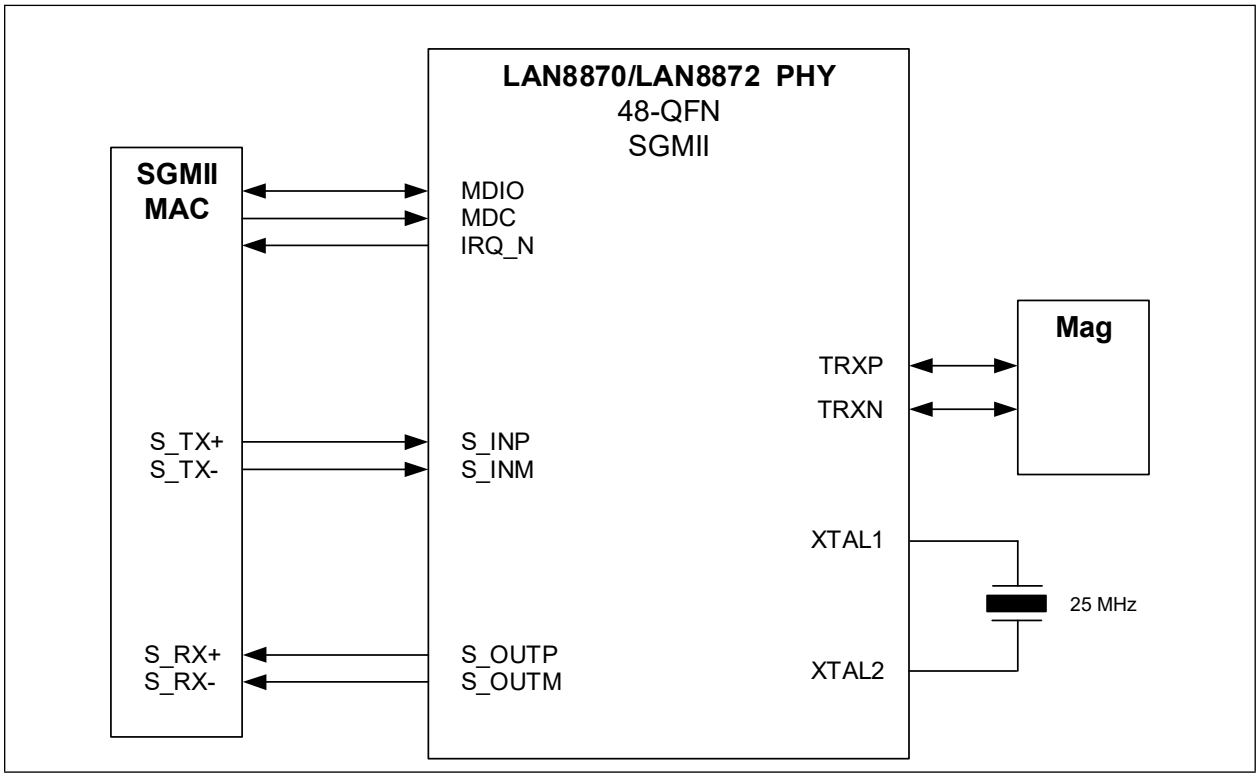
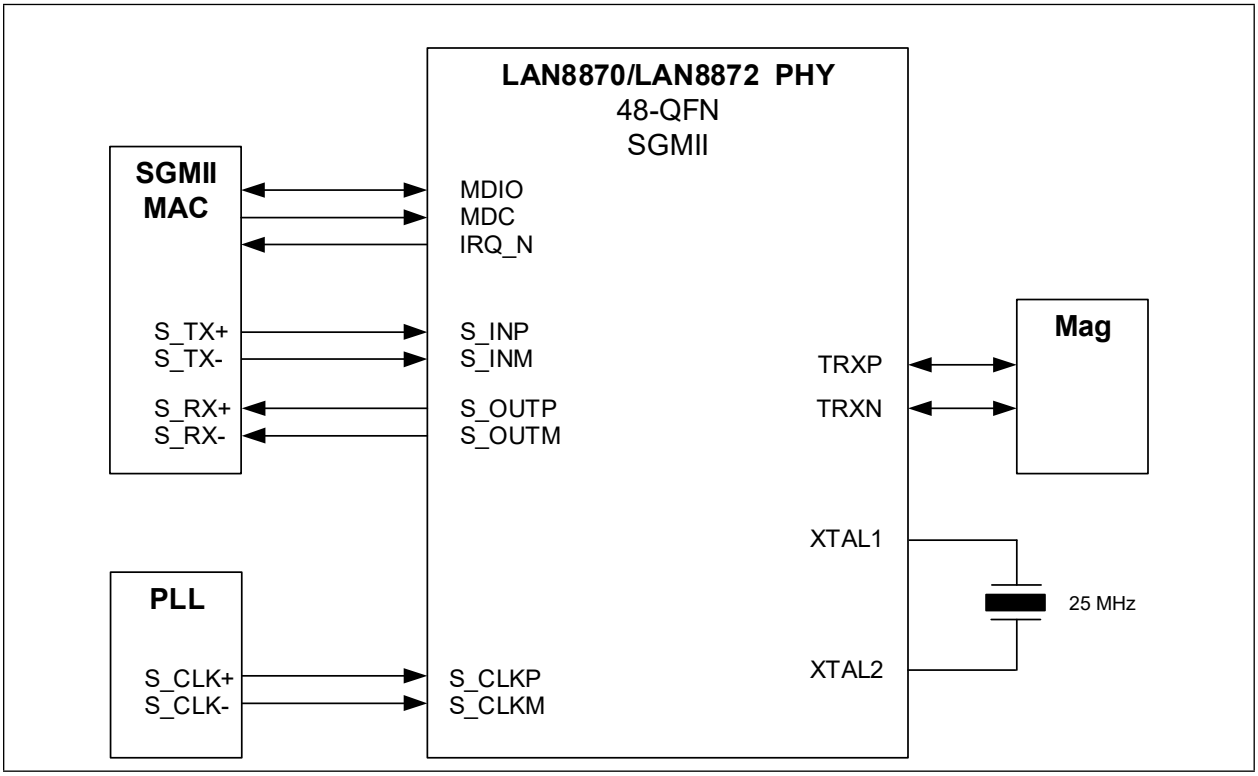


Figure 5-3 illustrates device connectivity in SGMII mode with an external SGMII reference clock. This mode is supported by the LAN8870 and LAN8872.

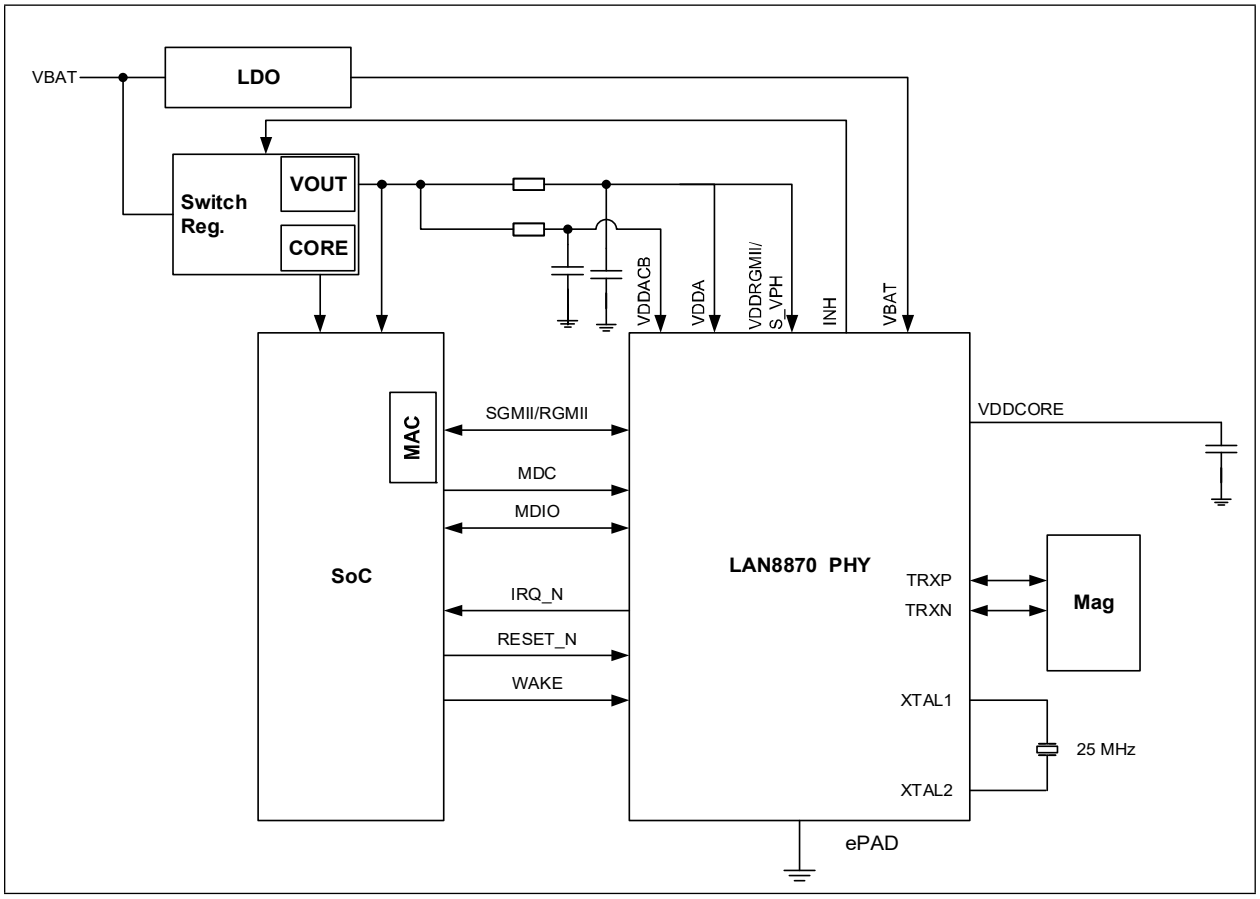
FIGURE 5-3: SGMII OPERATION WITH EXTERNAL SGMII REFERENCE CLOCK



5.2 Remote Wakeup Enabled Configuration

Figure 5-4 illustrates device connectivity in a remote wakeup enabled configuration.

FIGURE 5-4: REMOTE WAKEUP ENABLED CONFIGURATION



5.3 Power Connectivity

Figure 5-5 illustrates device power connectivity when RGMII is active and the LDO controller is not used. Only applies to LAN8870/LAN8871.

FIGURE 5-5: POWER CONNECTIVITY - RGMII (WITHOUT LDO)

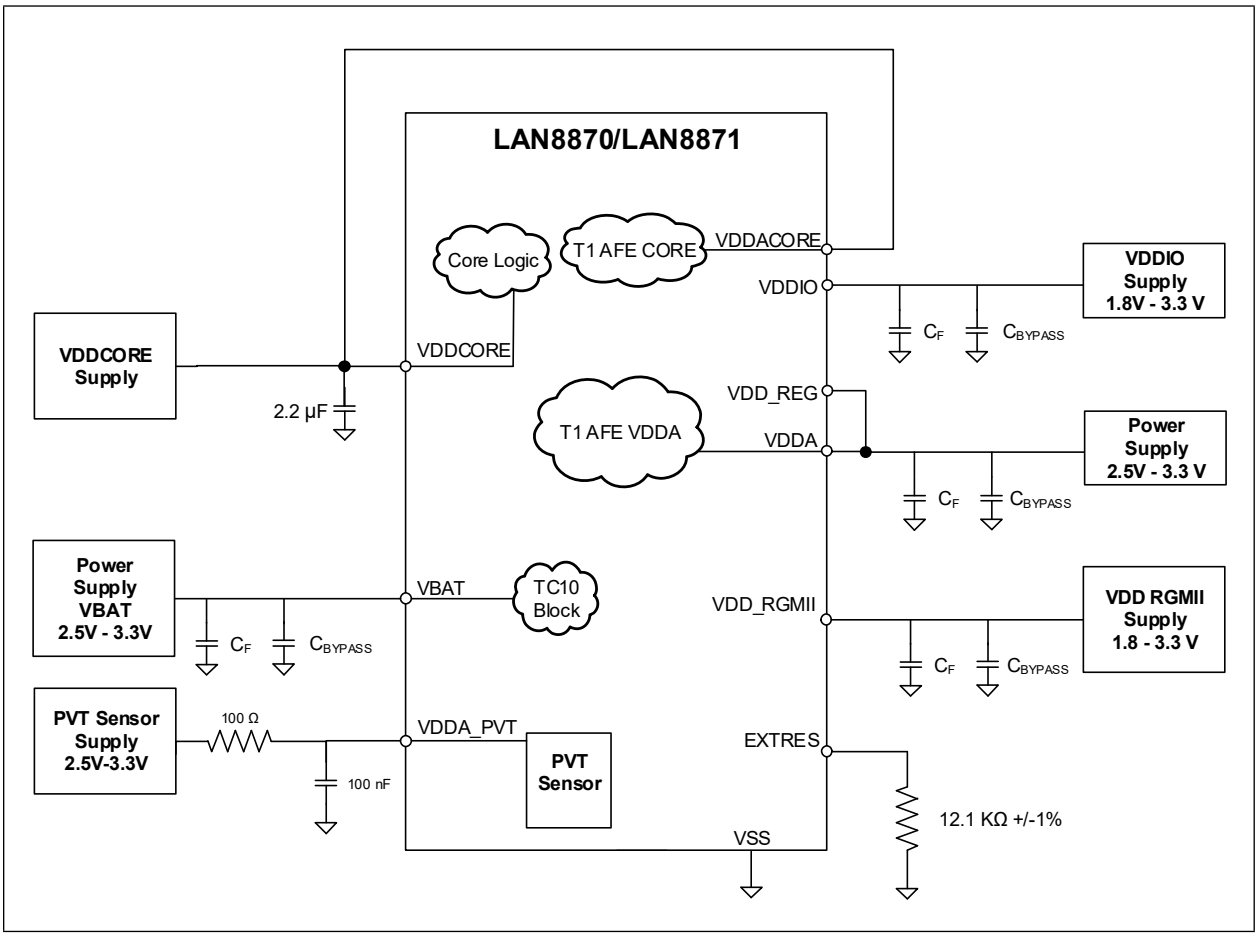
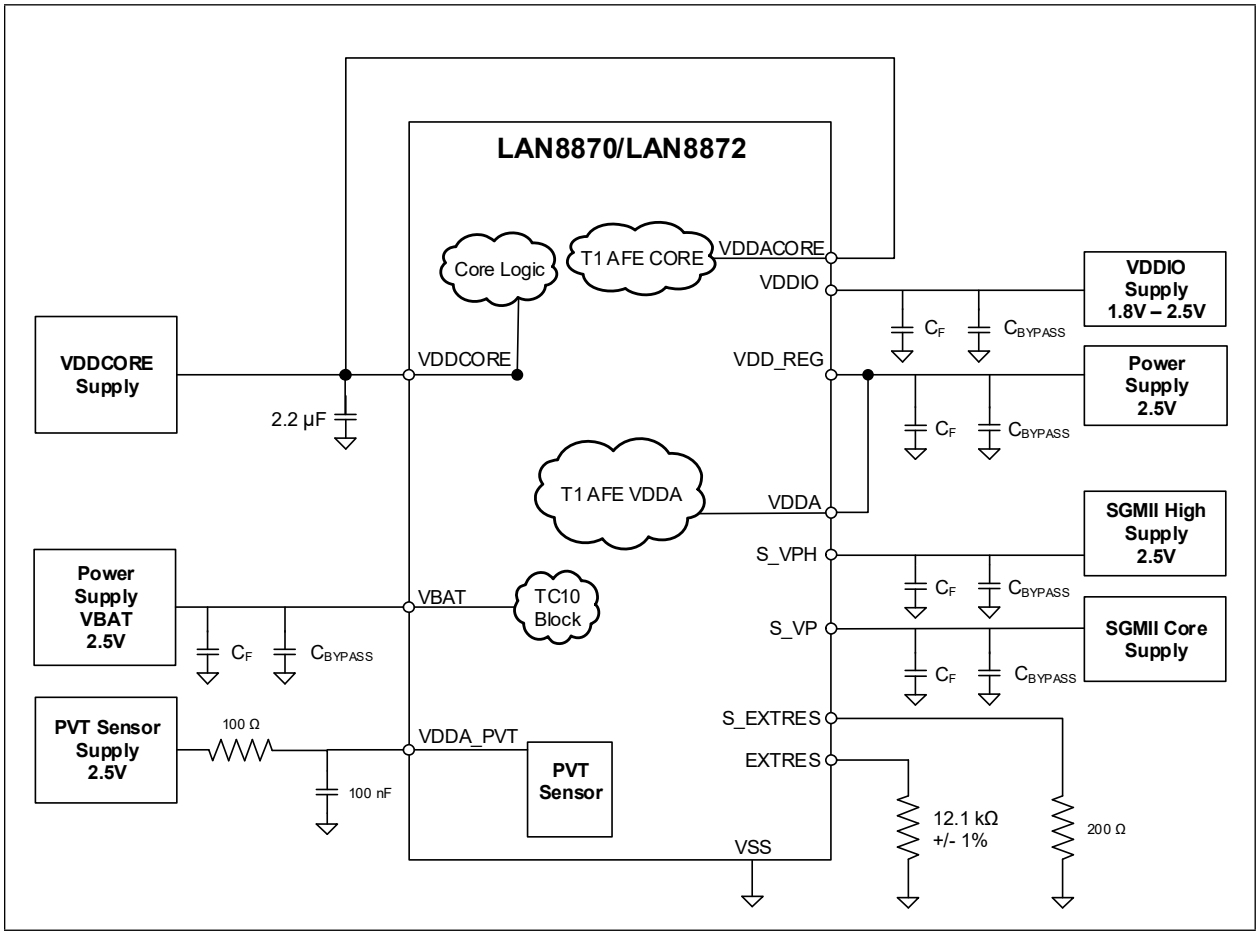


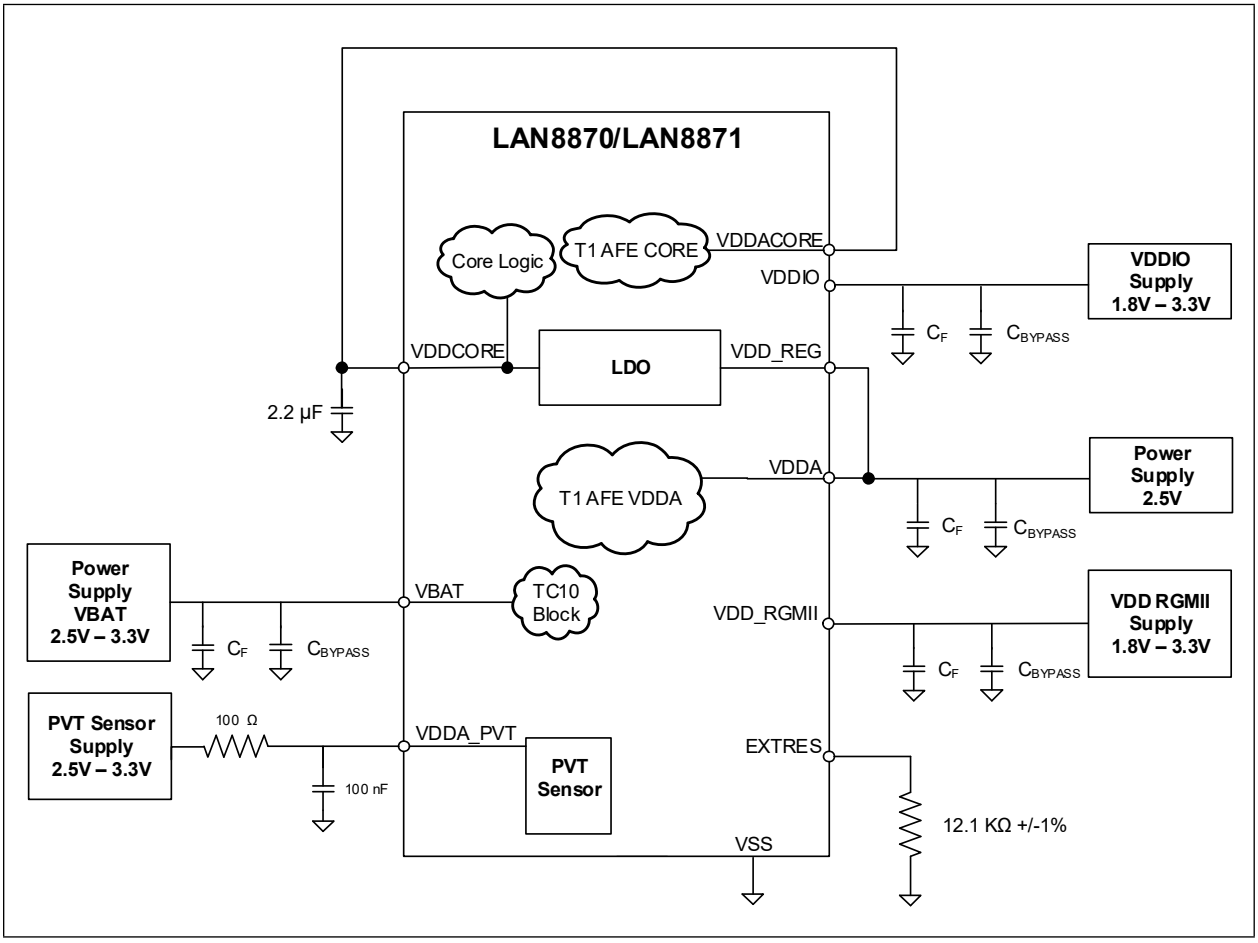
Figure 5-6 illustrates device power connectivity when SGMII is active and the LDO controller is not used. Only applies to LAN8870/LAN8872.

FIGURE 5-6: POWER CONNECTIVITY - SGMII (WITHOUT LDO)



The below power connectivity diagram (Figure 5-7) applies when both RGMII and the LDO controller are used. Only applicable to LAN8870/LAN8871.

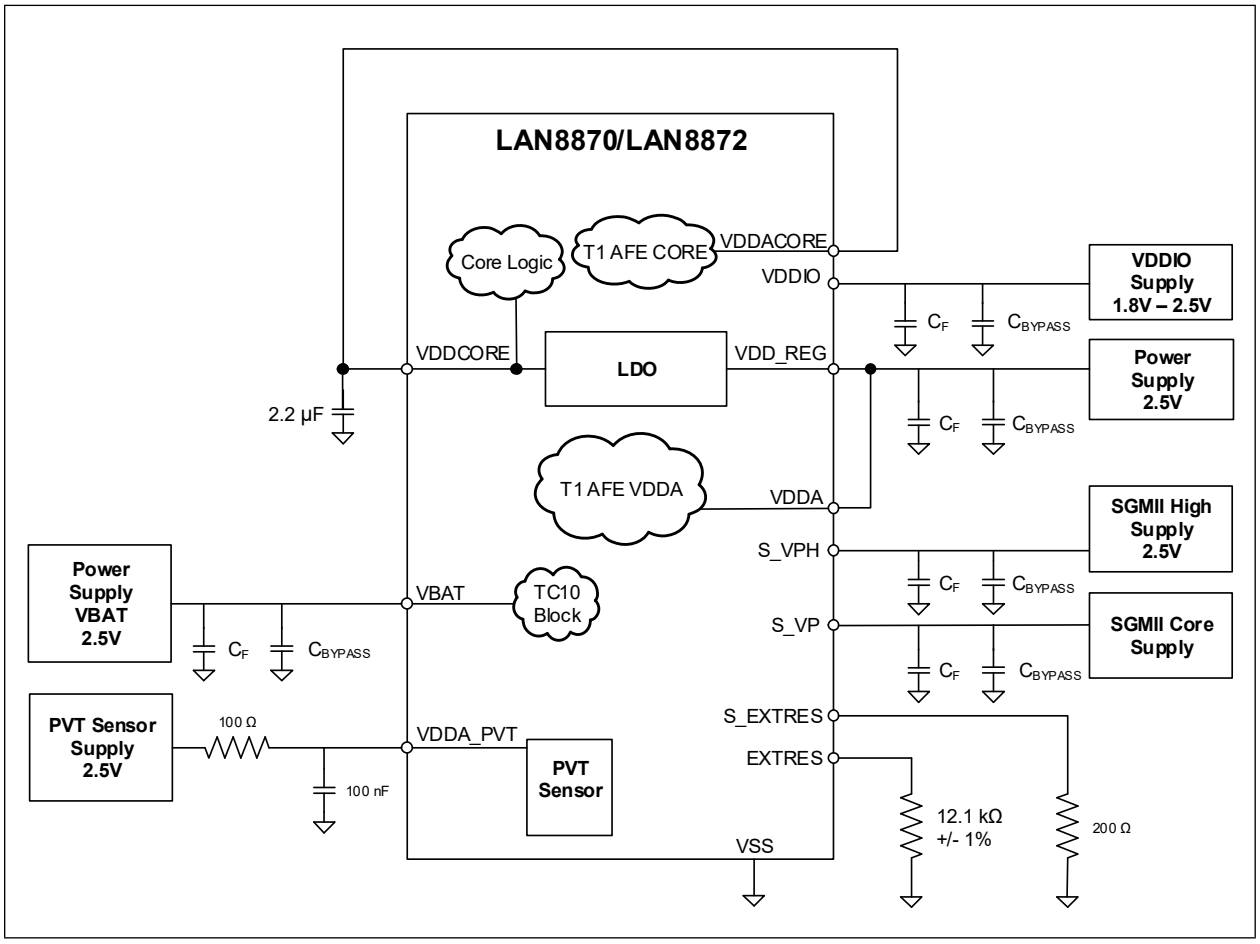
FIGURE 5-7: POWER CONNECTIVITY - RGMII WITH LDO ENABLED



Note: Do not connect **VSSA_PLL** to ground on the board. Let it float, and decouple it to **VDDA_PLL** as shown in Figure 5-7.

The below power connectivity diagram (Figure 5-8) applies to LAN8870/LAN8872 when both the LDO controller and SGMII are used.

FIGURE 5-8: POWER CONNECTIVITY - SGMII WITH LDO ENABLED



6.0 OPERATIONAL CHARACTERISTICS

6.1 Absolute Maximum Ratings*

Supply Voltage (**VDDIO**, **VDD_RGMII**, **VDD_REG**, **VBAT**, **VDDA**, **VDDA_PVT**) (Note 6-1) ..... 0 V to +4.0 V

Supply Voltage (**S_VPH**) ..... 0 V to +3.0 V

Supply Voltage (**VDDCORE**, **VDDACORE**, **S_VP**) ..... 0 V to +1.25 V

Positive voltage on input signal pins, with respect to ground ..... +4.0 V

Negative voltage on input signal pins, with respect to ground ..... -0.5 V

Storage Temperature ..... -55°C to +150°C

Lead Temperature Range ..... Refer to JEDEC Spec. J-STD-020

HBM ESD Performance (**TRXN**, **TRXP**) ..... +/-8 kV

HBM ESD Performance (all others) ..... +/-6 kV

Note 6-1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 6.2, Operating Conditions**, Section 6.5, DC Specifications, or any other applicable section of this specification is not implied.

6.2 Operating Conditions**

Supply Voltage (**VDDCORE**, **VDDACORE**, **S_VP**) ..... +1.067 V to +1.21 V

Supply Voltage (**VDDIO**, **VDD_RGMII**) ..... +1.71 V to +3.465 V

Supply Voltage (**S_VPH**) ..... +2.375 V to +2.625 V

Supply Voltage (**VDD_REG**, **VBAT**, **VDDA**, **VDDA_PVT**) ..... +2.375 V to +3.465 V

Positive voltage on input signal pins, with respect to ground ..... +3.465 V

Negative voltage on input signal pins, with respect to ground ..... -0.3 V

Ambient Operating Temperature in Still Air (T_A) ..... Note 6-2

**Proper operation of the device is guaranteed only within the ranges specified in this section.

Note 6-2 -40°C to 105°C for automotive version, -40°C to 85°C for industrial.

6.3 Package Thermal Specifications

TABLE 6-1: PACKAGE THERMAL PARAMETERS (48-VQFN)

Parameter	Symbol	Value (4-Layer PCB)	Value (6-Layer PCB)	Units	Notes
Junction-to-Ambient	Θ_{JA}	24	19	°C/W	0 Meters/second
		21	17		1 Meters/second
		20	16		2 Meters/second
Junction-to-Top-of-Package	Ψ_{JT}	0.1	0.09	°C/W	0 Meters/second
Junction-to-Case	Θ_{JC}	7.6	7.2	°C/W	0 Meters/second
Junction-to-Board	Θ_{JB}	9.5	8.3	°C/W	

Note: Thermal parameters are measured or estimated for devices in a multi-layer PCB per JESDN51. See Value column for PCB layer details.

6.4 Power Consumption

This section details the device power measurements taken over various operating conditions. Unless otherwise noted, all measurements were taken with power supplies at nominal values. Refer to Section 4.8, Power Management for a description of the power down modes.

6.4.1 REGULATOR DISABLED

TABLE 6-2: RGMII CURRENT CONSUMPTION AND POWER DISSIPATION (REG. DISABLED)

Mode	VDDCORE Current (mA)	VDD Current @3.3V (mA) (Note 6-3)	VDD Current @2.5V (mA) (Note 6-4)	Total Device Power @3.3V (mW)	Total Device Power @2.5V (mW)
SW Power Down	36	43	49	183	163
SLEEP (Note 6-5)	0	0.0145	0.0126	0.048	0.031
RESET	5	4	3	19	13
Link up, no traffic 1000BASE-T1	378	128	118	852	725
Link up, 100% traffic 1000BASE-T1	380	156	142	947	787
Link up, no traffic 100BASE-T1	156	115	106	557	442
Link up, 100% traffic 100BASE-T1	156	118	109	567	450

Note 6-3 This current measurement includes the following power rails at 3.3V: **VDDA**, **VDDA_PVT**, **VBAT**, **VDDIO** and **VDD_RGMII**.

Note 6-4 This current measurement includes the following power rails at 2.5V: **VDDA**, **VDDA_PVT**, **VBAT**, **VDDIO** and **VDD_RGMII**.

Note 6-5 **VDD** current for Sleep Mode is only for **VBAT**. All other power pins are assumed to be unpowered

TABLE 6-3: SGMII CURRENT CONSUMPTION AND POWER DISSIPATION (REG. DISABLED)

Mode	VDDCORE Current (mA)	VDD Current @2.5V (mA) (Note 6-6)	Total Device Power @2.5V (mW)
SW Power Down	36	49	163
SLEEP (Note 6-7)	0	0.0126	0.031
RESET	5	3	13
Link up, no traffic 1000BASE-T1	377	119	726
Link up, 100% traffic 1000BASE-T1	379	120	731
Link up, no traffic 100BASE-T1	156	110	452
Link up, 100% traffic 100BASE-T1	156	110	452

Note 6-6 This current measurement includes the following power rails at 2.5V: **VDDA**, **VDDA_PVT**, **VBAT**, **VDDIO** and **S_VPH**.

Note 6-7 **VDD** current for Sleep Mode is only for **VBAT**. All other power pins are assumed to be unpowered

6.4.2 REGULATOR ENABLED

TABLE 6-4: RGMII CURRENT CONSUMPTION AND POWER DISSIPATION (REG. ENABLED)

Mode	VDD Current @3.3V (mA) (Note 6-9)	VDD Current @2.5V (mA) (Note 6-8)	Total Device Power @3.3V (mW)	Total Device Power @2.5V (mW)
SW Power Down	14	21	46	53
SLEEP (Note 6-10)	0.0147	0.0131	0.048	0.033
RESET	2	2	7	5
Link up, no traffic, 1000BASE-T1	506	501	1670	1253
Link up, 100% traffic, 1000BASE-T1	539	527	1779	1318
Link up, no traffic, 100BASE-T1	267	263	881	658
Link up, 100% traffic, 100BASE-T1	271	266	894	665

Note 6-8 This current measurement includes the following power rails at 2.5V: **VDDA**, **VDDA_PVT**, **VBAT**, **VDDIO** and **VDD_RGMII**. 2.5V **VDDA** is advised for 105°C max ambient operation.

Note 6-9 This current measurement includes the following power rails at 3.3V: **VDDA**, **VDDA_PVT**, **VBAT**, **VDDIO** and **VDD_RGMII**..

Note 6-10 **VDD** current for Sleep Mode is only for **VBAT**. All other power pins are assumed to be unpowered.

TABLE 6-5: SGMII CURRENT CONSUMPTION AND POWER DISSIPATION (REG. ENABLED)

Mode	VDD Current @2.5V (mA) (Note 6-11)	Total Device Power @2.5V (mW)
SW Power Down	21	53
SLEEP (Note 6-12)	0.0131	0.033
RESET	2	5
Link up, no traffic, 1000BASE-T1	499	1248
Link up, 100% traffic, 1000BASE-T1	502	1255
Link up, no traffic, 100BASE-T1	266	665
Link up, 100% traffic, 100BASE-T1	266	665

Note 6-11 This current measurement includes the following power rails at 2.5V: **VDDA**, **VDDA_PVT**, **VBAT**, **VDDIO** and **S_VPH**.

Note 6-12 **VDD** current for Sleep Mode is only for **VBAT**. All other power pins are assumed to be unpowered.

6.5 DC Specifications

TABLE 6-6: DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ 1.8	Typ 2.5	Typ 3.3	Max	Unit	Notes
VIS-VDDIO Type Input Buffer								
Low Input Level	V_{ILI}	-0.3				0.39*VDDIO	V	
High Input Level	V_{IHI}	0.63*VDDIO				3.63	V	
Negative-Going Threshold	V_{ILT}	0.67	0.80	1.1	146	1.68	V	Schmitt
Positive-Going Threshold	V_{IHT}	1.80	0.94	1.25	1.62	1.85	V	Schmitt
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	109.9	149	148	164	219.4	mV	
Input Leakage (V_{IN} = VSS or VDDIO)	I_{IH}	-10				10	µA	Note 6-13
Input Capacitance	C_{IN}					2	pF	

TABLE 6-6: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Min	Typ 1.8	Typ 2.5	Typ 3.3	Max	Unit	Notes
VIS-VDD_RGMII Type Input Buffer								
Low Input Level	V_{ILI}	-0.3				0.39*VDD_RGMII	V	
High Input Level	V_{IHI}	0.63*VDD_RGMII				3.63	V	
Negative-Going Threshold	V_{ILT}	0.67	0.80	1.1	146	1.68	V	Schmitt
Positive-Going Threshold	V_{IHT}	1.80	0.94	1.25	1.62	1.85	V	Schmitt
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	109.9	149	148	164	219.4	mV	
Input Leakage (V_{IN} = VSS or VDD_RGMII)	I_{IH}	-10				10	µA	Note 6-13
Input Capacitance	C_{IN}					2	pF	
VIS-VBAT Type Input Buffer								
Low Input Level	V_{ILI}	-0.3				0.39*VBAT	V	
High Input Level	V_{IHI}	0.63*VBAT				3.63	V	
Negative-Going Threshold	V_{ILT}	0.67	N/A	1.1	1.46	1.68	V	Schmitt
Positive-Going Threshold	V_{IHT}	1.80	N/A	1.25	1.62	1.85	V	Schmitt
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	109.9	N/A	148	164	219.4	mV	
Input Leakage (V_{IN} = VSS or VBAT)	I_{IH}	-10				10	µA	Note 6-13
Input Capacitance	C_{IN}					2	pF	
VO-VDDIO Type Output Buffer								
Low Output Level	V_{OL}					0.6	V	
High Output Level	V_{OH}	VDDIO - 0.6					V	
VO-VDD_RGMII Type Output Buffer								
Low Output Level	V_{OL}					0.6	V	
High Output Level	V_{OH}	VDD_RGMII - 0.6					V	
VO-VBAT Type Output Buffer								
Low Output Level	V_{OL}					0.6	V	
High Output Level	V_{OH}	VBAT - 0.6					V	
VOD Type Output Buffer								
Low Output Level	V_{OL}					0.6	V	

TABLE 6-6: DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Min	Typ 1.8	Typ 2.5	Typ 3.3	Max	Unit	Notes
ICLK Type Input Buffer								Note 6-14
Low Input Level	V_{IL}					0.475	V	
High Input Level	V_{IH}	VDDCORE - 0.35					V	
Input Leakage	I_{IH}	-10				10	µA	

Note 6-13 This specification applies to all inputs and tri-stated bi-directional pins. Internal pull-down and pull-up resistors add +/- 50 µA per-pin (typical).

Note 6-14 XTAL1 can optionally be driven from a 25 MHz single-ended clock oscillator to which these specifications apply.

6.6 AC Specifications

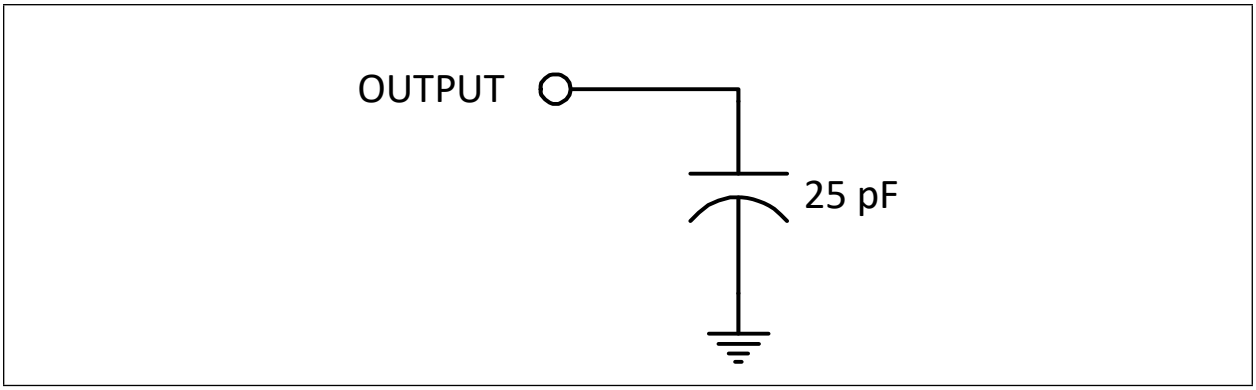
This section details the various AC timing specifications of the device.

Note: The Ethernet TX/RX pin timing adheres to the IEEE 802.3bw specification. Refer to the IEEE 802.3bw specification for detailed Ethernet timing information.

6.6.1 EQUIVALENT TEST LOAD

Output timing specifications assume a 25pF equivalent test load, unless otherwise noted, as illustrated in Figure 6-1.

FIGURE 6-1: OUTPUT EQUIVALENT TEST LOAD



6.6.2 POWER-ON CONFIGURATION STRAP TIMING

Figure 6-2 illustrates the configuration strap timing requirements, in relation to power-on, for applications where **RESET_N** is not used at power-on. The operational level (V_{opp}) for the external power supply is detailed in Section 6.2, Operating Conditions**.

FIGURE 6-2: POWER-ON CONFIGURATION STRAP TIMING

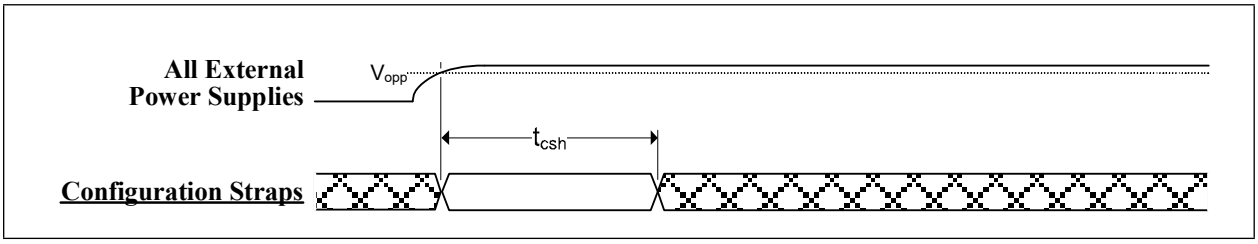


TABLE 6-7: POWER-ON CONFIGURATION STRAP TIMING

Symbol	Description	Min	Typ	Max	Units
t_{csh}	Configuration strap hold after external power supply at operational level	3			ms

6.6.3 RESET_N CONFIGURATION STRAP TIMING

Figure 6-3 illustrates the **RESET_N** timing requirements and its relation to the configuration straps. Assertion of **RESET_N** is not a requirement. However, if used, it must be asserted for the minimum period specified.

FIGURE 6-3: RESET_N CONFIGURATION STRAP TIMING

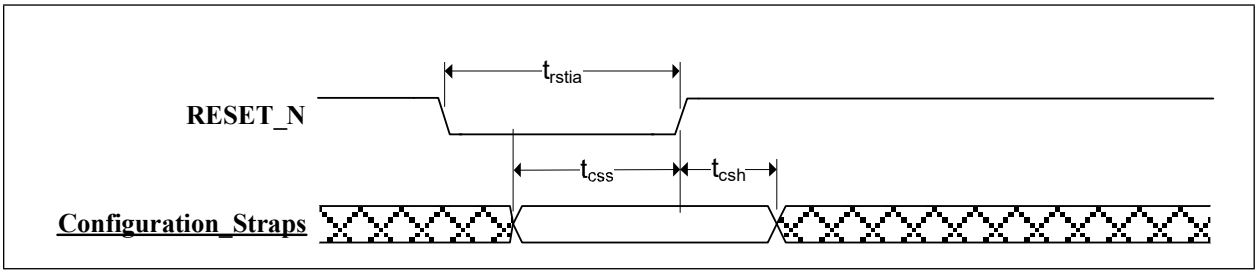


TABLE 6-8: RESET_N CONFIGURATION STRAP TIMING

Symbol	Description	Min	Typ	Max	Units
t_{rstia}	**RESET_N** input assertion time	40			ns
t_{css}	Configuration strap setup before **RESET_N** deassertion	20			ns
t_{csh}	Configuration strap hold after **RESET_N** deassertion	40			ns

6.6.4 POWER SEQUENCE TIMING

Power supplies must adhere to the following rules:

- All power supplies of the same voltage must be powered up/down together.
- There is no power-up sequencing requirement, however all power supplies must reach operational levels within the time periods specified in Table 6-9.
- There is no power-down sequencing or timing requirement, however the device must not be powered for an extended period of time without all supplies at operational levels.
- Following initial power-on, or if a power supply brownout occurs (i.e., one or more supplies drops below operational limits), a power-on reset must be executed once all power supplies reach operational levels. Refer to Section , Output timing specifications assume a 25pF equivalent test load, unless otherwise noted, as illustrated in Figure 6-1. for power-on reset requirements.
- Do not drive input signals without power supplied to the device.

Note: Violation of these specifications may damage the device.

FIGURE 6-4: POWER SEQUENCE TIMING

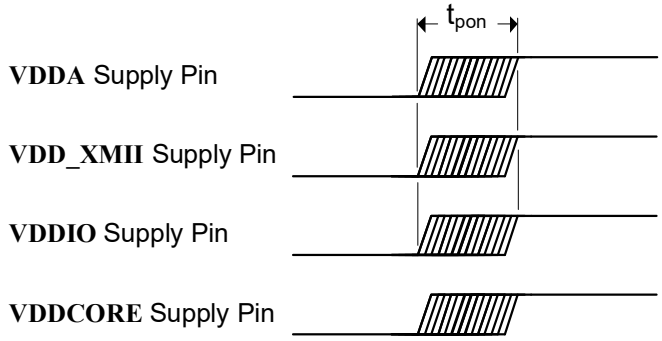


TABLE 6-9: POWER SEQUENCE TIMING

Symbol	Description	Min	Typ	Max	Units
t_{pon}	Power supply turn-on time	0		50	ms

Note: The **VDDIO** power supply can be run at 1.8V, 2.5V, or 3.3V.

Note: The **VDD_XMII** refers to **VDD_RGMII** for RGMII and **S_VPH** for SGMII.

Note: The **VDD_RGMII** power supply can be run at 1.8V, 2.5V, or 3.3V.

Note: The **S_VPH** power supply can be run at 2.5V.

6.6.5 RGMII TIMING (LAN8870/LAN8871 ONLY)

This section specifies the RGMII interface transmit and receive timing. The RGMII interface supports the independent enabling/disabling of the PHY **TXC** and **RXC** delays, each with unique timing properties. These timing are reflected in the following sub-sections.RGMII Transmit Timing (TXC Internal Delay Disabled - MAC Provides Delayed Clock)

Note:	All RGMII timing specifications assume a point-to-point test circuit as defined in Figure 3 of the RGMII specification 2.0.

6.6.5.1 RGMII Transmit Timing (TXC Internal Delay Disabled - MAC Provides Delayed Clock)

FIGURE 6-5: RGMII TRANSMIT TIMING (TXC INTERNAL DELAY DISABLED)

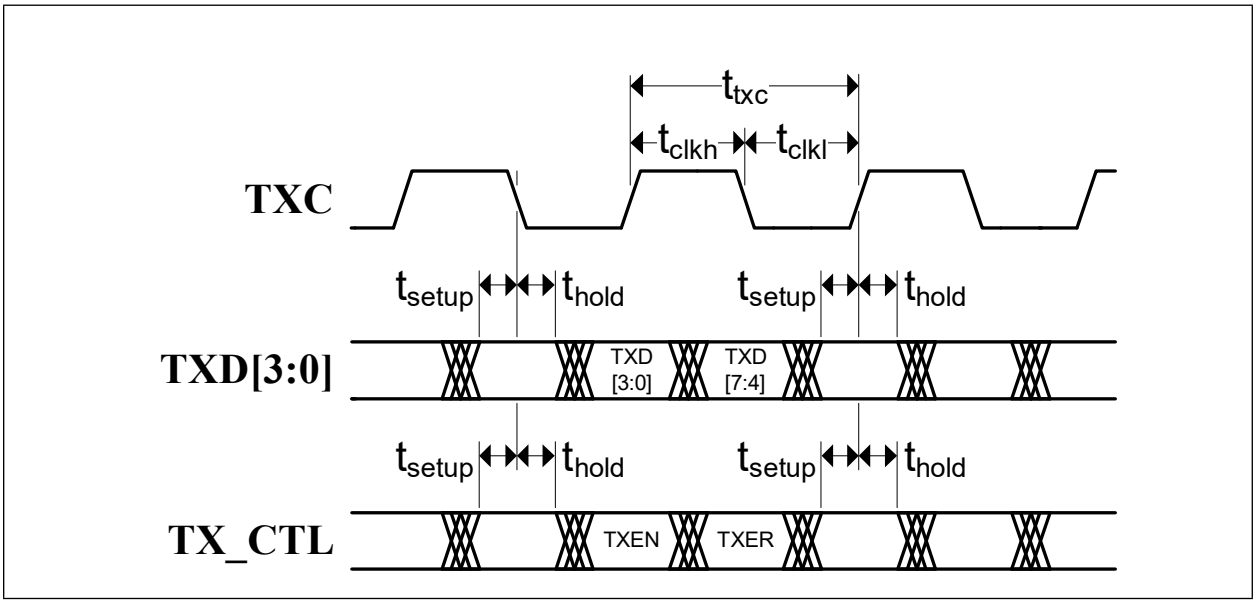


TABLE 6-10: RGMII TXC INTERNAL DELAY DISABLED (RGMII ID MODE / TC6 DoS MODE) TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{txc}	**TXC** period	Note 6-15	Note 6-16	Note 6-17	ns
t_{clkh}	**TXC** high time	Note 6-18	50	Note 6-19	%
t_{clkl}	**TXC** low time	Note 6-18	50	Note 6-19	%
t_{setup}	**TXD[3:0]**, **TX_CTL** setup time to edge of **TXC** (at inputs)	0.8 Note 6-20	2.0		ns
t_{hold}	**TXD[3:0]**, **TX_CTL** hold time after edge of **TXC** (at inputs)	0.8 Note 6-20	2.0		ns

Note 6-15 7.2ns for 1000Mbps operation and 36ns for 100Mbps operation. Minimum limits are non-sustainable long term.

Note 6-16 8ns for 1000Mbps operation and 40ns for 100Mbps operation.

Note 6-17 8.8ns for 1000Mbps operation and 44ns for 100Mbps operation. Maximum limits are non-sustainable long term.

Note 6-18 45% for 1000Mbps operation and 40% for 100Mbps.

Note 6-19 55% for 1000Mbps operation and 60% for 100Mbps.

Note 6-20 These values provide 0.2 ns margin beyond the RGMII specification and 0.25 ns margin beyond the TC6 specification.

6.6.5.2 RGMII Receive Timing (RXC Internal Delay Enabled - PHY Provides Delayed Clock)

FIGURE 6-6: RGMII RECEIVE TIMING (RXC INTERNAL DELAY ENABLED)

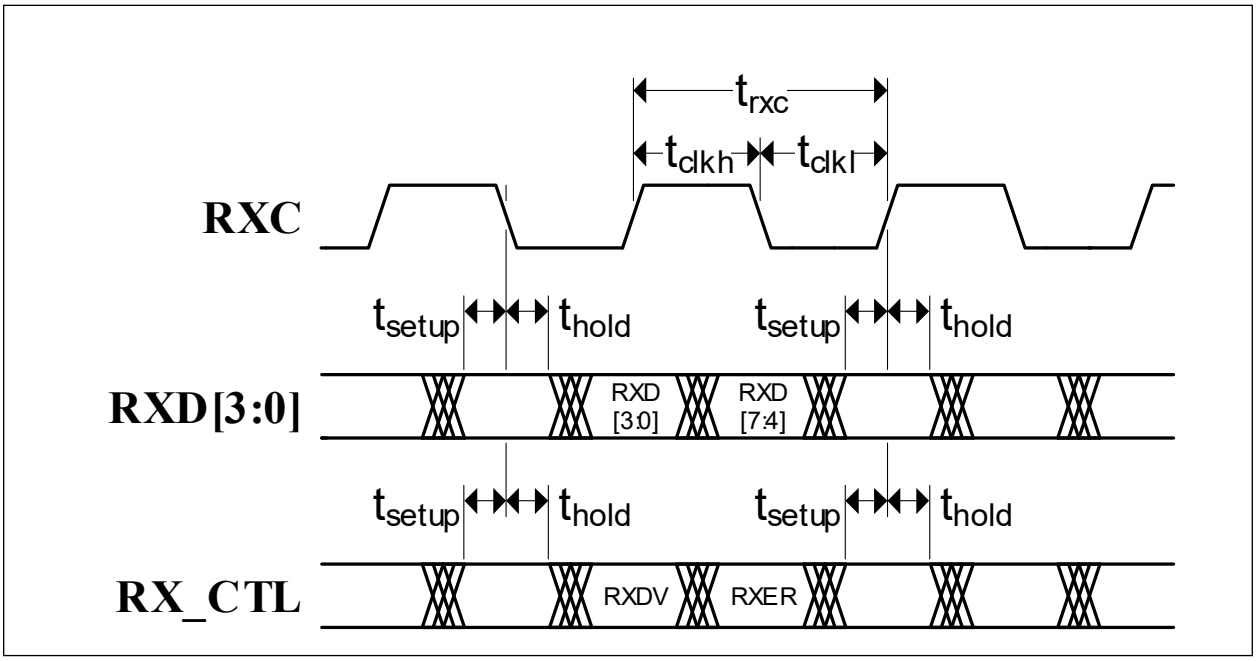


TABLE 6-11: RGMII RXC INTERNAL DELAY ENABLED (RGMII ID MODE / TC6 DoS MODE) TIMING VALUES

Symbol	Description	Min	Typ	Max	Units
t_{rxc}	**RXC** period	Note 6-21	Note 6-22	Note 6-23	ns
t_{clkh}	**RXC** high time	Note 6-24	50	Note 6-25	%
t_{clkl}	**RXC** low time	Note 6-24	50	Note 6-25	%
t_{setup}	**RXD[3:0]**, **RX_CTL** setup to edge of **RXC** (at outputs)	1.4 Note 6-26	2.0		ns
t_{hold}	**RXD[3:0]**, **RX_CTL** hold from edge of **RXC** (at outputs)	1.4 Note 6-26	2.0		ns

Note 6-21 7.2ns for 1000Mbps operation and 36ns for 100Mbps operation. Minimum limits are non-sustainable long term.

Note 6-22 8ns for 1000Mbps operation and 40ns for 100Mbps operation.

Note 6-23 8.8ns for 1000Mbps operation and 44ns for 100Mbps operation. Maximum limits are non-sustainable long term.

Note 6-24 45% for 1000Mbps operation and 40% for 100Mbps.

Note 6-25 55% for 1000Mbps operation and 60% for 100Mbps.

Note 6-26 These values provide 0.2 ns margin beyond the RGMII and TC6 specification.

6.6.6 SMI TIMING

This section specifies the SMI timing of the device.

FIGURE 6-7: SMI TIMING

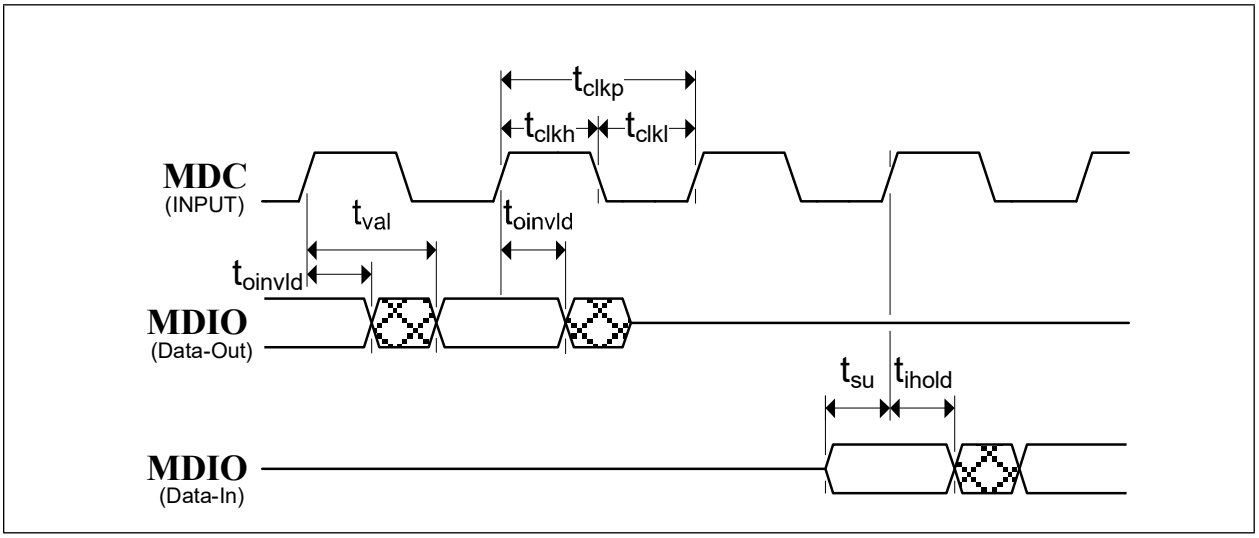


TABLE 6-12: SMI TIMING

Symbol	Description	Min	Typ	Max	Units
t_{clkp}	**MDC** period	40			ns
t_{clkh}	**MDC** high time	8 (80%)			ns
t_{clkl}	**MDC** low time	8(80%)			ns
t_{val}	**MDIO** (read from PHY) output valid from rising edge of **MDC**			20	ns
t_{oinvld}	**MDIO** (read from PHY) output invalid from rising edge of **MDC**	0			ns
t_{su}	**MDIO** (write to PHY) setup time to rising edge of **MDC**	8			ns
t_{ihold}	**MDIO** (write to PHY) input hold time after rising edge of **MDC**	8			ns

6.7 Clock Circuit

The device can accept either a 25 MHz crystal (preferred) or a 25 MHz single-ended clock oscillator (+/- 100 ppm) input reference. If the single-ended clock oscillator method is implemented, **XTAL2** should be left unconnected and **XTAL1** should be driven with a nominal 0-3.3 V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (**XTAL1**/**XTAL2**). See Table 6-13 for the recommended crystal specifications.

TABLE 6-13: CRYSTAL SPECIFICATIONS

Parameter	Symbol	Min	Nom	Max	Units	Notes
Crystal Cut			AT, typ			
Crystal Oscillation Mode			Fundamental Mode			
Crystal Calibration Mode			Parallel Resonant Mode			
Frequency	F_{fund}	-	25.000	-	MHz	
Frequency Tolerance @ 25°C	F_{tol}	-	-	+/-50	PPM	Note 6-27
Frequency Stability Over Temp	F_{temp}	-	-	+/-50	PPM	Note 6-27
Frequency Deviation Over Time	F_{age}	-	+/-3 to 5	-	PPM	Note 6-28
Total Allowable PPM Budget		-	-	+/-50	PPM	Note 6-29
Shunt Capacitance	C_O	-	-	*6*	pF	
Load Capacitance	C_L	-	-	*12*	pF	Note 6-30
Drive Level	P_W	-	-	*100*	uW	
Equivalent Series Resistance	R_1	-	-	50	Ohm	
Operating Temperature Range		*-40*	-	*+125*	°C	
XTAL1 Pin Capacitance		-	*2* typ	-	pF	Note 6-31
XTAL2 Pin Capacitance		-	*2* typ	-	pF	Note 6-31

Note 6-27 The maximum allowable values for Frequency Tolerance and Frequency Stability are application dependent. Since any particular application must meet the IEEE +/-100 PPM Total PPM Budget, the combination of these two values must be approximately +/-95 PPM (allowing for aging).

Note 6-28 Frequency Deviation Over Time is also referred to as Aging.

Note 6-29 The total deviation for the Transmitter Clock Frequency is specified by IEEE 802.3 as +/- 100 PPM.

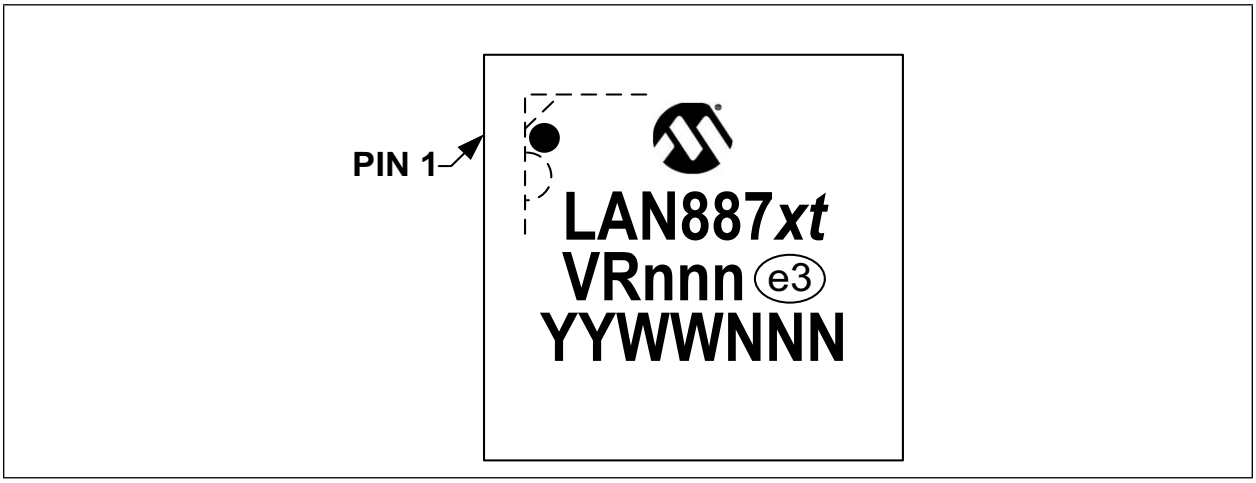
Note 6-30 Load Capacitance is calculated as the series combination of the total capacitive load of **XTAL1** and **XTAL2**.

Note 6-31 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The **XTAL1**/**XTAL2** pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

7.0 PACKAGE INFORMATION

Note: For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

7.1 Top Marking



Legend:

x	Part number (0, 1, or 2)
t	Temperature range designator *(i* = industrial, *v* = automotive)
V	Automotive indicator
R	Product revision
nnn	Internal code
e3	Pb-free JEDEC® designator for Matte Tin (Sn)
YY	Year code (last two digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information

7.2 48-VQFN

FIGURE 7-1: 48-VQFN PACKAGE (DRAWING)

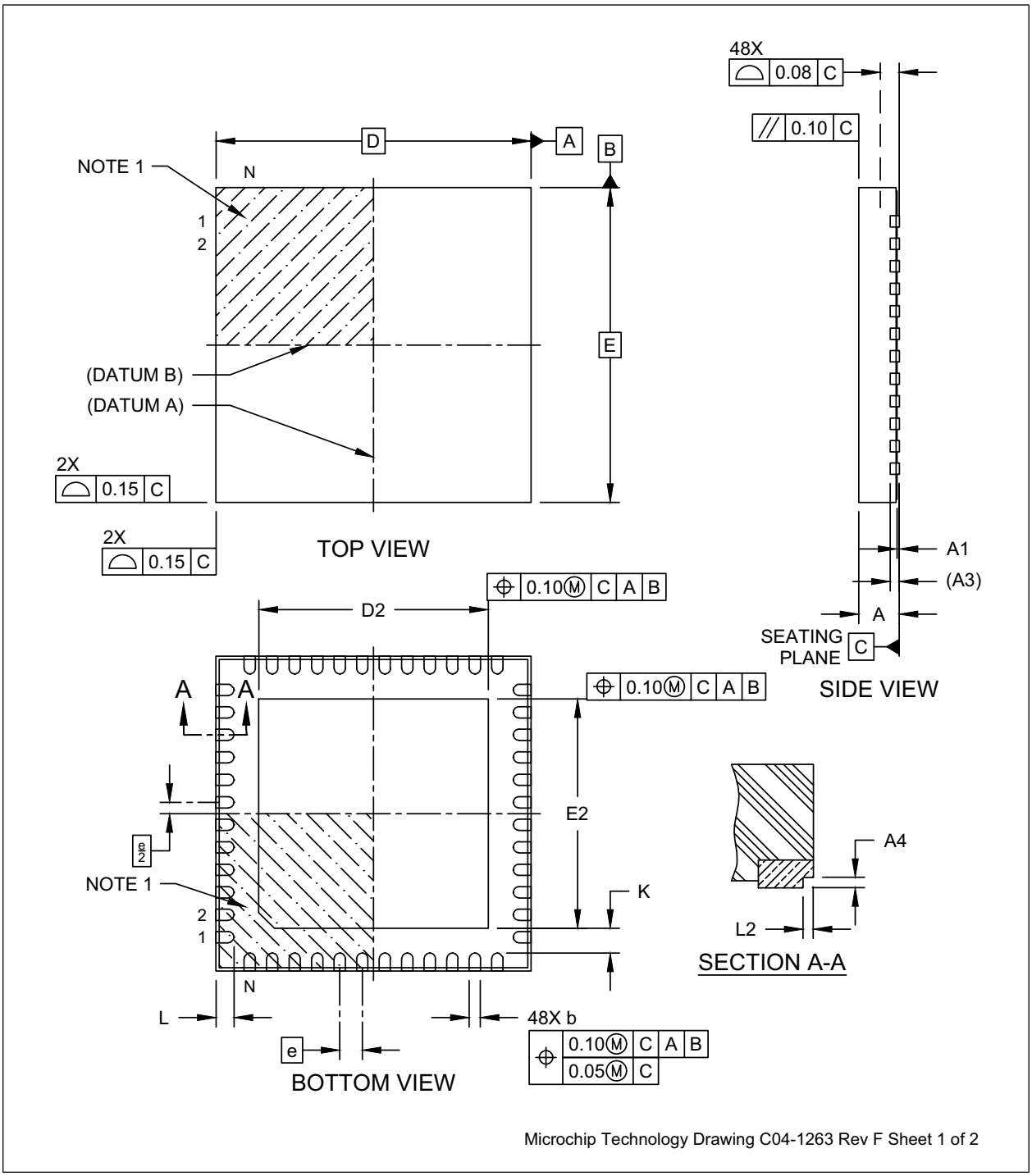
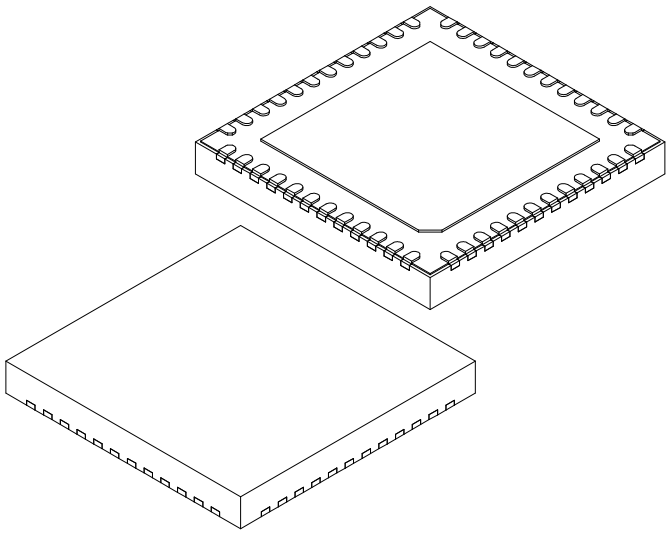


FIGURE 7-2: 48-VQFN PACKAGE (DIMENSIONS)



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		7.00 BSC	
Exposed Pad Length	D2	4.90	5.05	5.20
Overall Width	E		7.00 BSC	
Exposed Pad Width	E2	4.90	5.05	5.20
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Step Cut Height	A4	0.075	-	-
Step Cut Length	L2	-	-	0.075
Alternate Stepped Wettable Flank Dimensions				
Step Cut Height	A4	0.10	-	0.19
Step Cut Length	L2	-	-	0.085

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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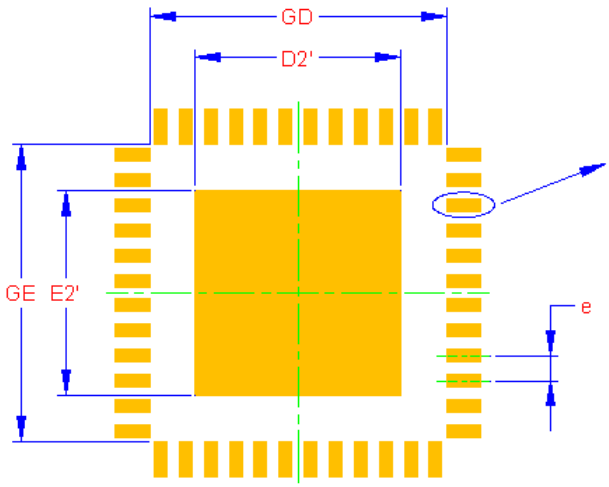
FIGURE 7-3: 48-VQFN PACKAGE (LAND-PATTERN)



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	6.00	-	6.10
D2'/E2'	-	4.10	-
X	-	0.28	0.28
Y	-	0.69	0.69
e		0.50	

PCB LAND PATTERN

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004828C (06-27-24)	Throughout Document	Removed support for 3.3 V for SGMII operation. Added notes advising +3.3 V is for RGMII operation only.
	Throughout Document	“VDD11” name changed to “VDDCORE”. “VDD11A” name changed to “VDDACORE”.
	Throughout Document	References to “1.1V” internal power supply have been renamed to “core”.
	Highlights, Top Marking, Product Identification System	Added information for LAN8870B product configuration.
	Key Benefits	Changed max 20uA to 15uA typical
	Table 1-2, "LAN887x Buffer Type Descriptions"	For buffer types VO-VDDIO, VO-VDD_RGMII, and VO-VBAT, the variable voltage output sink and source has been changed from “2/4/8/10 mA” to “5 mA” for each of their respective power domains.
	Section 3.0, Pin Descriptions	Removed RXER from pin 18, TXCLK from pin 30 and TXER from pin 38 from LAN8870/LAN8871 diagrams, Pin Assignments and Pin Descriptions.
	Section 3.2, Pin Descriptions	In description for pin REG_EN, “1.1V voltage domains” updated to “core voltage domains.”
	Section 4.1.1, Mean Square Error (MSE)	Third paragraph changed from: “In addition to the current MSE Value, the MSE Worst Case Value since the last read of the DCQ Mean Square Error Register is stored in the DCQ Mean Square Error Worst Case Register.” to: “In addition to the current MSE Value, the MSE Worst Case Value since the last read of the speed's MSE Register is stored in the speed's Worst Case MSE Register.”
	Section 4.1.1, Mean Square Error (MSE)	Fourth paragraph changed from: “The DCQ MSE / SQI Method A Enable bit in the DCQ Configuration 2 Register must be set to enable this measurement.” to: “For LAN8870 100BASE-T1, the MSE Measurement Enable bit in the TC1 100BASE-T1 MSE Register must be set to enable 100BASE-T1 MSE Measurement.”
	Section 4.1.1, Mean Square Error (MSE)	Added fifth paragraph: “For 1000BASE-T1, the 1000BASE-T1 DCQ/SQI Measurement Enable bit in the TC12 1000BASE-T1 DCQ/SQI Measurement Enable Register must be set to enable 1000BASE-T1 MSE measurement.”

TABLE A-1: REVISION HISTORY (CONTINUED)

Revision Level & Date	Section/Figure/Entry	Correction
	Section 4.1.2.1, SQI Method A	Second paragraph changed from: “The SQI value is stored in the DCQ SQI Method A Value field of the DCQ SQI Method A Register in 8 levels (between “000” = worst value and “111” = 7 = best value). In addition to the current SQI value, the lowest SQI value calculated since the last register read access is obtained via the DCQ SQI Method A Worst Case field of the DCQ SQI Method A Register.” to: “The SQI value is stored in the speed’s SQI Value field of the speed’s SQI Register in 8 levels (between “000” = worst value and “111” = 7 = best value). In addition to the current SQI value, the lowest SQI value calculated since the last register read access is obtained via the speed’s SQI Register Worst Case Value of the speed’s SQI Register.”
	Section 4.1.2.1, SQI Method A	Third paragraph changed from: “The DCQ MSE / SQI Method A Enable bit in the DCQ Configuration 2 Register must be set to enable this measurement.” to: “For LAN8870 100BASE-T1, both the 100BASE-T1 SQI Measurement Enable bit in the 100BASE-T1 SQI Configuration Register 1 and the 100BASE-T1 MSE and SQI enable bit in the 100BASE-T1 SQI Configuration 2 Register must be set. For 1000BASE-T1, the 1000BASE-T1 DCQ/SQI Measurement Enable bit must be set.”
	Section 4.1.2.2, SQI Method B	Third sentence of fourth paragraph changed from: “The result is available through SQI Method B Square Mean LSB Register and SQI Method B Square Mean MSB Register.” to: “For LAN8870 100BASE-T1, the result is in TC1 100BASE-T1 MSE register. For 1000BASE-T1, the result is in TC12 1000BASE-T1 MSE Register.”
	Section 4.1.3, Peak Mean Square Error (PMSE)	Fourth paragraph changed from: “Additionally, the Peak MSE Worst Case field of the DCQ Peak MSE Register contains the highest peak MSE value since the last time this register was read.” to: “Additionally, the speed's Worst Case Peak MSE Value in the speed's Peak MSE Register contains the highest peak MSE value since the last time this register was read.”

TABLE A-1: REVISION HISTORY (CONTINUED)

Revision Level & Date	Section/Figure/Entry	Correction
	Section 4.1.3, Peak Mean Square Error (PMSE)	Fifth paragraph changed from: “The DCQ pMSE Enable bit in DCQ Configuration 2 Register must be set to enable this measurement.” to: “For LAN8870 100BASE-T1, the Peak MSE Measurement Enable bit in 100BASE-T1 CONFIGURATION 2 REGISTER must be set to enable 100BASE-T1 pMSE Measurement. For 1000BASE-T1, the 1000BASE-T1 DCQ/SQI Measurement Enable bit in the TC12 1000BASE-T1 DCQ/SQI Measurement Enable Register must be set to enable 1000BASE-T1 pMSE measurement.”
	Section 4.2.2, WAKE_IN Wakeup	References to “is” corrected to “ms”.
	Section 4.2.3, INH Mode	Changed text: “The INH pin supports two operational modes which are defined by the inh_mode bit in Wakeup Common Control 0 Register.” to: “The INH pin supports two operational modes which are defined by the INH Mode bit in the TC10 Configuration Setup Register.”
	Section 4.2.4, WAKE_IN Polarity	Changed text: “The polarity of the WAKE_IN is determined via the wk_in_pol bit in the Wakeup Common Control 0 Register.” to: “The polarity of the WAKE_IN is determined via the WAKE_IN Polarity bit in the TC10 Configuration Setup Register.”
	Section 4.2.5, WAKE_OUT Mode	Changed text: “The polarity of the WAKE_OUT is determined via the wk_out_pol bit in the Wakeup Common Control 0 Register. The mode of operation is determined by the wk_out_mode field which allows for open-source, open-drain and push-pull operation.” to: “The polarity of the WAKE_OUT is determined via the WAKE_OUT Polarity bit in the TC10 Configuration Setup Register. The mode of operation is determined by the WAKE_OUT Mode bit in the TC10 Configuration Setup Register which allows for open-source, open-drain and push-pull operation.”
	Section 4.3, Over Temperature Detection	First sentence in this section removed: “A mechanism is provided within the device to detect when the die temperature exceeds 105°C.”
	Section 4.4, RGMII (LAN8870/LAN8871 Only)	Instances of RXCTRL and TXCTRL updated to RXCTL and TXCTL respectively

TABLE A-1: REVISION HISTORY (CONTINUED)

Revision Level & Date	Section/Figure/Entry	Correction
	Section 4.6, Serial Management Interface (SMI)	Second sentence in this section has been revised from: “This interface supports the standard PHY registers required by Clause 22 of the 802.3 standard, as well as “vendor-specific” registers allowed by the specification.” to: “This interface supports the standard PHY registers required by Clause 22 and Clause 45 of the 802.3 standard.”
	Section 4.7.5, Over-Temperature Reset	Changed text: “the OTMP_RESET” to: “an over-temperature reset”.
	Section 5.1, RGMII or SGMII Operation	Second paragraph in this section removed: “The LAN8870 cannot enter RGMII mode via strap option. This mode must be entered via register access. The user must configure the MAC_MODE_SEL field in the MIS_CFG_REG0 register and the SGMII_MUX_EN bit of the SGMII_CTL register. Additionally, the LAN8870 does not support the 125 MHz reference clock.”
	Figure 5-4	Changed “3.3 V” to “VOUT,” “VDDIO” to “VDDA,” “(R)MII/RGMII” to “SGMII/RGMII,” and “VDDRGMII” to “VDDRGMII/S_VPH.” Removed VDDARXTX and capacitor. Connected VDDRGMII/S_VPH to VOUT through ferrite bead/capacitor.
	Section 6.1, Absolute Maximum Ratings*	Removed VDD_RMII_VPH from first Supply Voltage entry. Added “Supply Voltage (S_VPH)....0 V to +3.0 V” entry.
	Section 6.1, Absolute Maximum Ratings*	HBM ESD information populated.
	Section 6.2, Operating Conditions**	Supply Voltage values for VDDCORE, VDDACORE, S_VP changed from “+1.045 V to +1.21 V” to “+1.067 V to +1.21 V”. Supply Voltage values for VDDIO, VDD_RGMII changed from “+1.62 V to +3.465 V” to “+1.71 V to +3.465 V”. S_VPH Supply Voltage broken out into its own row with operating range of +2.375 V to +2.625 V.
	Section 6.2, Operating Conditions**	3.3V lines high end limit changed from “+3.63V” to “+3.465V”.
	Section 6.3, Package Thermal Specifications	Junction-to-Ambient thermal numbers have been updated. The value for Θ_{JA} at 0 Meters/second was 31, but is now 19. The value for Θ_{JA} at 1 Meters/second was 27, but is now 24.

TABLE A-1: REVISION HISTORY (CONTINUED)

Revision Level & Date	Section/Figure/Entry	Correction
	Table 6-6, "DC Electrical Characteristics"	For buffer types VO-VDDIO, VO-VDD_RGMII, and VO-VBAT, both the minimum and maximum output levels have been changed from “0.4” to “0.6”. For buffer type VOD, the maximum output level has been changed from “0.4” to “0.6”. Notations that supported the previous values are obsolete and have been removed.
	Table 6-8, "RESET_N Configuration Strap Timing"	Table now updated to include values
	Table 6-9, "Power Sequence Timing"	Table now updated to include values
	Figure 6-4	Changed “3.3 V” to “VDDA”.
	Section 6.6.4, Power Sequence timing	Added the following notes: “Note: VDD_XMII refers to VDD_RGMII for RGMII and S_VPH for SGMII.” “Note: The S_VPH power supply can be run at 2.5V.”
	Section 6.6.5, RGMII Timing (LAN8870/LAN8871 Only)	The following RGMII Timing diagrams and tables have been removed for this release: “RGMII Transmit Timing (TXC Internal Delay Enabled - MAC Provides Delayed Clock)” and “RGMII Receive Timing (RXC Internal Delay Disabled - PHY Provides Delayed Clock)”.
	Table 6-12, "SMI Timing"	Table now updated to include values
	Section 7.1, Top Marking	Added “V” automotive indicator. Product revision variable indicator updated from “A” to “R”.
DS00004828B (2-22-24)	Section 3.1, Pin Assignments, Section 3.2, Pin Descriptions, Section 3.3, Configuration Straps	Added MAC_MODE_STRP to pin 30. Descriptions have been added to their appropriate areas. This addition only applies to LAN8870.
	Section 3.2, Pin Descriptions	Added pull up/pull down information for all configuration straps.
	Table 3-4, "Pin Descriptions"	Updated pin S_VP’s +1.1V SGMII core/transmitter power supply input to indicate “LAN8870/LAN8872 only,” previously stated “LAN8870/LAN8871 only”.
	Section 3.3.1, Speed Select (SPEED_SEL_STRP)	Updated to add “when device is in autonomous mode”.
	Section 4.1, Dynamic Channel Quality (DCQ) (TC1/TC12)	Updated OPEN Alliance compliance information.
	Section 4.1.3, Peak Mean Square Error (PMSE)	Updated TC-1 specification. Additionally, updated third paragraph of PMSE section from “100BASE-T1” to “100BASE-T1/1000BASE-T1”.
	Section 4.1.2.2, SQI Method B	Removed unnecessary register information.
	Section 4.3, Over Temperature Detection	Updated temperature from 135°C to 105°C
	Section 4.6, Serial Management Interface (SMI)	Removed the following sentence: “The minimum time between edges of the MDC is 160 ns”
	Section 4.10, IEEE 1588 (PTP)	Removed unnecessary PTP and SyncE information.

TABLE A-1: REVISION HISTORY (CONTINUED)

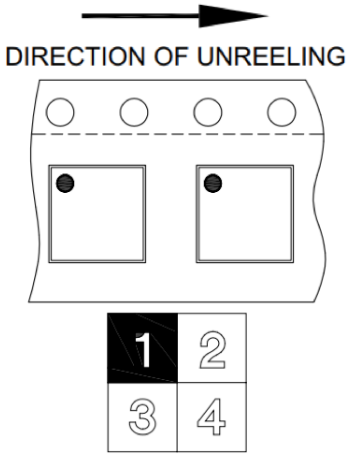
Revision Level & Date	Section/Figure/Entry	Correction
	Section 4.10.5, External 1588 Interface	Under 1588_LD_ADJ section, updated “LAN8871” to “LAN8870/1/2”.
	Figure 5-5, Figure 5-7, Figure 5-8	Figures updated to adjust power connectivity pin names, EXTRES values and resistor tolerance.
	Section 6.1, Absolute Maximum Ratings*	VDD11A and S_VP Absolute Maximum Ratings updated from “0 V to +4.0 V” to “0 V to +1.25 V”. VDD11 Absolute Maximum Ratings updated from “0 V to +1.4 V” to “0 V to +1.25 V”.
	Section 6.7, Clock Circuit	First sentence changed from “The device can accept either a 25 MHz crystal (preferred), a 25 MHz single-ended clock oscillator (+/- 100 ppm) input or an external, singled-ended 50MHz clock reference” to “The device can accept either a 25 MHz crystal (preferred) or a 25 MHz single-ended clock oscillator (+/- 100 ppm) input.”
DS00004828A (12-06-22)	All	Initial Release

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/	XXX	XXX
Device	Tape and Reel Option		Temperature Range		Package	Automotive Code

Device:	LAN8870	= 100/1000Mbps, RGMII/SGMII Interface
	LAN8871	= 1000Mbps, RGMII Interface
	LAN8872	= 1000Mbps, SGMII Interface
Extended Cable Reach Option:	Blank	= 1000BASE-T1 Type A (up to at least 15m)
	B	= 1000BASE-T1 Type B (up to at least 40m)
	Note:	Type-B option is only available with LAN8870
Tape and Reel Option:	Blank	= Standard packaging (tray)
	T	= Tape and Reel(Note 1)
Temperature Range:	V	= -40°C to +105°C (AEC-Q100 Grade 2 Automotive)
	I	= -40°C to +85°C (Industrial Grade)
Package:	PUA	= 48-pin VQFN
Automotive Code:	Vxx	= 3 character code with "V" prefix, specifying automotive product.



Examples:

a) LAN8870B-V/PUAVAO
Extended Cable Reach,
Tray, -40°C to +105°C, 48-pin VQFN

b) LAN8870BT-V/PUAVAO
Extended Cable Reach,
Tape & reel, -40°C to +105°C, 48-pin VQFN

c) LAN8870-V/PUAVAO
Tray, -40°C to +105°C, 48-pin VQFN

d) LAN8870T-I/PUA
Tape & reel, -40°C to +85°C, 48-pin VQFN

e) LAN8871-I/PUA
Tray, -40°C to +85°C, 48-pin VQFN

f) LAN8871T-V/PUAVAO
Tape & reel, -40°C to +105°C, 48-pin VQFN

g) LAN8872-I/PUA
Tray, -40°C to +85°C, 48-pin VQFN

h) LAN8872T-V/PUAVAO
Tape & reel, -40°C to +105°C, 48-pin VQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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