AN5483

LAN887x Register Definitions

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1.0 INTRODUCTION

The LAN887x Register Definitions application note provides a description of all customer-facing registers within the LAN887x device family and is meant for clarification of functionality during design and debugging. Register specific information pertaining to individual part numbers (LAN8870, LAN8871, LAN8872) will be defined within.

2.0 SECTIONS

This application note covers the following sections:

- Section 4.0, "Register Maps"
- Section 5.0, "Register Definitions"

3.0 REFERENCES

Consult the following documents for details on the specific parts referred to in this application note.

- *LAN887x Datasheet*
- *LAN8870 Hardware Design Checklist*
- *LAN8871 Hardware Design Checklist*
- *LAN8872 Hardware Design Checklist*

4.0 REGISTER MAPS

The LAN8870/LAN8871/LAN8872 supports the following standard registers. These registers are accessed through the SMI (MDIO/MDC) interface.

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TABLE 1: REGISTER SETS

Clause 45 ID	Register Set
0x00 (Clause 22)	Clause 22 Basic Registers
0x01	100BASE-T1/1000BASE-T1 PMA Common Registers
0x01	1000BASE-T1 PMA Registers
0x01	100BASE-T1/1000BASE-T1 Analog Front-End (AFE) Registers
0x03	100BASE-T1/1000BASE-T1 PCS Basic Registers
0x03	100BASE-T1/1000BASE-T1 PCS Registers
0x07	100BASE-T1/1000BASE-T1 Auto-Negotiation Registers
0x1E	100BASE-T1/1000BASE-T1 Wake/Sleep Parameter Registers
0x1E	Cable Diagnostics Registers
0x1E	1000BASE-T1 DSP Registers
0x1E	Miscellaneous Registers
0x1E	LED Registers
0x1E	TC10 Wake/Sleep Registers
0x1E	INT/GPIO/SGMII Registers
0x1E	Under-voltage/Over-voltage detection Registers
0x1E	Temperature Sensor Registers

TABLE 2: CLAUSE 22 BASIC REGISTERS

CL22 Address	Short Description	Register Name
0x00	Basic Control Register	CL22_BASIC_CONTROL
0x01	Basic Status Register	CL22_BASIC_STATUS
0x02	Device Identifier 1 Register	PHY_ID_1
0x03	Device Identifier 2 Register	PHY_ID_2
0x0D	MDD Access Control Register	CL45_INDIRECT_ACCESS_REG13
0x0E	MDD Access Data Register	CL45_INDIRECT_ACCESS_REG14

TABLE 3: 100BASE-T1/1000BASE-T1 PMA COMMON REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x01	0x00	PMA Control Register	PMA_CONTROL_1
0x01	0x01	PMA Status Register	PMA_STATUS_1
0x01	0x02	PMA Device ID 1	PMA DEVICE ID 1
0x01	0x03	PMA Device ID 2	PMA DEVICE ID 2

TABLE 3: 100BASE-T1/1000BASE-T1 PMA COMMON REGISTERS (CONTINUED)

CL45 Address	Register Address	Short Description	Register Name
0x01	0x04	PMA Speed Ability	PMA_SPEED_ABILITY
0x01	0x05	PMA Device Package Register 1	PMA_DEV_PKG1
0x01	0x06	PMA Device Package Register 2	PMA_DEV_PKG2
0x01	0x07	PMA Control Register 2	PMA_CONTROL_2
0x01	0x08	PMA Status Register 2	PMA_STATUS_2
0x01	0x09	PMA Transmit Disable	PMA_TX_DISABLE
0x01	0x0B	PMA Extended Ability Register 1	PMA_EXT_ABILITY
0x01	0x12	PMA Extended Ability Register 2	PMA_EXT_ABILITY_2
0x01	0x834	1000BASE-T1/100BASE-T1 PMA Control Register	PMA_CONTROL_T1
0x01	0x836	100BASE-T1 PMA Test Control Register - LAN8870 Only	PMA_TEST_CONTROL_T1

Note: 100BASE-T1 support is LAN8870 only.

TABLE 4: 1000BASE-T1 PMA REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x01	0x900	1000BASE-T1 Control Register	PMA_CONTROL
0x01	0x901	1000BASE-T1 PMA Status Register	PMA_STATUS
0x01	0x902	1000BASE-T1 Training Register	PMA_TRAINING_CONFIG
0x01	0x903	1000BASE-T1 Link Partner Training Status	LP_TRAINING_STAT
0x01	0x904	1000BASE-T1 Mode Control Register	TEST_MODE_CTRL

TABLE 5: 100BASE-T1/1000BASE-T1 ANALOG FRONT-END (AFE) REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x01	0x8089	AFE Port Test Control Register 1	AFE_PORT_TESTBUS_CTRL2
0x01	0x808B	AFE Port Test Control Register 2	AFE_PORT_TESTBUS_CTRL4
0x01	0x808D	AFE Port Test Control Register 3	AFE_PORT_TESTBUS_CTRL6
0x01	0x80B0	Transmit Amplitude Register	TX_AMPLT_1000T1_REG

Note: 100BASE-T1 support is LAN8870 only.

TABLE 6: 100BASE-T1/1000BASE-T1 PCS BASIC REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x03	0x00	PCS Control Register 1	PCS_CTRL1
0x03	0x01	PCS Status Register 1	PCS_STS1
0x03	0x02	PCS Device ID 1 Register	PCS_DEV_ID1
0x03	0x03	PCS Device ID 2 Register	PCS_DEV_ID2
0x03	0x05	PCS Device Package Register 1	PCS_DEV_PKG1
0x03	0x06	PCS Device Package Register 2	PCS_DEV_PKG2

Note: 100BASE-T1 support is LAN8870 only.

TABLE 7: 100BASE-T1/1000BASE-T1 PCS REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x03	0x900	1000BASE-T1 PCS Control Register	PCS_CONTROL
0x03	0x901	1000BASE-T1 PCS Status 1 Register	PCS_STATUS_1
0x03	0x902	1000BASE-T1 PCS Status 2 Register	PCS_STATUS_2
0x03	0x904	1000BASE-T1 OAM Transmit Register	OAM_TX
0x03	0x905	1000BASE-T1 OAM Message 0/1 Register	OAM_MSG_0_1
0x03	0x906	1000BASE-T1 OAM Message 2/3 Register	OAM_MSG_2_3
0x03	0x907	1000BASE-T1 OAM Message 4/5 Register	OAM_MSG_4_5
0x03	0x908	1000BASE-T1 OAM Message 6/7 Register	OAM_MSG_6_7
0x03	0x8033	OA TC12 FEC Counter Last Block Register	RSFEC_ERR_CNT_FLB
0x03	0x8036	OA TC12 Link Loss Com-Based Count Register	LFL_COMM_COUNT
0x03	0x8037	OA TC12 Link Loss Count Register	LFL_COUNT
0x03	0x803C	OAM PCS Status Register	OAM_PCS_DBG_STS
0x03	0x803D	OA TC12 Com Ready Register	LQ_COM_TC12
0x03	0x821F	OA TC12 Link-Up Fail Count Register	LINKUP_FAIL_COUNT
0x03	0x8220	Wake-Sleep Detection Length Register	SLEEP_WAKE_DET
0x03	0x8221	Wake-Sleep Send Length Register	SLEEP_WAKE_SEND
0x03	0x8232	Polarity Fix Enable Register	POLFLIP_FIX_TIMER
0x03	0x8240	WUP Send Length Register	WUP_LEN
0x03	0x8241	Sleep Abort/Reject Register	SLEEP_ABRT

TABLE 8: 100BASE-T1/1000BASE-T1 AUTO-NEGOTIATION REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x07	0x02	Auto-Negotiation Device ID 1 Register	ANEG_DEV_ID1
0x07	0x03	Auto-Negotiation Device ID 2 Register	ANEG_DEV_ID2
0x07	0x05	Auto-Negotiation Device Package Register 1	ANEG_DEV_PKG1
0x07	0x06	Auto-Negotiation Device Package Register 2	ANEG_DEV_PKG2
0x07	0x200	BASE-T1 Auto-Negotiation Control Register	ANEG_CNTRL_REG1
0x07	0x201	BASE-T1 Auto-Negotiation Status Register	ANEG_STAT_REG1
0x07	0x202	BASE-T1 Auto-Negotiation Advertisement Register 1	ANEG_ADV_REG1
0x07	0x203	BASE-T1 Auto-Negotiation Advertisement Register 2	ANEG_ADV_REG2
0x07	0x204	BASE-T1 Auto-Negotiation Advertisement Register 3	ANEG_ADV_REG3
0x07	0x205	BASE-T1 Link Partner Auto-Negotiation Advertisement Register 1	ANEG_LP_AB_REG1
0x07	0x206	BASE-T1 Link Partner Auto-Negotiation Advertisement Register 2	ANEG_LP_AB_REG2
0x07	0x207	BASE-T1 Link Partner Auto-Negotiation Advertisement Register 3	ANEG_LP_AB_REG3
0x07	0x208	BASE-T1 Auto-Negotiation Next Page Transmit Register 1	ANEG_NP_ADV_REG1
0x07	0x209	BASE-T1 Auto-Negotiation Next Page Transmit Register 2	ANEG_NP_ADV_REG2
0x07	0x20A	BASE-T1 Auto-Negotiation Next Page Transmit Register 3	ANEG_NP_ADV_REG3
0x07	0x20B	BASE-T1 Auto-Negotiation Link Partner Next Page Transmit Register 1	ANEG_LP_NPAB_REG1
0x07	0x20C	BASE-T1 Auto-Negotiation Link Partner Next Page Transmit Register 2	ANEG_LP_NPAB_REG2
0x07	0x20D	BASE-T1 Auto-Negotiation Link Partner Next Page Transmit Register 3	ANEG_LP_NPAB_REG3

Note: 100BASE-T1 support is LAN8870 only.

TABLE 9: 100BASE-T1/1000BASE-T1 WAKE/SLEEP PARAMETER REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x1E	0x10	TC10 WUR LPS Idle Control Register	REG_REG16
0x1E	0x1A	Hardware Configuration Initialization Register	REG_REG26
0x1E	0x125	TC10 Sleep Silent Enable Register	MISC37

Note: 100BASE-T1 support is LAN8870 only.

TABLE 10: CABLE DIAGNOSTICS REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x1E	0x404	Cable Diagnostics Slicer Coefficient Register	COEFF_PWR_DN_CONFIG_100
0x1E	0x40D	100BASE-T1 MSE/SQI Peak Coefficient Register (LAN8870 Only)	100_MSE_SQI_PEAK
0x1E	0x42E	100BASE-T1 SQI Configuration 1 Register (LAN8870 Only)	100_SQI_CONFIG1
0x1e	0x44A	100BASE-T1 SQI Configuration 2 Register (LAN8870 Only)	100_SQI_CONFIG2
0x1E	0x454	Cable Diagnostics Loop Register	KF_LOOP_SAT_CONFIG_100
0x1E	0x45A	Cable Diagnostics Start Register	START_CBL_DIAG_100
0x1E	0x45B	Cable Diagnostics TDR Configuration Register	CBL_DIAG_TDR_THRESH_100
0x1E	0x45C	Cable Diagnostics AGC Configuration Register	CBL_DIAG_AGC_THRESH_100
0x1E	0x45D	Cable Diagnostics Minimum Wait Configuration Register	CBL_DIAG_MIN_WAIT_CONFIG_100
0x1E	0x45E	Cable Diagnostics Maximum Wait Configuration Register	CBL_DIAG_MAX_WAIT_CONFIG_100
0x1E	0x45F	Cable Diagnostics Event Cycle Wait Time Configuration Register	CBL_DIAG_CYC_CONFIG_100
0x1E	0x460	Cable Diagnostic TX Pulse Configuration Register	CBL_DIAG_TX_PULSE_CONFIG_100
0x1E	0x462	Cable Diagnostic Minimum PGA Gain Register	CBL_DIAG_MIN_PGA_GAIN_100
0x1E	0x497	Cable Diagnostic AGC Gain Index Register	CBL_DIAG_AGC_GAIN_100
0x1E	0x499	Cable Diagnostic Positive Peak Value Register	CBL_DIAG_POS_PEAK_VALUE_100
0x1E	0x49A	Cable Diagnostic Negative Peak Value Register	CBL_DIAG_NEG_PEAK_VALUE_100
0x1E	0x49C	Cable Diagnostic Positive Peak Time Register	CBL_DIAG_POS_PEAK_TIME_100
0x1E	0x49D	Cable Diagnostic Negative Peak Time Register	CBL_DIAG_NEG_PEAK_TIME_100
0x1E	0x4C1	TC1 100BASE-T1 Worst Case MSE Register (LAN8870 Only)	TC1_MSE_WC_100
0x1E	0x4C2	TC1 100BASE-T1 MSE Register (LAN8870 Only)	TC1_MSE_100
0x1E	0x4C3	TC1 100BASE-T1 SQI Register (LAN8870 Only)	TC1_SQI_100
0x1E	0x4C4	TC1 100BASE-T1 Peak MSE Register (LAN8870 Only)	TC1 PMSE_100
0x1E	0x115	1000BASE-T1 Cable Diagnostics Enable (LAN8871/LAN8872 Only)	SQI_METHOD_SEL
0x1E	0xC00	1000BASE-T1 Cable Diagnostics Enable (LAN8871/LAN8872 Only)	CBL_DIAG_1000_EN

Note: 100BASE-T1 support is LAN8870 only.

TABLE 11: 1000BASE-T1 DSP REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x1E	0x80D	TC12 1000BASE-T1 DCQ/SQI Measurement Enable Register	TC12_SQI_MEAS_EN_1000

TABLE 11: 1000BASE-T1 DSP REGISTERS (CONTINUED)

CL45 Address	Register Address	Short Description	Register Name
0x1E	0x8B0	TC12 1000BASE-T1 MSE Register	TC12_MSE_1000
0x1E	0x8B1	TC12 1000BASE-T1 Worst Case MSE Register	TC12_MSE_WC_1000
0x1E	0x8B2	TC12 1000BASE-T1 SQI Register	TC12_SQI_1000
0x1E	0x8B3	TC12 1000BASE-T1 Peak MSE Register	TC12_PMSE_1000
0x1E	0x8D9	TC12 Link Training Time Register	TC12_LQ_LTT
0x1E	0x8DA	TC12 Local Receiver Time Register	TC12_LQ_LRT
0x1E	0x8DB	TC12 Remote Receiver Time Register	TC12_LQ_RRT
0x1E	0x9FA	TC12 Link Training Time 1us Counter Register	TC12_LQ_LTT_1US_CNTR
0x1E	0x9FB	TC12 Link Training Time 10us Counter Register	TC12_LQ_LTT_10US_CNTR
0x1E	0x9FC	TC12 Link Training Time 100us Counter Register	TC12_LQ_LTT_100US_CNTR

Note: 100BASE-T1 support is LAN8870 only.

TABLE 12: MISCELLANEOUS REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x1E	0xA00	MAC_MODE_SEL Configuration Register	MIS_CFG_REG0
0x1E	0xA01	TX RGMII Delay Register (LAN8870/LAN8871 Only)	MIS_DLL_CFG_REG0
0x1E	0xA02	RX RGMII Delay Register (LAN8870/LAN8871 Only	MIS_DLL_CFG_REG1
0x1E	0xA03	Loopback Register	MIS_CFG_REG2
0x1E	0xA09	RX Packet Error Counter Register	MIS_PKT_STAT_REG3
0x1E	0xA0D	Ethernet Package Generator (EPG) Enable Register	MIS_EPG_CFG1
0x1E	0xA11	Ethernet Package Generator (EPG) Payload Register	MIS_EPG_PYLD
0x1E	0xA12	Ethernet Package Generator (EPG) Packet Burst Count Register	MIS_EPG_BRST_CNT
0x1E	0xA13	Ethernet Package Generator (EPG) Burst Count Register	MIS_EPG_MBR_CNT
0x1E	0xA14	Ethernet Package Generator (EPG) Interpacket Gap Register	MIS_EPG_IPG_CFG
0x1E	0xA18	Ethernet Package Generator (EPG) Payload Length Register	MIS_EPG_PLEN

TABLE 13: LED REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x1E	0xC03	LED Configuration Register	COMMON_LED
0x1E	0xC04	LED1/LED2 Mode Selection Register	COMMON_LED2_LED1
0x1E	0xC05	LED3/LED4 Mode Selection Register	COMMON_LED4_LED3
0x1E	0xC10	TC10 Common Port Interrupt Mask Register	COMMON_PORT_INT_EN_CFG

TABLE 13: LED REGISTERS (CONTINUED)

CL45 Address	Register Address	Short Description	Register Name
0x1E	0xC11	TC10 Common Port Interrupt Status Register	COMMON_PORT_INT_STAT

TABLE 14: TC10 WAKE/SLEEP REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x1E	0xC20	TC10 Wake Out Register	TC10_REG_REG15
0x1E	0xC21	TC10 Wake/Sleep Request Send Register	TC10_REG_REG16
0x1E	0xC22	TC10 Interrupt Register	TC10_REG_REG24
0x1E	0xC24	TC10 Configuration Setup Register	TC10_MISC32
0x1E	0xC25	TC10 WAKE_OUT Configuration Register	TC10_MISC33
0x1E	0xC26	TC10 State Register	TC10_MISC34
0x1E	0xC27	TC10 WUP/WUR Configuration Register	TC10_MISC36
0x1E	0xC28	TC10 Sleep Silent Local Sleep Register	TC10_MISC37
0x1E	0xC29	TC10 Wake Up Port Control Register	TC10_MISC46
0x1E	0xC2A	TC10 Wake Up Common Register	TC10 WAKE_COMMON
0x1E	0xC2D	TC10 Sleep Abort/Sleep Reject Register	TC10_SLEEP_ABRT
0x1E	0xC2E	TC10 Sleep Fail Register	TC10_SLEEP_FAIL_STATUS
0x1E	0xC34	TC10 Sleep Request Timer Register	TC10_SLEEP_REQ_TMR_CFG
0x1E	0xC35	TC10 Sleep Acknowledge Register	TC10_SLEEP_ACK_TMR_CFG

TABLE 15: INT/GPIO/SGMII REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x1E	0xF000	Interrupt Status Register	INT_STS
0x1E	0xF001	Interrupt Mask Register	INT_MSK
0x1E	0xF002	Control 1 Register	CONTROL1
0x1E	0xF00A	GPIO Direction Register	GPIO_DIR
0x1E	0xF00B	GPIO Buffer Register	GPIO_BUF
0x1E	0xF00C	GPIO Data Register	GPIO_DATA
0x1E	0xF00D	GPIO Interrupt Status Register	GPIO_INT_STS
0x1E	0xF00E	GPIO Interrupt Mask Register	GPIO_INT_MSK
0x1E	0xF00F	GPIO Interrupt Polarity Register	GPIO_INT_POL
0x1E	0xF010	GPIO Interrupt PU/PD Override Register	GPIO_PU_PD_OVR
0x1E	0xF01A	SGMII/RGMII Mode Select Register (LAN8870 Only)	XGMII_CTL
0x1E	0xF01A	RGMII Control Register (LAN8871 Only)	RGMII_CTL
0x1E	0xF01A	SGMII Control Register (LAN8872 Only)	SGMII_CTL
0x1E	0xF01D	SGMII Hard Reset Register (LAN8870/ LAN8872 Only)	SGMII_HRST
0x1E	0xF01E	SGMII Soft Reset Register (LAN8870/LAN8872 Only)	SGMII_SRST

TABLE 15: INT/GPIO/SGMII REGISTERS (CONTINUED)

CL45 Address	Register Address	Short Description	Register Name
0x1E	0xF02C	SGMII Control Register (LAN8870/LAN8872 Only)	SGMII_CR_CTL
0x1E	0xF02D	SGMII Address Register (LAN8870/LAN8872 Only)	SGMII_CR_ADDR
0x1E	0xF02E	SGMII Data Register (LAN8870/LAN8872 Only)	SGMII_CR_DATA
0x1E	0xF02F	SGMII VREG Bypass Control Register (LAN8870/LAN8872 Only)	SGMII_VREG_BYP
0x1E	0xF034	SGMII PCS Configuration And Status Register (LAN8870/LAN8872 Only)	SGMII_PCS_CFG
0x1E	0xF03E	Chip Hard Reset Register	CHIP_HARD_RST
0x1E	0xF03F	Chip Soft Reset Register	CHIP_SOFT_RST
0x1E	0xF041	Configuration Strap Status Register	SKU_DBG_STS

TABLE 16: UNDER-VOLTAGE/OVER-VOLTAGE DETECTION REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x1E	0xF220	Under And Over Voltage Control Register	UVOV_CTL
0x1E	0xF221	Under And Over Voltage Control Interrupt Status Register	UVOV_INT_STS
0x1E	0xF222	Under And Over Voltage Interrupt Enable Register	UVOV_INT_EN
0x1E	0xF224	Under And Over Voltage Configuration 0 Register - VDDRGMII - LAN8870/LAN8871 Only	UVOV_CFG0_VDDRGMII
0x1E	0xF224	Under And Over Voltage Configuration 0 Register - S_VPH - LAN8872 Only	UVOV_CFG0_S_VPH
0x1E	0xF225	Under And Over Voltage Configuration 0 Register - VDDIO	UVOV_CFG0_VDDIO
0x1E	0xF226	Under And Over Voltage Configuration 0 Register - VDDA	UVOV_CFG0_VDDA
0x1E	0xF227	Under And Over Voltage Configuration 0 Register - VDD11	UVOV_CFG0_VDD11
0x1E	0xF228	Under And Over Voltage Configuration 1 Register - VDDRGMII - LAN8870/LAN8871 Only	UVOV_CFG1_VDDRGMII
0x1E	0xF228	Under And Over Voltage Configuration 1 Register - S_VPH - LAN8872 Only	UVOV_CFG1_S_VPH
0x1E	0xF229	Under And Over Voltage Configuration 1 Register - VDDIO	UVOV_CFG1_VDDIO
0x1E	0xF22A	Under And Over Voltage Configuration 1 Register - VDDA	UVOV_CFG1_VDDA
0x1E	0xF22B	Under And Over Voltage Configuration 1 Register - VDD11	UVOV_CFG1_VDD11
0x1E	0xF22C	Under And Over Voltage Configuration 2 Register - VDDRGMII - LAN8870/LAN8871 Only	UVOV_CFG2_VDDRGMII
0x1E	0xF22C	Under And Over Voltage Configuration 2 Register - S_VPH - LAN8872 Only	UVOV_CFG2_S_VPH

TABLE 16: UNDER-VOLTAGE/OVER-VOLTAGE DETECTION REGISTERS (CONTINUED)

CL45 Address	Register Address	Short Description	Register Name
0x1E	0xF22D	Under And Over Voltage Configuration 2 Register - VDDIO	UVOV_CFG2_VDDIO
0x1E	0xF22E	Under And Over Voltage Configuration 2 Register - VDDA	UVOV_CFG2_VDDA
0x1E	0xF22F	Under And Over Voltage Configuration 2 Register - VDD11	UVOV_CFG2_VDD11

TABLE 17: TEMPERATURE SENSOR REGISTERS

CL45 Address	Register Address	Short Description	Register Name
0x1E	0xF240	PVT Control 1 Register	PVT_CTL1
0x1E	0xF241	PVT Control 2 Register	PVT_CTL2
0x1E	0xF242	PVT Status Register	PVT_STS
0x1E	0xF244	PVT Interrupt Status Register	PVT_INT_STS
0x1E	0xF246	PVT Interrupt Mask Register	PVT_INT_MSK
0x1E	0xF248	PVT Data Register	PVT_DATA
0x1E	0xF24A	PVT Sample Time Register	PVT_SAMP_TIME
0x1E	0xF24C	PVT Thermal Comparator Control Register	PVT_THERM_COMP_CTL
0x1E	0xF24E	PVT Thermal Comparator Threshold0 Register	PVT_THERM_COMP_THR0
0x1E	0xF250	PVT Thermal Comparator Threshold1 Register	PVT_THERM_COMP_THR1
0x1E	0xF252	PVT Thermal Comparator Threshold2 Register	PVT_THERM_COMP_THR2
0x1E	0xF254	PVT Sample Clock Divider Register	PVT_SAMP_CLK_DIV
0x1E	0xF256	PVT Voltage Select Register	PVT_PSEL25
0x1E	0xF257	PVT Hard Reset Register	PVT_HARD_RST
0x1E	0xF258	PVT Soft Reset Register	PVT_SOFT_RST
0x1E	0xF259	PVT Clock Divider Register	PVT_CLK_DIVIDER

5.0 REGISTER DEFINITIONS

Register Definitions are divided into the following sections:

Unspecified fields in the registers must be written as zero and can be ignored on read. The access column shows the access for the field:

- R/W: Both read and write
- R/O: Read only
- W/O: Write only (read dummy)
- One-shot: Software writes '1', hardware resets when action is complete
- Sticky: Hardware sets bit, software clears it by writing '1'

5.1 Clause 22 Basic Registers

Standard registers provide direct read/write access to a 32-register address space, as defined in Clause 22 of the IEEE 802.3 Specification. Within this address space, the first 16 registers (Registers 0 to 15 (Fh)) are defined according to the IEEE specification, while the remaining 16 registers (Registers 16 (10h) to 31 (1Fh)) are defined specific to the PHY vendor.

5.1.1 BASIC CONTROL REGISTER

Register Name: CL22_BASIC_CONTROL

CL22 Register Address: 0x00 Size: 16 bits

Bits	Description	Type	Default
15	**Soft Reset** When set, this bit resets all the PHY and all its registers to their default state. This bit is self clearing. 1 = PHY software reset	R/W	0x0
14	**Loopback (PHY_LOOPBACK)** This bit enables/disables the loopback mode. When enabled, transmissions are not sent to network. Instead, they are looped back into the PHY. 0 = Loopback mode disabled (normal operation) 1 = Loopback mode enabled	R/W	0b
13	**Speed Select[0]** Together with Speed Select[1], sets speed per the following table: [Speed Select1][Speed Select0] 01 = 100Mbps 10 = 1000Mbps **Note:** Ignored if the Auto-Negotiation Enable bit of this register is 1	R/W	LAN8870: 1b LAN8871/ LAN8872: 0b
12	**Auto-Negotiation Enable** This bit enables/disables Auto-Negotiation. 0 = disable auto-negotiate process 1 = enable auto-negotiate process (overrides the Speed Select[0], Speed Select[1] and Duplex Mode bits of this register)	R/O	0b
11	**Power Down** This bit controls the power down mode of the PHY. 0 = Normal operation 1 = General power down mode	R/W	0b
10	**Isolate (PHY_ISO)** This bit controls the isolation of the PHY from the MII interface. 0 = Non-Isolated (Normal operation) 1 = Isolated	R/W	0b
9	**Restart Auto-Negotiation (PHY_RST_AN)** When set, this bit restarts the Auto-Negotiation process. This bit is self-clearing. 1 = Auto-Negotiation restarted	R/W	0b
8:7	**RESERVED**	R/O	10b
6	**Speed Select[1]** See description for Speed Select[0] for details.	R/W	LAN8870: 0b LAN8871/ LAN8872: 1b
5:0	**RESERVED**	R/O	000000b

5.1.2 BASIC STATUS REGISTER

CL22 Register Address: 0x01 Size: 16 bits

Register Name: CL22_BASIC_STATUS

Bits	Description	Type	Default
15:6	**RESERVED**	R/O	0000000000b
5	**Auto-Negotiation Complete** This bit indicates the status of the Auto-Negotiation process. 0 = Auto-Negotiation process not completed 1 = Auto-Negotiation process completed	R/O	0b
4	**RESERVED**	R/O	0b
3	**Auto-Negotiation Ability** This bit indicates the PHY's Auto-Negotiation ability. 0 = PHY is unable to perform Auto-Negotiation 1 = PHY is able to perform Auto-Negotiation	R/O	0b
2	**Link Status** This bit indicates the status of the link. 0 = Link is down 1 = Link is up	R/O	0b
1	**Jabber Detect** This bit indicates the status of the jabber condition. 0 = No jabber condition detected 1 = Jabber condition detected	R/O	0b
0	**RESERVED**	R/O	0b

5.1.3 DEVICE IDENTIFIER 1 REGISTER

CL22 Register Address: 0x02 Size: 16 bits

Register Name: PHY_ID_1

Bits	Description	Type	Default
15:0	**PHY ID Number** Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	R/W	0007h

5.1.4 DEVICE IDENTIFIER 2 REGISTER

CL22 Register Address: 0x03 Size: 16 bits

Register Name: PHY_ID_2

Bits	Description	Type	Default
15:10	**PHY ID Number** Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI), respectively.	R/W	110000b
9:4	**Model Number** Six-bit manufacturer's model number.	R/W	011111b
3:0	**Revision Number** Four-bit manufacturer's revision number: 1 = Rev. A0 2 = Rev. B0	R/W	0010b

5.1.5 MDD ACCESS CONTROL REGISTER

CL22 Register Address: 0x0D Size: 16 bits

Register Name: CL45_INDIRECT_ACCESS_REG13

Bits	Description	Type	Default
15:14	**MMD Function** This field is used to select the desired MMD function: 00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only	R/W	00b
13:5	**RESERVED**	RO	-
4:0	**MMD Device Address (DEVAD)** This field is used to select the desired MMD device address	R/W	00000b

5.1.6 MDD ACCESS DATA REGISTER

CL22 Register Address: 0x0E Size: 16 bits

Register Name: CL45_INDIRECT_ACCESS_REG14

Bits	Description	Type	Default
15:0	**MMD Register Address/Data** If the MMD Function field of the MMD Access Control Register is “00”, this field is used to indicate the MMD register address to read/write of the device specified in the MMD Device Address (DEVAD) field. Otherwise, this register is used to read/write data from/to the previously specified MMD address.	R/W	00b

5.2 100BASE-T1/1000BASE-T1 PMA Common Registers

5.2.1 PMA CONTROL REGISTER

CL45 Address: 0x01 Register Address: 0x00 Size: 16 bits

Register Name: PMA_CONTROL_1

Bits	Description	Type	Default
15	**Soft Reset** When set, this bit resets all the PHY and all its registers to their default state. This bit is self clearing. 1 = PHY software reset	R/W	0b
14:12	**RESERVED**	R/O	000b
11	**Low Power Mode** Always 0	R/W	0b
10:2	**RESERVED**	R/O	000000000b
1	**PMA Remote Loopback** Enables PMA Remote Loopback when set	R/W	0x0
0	**PMA Remote Loopback** Enables PMA Remote Loopback when set	R/W	0x0

5.2.2 PMA STATUS REGISTER

CL45 Address: 0x01 Register Address: 0x01 Size: 16 bits

Register Name: PMA_STATUS_1

Bit	Description	Type	Default
15:8	**RESERVED**	R/O	00h
7	**Fault** 1 = Fault condition detected 0 = Fault condition not detected	R/O	0b
6:3	**RESERVED**	R/O	0b
2	**Receive Link Status** 1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	R/O	0b
1	**Low Power Ability** 1 = PMA/PMD supports low-power mode 0 = PMA/PMD does not support low-power mode	R/O	1b
0	**RESERVED**	R/O	0b

5.2.3 PMA DEVICE ID 1

CL45 Address: 0x01 Register Address: 0x02 Size: 16 bits

Register Name: PMA DEVICE ID 1

Bits	Description	Type	Default
15:0	**PHY ID Number** Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively	R/W	0007h

5.2.4 PMA DEVICE ID 2

CL45 Address: 0x01 Register Address: 0x03 Size: 16 bits

Register Name: PMA DEVICE ID 2

Bits	Description	Type	Default
15:10	**PHY ID Number** Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI), respectively	R/W	110000b
9:4	**Model Number** Six-bit manufacturer's model number	R/W	011111b
3:0	**Revision Number** **Four-**bit manufacturer's revision number: 1 = Rev. A0 2 = Rev. B0	R/W	0010b

5.2.5 PMA SPEED ABILITY

CL45 Address: 0x01 Register Address: 0x04 Size: 16 bits

Register Name: PMA_SPEED_ABILITY

Bits	Description	Type	Default
15:6	**RESERVED**	R/O	0x000
5	**100M Capable (LAN8870 Only)** 1 – PHY is 100M Capable	R/O	0x1
4	**1000M Capable** 1 – PHY is 1000M Capable	R/O	0x1
3:0	**RESERVED**	R/O	0x0

5.2.6 PMA DEVICE PACKAGE REGISTER 1

CL45 Address: 0x01 Register Address: 0x05 Size: 16 bits

Register Name: PMA_DEV_PKG1

Bits	Description	Type	Default
15:4	**RESERVED**	R/O	000h
3	**PCS Present** 1 = PCS present in package 0 = PCS not present in package	R/O	1b

2	**RESERVED**	R/O	0b
1	**PMA/PMD Present** 1 = PMA/PMD present in package 0 = PMA/PMD not present in package	R/O	1b
0	**Clause 22 Registers Present** 1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	R/O	0b

5.2.7 PMA DEVICE PACKAGE REGISTER 2

CL45 Address: 0x01 Register Address: 0x06 Size: 16 bits

Register Name: PMA_DEV_PKG2

Bits	Description	Type	Default
15	**Vendor Spec 2** 1 = Vendor-specific device 2 present in package 0 = Vendor-specific device 2 not present in package	R/O	0b
14	**Vendor Spec 1** 1 = Vendor-specific device 1 present in package 0 = Vendor-specific device 1 not present in package	R/O	1b
13:0	**RESERVED**	R/O	000h

5.2.8 PMA CONTROL REGISTER 2

CL45 Address: **0x01** Register Address: 0x07 Size: 16 bits

This register is used to monitor the status of the PHY.

Register Name: PMA_CONTROL_2

Bits	Description	Type	Default
15:7	**RESERVED**	R/O	000000000b
6:0	**PMA/PMD Select Type** 0111101 – BASE-T1 PMA/PMD	R/W	0111101b

5.2.9 PMA STATUS REGISTER 2

CL45 Address: 0x01 Register Address: 0x08 Size: 16 bits

This register is used to monitor the status of the PHY.

Register Name: PMA_STATUS_2

Bits	Description	Type	Default
15:14	**Device Present** 10 – Device Present	R/O	10b
13	**TX Fault Ability** 1 - PMA/PMD has ability to detect a fault condition on the TX path	R/W	0b
12	**RX Fault Ability** 1 - PMA/PMD has ability to detect a fault condition on the RX path	R/W	1b
11	**TX Fault** 1 – Fault Condition Detected on TX Path	R/O	0b
10	**RX Fault** 1 – Fault Condition Detected on RX Path	R/W	1b
9	**Extended Abilities** 1 – Device has abilities listed in Register 1.11 (1h.0Bh)	R/O	1b
8	**PMD TX Disable Ability** Always 0 (PMA TX Always Enabled)	R/W	0b
7:1	**RESERVED**	R/W	0000000b
0	**PMA Local Loopback Ability** 1 – Device has PMA Loopback Ability	R/O	1b

5.2.10 PMA TRANSMIT DISABLE

CL45 Address: 0x01 Register Address: 0x09 Size: 16 bits

Register Name: PMA_TX_DISABLE

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	0000h
0	**Transmit Disable** Disables PMA Transmitter when set	R/W	0b

5.2.11 PMA EXTENDED ABILITY REGISTER 1

CL45 Address: 0x01 Register Address: 0x0B Size: 16 bits

Register Name: PMA_EXT_ABILITY

Bits	Description	Type	Default
15:12	**RESERVED**	R/O	0000b
11	**BASE-T1 Extended Abilities** 1 – Device has BASE-T1 Ability	R/O	1b
10:0	**RESERVED**	R/O	000h

5.2.12 PMA EXTENDED ABILITY REGISTER 2

CL45 Address: 0x01 Register Address: 0x12 Size: 16 bits

Register Name: PMA_EXT_ABILITY_2

Bits	Description	Type	Default
15:2	**RESERVED**	R/O	0000h
1	**1000BASE-T1 Extended Abilities** 1 – Device has 1000BASE-T1 Ability	R/O	1b
0	**100BASE-T1 Extended Abilities - LAN8870 Only** 1 – Device has 100BASE-T1 Ability **Note:** **RESERVED** in LAN8871/LAN8872	R/O	1b

5.2.13 1000BASE-T1/100BASE-T1 PMA CONTROL REGISTER

CL45 Address: 0x01 Register Address: 0x834 Size: 16 bits

Register Name: PMA_CONTROL_T1

Bits	Description	Type	Default
15	**RESERVED**	R/O	1b
14	**Master-Slave Configuration Value** 1 - Leader 0 – Follower **Note:** This setting is ignored if 07h.200h bit 12 is 1	R/W	1b
13:4	**RESERVED**	R/O	000h
3:0	**Type Selection** 0000 – 100BASE-T1 Speed - LAN8870 Only 0001 – 1000BASE-T1 Speed **Note:** This setting is ignored if 07h.200h bit 12 is 1	R/W	0001b

5.2.14 100BASE-T1 PMA TEST CONTROL REGISTER - LAN8870 ONLY

CL45 Address: 0x01 Register Address: 0x836 Size: 16 bits

Register Name: PMA_TEST_CONTROL_T1

Bits	Description	Type	Default
15:13	**100BASE-T1 Test Mode Control** 101 = Test mode 5 100 = Test mode 4 010 = Test mode 2 001 = Test mode 1 000 = Normal operation 111/110/011 = Reserved	R/W	0x000b
12:0	**RESERVED**	R/O	0x0000h

5.3 1000BASE-T1 PMA Registers

5.3.1 1000BASE-T1 CONTROL REGISTER

CL45 Address: 0x01 Register Address: 0x900 Size: 16 bits

Register Name: PMA_CONTROL

Bits	Description	Type	Default
15	**PMA/PMD Reset** 1 - PMA/PMD Reset 0 - Normal Operation	R/W	0b
14	**Transmit Disable** 1 - Transmit Disable 0 - Normal Operation	R/W	0b
13:12	**RESERVED**	R/O	00b
11	**Low-Power Mode** 1 – Low Power Mode 0 - Normal Operation	R/W	0b
10:0	**RESERVED**	R/O	000h

5.3.2 1000BASE-T1 PMA STATUS REGISTER

CL45 Address: 0x01 Register Address: 0x901 Size: 16 bits

Register Name: PMA_STATUS

Bits	Description	Type	Default
15:12	**RESERVED**	R/O	0000b
11	**1000BASE-T1 OAM Ability** 1 - PHY has 1000T1 OAM ability 0 - PHY does not have 1000T1 OAM ability	R/O	1b
10	**EEE Ability** 1 - PHY has EEE ability 0 - PHY does not have EEE ability	R/O	0b
9	**RX Fault Ability** 1 - PMA/PMD has ability to detect a fault condition on the receive path 0 - PMA/PMD does not have ability to detect a fault condition on the receive path	R/O	0b
8	**Low-Power Ability** 1 - PMA/PMD has the low power ability 0 - PMA/PMD does not have the low-power ability	R/O	0b

7:3	**RESERVED**	R/O	00000b
2	**RX Polarity** 1 - Receive polarity is reversed 0 - Receive polarity is not reversed	R/O	0b
1	**RESERVED**	R/O	000h
0	**RX Link Status**	R/O	

5.3.3 1000BASE-T1 TRAINING REGISTER

CL45 Address: 0x01 Register Address: 0x902 Size: 16 bits

Register Name: PMA_TRAINING_CONFIG

Bits	Description	Type	Default
15:11	**RESERVED**	R/O	0000b
10:4	**User Field** 7-bit user defined field to send to the link-partner	R/W	00h
3:2	**RESERVED**	R/O	00b
1	**1000BASE-T1 OAM Advertisement** 1 - 1000T1 OAM ability advertised to the link partner 0 - 1000T1 OAM ability not advertised to the link partner	R/W	1b
0	**EEE Advertisement** 1 - 1000T1 EEE ability advertised to the link partner 0 - 1000T1 EEE ability not advertised to the link partner	R/W	0b

5.3.4 1000BASE-T1 LINK PARTNER TRAINING STATUS

CL45 Address: 0x01 Register Address: 0x903 Size: 16 bits

Register Name: LP_TRAINING_STAT

Bits	Description	Type	Default
15:11	**RESERVED**	R/O	0000b
10:4	**Link Partner User Field** 7-bit user defined field from the link-partner	R/W	00h
3:2	**RESERVED**	R/O	00b
1	**Link Partner 1000BASE-T1 OAM Advertisement** 1 – Link Partner has 1000T1 OAM ability 0 - Link Partner does not have 1000T1 OAM ability	R/W	1b
0	**Link Partner EEE Advertisement** 1 - Link Partner has EEE ability 0 - Link Partner does not have EEE ability	R/W	0b

5.3.5 1000BASE-T1 MODE CONTROL REGISTER

CL45 Address: 0x01 Register Address: 0x904 Size: 16 bits

Register Name: TEST_MODE_CTRL

Bits	Description	Type	Default
15:13	**1000BASE-T1 Test Mode Control** 111 - Test Mode 7 110 - Test Mode 6 101 - Test Mode 5 100 - Test Mode 4 011 – Reserved 010 - Test Mode 2 001 - Test Mode 1 000 - Normal (Non-test) operation.	R/W	0x000b
12:0	**RESERVED**	R/O	0x0000h

5.4 100BASE-T1/1000BASE-T1 Analog Front-End (AFE) Registers

5.4.1 AFE PORT TEST CONTROL REGISTER 1

CL45 Address: 0x01 Register Address: 0x8089 Size: 16 bits

Register Name: AFE_PORT_TESTBUS_CTRL2

Bits	Description	Type	Default
15:8	**RESERVED**	R/O	00h
7	**600MHz and 750MHz Clock Enable** 1 – Enables internal 600MHz and 750MHz clocks	R/W	0b
6:0	**RESERVED**	R/O	00h

5.4.2 AFE PORT TEST CONTROL REGISTER 2

CL45 Address: 0x01 Register Address: 0x808B Size: 16 bits

Register Name: AFE_PORT_TESTBUS_CTRL4

Bits	Description	Type	Default
15:8	**RESERVED**	R/O	00h
7	**TX DAC Clock Select** 0 - Gasket Clock provides 600MHz/750MHz DAC Clock 1 – Port_clkgen provides 600MHz/750MHz DAC Clock	R/W	1b
6:0	**RESERVED**		0111000b

5.4.3 AFE PORT TEST CONTROL REGISTER 3

CL45 Address: 0x01 Register Address: 0x808D Size: 16 bits

Register Name: AFE_PORT_TESTBUS_CTRL6

Bits	Description	Type	Default
15:7	**RESERVED**	R/O	000h
6	**ADC Clock Mode** 1 - ADC sampling f=66MHz 0 - ADC sampling f=600MHz	R/W	0b
5:0	**RESERVED**		000000b

5.4.4 TRANSMIT AMPLITUDE REGISTER

CL45 Address: 0x01 Register Address: 0x80B0 Size: 16 bits

Register Name: TX_AMPLT_1000T1_REG

Bits	Description	Type	Default
15:6	**RESERVED**	R/O	000h
5:0	**TX Amplitude Control** This field controls the Fine Amplitude Control for 100BASE-T1/1000BASE-T1 operation **Note:** 100BASE-T1 support is LAN8870 only.	R/W	111111b

5.5 100BASE-T1/1000BASE-T1 PCS Basic Registers

5.5.1 PCS CONTROL REGISTER 1

CL45 Address: 0x03 Register Address: 0x00 Size: 16 bits

Register Name: PCS_CTRL1

Bits	Description	Type	Default
15	**PCS Reset** 1 - PCS Reset 0 - Normal operation (self-clearing)	R/W	0b
14	**PCS Loopback** When set, PCS Loopback is enabled	R/W	0b
13:12	**RESERVED**	R/O	0b
11	**PCS_LOW_PWR** When set, device enters low-power mode	R/W	0b
10:0	**RESERVED**	R/O	000h

5.5.2 PCS STATUS REGISTER 1

CL45 Address: 0x03 Register Address: 0x01 Size: 16 bits

Register Name: PCS_STS1

Bits	Description	Type	Default
15:3	**RESERVED**	R/O	0000h
2	**PCS Link Status** PCS receive link status (latch-low) 1 = PCS receive link up 0 = PCS receive link down **Note:** Reading this field will set it	R/O	0b
1	**PCS Low-Power Ability** 1 = PCS supports low-power mode 0 = PCS does not support low-power mode	R/O	1b
0	**RESERVED**	R/O	0b

5.5.3 PCS DEVICE ID 1 REGISTER

CL45 Address: 0x03 Register Address: 0x02 Size: 16 bits

Register Name: PCS_DEV_ID1

Bits	Description	Type	Default
15:0	**PHY ID Number** Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively	R/W	0007h

5.5.4 PCS DEVICE ID 2 REGISTER

CL45 Address: 0x03 Register Address: 0x03 Size: 16 bits

Register Name: PCS_DEV_ID2

Bits	Description	Type	Default
15:10	**PHY ID Number** Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI), respectively	R/W	110000b
9:4	**Model Number** Six-bit manufacturer's model number	R/W	011111b
3:0	**Revision Number** Four-bit manufacturer's revision number: 1 = Rev. A0 2 = Rev. B0	R/W	0010b

5.5.5 PCS DEVICE PACKAGE REGISTER 1

CL45 Address: 0x03 Register Address: 0x05 Size: 16 bits

Register Name: PCS_DEV_PKG1

Bits	Description	Type	Default
15:8	**RESERVED**	R/O	00h
7	**Auto-Negotiation Present** 1 = Auto-Negotiation present in package 0 = Auto-Negotiation not present in package	R/O	1b
6:4	**RESERVED**	R/O	000b
3	**PCS Present** 1 = PCS present in package 0 = PCS not present in package	R/O	1b
2	**RESERVED**	R/O	0b
1	**PMA/PMD Present** 1 = PMA/PMD present in package 0 = PMA/PMD not present in package	R/O	1b
0	**Clause 22 Registers Present** 1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	R/O	0b

5.5.6 PCS DEVICE PACKAGE REGISTER 2

CL45 Address: 0x03 Register Address: 0x06 Size: 16 bits

Register Name: PCS_DEV_PKG2

Bits	Description	Type	Default
15	**Vendor Spec 2** 1 - Vendor-specific device 2 present in package 0 - Vendor-specific device 2 not present in package	R/O	0b
14	**Vendor Spec 1** 1 - Vendor-specific device 1 present in package 0 - Vendor-specific device 1 not present in package	R/O	1b
13	**Clause 22 Extension Present** 1 - Clause 22 extension is present in the package 0 - Clause 22 extension is not present in the package	R/O	1b
12:0	**RESERVED**	R/O	000h

5.6 100BASE-T1/1000BASE-T1 PCS Registers

5.6.1 1000BASE-T1 PCS CONTROL REGISTER

CL45 Address: 0x03 Register Address: 0x900 Size: 16 bits

Register Name: PCS_CONTROL

Bits	Description	Type	Default
15	**PCS Reset** 1 - PCS Reset 0 - Normal operation (self-clearing)	R/W	0b
14	**PCS Loopback** When set, PCS Loopback is enabled	R/W	0b
13:0	**RESERVED**	R/O	0000h

5.6.2 1000BASE-T1 PCS STATUS 1 REGISTER

CL45 Address: 0x03 Register Address: 0x901 Size: 16 bits

Register Name: PCS_STATUS_1

Bits	Description	Type	Default
15:12	**RESERVED**	R/O	0000b
11	**TX_LPI_RCVD** 1 = Tx PCS has received LPI 0 = LPI not received	R/O	0b
10	**RX_LPI_RCVD** 1 = Rx PCS has received LPI 0 = LPI not received	R/O	0b
9	**TX_LPI_RCVNG** 1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	R/O	0b
8	**RX_LPI_RCVNG** 1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	R/O	0b
7	**Fault** 1 = Fault condition detected 0 = No fault condition detected	R/O	0b
6:3	**RESERVED**	R/O	0000b
2	**PCS Link Status** PCS receive link status (latch-low) 1 = PCS receive link up 0 = PCS receive link down	R/O	0b
1:0	**RESERVED**	R/O	00b

5.6.3 1000BASE-T1 PCS STATUS 2 REGISTER

CL45 Address: 0x03 Register Address: 0x902 Size: 16 bits

Register Name: PCS_STATUS_2

Bits	Description	Type	Default
15:11	**RESERVED**	R/O	00000b
10	**Receive Link Status** 1 = PCS receive link up 0 = PCS receive link down	R/O	0b

9	**PCS High BER** 1 = PCS reporting a high BER 0 = PCS not reporting a high BER	R/O	0b
8	**PCS Block Lock** 1 = PCS locked to received blocks 0 = PCS not locked to received blocks	R/O	0b
7	**Latched High BER** 1 = PCS has reported a high BER 0 = PCS has not reported a high BER	R/O	0b
6	**Latched Block Lock** 1 = PCS has block lock 0 = PCS does not have block lock	R/O	0b
5:0	**BER Counter**	R/O	000000b

5.6.4 1000BASE-T1 OAM TRANSMIT REGISTER

CL45 Address: 0x03 Register Address: 0x904 Size: 16 bits

Register Name: OAM_TX

Bits	Description	Type	Default
15	**1000BASE-T1 OAM Message Valid** This bit is used to indicate message data in registers 3h.904h through 3h.908h are valid and ready to be loaded. This bit shall self-clear when registers are loaded by the state machine. 1 = Message data in registers are valid 0 = Message data in registers are not valid	R/O	0b
14	**Toggle Value** Toggle value to be transmitted with message.	R/O	0b
13	**1000BASE-T1 OAM Message Received** This bit shall self-clear on read. 1 = 1000BASE-T1 OAM message received by link partner 0 = 1000BASE-T1 OAM message not received by link partner	R/O	0b
12	**Receive Message Toggle Value** Toggle value of message that was received by link partner as indicated in bit 13	R/O	0b
11:8	**Message Number** User-defined message number to send	R/O	0000b
7:4	**RESERVED**	R/O	0b
3	**Ping Received** Received PingTx value from latest good 1000BASE-T1 OAM frame received	R/O	0b
2	**Ping Transmitted** Ping value to send to link partner	R/O	0b

1:0	**Local SNR** 00 = PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal 11 = PHY SNR is good.	R/O	00b

5.6.5 1000BASE-T1 OAM MESSAGE 0/1 REGISTER

CL45 Address: 0x03 Register Address: 0x905 Size: 16 bits

Register Name: OAM_MSG_0_1

Bits	Description	Type	Default
15:8	**1000BASE-T1 OAM Message 1** 1000BASE-T1 OAM Message Octet 1	R/W	00000000b
7:0	**1000BASE-T1 OAM Message 0** 1000BASE-T1 OAM Message Octet 0	R/W	00000000b

5.6.6 1000BASE-T1 OAM MESSAGE 2/3 REGISTER

CL45 Address: 0x03 Register Address: 0x906 Size: 16 bits

Register Name: OAM_MSG_2_3

Bits	Description	Type	Default
15:8	**1000BASE-T1 OAM Message 3** 1000BASE-T1 OAM Message Octet 3	R/W	00000000b
7:0	**1000BASE-T1 OAM Message 2** 1000BASE-T1 OAM Message Octet 2	R/W	00000000b

5.6.7 1000BASE-T1 OAM MESSAGE 4/5 REGISTER

CL45 Address: 0x03 Register Address: 0x907 Size: 16 bits

Register Name: OAM_MSG_4_5

Bits	Description	Type	Default
15:8	**1000BASE-T1 OAM Message 5** 1000BASE-T1 OAM Message Octet 5	R/W	00000000b
7:0	**1000BASE-T1 OAM Message 4** 1000BASE-T1 OAM Message Octet 4	R/W	00000000b

5.6.8 1000BASE-T1 OAM MESSAGE 6/7 REGISTER

CL45 Address: 0x03 Register Address: 0x908 Size: 16 bits

Register Name: OAM_MSG_6_7

Bits	Description	Type	Default
15:8	**1000BASE-T1 OAM Message 7** 1000BASE-T1 OAM Message Octet 7	R/W	00000000b
7:0	**1000BASE-T1 OAM Message 6** 1000BASE-T1 OAM Message Octet 6	R/W	00000000b

5.6.9 OA TC12 FEC COUNTER LAST BLOCK REGISTER

CL45 Address: 0x03 Register Address: 0x8033 Size: 16 bits

Register Name: RSFEC_ERR_CNT_FLB

Bits	Description	Type	Default
15:10	**RESERVED**	R/W	000000b
9:0	**FEC Counter Last Block** FEC counter as defined in OA TC12. Reading this register will clear this counter.	R/W	000h

5.6.10 OA TC12 LINK LOSS COM-BASED COUNT REGISTER

CL45 Address: 0x03 Register Address: 0x8036 Size: 16 bits

Register Name: LFL_COMM_COUNT

Bits	Description	Type	Default
15:10	**Link Loss Count (COM-Based)** Number of link-losses that occurred since last power cycle (0 to 63). This counter caps at 63 and does not rollover until a reset event.	R/W	000000b
9:0	**Link Failure Count (COM-Based)** Number of Link Failures causing NOT a link loss since last power cycle (0 to 1023).	R/W	000h

5.6.11 OA TC12 LINK LOSS COUNT REGISTER

CL45 Address: 0x03 Register Address: 0x8037 Size: 16 bits

Register Name: LFL_COUNT

Bits	Description	Type	Default
15:10	**Link Loss Count** Number of link-losses that occurred since last power cycle (0 to 63). This counter caps at 63 and does not rollover until a reset event.	R/W	000000b
9:0	**Link Failure Count** Number of Link Failures causing NOT a link loss since last power cycle (0 to 1023).	R/W	000h

5.6.12 OAM PCS STATUS REGISTER

CL45 Address: 0x03 Register Address: 0x803C Size: 16 bits

Register Name: OAM_PCS_DBG_STS

Bits	Description	Type	Default
15:9	**RESERVED**	R/W	0000000b
8	**OAM RX CRC Not OK** CRC Not-OK for the received OAM frame. Latch-High and Clear on Read.	R/W	0b
7	**Wake-Up Request (WUR) Received - OAM** WUR received in the OAM message. Latch-High and Clear on Read. **Note:** Only seen when PHY is not in Sleep State (WUP sent if PHY is in Sleep State)		0b

6	**Low-Power Sleep Request (LPS) Received - OAM** LPS received in the OAM message. Latch-High and Clear on Read		0b
5:3	**OAM RX Current state**		000b
2:0	**OAM TX Current state**		000b

5.6.13 OA TC12 COM READY REGISTER

CL45 Address: 0x03 Register Address: 0x803D Size: 16 bits

Register Name: LQ_COM_TC12

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	0000h
0	**COM Ready** Communication ready (COM). Local Receiver = 1 AND Remote Receiver = 1	R/O	0b

5.6.14 OA TC12 LINK-UP FAIL COUNT REGISTER

CL45 Address: 0x03 Register Address: 0x821F Size: 16 bits

Register Name: LINKUP_FAIL_COUNT

Bits	Description	Type	Default
15:8	**RESERVED**.	R/W	00000000b
7:0	**Link-Up Failure Count** The number of link up failed attempts. The counter stops at max value 255.	R/W	00000000b

5.6.15 WAKE-SLEEP DETECTION LENGTH REGISTER

CL45 Address: 0x03 Register Address: 0x8220 Size: 16 bits

Register Name: SLEEP_WAKE_DET

Bits	Description	Type	Default
15:8	**Wake-Up Request (WUR) Detection Length** WUR code detect length. This field has units of 30 ns.	R/W	00111111b
7:0	**Low-Power Sleep Request (LPS) Detection Length** LPS code detect length. This field has units of 30 ns.	R/W	00111111b

5.6.16 WAKE-SLEEP SEND LENGTH REGISTER

CL45 Address: 0x03 Register Address: 0x8221 Size: 16 bits

Register Name: SLEEP_WAKE_SEND

Bits	Description	Type	Default
15:8	**Wake-Up Request (WUR) Send Length** WUR code send length. This field has units of 30 ns.	R/W	00111111b
7:0	**Low-Power Sleep Request (LPS) Send Length** LPS code send length. This field has units of 30 ns.	R/W	00111111b

5.6.17 POLARITY FIX ENABLE REGISTER

CL45 Address: 0x03 Register Address: 0x8232 Size: 16 bits

Register Name: POLFLIP_FIX_TIMER

Bits	Description	Type	Default
15:8	**RESERVED**	R/O	00000000b
7	**Polarity Flip Fix Enable** Enable the feature of polarity flip check even on link training restart condition after link-down.	R/W	1b
6:0	**Polarity Flip Fix Enable Timer** Timer to enable the polarity flip check in slave mode upon reset removal or link training restart. This timer is in millisecond and valid only when bit 7 is set to 1.	R/W	0000110b

5.6.18 WUP SEND LENGTH REGISTER

CL45 Address: 0x03 Register Address: 0x8240 Size: 16 bits

Register Name: WUP_LEN

Bits	Description	Type	Default
15:8	**RESERVED**	R/O	00000000b
7:0	**Wake-Up Pulse (WUP) Send Length** WUP code send length. **Note:** This field has units of 8 ns.	R/W	01111111b

5.6.19 SLEEP ABORT/REJECT REGISTER

CL45 Address: 0x03 Register Address: 0x8241 Size: 16 bits

Register Name: SLEEP_ABRT

Bits	Description	Type	Default
15:6	**RESERVED**	R/O	000h
5	**Sleep Abort** When set, a pending sleep request, received via link partner LPS signaling, is aborted	R/W	0b
4	**Sleep Reject** When set, all sleep requests shall be rejected	R/W	0b
3:0	**RESERVED**	R/W	0000b

5.7 100BASE-T1/1000BASE-T1 Auto-Negotiation Registers

5.7.1 AUTO-NEGOTIATION DEVICE ID 1 REGISTER

CL45 Address: 0x07 Register Address: 0x02 Size: 16 bits

Register Name: ANEG_DEV_ID1

Bits	Description	Type	Default
15:0	**PHY ID Number** Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively	R/W	0007h

5.7.2 AUTO-NEGOTIATION DEVICE ID 2 REGISTER

CL45 Address: 0x07 Register Address: 0x03 Size: 16 bits

Register Name: ANEG_DEV_ID2

Bits	Description	Type	Default
15:10	**PHY ID Number** Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI), respectively	R/W	00110000b
9:4	**Model Number** Six-bit manufacturer's model number	R/W	011111b
3:0	**Revision Number** Four-bit manufacturer's revision number: 1 = Rev. A0 2 = Rev. B0	R/W	0010b

5.7.3 AUTO-NEGOTIATION DEVICE PACKAGE REGISTER 1

CL45 Address: 0x07 Registevr Address: 0x05 Size: 16 bits

Register Name: ANEG_DEV_PKG1

Bits	Description	Type	Default
15:8	**RESERVED**	R/O	00h
7	**Auto-Negotiation Present** 1 = Auto-Negotiation present in package 0 = Auto-Negotiation not present in package	R/O	1b
6:4	**RESERVED**	R/O	000b
3	**PCS Present** 1 = PCS present in package 0 = PCS not present in package	R/O	1b
2	**RESERVED**	R/O	0b
1	**PMA/PMD Present** 1 = PMA/PMD present in package 0 = PMA/PMD not present in package	R/O	1b
0	**Clause 22 Registers Present** 1 = Clause 22 registers present in package 0 = Clause 22 registers not present in package	R/O	0b

5.7.4 AUTO-NEGOTIATION DEVICE PACKAGE REGISTER 2

CL45 Address: 0x07 Register Address: 0x06 Size: 16 bits

Register Name: ANEG_DEV_PKG2

Bits	Description	Type	Default
15	**Vendor Spec 2** 1 - Vendor-specific device 2 present in package 0 - Vendor-specific device 2 not present in package	R/O	0b
14	**Vendor Spec 1** 1 - Vendor-specific device 1 present in package 0 - Vendor-specific device 1 not present in package	R/O	1b
13	**Clause 22 Extension Present** 1 - Clause 22 extension is present in the package 0 - Clause 22 extension is not present in the package	R/O	1b
12:0	**RESERVED**	R/O	000h

5.7.5 BASE-T1 AUTO-NEGOTIATION CONTROL REGISTER

CL45 Address: 0x07 Register Address: 0x200 Size: 16 bits

Register Name: ANEG_CNTRL_REG1

Bits	Description	Type	Default
15	**Auto-Negotiation Reset** 1 – Auto-Negotiation Reset 0 – Auto-Negotiation Normal Operation	R/O	0b
14:13	**RESERVED**	R/O	00b
12	**Auto-Negotiation Enable** 1 – Enables Auto-Negotiation 0 – Disables Auto-Negotiation	R/O	0b
11:10	**RESERVED**	R/O	00b
9	**Auto-Negotiation Restart** 1 – Restart Auto-Negotiation	R/O	0b
8:0	**RESERVED**	R/O	000000000b

5.7.6 BASE-T1 AUTO-NEGOTIATION STATUS REGISTER

CL45 Address: 0x07 Register Address: 0x201 Size: 16 bits

Register Name: ANEG_STAT_REG1

Bits	Description	Type	Default
15:7	**RESERVED**	R/O	000000000b
6	**Page Received** 1 – A page has been received 0 – A page has not been received	R/O	0b
5	**Auto-Negotiation Complete** 1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	R/O	0b
4	**Remote Fault** 1 = remote fault condition detected 0 = no remote fault condition detected	R/O	0b
3	**Auto-Negotiation Ability** 1 – Device able to perform auto-negotiation 0 – Device is unable to perform auto-negotiation	R/O	0b
2	**Link Status** 1 – Link is up 0 – Link is down	R/O	0b
1:0	**RESERVED**	R/O	000000000b

5.7.7 BASE-T1 AUTO-NEGOTIATION ADVERTISEMENT REGISTER 1

CL45 Address: 0x07 Register Address: 0x202 Size: 16 bits

Register Name: ANEG_ADV_REG1

Bits	Description	Type	Default
15	**Auto-Negotiation Next Page** This bit indicates the link partner PHY page capability. 0 = Link partner PHY does not advertise next page capability 1 = Link partner PHY advertises next page capability	R/O	005h
14	**Auto-Negotiation Acknowledge** This bit indicates whether the link code word has been received from the partner. 0 = Link code word not yet received from partner 1 = Link code word received from partner	R/O	0b

13	**Auto-Negotiation Remote Fault** This bit indicates whether a remote fault has been detected. 0 = No remote fault 1 = Remote fault detected	R/O	0b
12	**Auto-Negotiation Force Master/Slave** 0 – Preferred Mode 1 – Forced Mode Used with Leader/Follower preference in Reg 7.0x203.4	R/O	0b
11:10	**Auto-Negotiation Pause Ability** Bit 11 – Asymmetric Pause Capability Bit 10 – Symmetric Pause Capability	R/O	00b
9:5	**Auto-Negotiation Link Partner Echoed Nonce Field** Device's Transmitted Nonce Field	R/O	00000b
4:0	**Auto-Negotiation Link Partner Selector Field** 00001 - IEEE 802.3	R/O	00001b

5.7.8 BASE-T1 AUTO-NEGOTIATION ADVERTISEMENT REGISTER 2

CL45 Address: 0x07 Register Address: 0x203 Size: 16 bits

Register Name: ANEG_ADV_REG2

Bits	Description	Type	Default
15:5	**Auto-Negotiation Technology Ability [10:0]** Bit 7: Ability [2] => 1000BASE-T1 Ability Bit 5: Ability [0] => 100BASE-T1 Ability **Note:** 100BASE-T1 support is LAN8870 only. **Note:** In LAN8871/LAN8872, bit 5 is RESERVED	R/O	005h
4	**ANEG Transmitted Nonce Field - T[4]** 0 – Link Partner Device prefers to be Follower 1 - Link Partner Device prefers to be Leader	R/O	0b
3:0	**ANEG Transmitted Nonce Field – T[3:0]** Random value captured by arbiter	R/O	0000b

5.7.9 BASE-T1 AUTO-NEGOTIATION ADVERTISEMENT REGISTER 3

CL45 Address: 0x07 Register Address: 0x204 Size: 16 bits

Register Name: ANEG_ADV_REG3

Bits	Description	Type	Default
15:0	**Auto-Negotiation Technology Ability [26:11]**	R/O	0000h

5.7.10 BASE-T1 LINK PARTNER AUTO-NEGOTIATION ADVERTISEMENT REGISTER 1

CL45 Address: 0x07 Register Address: 0x205 Size: 16 bits

Register Name: ANEG_LP_AB_REG1

Bits	Description	Type	Default
15	**Auto-Negotiation Link Partner Next Page** This bit indicates the link partner PHY page capability. 0 = Link partner PHY does not advertise next page capability 1 = Link partner PHY advertises next page capability	R/O	005h
14	**Auto-Negotiation Link Partner Acknowledge** This bit indicates whether the link code word has been received from the partner. 0 = Link code word not yet received from partner 1 = Link code word received from partner	R/O	0b
13	**Auto-Negotiation Link Partner Remote Fault** This bit indicates whether a remote fault has been detected. 0 = No remote fault 1 = Remote fault detected	R/O	0b
12	**Auto-Negotiation Link Partner Force Master/Slave** 0 – Preferred Mode 1 – Forced Mode Used with Leader/Follower preference in Reg 7.0x206.4	R/O	0b
11:10	**Auto-Negotiation Link Partner Pause Ability** Bit 11 – Link Partner Asymmetric Pause Capability Bit 10 – Link Partner Symmetric Pause Capability	R/O	00b
9:5	**Auto-Negotiation Link Partner Echoed Nonce Field** Link Partner's Transmitted Nonce Field	R/O	00000b
4:0	**Auto-Negotiation Link Partner Selector Field** 00000 if No Link Partner 00001 if there is a Link Partner (00001 - IEEE 802.3)	R/O	00000b or 00001b

Note: A read of Register 7.0x205 latches the contents of Registers 7.0x206 and 7.0x207

5.7.11 BASE-T1 LINK PARTNER AUTO-NEGOTIATION ADVERTISEMENT REGISTER 2

CL45 Address: 0x07 Register Address: 0x206 Size: 16 bits

Register Name: ANEG_LP_AB_REG2

Bits	Description	Type	Default
15:5	**Auto-Negotiation Link Partner Ability [10:0]** Bit 7: Ability [2] => 1000BASE-T1 Ability Bit 5: Ability [0] => 100BASE-T1 Ability **Note:** 100BASE-T1 support is LAN8870 only. **Note:** In LAN8871/LAN8872, bit 5 is RESERVED	R/O	000h
4	**ANEG Link Partner Transmitted Nonce Field - T[4]** 0 - Link Partner Device prefers to be Follower 1 - Link Partner Device prefers to be Leader	R/O	0b
3:0	**ANEG Link Partner Transmitted Nonce Field – T[3:0]** Random value captured by arbiter	R/O	0000b

5.7.12 BASE-T1 LINK PARTNER AUTO-NEGOTIATION ADVERTISEMENT REGISTER 3

CL45 Address: 0x07 Register Address: 0x207 Size: 16 bits

Register Name: ANEG_LP_AB_REG3

Bits	Description	Type	Default
15:0	**Auto-Negotiation Link Partner Ability [26:11]**	R/O	0000h

5.7.13 BASE-T1 AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER 1

CL45 Address: 0x07 Register Address: 0x208 Size: 16 bits

Register Name: ANEG_NP_ADV_REG1

Bits	Description	Type	Default
15	**Auto-Negotiation Next Page Ability** 0 = Device has no next page ability 1 = Device has next page ability	R/O	0b
14	**Auto-Negotiation Next Page Acknowledge**	R/O	0b
13	**Auto-Negotiation Next Page Message Page**	R/O	1b
12	**Auto-Negotiation Next Page Acknowledge 2**	R/O	0b
11	**Auto-Negotiation Next Page Toggle Field**	R/O	0b
10:0	**Auto-Negotiation Next Page Unformatted field 1** Auto-Negotiation Message/Unformatted Field	R/O	001h

5.7.14 BASE-T1 AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER 2

CL45 Address: 0x07 Register Address: 0x209 Size: 16 bits

Register Name: ANEG_NP_ADV_REG2

Bits	Description	Type	Default
15:0	**Auto-Negotiation Next Page Unformatted field 2** Auto-Negotiation Next Page Unformatted field [26:11] or [15:0] depending on whether the message page bit is clear or set.	R/O	0x0000

5.7.15 BASE-T1 AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER 3

CL45 Address: 0x07 Register Address: 0x20A Size: 16 bits

Register Name: ANEG_NP_ADV_REG3

Bits	Description	Type	Default
15:0	**Auto-Negotiation Next Page Unformatted field 3** Auto-Negotiation Next Page Unformatted field [42:27] or [31:0] (value latched when reg 523 is read)	R/O	0x0000

5.7.16 BASE-T1 AUTO-NEGOTIATION LINK PARTNER NEXT PAGE TRANSMIT REGISTER 1

CL45 Address: 0x07 Register Address: 0x20B Size: 16 bits

Register Name: ANEG_LP_NPAB_REG1

Bits	Description	Type	Default
15	**Auto-Negotiation Link Partner Next Page Ability** 0 = Link Partner has no next page ability 1 = Link Partner has next page ability	R/O	0x0
14	**Auto-Negotiation Link Partner Next Page Acknowledge**	R/O	0x0
13	**Auto-Negotiation Link Partner Next Page Message Page**	R/O	0x0
12	**Auto-Negotiation Link Partner Next Page Acknowledge 2**	R/O	0x0
11	**Auto-Negotiation Link Partner Next Page Toggle Field**	R/O	0x0
10:0	**Auto-Negotiation Link Partner Next Page Unformatted field 1** Auto-Negotiation Link Partner Message/Unformatted Field	R/O	0x000

5.7.17 BASE-T1 AUTO-NEGOTIATION LINK PARTNER NEXT PAGE TRANSMIT REGISTER 2

CL45 Address: 0x07 Register Address: 0x20C Size: 16 bits

Register Name: ANEG_LP_NPAB_REG2

Bits	Description	Type	Default
15:0	**Auto-Negotiation Link Partner Next Page Unformatted field 2** Auto-Negotiation Link Partner Next Page Unformatted field [26:11] or [15:0] depending on whether the message page bit is clear or set.	R/O	0x0000

5.7.18 BASE-T1 AUTO-NEGOTIATION LINK PARTNER NEXT PAGE TRANSMIT REGISTER 3

CL45 Address: 0x07 Register Address: 0x20D Size: 16 bits

Register Name: ANEG_LP_NPAB_REG3

Bits	Description	Type	Default
15:0	**Auto-Negotiation Link Partner Next Page Unformatted field 3** Auto-Negotiation Link Partner Next Page Unformatted field [42:27] or [31:0] (value latched when reg 523 is read)	R/O	0x0000

5.8 100BASE-T1/1000BASE-T1 Wake/Sleep Parameter Registers

5.8.1 TC10 WUR LPS IDLE CONTROL REGISTER

CL45 Address: 0x1E Register Address: 0x10 Size: 16 bits

Register Name: REG_REG16

Bits	Description	Type	Default
15:6	**RESERVED**	R/O	000h
5	**TC10 WUR LPS Idle Control** 0 – Operation without TC10 1 – Operation with TC10 to detect WUR and LPS	R/W	0b
4:0	**RESERVED**	R/O	10100b

5.8.2 HARDWARE CONFIGURATION INITIALIZATION REGISTER

CL45 Address: 0x1E Register Address: 0x1A Size: 16 bits

Register Name: REG_REG26

Bits	Description	Type	Default
15:9	**RESERVED**	R/O	000001b
8	**HW Initialization** 1 – Enable Hardware Configuration Sequence	R/W	0b
7:4	**RESERVED**	R/O	0000b
3	**Force Energy Detect** 1 – Forces Energy Detect On	R/W	0b
2:0	**RESERVED**	R/O	000b

5.8.3 TC10 SLEEP SILENT ENABLE REGISTER

CL45 Address: 0x1E Register Address: 0x125 Size: 16 bits

Register Name: MISC37

Bits	Description	Type	Default
15:6	**RESERVED**	R/O	000h
5	**TC10 Sleep Silent Enable** 1 – Enables Sleep_Silent state for TC10 Operation	R/W	0b
4:0	**RESERVED**	R/O	00000b

5.9 Cable Diagnostics Registers

5.9.1 CABLE DIAGNOSTICS SLICER COEFFICIENT REGISTER

CL45 Address: 0x1E Register Address: 0x404 Size: 16 bits

Register Name: COEFF_PWR_DN_CONFIG_100

Bits	Description	Type	Default
15:0	**Cable Diagnostics Slicer Coefficient Register** Bits[15:1] determine the Cable Diagnostics routine slicer threshold and should not be changed. Bit 0 needs to be 0 to start the Cable Diagnostics routine	R/O	16D7h

5.9.2 100BASE-T1 MSE/SQI PEAK COEFFICIENT REGISTER (LAN8870 ONLY)

CL45 Address: 0x1E Register Address: 0x40D Size: 16 bits

Register Name: 100_MSE_SQI_PEAK

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	000000b
9:8	**100BASE-T1 SQI Update** Both bits must be set to update SQI Measurement.	R/W	0b
7:1	**RESERVED**	R/W	000000b
0	**100BASE-T1 Peak Coefficient Enable**	R/W	0b

5.9.3 100BASE-T1 SQI CONFIGURATION 1 REGISTER (LAN8870 ONLY)

CL45 Address: 0x1E Register Address: 0x42E Size: 16 bits

Register Name: 100_SQI_CONFIG1

Bits	Description	Type	Default
15:8	**RESERVED**	R/O	10010101b
7	**DCQ/SQI Reset** DCQ and SQI are in Reset when set. Clear bit for DCQ/SQI Measurements	R/W	1b
6	**100BASE-T1 SQI Mode Select** 0: Absolute 1: Square Mode For MSE/SQI, this bit must be set.	R/W	0b
0	**100BASE-T1 SQI Measurement Enable** This bit enables MSE/SQI Measurements	R/W	0b
4:0	**RESERVED**	R/O	01101b

5.9.4 100BASE-T1 SQI CONFIGURATION 2 REGISTER (LAN8870 ONLY)

CL45 Address: 0x1E Register Address: 0x44A Size: 16 bits

Register Name: 100_SQI_CONFIG2

Bits	Description	Type	Default
15:12	**RESERVED**	R/O	0000h
1	**100BASE-T1 Peak MSE Enable** This bit must be set for peak MSE (pMSE) to be enabled	R/W	0b
0	**100BASE-T1 MSE and SQI Enable** This bit must be set for MSE and SQI to be enabled	R/W	0b

5.9.5 CABLE DIAGNOSTICS LOOP REGISTER

CL45 Address: 0x1E Register Address: 0x454 Size: 16 bits

Register Name: KF_LOOP_SAT_CONFIG_100

Bits	Description	Type	Default
15:12	**RESERVED**	R/O	0000b
11	**KP Loop Saturation Reset** Resets Loop used for Cable Diagnostics Calculation	R/W	0b
10	**KP Loop Saturation Enable** Enables Loop used for Cable Diagnostics Calculation	R/W	1b

9:0	**KP Loop Saturation Value** Loop Value used for Cable Diagnostics Calculation	R/W	078h

5.9.6 CABLE DIAGNOSTICS START REGISTER

CL45 Address: 0x1E Register Address: 0x45A Size: 16 bits

Register Name: START_CBL_DIAG_100

Bits	Description	Type	Default
15:2	**RESERVED**	R/O	0000h
1	**Cable Diagnostics Done** 1 – Cable Diagnostics Test is complete	R/O	0b
0	**Start Cable Diagnostics** 1 – Start Cable Diagnostic Test	R/W	0b

5.9.7 CABLE DIAGNOSTICS TDR CONFIGURATION REGISTER

CL45 Address: 0x1E Register Address: 0x45B Size: 16 bits

Register Name: CBL_DIAG_TDR_THRESH_100

Bits	Description	Type	Default
15:6	**RESERVED**	R/O	000h
5:0	**Cable Diagnostics TDR Threshold** Sets Cable Diagnostics TDR Threshold	R/W	000001b

5.9.8 CABLE DIAGNOSTICS AGC CONFIGURATION REGISTER

CL45 Address: 0x1E Register Address: 0x45C Size: 16 bits

Register Name: CBL_DIAG_AGC_THRESH_100

Bits	Description	Type	Default
15:6	**RESERVED**	R/O	000h
5:0	**Cable Diagnostics AGC Threshold** Sets Cable Diagnostics AGC Threshold	R/W	101000b

5.9.9 CABLE DIAGNOSTICS MINIMUM WAIT CONFIGURATION REGISTER

CL45 Address: 0x1E Register Address: 0x45D Size: 16 bits

Register Name: CBL_DIAG_MIN_WAIT_CONFIG_100

Bits	Description	Type	Default
15:7	**RESERVED**	R/O	000h
6:0	**Cable Diagnostics Minimum Wait** Cable Diagnostics Minimum Wait time in cycles	R/W	0000011b

5.9.10 CABLE DIAGNOSTICS MAXIMUM WAIT CONFIGURATION REGISTER

CL45 Address: 0x1E Register Address: 0x45E Size: 16 bits

Register Name: CBL_DIAG_MAX_WAIT_CONFIG_100

Bits	Description	Type	Default
15:7	**RESERVED**	R/O	000h
6:0	**Cable Diagnostics Maximum Wait** Cable Diagnostics Maximum Wait time in cycles	R/W	0011110b

5.9.11 CABLE DIAGNOSTICS EVENT CYCLE WAIT TIME CONFIGURATION REGISTER

CL45 Address: 0x1E Register Address: 0x45F Size: 16 bits

Register Name: CBL_DIAG_CYC_CONFIG_100

Bits	Description	Type	Default
15:0	**Cable Diagnostic Event Cycle Wait Time Configuration** Number of symbol period wait time to resend TDR pulse	R/W	0028h

5.9.12 CABLE DIAGNOSTIC TX PULSE CONFIGURATION REGISTER

CL45 Address: 0x1E Register Address: 0x460 Size: 16 bits

Register Name: CBL_DIAG_TX_PULSE_CONFIG_100

Bits	Description	Type	Default

15:0	**Cable Diagnostic TX Pulse Configuration** Configures Cable Diagnostic TX Pulses. Leave at default (0x44D5)	R/W	44D5h

5.9.13 CABLE DIAGNOSTIC MINIMUM PGA GAIN REGISTER

CL45 Address: 0x1E Register Address: 0x462 Size: 16 bits

Register Name: CBL_DIAG_MIN_PGA_GAIN_100

Bits	Description	Type	Default
15:5	**RESERVED**	R/O	000h
4:0	**Cable Diagnostic Minimum PGA Gain** Configures Cable Diagnostic Minimum PGA Gain	R/W	01110b

5.9.14 CABLE DIAGNOSTIC AGC GAIN INDEX REGISTER

CL45 Address: 0x1E Register Address: 0x497 Size: 16 bits

Register Name: CBL_DIAG_AGC_GAIN_100

Bits	Description	Type	Default
15:5	**RESERVED**	R/O	000h
4:0	**Cable Diagnostic AGC Gain** Cable Diagnostic AGC Gain Index	R/W	00000b

5.9.15 CABLE DIAGNOSTIC POSITIVE PEAK VALUE REGISTER

CL45 Address: 0x1E Register Address: 0x499 Size: 16 bits

Register Name: CBL_DIAG_POS_PEAK_VALUE_100

Bits	Description	Type	Default
15:5	**RESERVED**	R/O	000h
4:0	**Cable Diagnostic Positive Peak Value** Cable Diagnostic Positive Peak Value (unsigned)	R/W	00000b

5.9.16 CABLE DIAGNOSTIC NEGATIVE PEAK VALUE REGISTER

CL45 Address: 0x1E Register Address: 0x49A Size: 16 bits

Register Name: CBL_DIAG_NEG_PEAK_VALUE_100

Bits	Description	Type	Default
15:5	**RESERVED**	R/O	000h
4:0	**Cable Diagnostic Negative Peak Value** Cable Diagnostic Negative Peak Value (unsigned)	R/W	00000b

5.9.17 CABLE DIAGNOSTIC POSITIVE PEAK TIME REGISTER

CL45 Address: 0x1E Register Address: 0x49C Size: 16 bits

Register Name: CBL_DIAG_POS_PEAK_TIME_100

Bits	Description	Type	Default
15:14	**RESERVED**	R/O	000h
13:7	**Cable Diagnostic Positive Peak Time - Cycles** Cable Diagnostic Positive Peak Time in Cycles	R/O	0000000b
6:0	**Cable Diagnostic Positive Peak Time - Phase** Cable Diagnostic Positive Peak Time in Phase	R/O	0000000b

5.9.18 CABLE DIAGNOSTIC NEGATIVE PEAK TIME REGISTER

CL45 Address: 0x1E Register Address: 0x49D Size: 16 bits

Register Name: CBL_DIAG_NEG_PEAK_TIME_100

Bits	Description	Type	Default
15:14	**RESERVED**	R/O	000h
13:7	**Cable Diagnostic Negative Peak Time - Cycles** Cable Diagnostic Negative Peak Time in Cycles	R/O	0000000b
6:0	**Cable Diagnostic Negative Peak Time - Phase** Cable Diagnostic Negative Peak Time in Phases	R/O	0000000b

5.9.19 TC1 100BASE-T1 WORST CASE MSE REGISTER (LAN8870 ONLY)

CL45 Address: 0x1E Register Address: 0x4C1 Size: 16 bits

Register Name: TC1_MSE_WC_100

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	000000b
9	**100BASE-T1 Worst Case MSE Value Valid** 1 – 100BASE-T1 Worst Case MSE Value since last read is valid	R/O	0b
8:0	**100BASE-T1 Worst Case MSE Value** 100BASE-T1 Worst Case MSE Value since last read	R/O	000000000b

5.9.20 TC1 100BASE-T1 MSE REGISTER (LAN8870 ONLY)

CL45 Address: 0x1E Register Address: 0x4C2 Size: 16 bits

Register Name: TC1_MSE_100

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	000000b
9	**100BASE-T1 MSE Value Valid** 1 – 100BASE-T1 Current MSE Value Valid	R/O	0b
8:0	**100BASE-T1 MSE Value** 100BASE-T1 Current MSE Value	R/O	000000000b

5.9.21 TC1 100BASE-T1 SQI REGISTER (LAN8870 ONLY)

CL45 Address: 0x1E Register Address: 0x4C3 Size: 16 bits

Register Name: TC1_SQI_100

Bits	Description	Type	Default
15:8	**RESERVED**	R/O	00000000b
7:5	**100BASE-T1 SQI Value** Worst Case SQI Value between 0 and 7 since last read of this register	R/O	000b
4	**RESERVED**	R/O	0b
3:1	**100BASE-T1 SQI Value** SQI Value between 0 and 7 (7 is best). Note: Link Down will result in 0.	R/O	000b
0	**RESERVED**	R/O	0b

5.9.22 TC1 100BASE-T1 PEAK MSE REGISTER (LAN8870 ONLY)

CL45 Address: 0x1E Register Address: 0x4C4 Size: 16 bits

Register Name: TC1 PMSE_100

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	000000b
9	**100BASE-T1 Peak MSE Value Valid** 1 – 100BASE-T1 Peak MSE Value Valid	R/O	0b
8:0	**100BASE-T1 Peak MSE Value** 100BASE-T1 Peak MSE Value	R/O	000000000b

5.9.23 100BASE-T1 SQI METHOD SELECT REGISTER (LAN8870 ONLY)

CL45 Address: 0x1E Register Address: 0x115 Size: 16 bits

Register Name: SQI_METHOD_SEL

Bits	Description	Type	Default
15:3	**RESERVED**	R/O	0000h
2:0	**SQI Method Select** 000: SQI Method B (MSE Method) 010: SQI Method A (TC1)	R/W	000b

5.9.24 1000BASE-T1 CABLE DIAGNOSTICS ENABLE (LAN8871/LAN8872 ONLY)

CL45 Address: 0x1E Register Address: 0xC00 Size: 16 bits

Register Name: CBL_DIAG_1000_EN

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	000000b
9	**1000BASE Cable Diagnostics Enable** 1 - Enables Cable Diagnostics Registers for 1000BASE-T1 Cable Diagnostics Measurement	R/W	0b
8:0	**RESERVED**	R/O	000000000b

5.10 1000BASE-T1 DSP Registers

5.10.1 TC12 1000BASE-T1 DCQ/SQI MEASUREMENT ENABLE REGISTER

CL45 Address: 0x1E Register Address: 0x80D Size: 16 bits

Register Name: TC12_SQI_MEAS_EN_1000

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	000000b
9	**1000BASE-T1 DCQ/SQI Measurement Active** 0 – 1000BASE-T1 DCQ/SQI Measurement is either complete or inactive 1 – 1000BASE-T1 DCQ/SQI Measurement in progress	R/O	0b
8	**1000BASE-T1 DCQ/SQI Measurement Enable** 1 – Enables 1000BASE-T1 DCQ/SQI Measurement	R/W	0b
7:0	**RESERVED**	R/O	00000000b

5.10.2 TC12 1000BASE-T1 MSE REGISTER

CL45 Address: 0x1E Register Address: 0x8B0 Size: 16 bits

Register Name: TC12_MSE_1000

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	000000b
9	**1000BASE-T1 MSE Value Valid** 1 – 1000BASE-T1 Current MSE Value Valid	R/O	0b
8:0	**1000BASE-T1 MSE Value** 1000BASE-T1 Current MSE Value	R/O	000000000b

5.10.3 TC12 1000BASE-T1 WORST CASE MSE REGISTER

CL45 Address: 0x1E Register Address: 0x8B1 Size: 16 bits

Register Name: TC12_MSE_WC_1000

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	000000b
9	**1000BASE-T1 Worst Case MSE Value Valid** 1 – 1000BASE-T1 Worst Case MSE Value since last read is valid	R/O	0b
8:0	**1000BASE-T1 Worst Case MSE Value** 1000BASE-T Worst Case MSE Value since last read	R/O	000000000b

5.10.4 TC12 1000BASE-T1 SQI REGISTER

CL45 Address: 0x1E Register Address: 0x8B2 Size: 16 bits

Register Name: TC12_SQI_1000

Bits	Description	Type	Default
15:8	**RESERVED**	R/O	00000000b
7:5	**1000BASE-T1 SQI Value** Worst Case SQI Value between 0 and 7 since last read of this register	R/O	000b
4	**RESERVED**	R/O	0b
3:1	**1000BASE-T1 SQI Value** SQI Value between 0 and 7 (7 is best). Note: Link Down will result in 0.	R/O	000b
0	**RESERVED**	R/O	0b

5.10.5 TC12 1000BASE-T1 PEAK MSE REGISTER

CL45 Address: 0x1E Register Address: 0x8B3 Size: 16 bits

Register Name: TC12_PMSE_1000

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	000000b
9	**1000BASE-T1 Peak MSE Value Valid** 1 – 1000BASE-T1 Peak MSE Value Valid	R/O	0b
8:0	**1000BASE-T1 Peak MSE Value** 1000BASE-T1 Peak MSE Value	R/O	000000000b

5.10.6 TC12 LINK TRAINING TIME REGISTER

CL45 Address: 0x1E Register Address: 0x8D9 Size: 16 bits

Register Name: TC12_LQ_LTT

Bits	Description	Type	Default
15:12	**RESERVED**	R/O	0000b
11:0	**Link Training Time (LTT)** Information about the total link up time from enabling the PHY until the link is established. 0x00 = 0ms link time 0xFA = 250ms link time 0xFB = longer than 250ms link time	R/O	000h

5.10.7 TC12 LOCAL RECEIVER TIME REGISTER

CL45 Address: 0x1E Register Address: 0x8DA Size: 16 bits

Register Name: TC12_LQ_LRT

Bits	Description	Type	Default
15:8	**RESERVED**	R/O	00000000b
7:0	**Local Receiver Time (LRT)** Time until local receiver = OK 0x00 = 0ms until local receiver is OK 0xFA = 250ms until local receiver is OK 0xFB = > 250ms until local receiver is OK	R/O	00000000b

5.10.8 TC12 REMOTE RECEIVER TIME REGISTER

CL45 Address: 0x1E Register Address: 0x8DB Size: 16 bits

Register Name: TC12_LQ_RRT

Bits	Description	Type	Default
15:8	**RESERVED**	R/O	0x00
7:0	**Remote Receiver Time (RRT)** Time until remote receiver = OK 0x00 = 0ms until remote receiver is OK 0xFA = 250ms until remote receiver is OK 0xFB = > 250ms until remote receiver is OK	R/O	0x00

5.10.9 TC12 LINK TRAINING TIME 1US COUNTER REGISTER

CL45 Address: 0x1E Register Address: 0x9FA Size: 16 bits

Register Name: TC12_LQ_LTT_1US_CNTR

Bits	Description	Type	Default
15:4	**RESERVED**	R/O	000h
3:0	**Link Training Time 1us Counter** For LTT Timer, this register provides accuracy up to 1us.	R/O	0000b

5.10.10 TC12 LINK TRAINING TIME 10US COUNTER REGISTER

CL45 Address: 0x1E Register Address: 0x9FB Size: 16 bits

Register Name: TC12_LQ_LTT_10US_CNTR

Bits	Description	Type	Default
15:4	**RESERVED**	R/O	000h
3:0	**Link Training Time 10us Counter** For LTT Timer, this register provides accuracy up to 10us.	R/O	0000b

5.10.11 TC12 LINK TRAINING TIME 100US COUNTER REGISTER

CL45 Address: 0x1E Register Address: 0x9FC Size: 16 bits

Register Name: TC12_LQ_LTT_100US_CNTR

Bits	Description	Type	Default
15:4	**RESERVED**	R/O	000h
3:0	**Link Training Time 100us Counter** For LTT Timer, this register provides accuracy up to 100us.	R/O	0000b

5.11 Miscellaneous Registers

5.11.1 MAC_MODE_SEL CONFIGURATION REGISTER

CL45 Address: 0x1E Register Address: 0xA00 Size: 16 bits

Register Name: MIS_CFG_REG0

Bits	Description	Type	Default
15:2	**RESERVED**	R/O	0000h
1:0	**MAC_MODE_SEL Configuration** MAC Operating Mode Select: 2'b00 - Reserved; 2'b01 - RGMII 2'b10 - Reserved 2'b11 - SGMII	LAN8870: R/W LAN8871/ LAN8872: R/O	LAN8870/ LAN8871: 01b LAN8872: 11b

5.11.2 TX RGMII DELAY REGISTER (LAN8870/LAN8871 ONLY)

CL45 Address: 0x1E Register Address: 0xA01 Size: 16 bits

Register Name: MIS_DLL_CFG_REG0

Bits	Description	Type	Default
15	**TXC RGMII 2ns Delay Enable** 0 – Disables TXC delay 1 – Enables 2ns delay on TXC from TXD[3:0]/TX_CTL	R/O	0b
14:8	**TX DLL TAP Adjustment** Control register to adjust Transmit DLL tuned tap to compensate output mux delay. The default value is the preferred value for operation	R/W	0011011b

7:1	**TX DLL TAP Select** Control register to select tap element to prevent glitches that might occur when delay is first locked for Transmit DLL	R/W	1000011b
0	**TX DLL Enable** Enable signal for TX DLL tuning FSM for balancing clocks during RGMII mode. This needs to be asserted HIGH when in RGMII mode and RGMII TX Delay is necessary.	R/W	0b

5.11.3 RX RGMII DELAY REGISTER (LAN8870/LAN8871 ONLY

CL45 Address: 0x1E Register Address: 0xA02 Size: 16 bits

Register Name: MIS_DLL_CFG_REG1

Bits	Description	Type	Default
15	**RXC RGMII 2ns Delay Enable** 0 – Disables RXC delay 1 – Enables 2ns delay on RXC from RXD[3:0]/RX_CTL	R/O	1b
14:8	**RX DLL TAP Adjustment** Control register to adjust Receive DLL tuned tap to compensate output mux delay. The default value is the preferred value for operation	R/W	0011011b
7:1	**RX DLL TAP Select** Control register to select tap element to prevent glitches that might occur when delay is first locked for Receive DLL	R/W	1000011b
0	**RX DLL Enable** Enable signal for RX DLL tuning FSM for balancing clocks during RGMII mode. This needs to be asserted HIGH when in RGMII mode and RGMII RX Delay is necessary.	R/W	1b

5.11.4 LOOPBACK REGISTER

CL45 Address: 0x1E Register Address: 0xA03 Size: 16 bits

Register Name: MIS_CFG_REG2

Bits	Description	Type	Default
15:4	**RESERVED**	R/O	268h
3	**I/O Loopback** Control register to adjust Receive DLL tuned tap to compensate output mux delay. The default value is the preferred value for operation	R/W	0b

2	**Far End Loopback** Control register to select tap element to prevent glitches that might occur when delay is first locked for Receive DLL	R/W	0b
1	**Near End Loopback** 1 – Enables Near End Loopback	R/W	0b
0	**RESERVED**	R/O	0b

5.11.5 RX PACKET ERROR COUNTER REGISTER

CL45 Address: 0x1E Register Address: 0xA09 Size: 16 bits

Register Name: MIS_PKT_STAT_REG3

Bits	Description	Type	Default
15:0	**RX Packet Error Counter** Counter that tracks errored packets detected by PCS in RX direction. This register saturates at 0xFFFF in the case of more errors. **Note:** Reading this field will clear it.	R/O	0000h

5.11.6 ETHERNET PACKAGE GENERATOR (EPG) ENABLE REGISTER

CL45 Address: 0x1E Register Address: 0xA0D Size: 16 bits

Register Name: MIS_EPG_CFG1

Bits	Description	Type	Default
15	**EPG Enable** 0 – Stops EPG 1- Runs EPG	R/O	0b
14	**EPG FCS Generation** 0 – Good FCS 1 – Bad FCS	R/W	0b
13:9	**RESERVED**	R/O	00000b
8	**EPG Run Status** 1 – EPG is running	R/O	0b
7	**RESERVED**	R/O	0b
6	**EPG Random Packet Length** EPG Generates Random Packet Lengths	R/W	0b
5:4	**RESERVED**	R/O	00b

3	**EPG Random Payload Enable** EPG Random Payload Enable. When set to 1, Random payload is selected and when set to 0, Fixed payload. In case of fixed payload, epg_payload (Register 1E.0A11) is used to replicate across the generated EPG packet based on epg_pkt_len configuration in Register 1E.0A18.	R/W	0b
2	**EPG Multi-Burst Enable** EPG Generates Multiple bursts of Packets	R/W	0b
1	**EPG Continuous Run Enable** 0 - Run EPG for single iteration 1 - Run EPG in Continuous mode	R/W	0b
0	**EPG Enable** Enables all modes in this register	R/W	0b

5.11.7 ETHERNET PACKAGE GENERATOR (EPG) PAYLOAD REGISTER

CL45 Address: 0x1E Register Address: 0xA11 Size: 16 bits

Register Name: MIS_EPG_PYLD

Bits	Description	Type	Default
15:0	**EPG Payload** EPG Packet Payload Data. This payload data gets replicated across the packet.	R/W	0000h

5.11.8 ETHERNET PACKAGE GENERATOR (EPG) PACKET BURST COUNT REGISTER

CL45 Address: 0x1E Register Address: 0xA12 Size: 16 bits

Register Name: MIS_EPG_BRST_CNT

Bits	Description	Type	Default
15:0	**EPG Packet Burst Count** Number of Packets sent in EPG burst	R/W	000Ah

5.11.9 ETHERNET PACKAGE GENERATOR (EPG) BURST COUNT REGISTER

CL45 Address: 0x1E Register Address: 0xA13 Size: 16 bits

Register Name: MIS_EPG_MBR_CNT

Bits	Description	Type	Default
15:0	**EPG Burst Count** Number of bursts sent in a sequence during EPG mode	R/W	001Eh

5.11.10 ETHERNET PACKAGE GENERATOR (EPG) INTERPACKET GAP REGISTER

CL45 Address: 0x1E Register Address: 0xA14 Size: 16 bits

Register Name: MIS_EPG_IPG_CFG

Bits	Description	Type	Default
15:0	**EPG Interpacket Gap** EPG Interpacket gap in bytes.	R/W	000Ch

5.11.11 ETHERNET PACKAGE GENERATOR (EPG) PAYLOAD LENGTH REGISTER

CL45 Address: 0x1E Register Address: 0xA18 Size: 16 bits

Register Name: MIS_EPG_PLEN

Bits	Description	Type	Default
15:0	**EPG Packet Length** EPG Interpacket gap in bytes.	R/W	007Dh

5.12 LED Registers

5.12.1 LED CONFIGURATION REGISTER

CL45 Address: 0x1E Register Address: 0xC03 Size: 16 bits

Register Name: COMMON_LED

Bits	Description	Type	Default
15:9	**RESERVED**	R/O	0000000b
8	**RESERVED**	R/W	0b

7:4	**LED Invert Polarity** Invert the polarity of the LED whose bit is set (LED default polarity is active-low). bit 3 => LED4 bit 2 => LED3 bit 1 => LED2 bit 0 => LED1	R/W	0000b
3:0	**LED Tri-State** When set, tri-state each LED when the LED level is high (otherwise actively drive it high for high levels). Each LED is always driven low when the LED level is low. bit 3 => LED4 bit 2 => LED3 bit 1 => LED2 bit 0 => LED1	R/W	0000b

5.12.2 LED1/LED2 MODE SELECTION REGISTER

CL45 Address: 0x1E Register Address: 0xC04 Size: 16 bits

Register Name: COMMON_LED2_LED1

Bits	Description	Type	Default
15:13	**RESERVED**	R/W	000b
12:8	**LED2 Mode Selection** Mode select for LED2. For each of the modes, the respective status will propagate to LED2. 5h0 => Link Status with Activity for any speed. 5'h1 => Link Status with Activity for speed 1000. 5'h2 => Link Status with Activity for speed 100 5'h3 => Link Status (without Activity blinking) for any speed. 5'h4 => RESERVED 5'h5 => Local Receiver Status 5'h6 => Remote Receiver Status 5'h7 => Negotiated Speed (ON: 1000; OFF: 100). 5'h8 => Master/Slave Mode (ON: Master; OFF: Slave) 5'h9 => PCS TX Error Status 5'hA => PCS RX Error Status 5'hB => PCS TX Activity 5'hC => PCS RX Activity 5'hD => Wake-on-LAN 5'hE => Force LED OFF 5'hF => Force LED ON 5'h10-5'h1F => RESERVED		00001b
7:4	**RESERVED**		000b

4:0	**LED1 Mode Selection** Mode select for LED1. For each of the modes, the respective status will propagate to LED1. Mode select definitions are the same as for LED2.		00000b

5.12.3 LED3/LED4 MODE SELECTION REGISTER

CL45 Address: 0x1E Register Address: 0xC05 Size: 16 bits

Register Name: COMMON_LED4_LED3

Bits	Description	Type	Default
15:13	**RESERVED**	R/W	000b
12:8	**LED4 Mode Selection** Mode select for LED4. For each of the modes, the respective status will propagate to LED4. 5h0 => Link Status with Activity for any speed. 5'h1 => Link Status with Activity for speed 1000. 5'h2 => Link Status with Activity for speed 100 5'h3 => Link Status (without Activity blinking) for any speed. 5'h4 => RESERVED 5'h5 => Local Receiver Status 5'h6 => Remote Receiver Status 5'h7 => Negotiated Speed (ON: 1000; OFF: 100). 5'h8 => Master/Slave Mode (ON: Master; OFF: Slave) 5'h9 => PCS TX Error Status 5'hA => PCS RX Error Status 5'hB => PCS TX Activity 5'hC => PCS RX Activity 5'hD => Wake-on-LAN 5'hE => Force LED OFF 5'hF => Force LED ON 5'h10-5'h1F => RESERVED		01010b
7:4	**RESERVED**		000b
4:0	**LED3 Mode Selection** Mode select for LED3. For each of the modes, the respective status will propagate to LED3. Mode select definitions are the same as for LED4.		01000b

5.12.4 TC10 COMMON PORT INTERRUPT MASK REGISTER

CL45 Address: 0x1E Register Address: 0xC10 Size: 16 bits

Register Name: COMMON_PORT_INT_EN_CFG

Bits	Description	Type	Default
15:7	**RESERVED**	R/O	000000000b
6	**WUP/WUR Received Interrupt Mask** Interrupt mask for Device Receiving WUP/WUR Interrupt	R/W	0b
5	**LPS Received Interrupt Mask** Interrupt mask for Device Receiving LPS Interrupt	R/W	0b
4	**WAKE_IN Interrupt Mask** Interrupt mask for Device Wake through WAKE_IN pin Interrupt	R/W	0b
3:0	**RESERVED**	R/O	000b

5.12.5 TC10 COMMON PORT INTERRUPT STATUS REGISTER

CL45 Address: 0x1E Register Address: 0xC11 Size: 16 bits

Register Name: COMMON_PORT_INT_STAT

Bits	Description	Type	Default
15:7	**RESERVED**	R/O	000000000b
6	**WUP/WUR Received Interrupt** Interrupt for Device Receiving WUP/WUR	R/W	0b
5	**LPS Received Interrupt Mask** Interrupt for Device Receiving LPS	R/W	0b
4	**WAKE_IN Interrupt Mask** Interrupt for Device Wake through WAKE_IN pin	R/W	0b
3:0	**RESERVED**	R/O	000b

5.13 TC10 Wake/Sleep Registers

5.13.1 TC10 WAKE OUT REGISTER

CL45 Address: 0x1E Register Address: 0xC20 Size: 16 bits

Register Name: TC10_REG_REG15

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	0000h
0	**WAKE OUT Pin Request Active** 1 – WAKE_OUT Pin is Enabled in Device	R/O	0b

5.13.2 TC10 WAKE/SLEEP REQUEST SEND REGISTER

CL45 Address: 0x1E Register Address: 0xC21 Size: 16 bits

Register Name: TC10_REG_REG16

Bits	Description	Type	Default
15:14	**RESERVED**	R/O	00b
13	**Wake Request Send (Send WUP/WUR)** Device sends WUP/WUR Wake Request Note: A WUP can only be sent when device is in Sleep State if INH does not control non-VBAT voltage regulators to the device.	R/W	0b
12	**Sleep Request Send (Send LPS)** Device sends LPS Request	R/W	0b
11:0	**RESERVED**	R/O	000h

5.13.3 TC10 INTERRUPT REGISTER

CL45 Address: 0x1E Register Address: 0xC22 Size: 16 bits

Register Name: TC10_REG_REG24

Bits	Description	Type	Default
15:5	**RESERVED**	R/O	000h
4	**OAM LPS Received Interrupt (1000BASE-T1 Only)** Interrupt for Receiving OAM Message with LPS flag set. Indicates Device received LPS through OAM Message	R/O	0b

3	**OAM WUR Received Interrupt (1000BASE-T1 Only)** Interrupt for Receiving OAM Message with WUR flag set. Indicates Device received WUR through OAM Message	R/O	0b
2	**WAKE_IN Interrupt** Interrupt indicating device wake up occurred from WAKE_IN Pulse	R/O	0b
1	**LPS Received Interrupt (100BASE-T1 and 1000BASE-T1)** Interrupt indicating LPS has been received	R/O	0b
0	**WUP/WUR Received Interrupt (100BASE-T1 and 1000BASE-T1)** Interrupt indicating either a WUP or a WUR has been received	R/O	0b

5.13.4 TC10 CONFIGURATION SETUP REGISTER

CL45 Address: 0x1E Register Address: 0xC24 Size: 16 bits

Register Name: TC10_MISC32

Bits	Description	Type	Default
15	**EPG Enable** 0 – Stops EPG 1 – Runs EPG	R/O	0b
14:13	**RESERVED**	R/O	00b
12	**WAKE_IN Polarity** Polarity of the WAKE_IN pin. 0b: Active-High (Default) Wake event detected on a low-to-high transition. 1b: Active-Low Wake event detected on a high-to-low transition.	R/W	0b
11	**WAKE_OUT Polarity** Polarity of the WAKE_OUT pin. 0b: Active-High (Default) Pin supports generation of a low-to-high pulse upon detection of wakeup event. 1b: Active-Low Pin supports generation of a high-to-low pulse upon detection of wakeup event.	R/W	0b
10:9	**WAKE_OUT Mode** Defines the mode of operation for the WAKE_OUT pin. 00b: Push/Pull driver 01b: Open Source 1xb: Open Drain	R/W	00b

8	**INH Mode** Mode of operation for the INH pin. 0b: Open Source Mode (Default) Active State: Drive 1b (VBAT) TC10 Sleep State: High-Ohmic In this mode an external pull-down resistor must be placed on this pin 1b: Open Drain Mode Active State: High-Ohmic TC10 Sleep State: 0b. In this mode an external pull-up resistor to VBAT must be on this pin	R/O	0b
7	**WAKE_OUT Auto-Forward Enable** When set WAKE_OUT is autonomously asserted by HW in response to wake up request (WUP/WAKE_IN).	R/O	0b
6	**Ring Oscillator Status** Ring Oscillator Status. When set, Ring Oscillator (for TC10 sleep mode) is enabled	R/O	0b
5	**Ring Oscillator Enable** When set, Ring Oscillator (for TC10 sleep mode) is enabled	R/W	1b
4	**WAKE_OUT Debounce Units** Unit for the WAKE_OUT Debouncer to determine wake pulse (Register 1E.0C25). 0 – us 1 – ms	R/W	0b
3	**WAKE_IN Debounce Units** Unit for the WAKE_IN Debouncer to determine wake pulse (Register 1E.0C25). 0 – us 1 – ms	R/W	0b
2	**Sleep Enable** Enables device to enter TC10 Sleep state	R/W	0b
1	**INH Enable** INH Enabled for TC10 operation. When enabled, INH is low when device is in sleep state and INH is high when the device is active.	R/W	1b
0	**WAKE_IN Enable** Enables WAKE_IN to wake the device from TC10 Sleep State	R/W	1b

5.13.5 TC10 WAKE_OUT CONFIGURATION REGISTER

CL45 Address: 0x1E Register Address: 0xC25 Size: 16 bits

Register Name: TC10_MISC33

Bits	Description	Type	Default
15:8	**WAKE_IN Debounce Value** WAKE_IN pulse width to determine wake event occurred. The units are determined by Register 1E.0C24 bit 13 (0 – us, 1 – ms)	R/O	00000000b
7:0	**WAKE_OUT Pulse Length** Pulse width of wake signal indication on WAKE_OUT pin. The units are determined by Register 1E.0C24 bit 4 (0 – us, 1 - ms)	R/O	00000000b

5.13.6 TC10 STATE REGISTER

CL45 Address: 0x1E Register Address: 0xC26 Size: 16 bits

Register Name: TC10_MISC34

Bits	Description	Type	Default
15:3	**RESERVED**	R/O	0000h
2:0	**TC10 Current State** Indicates the current state of TC10 State Machine. 000b: START (RESET) 001b: NORMAL 010b: SLEEP_ACK 011b; SLEEP_REQ 100b: SLEEP_FAIL 101b: SLEEP_SILENT 110b: SLEEP	R/O	000b

5.13.7 TC10 WUP/WUR CONFIGURATION REGISTER

CL45 Address: 0x1E Register Address: 0xC27 Size: 16 bits

Register Name: TC10_MISC36

Bits	Description	Type	Default
15	**VBAT Port WUP Copy Register** When set the VBAT port registers are copied from the core domain and into the VBAT domain. This bit clears after the operation completes	R/W/SC	0b
14:13	**WUP Filter Length** Tunes the WUP detection filter.	R/W	00b

12	**WUP Auto-Forward Enable** When set WUP packet is automatically send in response to the assertion of the WAKE_IN pin while in sleep.	R/W	0b
11	**WUP Debounce Units** Unit for the WUP Debouncer to determine wake pulse (bits 7:0 in this register). 0 – us 1 – ms	R/W	0b
10:9	**Wake Signal Detection Tune** Used to tune WUP signal detector block on the MDI interface.	R/W	00b
8	**WUP Enable over MDI** When set, the MDI pins are enabled for wakeup event detection while device is in Sleep state. This bit is required for TC10 operation.	R/W	0b
7:0	**WAKE Up Pulse (WUP) Debounce Value** This register defines the value used for the WUP debouncer. This register has units of 8 µs. Suggested value is 0x10.	R/W	00000000b

5.13.8 TC10 SLEEP SILENT LOCAL SLEEP REGISTER

CL45 Address: 0x1E Register Address: 0xC28 Size: 16 bits

Register Name: TC10_MISC37

Bits	Description	Type	Default
15:6	**RESERVED**	R/O	000h
5	**TC10 Sleep Silent Enable** Enables Device for Sleep Silent State. This is needed for the device to be able to enter TC10 Sleep state	R/O	00b
4:1	**RESERVED**	R/O	0000b
0	**Force Sleep** TC10 Force Sleep – Sets Device into Local Sleep State	R/W	0b

5.13.9 TC10 WAKE UP PORT CONTROL REGISTER

CL45 Address: 0x1E Register Address: 0xC29 Size: 16 bits

Register Name: TC10_MISC46

Bits	Description	Type	Default
15:3	**RESERVED**	R/O	000h
2	**Ring Oscillator Enable - Active** Enables Ring Oscillator from being disabled when in a non-SLEEP state.	R/O	1b
1:0	**RESERVED**	R/O	00b

5.13.10 TC10 WAKE UP COMMON REGISTER

CL45 Address: 0x1E Register Address: 0xC2A Size: 16 bits

Register Name: TC10 WAKE_COMMON

Bits	Description	Type	Default
15:2	**RESERVED**	R/O	000h
1	**100BASE-T1 WUP Send** When device is either in 100BASE-T1 forced speed or Auto-Negotiation mode with 100BASE-T1 speed advertised, this bit enables the device to send a 100BASE-T1 WUP to the link partner.This bit should be cleared in 1000BASE-T1 forced speed. **Note:** This bit only has meaning for LAN8870.	R/W	0b
0	**RESERVED**	R/O	0b

5.13.11 TC10 SLEEP ABORT/SLEEP REJECT REGISTER

CL45 Address: 0x1E Register Address: 0xC2D Size: 16 bits

Register Name: TC10_SLEEP_ABRT

Bits	Description	Type	Default
15:6	**RESERVED**	R/O	000h
5	**Sleep Abort** When set, the device will abort a pending sleep request	R/W	0b
4	**Sleep Reject** When set, the device will reject any sleep requests (rejects LPS)	R/W	0b
3:0	**RESERVED**	R/O	0000b

5.13.12 TC10 SLEEP FAIL REGISTER

CL45 Address: 0x1E Register Address: 0xC2E Size: 16 bits

Register Name: TC10_SLEEP_FAIL_STATUS

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	0000h
0	**Sleep Fail** Indicates when device fails to enter sleep state. Latches high. Clears on read.	R/O	0b

5.13.13 TC10 SLEEP REQUEST TIMER REGISTER

CL45 Address: 0x1E Register Address: 0xC34 Size: 16 bits

Register Name: TC10_SLEEP_REQ_TMR_CFG

Bits	Description	Type	Default
15:0	**Sleep Request Timer** TC-10 Sleep request timer in terms of milli-seconds. Default value is 16 ms (applicable for both 100T1 and 1000T1 speeds).	R/W	0010h

5.13.14 TC10 SLEEP ACKNOWLEDGE REGISTER

CL45 Address: 0x1E Register Address: 0xC35 Size: 16 bits

Register Name: TC10_SLEEP_ACK_TMR_CFG

Bits	Description	Type	Default
15:0	**Sleep Acknowledge Timer** TC-10 Sleep Acknowledge timer in terms of milli-seconds. Default value is 8 ms (applicable for both 100T1 and 1000T1 speeds).	R/W	0008h

5.14 INT/GPIO/SGMII Registers

5.14.1 INTERRUPT STATUS REGISTER

CL45 Address: 0x1E Register Address: 0xF000 Size: 16 bits

Register Name: INT_STS

Bits	Description	Type	Default
15:11	**RESERVED**	R/O	00000b
10	**GPIO Status** Interrupt for GPIO Indication	R/O	0b
9	**PVT Status** Interrupt for PVT Status Indication	R/O	0b
8:6	**RESERVED**	R/O	000b
5	**UVOV Status** Interrupt for UVOV Status Indication	R/O	0b
4:2	**RESERVED**	R/O	000b
1	**Link Up Status** Interrupt for Link Up Status Indication	R/O	0b
0	**Link Down Status** Interrupt for Link Down Status Indication	R/O	0b

5.14.2 INTERRUPT MASK REGISTER

CL45 Address: 0x1E Register Address: 0xF001 Size: 16 bits

Register Name: INT_MSK

Bits	Description	Type	Default
15:11	**RESERVED**	R/O	00011b
10	**GPIO Interrupt Mask** GPIO Indication Interrupt Mask 0 – Interrupt Enabled 1 – Interrupt Disabled	R/O	1b
9	**PVT Interrupt Mask** PVT Status Interrupt Mask 0 – Interrupt Enabled 1 – Interrupt Disabled	R/O	1b
8:6	**RESERVED**	R/O	000b

5	**UVOV Interrupt Mask** UVOV Status Interrupt Mask 0 – Interrupt Enabled 1 – Interrupt Disabled	R/O	1b
4:2	**RESERVED**	R/O	111b
1	**Link Up Interrupt Mask** Link Up Status Interrupt Mask 0 – Interrupt Enabled 1 – Interrupt Disabled	R/O	1b
0	**Link Down Interrupt Mask** Link Down Status Interrupt Mask 0 – Interrupt Enabled 1 – Interrupt Disabled	R/O	1b

5.14.3 CONTROL 1 REGISTER

CL45 Address: 0x1E Register Address: 0xF002 Size: 16 bits

Register Name: CONTROL1

Bits	Description	Type	Default
15	**RESERVED**	R/O	0b
14:13	**CLKOUT Select** Determine the frequency of the CLKOUT pin. 00: CLK_XTAL (25 MHz) 01: 25 MHz 10: 50 MHz 11: 125 MHz	R/W	00b
12	**CLOCKOUT Enable** When set, clock from bits CLKOUT Select field is output on CLKOUT pin.	R/W	0b
11	**RESERVED**	R/O	0b
10:8	**IEEE1588 Pin Select** Each bit enables the corresponding 1588 function in the pin mux. 1588_pin_sel[2] = 1588_CLK_LD_ADJ 1588_pin_sel[1] = 1588_REF_CLK 1588_pin_sel[0] = 1588_EVT	R/O	000b
7	**RESERVED**	R/O	0b
6:4	**GPIO Pin Select** Each bit enables the corresponding gpio in the pin mux. gpio_pin_sel[2] = GPIO3 gpio_pin_sel[1] = GPIO2 gpio_pin_sel[0] = GPIO1	R/O	000b
3:2	**RESERVED**	R/O	00b

1:0	**LED Pin Select** Each bit enables the corresponding LED in the pin mux. led_pin_sel[0] = LED1 led_pin_sel[1] = LED4	R/O	00b

5.14.4 GPIO DIRECTION REGISTER

CL45 Address: 0x1E Register Address: 0xF00A Size: 16 bits

Register Name: GPIO_DIR

Bits	Description	Type	Default
15:3	**RESERVED**	R/O	0000h
2:0	**GPIO Direction** When set, enables the corresponding GPIO as an output. When cleared the GPIO is enabled as an input.	R/W	000b

5.14.5 GPIO BUFFER REGISTER

CL45 Address: 0x1E Register Address: 0xF00B Size: 16 bits

Register Name: GPIO_BUF

Bits	Description	Type	Default
15:3	**RESERVED**	R/O	0000h
2:0	**GPIO Buffer Type** When set, the output buffer for the corresponding GPIO signal is configured as a push/pull driver. When cleared, the corresponding GPIO signal is configured as an open-drain driver.	R/W	000b

5.14.6 GPIO DATA REGISTER

CL45 Address: 0x1E Register Address: 0xF00C Size: 16 bits

Register Name: GPIO_DATA

Bits	Description	Type	Default
15:3	**RESERVED**	R/O	0000h
2:0	**GPIO Data** When enabled as an output, the value written is reflected on the GPIO. When read, the value always reflects the current state of the corresponding GPIO pin, regardless of the value written or the GPIO direction.	R/W	000b

5.14.7 GPIO INTERRUPT STATUS REGISTER

CL45 Address: 0x1E Register Address: 0xF00D Size: 16 bits

Register Name: GPIO_INT_STS

Bits	Description	Type	Default
15:3	**RESERVED**	R/O	0000h
2:0	**GPIO Interrupt Status** Interrupts generated from the GPIOs. **Note:** The sources for these interrupts are level sensitive. **Note:** The GPIO inputs must be stable for ~16ns (2 consecutive 125MHz edges) to be recognized. **Note:** Reading this field will clear it.	R/W	000b

5.14.8 GPIO INTERRUPT MASK REGISTER

CL45 Address: 0x1E Register Address: 0xF00E Size: 16 bits

Register Name: GPIO_INT_MSK

Bits	Description	Type	Default
15:3	**RESERVED**	R/O	0000h
2:0	**GPIO Interrupt Mask** When set, the respective GPIO interrupt is disabled. When clear, the respective GPIO interrupt is enabled.	R/W	111b

5.14.9 GPIO INTERRUPT POLARITY REGISTER

CL45 Address: 0x1E Register Address: 0xF00F Size: 16 bits

Register Name: GPIO_INT_POL

Bits	Description	Type	Default
15:3	**RESERVED**	R/O	0000h
2:0	**GPIO Interrupt Polarity** When clear, an interrupt is triggered when the GPIO input is low. When set, an interrupt is triggered when the GPIO input is high.	R/W	000b

5.14.10 GPIO INTERRUPT PU/PD OVERRIDE REGISTER

CL45 Address: 0x1E Register Address: 0xF010 Size: 16 bits

Register Name: GPIO_PU_PD_OVR

Bits	Description	Type	Default
15:6	**RESERVED**	R/O	000h
5:4	**GPIO3 PU/PD Override Interrupt Polarity** 00 = No Override (PU or PD determined by hardware) 01 = GPIO3 has Pullup, no Pulldown 10 = GPIO3 has Pulldown, no Pullup 11 = GPIO3 has no Pullup, no Pulldown	R/W	00b
3:2	**GPIO2 PU/PD Override Interrupt Polarity** 00 = No Override (PU or PD determined by hardware) 01 = GPIO2 has Pullup, no Pulldown 10 = GPIO2 has Pulldown, no Pullup 11 = GPIO2 has no Pullup, no Pulldown	R/W	00b
1:0	**GPIO1 PU/PD Override Interrupt Polarity** 00 = No Override (PU or PD determined by hardware) 01 = GPIO1 has Pullup, no Pulldown 10 = GPIO1 has Pulldown, no Pullup 11 = GPIO1 has no Pullup, no Pulldown	R/W	00b

5.14.11 SGMII/RGMII MODE SELECT REGISTER (LAN8870 ONLY)

CL45 Address: 0x1E Register Address: 0xF01A Size: 16 bits

Register Name: XGMII_CTL

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	000h
0	**SGMII/RGMII Mode Select** This bit controls the RGMII_SGMII mux. 0 – MAC is in RGMII Mode 1 – MAC is in SGMII Mode **Note:** Default is set by MAC_MODE_SEL strap. If MAC_MODE_SEL strap is floated, default is RGMII.	R/W	00b

5.14.12 RGMII CONTROL REGISTER (LAN8871 ONLY)

CL45 Address: 0x1E Register Address: 0xF01A Size: 16 bits

Register Name: RGMII_CTL

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	000h
0	**RGMII Mode Select** 0 – MAC is in RGMII Mode	R/W	0b

5.14.13 SGMII CONTROL REGISTER (LAN8872 ONLY)

CL45 Address: 0x1E Register Address: 0xF01A Size: 16 bits

Register Name: SGMII_CTL

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	000h
0	**SGMII Mode Select** 1 – MAC is in SGMII Mode	R/W	1b

5.14.14 SGMII HARD RESET REGISTER (LAN8870/LAN8872 ONLY)

CL45 Address: 0x1E Register Address: 0xF01D Size: 16 bits

Register Name: SGMII_HRST

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	000h
0	**SGMII Hard Reset** When set this resets the SGMII configuration registers to their default state.	R/W	0b

5.14.15 SGMII SOFT RESET REGISTER (LAN8870/LAN8872 ONLY)

CL45 Address: 0x1E Register Address: 0xF01E Size: 16 bits

Register Name: SGMII_SRST

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	000h
0	**SGMII Soft Reset** When set this resets the SGMII Extender, XAUI PHY, and the SGMII PCS blocks but does not affect the state of all SGMII configuration registers.	R/W	0b

5.14.16 SGMII CONTROL REGISTER (LAN8870/LAN8872 ONLY)

CL45 Address: 0x1E Register Address: 0xF02C Size: 16 bits

Register Name: SGMII_CR_CTL

Bits	Description	Type	Default
15:2	**RESERVED**	R/O	000h
1	**SGMII Control Register Read/Write** This bit controls whether a Read or Write operation is to be performed 0 = read 1 = write	R/W	0b
0	**START Busy** Assert this bit to initiate a CR read or write transfer. The bit self-clears when the transfer is completed. This bit must be deasserted before writing to the SGMII Control Register, SGMII Address Register, or the SGMII Data Register. 0 = CR interface not busy 1 = CR interface busy	R/W	0b

5.14.17 SGMII ADDRESS REGISTER (LAN8870/LAN8872 ONLY)

CL45 Address: 0x1E Register Address: 0xF02D Size: 16 bits

Register Name: SGMII_CR_ADDR

Bits	Description	Type	Default
15:0	**SGMII Address** This field provides the register address for the CR read or write transfer. This field must not be changed when START_BUSY is asserted.	R/W	0000h

5.14.18 SGMII DATA REGISTER (LAN8870/LAN8872 ONLY)

CL45 Address: 0x1E Register Address: 0xF02E Size: 16 bits

Register Name: SGMII_CR_DATA

Bits	Description	Type	Default
15:0	**SGMII Data** This field provides the data for the CR read or write transfer. This field must not be changed when START_BUSY is asserted.	R/W	0000h

5.14.19 SGMII VREG BYPASS CONTROL REGISTER (LAN8870/LAN8872 ONLY)

CL45 Address: 0x1E Register Address: 0xF02F Size: 16 bits

Register Name: SGMII_VREG_BYP

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	0003h
0	**VREG Bypass** Controls the VREG_BYPASS input pin into the XAUI PHY. 1 = SGMII will be powered directly from 2.5V (regulator bypassed) 0 = SGMII will be powered from internal 2.5V regulator (regulator in use)	R/W	0b

5.14.20 SGMII PCS CONFIGURATION AND STATUS REGISTER (LAN8870/LAN8872 ONLY)

CL45 Address: 0x1E Register Address: 0xF034 Size: 16 bits

Register Name: SGMII_PCS_CFG

Bits	Description	Type	Default
15:12	**RESERVED**	R/O	0000b
11	**SGMII Save Preamble** Preserves preamble when using PCH/MCH or preemption. When this bit is cleared, the PCS may occasionally drop a preamble byte due to even/odd byte alignment requirements 0 = Preamble Preservation disabled 1 = Preamble Preservation enabled	R/W	1b
10	**SGMII Link Status Type** Define type of SGMII link status indication 1 = SGMII Link Partner up/down indication from lp_adv_ability[15] 0 = Sync Status from SGMII PCS state machine	R/O	0003h

9	**SGMII VREG Bypass** Controls the VREG_BYPASS input pin into the XAUI PHY. 1 = SGMII will be powered directly from 2.5V (regulator bypassed) 0 = SGMII will be powered from internal 2.5V regulator (regulator in use)	R/W	0b
8	**RESERVED**	R/O	0b
7	**SGMII Signal Detect Polarity** Selects the polarity of the signal_detect line 0 = a 0 on the signal_detect line indicates active signal 1 = a 1 on the signal_detect line indicates active signal		1b
6	**SGMII Signal Detect Enable** Signal detect enable 0 = the signal_detect line is ignored. The SGMII PCS assumes an active signal_detect at all times. 1 = the signal_detect line is used to determine if a signal is detected		1b
5	**SGMII Signal Detect** Provides the current status of the SGMII signal detect. 0 = no signal is detected 1= signal is detected		0b
4	**SGMII Link Status** Indicates whether the SGMII link is up or down. The SGMII link is up when the ANEG state machine is in either the LINK_OK state, or the ANEG_DISABLE_LINK_OK state. 0 = SGMII link is down 1 = SGMII is up	R/O	0b
3	**SGMII Sync Status** Indicates if the SGMII PCS has successfully synchronized 0 = SGMII PCS is not synchronized 1 = SGMII PCS is synchronized	R/O	0b
2	**RESERVED**	R/O	0b
1	**SGMII Link Status Change** This bit indicates a change of SGMII PCS Link status. 0 = no change of SGMII PCS Link status 1 = SGMII PCS Link status has changed **Note:** Reading this field will clear it	R/O	0b
0	**SGMII Sync Status Change** This bit indicates a change of SGMII PCS Sync status. 0 = no change of SGMII PCS Sync status 1 = SGMII PCS Sync status has changed **Note:** Reading this field will clear it.	R/O	0b

5.14.21 CHIP HARD RESET REGISTER

CL45 Address: 0x1E Register Address: 0xF03E Size: 16 bits

Register Name: CHIP_HARD_RST

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	0000h
0	**Chip Hard Reset** Write a one to this bit to perform a chip-wide hard reset.	R/W	0b

5.14.22 CHIP SOFT RESET REGISTER

CL45 Address: 0x1E Register Address: 0xF03F Size: 16 bits

Register Name: CHIP_SOFT_RST

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	0000h
0	**Chip Soft Reset** Write a one to this bit to perform a chip-wide soft reset.	R/W	0b

5.14.23 CONFIGURATION STRAP STATUS REGISTER

CL45 Address: 0x1E Register Address: 0xF041 Size: 16 bits

Register Name: SKU_DBG_STS

Bits	Description	Type	Default
15:12	**RESERVED**	R/O	0000b
11:3	**Configuration Strap Status** Returns the status of the STRAP pins. STRAP_STS[8]: MAC_MODE_STRP STRAP_STS[7]: Reserved STRAP_STS[6]: Reserved STRAP_STS[5]: AUTO_MODE_EN_STRP STRAP_STS[4]: MODE_STRP/PHYAD4_STRP STRAP_STS[3]: AUTO_NEG_EN_STRP/PHYAD3_STRP STRAP_STS[2]: SPEED_SEL_STRP/PHYAD2_STRP STRAP_STS[1]: PHYAD1_STRP STRAP_STS[0]: PHYAD0_STRP **Note:** The reset value depends on the strap values.	R/W	000000000b
2:0	**RESERVED**	R/O	000b

5.15 Under-Voltage/Over-Voltage Detection Registers

5.15.1 UNDER AND OVER VOLTAGE CONTROL REGISTER

CL45 Address: 0x1E Register Address: 0xF220 Size: 16 bits

Register Name: UVOV_CTL

Bits	Description	Type	Default
15:2	**RESERVED**	R/O	0000h
1	**Over-Voltage Enable** This bit enables over voltage detection. This bit should be set only after all over voltage registers have been configured	R/W	000000000b
0	**Under-Voltage Enable** This bit enables under voltage detection. This bit should be set only after all under voltage registers have been configured	R/O	000b

5.15.2 UNDER AND OVER VOLTAGE CONTROL INTERRUPT STATUS REGISTER

CL45 Address: 0x1E Register Address: 0xF221 Size: 16 bits

Register Name: UVOV_INT_STS

Bits	Description	Type	Default
15:3	**RESERVED**	R/O	0000b
2	**Over-Voltage Interrupt Status**	R/O	0000b
1	**Under-Voltage Interrupt Status**	R/O	0000b
0	**Trim Interrupt Status**	R/O	0000b

5.15.3 UNDER AND OVER VOLTAGE INTERRUPT ENABLE REGISTER

CL45 Address: 0x1E Register Address: 0xF222 Size: 16 bits

Register Name: UVOV_INT_EN

Bits	Description	Type	Default
15:3	**RESERVED**	R/O	0000b
2	**Over-Voltage Interrupt Enable** When set the respective interrupt is enabled. This bit is cleared by the corresponding interrupt disable bit.	R/W	0000b

1	**Under-Voltage Interrupt Enable** When set the respective interrupt is enabled. This bit is cleared by the corresponding interrupt disable bit.	R/W	0000b
0	**Trim Interrupt Enable** When set the respective interrupt is enabled. This bit is cleared by the corresponding interrupt disable bit.	R/W	0000b

5.15.4 UNDER AND OVER VOLTAGE CONFIGURATION 0 REGISTER - VDDRGMII - LAN8870/ LAN8871 ONLY

CL45 Address: 0x1E Register Address: 0xF224 Size: 16 bits

Register Name: UVOV_CFG0_VDDRGMII

Bits	Description	Type	Default
15:12	**RESERVED**	R/O	0000b
11	**Over-voltage Reset Enable - VDDRGMII** When set the respective over voltage detection channel can generate a system reset.	R/W	0b
10	**Under-voltage Reset Enable - VDDRGMII** When set the respective under voltage detection channel can generate a system reset.	R/W	0b
9:8	**Supply Level Detect Reference Level – VDDRGMII (suplvl_det_vddrgmii)** When suplvl_det_vddrgmii is cleared this field specifies the reference voltage to be used by UV/OV module. 00b: 1.8V 01b: 2.5V 1Xb: 3.3V	R/W	00b
7	**Supply Level Detect - VDDRGMII** When set the supply voltage is internally detected for the UV/OV module. Otherwise, the UV/OV detector will use the value specified in VDD_REF_SEL. 0b: Use value specified in VDD_REF_SEL. 1b: Use internally detected VDD. **Note:** When a value of one is written to this bit the SUPPLVL_DET input to the UV/OV module shall drive 1b for 10us.	R/W	0b
6	**Trim Enable - VDDRGMII** When set this bit enables the trimming function. This bit self clears after the trim function completes.	R/W	0b
5:4	**Over-voltage Range Select** Over-voltage range select. Where X is VDD. 00b: X-X*(5/100) 01b: X-X*(7.5/100) 10b: X-X*(10/100) 11b: X-X*(2.5/100)	R/W	01b

3:2	**Under-voltage Range Select** Under-voltage range select. Where X is VDD. 00b: X-X*(5/100) 01b: X-X*(7.5/100) 10b: X-X*(10/100) 11b: X-X*(2.5/100)	R/W	01b
1	**Over-voltage Detection Enable - VDDRGMII** This bit enables over voltage detection for this detector.	R/W	0b
0	**Under-voltage Detection Enable - VDDRGMII** This bit enables under voltage detection for this detector.	R/W	0b

5.15.5 UNDER AND OVER VOLTAGE CONFIGURATION 0 REGISTER - S_VPH - LAN8872 ONLY

CL45 Address: 0x1E Register Address: 0xF224 Size: 16 bits

Register Name: UVOV_CFG0_S_VPH

Bits	Description	Type	Default
15:12	**RESERVED**	R/O	0000b
11	**Over-voltage Reset Enable - S_VPH** When set the respective over voltage detection channel can generate a system reset.	R/W	0b
10	**Under-voltage Reset Enable - S_VPH** When set the respective under voltage detection channel can generate a system reset.	R/W	0b
9:8	**Supply Level Detect Reference Level – S_VPH (suplvl_det_svph)** When suplvl_det_svph is cleared this field specifies the reference voltage to be used by UV/OV module. 00b: 1.8V 01b: 2.5V 1Xb: RESERVED	R/W	00b
7	**Supply Level Detect - S_VPH** When set the supply voltage is internally detected for the UV/OV module. Otherwise, the UV/OV detector will use the value specified in VDD_REF_SEL. 0b: Use value specified in VDD_REF_SEL. 1b: Use internally detected VDD. **Note:** When a value of one is written to this bit the SUPPLVL_DET input to the UV/OV module shall drive 1b for 10us.	R/W	0b
6	**Trim Enable - S_VPH** When set this bit enables the trimming function. This bit self clears after the trim function completes.	R/W	0b

5:4	**Over-voltage Range Select** Over-voltage range select. Where X is VDD. 00b: X-X*(5/100) 01b: X-X*(7.5/100) 10b: X-X*(10/100) 11b: X-X*(2.5/100)	R/W	01b
3:2	**Under-voltage Range Select** Under-voltage range select. Where X is VDD. 00b: X-X*(5/100) 01b: X-X*(7.5/100) 10b: X-X*(10/100) 11b: X-X*(2.5/100)	R/W	01b
1	**Over-voltage Detection Enable - S_VPH** This bit enables over voltage detection for this detector.	R/W	0b
0	**Under-voltage Detection Enable - S_VPH** This bit enables under voltage detection for this detector.	R/W	0b

5.15.6 UNDER AND OVER VOLTAGE CONFIGURATION 0 REGISTER - VDDIO

CL45 Address: 0x1E Register Address: 0xF225 Size: 16 bits

Register Name: UVOV_CFG0_VDDIO

Bits	Description	Type	Default
15:12	**RESERVED**	R/O	0000b
11	**Over-voltage Reset Enable - VDDIO** When set the respective over voltage detection channel can generate a system reset.	R/W	0b
10	**Under-voltage Reset Enable - VDDIO** When set the respective under voltage detection channel can generate a system reset.	R/W	0b
9:8	**Supply Level Detect Reference Level – VDDIO (suplvl_det_vddio)** When suplvl_det_vddio is cleared this field specifies the reference voltage to be used by UV/OV module. 00b: 1.8V 01b: 2.5V 1Xb: 3.3V (Note 5-1) **Note 5-1** 1Xb is RESERVED in LAN8872	R/W	00b

7	**Supply Level Detect - VDDIO** When set the supply voltage is internally detected for the UV/OV module. Otherwise, the UV/OV detector will use the value specified in VDD_REF_SEL. 0b: Use value specified in VDD_REF_SEL. 1b: Use internally detected VDD. When a value of one is written to this bit the SUPPLVL_DET input to the UV/OV module shall drive 1b for 10us.	R/W	0b
6	**Trim Enable - VDDIO** When set this bit enables the trimming function. This bit self clears after the trim function completes.	R/W	0b
5:4	**Over-voltage Range Select** Over-voltage range select. Where X is VDD. 00b: X-X*(5/100) 01b: X-X*(7.5/100) 10b: X-X*(10/100) 11b: X-X*(2.5/100)	R/W	01b
3:2	**Under-voltage Range Select** Under-voltage range select. Where X is VDD. 00b: X-X*(5/100) 01b: X-X*(7.5/100) 10b: X-X*(10/100) 11b: X-X*(2.5/100)	R/W	01b
1	**Over-voltage Detection Enable - VDDIO** This bit enables over voltage detection for this detector.	R/W	0b
0	**Under-voltage Detection Enable - VDDIO** This bit enables under voltage detection for this detector.	R/W	0b

5.15.7 UNDER AND OVER VOLTAGE CONFIGURATION 0 REGISTER - VDDA

CL45 Address: 0x1E Register Address: 0xF226 Size: 16 bits

Register Name: UVOV_CFG0_VDDA

Bits	Description	Type	Default
15:12	**RESERVED**	R/O	0000b
11	**Over-voltage Reset Enable - VDDA** When set the respective over voltage detection channel can generate a system reset.	R/W	0b
10	**Under-voltage Reset Enable - VDDA** When set the respective under voltage detection channel can generate a system reset.	R/W	0b

9:8	**Supply Level Detect Reference Level – VDDA (suplvl_det_vdda)** When suplvl_det_vdda is cleared this field specifies the reference voltage to be used by UV/OV module. 00b: 1.8V 01b: 2.5V 1Xb: 3.3V (Note 5-2) **Note 5-2** 1Xb is RESERVED in LAN8872	R/W	00b
7	**Supply Level Detect - VDDA** When set the supply voltage is internally detected for the UV/OV module. Otherwise, the UV/OV detector will use the value specified in VDD_REF_SEL. 0b: Use value specified in VDD_REF_SEL. 1b: Use internally detected VDD. When a value of one is written to this bit the SUPPLVL_DET input to the UV/OV module shall drive 1b for 10us.	R/W	0b
6	**Trim Enable - VDDA** When set this bit enables the trimming function. This bit self clears after the trim function completes.	R/W	0b
5:4	**Over-voltage Range Select** Over-voltage range select. Where X is VDD. 00b: X-X*(5/100) 01b: X-X*(7.5/100) 10b: X-X*(10/100) 11b: X-X*(2.5/100)	R/W	01b
3:2	**Under-voltage Range Select** Under-voltage range select. Where X is VDD. 00b: X-X*(5/100) 01b: X-X*(7.5/100) 10b: X-X*(10/100) 11b: X-X*(2.5/100)	R/W	01b
1	**Over-voltage Detection Enable - VDDA** This bit enables over voltage detection for this detector.	R/W	0b
0	**Under-voltage Detection Enable - VDDA** This bit enables under voltage detection for this detector.	R/W	0b

5.15.8 UNDER AND OVER VOLTAGE CONFIGURATION 0 REGISTER - VDD11

CL45 Address: 0x1E Register Address: 0xF227 Size: 16 bits

Register Name: UVOV_CFG0_VDD11

Bits	Description	Type	Default
15:12	**RESERVED**	R/O	0000b
11	**Over-voltage Reset Enable - VDD11** When set the respective over voltage detection channel can generate a system reset.	R/W	0b
10	**Under-voltage Reset Enable - VDD11** When set the respective under voltage detection channel can generate a system reset.	R/W	0b
9:8	**Supply Level Detect Reference Level – VDD11 (suplvl_det_vdd11)** When suplvl_det_vdd11 is cleared this field specifies the reference voltage to be used by UV/OV module. 00b: 1.8V 01b: 2.5V 1Xb: 3.3V (Note 5-3) **Note 5-3** 1Xb is RESERVED in LAN8872	R/W	00b
7	**Supply Level Detect - VDD11** When set the supply voltage is internally detected for the UV/OV module. Otherwise, the UV/OV detector will use the value specified in VDD_REF_SEL. 0b: Use value specified in VDD_REF_SEL. 1b: Use internally detected VDD. When a value of one is written to this bit the SUPPLVL_DET input to the UV/OV module shall drive 1b for 10us.	R/W	0b
6	**Trim Enable - VDD11** When set this bit enables the trimming function. This bit self clears after the trim function completes.	R/W	0b
5:4	**Over-voltage Range Select** Over-voltage range select. Where X is VDD. 00b: X-X*(5/100) 01b: X-X*(7.5/100) 10b: X-X*(10/100) 11b: X-X*(2.5/100)	R/W	01b
3:2	**Under-voltage Range Select** Under-voltage range select. Where X is VDD. 00b: X-X*(5/100) 01b: X-X*(7.5/100) 10b: X-X*(10/100) 11b: X-X*(2.5/100)	R/W	01b

1	**Over-voltage Detection Enable - VDD11** This bit enables over voltage detection for this detector.	R/W	0b
0	**Under-voltage Detection Enable - VDD11** This bit enables under voltage detection for this detector.	R/W	0b

5.15.9 UNDER AND OVER VOLTAGE CONFIGURATION 1 REGISTER - VDDRGMII - LAN8870/ LAN8871 ONLY

CL45 Address: 0x1E Register Address: 0xF228 Size: 16 bits

Register Name: UVOV_CFG1_VDDRGMII

Bits	Description	Type	Default
15	**RESERVED**	R/O	0b
14:12	**Temperature Tune - VDDRGMII** Temperature trim tune input for VDDRGMII	R/W	000b
11:6	**Magnitude Tune – VDDRGMII** Magnitude trim tune input for VDDRGMII	R/W	000000b
5:0	**Trim Magnitude Tune - VDDRGMII** This field is used to report the result of the trim sequence. When Trim Enable in Register 1E.F224 is asserted, the value in this register is used by the internal HW FSM as the starting point for the trim sequence. This value is decremented automatically until the UV output of this UVOV module toggles. After the trim process completes the new value is loaded into this register. The Trim Enable bit then self clears and the respective interrupt asserts.	R/W	111111b

5.15.10 UNDER AND OVER VOLTAGE CONFIGURATION 1 REGISTER - S_VPH - LAN8872 ONLY

CL45 Address: 0x1E Register Address: 0xF228 Size: 16 bits

Register Name: UVOV_CFG1_S_VPH

Bits	Description	Type	Default
15	**RESERVED**	R/O	0b
14:12	**Temperature Tune - S_VPH** Temperature trim tune input for S_VPH	R/W	000b
11:6	**Magnitude Tune – S_VPH** Magnitude trim tune input for S_VPH	R/W	000000b

5:0	**Trim Magnitude Tune - S_VPH** This field is used to report the result of the trim sequence. When Trim Enable in Register 1E.F224 is asserted, the value in this register is used by the internal HW FSM as the starting point for the trim sequence. This value is decremented automatically until the UV output of this UVOV module toggles. After the trim process completes the new value is loaded into this register. The Trim Enable bit then self clears and the respective interrupt asserts.	R/W	111111b

5.15.11 UNDER AND OVER VOLTAGE CONFIGURATION 1 REGISTER - VDDIO

CL45 Address: 0x1E Register Address: 0xF229 Size: 16 bits

Register Name: UVOV_CFG1_VDDIO

Bits	Description	Type	Default
15	**RESERVED**	R/O	0b
14:12	**Temperature Tune - VDDIO** Temperature trim tune input for VDDIO	R/W	000b
11:6	**Magnitude Tune – VDDIO** Magnitude trim tune input for VDDIO	R/W	000000b
5:0	**Trim Magnitude Tune - VDDIO** This field is used to report the result of the trim sequence. When Trim Enable in Register 1E.F225 is asserted, the value in this register is used by the internal HW FSM as the starting point for the trim sequence. This value is decremented automatically until the UV output of this UVOV module toggles. After the trim process completes the new value is loaded into this register. The Trim Enable bit then self clears and the respective interrupt asserts.	R/W	111111b

5.15.12 UNDER AND OVER VOLTAGE CONFIGURATION 1 REGISTER - VDDA

CL45 Address: 0x1E Register Address: 0xF22A Size: 16 bits

Register Name: UVOV_CFG1_VDDA

Bits	Description	Type	Default
15	**RESERVED**	R/O	0b
14:12	**Temperature Tune - VDDA** Temperature trim tune input for VDD1A	R/W	000b
11:6	**Magnitude Tune – VDDA** Magnitude trim tune input for VDDA	R/W	000000b

5:0	**Trim Magnitude Tune – VDDA** This field is used to report the result of the trim sequence. When Trim Enable in Register 1E.F226 is asserted, the value in this register is used by the internal HW FSM as the starting point for the trim sequence. This value is decremented automatically until the UV output of this UVOV module toggles. After the trim process completes the new value is loaded into this register. The Trim Enable bit then self clears and the respective interrupt asserts.	R/W	111111b

5.15.13 UNDER AND OVER VOLTAGE CONFIGURATION 1 REGISTER - VDD11

CL45 Address: 0x1E Register Address: 0xF22B Size: 16 bits

Register Name: UVOV_CFG1_VDD11

Bits	Description	Type	Default
15	**RESERVED**	R/O	0b
14:12	**Temperature Tune – VDD11** Temperature trim tune input for VDD11	R/W	000b
11:6	**Magnitude Tune – VDD11** Magnitude trim tune input for VDD11	R/W	000000b
5:0	**Trim Magnitude Tune – VDD11** This field is used to report the result of the trim sequence. When Trim Enable in Register 1E.F227 is asserted, the value in this register is used by the internal HW FSM as the starting point for the trim sequence. This value is decremented automatically until the UV output of this UVOV module toggles. After the trim process completes the new value is loaded into this register. The Trim Enable bit then self clears and the respective interrupt asserts.	R/W	111111b

5.15.14 UNDER AND OVER VOLTAGE CONFIGURATION 2 REGISTER - VDDRGMII - LAN8870/ LAN8871 ONLY

CL45 Address: 0x1E Register Address: 0xF22C Size: 16 bits

Register Name: UVOV_CFG2_VDDRGMII

Bits	Description	Type	Default
15:8	**UVOV Debouncer Value – VDDRGMII** Specifies the debounce value used or UV and OV channels that have debounce enabled. This register has units of 8 ns. A value of 0h disables the debouncer.	R/W	11111111b
7:4	**RESERVED**	R/O	0000b

3	**3.3V UVOV Status - VDDRGMII** Provides the real time status of the UVOV detector's 3.3V output signal.	R/O	0b
2	**2.5V UVOV Status - VDDRGMII** Provides the real time status of the UVOV detector's 2.5V output signal.	R/O	0b
1	**Over-voltage Status - VDDRGMII** Provides the real time status of the UVOV detectors OV_CR output signal.	R/O	0b
0	**Under-voltage Status - VDDRGMII** Provides the real time status of the UVOV detectors OV_CR output signal.	R/O	0b

5.15.15 UNDER AND OVER VOLTAGE CONFIGURATION 2 REGISTER - S_VPH - LAN8872 ONLY

CL45 Address: 0x1E Register Address: 0xF22C Size: 16 bits

Register Name: UVOV_CFG2_S_VPH

Bits	Description	Type	Default
15:8	**UVOV Debouncer Value – S_VPH** Specifies the debounce value used or UV and OV channels that have debounce enabled. This register has units of 8 ns. A value of 0h disables the debouncer.	R/W	11111111b
7:3	**RESERVED**	R/O	00000b
2	**2.5V UVOV Status - S_VPH** Provides the real time status of the UVOV detector's 2.5V output signal.	R/O	0b
1	**Over-voltage Status - S_VPH** Provides the real time status of the UVOV detectors OV_CR output signal.	R/O	0b
0	**Under-voltage Status - S_VPH** Provides the real time status of the UVOV detectors OV_CR output signal.	R/O	0b

5.15.16 UNDER AND OVER VOLTAGE CONFIGURATION 2 REGISTER - VDDIO

CL45 Address: 0x1E Register Address: 0xF22D Size: 16 bits

Register Name: UVOV_CFG2_VDDIO

Bits	Description	Type	Default
15:8	**UVOV Debouncer Value – VDDIO** Specifies the debounce value used or UV and OV channels that have debounce enabled. This register has units of 8 ns. A value of 0h disables the debouncer.	R/W	11111111b
7:4	**RESERVED**	R/O	0000b
3	**3.3V UVOV Status - VDDIO** Provides the real time status of the UVOV detector's 3.3V output signal. **Note:** This bit is RESERVED in LAN8872, and when grouped with the bit sequence above, their default value is 00000b.	R/O	0b
2	**2.5V UVOV Status - VDDIO** Provides the real time status of the UVOV detector's 2.5V output signal.	R/O	0b
1	**Over-voltage Status - VDDIO** Provides the real time status of the UVOV detectors OV_CR output signal.	R/O	0b
0	**Under-voltage Status - VDDIO** Provides the real time status of the UVOV detectors OV_CR output signal.	R/O	0b

5.15.17 UNDER AND OVER VOLTAGE CONFIGURATION 2 REGISTER - VDDA

CL45 Address: 0x1E Register Address: 0xF22E Size: 16 bits

Register Name: UVOV_CFG2_VDDA

Bits	Description	Type	Default
15:8	**UVOV Debouncer Value – VDDA** Specifies the debounce value used or UV and OV channels that have debounce enabled. This register has units of 8 ns. A value of 0h disables the debouncer.	R/W	11111111b
7:4	**RESERVED**	R/O	0000b
3	**3.3V UVOV Status - VDDA** Provides the real time status of the UVOV detector's 3.3V output signal. **Note:** This bit is RESERVED in LAN8872, and when grouped with the bit sequence above, their default value is 00000b.	R/O	0b

2	**2.5V UVOV Status - VDDA** Provides the real time status of the UVOV detector's 2.5V output signal.	R/O	0b
1	**Over-voltage Status - VDDA** Provides the real time status of the UVOV detectors OV_CR output signal.	R/O	0b
0	**Under-voltage Status - VDDA** Provides the real time status of the UVOV detectors OV_CR output signal.	R/O	0b

5.15.18 UNDER AND OVER VOLTAGE CONFIGURATION 2 REGISTER - VDD11

CL45 Address: 0x1E Register Address: 0xF22F Size: 16 bits

Register Name: UVOV_CFG2_VDD11

Bits	Description	Type	Default
15:8	**UVOV Debouncer Value – VDD11** Specifies the debounce value used or UV and OV channels that have debounce enabled. This register has units of 8 ns. A value of 0h disables the debouncer.	R/W	11111111b
7:2	**RESERVED**	R/O	000000b
1	**Over-voltage Status – VDD11** Provides the real time status of the UVOV detectors OV_CR output signal.	R/O	0b
0	**Under-voltage Status – VDD11** Provides the real time status of the UVOV detectors OV_CR output signal.	R/O	0b

5.16 Temperature Sensor Registers

5.16.1 PVT CONTROL 1 REGISTER

CL45 Address: 0x1E Register Address: 0xF240 Size: 16 bits

Register Name: PVT_CTL1

Bits	Description	Type	Default
15	**RESERVED**	R/O	0b
14	**PVT Reset Enable** When set a Threshold2 Match will force a chip level reset on the device.	R/W	0b
13	**PVT Sleep Enable** When set a Threshold2 Match will force the device into the TC10 Sleep state.	R/W	0b

12:8	**PVT Input Trim** TRIM[4:0] input pins of the AB PVT IP.	R/W	01111b
7	**Probe VREG Enable** PROBE_VREG_ENA input pin of the AB PVT IP	R/W	0b
6:5	**VSEL Select** Selects the VIN[3:0] input, this is an input to the VSEL[1:0] input pins of the AB PVT IP.	R/W	00b
4:2	**RESERVED**	R/W	000b
1	**PVT Enable** If Select ENA=1, this is connected to the ENA input pin of the AB PVT IP	R/W	0b
0	**Select ENA** Selects if the ENA input pin to the AB PVT IP is controlled by HW or SW 0: ENA is controlled by HW 1: ENA is controlled by SW	R/W	1b

5.16.2 PVT CONTROL 2 REGISTER

CL45 Address: 0x1E Register Address: 0xF241 Size: 16 bits

Register Name: PVT_CTL2

Bits	Description	Type	Default
15:6	**RESERVED**	R/O	000h
5:0	**VTRIM Select** VTRIM[5:0] input pins of the AB PVT IP	R/W	000000b

5.16.3 PVT STATUS REGISTER

CL45 Address: 0x1E Register Address: 0xF242 Size: 16 bits

Register Name: PVT_STS

Bits	Description	Type	Default
15:5	**RESERVED**	R/O	000h
4	**Thermal Threshold2 Match** Thermal overload mode signal	R/O	0b
3	**Thermal Threshold1 Match** Thermal warning mode signal	R/O	0b
2	**Thermal Threshold0 Match** Thermal warning mode signal with hysteresis	R/O	0b

1	**Data Valid Status** PVT Data Valid status	R/O	0b
0	**ENA Status** ENA Status value	R/O	0b

5.16.4 PVT INTERRUPT STATUS REGISTER

CL45 Address: 0x1E Register Address: 0xF244 Size: 16 bits

Register Name: PVT_INT_STS

Bits	Description	Type	Default
15:5	**RESERVED**	R/O	000h
4	**Thermal Threshold2 Change Interrupt** 1 = change in Thermal Threshold2 value 0 = no change in Thermal Threshold2 value	R/O	0b
3	**Thermal Threshold1 Change Interrupt** 1 = change in Thermal Threshold1 value 0 = no change in Thermal Threshold1 value	R/O	0b
2	**Thermal Threshold0 Change Interrupt** 1 = change in Thermal Threshold0 value 0 = no change in Thermal Threshold0 value	R/O	0b
1	**Data Valid Status Change Interrupt** PVT Data Valid status change interrupt 1 = change in PVT Data Valid value 0 = no change in PVT Data Valid value	R/O	0b
0	**ENA Status Change Interrupt** 1 = change in ENA Status value 0 = no change in ENA Status value	R/O	0b

5.16.5 PVT INTERRUPT MASK REGISTER

CL45 Address: 0x1E Register Address: 0xF246 Size: 16 bits

Register Name: PVT_INT_MSK

Bits	Description	Type	Default
15:5	**RESERVED**	R/O	000h
4	**Thermal Threshold2 Change Interrupt Mask** When set to 0 generates an interrupt when Thermal Threshold2 Change Interrupt is set. When 1, this interrupt is disabled.	R/O	0b

3	**Thermal Threshold1 Change Interrupt Mask** When set to 0 generates an interrupt when Thermal Threshold1 Change Interrupt is set. When 1, this interrupt is disabled.	R/O	0b
2	**Thermal Threshold0 Change Interrupt Mask** When set to 0 generates an interrupt when Thermal Threshold0 Change Interrupt is set. When 1, this interrupt is disabled.	R/O	0b
1	**Data Valid Status Change Interrupt Mask** When set to 0 generates an interrupt when Data Valid Status Change Interrupt is set. When 1, this interrupt is disabled	R/O	0b
0	**ENA Status Change Interrupt Mask** When set to 0 generates an interrupt when ENA Status Change Interrupt is set. When 1, this interrupt is disabled	R/O	0b

5.16.6 PVT DATA REGISTER

CL45 Address: 0x1E Register Address: 0xF248 Size: 16 bits

Register Name: PVT_DATA

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	0
9:0	**PVT Data** The last sensed value from the DATA_OUT[9:0] pins of the AB PVT IP	R/O	000h

5.16.7 PVT SAMPLE TIME REGISTER

CL45 Address: 0x1E Register Address: 0xF24A Size: 16 bits

Register Name: PVT_SAMP_TIME

Bits	Description	Type	Default
15:0	**Sample Time** Time between samples taken from the AB PVT IP. 0000h = HW takes a sample whenever DATA_VALID is asserted 0001h-FFFFh: sample time in ms	R/O	0000h

5.16.8 PVT THERMAL COMPARATOR CONTROL REGISTER

CL45 Address: 0x1E Register Address: 0xF24C Size: 16 bits

Register Name: PVT_THERM_COMP_CTL

Bits	Description	Type	Default
15:2	**RESERVED**	R/O	0000h
1:0	**Thermal Comparator Control** This field controls the Thermal Comparator. It is sampled every 100 us. 00 = Comparator is disabled 01 = Comparator is enabled 10 = RESERVED 11 = RESERVED	R/W	00b

5.16.9 PVT THERMAL COMPARATOR THRESHOLD0 REGISTER

CL45 Address: 0x1E Register Address: 0xF24E Size: 16 bits

Register Name: PVT_THERM_COMP_THR0

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	000000b
9:0	**Thermal Comparator Threshold0** Comparator threshold 0 value, units are VDDA/1024.	R/W	000h

5.16.10 PVT THERMAL COMPARATOR THRESHOLD1 REGISTER

CL45 Address: 0x1E Register Address: 0xF250 Size: 16 bits

Register Name: PVT_THERM_COMP_THR1

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	000000b
9:0	**Thermal Comparator Threshold1** Comparator threshold 1 value, units are VDDA/1024.	R/W	000h

5.16.11 PVT THERMAL COMPARATOR THRESHOLD2 REGISTER

CL45 Address: 0x1E Register Address: 0xF252 Size: 16 bits

Register Name: PVT_THERM_COMP_THR2

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	000000b
9:0	**Thermal Comparator Threshold2** Comparator threshold 2 value, units are VDDA/1024.	R/W	000h

5.16.12 PVT SAMPLE CLOCK DIVIDER REGISTER

CL45 Address: 0x1E Register Address: 0xF254 Size: 16 bits

Register Name: PVT_SAMP_CLK_DIV

Bits	Description	Type	Default
15:0	**Sample Clock Divider** This register is used with the AB PVT Clock Divider Register to generate the 1 kHz AB PVT sampling clock. SAMPLE_CLK_DIV provides the divisor value to divide the 1.15-1.25 MHz AB PVT clock down to 1 kHz. Value is set based on frequency of AB PVT sampling clock, as follows. AB PVT sampling clock = 1.15 MHz, SAMPLE_CLK_DIV = d1150 (047Eh).	R/W	04B0h

5.16.13 PVT VOLTAGE SELECT REGISTER

CL45 Address: 0x1E Register Address: 0xF256 Size: 16 bits

Register Name: PVT_PSEL25

Bits	Description	Type	Default
15:10	**RESERVED**	R/O	0000h
9:0	**PVT Select Voltage** Controls whether the AB PVT IP runs from 2.5V or 3.3V. The default is 3.3V, set this bit to 1 if VDDAH is connected to 2.5V.	R/W	000h

5.16.14 PVT HARD RESET REGISTER

CL45 Address: 0x1E Register Address: 0xF257 Size: 16 bits

Register Name: PVT_HARD_RST

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	0000h
0	**PVT Hard Reset** 1 = Reset the AB PVT and set all configuration registers to their default state. Writing a zero has no effect.	R/W	0b

5.16.15 PVT SOFT RESET REGISTER

CL45 Address: 0x1E Register Address: 0xF258 Size: 16 bits

Register Name: PVT_SOFT_RST

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	0000h
0	**PVT Soft Reset** 1 = Reset the AB PVT except all configuration registers Writing a zero has no effect	R/W	0b

5.16.16 PVT CLOCK DIVIDER REGISTER

CL45 Address: 0x1E Register Address: 0xF259 Size: 16 bits

Register Name: PVT_CLK_DIVIDER

Bits	Description	Type	Default
15:1	**RESERVED**	R/O	00000000b
0	**PVT Clock Divider** Value is set based on desired value of AB PVT sampling clock, as follows. For 200 MHz system clock: PVT_CLK_DIV = 'd160 (A0h) results in AB PVT clock frequency of 1.25 MHz PVT_CLK_DIV = 'd167 (A7h) results in AB PVT clock frequency of 1.2 MHz approx (1.197M in exact) PVT_CLK_DIV = 'd173 (ADh) results in AB PVT clock frequency of 1.156 MHz	R/W	10100111b

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005483A (06-24-24)	Initial release	

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