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Supporting 100BASE-FX Fiber Media for Microchip's Ethernet Controller, Switch and EtherCAT Controller

Author: *Anant Dalimkar*
Microchip Technology, Inc.

INTRODUCTION

Microchip provides design solutions targeted to support next generation Ethernet switches, EtherCAT® industrial controllers and a 10/100 Industrial Ethernet MAC/PHY controllers. The Ethernet switch products are divided into host bus and MII categories with the host bus versions supporting a full featured Ethernet MAC residing behind the switch fabric. The non-host bus versions support various MII, RMII and Turbo MII options with 1 and 2 port options.

The following table lists the various products available.

Part Number	Description
LAN9250	10/100 Industrial Ethernet Controller & PHY
LAN9252	2/3-Port EtherCAT Slave Controller with Integrated Ethernet PHYs
LAN9352	2-Port 10/100 Managed Ethernet Switch with 16-Bit Non-PCI CPU Interface
LAN9353	3-Port 10/100 Managed Ethernet Switch with Single MII/Turbo MII or Dual RMII
LAN9354	3-Port 10/100 Managed Ethernet Switch with Single RMII
LAN9355	3-Port 10/100 Managed Ethernet Switch with Dual MII/RMII/Turbo MII

This document will highlight the design differences needed to implement 100BASE-FX fiber media on Microchips' Ethernet Controller, Switch and EtherCAT Controller.

This document includes the following topics:

- Feature Differences for 100BASE-FX on page 3
- EtherCAT Over Optical Links (FX) — Applicable Only for LAN9252 on page 9

Audience

The target audiences for this document are hardware design engineers and managers using Microchips' Ethernet Controller, Switch and EtherCAT Controller in a 100BASE-FX application.

References

The following documents should be referenced when using this application note. See your Microchip representative for availability.

- LAN9250 Datasheet
- LAN9252 Datasheet
- LAN9352/LAN9354/LAN9355 Datasheet
- LAN9355 Datasheet

Terms and Abbreviations

- MII - Media Independent Interface
- RMII - Reduced Media Independent Interface
- EEE - Energy-Efficient Ethernet
- SFF - Small Form Factor
- SFP - Small Form Factor Pluggable
- SMI - Serial Management Interface
- MAC - Media Access Control
- PHY - Physical layer device
- EEE - Energy Efficient Ethernet

FEATURE DIFFERENCES FOR 100BASE-FX

This section describes the hardware and software differences for a designer to implement the new 100BASE-FX fiber media in Microchip's Ethernet Controller, Switch and EtherCAT Controller.

Hardware Details

100BASE-FX support via external fiber transceiver.

When set for 100BASE-FX operation, the scrambler and MTL-3 blocks are disable and the analog RX and TX pins are changed to differential LVPECL pins and connect through external terminations to the external Fiber transceiver. The differential LVPECL pins support a signal voltage range compatible with SFF (LVPECL) and SFP (reduced LVPECL) type transceivers.

While in 100BASE-FX operation, the quality of the receive signal is provided by the external transceiver as either an open-drain, CMOS level, Loss of Signal (SFP) or a LVPECL Signal Detect (SFF).

100BASE-FX ENABLE AND LOS/SD SELECTION

100BASE-FX operation is enabled by the use of the FX mode straps (fx_mode_strap_1 and fx_mode_strap_2) and is reflected in the 100BASE-FX Mode (FX_MODE) bit in the PHY x Special Modes Register (PHY_SPECIAL_MODES_x).

Loss of Signal mode is selected for both PHYs by the three level FXLOSEN strap input pin. The three levels correspond to Loss of Signal mode for a) neither PHY (less than 1 V (typ.)), b) PHY A (greater such as than 1 V (typ.) but less than 2 V (typ.)) or c) both PHYs [greater than 2 V (typ.)]. It is not possible to select Loss of Signal mode for only PHY B.

If Loss of Signal mode is not selected, then Signal Detect mode is selected, independently, by the FXSDENA or FXSDENB strap input pin. When greater than 1 V (typ.), Signal Detect mode is enabled, when less than 1 V (typ.), copper twisted pair is enabled.

Note:	The FXSDENA strap input pin is shared with the FXSDA pin and the FXSDENB strap input pin is shared with the FXSDB pin. As such, the LVPECL levels ensure that the input is greater than 1 V (typ.) and that Signal Detect mode is selected. When TP copper is desired, the Signal Detect input function is not required and the pin should be set to 0 V.

Care must be taken such that an non-powered or disabled transceiver does not load the Signal Detect input below the valid LVPECL level.

TABLE 1: 100BASE-FX LOS, SD AND TP COPPER SELECTION PHY A

FLXLOSEN	FXSDENA	PHY Mode
<1 V (typ.)	<1 V (typ.)	TP copper
	>1 V (typ.)	100BASE-FX Signal Detect (SFF)
>1 V (typ.)	NA	100BASE-FX LOS (SFP)

TABLE 2: 100BASE-FX LOS, SD AND TP COPPER SELECTION PHY B

FLXLOSEN	FXSDENA	PHY Mode
<1 V (typ.)	<1 V (typ.)	TP copper
	>1 V (typ.)	100BASE-FX Signal Detect (SFF)
>2 V (typ.)	NA	100BASE-FX LOS (SFP)

Signal Detection (SD)

Signal Detection (SD), which requires single-ended 3.3V LVPECL levels and support the Small Form Factor (SFF) optical Module. Signal detect is use to determine the Normal operation, optical signaling detected.

SD is a logical complement of Loss of Signal (LOS).

- Single Ended LVPECL
  - SD> VLVPECL_COMMON_MODE - Normal Operation, Optical signaling detected
  - SD <VLVPECL_COMMON_MODE - No optical signal detected
- 50Ω Single-ended Impedance

Loss of Signal (LOS)

Loss of Sync (LOS) which requires CMOS levels and supports the Small Form-Factor Pluggable (SFP) optical module. LOS is an Open Drain/Collector. LOS is a logical complement of Signal Detect (SD).

- LOS<0.8V Normal Operation - Optical signaling detected
- LOS>2.0V No optical signal detected

LOS (Loss of signal) is an Open Drain/Collector output, which should be pulled up with a 4.7K-10K resistor.

CONNECTION TO 100BASE-FX FIBER MODULE

The FX mode enables the 10/100Mbps Ethernet PHY transport data over fiber optics medium using Fiber Optics Transceivers (FOT). The FX mode supports two form factors running at 100Mbps. The Small Form Factor (SFF) module can be configured using an AC or DC coupled channel while the Small Form Factor Pluggable (SFP) module can only be configured in an AC coupled channel.

SFF:

- DC/AC Coupled
  - 100Ω equivalent TX/RX termination

SFP:

- AC Coupled
  - 100Ω TX/RX termination

The FX mode transceivers incorporate an LVPECL differential driver to transmit the 4b5b encoded data, while the receiver supports both LVDS and LVPECL signal levels.

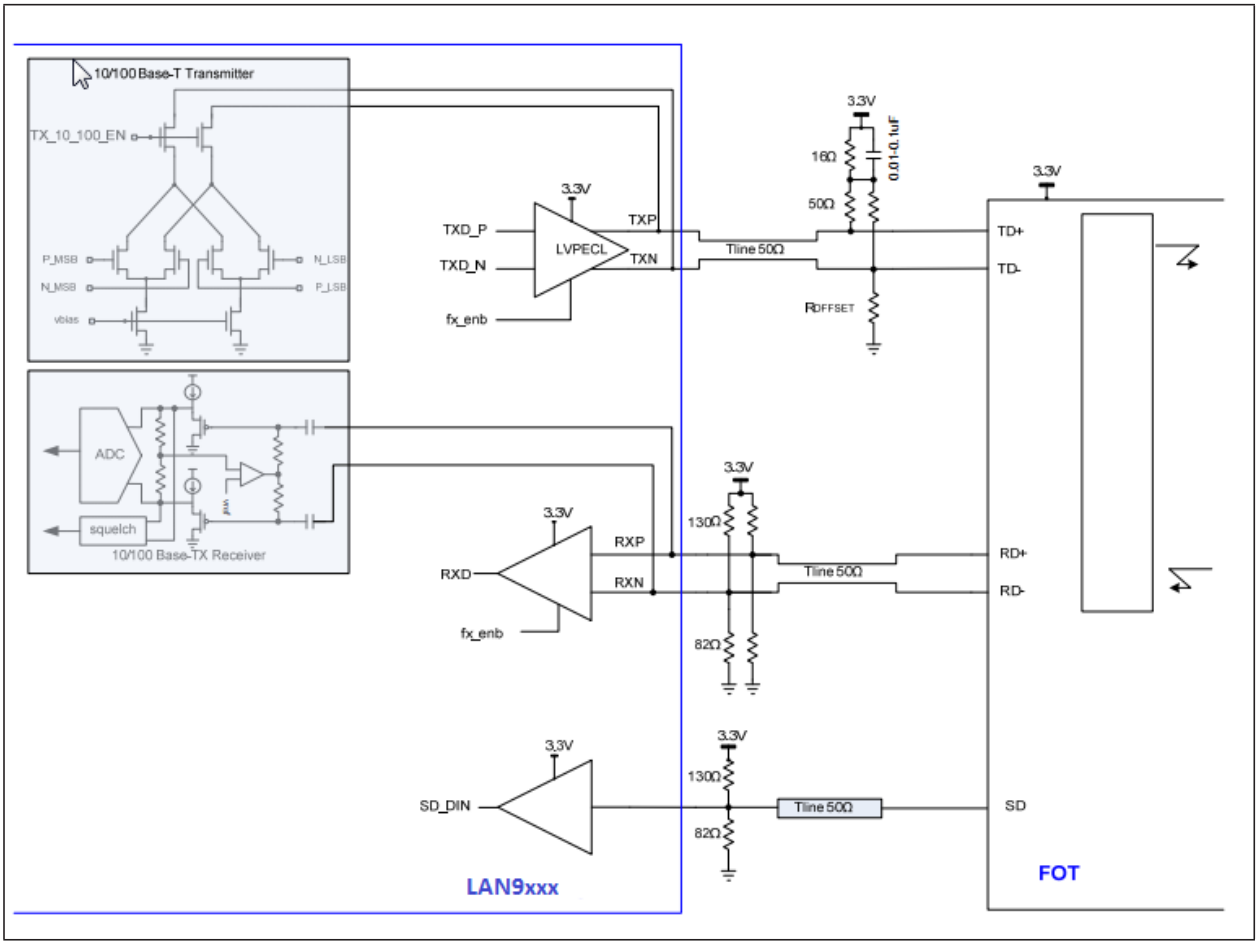
The following block diagrams show a common interface between the 10/100Mbps Ethernet PHY and the FOT for various configurations.

DC COUPLED (SFF MODULE)

Note: DC coupling is recommended for 3.3V FOT modules.

The Jutland FX mode LVPECL output driver always requires a 50Ω termination. An additional 16Ω is required to set the proper common mode voltage for the FOT. This configuration works only for 3.3V FOT. If the PHY is required to interface with 5V FOT, the value of the resistor that sets the common mode voltage must change. It is recommended to use DC coupling for 3.3V FOTs. It is also a good practice to place the 50Ω termination resistor as close to the FOT as possible to minimize noise due to reflection. The Jutland FX mode receiver incorporates the 50Ω termination resistor external to the PHY to reduce on chip power and have flexibility on the value of the termination resistors to be used with AC coupled channels. If offset is required on the transmitter path, resistor ROFFSET can be added from the TXN pad to ground. The value of the resistor is determined by the amount of offset required. Signal detect is almost always DC coupled, and requires a 50Ω impedance with a 1.3V common-mode voltage.

FIGURE 1: 100BASE-FX DC COUPLED CONFIGURATION (SFF MODE)

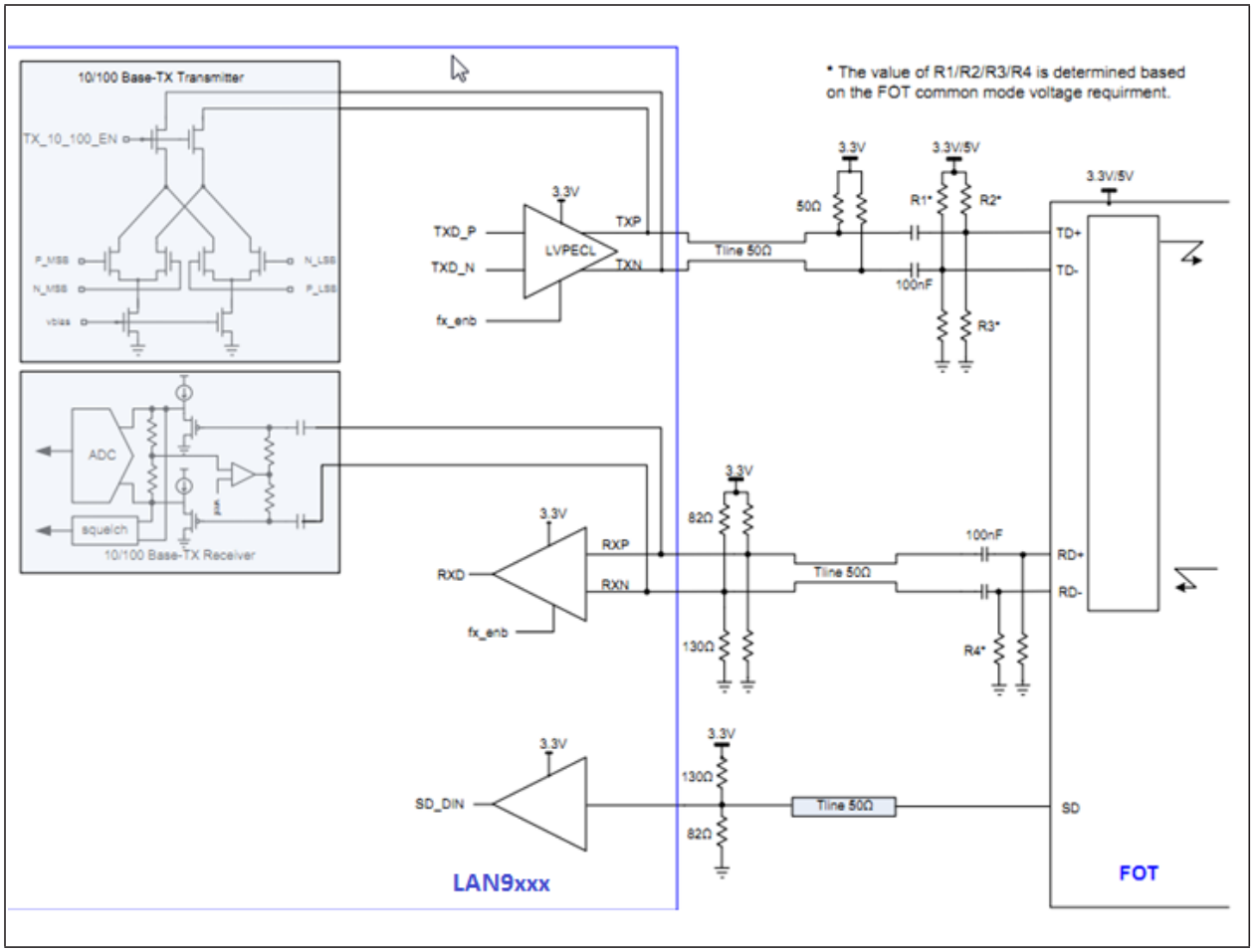


AC COUPLED (SFF MODULE)

Note: AC coupling is recommended for 5V FOT modules.

The Jutland FX mode LVPECL output driver always requires a 50Ω external termination. It is a good practice to place the 50Ω termination resistor as close to the FOT as possible to minimize noise due to reflection. The common mode voltage of the receiver is set to be the same as LVPECL common mode voltage (VDD-1.3V). If offset is required on the transmitter path, increase or decrease the pull up resistor at TD- as compared to the pull up resistor at TD+. The value of the mismatch between the pull up resistors is determined by the amount of offset required by the FOT. If zero offset is required, the value of the two pull up resistors, R1* & R2*, at TD+ and TD- are equal. Signal detect should be DC coupled and include a 50Ω termination set to a common-mode voltage of 1.3V.

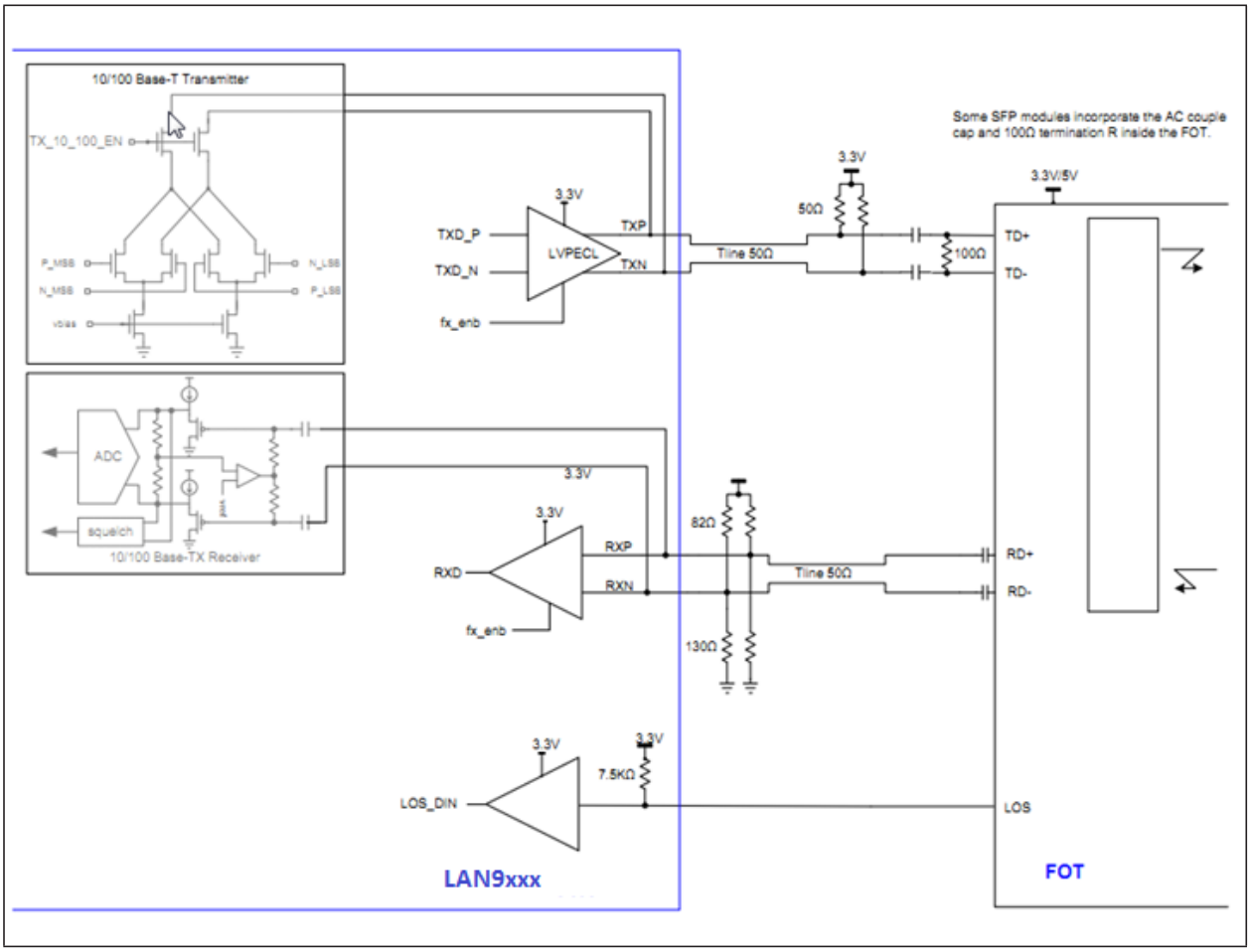
FIGURE 2: 100BASE-FX AC COUPLED CONFIGURATION (SFF MODE)



AC COUPLED (SFP MODULE)

The SFP module operates in a reduced LVPECL signaling level due to the AC couple nature of the channel and the 100Ω termination resistor embedded within the FOT module. The AC couple capacitor may or may not be embedded within the FOT module. The LVPECL transmitted data signal level will get reduced by half at the FOT input (TD+/-) due to the additional 100Ω termination. On the receive side, the 82Ω/130Ω off chip termination resistors sets the 50Ω termination as well as the common mode voltage for the receiver. Jutland receiver requires the 50Ω termination resistors to be placed as close to the Jutland PHY as possible to minimize noise due to reflection. Signal detect should be DC coupled and include a 50Ω termination set to a common-mode voltage of 1.3V.

FIGURE 3: 100BASE-FX AC COUPLED CONFIGURATION (SFP MODE)



Register Settings

The Physical PHYs comply with the IEEE 802.3 Physical Layer for Twisted Pair Ethernet and can be configured for full/half duplex 100 Mbps (100BASE-TX / 100BASE-FX) or 10 Mbps (10BASE-T) Ethernet operation. All PHY registers follow the IEEE 802.3 (clause 22.2.4) specified MII management register set and are fully configurable.

100BASE-FX operation is enabled by the use of the FX mode straps (fx_mode_strap_1 and fx_mode_strap_2) and is reflected in the 100BASE-FX Mode (FX_MODE) bit in the PHY x Special Modes Register (PHY_SPECIAL_MODES_x).

Fiber Optical Modules

Several Fiber optical modules may be used with an Ethernet PHY that supports 100Base-FX (IEEE 802.3u):

Small Form Factor (SFF) Transceiver

- AFBR-59E4APZ - Avago Technologies
- (New 2x5 DIP style Package)

- Differential LVPECL - TX, RX
- Single Ended LVPECL - Signal Detect (SD)
- 3.3V Supply
- Supported DC Coupling only

FIGURE 4: SMALL FORM FACTOR (SFF) TRANSCEIVER

Small Form-factor Pluggable (SFP) Transceiver

- FTLF1318P2xCL - Finisar Corporation
- Reduced LVPECL - TX, RX
- Open Drain/Collector - Loss of Signal
- 3.3V Supply
- Supported AC Coupling only

FIGURE 5: SMALL FORM FACTOR PLUGGABLE (SFP) TRANSCEIVER

Operational Controls and Indications

SUPPORTED FEATURES FOR 100BASE-FX

Because the 100BASE-FX mode uses 100BASE-T resources, its operational controls and indications are those of the 100BASE-T mode, such as LEDs, link status indication, and loopback modes.

- LED Indication - Any LED that supported 100BASE-TX will now support 100BASE-FX indication
- Link Status - For Link Status Indication, the Link Status bit Register 1.2 will indicate if a link is present for 100BASE-FX

FEATURES NOT SUPPORTED FOR 100BASE-FX

Feature not supported in FX mode includes Auto negotiation, AMDIX, TDR, EDPD, and EEE features.

ETHERCAT OVER OPTICAL LINKS (FX) — APPLICABLE ONLY FOR LAN9252

EtherCAT communication over optical links using Ethernet PHYs is possible, but some requirements of EtherCAT have to be respected, and some characteristics of EtherCAT slave controllers have to be considered.

The intention of this chapter is to share current knowledge about FX operation with EtherCAT.

Link Partner Notification and Loop Closing

The main principle of operation in case of link errors is disabling unreliable links by closing loops. This is automatically performed by the ESCs. The ESCs rely on the LINK_MII signal from the PHYs for detecting the link state.

With FX PHYs, it could happen that the Transceiver device is powered, while the PHY (and/or the ESC) is not active. The communication partner would detect a signal, causing him to open the link. All frames will get lost because the PHY (or the ESC) is not operating.

So at least the following two requirements have to be fulfilled, otherwise frames will be lost:

- ESC in reset state → Transceiver disabled
- PHY in reset state → Transceiver disabled

The recommended solution for this issue is to enable the Transceiver with the PHY's reset signal. If the transceiver has no suitable input, the power supply of the Transceiver can be switched off. Since the PHY's reset should be controlled by the ESC's reset output (delayed, see later), the Transceiver will power down while the PHY is in the reset state and also while the ESC is in the reset state. Thus, the ESC and the PHY will be active when the Transceiver gets active, and no frames are lost.

FAR-END-FAULT (FEF) INDICATION

LAN9252 offer a feature called Far-End-Fault generation/detection. The intention is to inform the link partner of a bad link.

The FEF feature is advantageous for EtherCAT, because the PHYs will only indicate a link when the signal quality is high enough. Without FEF, the EtherCAT slave controllers have to rely on the Enhanced Link detection feature for detecting a low quality link.

Nevertheless, Enhanced Link detection becomes active only after the link is already established, thus, in case of a low quality link, the link status will be toggling on/off (link up → Enhanced link detection tears down link → link up …). This is sufficient to locate an issue in the network, but it might disturb operation of the remaining network.

So, it is highly recommended to use PHYs which fully implement FEF generation and detection.

Standard Link Detection

The Enhanced link detection restarts auto-negotiation between the PHYs if a certain level of receive errors is reached. With FX PHYs, auto-negotiation is not available (it is a 100Base-TX feature). Typically, PHYs ignore the restart auto-negotiation request. As a consequence, the EtherCAT slave controller waits endlessly for the link to go down. Other PHYs might get into a dead-lock, because auto-negotiation is enabled by the restart auto-negotiation request, but it will not complete due to the FX operation mode.

Thus, Enhanced Link Detection has to be turned off for FX links (unless Enhanced FX Link Detection is used, which is recommended.

ISSUE: TEMPORARY ENHANCED LINK DETECTION WHILE EEPROM IS LOADING

Enhanced Link Detection is enabled after Reset, and it can only be disabled by EEPROM. This takes about 170 ms. In the meantime, the FX PHYs are powering up. Since they do not need to go through an auto-negotiation sequence, the link (signal detect) comes very early. It is possible that the link is detected, but communication is not possible (RX_ERR are detected). This can trigger the ESC to restart auto-negotiation before the EEPROM is loaded, resulting in the ESC waiting for the link to go down. This will probably not happen because the PHY ignores this command, so the ESC remains in a dead-lock situation.

The recommended solution to overcome this issue is to power up the FX PHY (and the transceiver) at least 170 ms after the ESC, such as by an additional reset controller with delay or power sequencing (Figure 6 or Figure 7).

Another recommended solution is the Enhanced FX Link Detection on page 10.

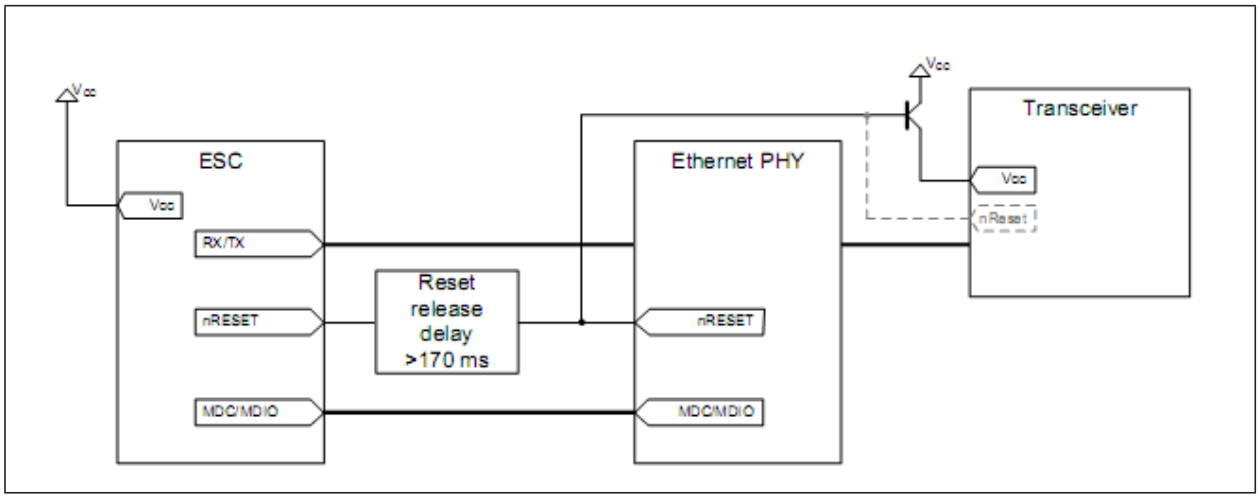
Minimum solutions without Enhanced Link Detection:

These two solutions represent the minimum solution for proper power-up and reset operation, but they have drawbacks in detection low quality links. The preferred solution is the Enhanced FX Link Detection, see later.

Standard Link Detection: By Delayed Reset to FX-PHY

RESET to External PHY is delayed by 170 ms after ESC (LAN9252) getting ready.

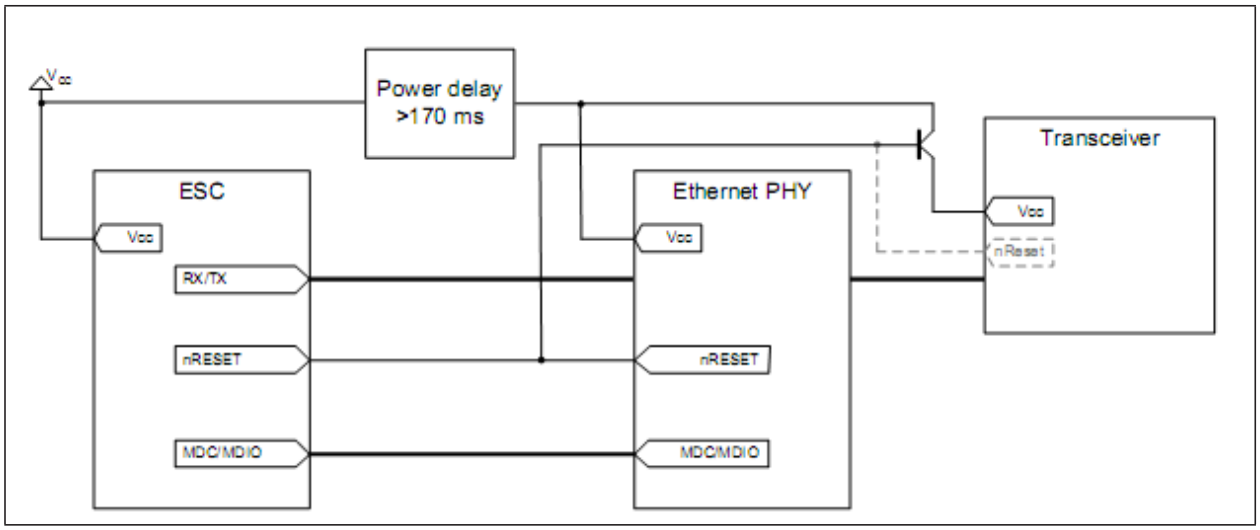
FIGURE 6: PHY RESET RELEASE DELAY WITH TRANSCEIVER POWER DOWN/RESET



Standard Link Detection: By Power Sequencing

POWER to External PHY is delayed by 170 ms after ESC getting powered up.

FIGURE 7: PHY POWER SEQUENCING WITH TRANSCEIVER POWER DOWN/RESET



Enhanced FX Link Detection

In order to detect erroneous links fast enough, it is desirable to use the error detection principle of Enhanced

Link Detection also for FX PHYs. One possible solution is to use the Enhanced Link Detection logic inside the ESC, and another possible solution is to implement enhanced link detection logic with external logic, such as a CPLD.

LAN9252 ESC does not support Enhanced Link Detection logic for external MII port; hence external logic should implement using micro controller/CPLD.

The preferred solution is to let the ESC count the RX_ERR of the PHY, and to detect the restart auto-negotiation request of the ESC by some additional logic (CPLD or µController etc.) attached to the MII management interface. This logic should reset the PHY and the Transceiver (power-down) for a short time. This reset causes a link down, which will be detected by the local ESC (which will leave its potential dead-lock state), and by the communication partner (link down, loop closed). If this solution is chosen, Enhanced Link Detection can be enabled in the EEPROM.

The MII management interface is still connected to the PHY, the CPLD/µC just snoops the bus. It is possible to use one CPLD/µC for all ports of the ESC. The PHY address has to be evaluated and individual reset outputs for each PHY have to be used.

PROPOSED SOLUTIONS WITH ENHANCED LINK DETECTION

The following images, Figure 8 and Figure 9, display the proposed solutions with enhanced link detection.

FIGURE 8: CPLD/µC DETECTS AUTO-NEGOTIATION RESTART COMMAND AND RESETS PHY AND TRANSCEIVER

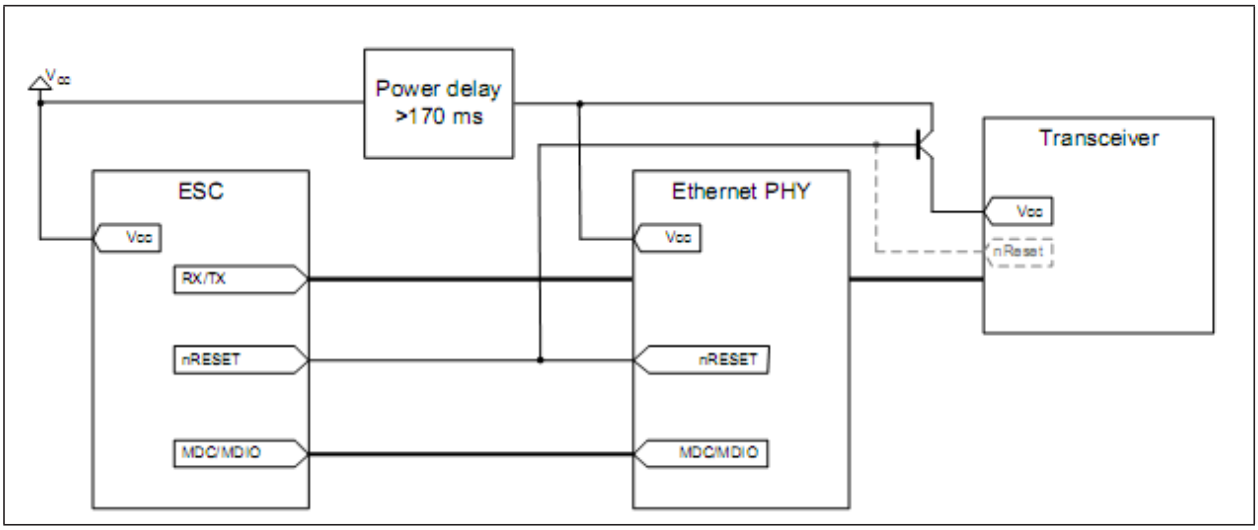
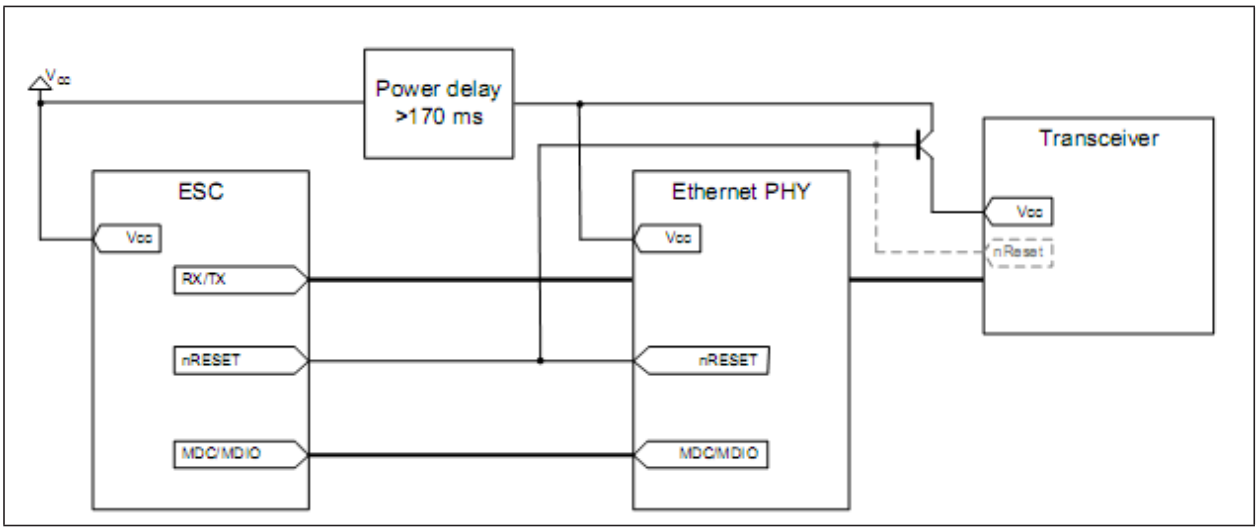


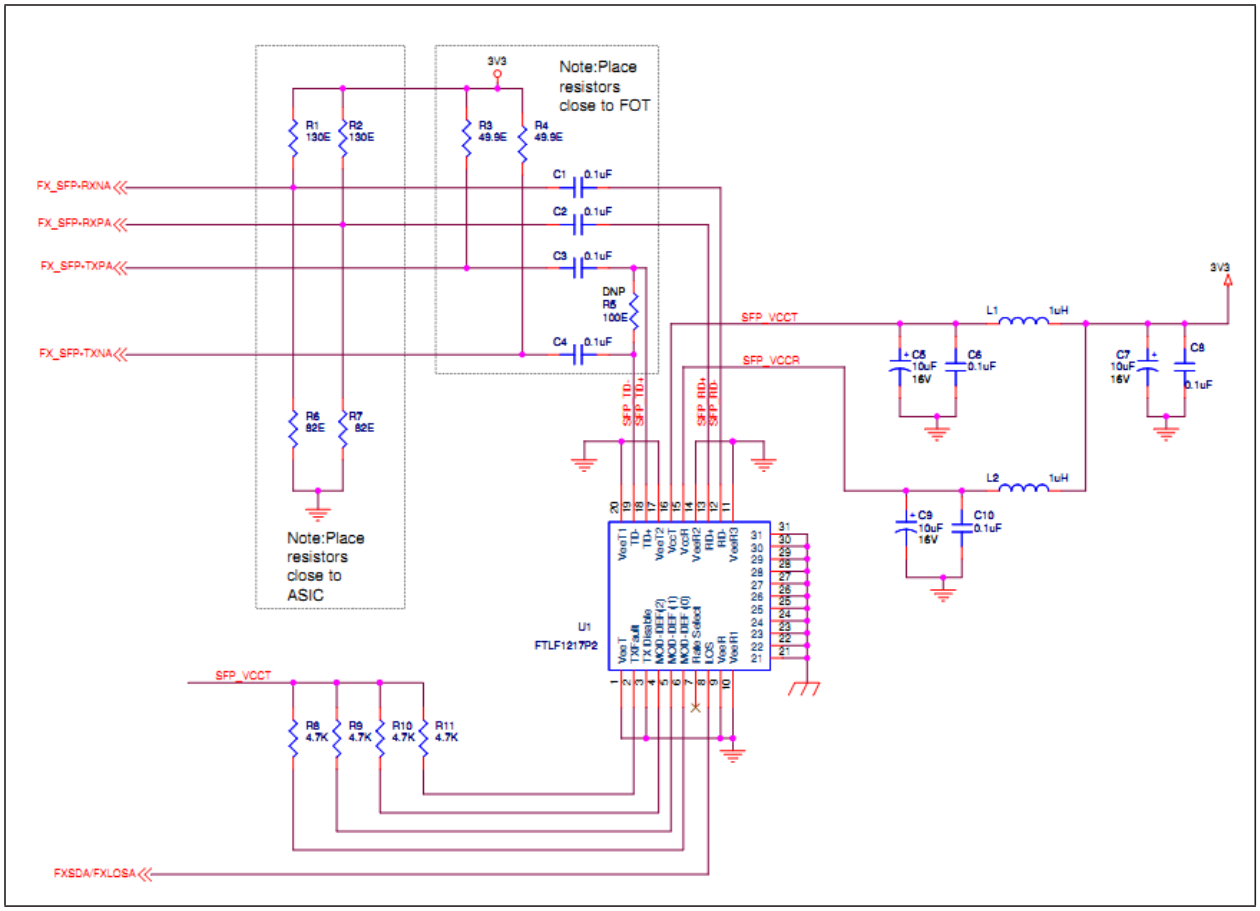
FIGURE 9: CPLD/µC DETECTS AUTO-NEGOTIATION RESTART COMMAND AND POWERS DOWN PHY AND TRANSCEIVER



Note: In Figure 9, the CPLD/µC is connected to the nRESET signal of the ESC/PHY to power-down/reset the transceiver while the ESC/PHY is in reset state.

APPENDIX A: SCHEMATICS

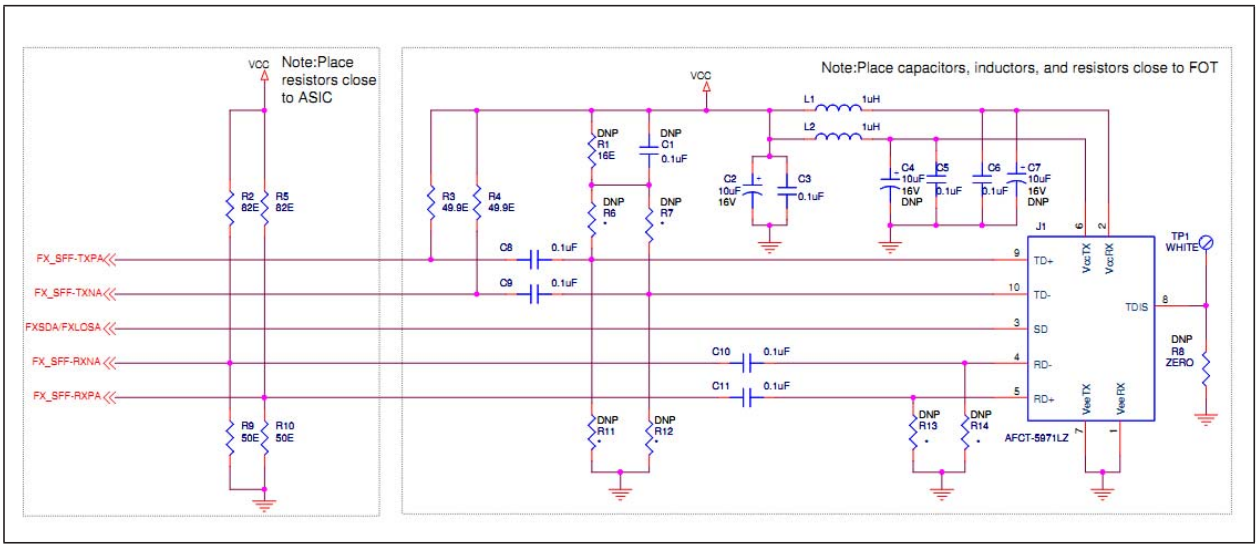
FIGURE A-1: SCHEMATIC A: INTERFACE BETWEEN LAN9XXX AND THE SFP (FTLF1318P2) FOT



Note 1: SFP Transceiver FTLF1318P2, TX/RX DATA lines are AC coupled, Hence C1,C2, C3 and C4 are not required externally.

2: Refer to FOT supplier's recommendation regarding the interface between LAN9xxx and FOT. The proposed termination is recommended for AC Coupled Configuration (SFP mode).
Other terminations could also be applicable, depending on the FOT interface.

FIGURE A-2: SCHEMATIC B: INTERFACE BETWEEN LAN9XXX AND THE SFF (AFBR-59E4APZ) FOT



Note 1: SFF Transceiver AFBR-59E4APZ, TX/RX DATA lines are AC coupled, Hence C8,C9, C10 and C11 are not required externally.

2: Refer to FOT supplier's recommendation regarding the interface between LAN9xxx and FOT. The proposed termination is recommended for AC Coupled Configuration (SFF mode). Other terminations could also be applicable, depending on the FOT interface.

APPENDIX B: APPLICATION NOTE REVISION HISTORY

TABLE B-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
Rev. A, Sept. 2015	Initial release.	

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