AN4284

LAN8804/LAN8814 General Register Definitions

1.0 INTRODUCTION

The LAN8804/LAN8814 General Register Definitions application note provides a description of all general registers within the LAN8804/LAN8814 and is meant for clarification of functionality during design and debugging. This document should be used in conjunction with the LAN8804/LAN8814 GPHY Register Definitions application note.

1.1 Sections

This document includes the following topics:

1.2 References

Consult the following documents for additional device details:

- LAN8804 Data Sheet, www.microchip.com
- LAN8814 Data Sheet, www.microchip.com
- LAN8804/LAN8814 GPHY Register Definitions, www.microchip.com

2.0 REGISTER MAP

TABLE 2-1: DEVICE COMMON REGISTERS (EP 4)

Index (in decimal)	Index (in hex)	Register Name
EP4 Chip Configuration/Control Registers		
0	0	Strap Status 1 Register
1	1	RESERVED
2	2	RESERVED
3	3	RESERVED
4	4	RESERVED
5	5	Output Control Register
6	6	RESERVED
7	7	RESERVED
8	8	Chip Hard Reset Register
9	9	Chip Soft Reset Register
10	Ah	RESERVED
11	Bh	SKU Register
12	Ch	RESERVED
13-23	Dh-17h	Not Used
24-31	18h-1Fh	Software Scratchpad Registers
EP4 GPIO Registers		
32	20h	General Purpose IO Enable 1 Register (GPIO_EN1)
33	21h	General Purpose IO Enable 2 Register (GPIO_EN2)
34	22h	General Purpose IO Direction 1 Register (GPIO_DIR1)
35	23h	General Purpose IO Direction 2 Register (GPIO_DIR2)
36	24h	General Purpose IO Buffer Type 1 Register (GPIO_BUF1)
37	25h	General Purpose IO Buffer Type 2 Register (GPIO_BUF2)
38	26h	General Purpose IO Data 1 Register (GPIO_DATA1)
39	27h	General Purpose IO Data 2 Register (GPIO_DATA2)
40	28h	General Purpose IO Interrupt Status 1 Register (GPIO_INT_STS1)
41	29h	General Purpose IO Interrupt Status 2 Register (GPIO_INT_STS2)
42	2Ah	General Purpose IO Interrupt Enable 1 Register (GPIO_INT_EN1)
43	2Bh	General Purpose IO Interrupt Enable 2 Register (GPIO_INT_EN2)
44	2Ch	General Purpose IO Interrupt Polarity 1 Register (GPIO_INT_POL1)
45	2Dh	General Purpose IO Interrupt Polarity 2 Register (GPIO_INT_POL2)
46	2Eh	General Purpose IO Pullup Pulldown Override 1 Register (GPIO_PU_PD_OVERRIDE1)
47	2Fh	General Purpose IO Pullup Pulldown Override 2 Register (GPIO_PU_PD_OVERRIDE2)
48	30h	General Purpose IO Pullup Pulldown Override 3 Register (GPIO_PU_PD_OVERRIDE3)
49	31h	General Purpose IO SOF Select Register
50	32h	Not Used
EP4 Chip Interrupt Registers		
51	33h	Chip-level Interrupt Status Register

TABLE 2-1: DEVICE COMMON REGISTERS (EP 4) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
52	34h	Chip-Level Interrupt Control Register
53	35h	RESERVED
54-63	36h-3Fh	Not Used
EP4 QSGMII Configuration Registers		
64	40h	QSGMII Extender Configuration and Status Register
65	41h	QSGMII Status Register
66	42h	QSGMII Hard Reset Register
67	43h	QSGMII Soft Reset Register
68	44h	QSGMII Mux Control Register
69	45h	QSGMII Auto ANEG Enable Register
69-127	44h-7Fh	Not Used
EP4 QSGMII SerDes Registers		
128	80h	QSGMII SerDes Receive Lane Status Register
129	81h	QSGMII SerDes Transmit Level Control Register
130	82h	QSGMII SerDes Transmit General Control Register
131	83h	QSGMII SerDes Transmit Status Register
132	84h	RESERVED
133	85h	QSGMII SerDes Receive Equalization Control Register
134	86h	QSGMII SerDes Receive Loss of Signal Control Register
135	87h	RESERVED
136	88h	QSGMII SerDes Receive Level Control Register
137	89h	QSGMII SerDes Miscellaneous Control Register
138	8Ah	QSGMII SerDes Control and Status Register
139	8Bh	QSGMII SerDes CR Control Register
140	8Ch	QSGMII SerDes CR Address Register
141	8Dh	QSGMII SerDes CR Data Register
142	8Eh	QSGMII SerDes VREG_BYP Status Register
143-255	8Fh-FFh	Not Used
EP4 Recovered Clock Output Registers		
256	100h	Recovered Clock Output 1 Selector Register
257	101h	Recovered Clock Output 1 Divider Register
258	102h	Recovered Clock Output 2 Selector Register
259	103h	Recovered Clock Output 2 Divider Register
260-319	104h-13Fh	Not Used
EP4 1588 PLL Registers		
320	140h	1588 PLL Reset Register
321	141h	1588 PLL Bypass Register
322	142h	1588 PLL Status Register
323	143h	1588 PLL Divider Register
324	144h	1588 PLL Filter Range Register
325-383	145h-17Fh	Not Used

TABLE 2-1: DEVICE COMMON REGISTERS (EP 4) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
EP4 PVT Registers		
384	180h	AB PVT Control Register 1
385	181h	AB PVT Control Register 2
386	182h	AB PVT Status Register
387	183h	Reserved (do not use)
388	184h	AB PVT Interrupt Status Register
389	185h	Reserved (do not use)
390	186h	AB PVT Interrupt Mask Register
391	187h	Reserved (do not use)
392	188h	AB PVT Data Register
393	189h	Reserved (do not use)
394	18Ah	AB PVT Sample Time Register
395	18Bh	Reserved (do not use)
396	18Ch	AB PVT Thermal Comparator Control Register
397	18Dh	Reserved (do not use)
398	18Eh	AB PVT Thermal Comparator Threshold 0 Register
399	18Fh	Reserved (do not use)
400	190hh	AB PVT Thermal Comparator Threshold 1 Register
401	191h	Reserved (do not use)
402	192h	AB PVT Thermal Comparator Threshold 2 Register
403	193h	Reserved (do not use)
404	194h	AB PVT Sample Clock Divider Register
405	195h	Reserved (do not use)
406	196h	AB PVT PSEL25 Register
407	197h	AB PVT Hard Reset Register
408	198h	AB PVT Soft Reset Register
409	199h	AB PVT Clock Divider Register
410-447	19Ah-1BFh	Not Used
EP4 Not Used		
448-511	1C0h-1FFh	Not Used
EP4 Chip 1588 Common Registers		
512	200h	PTP Command and Control Register (PTP_CMD_CTL)
513	201h	PTP General Configuration Register (PTP_GENERAL_CONFIG)
514	202h	PTP Reference Clock Configuration Register (PTP_REF_CLK_CFG)
515	203h	PTP Common Interrupt Status Register (PTP_COMMON_INT_STS)
516	204h	PTP Common Interrupt Enable Register (PTP_COMMON_INT_EN)
517	205h	PTP LTC Set Seconds High Register (PTP_LTC_SET_SEC_HI)
518	206h	PTP LTC Set Seconds Mid Register (PTP_LTC_SET_SEC_MID)
519	207h	PTP LTC Set Seconds Low Register (PTP_LTC_SET_SEC_LO)
520	208h	PTP LTC Set Nanoseconds High Register (PTP_LTC_SET_NS_HI)
521	209h	PTP LTC Set Nanoseconds Low Register (PTP_LTC_SET_NS_LO)
522	20Ah	PTP LTC Set Sub-Nanoseconds High Register (PTP_LTC_SET_-SUBNS_HI)

TABLE 2-1: DEVICE COMMON REGISTERS (EP 4) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
523	20Bh	PTP LTC Set Sub-Nanoseconds Low Register (PTP_LTC_SET_-SUBNS_LO)
524	20Ch	PTP LTC Rate Adjustment High Register (PTP_LTC_RATE_ADJ_HI)
525	20Dh	PTP LTC Rate Adjustment Low Register (PTP_LTC_RATE_ADJ_LO)
526	20Eh	PTP LTC Temporary Rate Adjustment High Register (PTP_LTC_-TEMP_RATE_ADJ_HI)
527	20Fh	PTP LTC Temporary Rate Adjustment Low Register (PTP_LTC_-TEMP_RATE_ADJ_LO)
528	210h	PTP LTC Temporary Rate Duration High Register (PTP_LTC_-TEMP_RATE_DURATION_HI)
529	211h	PTP LTC Temporary Rate Duration Low Register (PTP_LTC_-TEMP_RATE_DURATION_LO)
530	212h	PTP LTC Step Adjustment High Register (PTP_LTC_STEP_ADJ_HI)
531	213h	PTP LTC Step Adjustment Low Register (PTP_LTC_STEP_ADJ_LO)
532	214h	PTP LTC External Adjustment Configuration Register (PTP_LTC_EX-T_ADJ_CFG)
533	215h	PTP LTC Target x Seconds High Register (PTP_LTC_TAR-GET_SEC_HI_x) x = A
534	216h	PTP LTC Target x Seconds Low Register (PTP_LTC_TAR-GET_SEC_LO_x) x = A
535	217h	PTP LTC Target x Nanoseconds High Register (PTP_LTC_TAR-GET_NS_HI_x) x = A
536	218h	PTP LTC Target x Nanoseconds Low Register (PTP_LTC_TAR-GET_NS_LO_x) x = A
537	219h	PTP LTC Target x Reload/Add Seconds High Register (PTP_LTC_TARGET_RELOAD_SEC_HI_x) x = A
538	21Ah	PTP LTC Target x Reload/Add Seconds Low Register (PTP_LTC_TAR-GET_RELOAD_SEC_LO_x) x = A
539	21Bh	PTP LTC Target x Reload/Add Nanoseconds High Register (PTP_LTC_TARGET_RELOAD_NS_HI_x) x = A
540	21Ch	PTP LTC Target x Reload/Add Nanoseconds Low Register (PTP_LTC_TARGET_RELOAD_NS_LO_x) x = A
541	21Dh	PTP LTC Target x Actual Nanoseconds High Register (PTP_LTC_TAR-GET_ACT_NS_HI_x) x = A
542	21Eh	PTP LTC Target x Actual Nanoseconds Low Register (PTP_LTC_TAR-GET_ACT_NS_LO_x) x = A
543	21Fh	PTP LTC Target x Seconds High Register (PTP_LTC_TAR-GET_SEC_HI_x) x = B
544	220h	PTP LTC Target x Seconds Low Register (PTP_LTC_TAR-GET_SEC_LO_x) x = B
545	221h	PTP LTC Target x Nanoseconds High Register (PTP_LTC_TAR-GET_NS_HI_x) x = B
546	222h	PTP LTC Target x Nanoseconds Low Register (PTP_LTC_TAR-GET_NS_LO_x) x = B
547	223h	PTP LTC Target x Reload/Add Seconds High Register (PTP_LTC_TARGET_RELOAD_SEC_HI_x) x = B
548	224h	PTP LTC Target x Reload/Add Seconds Low Register (PTP_LTC_TAR-GET_RELOAD_SEC_LO_x) x = B

TABLE 2-1: DEVICE COMMON REGISTERS (EP 4) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
549	225h	PTP LTC Target x Reload/Add Nanoseconds High Register (PTP_LTC_TARGET_RELOAD_NS_HI_x) x = B
550	226h	PTP LTC Target x Reload/Add Nanoseconds Low Register (PTP_LTC_TARGET_RELOAD_NS_LO_x) x = B
551	227h	PTP LTC Target x Actual Nanoseconds High Register (PTP_LTC_TARGET_ACT_NS_HI_x) x = B
552	228h	PTP LTC Target x Actual Nanoseconds Low Register (PTP_LTC_TARGET_ACT_NS_LO_x) x = B
553	229h	PTP LTC Read Seconds High Register (PTP_LTC_RD_SEC_HI)
554	22Ah	PTP LTC Read Seconds Mid Register (PTP_LTC_RD_SEC_MID)
555	22Bh	PTP LTC Read Seconds Low Register (PTP_LTC_RD_SEC_LO)
556	22Ch	PTP LTC Read Nanoseconds High Register (PTP_LTC_RD_NS_HI)
557	22Dh	PTP LTC Read Nanoseconds Low Register (PTP_LTC_RD_NS_LO)
558	22Eh	PTP LTC Read Sub-Nanoseconds High Register (PTP_LTC_RD_-SUBNS_HI)
559	22Fh	PTP LTC Read Sub-Nanoseconds Low Register (PTP_LTC_RD_-SUBNS_LO)
560	230h	PTP GPIO Select Register (PTP_GPIO_SEL)
561	231h	PTP GPIO Capture Map High Register (PTP_GPIO_CAP_MAP_HI)
562	232h	PTP GPIO Capture Map Low Register (PTP_GPIO_CAP_MAP_LO)
563	233h	PTP GPIO Capture Enable Register (PTP_GPIO_CAP_EN)
564	234h	PTP GPIO Capture Lock Register (PTP_GPIO_CAP_LOCK)
565	235h	PTP GPIO x Rising Edge LTC Seconds High Capture Register (PTP_GPIO_RE_LTC_SEC_HI_CAP_x)
566	236h	PTP GPIO x Rising Edge LTC Seconds Low Capture Register (PTP_GPIO_RE_LTC_SEC_LO_CAP_x)
567	237h	PTP GPIO x Rising Edge LTC Nanoseconds High Capture Register (PTP_GPIO_RE_LTC_NS_HI_CAP_x)
568	238h	PTP GPIO x Rising Edge LTC Nanoseconds Low Capture Register (PTP_GPIO_RE_LTC_NS_LO_CAP_x)
569	239h	PTP GPIO x Falling Edge LTC Seconds High Capture Register (PTP_GPIO_FE_LTC_SEC_HI_CAP_x)
570	23Ah	PTP GPIO x Falling Edge LTC Seconds Low Capture Register (PTP_GPIO_FE_LTC_SEC_LO_CAP_x)
571	23Bh	PTP GPIO x Falling Edge LTC Nanoseconds High Capture Register (PTP_GPIO_FE_LTC_NS_HI_CAP_x)
572	23Ch	PTP GPIO x Falling Edge LTC Nanoseconds Low Capture Register (PTP_GPIO_FE_LTC_NS_LO_CAP_x)
573	23Dh	PTP GPIO Capture Status Register (PTP_GPIO_CAP_STS)
574	23Eh	PTP GPIO Interrupt Clear Configuration Register (PTP_GPIO_INT_-CLR_CFG)
575	23Fh	PTP LTC Hard Reset Register
576	240h	PTP LTC Soft Reset Register
577	241h	PTP Operating Mode Register
578	242h	PTP Revision Register
579	243h	PTP PCH SubPortID Register
580	244h	PTP Latency Correction Control Register

TABLE 2-1: DEVICE COMMON REGISTERS (EP 4) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
581-767	245h-2FFh	Not Used
EP4 1588 Serial Timestamp Interface Registers		
768	300h	1588 STI Configuration Register
769	301h	1588 STI Tx Count Register
770	302h	1588 STI Hard Reset Register
771	303h	1588 STI Soft Reset Register

TABLE 2-2: DEVICE PORT-SPECIFIC REGISTERS (EP 5)

Index (in decimal)	Index (in hex)	Register Name
EP5 LED Control Registers		
0	0	LED Control Register 1
1	1	LED Control Register 2
2-15	2-0Fh	Not Used
EP5 QSGMII PCS1G Registers		
16	10h	QSGMII PCS1G Hard Reset Register
17	11h	QSGMII PCS1G Soft Reset Register
18	12h	QSGMII PCS1G Configuration and Status Register
19	13h	QSGMII PCS1G ANEG Configuration Register
20	14h	QSGMII PCS1G ANEG Tx Advertised Abilities Register
21	15h	QSGMII PCS1G ANEG Tx NP Data Register
22	16h	QSGMII PCS1G ANEG LP Advertised Abilities Register
23	17h	QSGMII PCS1G ANEG LP NP Data Register
24	18h	QSGMII PCS1G Debug Register
25	19h	QSGMII PCS1G LPI Configuration and Status Register
26	1Ah	QSGMII PCS1G Test Pattern Configuration and Status Register
27-31	1Bh-1Fh	Not Used
32	20h	RX RA FIFO Thresholds 1 Register
33	21h	RX RA FIFO Thresholds 2 Register
34	22h	RX RA FIFO Thresholds 3 Register
35	23h	RX RA FIFO Read Count Configuration Register
36	24h	RX RA FIFO IFG Count Register
37	25h	RX RA FIFO Status Register
38	26h	TX RA FIFO Thresholds 1 Register
39	27h	TX RA FIFO Thresholds 2 Register
40	28h	TX RA FIFO Thresholds 3 Register
41	29h	TX RA FIFO Write Count Configuration Register
42	2Ah	TX RA FIFO IFG Count Register
43	2Bh	TX RA FIFO Status Register
44	2Ch	Tx RA FIFO Reset Register
45	2Dh	Rx RA FIFO Reset Register
46	2Eh	RESERVED
47	2Fh	RX RA FIFO IN HIGH COUNT Register

TABLE 2-2: DEVICE PORT-SPECIFIC REGISTERS (EP 5) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
48	30h	RX RA FIFO IN LOW COUNT Register
49	31h	RX RA FIFO OUT HIGH COUNT Register
50	32h	RX RA FIFO OUT LOW COUNT Register
51	33h	TX RA FIFO IN HIGH COUNT Register
52	34h	TX RA FIFO IN LOW COUNT Register
53	35h	TX RA FIFO OUT HIGH COUNT Register
54	36h	TX RA FIFO OUT LOW COUNT Register
55	37h	RX RA AEMPTY COUNT HIGH Register
56	38h	RX RA AEMPTY COUNT LOW Register
57	39h	RX RA AFULL COUNT HIGH Register
58	3Ah	RX RA AFULL COUNT LOW Register
59	3Bh	RX RA EMPTY COUNT Register
60	3Ch	RX RA FULL COUNT Register
61	3Dh	TX RA AEMPTY COUNT HIGH Register
62	3Eh	TX RA AEMPTY COUNT LOW Register
63	3Fh	TX RA AFULL COUNT HIGH Register
64	40h	TX RA AFULL COUNT LOW Register
65	41h	TX RA EMPTY COUNT Register
66	42h	TX RA FULL COUNT Register
67-79	43h-4Fh	Not Used
EP5 Port Control Registers		
80	50h	Port Hard Reset Register
81	51h	Port Soft Reset Register
82-95	52h-5Fh	Not Used
EP5 Not Used		
96-511	60h-1FFh	Not Used
EP5 1588 Port-Specific Registers		
512	200h	PTP TSU Interrupt Enable Register (PTP_TSU_INT_EN)
513	201h	PTP TSU Interrupt Status Register (PTP_TSU_INT_STS)
514	202h	PTP Modification Error Register (PTP_MOD_ERR)
515	203h	PTP RX User MAC Address High Register (PTP_RX_USER_MAC_HI)
516	204h	PTP RX User MAC Address Mid Register (PTP_RX_US-ER_MAC_MID)
517	205h	PTP RX User MAC Address Low Register (PTP_RX_USER_MAC_LO)
518	206h	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x = 0
519	207h	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x = 1
520	208h	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x = 2
521	209h	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x = 3
522	20Ah	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x = 4

TABLE 2-2: DEVICE PORT-SPECIFIC REGISTERS (EP 5) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
523	20Bh	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x = 5
524	20Ch	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x = 6
525	20Dh	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x = 7
526	20Eh	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x = 0
527	20Fh	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x = 1
528	210h	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x = 2
529	211h	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x = 3
530	212h	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x = 4
531	213h	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x = 5
532	214h	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x = 6
533	215h	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x = 7
534	216h	VLAN Ethernet Type ID Register (VLAN_TYPE_ID)
535	217h	VLAN 1 Type/ID Register (VLAN1_TYPE_ID)
536	218h	VLAN 1 ID Mask Register (VLAN1_ID_MASK)
537	219h	VLAN 1 VID Range Upper Register (VLAN1_VID_RANGE_UP)
538	21Ah	VLAN 1 VID Range Lower Register (VLAN1_VID_RANGE_LO)
539	21Bh	VLAN 2 Type/ID Register (VLAN2_TYPE_ID)
540	21Ch	VLAN 2 ID Mask Register (VLAN2_ID_MASK)
541	21Dh	VLAN 2 VID Range Upper Register (VLAN2_VID_RANGE_UP)
542	21Eh	VLAN 2 VID Range Lower Register (VLAN2_VID_RANGE_LO)
543	21Fh	LLC Ethernet Type ID Register (LLC_TYPE_ID)
544	220h	PTP RX Latency 10Mbps Register (PTP_RX_LATENCY_10)
545	221h	PTP TX Latency 10Mbps Register (PTP_TX_LATENCY_10)
546	222h	PTP RX Latency 100Mbps Register (PTP_RX_LATENCY_100)
547	223h	PTP TX Latency 100Mbps Register (PTP_TX_LATENCY_100)
548	224h	PTP RX Latency 1000Mbps Register (PTP_RX_LATENCY_1000)
549	225h	PTP TX Latency 1000Mbps Register (PTP_TX_LATENCY_1000)
550	226h	PTP Asymmetry Delay High Register (PTP_ASYM_DLY_HI)
551	227h	PTP Asymmetry Delay Low Register (PTP_ASYM_DLY_LO)
552	228h	PTP Peer Delay High Register (PTP_PEERDLY_HI)
553	229h	PTP Peer Delay Low Register (PTP_PEERDLY_LO)
554	22Ah	PTP Capture Information Register (PTP_CAP_INFO)
555	22Bh	PTP TX User MAC Address High Register (PTP_TX_USER_MAC_HI)
556	22Ch	PTP TX User MAC Address Mid Register (PTP_TX_USER_MAC_MID)
557	22Dh	PTP TX User MAC Address Low Register (PTP_TX_USER_MAC_LO)

TABLE 2-2: DEVICE PORT-SPECIFIC REGISTERS (EP 5) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
558	22Eh	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x = 0
559	22Fh	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x = 1
560	230h	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x = 2
561	231h	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x = 3
562	232h	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x = 4
563	233h	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x = 5
564	234h	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x = 6
565	235h	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x = 7
566	236h	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x = 0
567	237h	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x = 1
568	238h	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x = 2
569	239h	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x = 3
570	23Ah	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x = 4
571	23Bh	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x = 5
572	23Bh	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x = 6
573	23Dh	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x = 7
574-577	23Eh-240h	RESERVED (Not Used)
578	242h	PTP RX Parsing Configuration Register (PTP_RX_PARSE_CONFIG)
579	243h	PTP RX Parsing VLAN Configuration Register (PTP_RX-_PARSE_VLAN_CONFIG)
580	244h	PTP RX Parsing Layer2 Format Address Enable Register (PTP_RX-_PARSE_L2_ADDR_EN)
581	245h	PTP RX Parsing IP Format Address Enable Register (PTP_RX-_PARSE_IP_ADDR_EN)
582	246h	PTP RX Parsing UDP Source Port Register (PTP_RX_PARSE_UD-P_SRC_PORT)
583	247h	PTP RX Parsing UDP Destination Port Register (PTP_RX-_PARSE_UDP_DEST_PORT)
584	248h	PTP RX Version Register (PTP_RX_VERSION)
585	249h	PTP RX Domain/Domain Range Lower Register (PTP_RX_DO-MAIN_DOMAIN_LO)
586	24Ah	PTP RX Domain Mask/Domain Range Upper Register (PTP_RX_DO-MAIN_MASK_DOMAIN_UP)

TABLE 2-2: DEVICE PORT-SPECIFIC REGISTERS (EP 5) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
587	24Bh	PTP RX SdoId/SdoId Range Lower Register (PTP_RX_SDOID_SDOID_LO)
588	24Ch	PTP RX SdoId Mask/SdoId Range Upper Register (PTP_RX_SDOID_MASK_SDOID_UP)
589	24Dh	PTP RX Timestamp Enable Register (PTP_RX_TIMESTAMP_EN)
590	24Eh	PTP RX Timestamp Configuration Register (PTP_RX_TIMESTAMP_CONFIG)
591	24Fh	PTP RX Modification Register (PTP_RX_MOD)
592	250h	PTP RX Reserved Bytes Configuration Register (PTP_RX_RSVD_BYTE_CFG)
593	251h	PTP RX Tail Tag Register (PTP_RX_TAIL_TAG)
594	252h	PTP RX Correction Field Modification Enable Register (PTP_RX_CF_MOD_EN)
595	253h	PTP RX Correction Field Configuration Register (PTP_RX_CF_CFG)
596	254h	PTP RX Ingress Time Nanoseconds High Register (PTP_RX_INGRESS_NS_HI)
597	255h	PTP RX Ingress Time Nanoseconds Low Register (PTP_RX_INGRESS_NS_LO)
598	256h	PTP RX Ingress Time Seconds High Register (PTP_RX_INGRESS_SEC_HI)
599	257h	PTP RX Ingress Time Seconds Low Register (PTP_RX_INGRESS_SEC_LO)
600	258h	PTP RX Message Header 1 Register (PTP_RX_MSG_HEADER1)
601	259h	PTP RX Message Header 2 Register (PTP_RX_MSG_HEADER2)
602	25Ah	PTP RX Pdelay_Req Ingress Time Seconds High Register (PTP_RX_PDREQ_SEC_HI)
603	25Bh	PTP RX Pdelay_Req Ingress Time Seconds Mid Register (PTP_RX_PDREQ_SEC_MID)
604	25Ch	PTP RX Pdelay_Req Ingress Time Seconds low Register (PTP_RX_PDREQ_SEC_LOW)
605	25Dh	PTP RX Pdelay_Req Ingress Time Nanoseconds High Register (PTP_RX_PDREQ_NS_HI)
606	25Eh	PTP RX Pdelay_Req Ingress Time Nanoseconds Low Register (PTP_RX_PDREQ_NS_LO)
607	25Fh	PTP RX Raw Ingress Time Seconds Register (PTP_RX_RAW_TS_SEC)
608	260h	PTP RX Raw Ingress Time Nanoseconds High Register (PTP_RX_RAW_TS_NS_HI)
609	261h	PTP RX Raw Ingress Time Nanoseconds Low Register (PTP_RX_RAW_TS_NS_LO)
610	262h	PTP RX Checksum Dropped Count High Register (PTP_RX_CHKSUM_DROPPED_CNT_HI)
611	263h	PTP RX Checksum Dropped Count Low Register (PTP_RX_CHKSUM_DROPPED_CNT_LO)
612	264h	PTP RX Frames Modified Count High Register (PTP_RX_FRMS_MOD_CNT_HI)
613	265h	PTP RX Frames Modified Count Low Register (PTP_RX_FRMS_MOD_CNT_LO)

TABLE 2-2: DEVICE PORT-SPECIFIC REGISTERS (EP 5) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
614-641	266h-281h	RESERVED/Not Used
642	282h	PTP TX Parsing Configuration Register (PTP_TX_PARSE_CONFIG)
643	283h	PTP TX Parsing VLAN Configuration Register (PTP_TX-_PARSE_VLAN_CONFIG)
644	284h	PTP TX Parsing Layer2 Format Address Enable Register (PTP_TX-_PARSE_L2_ADDR_EN)
645	285h	PTP TX Parsing IP Format Address Enable Register (PTP_TX-_PARSE_IP_ADDR_EN)
646	286h	PTP TX Parsing UDP Source Port Register (PTP_TX_PARSE_UD-P_SRC_PORT)
647	287h	PTP TX Parsing UDP Destination Port Register (PTP_TX_PARSE_UD-P_DEST_PORT)
648	288h	PTP TX Version Register (PTP_TX_VERSION)
649	289h	PTP TX Domain/Domain Range Lower Register (PTP_TX_DO-MAIN_DOMAIN_LO)
650	28Ah	PTP TX Domain Mask/Domain Range Upper Register (PTP_TX_DO-MAIN_MASK_DOMAIN_UP)
651	28Bh	PTP TX SdoId/SdoId Range Lower Register (PTP_TX_SDOID_S-DOID_LO)
652	28Ch	PTP TX SdoId Mask/SdoId Range Upper Register (PTP_TX_S-DOID_MASK_SDOID_UP)
653	28Dh	PTP TX Timestamp Enable Register (PTP_TX_TIMESTAMP_EN)
654	28Eh	PTP TX Timestamp Configuration Register (PTP_TX_TIMESTAMP_-CONFIG)
655	28Fh	PTP TX Modification Register (PTP_TX_MOD)
656	290h	PTP TX Reserved Bytes Configuration Register (PTP_TX_RSVD_-BYTE_CFG)
657	291h	PTP TX Tail Tag Register (PTP_TX_TAIL_TAG)
658	292h	PTP TX Correction Field Modification Enable Register (PTP_TX_CF_-MOD_EN)
659	293h	PTP TX Correction Field Configuration Register (PTP_TX_CF_CFG)
660	294h	PTP TX Egress Time Nanoseconds High Register (PTP_TX-_EGRESS_NS_HI)
661	295h	PTP TX Egress Time Nanoseconds Low Register (PTP_TX-_EGRESS_NS_LO)
662	296h	PTP TX Egress Time Seconds High Register (PTP_TX-_EGRESS_SEC_HI)
663	297h	PTP TX Egress Time Seconds Low Register (PTP_TX-_EGRESS_SEC_LO)
664	298h	PTP TX Message Header 1 Register (PTP_TX_MSG_HEADER1)
665	299h	PTP TX Message Header 2 Register (PTP_TX_MSG_HEADER2)
666	29Ah	PTP TX Sync Egress Time Seconds High Register (PTP_TX_SYN-C_SEC_HI)
667	29Bh	PTP TX Sync Egress Time Seconds Mid Register (PTP_TX_SYN-C_SEC_MID)
668	29Ch	PTP TX Sync Egress Time Seconds Low Register (PTP_TX_SYN-C_SEC_LOW)

TABLE 2-2: DEVICE PORT-SPECIFIC REGISTERS (EP 5) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
669	29Dh	PTP TX Sync Egress Time Nanoseconds High Register (PTP_TX_SYNC_NS_HI)
670	29Eh	PTP TX Sync Egress Time Nanoseconds Low Register (PTP_TX_SYNC_NS_LO)
671	29Fh	PTP TX Pdelay_Resp Egress Time Seconds High Register (PTP_TX_PDRESP_SEC_HI)
672	2A0h	PTP TX Pdelay_Resp Egress Time Seconds Mid Register (PTP_TX_PDRESP_SEC_MID)
673	2A1h	PTP TX Pdelay_Resp Egress Time Seconds low Register (PTP_TX_PDRESP_SEC_LOW)
674	2A2h	PTP TX Pdelay_Resp Egress Time Nanoseconds High Register (PTP_TX_PDRESP_NS_HI)
675	2A3h	PTP TX Pdelay_Resp Egress Time Nanoseconds Low Register (PTP_TX_PDRESP_NS_LO)
676	2A4h	PTP TX Raw Egress Time Seconds Register (PTP_TX_RAW_TS_SEC)
677	2A5h	PTP TX Raw Egress Time Nanoseconds High Register (PTP_TX_RAW_TS_NS_HI)
678	2A6h	PTP TX Raw Egress Time Nanoseconds Low Register (PTP_TX_RAW_TS_NS_LO)
679	2A7h	PTP TX Checksum Dropped Count High Register (PTP_TX_CHKSUM_DROPPED_CNT_HI)
680	2A8h	PTP TX Checksum Dropped Count Low Register (PTP_TX_CHKSUM_DROPPED_CNT_LO)
681	2A9h	PTP TX Frames Modified Count High Register (PTP_TX_FRMS_MOD_CNT_HI)
682	2AAh	PTP TX Frames Modified Count Low Register (PTP_TX_FRMS_MOD_CNT_LO)
683-703	2ABh-2BFh	RESERVED (Not Used)
704	2C0h	TSU General Configuration Register (TSU_GENERAL_CONFIG)
705	2C1h	TSU Hard Reset Register
706	2C2h	TSU Soft Reset Register
707	2C3h	PTP PCH Format Mismatch Register

2.1 Extended Page 4 Registers

Device Common Registers are mapped to EP4.

2.1.1 STRAP STATUS 1 REGISTER

Index (In decimal): EP 4.0 Size: 16 bits

This register indicates the value of device straps that were latched into the device at reset. It also indicates the value of the COMA_MODE input pin (live input pin, not a strap).

Bits	Description	Type	Default
15	**Strap_Port3_LED2_POL** Strap status of LED polarity 0 = Active low 1 = Active high	RO	Note 1
14	**Strap_Port3_LED1_POL** Strap status of LED polarity 0 = Active low 1 = Active high	RO	Note 1
13	**Strap_Port2_LED2_POL** Strap status of LED polarity 0 = Active low 1 = Active high	RO	Note 1
12	**Strap_Port2_LED1_POL** Strap status of LED polarity 0 = Active low 1 = Active high	RO	Note 1
11	**Strap_Port1_LED2_POL** Strap status of LED polarity 0 = Active low 1 = Active high	RO	Note 1
10	**Strap_Port1_LED1_POL** Strap status of LED polarity 0 = Active low 1 = Active high	RO	Note 1
9	**Strap_Port0_LED2_POL** Strap status of LED polarity 0 = Active low 1 = Active high	RO	Note 1
8	**Strap_Port0_LED1_POL** Strap status of LED polarity 0 = Active low 1 = Active high	RO	Note 1
7	**Strap_led_single** Strap status of single LED	RO	Note 2
6	**RESERVED**	RO	—
5	**COMA_MODE** Read-only status of the COMA_MODE input pin 0 = Normal operation 1 = Coma mode	RO	—

Note 1: Set by the inverse of each LED-POL strapping pin.
2: Set by the LED_MODE strapping pin.
3: Set by the PHYAD[4:0] strapping pins.

Bits	Description	Type	Default
4:0	**strap_phyad[4:0]** Strap-in value for PHY address	RO	Note 3

Note 1: Set by the inverse of each LED-POL strapping pin.
2: Set by the LED_MODE strapping pin.
3: Set by the PHYAD[4:0] strapping pins.

2.1.2 OUTPUT CONTROL REGISTER

Index (In decimal): EP 4.5 Size: 16 bits

This register selects the output buffer type and polarity of the INT_N, MDIO.

Bits	Description	Type	Default
15	**MDIO Buffer Type** When set to a 0, the MDIO output is open-drain. When set to a 1, the MDIO output is push-pull. To configure MDIO Output to Push-Pull, EP4.5 bit 15 (MDIO Buffer Type) must be set to 1, and also direct register 17 bit 9 must be set to 1 for all ports.	R/W	0b
14	**INT Buffer Type** When set to a 0, the INT_N output is open-drain. When set to a 1, the INT_N output is push-pull. **Note:** If the buffer type is set to open-drain, INT_N is always active low.	R/W	0b
13:8	**RESERVED**	RO	—
7	**RESERVED**	RO	—
6	**RESERVED**	RO	—
5:0	**RESERVED**	RO	—

2.1.3 CHIP HARD RESET REGISTER

Index (In decimal): EP 4.8 Size: 16 bits

This register resets the entire chip including all logic blocks and macros, and sets all configuration registers to their default state.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Chip Hard Reset** 1 = Reset the chip and set all configuration registers to their default state Writing a zero has no effect	W1S/SC	0b

2.1.4 CHIP SOFT RESET REGISTER

Index (In decimal): EP 4.9 Size: 16 bits

This register resets the entire chip except the GPHYs including all logic blocks and macros, but does not reset any configuration registers. The GPHYs may each be soft-reset individually using the Software Soft Reset in each GPHY.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Chip Soft Reset** 1 = Reset the chip except GPHY and all configuration registers Writing a zero has no effect	W1S/SC	0b

2.1.5 SKU REGISTER

Index (In decimal): EP 4.11 Size: 16 bits

This register is decoded from chip-level bondout options and provides the device SKU.

Bits	Description	Type	Default
15:0	**SKU[15:0]** Valid values are: • 8804 • 8814 • 8802 • 8812 • 8808 • 8818 • 8806 • 8816	RO	—

2.1.6 SOFTWARE SCRATCHPAD REGISTERS

Index (In decimal): EP 4.24-31 Size: 16 bits

These registers are provided for software use, they have no other function.

Register	Bits	Description	Type	Default
24	15:0	**Scratchpad Register 0** This register is writeable from software and readable by software, but provides no other functionality.	R/W	00h
25	15:0	**Scratchpad Register 1** This register is writeable from software and readable by software, but provides no other functionality.	R/W	00h
26	15:0	**Scratchpad Register 2** This register is writeable from software and readable by software, but provides no other functionality.	R/W	00h
27	15:0	**Scratchpad Register 3** This register is writeable from software and readable by software, but provides no other functionality.	R/W	00h
28	15:0	**Scratchpad Register 4** This register is writeable from software and readable by software, but provides no other functionality.	R/W	00h
29	15:0	**Scratchpad Register 5** This register is writeable from software and readable by software, but provides no other functionality.	R/W	00h
30	15:0	**Scratchpad Register 6** This register is writeable from software and readable by software, but provides no other functionality.	R/W	00h
31	15:0	**Scratchpad Register 7** This register is writeable from software and readable by software, but provides no other functionality.	R/W	00h

2.1.7 GENERAL PURPOSE IO ENABLE 1 REGISTER (GPIO_EN1)

Index (In decimal): EP 4.32 Size: 16 bits

This register configures each GPIO[23:16] as a GPIO or an Alternate Function.

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**GPIO Enable (GPIO_EN[23:16])** 0 = Alternate Function (if applicable) 1 = GPIO Not all GPIOs have an Alternate Function. If no Alternate Function exists, both values of the applicable GPIO_EN result in GPIO. See DOS for listing of Alternate Functions for each GPIO.	R/W	00h

Note:

- Port LED Alternate Function: Port LED Buffer Type must be configured as open-drain or push-pull. Open-drain LED outputs will automatically choose between open-drain and open-source based on LED Polarity.
- Recovered Clock Out Alternate Function: Buffer Type is automatically set as Output push-pull.
- Recovered Clock In Alternate Function: Buffer Type is automatically set as Input.
- SOF Alternate Function: Buffer Type is automatically set as Output push-pull.
- 1588 Event Alternate Function: Buffer Type is automatically set as Output push-pull. Note this Alternate Function can serve as PPS Out.
- 1588 Load/Adjust Alternate Function: Buffer type is automatically set as Input.
- 1588 Serial Timestamp Interface Alternate Function: Buffer Type is automatically set as Output push-pull.
- 1588 External Reference Clock Alternate Function: Buffer Type is automatically set as Input.

2.1.8 GENERAL PURPOSE IO ENABLE 2 REGISTER (GPIO_EN2)

Index (In decimal): EP 4.33 Size: 16 bits

This register configures each GPIO[15:0] As a GPIO or Alternate Function.

Bits	Description	Type	Default
15:0	**GPIO Enable (GPIO_EN[15:0])** 0 = Alternate Function (if applicable) 1 = GPIO Not all GPIOs have an Alternate Function. If no Alternate Function exists, both values of the applicable GPIO_EN result in GPIO. See DOS for listing of Alternate Functions for each GPIO.	R/W	0000h

Note:

- Port LED Alternate Function: Port LED Buffer Type must be configured as open-drain or push-pull. Open-drain LED outputs will automatically choose between open-drain and open-source based on LED Polarity.
- Recovered Clock Out Alternate Function: Buffer Type is automatically set as Output push-pull.
- Recovered Clock In Alternate Function: Buffer Type is automatically set as Input.
- SOF Alternate Function: Buffer Type is automatically set as Output push-pull.
- 1588 Event Alternate Function: Buffer Type is automatically set as Output push-pull. Note this Alternate Function can serve as PPS Out.
- 1588 Load/Adjust Alternate Function: Buffer type is automatically set as Input.
- 1588 Serial Timestamp Interface Alternate Function: Buffer Type is automatically set as Output push-pull.
- 1588 External Reference Clock Alternate Function: Buffer Type is automatically set as Input.

2.1.9 GENERAL PURPOSE IO DIRECTION 1 REGISTER (GPIO_DIR1)

Index (In decimal): EP 4.34 Size: 16 bits

This register controls the GPIO[23:16] directions.

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**GPIO Direction (GPIO_DIR[23:16])** When set, enables the corresponding GPIO as an output. When cleared the GPIO is enabled as an input.	R/W	00h

2.1.10 GENERAL PURPOSE IO DIRECTION 2 REGISTER (GPIO_DIR2)

Index (In decimal): EP 4.35 Size: 16 bits

This register controls the GPIO[15:0] directions.

Bits	Description	Type	Default
15:0	**GPIO Direction (GPIO_DIR[15:0])** When set, enables the corresponding GPIO as an output. When cleared the GPIO is enabled as an input.	R/W	0000h

2.1.11 GENERAL PURPOSE IO BUFFER TYPE 1 REGISTER (GPIO_BUF1)

Index (In decimal): EP 4.36 Size: 16 bits

This register sets the GPIO[23:16] output buffer types.

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**GPIO Buffer Type (GPIO_BUF[23:16])** When set, the output buffer for the corresponding GPIO signal is configured as a push/pull driver. When cleared, the corresponding GPIO signal is configured as an open-drain driver.	R/W	00h

2.1.12 GENERAL PURPOSE IO BUFFER TYPE 2 REGISTER (GPIO_BUF2)

Index (In decimal): EP 4.37 Size: 16 bits

This register sets the GPIO[15:0] output buffer types.

Bits	Description	Type	Default
15:0	**GPIO Buffer Type (GPIO_BUF[15:0])** When set, the output buffer for the corresponding GPIO signal is configured as a push/pull driver. When cleared, the corresponding GPIO signal is configured as an open-drain driver.	R/W	0000h

2.1.13 GENERAL PURPOSE IO DATA 1 REGISTER (GPIO_DATA1)

Index (In decimal): EP 4.38 Size: 16 bits

This register sets or reads the GPIO[23:16] data values.

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**GPIO Data (GPIO_D[23:16])** When enabled as an output, the value written is reflected on the GPIO. When read, the value always reflects the current state of the corresponding GPIO pin, regardless of the value written or the GPIO direction.	R/W	00h

2.1.14 GENERAL PURPOSE IO DATA 2 REGISTER (GPIO_DATA2)

Index (In decimal): EP 4.39 Size: 16 bits

This register sets or reads the GPIO[15:0] data values.

Bits	Description	Type	Default
15:0	**GPIO Data (GPIO_D[15:0])** When enabled as an output, the value written is reflected on the GPIO. When read, the value always reflects the current state of the corresponding GPIO pin, regardless of the value written or the GPIO direction.	R/W	0000h

2.1.15 GENERAL PURPOSE IO INTERRUPT STATUS 1 REGISTER (GPIO_INT_STS1)

Index (In decimal): EP 4.40 Size: 16 bits

This register contains the GPIO[23:16] interrupt status bits. Interrupt status bits in this register reflect the state of the interrupt source regardless of the state of the corresponding enable. In order for a GPIO to function as an interrupt source, it must be enabled as a GPIO and configured as an input.

Reading this register clears the interrupt status.

Note 1: GPIOs must not cause an interrupt status to be set when not configured as a GPIO.

2: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**GPIO Interrupt (GPIO_INT[23:16])** Interrupts generated from the GPIOs. **Note:** The sources for these interrupts are level-sensitive. The GPIO inputs must be stable for ~16 ns (two consecutive 125 MHz edges) to be recognized.	RC	Note 1

Note 1: The default depends on the state of the GPIO pin.

2.1.16 GENERAL PURPOSE IO INTERRUPT STATUS 2 REGISTER (GPIO_INT_STS2)

Index (In decimal): EP 4.41 Size: 16 bits

This register contains the GPIO[15:0] interrupt status bits. Interrupt status bits in this register reflect the state of the interrupt source regardless of the state of the corresponding enable. In order for a GPIO to function as an interrupt source, it must be enabled as a GPIO and configured as an input.

Reading this register clears the interrupt status.

Note 1: GPIOs must not cause an interrupt status to be set when not configured as a GPIO.

2: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15:0	**GPIO Interrupt (GPIO_INT[15:0])** Interrupts generated from the GPIOs. **Note:** The sources for these interrupts are level-sensitive. The GPIO inputs must be stable for ~16 ns (two consecutive 125 MHz edges) to be recognized.	RC	Note 1

Note 1: The default depends on the state of the GPIO pin.

2.1.17 GENERAL PURPOSE IO INTERRUPT ENABLE 1 REGISTER (GPIO_INT_EN1)

Index (In decimal): EP 4.42 Size: 16 bits

This register is used to enable the corresponding bits in the General Purpose IO Interrupt Status 1 Register (GPIO_INT_STS1) as an interrupt source. In order for a GPIO to function as an interrupt source, it must be enabled as a GPIO and configured as an input.

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**GPIO Interrupt Enable (GPIO_INT_EN[23:16])** When set, interrupts are enabled from the GPIOs.	R/W	00h

2.1.18 GENERAL PURPOSE IO INTERRUPT ENABLE 2 REGISTER (GPIO_INT_EN2)

Index (In decimal): EP 4.43 Size: 16 bits

This register is used to enable the corresponding bits in the General Purpose IO Interrupt Status 1 Register (GPIO_INT_STS1) as an interrupt source. In order for a GPIO to function as an interrupt source, it must be enabled as a GPIO and configured as an input.

Bits	Description	Type	Default
15:0	**GPIO Interrupt Enable (GPIO_INT_EN[15:0])** When set, interrupts are enabled from the GPIOs.	R/W	0000h

2.1.19 GENERAL PURPOSE IO INTERRUPT POLARITY 1 REGISTER (GPIO_INT_POL1)

Index (In decimal): EP 4.44 Size: 16 bits

This register configures the GPIO[23:16] interrupt polarities.

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**GPIO Interrupt Polarity (GPIO_INT_POL[23:16])** When clear, an interrupt is triggered when the GPIO input is low. When set, an interrupt is triggered when the GPIO input is high.	R/W	00h

2.1.20 GENERAL PURPOSE IO INTERRUPT POLARITY 2 REGISTER (GPIO_INT_POL2)

Index (In decimal): EP 4.45 Size: 16 bits

This register configures the GPIO[15:0] interrupt polarities.

Bits	Description	Type	Default
15:0	**GPIO Interrupt Polarity (GPIO_INT_POL[15:0])** When clear, an interrupt is triggered when the GPIO input is low. When set, an interrupt is triggered when the GPIO input is high.	R/W	0000h

2.1.21 GENERAL PURPOSE IO PULLUP PULLDOWN OVERRIDE 1 REGISTER (GPIO_PU_PD_OVERRIDE1)

Index (In decimal): EP 4.46 Size: 16 bits

This register provides the ability to override the internal pull-up or pull-down resistor selection.

Bits	Description	Type	Default
15:14	**GPIO 23 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
13:12	**GPIO 22 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
11:10	**GPIO 21 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
9:8	**GPIO 20 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
7:6	**GPIO 19 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
5:4	**GPIO 18 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
3:2	**GPIO 17 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
1:0	**GPIO 16 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b

2.1.22 GENERAL PURPOSE IO PULLUP PULLDOWN OVERRIDE 2 REGISTER (GPIO_PU_PD_OVERRIDE2)

Index (In decimal): EP 4.47 Size: 16 bits

This register provides the ability to override the internal pull-up or pull-down resistor selection.

Bits	Description	Type	Default
15:14	**GPIO 15 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
13:12	**GPIO 14 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
11:10	**GPIO 13 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
9:8	**GPIO 12 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
7:6	**GPIO 11 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
5:4	**GPIO 10 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
3:2	**GPIO 9 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
1:0	**GPIO 8 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b

2.1.23 GENERAL PURPOSE IO PULLUP PULLDOWN OVERRIDE 3 REGISTER (GPIO_PU_PD_OVERRIDE3)

Index (In decimal): EP 4.48 Size: 16 bits

This register provides the ability to override the internal pull-up or pull-down resistor selection.

Bits	Description	Type	Default
15:14	**GPIO 7 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
13:12	**GPIO 6 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
11:10	**GPIO 5 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
9:8	**GPIO 4 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
7:6	**GPIO 3 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
5:4	**GPIO 2 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
3:2	**GPIO 1 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b
1:0	**GPIO 0 PU PD Override (1:0)** 00 = No Override (PU or PD determined by hardware) 01 = GPIO has Pull-up, no Pull-down 10 = GPIO has Pull-down, no Pull-up 11 = GPIO has no Pull-up, no Pull-down	R/W	00b

2.1.24 GENERAL PURPOSE IO SOF SELECT REGISTER

Index (In decimal): EP 4.49 Size: 16 bits

This register controls which SOF pulse is output on each GPIO enabled as an SOF Alternate Function pin.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:9	**SOF3_SEL[2:0]** 000 = Output is Port 0 Tx SOF 001 = Output is Port 0 Rx SOF 010 = Output is Port 1 Tx SOF 011 = Output is Port 1 Rx SOF 100 = Output is Port 2 Tx SOF 101 = Output is Port 2 Rx SOF 110 = Output is Port 3 Tx SOF 111 = Output is Port 3 Rx SOF	R/W	000b
8:6	**SOF2_SEL[2:0]** 000 = Output is Port 0 Tx SOF 001 = Output is Port 0 Rx SOF 010 = Output is Port 1 Tx SOF 011 = Output is Port 1 Rx SOF 100 = Output is Port 2 Tx SOF 101 = Output is Port 2 Rx SOF 110 = Output is Port 3 Tx SOF 111 = Output is Port 3 Rx SOF	R/W	010b
5:3	**SOF1_SEL[2:0]** 000 = Output is Port 0 Tx SOF 001 = Output is Port 0 Rx SOF 010 = Output is Port 1 Tx SOF 011 = Output is Port 1 Rx SOF 100 = Output is Port 2 Tx SOF 101 = Output is Port 2 Rx SOF 110 = Output is Port 3 Tx SOF 111 = Output is Port 3 Rx SOF	R/W	100b
2:0	**SOF0_SEL[2:0]** 000 = Output is Port 0 Tx SOF 001 = Output is Port 0 Rx SOF 010 = Output is Port 1 Tx SOF 011 = Output is Port 1 Rx SOF 100 = Output is Port 2 Tx SOF 101 = Output is Port 2 Rx SOF 110 = Output is Port 3 Tx SOF 111 = Output is Port 3 Rx SOF	R/W	110b

2.1.25 CHIP-LEVEL INTERRUPT STATUS REGISTER

Index (In decimal): EP 4.51 Size: 16 bits

This register contains the Chip-level interrupt status bits. Interrupt status bits in this register identify the block-level function(s) generating interrupt(s).

Reading this register does not clear the interrupt status. Clearing the interrupt is interrupt-specific, either by clearing the cause of the interrupt at its source or reading the applicable bit in the block-level ISR.

Bits	Description	Type	Default
15:11	**RESERVED**	RO	—
10	**GPIO Interrupt** Interrupts are being generated by one or more GPIOs	RO	Note 1
9	**AB PVT Monitor Interrupt** Interrupts are being generated by the AB PVT Monitor	RO	Note 1
8	**1588 Common Interrupt** Interrupts are being generated by the 1588 Common functions	RO	Note 1
7	**GPHY Hard Macro 3 Interrupt** Interrupts are being generated by GPHY Hard Macro 3	RO	Note 1
6	**GPHY Hard Macro 2 Interrupt** Interrupts are being generated by GPHY Hard Macro 2	RO	Note 1
5	**GPHY Hard Macro 1 Interrupt** Interrupts are being generated by GPHY Hard Macro 1	RO	Note 1
4	**GPHY Hard Macro 0 Interrupt** Interrupts are being generated by GPHY Hard Macro 0	RO	Note 1
3	**1588 TSU 3 Interrupt** Interrupts are being generated by 1588 TSU 3	RO	Note 1
2	**1588 TSU 2 Interrupt** Interrupts are being generated by 1588 TSU 2	RO	Note 1
1	**1588 TSU 1 Interrupt** Interrupts are being generated by 1588 TSU 1	RO	Note 1
0	**1588 TSU 0 Interrupt** Interrupts are being generated by 1588 TSU 0	RO	Note 1

Note 1: The default is depends on the state of the block-level interrupt (which all default to 0b inactive).

2.1.26 CHIP-LEVEL INTERRUPT CONTROL REGISTER

Index (In decimal): EP 4.52 Size: 16 bits

This register is used to configure chip-level interrupt behavior.

Bits	Description	Type	Default
15:2	**RESERVED**	RO	—
1	Intr Polarity Invert 1 = Invert 0 = Normal If the INT_N buffer type is set to open-drain, INT_N is always active low. (moved from Pfeiffer A1 Control Register)	R/W	0b
0	**Chip-level Interrupt Enable** 1 = Enable chip-level interrupts 0 = Disable chip-level interrupts **Note:** Both this chip-level interrupt enable and any applicable block-level interrupt enable must be active for an interrupt to be generated.	R/W	0b

2.1.27 QSGMII EXTENDER CONFIGURATION AND STATUS REGISTER

Index (In decimal): EP 4.64 Size: 16 bits

This register configures the QSGMII Extender.

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7	**FLIP_LANES** Flip or swap lanes (lane 0 with lane 3, lane 1 with lane 2)	R/W	0
6	**SHYST_DIS** Disable hysteresis of synchronization state machine	R/W	0
5	**E_DET_ENA** Enable 8b10b error propagation (8b10b errors code-groups are replaced by K30.7 error symbols)	R/W	1
4	**USE_I1_ENA** Use /I1/ during Idle sequencing only	R/W	0
3:0	**RESERVED**	RO	—

2.1.28 QSGMII STATUS REGISTER

Index (In decimal): EP 4.65 Size: 16 bits

This register provides QSGMII status.

Bits	Description	Type	Default
15:5	**RESERVED**	RO	—
4	**SYNC_STAT** Set when QSGMII channel has successfully synchronized on K28.1. This field is only valid when SHYST_DIS is 1.	RO	0
3	**SYNC_STAT_PORT0** Synchronization status of Port 0. Note this status is also available in PCS1G.	RO	0
2	**SYNC_STAT_PORT1** Synchronization status of Port 1. Note this status is also available in PCS1G.	RO	0
1	**SYNC_STAT_PORT2** Synchronization status of Port 2. Note this status is also available in PCS1G.	RO	0
0	**SYNC_STAT_PORT3** Synchronization status of Port 3. Note this status is also available in PCS1G.	RO	0

2.1.29 QSGMII HARD RESET REGISTER

Index (In decimal): EP 4.66 Size: 16 bits

This register resets the QSGMII Extender, QSGMII SerDes, and the four QSGMII PCS1G blocks and sets all related configuration registers to their default state.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**QSGMII Hard Reset** 1 = Reset the QSGMII Extender, QSGMII SerDes, and QSGMII PCS1G and set all configuration registers to their default state Writing a zero has no effect.	W1S/SC	0b

2.1.30 QSGMII SOFT RESET REGISTER

Index (In decimal): EP 4.67 Size: 16 bits

This register resets the QSGMII Extender, QSGMII SerDes, and the four QSGMII PCS1G blocks but does not reset any configuration registers.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**QSGMII Soft Reset** 1 = Reset the QSGMII Extender, QSGMII SerDes, and QSGMII PCS1G except all configuration registers Writing a zero has no effect.	W1S/SC	0b

2.1.31 QSGMII MUX CONTROL REGISTER

Index (In decimal): EP 4.68 Size: 16 bits

This register controls the multiplexing order of the four ports across QSGMII. It is intended as a debug register to be used when inter-operating with other vendor QSGMII implementations which use a different/unexpected multiplexing order.

Bits	Description	Type	Default
15:14	**QSGMII Tx Slot 1** The first slot after K28.1 00 = Port 0 01 = Port 1 10 = Port 2 11 = Port 3	R/W	00b
13:12	**QSGMII Tx Slot 2** The second slot after K28.1 00 = Port 0 01 = Port 1 10 = Port 2 11 = Port 3	R/W	01b
11:10	**QSGMII Tx Slot 3** The third slot after K28.1 00 = Port 0 01 = Port 1 10 = Port 2 11 = Port 3	R/W	10b
9:8	**QSGMII Tx Slot 4** The fourth slot after K28.1 00 = Port 0 01 = Port 1 10 = Port 2 11 = Port 3	R/W	11b
7:6	**QSGMII Rx Slot 1** The first slot after K28.1 00 = Port 0 01 = Port 1 10 = Port 2 11 = Port 3	R/W	00b
5:4	**QSGMII Rx Slot 2** The second slot after K28.1 00 = Port 0 01 = Port 1 10 = Port 2 11 = Port 3	R/W	01b
3:2	**QSGMII Rx Slot 3** The third slot after K28.1 00 = Port 0 01 = Port 1 10 = Port 2 11 = Port 3	R/W	10b

Bits	Description	Type	Default
1:0	**QSGMII Rx Slot 4** The fourth slot after K28.1 00 = Port 0 01 = Port 1 10 = Port 2 11 = Port 3	R/W	11b

2.1.32 QSGMII AUTO ANEG ENABLE REGISTER

Index (In decimal): EP 4.69 Size: 16 bits

This register enables the QSGMII interface to automatically come up running out of reset.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**QSGMII_AUTO_ANEG_ENA** *When this bit is 1, will automatically configure the QSGMII operation based on each GPHY IP speed status, then perform auto-negotiation over the QSGMII link.* 0 = QSGMII Auto ANEG not enabled 1 = QSGMII Auto ANEG enabled	R/W	1b

2.1.33 QSGMII SERDES RECEIVE LANE STATUS REGISTER

Index (In decimal): EP 4.128 Size: 16 bits

This register provides QSGMII SerDes receive lane status.

Bits	Description	Type	Default
15:3	**RESERVED**	RO	—
2	**RX_VALID** DPLL lock status 0 = Not locked 1 = Locked	RO	0b
1	**RX_PLL_STATE** Receive DPLL state 0 = Not in Power_Good state 1 = In Power_Good state	RO	0b
0	**SIG_DET** Receive signal detect 0 = Receive signal not detected 1 = Receive signal detected	RO	0b

2.1.34 QSGMII SERDES TRANSMIT LEVEL CONTROL REGISTER

Index (In decimal): EP 4.129 Size: 16 bits

This register provides QSGMII SerDes transmit level adjustment. QSGMII Soft Reset must be toggled in order for any value written to this register to take effect. See EP 4.67 for QSGMII Soft Reset.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:7	**TX_LEVEL[6:0]** This field sets the peak-to-peak differential output level of the transmitter driver output. The amplitude is specified in volts according to following formula: 1.33*TX_LEVEL[6:0]/64	R/W	7fh
6:0	**TX_BOOST[6:0]** This field sets the pre-emphasis level of the transmitter driver output. The amplitude is specified in decibels according to following formula: (TX_BOOST[6:0]+1)/4	R/W	0ah

2.1.35 QSGMII SERDES TRANSMIT GENERAL CONTROL REGISTER

Index (In decimal): EP 4.130 Size: 16 bits

This register provides general configuration for the QSGMII SerDes transmitter.

Bits	Description	Type	Default
15	**TX_VBOOST_EN** Enables the current mode Tx Swing boost 0 = Disabled 1 = Enabled	R/W	0b
14:12	**TX_VBOOST_LVL[2:0]** This field sets the launch amplitude of the transmit driver output.	R/W	100b
11	**TX_DISABLE_L0** 0 = Tx SerDes lane enabled 1 = Tx SerDes lane disabled	R/W	0b
10	**TX_DT_EN** Output driver enable 0 = Disabled 1 = Enabled	R/W	1b
9	**TX_RST** Transmitter reset 0 = Not reset 1 = Reset	R/W	0b
8	**TX_INV** Inverts the logic levels on the differential transmitter output 0 = Not inverted 1 = Inverted **Note:** This bit is inverted by default to align with the package pinout.	R/W	1b
7	**TX_DET_RX_REQ** When asserted, this bit initiates the Receiver_Detection operation. This bit should be set to 1 only when TX_DET_RX_ACK in the QSGMII SerDes Transmit Status Register is set to 0. When TX_DET_RX_ACK is set to 1, it should not be set to 0 until TX_DET_RX_ACK is set to 1.	R/W	0b
6	**TX_CM_EN** Transmit Common Mode enable 1 = Enable Transmit Common Mode to be held at half of vptx 0 = Disable Transmit Common Mode to be held at half of vptx. Transmit Common Mode will be weakly pulled to ground.	R/W	1b
5	**RESERVED**	RO	—
4:0	**TX_TERM_OFFSET[4:0]** Transmit termination offset This field applies an offset to the resistor calibration value. QSGMII Soft Reset must be toggled in order for any value written to this register to take effect. See EP 4.67 for QSGMII Soft Reset.	R/W	00h

2.1.36 QSGMII SERDES TRANSMIT STATUS REGISTER

Index (In decimal): EP 4.131 Size: 16 bits

This register provides status of the QSGMII SerDes transmitter.

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**TX_DET_RX_RESLT** Transmit Receiver_Detection result 0 = No receiver detected 1 = Receiver detected	RO	0b
2	**TX_DET_RX_ACK** Transmit Receiver_Detection acknowledgment When set to 1, this field indicates that the Receiver_Detection operation, requested by asserting TX_DET_RX_REQ, is complete. RX_DET_RX-_ACK is deasserted only when TX_DET_RX_REQ is deasserted.	RO	0b
1	**TX_CMNST** Transmit Common Mode State 0 = Transmit Common Mode level has not reached its intended value 1 = Transmit Common Mode level has reached its intended value	RO	0b
0	**TX_ST** Transmit Active State 0 = Transmitter is not active 1 = Transmitter is active. Transmitter has reached its intended level and is able to transmit data.	RO	0b

2.1.37 QSGMII SERDES RECEIVE EQUALIZATION CONTROL REGISTER

Index (In decimal): EP 4.133 Size: 16 bits

This register configures QSGMII SerDes receiver equalization.

Bits	Description	Type	Default
15:3	**RESERVED**	RO	—
2:0	**RX_EQ_VAL0[2:0]** This field controls the equalization boost level of the receiver	R/W	03h

2.1.38 QSGMII SERDES RECEIVE LOSS OF SIGNAL CONTROL REGISTER

Index (In decimal): EP 4.134 Size: 16 bits

This register configures the QSGMII SerDes receiver Loss of Signal detection.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6:0	**RX_LOS_FLTR[6:0]** This field provides the LOS filter value.	R/W	0Eh

2.1.39 QSGMII SERDES RECEIVE LEVEL CONTROL REGISTER

Index (In decimal): EP 4.136 Size: 16 bits

This register configures receiver levels for the QSGMII SerDes.

Bits	Description	Type	Default
15:13	**RESERVED**	RO	—
12:8	**ACJT_LEVEL[4:0]** Receiver sensitivity level control	R/W	00000b
7:5	**LOS_BIAS[2:0]** Loss of Signal detector threshold control A positive binary bit setting change results in a +15 mVp incremental change in the LOS threshold. A negative binary setting change results in a -15 mVp incremental change in the LOS threshold. The setting 3'b000 is reserved and must not be used.	R/W	001b
4:0	**LOS_LEVEL[4:0]** Loss of Signal detector sensitivity control	R/W	01001b

2.1.40 QSGMII SERDES MISCELLANEOUS CONTROL REGISTER

Index (In decimal): EP 4.137 Size: 16 bits

This register provides miscellaneous control for the QSGMII SerDes.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:5	**SSC_REF_CLK_SEL[8:0]** Spread Spectrum Reference Clock Shifting Control This field provides control to help non-standard oscillator frequencies generate targeted MPLL output rates.	R/W	000h
4	**LB_MODE** Analog loopback, from Tx serial output to Rx serial input. 0 = Loopback disabled 1 = Loopback enabled. LOS not detected when LB_MODE=1.	R/W	0b
3:2	**RX_RATE[1:0]** Selects receiver baud rate, as follows: 00 = mpll_baud_clk 01 = mpll_baud_clk/2 10 = mpll_baud_clk/4 11 = RESERVED	R/W	00b
1:0	**TX_RATE[1:0]** Selects transmitter baud rate, as follows: 00 = mpll_baud_clk 01 = mpll_baud_clk/2 10 = mpll_baud_clk/4 11 = RESERVED	R/W	00b

2.1.41 QSGMII SERDES CONTROL AND STATUS REGISTER

Index (In decimal): EP 4.138 Size: 16 bits

This register provides power-up/power-down control and status for the QSGMII SerDes.

Bits	Description	Type	Default
15:6	**RESERVED**	RO	—
5	**POWER_DOWN** 0 = Normal operation 1 = Power-down mode, turns off transmitter, receiver, and all clocks	R/W	0b
4	**PSAVE** 0 = Normal operation 1 = Power save mode, turns off transmitter and receiver	R/W	0b
3	**BYP_SEQ** 0 = The normal power-up flow is followed, where the PCS1G waits for SerDes PLLs to be stable before becoming operational. 1 = The normal power-up flow is bypassed, where the PCS1G does not wait for SerDes PLLs to be stable before becoming operational. This mode is useful mainly for emulation.	R/W	0b
2:0	PSEQ_STATE(2:0) This field indicates the state variable value of the power-up sequence module. 000 = Wait for MPLL On 001 = Wait for Tx Up 010 = Wait for Rx Up 011/100 = Tx/Rx Stable 101 = Wait for Rx Down (MPLL still ON) 110 = MPLL OFF 111 = Reserved	RO	—

2.1.42 QSGMII SERDES CR CONTROL REGISTER

Index (In decimal): EP 4.139 Size: 16 bits

The CR Control, Address, and Data Registers provide access to additional advanced SerDes registers. QSGMII Soft Reset must be toggled in order for any value written to this Transmitter Equalization Control group to take effect. See EP 4.67 for QSGMII Soft Reset.

Bits	Description	Type	Default
15:2	**RESERVED**	RO	—
1	**WR_RDN** This bit controls whether a Read or Write operation is to be performed 0 = Read 1 = Write	R/W	0b
0	**START_BUSY** Assert this bit to initiate a CR read or write transfer. The bit self-clears when the transfer is completed. This bit must be deasserted before writing to the CR Control Register, CR Address Register, or the CR Data Register. 0 = CR interface not busy 1 = CR interface busy	W1S/SC	0b

2.1.43 QSGMII SERDES CR ADDRESS REGISTER

Index (In decimal): EP 4.140 Size: 16 bits

The CR Control, Address, and Data Registers provide access to additional advanced SerDes registers. QSGMII Soft Reset must be toggled in order for any value written to this Transmitter Equalization Control group to take effect. See EP 4.67 for QSGMII Soft Reset.

Bits	Description	Type	Default
15:0	**ADDRESS [15:0]** This field provides the register address for the CR read or write transfer. This field must not be changed when START_BUSY is asserted.	R/W	0000h

2.1.44 QSGMII SERDES CR DATA REGISTER

Index (In decimal): EP 4.141 Size: 16 bits

The CR Control, Address, and Data Registers provide access to additional advanced SerDes registers. QSGMII Soft Reset must be toggled in order for any value written to this Transmitter Equalization Control group to take effect. See EP 4.67 for QSGMII Soft Reset.

Bits	Description	Type	Default
15:0	**DATA [15:0]** This field provides the data for the CR read or write transfer. This field must not be changed when START_BUSY is asserted.	R/W	0000h

2.1.45 QSGMII SERDES VREG_BYP STATUS REGISTER

Index (In decimal): EP 4.142 Size: 16 bits

This register provides the value of the VREG_BYP I/O pin, for test purposes.

Bits	Description	Type	Default
15:3	**RESERVED**	RO	—
4:3	**REFCLK_SEL[1:0]** Read-only status of the REFCLK_SEL[1:0] input pins 00 = SYSPLL ref is 25 MHz from XI/XO QSGMII ref is 25 MHz from XI/XO 01 = SYSPLL ref is 25 MHz from XI/XO QSGMII ref is from QSGMII_EXT_REF input pins 10 = SYSPLL ref is 25 MHz from CK125_REF_IN input pins QSGMII ref is 125 MHz from CK125_REF_IN input pins 11 = RESERVED	RO	—
2	**TX_MSB_TO_LSB** Controls Tx data bit order from QSGMII Extender to SerDes 1 = Swaps the Tx data bit order 0 = Does not swap the Tx data bit order	R/W	1b
1	**RX_MSB_TO_LSB** Controls Rx data bit order from SerDes to QSGMII Extender 1 = Swaps the Rx data bit order 0 = Does not swap the Rx data bit order	R/W	1b
0	**VREG_BYP** Read-only status of the VREG_BYPASS input pin 1 = SerDes will be powered directly from 2.5V (regulator bypassed) 0 = SerDes will be powered from internal 3.3V->2.5V regulator (regulator in use)	RO	—

2.1.46 RECOVERED CLOCK OUTPUT 1 SELECTOR REGISTER

Index (In decimal): EP 4.256 Size: 16 bits

This register configures the source for Recovered Clock Output 1. To use a Recovered Clock Input or Output it must be enabled as a GPIO Alternate Function.

Bits	Description	Type	Default
15:3	**RESERVED**	RO	—
2:0	**Recovered Clock Output 1 Selector [2:0]** This field selects the source for Recovered Clock Output 1. 000 = GPHY Port 0 001 = GPHY Port 1 010 = GPHY Port 2 011 = GPHY Port 3 100 = Recovered Clock Input 1 101 = Recovered Clock Input 2 110 = Reserved 111 = Zero. Forces Recovered Clock Output 1 to 0.	R/W	000b

2.1.47 RECOVERED CLOCK OUTPUT 1 DIVIDER REGISTER

Index (In decimal): EP 4.257 Size: 16 bits

This register configures the divider for Recovered Clock Output 1.

Bits	Description	Type	Default
15:6	**RESERVED**	RO	—
5:0	**Recovered Clock Output 1 Divider [5:0]** This field controls the divider for Recovered Clock Output 1. 000000 = Reserved 000001 = Output Clock frequency is the Input Clock Frequency divided by 1 | | 111111 = Output Clock frequency is the Input clock Frequency divided by 63	R/W	000001b

2.1.48 RECOVERED CLOCK OUTPUT 2 SELECTOR REGISTER

Index (In decimal): EP 4.258 Size: 16 bits

This register configures the source for Recovered Clock Output 2. To use a Recovered Clock Input or Output it must be enabled as a GPIO Alternate Function.

Bits	Description	Type	Default
15:3	**RESERVED**	RO	—
2:0	**Recovered Clock Output 2 Selector [2:0]** This field selects the source for Recovered Clock Output 2. 000 = GPHY Port 0 001 = GPHY Port 1 010 = GPHY Port 2 011 = GPHY Port 3 100 = Recovered Clock Input 1 101 = Recovered Clock Input 2 110 = Reserved 111 = Zero. Forces Recovered Clock Output 2 to 0.	R/W	000b

2.1.49 RECOVERED CLOCK OUTPUT 2 DIVIDER REGISTER

Index (In decimal): EP 4.259 Size: 16 bits

This register configures the divider for Recovered Clock Output 2.

Bits	Description	Type	Default
15:6	**RESERVED**	RO	—
5:0	**Recovered Clock Output 2 Divider [1:0]** This field controls the divider for Recovered Clock Output 2. 000000 = Reserved 000001 = Output Clock frequency is the Input Clock Frequency divided by 1 | | 111111 = Output Clock frequency is the Input clock Frequency divided by 63	R/W	000001b

2.1.50 1588 PLL RESET REGISTER

Index (In decimal): EP 4.320 Size: 16 bits

This register resets the 1588 PLL. The PLL core is in power-down mode during reset.

Note:	The 1588 PLL output is unstable for 50 µs following deassertion of reset. The 1588 PLL output clock should be gated inactive for this duration to ensure proper functioning of any logic using this clock.

It is recommended that either Bypass or Reset is asserted until all configuration controls are set to the desired working state, and the power and input reference clock are stable and within operating range, and the feedback path is functional.

Either Bypass or Reset may be used for power-down IDDQ testing.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**1588 PLL Reset** 1 = Reset the 1588 PLL Writing a zero has no effect.	W1S/SC	0b

2.1.51 1588 PLL BYPASS REGISTER

Index (In decimal): EP 4.321 Size: 16 bits

This register bypasses the 1588 PLL. The PLL core is in power-down mode during bypass.

Note:	The 1588 PLL output is unstable for 50 µs following deassertion of bypass. The 1588 PLL output clock should be gated inactive for this duration to ensure proper functioning of any logic using this clock.

It is recommended that either Bypass or Reset is asserted until all configuration controls are set to the desired working state, and the power and input reference clock are stable and within operating range, and the feedback path is functional.

Either Bypass or Reset may be used for power-down IDDQ testing.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**1588 PLL Bypass** 1 = Bypass the 1588 PLL 0 = Disable Bypass (normal PLL operation)	R/W	0b

2.1.52 1588 PLL STATUS REGISTER

Index (In decimal): EP 4.322 Size: 16 bits

This register provides the Lock status of the 1588 PLL. It is possible to configure an interrupt for the 1588 PLL transitioning from Locked to Out of Lock. See PTP_COMMON_INT_EN and PTP_COMMON_INT_STS for more details.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**1588 PLL Lock Status** 1 = The 1588 PLL is locked (normal PLL operation) 0 = The 1588 PLL is not locked (PLL Out of Lock)	RO	Note 1

Note 1: The default depends on the Lock state of the 1588 PLL.

2.1.53 1588 PLL DIVIDER REGISTER

Index (In decimal): EP 4.323 Size: 16 bits

This register controls the 1588 PLL dividers which configure the frequency of the internal 1588 clock. The default settings correspond to 125 MHz internal reference clock input and 250 MHz internal 1588 clock.

Note:	The 1588 PLL IP block FSE input pin should be tied off high (always use IP block feedback divider), and the FB input pin should be tied off low.

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14:10	**1588 PLL DIVR [4:0]** This field controls the input reference clock divider. The divided-down input reference frequency must be between 10 MHz and 200 MHz. 00000 = /1 00001 = /2 00010 = /3 | 11111 = /32	R/W	00100b
9:3	**1588 PLL DIVF [6:0]** This field controls the feedback reference clock divider (note there is an additional /2 divider hard-wired into the feedback path). The resulting VCO output frequency must be between 1000 MHz and 2000 MHz. 0000000 = /1 0000001 = /2 0000010 = /3 | 1111111 = /128	R/W	0010011b
2:0	**1588 PLL DIVQ [2:0]** This field controls the VCO output divider. The divided-down output frequency must be either 200 or 250 MHz. 000 = RESERVED 001 = /2 010 = /4 011 = /8 100 = /16 101 = /32 110 = /64 111 = RESERVED	R/W	010b

2.1.54 1588 PLL FILTER RANGE REGISTER

Index (In decimal): EP 4.324 Size: 16 bits

This register configures the 1588 PLL Filter range. It must be set to the range which includes the divided-down input reference frequency (PD_REF_IN). The default setting corresponds to 125 MHz internal reference clock input and 250 MHz internal 1588 clock.

Bits	Description	Type	Default
15:3	**RESERVED**	RO	—
2:0	**1588 PLL Range [2:0]** This field controls the 1588 PLL Filter range. 000 = Bypass 001 = RESERVED 010 = PD_REF_IN is 10-16 MHz 011 = PD_REF_IN is 16-26 MHz 100 = PD_REF_IN is 26-42 MHz 101 = PD_REF_IN is 42-68 MHz 110 = PD_REF_IN is 68-110 MHz 111 = PD_REF_IN is 110-200 MHz	R/W	011b

2.1.55 AB PVT CONTROL REGISTER 1

Index (In decimal): EP 4.384 Size: 16 bits

This register provides control of the AB PVT IP.

Bits	Description	Type	Default
15:13	**RESERVED**	RO	—
12:8	**SEL_TRIM[4:0]** TRIM[4:0] input pins of the AB PVT IP	R/W	01111b
7	**PROBE_VREG_EN** PROBE_VREG_ENA input pin of the AB PVT IP	R/W	0b
6:5	**SEL_VSEL[1:0]** Selects the VIN[3:0] input, this is an input to the VSEL[1:0] input pins of the AB PVT IP	R/W	00b
4	**SEL_VSAMPLE** Select for the Voltage Sample mode VSAMPLE input pin of the AB PVT IP	R/W	0b
3:2	**SEL_PSAMPLE[1:0]** Select for the Process Sample mode PSAMPLE[1:0] input pins of the AB PVT IP	R/W	00b
1	**PVT_EN** If SEL_ENA =1, this is connected to the ENA input pin of the AB PVT IP.	R/W	0b
0	**SEL_ENA** Selects if the ENA input pin to the AB PVT IP is controlled by HW or SW. 0 = ENA is controlled by HW 1 = ENA is controlled by SW	R/W	1b

2.1.56 AB PVT CONTROL REGISTER 2

Index (In decimal): EP 4.385 Size: 16 bits

This register controls the VTRIM inputs of the AB PVT IP.

Bits	Description	Type	Default
15:6	**RESERVED**	RO	—
5:0	**SEL_VTRIM[5:0]** VTRIM[5:0] input pins of the AB PVT IP	R/W	000000b

2.1.57 AB PVT STATUS REGISTER

Index (In decimal): EP 4.386 Size: 16 bits

This register provides status from the AB PVT IP.

Bits	Description	Type	Default
15:5	**RESERVED**	RO	—
4	**THERM2_THR_MATCH** Thermal Threshold 2 Match. Thermal overload mode signal.	RO	0b
3	**THERM1_THR_MATCH** Thermal Threshold 1 Match. Thermal warning mode signal.	RO	0b
2	**THERM0_THR_MATCH** Thermal Threshold 0 Match. Thermal warning mode signal with hysteresis.	RO	0b
1	**DATA_VALID_STAT** DATA_VALID output pin of the AB PVT IP	RO	0b
0	**ENA_STAT** Value of the ENA input pin of the AB PVT IP	RO	0b

2.1.58 AB PVT INTERRUPT STATUS REGISTER

Index (In decimal): EP 4.388 Size: 16 bits

This register provides interrupt status associated with the AB PVT IP.

Bits	Description	Type	Default
15:5	**RESERVED**	RO	—
4	**THERM2_CHANGE_INT** 1 = Change in value of THERM2_THR_MATCH 0 = No change in value of THERM2_THR_MATCH	R/W1C	0b
3	**THERM1_CHANGE_INT** 1 = Change in value of THERM1_THR_MATCH 0 = No change in value of THERM1_THR_MATCH	R/W1C	0b
2	**THERM0_CHANGE_INT** 1 = Change in value of THERM0_THR_MATCH 0 = No change in value of THERM0_THR_MATCH	R/W1C	0b
1	**DATA_VALID_INT** 1 = Change in value of DATA_VALID_STAT 0 = No change in value of DATA_VALID_STAT	R/W1C	0b
0	**ENA_INT** 1 = Change in value of ENA_STAT 0 = No change in value of ENA_STAT	R/W1C	0b

2.1.59 AB PVT INTERRUPT MASK REGISTER

Index (In decimal): EP 4.390 Size: 16 bits

This register provides interrupt control associated with the AB PVT IP.

Bits	Description	Type	Default
15:5	**RESERVED**	RO	—
4	**THERM2_CHANGE_MSK** When set to 0 generates an interrupt when THERM2_CHANGE_INT is set.	R/W	1b
3	**THERM1_CHANGE_MSK** When set to 0 generates an interrupt when THERM1_CHANGE_INT is set.	R/W	1b
2	**THERM0_CHANGE_MSK** When set to 0 generates an interrupt when THERM0_CHANGE_INT is set.	R/W	1b
1	**DATA_VALID_MSK** When set to 0 generates an interrupt when DATA_VALID_INT is set.	R/W	1b
0	**ENA_STAT_MSK** When set to 0 generates an interrupt when ENA_INT is set.	R/W	1b

2.1.60 AB PVT DATA REGISTER

Index (In decimal): EP 4.392 Size: 16 bits

This register provides the Data output (die process, voltage or temperature) of the AB PVT IP.

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9:0	**PVT_DATA[9:0]** The last sensed value from the DATA_OUT[9:0] pins of the AB PVT IP	RO	000h

2.1.61 AB PVT SAMPLE TIME REGISTER

Index (In decimal): EP 4.394 Size: 16 bits

This register controls the hardware sampling of the AB PVT IP.

Bits	Description	Type	Default
15:0	**SAMPLE_TIME[15:0]** Time between samples taken from the AB PVT IP. 0000h = HW takes a sample whenever DATA_VALID is asserted 0001h-FFFFh: sample time in ms	R/W	0000h

2.1.62 AB PVT THERMAL COMPARATOR CONTROL REGISTER

Index (In decimal): EP 4.396 Size: 16 bits

This register controls the Thermal Comparator associated with the AB PVT IP.

Bits	Description	Type	Default
15:2	**RESERVED**	RO	—
1:0	**THERM_COMP_CTL[1:0]** This field controls the Thermal Comparator. It is sampled every 100 µs. 00 = Comparator is disabled 01 = Comparator is enabled 10 = RESERVED 11 = RESERVED	R/W	00b

2.1.63 AB PVT THERMAL COMPARATOR THRESHOLD 0 REGISTER

Index (In decimal): EP 4.398 Size: 16 bits

This register contains the Thermal Comparator Threshold 0.

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9:0	**THERM0_CMP_THRESHOLD[9:0]** Comparator threshold value, units are 2.5V/1024.	R/W	000h

2.1.64 AB PVT THERMAL COMPARATOR THRESHOLD 1 REGISTER

Index (In decimal): EP 4.400 Size: 16 bits

This register contains the Thermal Comparator Threshold 1.

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9:0	**THERM1_CMP_THRESHOLD[9:0]** Comparator threshold value, units are 2.5V/1024.	R/W	000h

2.1.65 AB PVT THERMAL COMPARATOR THRESHOLD 2 REGISTER

Index (In decimal): EP 4.402 Size: 16 bits

This register contains the Thermal Comparator Threshold 2.

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9:0	**THERM2_CMP_THRESHOLD[9:0]** Comparator threshold value, units are 2.5V/1024.	R/W	000h

2.1.66 AB PVT SAMPLE CLOCK DIVIDER REGISTER

Index (In decimal): EP 4.404 Size: 16 bits

This register is used with the AB PVT Clock Divider Register to generate the 1 kHz AB PVT sampling clock. SAMPLE_-CLK_DIV provides the divisor value to divide the 1.15-1.25 MHz AB PVT clock down to 1 kHz.

Bits	Description	Type	Default
15:0	**SAMPLE_CLK_DIV[15:0]** Value is set based on frequency of AB PVT sampling clock, as follows. AB PVT sampling clock = 1.15 MHz, SAMPLE_CLK_DIV = ‘d1150 (047Eh) | AB PVT sampling clock = 1.25 MHz, SAMPLE_CLK_DIV = ‘d1250 (04E2h)	R/W	047Eh

2.1.67 AB PVT PSEL25 REGISTER

Index (In decimal): EP 4.406 Size: 16 bits

This register controls whether the AB PVT IP runs from 2.5V or 3.3V.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**PSEL_25** Controls whether the AB PVT IP runs from 2.5V or 3.3V. The default is 3.3V, set this bit to 1 if VDDAH is connected to 2.5V. 0 = VDDAH is connected to 3.3V 1 = VDDAH is connected to 2.5V ***Caution:*** *Do not set this bit to 1 if VDDAH is connected to 3.3V, as damage to the chip may result.*	R/W	0b

2.1.68 AB PVT HARD RESET REGISTER

Index (In decimal): EP 4.407 Size: 16 bits

This register resets the AB PVT and sets all related configuration registers to their default state.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**AB PVT Hard Reset** 1 = Reset the AB PVT and set all configuration registers to their default state Writing a zero has no effect.	W1S/SC	0b

2.1.69 AB PVT SOFT RESET REGISTER

Index (In decimal): EP 4.408 Size: 16 bits

This register resets the AB PVT but does not reset any configuration registers.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**AB PVT Soft Reset** 1 = Reset the AB PVT except all configuration registers Writing a zero has no effect	W1S/SC	0b

2.1.70 AB PVT CLOCK DIVIDER REGISTER

Index (In decimal): EP 4.409 Size: 16 bits

This register is used with the AB PVT Sample Clock Divider Register to generate the AB PVT clocks. PVT_CLK_DIV provides the divisor value to divide the 125 MHz to the required range of 1.15-1.25 MHz.

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**PVT_CLK_DIV[7:0]** Value is set based on desired value of AB PVT sampling clock, as follows. Assuming 125 MHz system clock: PVT_CLK_DIV = ‘d100 (64h) results in AB PVT clock frequency of 1.25 MHz | PVT_CLK_DIV = ‘d108 (6Ch) results in AB PVT clock frequency of 1.157 MHz	R/W	6Ch

2.1.71 PTP COMMAND AND CONTROL REGISTER (PTP_CMD_CTL)

Index (In decimal): EP 4.512 Size: 16 bits

Bits	Description	Type	Default
15	**LTC Delayed Step Seconds (PTP_LTC_DLYD_STEP_SECONDS)** Writing a one to this bit arms the adding or subtracting of the lower four bits of the LTC Step Adjustment Value (PTP_LTC_STEP_ADJ_VALUE) field in the PTP LTC Step Adjustment Low Register (PTP_LTC_STEP_ADJ_LO) to or from the seconds portion of the 1588 Local Time Counter. The choice of adding or subtracting is set using the LTC Step Adjustment Direction (PTP_LTC_STEP_ADJ_DIR) bit. Once armed, the 1588 Local Time Counter is adjusted when the Local Time Counter nanoseconds rolls over to or past zero. This bit self-clears at that time. Writing a zero to this bit has no effect. This action is only valid when **PTP_LTC_TEMP_RATE_SEL** = 0.	W1S/SC	0b

Bits	Description	Type	Default
14	**LTC Delayed Load (PTP_LTC_DLYD_LOAD)** Writing a one to this bit arms the delayed writing of the value of the PTP LTC Set Seconds High/Mid/Low Registers (PTP_LTC_SET_SEC_HI/MID/LO), the PTP LTC Set Nanoseconds High/Low Registers (PTP_LTC_SET_NS_HI/LO) and the PTP LTC Set Sub-Nanoseconds High/Low Registers (PTP_LTC_SET_SUBNS_HI/LO) into the 1588 Local Time Counter. Once armed, the 1588 Local Time Counter is loaded when the Local Time Counter nanoseconds rolls over to or past zero. This bit self-clears at that time. Writing a zero to this bit has no effect. This action is only valid when **PTP_LTC_TEMP_RATE_SEL** = 0.	W1S/SC	0b
13	**LTC Target Read (PTP_LTC_TARGET_READ)** Writing a one to this bit causes the current values of both of the 1588 Local Time targets (A and B) to be saved into the PTP LTC Target x Seconds High/Low Registers (PTP_LTC_TARGET_SEC_HI/LO_x) and the PTP LTC Target x Nanoseconds High/Low Registers (PTP_LTC_TARGET_NS_HI/LO_x) so they can be read. Writing a zero to this bit has no effect.	W1S/SC	0b
12:9	**PTP Manual Capture Select 3-0 (PTP_MANUAL_CAPTURE_SEL[3:0])** These bits specify which PTP GPIO Capture Register set is used during a manual capture. Bit 3 selects the rising edge or falling edge registers: 0 = Rising edge 1 = Falling edge Bits 2:0 select PTP GPIO Capture Register set number: 000 = PTP GPIO Capture Register set 0 | 111 = PTP GPIO Capture Register set 7 **Note:** All eight PTP GPIO Capture Register sets are available.	R/W	0000b
8	**PTP Manual Capture (PTP_MANUAL_CAPTURE)** Writing a one to this bit causes the current value of the 1588 Local Time Counter to be saved into the PTP GPIO Capture Register set specified above. The bit corresponding to the GPIO pin (not the PTP GPIO Capture Register set) in the PTP Common Interrupt Status Register (PTP_COMMON_INT_STS) is also set. Writing a zero to this bit has no effect.	W1S/SC	0b
7	**LTC Temporary Rate (PTP_LTC_TEMP_RATE)** Writing a one to this bit enables the use of the temporary Local Time rate adjustment specified in the PTP LTC Temporary Rate Adjustment High/Low Registers (PTP_LTC_TEMP_RATE_ADJ_HI/LO) for the duration specified in the PTP LTC Temporary Rate Duration High/Low Registers (PTP_LTC_TEMP_RATE_DURATION_HI/LO). Writing a zero to this bit has no effect. This action is only valid when **PTP_LTC_TEMP_RATE_SEL** = 0.	W1S/SC	0b

Bits	Description	Type	Default
6	**LTC Step Nanoseconds (PTP_LTC_STEP_NANOSECONDS)** Writing a one to this bit adds the value of the LTC Step Adjustment Value (PTP_LTC_STEP_ADJ_VALUE) field in the PTP LTC Step Adjustment High/Low Registers (PTP_LTC_STEP_ADJ_HI/LO) to the nanoseconds portion of the 1588 Local Time Counter. Writing a zero to this bit has no effect. This action is only valid when **PTP_LTC_TEMP_RATE_SEL** = 0.	W1S/SC	0b
5	**LTC Step Seconds (PTP_LTC_STEP_SECONDS)** Writing a one to this bit adds or subtracts the lower four bits of the LTC Step Adjustment Value (PTP_LTC_STEP_ADJ_VALUE) field in the PTP LTC Step Adjustment Low Register (PTP_LTC_STEP_ADJ_LO) to or from the seconds portion of the 1588 Local Time Counter. The choice of adding or subtracting is set using the LTC Step Adjustment Direction (PTP_LTC_-STEP_ADJ_DIR) bit. Writing a zero to this bit has no effect. This action is only valid when **PTP_LTC_TEMP_RATE_SEL** = 0.	W1S/SC	0b
4	**LTC Load (PTP_LTC_LOAD)** Writing a one to this bit writes the value of the PTP LTC Set Seconds High/Mid/Low Registers (PTP_LTC_SET_SEC_HI/MID/LO), the PTP LTC Set Nanoseconds High/Low Registers (PTP_LTC_SET_NS_HI/LO) and the PTP LTC Set Sub-Nanoseconds High/Low Registers (PTP_LTC_SET_-SUBNS_HI/LO) into the 1588 Local Time Counter. Writing a zero to this bit has no effect. This action is only valid when **PTP_LTC_TEMP_RATE_SEL** = 0.	W1S/SC	0b
3	**LTC Read (PTP_LTC_READ)** Writing a one to this bit causes the current value of the 1588 Local Time Counter to be saved into the PTP LTC Read Seconds High/Mid/Low Registers (PTP_LTC_RD_SEC_HI/MID/LO), the PTP LTC Read Nanoseconds High/Low Registers (PTP_LTC_RD_NS_HI/LO) and the PTP LTC Read Sub-Nanoseconds High/Low Registers (PTP_LTC_RD_SUBNS_HI/LO) so it can be read. Writing a zero to this bit has no effect.	W1S/SC	0b
2	**LTC Temporary Rate Adjust Select (PTP_LTC_TEMP_RATE_SEL)** This field controls whether LTC adjustment is performed by software or external pin (GPIO or ePPS). 0 = LTC adjust is software-controlled using PTP_LTC_TEMP_RATE 1 = LTC adjust is externally controlled using 1588_LD_ADJ or ePPS. See the PTP_LTC_EXT_ADJ_CFG register for more details.	R/W	0b
1	**PTP Enable (PTP_ENABLE)** Writing a one to this bit will enable the 1588 LTC and TSUs. Reading this bit will return the current enabled value. Writing a zero to this bit has no effect. (moved from Pfeiffer MMD 2.256)	R/W1S	0b

Bits	Description	Type	Default
0	**PTP Disable (PTP_DISABLE)** Writing a one to this bit will cause the PTP Enable (PTP_ENABLE) to clear once all current frame processing is completed. No new frame processing will be started if this bit is set. Writing a zero to this bit has no effect. (moved from Pfeiffer MMD 2.256)	W1S/SC	0b

2.1.72 PTP GENERAL CONFIGURATION REGISTER (PTP_GENERAL_CONFIG)

Index (In decimal): EP 4.513 Size: 16 bits

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:8	**Local Time Event Channel B Mode (LTC_EVENT_B[3:0])** These bits determine the output on Local Time Event Channel B when a Local Time Target compare event occurs. 0000 = 100 ns 0001 = 500 ns 0010 = 1 µs 0011 = 5 µs 0100 = 10 µs 0101 = 50 µs 0110 = 100 µs 0111 = 500 µs 1000 = 1 ms 1001 = 5 ms 1010 = 10 ms 1011 = 50 ms 1100 = 100 ms 1101 = 200 ms 1110 = Toggle 1111 = PTP_TIMER_INT_B bit value in the PTP_COMMON_INT_STS register	R/W	00b

Bits	Description	Type	Default
7:4	**Local Time Event Channel A Mode (LTC_EVENT_A[3:0])** These bits determine the output on Local Time Event Channel A when a Local Time Target compare event occurs. 0000 = 100 ns 0001 = 500 ns 0010 = 1 µs 0011 = 5 µs 0100 = 10 µs 0101 = 50 µs 0110 = 100 µs 0111 = 500 µs 1000 = 1 ms 1001 = 5 ms 1010 = 10 ms 1011 = 50 ms 1100 = 100 ms 1101 = 200 ms 1110 = Toggle 1111 = PTP_TIMER_INT_A bit value in the PTP_COMMON_INT_STS register	R/W	00b
3	**Local Time Event Polarity Channel B (LTC_EVENT_POL_B)** This bit determines the output polarity of Local Time Event Channel B. 0 = Active low 1 = Active high **Note:** The polarity applies to all event modes including the Toggle mode.	R/W	0b
2	**Reload/Add B (RELOAD_ADD_B)** This bit determines the course of action when a Local Time Target compare event for Local Time Event Channel B occurs. When set, the PTP LTC Target x Seconds High/Low Registers (PTP_LTC_TARGET_SEC_HI/LO_x) and PTP LTC Target x Nanoseconds High/Low Registers (PTP_LTC_TARGET_NS_HI/LO_x) are loaded from the PTP LTC Target x Reload/Add Seconds High/Low Registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x) and PTP LTC Target x Reload/Add Nanoseconds High/Low Registers (PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) x = B. When low, the Local Time Target Registers are incremented by the Local Time Target Reload Registers. 0 = Increment upon a Local Time target compare event 1 = Reload upon a Local Time target compare event	R/W	0b
1	**Local Time Event Polarity Channel A (LTC_EVENT_POL_A)** This bit determines the output polarity of Local Time Event Channel A. 0 = Active low 1 = Active high **Note:** The polarity applies to all event modes including the Toggle mode.	R/W	0b

Bits	Description	Type	Default
0	**Reload/Add A (RELOAD_ADD_A)** This bit determines the course of action when a Local Time Target compare event for Local Time Event Channel A occurs. When set, the PTP LTC Target x Seconds High/Low Registers (PTP_LTC_TARGET_SEC_HI/LO_x) and PTP LTC Target x Nanoseconds High/Low Registers (PTP_LTC_TARGET_NS_HI/LO_x) are loaded from the PTP LTC Target x Reload/Add Seconds High/Low Registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x) and PTP LTC Target x Reload/Add Nanoseconds High/Low Registers (PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) x = A. When low, the Local Time Target Registers are incremented by the Local Time Target Reload Registers. 0 = Increment upon a Local Time target compare event 1 = Reload upon a Local Time target compare event	R/W	0b

To use Local Time Event A/B the appropriate pins must be enabled as GPIO Alternate Functions.

Note: Local Time Event A/B can be configured to operate as a PPS output.

2.1.73 PTP REFERENCE CLOCK CONFIGURATION REGISTER (PTP_REF_CLK_CFG)

Index (In decimal): EP 4.514 Size: 16 bits

This read/write register configures the 1588 reference clock.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13	**Embedded 1PPS Enable (EPPS_ENABLE)** This bit enables ePPS operation on the 1588_REF_CLK input pin. ePPS is only supported with external 25 MHz 1588 reference clock. 0 = ePPS disabled 1 = ePPS enabled **Note:** This bit is only valid when the Reference Clock Source field is set to External 1588_REF_CLK.	R/W	0b
12:10	**Reference Clock Source [2:0]** This field selects the clock which is used as the 1588 PLL reference clock. 000 = 125 MHz clock from internal System PLL 001 = 125 MHz QSGMII recovered clock 010 = External 1588_REF_CLK (can be 10 MHz, 25 MHz, or 125 MHz) 011 = RESERVED 100 = Recovered clock from Port 0 Rx (can be 25 MHz or 125 MHz) 101 = Recovered clock from Port 1 Rx (can be 25 MHz or 125 MHz) 110 = Recovered clock from Port 2 Rx (can be 25 MHz or 125 MHz) 111 = Recovered clock from Port 3 Rx (can be 25 MHz or 125 MHz) **Note 1:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit is set. **2:** Recovered port timing is only supported for 1G or 100M port speeds. (This field definition is changed from Pfeiffer)	R/W	000b
9	**Reference Clock Period Override** This field must be set to 1b. When clear, the period of the reference clock is determined by the H/W based on the source selection and the current receive data rate if needed. When set, the period of the reference clock is specified by the value in the Reference Clock Period field. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit is set.	R/W	1b
8:0	**Reference Clock Period [8:0]** This field specifies the period, in nanoseconds, of the reference clock. Valid values are 4 (250 MHz) and 5 (200 Mhz). **Note 1:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit is set. **2:** The Reference Clock Source and Reference Clock Period Override bits must be set prior to updating this field.	R/W	004h

2.1.74 PTP COMMON INTERRUPT STATUS REGISTER (PTP_COMMON_INT_STS)

Index (In decimal): EP 4.515 Size: 16 bits

This register contains the 1588 Common interrupt status bits.

Reading this register clears the interrupt sources. RO sources must be cleared at their lower level register.

If enabled in the PTP Common Interrupt Enable Register (PTP_COMMON_INT_EN), these interrupt bits are cascaded into the 1588 Common Interrupt bit of the Chip-Level Interrupt Status Register. Status bits will still reflect the status of the interrupt source regardless of whether the source is enabled as an interrupt.

Note: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneous event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**1588 PLL Lock State** This interrupt indicates that the Lock State of the 1588 PLL has changed	RC	0b
2	**PTP GPIO Capture Interrupt (PTP_GPIO_CAP_INT)** This interrupt indicates that a GPIO capture event occurred and its time stored.	RO	0b
1	**PTP Timer Interrupt B (PTP_TIMER_INT_B)** This interrupt indicates that the 1588 Local Time Counter equaled or passed the Local Time Event Channel B Local Time Target value. **Note:** This bit is also cleared by an active edge on a GPIO if enabled.	RC	0b
0	**PTP Timer Interrupt A (PTP_TIMER_INT_A)** This interrupt indicates that the 1588 Local Time equaled or passed the Local Time Event Channel A Local Time Target value. **Note:** This bit is also cleared by an active edge on a GPIO if enabled.	RC	0b

2.1.75 PTP COMMON INTERRUPT ENABLE REGISTER (PTP_COMMON_INT_EN)

Index (In decimal): EP 4.516 Size: 16 bits

This register enables the corresponding bits in the PTP Common Interrupt Status Register (PTP_COMMON_INT_STS).

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**1588 PLL Lock State Enable**	R/W	0b
2	**PTP GPIO Capture Interrupt Enable (PTP_GPIO_CAP_EN)**	R/W	0b
1	**PTP Timer B Interrupt Enable (PTP_TIMER_EN_B)**	R/W	0b
0	**PTP Timer A Interrupt Enable (PTP_TIMER_EN_A)**	R/W	0b

2.1.76 PTP LTC SET SECONDS HIGH REGISTER (PTP_LTC_SET_SEC_HI)

Index (In decimal): EP 4.517 Size: 16 bits

This register contains the upper 16 bits of the seconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set, or when GPIO load is triggered (enabled using LTC LOAD EXTERNAL ENABLE).

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[47:32])** This field contains the upper 16 bits of the seconds portion of the 1588 Local Time Counter.	R/W	0000h

2.1.77 PTP LTC SET SECONDS MID REGISTER (PTP_LTC_SET_SEC_MID)

Index (In decimal): EP 4.518 Size: 16 bits

This register contains the middle 16 bits of the seconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set, or when GPIO load is triggered (enabled using LTC LOAD EXTERNAL ENABLE).

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[31:16])** This field contains the middle 16 bits of the seconds portion of the 1588 Local Time Counter.	R/W	0000h

2.1.78 PTP LTC SET SECONDS LOW REGISTER (PTP_LTC_SET_SEC_LO)

Index (In decimal): EP 4.519 Size: 16 bits

This register contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set, or when GPIO load is triggered (enabled using LTC LOAD EXTERNAL ENABLE).

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[15:0])** This field contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter.	R/W	0000h

2.1.79 PTP LTC SET NANOSECONDS HIGH REGISTER (PTP_LTC_SET_NS_HI)

Index (In decimal): EP 4.520 Size: 16 bits

This register contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set, or when GPIO load is triggered (enabled using LTC LOAD EXTERNAL ENABLE).

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:0	**LTC Nanoseconds (PTP_LTC_NS[29:16])** This field contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter.	R/W	0000h

2.1.80 PTP LTC SET NANOSECONDS LOW REGISTER (PTP_LTC_SET_NS_LO)

Index (In decimal): EP 4.521 Size: 16 bits

This register contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set, or when GPIO load is triggered (enabled using LTC LOAD EXTERNAL ENABLE).

Bits	Description	Type	Default
15:0	**LTC Nanoseconds (PTP_LTC_NS[15:0])** This field contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter.	R/W	0000h

2.1.81 PTP LTC SET SUB-NANOSECONDS HIGH REGISTER (PTP_LTC_SET_SUBNS_HI)

Index (In decimal): EP 4.522 Size: 16 bits

This register contains the upper 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set, or when GPIO load is triggered (enabled using LTC LOAD EXTERNAL ENABLE).

Bits	Description	Type	Default
15:0	**LTC Sub-Nanoseconds (PTP_LTC_SUBNS[31:16])** This field contains the upper 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter.	R/W	0000h

2.1.82 PTP LTC SET SUB-NANOSECONDS LOW REGISTER (PTP_LTC_SET_SUBNS_LO)

Index (In decimal): EP 4.523 Size: 16 bits

This register contains the lower 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set, or when GPIO load is triggered (enabled using LTC LOAD EXTERNAL ENABLE).

Bits	Description	Type	Default
15:0	**LTC Sub-Nanoseconds (PTP_LTC_SUBNS[15:0])** This field contains the lower 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter.	R/W	0000h

2.1.83 PTP LTC RATE ADJUSTMENT HIGH REGISTER (PTP_LTC_RATE_ADJ_HI)

Index (In decimal): EP 4.524 Size: 16 bits

This register along with the PTP LTC Rate Adjustment Low Register (PTP_LTC_RATE_ADJ_LO) is used to adjust the rate of the 1588 Local Time Counter. This register contains the upper 14 bits of the rate adjustment value and the adjustment direction bit.

Bits	Description	Type	Default
15	**LTC Rate Adjustment Direction (PTP_LTC_RATE_ADJ_DIR)** This field specifies if the 1588 Rate Adjustment causes the 1588 Local Time Counter to be faster or slower than the reference clock. 0 = Slower (1588 Local Time Counter increments by 1 ns less) 1 = Faster (1588 Local Time Counter increments by 1 ns more)	R/W	0b
14	**RESERVED**	RO	—
13:0	**LTC Rate Adjustment Value (PTP_LTC_RATE_ADJ_VALUE[29:16])** This field indicates an adjustment to the reference clock period of the 1588 Local Time Counter in units of 2^{-32} ns. On each reference clock cycle, this value is added to the 32-bit sub-nanoseconds portion of the 1588 Local Time Counter. When the sub-nanoseconds portion rolls over past zero, the 1588 Local Time Counter will be adjusted by 1 ns.	R/W	0000h

Note: Both registers (PTP_LTC_RATE_ADJ_LO/HI) must be written for either to be affected.

2.1.84 PTP LTC RATE ADJUSTMENT LOW REGISTER (PTP_LTC_RATE_ADJ_LO)

Index (In decimal): EP 4.525 Size: 16 bits

This register contains the lower 16 bits of the rate adjustment value.

Bits	Description	Type	Default
15:0	**LTC Rate Adjustment Value (PTP_LTC_RATE_ADJ_VALUE[15:0])** This field indicates an adjustment to the reference clock period of the 1588 Local Time Counter in units of 2^{-32} ns. On each reference clock cycle, this value is added to the 32-bit sub-nanoseconds portion of the 1588 Local Time Counter. When the sub-nanoseconds portion rolls over past zero, the 1588 Local Time Counter will be adjusted by 1 ns.	R/W	0000h

Note: Both registers (PTP_LTC_RATE_ADJ_LO/HI) must be written for either to be affected.

2.1.85 PTP LTC TEMPORARY RATE ADJUSTMENT HIGH REGISTER (PTP_LTC_TEMP_RATE_ADJ_HI)

Index (In decimal): EP 4.526 Size: 16 bits

This register along with the PTP LTC Temporary Rate Adjustment Low Register (PTP_LTC_TEMP_RATE_ADJ_LO) is used to adjust the rate of the 1588 Local Time Counter. Every reference clock period, 1588 Local Time Counter is normally incremented by the reference clock period value. This register is used to occasionally change that increment by 1 ns additional or one less. This register contains the upper 14 bits of the temporary rate adjustment value and the adjustment direction bit.

Bits	Description	Type	Default
15	**LTC Temporary Rate Adjustment Direction (PTP_LTC_TEMP_RATE_ADJ_DIR)** This field specifies if the 1588 Temporary Rate Adjustment causes the 1588 Local Time Counter to be faster or slower than the reference clock. 0 = Slower (1588 Local Time Counter increments by 1 ns less) 1 = Faster (1588 Local Time Counter increments by 1 ns more)	R/W	0b
14	**RESERVED**	RO	—
13:0	**LTC Temporary Rate Adjustment Value (PTP_LTC_TEMP_RATE_ADJ_VALUE[29:16])** This field indicates a temporary adjustment to the reference clock period of the 1588 Local Time Counter in units of 2^{-32} ns. On each reference clock cycle, this value is added to the 32-bit sub-nanoseconds portion of the 1588 Local Time Counter. When the sub-nanoseconds portion rolls over past zero, the 1588 Local Time Counter will be adjusted by 1 ns.	R/W	0000h

2.1.86 PTP LTC TEMPORARY RATE ADJUSTMENT LOW REGISTER (PTP_LTC_TEMP_RATE_ADJ_LO)

Index (In decimal): EP 4.527 Size: 16 bits

This register contains the lower 16 bits of the temporary rate adjustment value.

Bits	Description	Type	Default
15:0	**LTC Temporary Rate Adjustment Value (PTP_LTC_TEMP_RATE_ADJ_VALUE[15:0])** This field indicates a temporary adjustment to the reference clock period of the 1588 Local Time Counter in units of 2^{-32} ns. On each reference clock cycle, this value is added to the 32-bit sub-nanoseconds portion of the 1588 Local Time Counter. When the sub-nanoseconds portion rolls over past zero, the 1588 Local Time Counter will be adjusted by 1 ns.	R/W	0000h

2.1.87 PTP LTC TEMPORARY RATE DURATION HIGH REGISTER (PTP_LTC_TEMP_RATE_DURATION_HI)

Index (In decimal): EP 4.528 Size: 16 bits

This register along with the PTP LTC Temporary Rate Duration Low Register (PTP_LTC_TEMP_RATE_DURATION_LO) specifies the active duration of the temporary rate adjustment. This register contains the upper 16 bits of the temporary rate duration value.

Bits	Description	Type	Default
15:0	**LTC Temporary Rate Duration (PTP_LTC_TEMP_RATE_DURATION[31:16])** This field specifies the duration of the temporary rate adjustment in reference clock cycles.	R/W	0000h

2.1.88 PTP LTC TEMPORARY RATE DURATION LOW REGISTER (PTP_LTC_TEMP_RATE_DURATION_LO)

Index (In decimal): EP 4.529 Size: 16 bits

This register contains the lower 16 bits of the temporary rate duration value.

Bits	Description	Type	Default
15:0	**LTC Temporary Rate Duration (PTP_LTC_TEMP_RATE_DURATION[15:0])** This field specifies the duration of the temporary rate adjustment in reference clock cycles.	R/W	0000h

2.1.89 PTP LTC STEP ADJUSTMENT HIGH REGISTER (PTP_LTC_STEP_ADJ_HI)

Index (In decimal): EP 4.530 Size: 16 bits

This register along with the PTP LTC Step Adjustment Low Register (PTP_LTC_STEP_ADJ_LO) is used to perform a one-time adjustment to either the seconds portion or the nanoseconds portion of the 1588 Local Time Counter. The amount and direction can be specified. This register contains the upper 14 bits of the step adjustment value and the step adjustment direction bit.

Bits	Description	Type	Default
15	**LTC Step Adjustment Direction (PTP_LTC_STEP_ADJ_DIR)** This field specifies if the LTC Step Adjustment Value (PTP_LTC_STEP_ADJ_VALUE[29:16]) is added to or subtracted from the 1588 Local Time Counter. 0 = Subtracted 1 = Added **Note:** Only addition is supported for the nanoseconds portion of the 1588 Local Time Counter.	R/W	0b
14	**RESERVED**	RO	—
13:0	**LTC Step Adjustment Value (PTP_LTC_STEP_ADJ_VALUE[29:16])** When the nanoseconds portion of the 1588 Local Time Counter is being adjusted, this field specifies the amount to add. This is in lieu of the normal reference clock period increment. When the seconds portion of the 1588 Local Time Counter is being adjusted, this field is not used.	R/W	0000h

2.1.90 PTP LTC STEP ADJUSTMENT LOW REGISTER (PTP_LTC_STEP_ADJ_LO)

Index (In decimal): EP 4.531 Size: 16 bits

This register contains the lower 16 bits of the step adjustment value.

Bits	Description	Type	Default
15:0	**LTC Step Adjustment Value (PTP_LTC_STEP_ADJ_VALUE[15:0])** When the nanoseconds portion of the 1588 Local Time Counter is being adjusted, this field specifies the amount to add. This is in lieu of the normal reference clock period increment. When the seconds portion of the 1588 Local Time Counter is being adjusted, the lower four bits of this field specify the amount to add to or subtract.	R/W	0000h

2.1.91 PTP LTC EXTERNAL ADJUSTMENT CONFIGURATION REGISTER (PTP_LTC_EXT_ADJ_CFG)

Index (In decimal): EP 4.532 Size: 16 bits

This read/write register is used to configure control of the 1588 Local Time Counter adjustments.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6	**GPIO_EPPS_SEL** This bit selects whether a GPIO or ePPS is the external LTC load/adjust source. GPIO_EPPS_SEL is only valid when PTP_LTC_TEMP_RATE_SEL = 1. 0 = External load/adjust source is GPIO 1 = External load/adjust source is ePPS	R/W	0b
5	**Serial Time of Day Enable (PTP_LTC_SERIAL_TOD_ENABLE)** This bit selects the TOD source for an External LTC Load operation. 0 = TOD is loaded from internal PTP LTC Set registers. In this case, a rising edge is required on the 1588_CLK_LD_ADJ pin. 1 = TOD is loaded from the 1588_CLK_LD_ADJ pin. In this case, 1PPS and Serial TOD encoding are both required on the 1588_CLK_LD_ADJ pin (ePPS is not supported in this mode). Serial TOD Load is only valid when PTP_LTC_TEMP_RATE_SEL = 1, GPIO_EPPS_SEL = 0, and PTP_LTC_EXTERNAL_LOAD_ENABLE = 1. This bit only selects the source of TOD for an External TOD Load. The External TOD Load operation itself must be configured using PTP_LTC_EXTERNAL_LOAD_ENABLE, PTP_LTC_TEMP_RATE_SEL, and PTP_LTC_EXTERNAL_MODE. This function is new compared to Pfeiffer.	R/W	0b
4	**LTC External Adjust Mode (PTP_LTC_EXTERNAL_MODE)** This bit configures whether only the first rising edge on the selected GPIO (or the first ePPS) causes an adjustment (one-shot) or every rising edge on the selected GPIO (or every ePPS) causes adjustments (static). 0 = One-shot adjustment. To initiate a one-shot adjustment, software must first clear this bit to 0, then set the appropriate adjustment bit (one of PTP_LTC_EXT_ADJ_CFG bits 3:0). Hardware will self-clear the adjustment bit from PTP_LTC_EXT_ADJ_CFG. 1 = Static (repeating) adjustments. To initiate static (repeating adjustments, software must first set this bit to 1, then set the appropriate adjustment bit (one of PTP_LTC_EXT_ADJ_CFG bits 3:0). To terminate static (repeating) adjustments, software must clear this bit to 0. Hardware will self-clear the adjustment bit from PTP_LTC_EXT_ADJ_CFG. **Note:** This bit definition is changed.	R/W	0b

Bits	Description	Type	Default
3	**LTC Temporary Rate Adjustment External Mode Enable** Enables a rising edge on the selected GPIO (or an ePPS) to cause a temporary rate adjustment to the to the 1588 Local Time Counter as specified by the PTP_LTC_TEMP_RATE_ADJ_HI/LO and PTP_LTC_TEMP_RATE_DURATION_HI/LO registers. External adjustment is only valid when PTP_LTC_TEMP_RATE_SEL = 1. One-shot or static/repeating adjustment is controlled by PTP_LTC_EXTERNAL_MODE. GPIO or ePPS selection is controlled by GPIO_EPPS_SEL. One-shot adjustment (PTP_LTC_EXTERNAL_MODE = 0). Software sets the bit to 1, hardware clears the bit after one adjustment is completed. Software may also clear the bit to 0. If cleared by software before an adjustment has started, the adjustment will not start. If cleared by software during an adjustment, the adjustment will complete. Static (repeating) adjustment (PTP_LTC_EXTERNAL_MODE = 1). Software sets the bit to 1, adjustments are made by hardware every time a GPIO rising edge or ePPS is detected. Software may not clear the bit to 0, When software terminates repeating adjustments, hardware will clear the bit to 0. To terminate repeating adjustments, software must clear PTP_LTC_EXTERNAL_MODE to 0. **Note:** This bit definition is changed.	R/W/SC	0b
2	**LTC Step Nanoseconds External Enable** Enables a rising edge on the selected GPIO (or an ePPS) to cause a step adjustment to the 1588 Local Time Counter nanoseconds as specified by the PTP_LTC_STEP_ADJ_HI/LO registers. External adjustment is only valid when PTP_LTC_TEMP_RATE_SEL = 1. One-shot or static/repeating adjustment is controlled by PTP_LTC_EXTERNAL_MODE. GPIO or ePPS selection is controlled by GPIO_EPPS_SEL. One-shot adjustment (PTP_LTC_EXTERNAL_MODE = 0). Software sets the bit to 1, hardware clears the bit after one adjustment is completed. Software may also clear the bit to 0. If cleared by software before an adjustment has started, the adjustment will not start. If cleared by software during an adjustment, the adjustment will complete. Static (repeating) adjustment (PTP_LTC_EXTERNAL_MODE = 1). Software sets the bit to 1, adjustments are made by hardware every time a GPIO rising edge or ePPS is detected. Software may not clear the bit to 0, When software terminates repeating adjustments, hardware will clear the bit to 0. To terminate repeating adjustments, software must clear PTP_LTC_EXTERNAL_MODE to 0. **Note:** This bit definition is changed.	R/W/SC	0b

Bits	Description	Type	Default
1	**LTC Step Seconds External Enable** Enables a rising edge on the selected GPIO (or an ePPS) to cause a step adjustment to the 1588 Local Time Counter seconds as specified by the PTP_LTC_STEP_ADJ_HI/LO registers. External adjustment is only valid when PTP_LTC_TEMP_RATE_SEL = 1. One-shot or static/repeating adjustment is controlled by PTP_LTC_EXTERNAL_MODE. GPIO or ePPS selection is controlled by GPIO_EPPS_SEL. One-shot adjustment (PTP_LTC_EXTERNAL_MODE = 0). Software sets the bit to 1, hardware clears the bit after one adjustment is completed. Software may also clear the bit to 0. If cleared by software before an adjustment has started, the adjustment will not start. If cleared by software during an adjustment, the adjustment will complete. Static (repeating) adjustment (PTP_LTC_EXTERNAL_MODE = 1). Software sets the bit to 1, adjustments are made by hardware every time a GPIO rising edge or ePPS is detected. Software may not clear the bit to 0, When software terminates repeating adjustments, hardware will clear the bit to 0. To terminate repeating adjustments, software must clear PTP_LTC_EXTERNAL_MODE to 0. **Note:** This bit definition is changed.	R/W/SC	0b
0	**LTC Load External Enable (PTP_LTC_EXTERNAL_LOAD_ENABLE)** Enables a rising edge on the selected GPIO (or an ePPS) to cause the 1588 Local Time Counter to be loaded from one of these: • (PTP_LTC_SERIAL_TOD_ENABLE = 0): The PTP_LTC_SET_SEC_HI/LO, PTP_LTC_SET_NS_HI/LO, and PTP_LTC_SET_SUBNS_HI/LO registers • (PTP_LTC_SERIAL_TOD_ENABLE = 1). The 1588_CLK_LD_ADJ pin External adjustment is only valid when PTP_LTC_TEMP_RATE_SEL = 1. One-shot or static/repeating adjustment is controlled by PTP_LTC_EXTERNAL_MODE. GPIO or ePPS selection is controlled by GPIO_EPPS_SEL. One-shot LTC Load (PTP_LTC_EXTERNAL_MODE = 0). Software sets the bit to 1, hardware clears the bit after one LTC Load is completed. Software may also clear the bit to 0. If cleared by software before an LTC Load has started, the LTC Load will not start. If cleared by software during an LTC Load, the LTC Load will complete. Static (repeating) LTC Load (PTP_LTC_EXTERNAL_MODE = 1). Software sets the bit to 1, LTC Load is performed by hardware every time a rising edge is detected on the GPIO. Software may not clear the bit to 0, When software terminates repeating LTC Loads, hardware will clear the bit to 0. To terminate repeating LTC Loads, software must clear PTP_LTC_EXTERNAL_MODE to 0. **Note:** This bit definition is changed.	R/W/SC	0b

To use the external 1588_LD_ADJ pin it must be enabled as a GPIO Alternate Function, and GPIO_EPPS_SEL must be set to GPIO. To use the ePPS, the external 1588 reference clock must be in use, EPPS_ENABLE must be enabled, and GPIO_EPPS_SEL must be set to EPPS.

To initiate static adjust operation:

1. Ensure PTP_LTC_EXTERNAL_MODE is set to 1 and all four bits of PTP_LTC_EXT_ADJ_CFG[3:0] are cleared to 0.
2. Set one bit of PTP_LTC_EXT_ADJ_CFG[3:0] to 1. This initiates the static adjustment.
   - So PTP_LTC_EXTERNAL_MODE = 1b and PTP_LTC_EXT_ADJ_CFG[3:0] = 0001b, 0010b, 0100b, or 1000b.
3. The selected adjustment will then be made every GPIO rising edge or ePPS until static adjust operation is terminated.

To terminate static adjust operation:

1. Clear PTP_LTC_EXTERNAL_MODE to 0. One bit of PTP_LTC_EXT_ADJ_CFG[3:0] is supposed to be 1 before this bit is cleared. This condition terminates the static adjust operation.
2. Hardware then self-clears the PTP_LTC_EXT_ADJ[3:0] bits (only one of these bits is supposed to be set).
   - So PTP_LTC_EXTERNAL_MODE = 0b and PTP_LTC_EXT_ADJ_CFG[3:0] = 000b.
   - Clearing the PTP_LTC_EXT_ADJ_CFG bits and stopping the adjustment will occur even if no more GPIO rising edges or ePPS are detected.

To initiate one-shot adjust operation:

1. Ensure PTP_LTC_EXTERNAL_MODE and all four bits of PTP_LTC_EXT_ADJ_CFG[3:0] are cleared to zero.
2. Set one bit of PTP_LTC_EXT_ADJ_CFG[3:0] to 1. This initiates the one-shot adjustment.
   - So PTP_LTC_EXTERNAL_MODE = 0b and PTP_LTC_EXT_ADJ_CFG[3:0] = 0001b, 0010b, 0100b, or 1000b.
3. The selected adjustment will then be made on the next GPIO rising edge or ePPS.
4. Hardware then self-clears the PTP_LTC_EXT_ADJ[3:0] bits (only one of these bits is supposed to be set).
   - So PTP_LTC_EXTERNAL_MODE = 0b and PTP_LTC_EXT_ADJ_CFG[3:0] = 000b

Clearing the PTP_LTC_EXT_ADJ_CFG bits and stopping the adjustment will occur even if no more GPIO rising edges or ePPS are detected.

2.1.92 PTP LTC TARGET X SECONDS HIGH REGISTER (PTP_LTC_TARGET_SEC_HI_X)

Index (In decimal): Channel A: EP 4.533 Channel B: EP 4.543 Size: 16 bits

This read/write register combined with the PTP LTC Target x Seconds Low Register (PTP_LTC_TARGET_SEC_LO_x) and the PTP LTC Target x Nanoseconds High/Lo Registers (PTP_LTC_TARGET_NS_HI/LO_x) form the 1588 Local Time Target value. This register contains the upper 16 bits of the target seconds.

Bits	Description	Type	Default
15:0	**LTC Target Seconds (LTC_TARGET_SEC[31:16])** This field contains the seconds portion of the 1588 Local Time Compare value.	R/W	0000h

Note 1: All four registers (PTP_LTC_TARGET_SEC_LO/HI_x and PTP_LTC_TARGET_NS_HI/LO_x) must be written for any to be affected.

2: The value read is the saved value of the 1588 Local Time Target when the LTC Target Read (PTP_LTC_TARGET_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set or the last value written.

3: When the LTC Target Read (PTP_LTC_TARGET_READ) bit is set, the previous value written to this register is overwritten. Normally, a read command would not be requested in between writing this register and the other three.

4: Writes to this register will overwrite the previous result of a LTC Target Read command. Normally, a write would not be done in between issuing LTC Target Read command and reading this register.

2.1.93 PTP LTC TARGET X SECONDS LOW REGISTER (PTP_LTC_TARGET_SEC_LO_X)

Index (In decimal): Channel A: EP 4.534 Channel B: EP 4.544 Size: 16 bits

This register contains the lower 16 bits of the target seconds.

Bits	Description	Type	Default
15:0	**LTC Target Seconds (LTC_TARGET_SEC[15:0])** This field contains the seconds portion of the 1588 Local Time Compare value.	R/W	0000h

Note 1: All four registers (PTP_LTC_TARGET_SEC_LO/HI_x and PTP_LTC_TARGET_NS_HI/LO_x) must be written for any to be affected.

2: The value read is the saved value of the 1588 Local Time Target when the LTC Target Read (PTP_LTC_TARGET_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set or the last value written.

3: When the LTC Target Read (PTP_LTC_TARGET_READ) bit is set, the previous value written to this register is overwritten. Normally, a read command would not be requested in between writing this register and the other three.

4: Writes to this register will overwrite the previous result of a LTC Target Read command. Normally, a write would not be done in between issuing LTC Target Read command and reading this register.

2.1.94 PTP LTC TARGET X NANOSECONDS HIGH REGISTER (PTP_LTC_TARGET_NS_HI_X)

Index (In decimal): Channel A: EP 4.535 Size: 16 bits
Channel B: EP 4.545

This read/write register combined with PTP LTC Target x Seconds Low/High Registers (PTP_LTC_TARGET_SEC_HI/LO_x) and the PTP LTC Target x Nanoseconds Low Register (PTP_LTC_TARGET_NS_LO_x) form the 1588 Local Time Target value. This register contains the upper 14 bits of the target nanoseconds.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:0	**LTC Target Nanoseconds (LTC_TARGET_NS[29:16])** This field contains the nanoseconds portion of the 1588 Local Time Compare value.	R/W	0000h

Note 1: All four registers (PTP_LTC_TARGET_SEC_LO/HI_x and PTP_LTC_TARGET_NS_HI/LO_x) must be written for any to be affected.

2: The value read is the saved value of the 1588 Local Time Target when the LTC Target Read (PTP_LTC_TARGET_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set or the last value written.

3: When the LTC Target Read (PTP_LTC_TARGET_READ) bit is set, the previous value written to this register is overwritten. Normally, a read command would not be requested in between writing this register and the other three.

4: Writes to this register will overwrite the previous result of a LTC Target Read command. Normally, a write would not be done in between issuing LTC Target Read command and reading this register.

2.1.95 PTP LTC TARGET X NANOSECONDS LOW REGISTER (PTP_LTC_TARGET_NS_LO_X)

Index (In decimal): Channel A: EP 4.536 Size: 16 bits
Channel B: EP 4.546

This register contains the lower 16 bits of the target nanoseconds.

Bits	Description	Type	Default
15:0	**LTC Target Nanoseconds (LTC_TARGET_NS[15:0])** This field contains the nanoseconds portion of the 1588 Local Time Compare value.	R/W	0000h

Note 1: All four registers (PTP_LTC_TARGET_SEC_LO/HI_x and PTP_LTC_TARGET_NS_HI/LO_x) must be written for any to be affected.

2: The value read is the saved value of the 1588 Local Time Target when the LTC Target Read (PTP_LTC_TARGET_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set or the last value written.

3: When the LTC Target Read (PTP_LTC_TARGET_READ) bit is set, the previous value written to this register is overwritten. Normally, a read command would not be requested in between writing this register and the other three.

4: Writes to this register will overwrite the previous result of a LTC Target Read command. Normally, a write would not be done in between issuing LTC Target Read command and reading this register.

2.1.96 PTP LTC TARGET X RELOAD/ADD SECONDS HIGH REGISTER (PTP_LTC_TARGET_RELOAD_SEC_HI_X)

Index (In decimal): Channel A: EP 4.537
Channel B: EP 4.547
Size: 16 bits

This read/write register combined with the PTP LTC Target x Reload/Add Seconds Low Register (PTP_LTC_TARGET_RELOAD_SEC_LO_x) and the PTP LTC Target x Reload/Add NanoSeconds High/Low Registers (PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) form the 1588 Local Time Target Reload value. This register contains the upper 16 bits of the target reload/add seconds.

Bits	Description	Type	Default
15:0	**LTC Target Reload Seconds (LTC_TARGET_RELOAD_SEC[31:16])** This field contains the seconds portion of the 1588 Local Time Target Reload value that is reloaded to the 1588 Local Time Target Compare value.	R/W	0000h

Note: All four registers (PTP_LTC_TARGET_RELOAD_SEC_LO/HI_x and PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) must be written for any to be affected.

2.1.97 PTP LTC TARGET X RELOAD/ADD SECONDS LOW REGISTER (PTP_LTC_TARGET_RELOAD_SEC_LO_X)

Index (In decimal): Channel A: EP 4.538
Channel B: EP 4.548
Size: 16 bits

This register contains the lower 16 bits of the target reload/add seconds.

Bits	Description	Type	Default
15:0	**LTC Target Reload Seconds (LTC_TARGET_RELOAD_SEC[15:0])** This field contains the seconds portion of the 1588 Local Time Target Reload value that is reloaded to the 1588 Local Time Target Compare value.	R/W	0000h

Note: All four registers (PTP_LTC_TARGET_RELOAD_SEC_LO/HI_x and PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) must be written for any to be affected.

2.1.98 PTP LTC TARGET X RELOAD/ADD NANOSECONDS HIGH REGISTER (PTP_LTC_TARGET_RELOAD_NS_HI_X)

Index (In decimal): Channel A: EP 4.539 Channel B: EP 4.549 Size: 16 bits

This read/write register combined with the PTP LTC Target x Reload/Add Seconds High/Low Registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x) and the PTP LTC Target x Reload/Add Nanoseconds Low Register (PTP_LTC_TARGET_RELOAD_NS_LO_x) form the 1588 Local Time Target Reload value. This register contains the upper 14 bits of the target reload/add nanoseconds.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:0	**LTC Target Reload Nanoseconds (LTC_TARGET_RELOAD_NS[29:16])** This field contains the nanoseconds portion of the 1588 Local Time Target Reload value that is reloaded to the 1588 Local Time Target Compare value.	R/W	0000h

Note: All four registers (PTP_LTC_TARGET_RELOAD_SEC_LO/HI_x and PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) must be written for any to be affected.

2.1.99 PTP LTC TARGET X RELOAD/ADD NANOSECONDS LOW REGISTER (PTP_LTC_TARGET_RELOAD_NS_LO_X)

Index (In decimal): Channel A: EP 4.540 Channel B: EP 4.550 Size: 16 bits

This register contains the lower 16 bits of the target reload/add nanoseconds.

Bits	Description	Type	Default
15:0	**LTC Target Reload Nanoseconds (LTC_TARGET_RELOAD_NS[15:0])** This field contains the nanoseconds portion of the 1588 Local Time Target Reload value that is reloaded to the 1588 Local Time Target Compare value.	R/W	0000h

Note: All four registers (PTP_LTC_TARGET_RELOAD_SEC_LO/HI_x and PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) must be written for any to be affected.

2.1.100 PTP LTC TARGET X ACTUAL NANOSECONDS HIGH REGISTER (PTP_LTC_TARGET_ACT_NS_HI_X)

Index (In decimal): Channel A: EP 4.541
Channel B: EP 4.551
Size: 16 bits

This read only register combined and the PTP LTC Target x Actual Nanoseconds Low Register (PTP_LTC_TARGET_ACT_NS_LO_x) contain the 1588 Local Time Counter nanoseconds value when the Local Time event occurs. This register contains the upper 14 bits of the LTC target actual nanoseconds.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:0	**LTC Target Actual Nanoseconds (LTC_TARGET_ACT_NS[29:16])** This field contains the nanoseconds portion of the 1588 Local Time Target Compare value.	RO	0000h

2.1.101 PTP LTC TARGET X ACTUAL NANOSECONDS LOW REGISTER (PTP_LTC_TARGET_ACT_NS_LO_X)

Index (In decimal): Channel A: EP 4.542
Channel B: EP 4.552
Size: 16 bits

This register contains the lower 16 bits of the target actual nanoseconds.

Bits	Description	Type	Default
15:0	**LTC Target Actual Nanoseconds (LTC_TARGET_ACT_NS[15:0])** This field contains the nanoseconds portion of the 1588 Local Time Target Compare value.	RO	0000h

2.1.102 PTP LTC READ SECONDS HIGH REGISTER (PTP_LTC_RD_SEC_HI)

Index (In decimal): EP 4.553
Size: 16 bits

This register contains the upper 16 bits of the seconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[47:32])** This field contains the upper 16 bits of the seconds portion of the 1588 Local Time Counter.	RO	0000h

The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

2.1.103 PTP LTC READ SECONDS MID REGISTER (PTP_LTC_RD_SEC_MID)

Index (In decimal): EP 4.554 Size: 16 bits

This register contains the middle 16 bits of the seconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[31:16])** This field contains the middle 16 bits of the seconds portion of the 1588 Local Time Counter.	RO	0000h

The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

2.1.104 PTP LTC READ SECONDS LOW REGISTER (PTP_LTC_RD_SEC_LO)

Index (In decimal): EP 4.555 Size: 16 bits

This register contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[15:0])** This field contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter.	RO	0000h

The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

2.1.105 PTP LTC READ NANOSECONDS HIGH REGISTER (PTP_LTC_RD_NS_HI)

Index (In decimal): EP 4.556 Size: 16 bits

This register contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:0	**LTC Nanoseconds (PTP_LTC_NS[29:16])** This field contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

2.1.106 PTP LTC READ NANOSECONDS LOW REGISTER (PTP_LTC_RD_NS_LO)

Index (In decimal): EP 4.557 Size: 16 bits

This register contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:0	**LTC Nanoseconds (PTP_LTC_NS[15:0])** This field contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

2.1.107 PTP LTC READ SUB-NANOSECONDS HIGH REGISTER (PTP_LTC_RD_SUBNS_HI)

Index (In decimal): EP 4.558 Size: 16 bits

This register contains the upper 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:0	**LTC Sub-Nanoseconds (PTP_LTC_SUBNS[31:16])** This field contains the upper 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

2.1.108 PTP LTC READ SUB-NANOSECONDS LOW REGISTER (PTP_LTC_RD_SUBNS_LO)

Index (In decimal): EP 4.559 Size: 16 bits

This register contains the lower 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:0	**LTC Sub-Nanoseconds (PTP_LTC_SUBNS[15:0])** This field contains the lower 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

2.1.109 PTP GPIO SELECT REGISTER (PTP_GPIO_SEL)

Index (In decimal): EP 4.560 Size: 16 bits

Bits	Description	Type	Default
15:11	**RESERVED**	RO	—
10:8	**GPIO Select (GPIO_SEL[2:0])** This field specifies which set of PTP GPIO Capture Registers the various GPIO x registers will access.	R/W	000b
7:0	**RESERVED**	RO	—

2.1.110 PTP GPIO CAPTURE MAP HIGH REGISTER (PTP_GPIO_CAP_MAP_HI)

Index (In decimal): EP 4.561 Size: 16 bits

This register maps the sixteen GPIOs 0-15 into the upper four PTP GPIO Capture Register sets. The PTP GPIO Capture functionality must still be enabled using the PTP GPIO Capture Enable Register.

There are eight sets of rising edge and eight sets of falling edge PTP GPIO Capture Register sets (x = 0 through 7).

Bits	Description	Type	Default
15:12	**PTP GPIO Capture 7 Register Map (PTP_GPIO_CAP_7 MAP[3:0])** These bits map one of GPIO[15:0] to this PTP GPIO Capture Register set. 0000 = GPIO 0 is mapped to this PTP GPIO Capture Register set. | 1111 = GPIO 15 is mapped to this PTP GPIO Capture Register set.	R/W	0000b
11:8	**PTP GPIO Capture 6 Register Map (PTP_GPIO_CAP_6 MAP[3:0])** These bits map one of GPIO[15:0] to this PTP GPIO Capture Register set. 0000 = GPIO 0 is mapped to this PTP GPIO Capture Register set. | 1111 = GPIO 15 is mapped to this PTP GPIO Capture Register set.	R/W	0000b
7:4	**PTP GPIO Capture 5 Register Map (PTP_GPIO_CAP_5 MAP[3:0])** These bits map one of GPIO[15:0] to this PTP GPIO Capture Register set. 0000 = GPIO 0 is mapped to this PTP GPIO Capture Register set. | 1111 = GPIO 15 is mapped to this PTP GPIO Capture Register set.	R/W	0000b
3:0	**PTP GPIO Capture 4 Register Map (PTP_GPIO_CAP_4 MAP[3:0])** These bits map one of GPIO[15:0] to this PTP GPIO Capture Register set. 0000 = GPIO 0 is mapped to this PTP GPIO Capture Register set. | 1111 = GPIO 15 is mapped to this PTP GPIO Capture Register set.	R/W	0000b

2.1.111 PTP GPIO CAPTURE MAP LOW REGISTER (PTP_GPIO_CAP_MAP_LO)

Index (In decimal): EP 4.562 Size: 16 bits

This register maps the sixteen GPIOs 0-15 into the lower four PTP GPIO Capture Register sets. The PTP GPIO Capture functionality must still be enabled using the PTP GPIO Capture Enable Register.

There are eight sets of rising edge and eight sets of falling edge PTP GPIO Capture Register sets (x = 0 through 7).

Bits	Description	Type	Default
15:12	**PTP GPIO Capture 3 Register Map (PTP_GPIO_CAP_3 MAP[3:0])** These bits map one of GPIO[15:0] to this PTP GPIO Capture Register set. 0000 = GPIO 0 is mapped to this PTP GPIO Capture Register set. | 1111 = GPIO 15 is mapped to this PTP GPIO Capture Register set.	R/W	0000b
11:8	**PTP GPIO Capture 2 Register Map (PTP_GPIO_CAP_2 MAP[3:0])** These bits map one of GPIO[15:0] to this PTP GPIO Capture Register set. 0000 = GPIO 0 is mapped to this PTP GPIO Capture Register set. | 1111 = GPIO 15 is mapped to this PTP GPIO Capture Register set.	R/W	0000b
7:4	**PTP GPIO Capture 1 Register Map (PTP_GPIO_CAP_1 MAP[3:0])** These bits map one of GPIO[15:0] to this PTP GPIO Capture Register set. 0000 = GPIO 0 is mapped to this PTP GPIO Capture Register set. | 1111 = GPIO 15 is mapped to this PTP GPIO Capture Register set.	R/W	0000b
3:0	**PTP GPIO Capture 0 Register Map (PTP_GPIO_CAP_0 MAP[3:0])** These bits map one of GPIO[15:0] to this PTP GPIO Capture Register set. 0000 = GPIO 0 is mapped to this PTP GPIO Capture Register set. | 1111 = GPIO 15 is mapped to this PTP GPIO Capture Register set.	R/W	0000b

2.1.112 PTP GPIO CAPTURE ENABLE REGISTER (PTP_GPIO_CAP_EN)

Index (In decimal): EP 4.563 Size: 16 bits

There are eight sets of rising edge and eight sets of falling edge PTP GPIO Capture Registers (x = 0 through 7).

Bits	Description	Type	Default
15:8	**GPIO Falling Edge Capture Enable 7-0 (GPIO_FE_CAPTURE_ENABLE[7:0])** These bits enable the falling edge of the selected GPIO input to capture the 1588 Local Time Counter value into the respective PTP GPIO Capture register set and to set the respective PTP_GPIO interrupt. 0 = Disables GPIO Capture 1 = Enables GPIO Capture	R/W	00h
7:0	**GPIO Rising Edge Capture Enable 7-0 (GPIO_RE_CAPTURE_ENABLE[7:0])** These bits enable the rising edge of the selected GPIO input to capture the 1588 Local Time Counter value into the respective PTP GPIO Capture register set and to set the respective PTP_GPIO interrupt. 0 = Disables GPIO Capture 1 = Enables GPIO Capture	R/W	00h

2.1.113 PTP GPIO CAPTURE LOCK REGISTER (PTP_GPIO_CAP_LOCK)

Index (In decimal): EP 4.564 Size: 16 bits

There are eight sets of rising edge and eight sets of falling edge PTP GPIO Capture Registers (x = 0 through 7).

Bits	Description	Type	Default
15:8	**Lock Enable GPIO Falling Edge (LOCK_GPIO_FE[7:0])** These bits enable/disables the GPIO falling edge lock. This lock prevents a 1588 capture from overwriting the Local Time value if the GPIO falling edge interrupt is already set due to a previous capture. 0 = Disables GPIO falling edge lock 1 = Enables GPIO falling edge lock	R/W	FFh
7:0	**Lock Enable GPIO Rising Edge (LOCK_GPIO_RE[7:0])** These bits enable/disables the GPIO rising edge lock. This lock prevents a 1588 capture from overwriting the Local Time value if the GPIO rising edge interrupt is already set due to a previous capture. 0 = Disables GPIO rising edge lock 1 = Enables GPIO rising edge lock	R/W	FFh

2.1.114 PTP GPIO X RISING EDGE LTC SECONDS HIGH CAPTURE REGISTER (PTP_GPIO_RE_LTC_SEC_HI_CAP_X)

Index (In decimal): EP 4.565 Size: 16 bits

This read only register contains the upper 16 bits of seconds of the rising edge PTP GPIO Capture.

Note 1: There are eight sets of rising edge and eight sets of falling edge PTP GPIO Capture Registers (x = 0 through 7). Values are only valid if the appropriate PTP GPIO Rising Edge Capture Status (PTP_GPIO_RE_STS[7:0]) bit indicates that a timestamp is available.

2: Unless the corresponding Lock Enable GPIO Rising Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this and the other three rising edge capture registers. Software techniques are required to avoid reading intermediate values.

3: The PTP GPIO Capture Register accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the upper 16 bits of the seconds portion of the timestamp upon the rising edge of a GPIO or upon a software commanded manual capture.	RO	0000h

2.1.115 PTP GPIO X RISING EDGE LTC SECONDS LOW CAPTURE REGISTER (PTP_GPIO_RE_LTC_SEC_LO_CAP_X)

Index (In decimal): EP 4.566 Size: 16 bits

This read only register contains the lower 16 bits of seconds of the rising edge PTP GPIO Capture.

Note 1: There are eight sets of rising edge and eight sets of falling edge PTP GPIO Capture registers (x = 0 through 7). Values are only valid if the appropriate PTP GPIO Rising Edge Capture Status (PTP_GPIO_RE_STS[7:0]) bit indicates that a timestamp is available.

2: Unless the corresponding Lock Enable GPIO Rising Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this and the other three rising edge capture registers. Software techniques are required to avoid reading intermediate values.

3: The PTP GPIO Capture Register accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[15:0])** This field contains the lower 16 bits of the seconds portion of the timestamp upon the rising edge of a GPIO or upon a software commanded manual capture.	RO	0000h

2.1.116 PTP GPIO X RISING EDGE LTC NANOSECONDS HIGH CAPTURE REGISTER (PTP_GPIO_RE_LTC_NS_HI_CAP_X)

Index (In decimal): EP 4.567 Size: 16 bits

This read only register contains the upper 14 bits of nanoseconds of the rising edge PTP GPIO Capture.

Note 1: There are eight sets of rising edge and eight sets of falling edge PTP GPIO Capture registers (x = 0 through 7). Values are only valid if the appropriate PTP GPIO Rising Edge Capture Status (PTP_GPIO_RE_STS[7:0]) bit indicates that a timestamp is available.

2: Unless the corresponding Lock Enable GPIO Rising Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this and the other three rising edge capture registers. Software techniques are required to avoid reading intermediate values.

3: The PTP GPIO Capture Register accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**Timestamp Input Phase (TS_PHASE)** This bit indicates if the GPIO input occurred in the first or second half of the 1588 reference clock period and can be used to reduce the asynchronous uncertainly. 1 = Input occurred in the first half period 0 = Input occurred in the second half period **Note:** This bit is not valid for a software commanded manual capture.	RO	0b
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the upper 14 bits of the nanoseconds portion of the timestamp upon the rising edge of a GPIO or upon a software commanded manual capture.	RO	0000h

2.1.117 PTP GPIO X RISING EDGE LTC NANOSECONDS LOW CAPTURE REGISTER (PTP_GPIO_RE_LTC_NS_LO_CAP_X)

Index (In decimal): EP 4.568 Size: 16 bits

This read only register contains the lower 16 bits of nanoseconds of the rising edge PTP GPIO Capture.

Note 1: There are eight sets of rising edge and eight sets of falling edge PTP GPIO Capture registers (x = 0 through 7). Values are only valid if the appropriate PTP GPIO Rising Edge Capture Status (PTP_GPIO_RE_STS[7:0]) bit indicates that a timestamp is available.

2: Unless the corresponding Lock Enable GPIO Rising Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this and the other three rising edge capture registers. Software techniques are required to avoid reading intermediate values.

3: The PTP GPIO Capture Register accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Bits	Description	Type	Default
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the lower 16 bits of the nanoseconds portion of the timestamp upon the rising edge of a GPIO or upon a software commanded manual capture.	RO	0000h

2.1.118 PTP GPIO X FALLING EDGE LTC SECONDS HIGH CAPTURE REGISTER (PTP_GPIO_FE_LTC_SEC_HI_CAP_X)

Index (In decimal): EP 4.569 Size: 16 bits

This read only register contains the upper 16 bits of seconds of the falling edge PTP GPIO Capture.

Note 1: There are eight sets of rising edge and eight sets of falling edge PTP GPIO Capture registers (x = 0 through 7). Values are only valid if the appropriate PTP GPIO Falling Edge Capture Status (PTP_GPIO_RE_STS[7:0]) bit indicates that a timestamp is available.

2: Unless the corresponding Lock Enable GPIO Falling Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this and the other three falling edge capture registers. Software techniques are required to avoid reading intermediate values.

3: The PTP GPIO Capture Register accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the upper 16 bits of the seconds portion of the timestamp upon the falling edge of a GPIO or upon a software commanded manual capture.	RO	0000h

2.1.119 PTP GPIO X FALLING EDGE LTC SECONDS LOW CAPTURE REGISTER (PTP_GPIO_FE_LTC_SEC_LO_CAP_X)

Index (In decimal): EP 4.570 Size: 16 bits

This read only register contains the lower 16 bits of seconds of the falling edge PTP GPIO Capture.

Note 1: There are eight sets of rising edge and eight sets of falling edge PTP GPIO Capture registers (x = 0 through 7). Values are only valid if the appropriate PTP GPIO Falling Edge Capture Status (PTP_GPIO_RE_STS[7:0]) bit indicates that a timestamp is available.

2: Unless the corresponding Lock Enable GPIO Falling Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this and the other three falling edge capture registers. Software techniques are required to avoid reading intermediate values.

3: The PTP GPIO Capture Register accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[15:0])** This field contains the lower 16 bits of the seconds portion of the timestamp upon the falling edge of a GPIO or upon a software commanded manual capture.	RO	0000h

2.1.120 PTP GPIO X FALLING EDGE LTC NANOSECONDS HIGH CAPTURE REGISTER (PTP_GPIO_FE_LTC_NS_HI_CAP_X)

Index (In decimal): EP 4.571 Size: 16 bits

This read only register contains the upper 14 bits of nanoseconds of the falling edge PTP GPIO Capture.

Note 1: There are eight sets of rising edge and eight sets of falling edge PTP GPIO Capture registers (x = 0 through 7). Values are only valid if the appropriate PTP GPIO Falling Edge Capture Status (PTP_GPIO_RE_STS[7:0]) bit indicates that a timestamp is available.

2: Unless the corresponding Lock Enable GPIO Falling Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this and the other three falling edge capture registers. Software techniques are required to avoid reading intermediate values.

3: The PTP GPIO Capture Register accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**Timestamp Input Phase (TS_PHASE)** This bit indicates if the GPIO input occurred in the first or second half of the 1588 reference clock period and can be used to reduce the asynchronous uncertainly. 1 = Input occurred in the first half period 0 = Input occurred in the second half period **Note:** This bit is not valid for a software commanded manual capture.	RO	0b
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the upper 14 bits of the nanoseconds portion of the time-stamp upon the falling edge of a GPIO or upon a software commanded manual capture.	RO	0000h

2.1.121 PTP GPIO X FALLING EDGE LTC NANOSECONDS LOW CAPTURE REGISTER (PTP_GPIO_FE_LTC_NS_LO_CAP_X)

Index (In decimal): EP 4.572 Size: 16 bits

This read only register contains the lower 16 bits of nanoseconds of the falling edge PTP GPIO Capture.

Note 1: There are eight sets of rising edge and eight sets of falling edge capture registers (x = 0 through 7). Values are only valid if the appropriate PTP GPIO Falling Edge Capture Status (PTP_GPIO_RE_STS[7:0]) bit indicates that a timestamp is available.

2: Unless the corresponding Lock Enable GPIO Falling Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this and the other three falling edge capture registers. Software techniques are required to avoid reading intermediate values.

3: The PTP GPIO Capture Register accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Bits	Description	Type	Default
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the lower 16 bits of the nanoseconds portion of the time-stamp upon the falling edge of a GPIO or upon a software commanded manual capture.	RO	0000h

2.1.122 PTP GPIO CAPTURE STATUS REGISTER (PTP_GPIO_CAP_STS)

Index (In decimal): EP 4.573 Size: 16 bits

This register contains the PTP GPIO Capture status bits.

Reading this register clears the interrupt sources.

Note: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15:8	**PTP GPIO Falling Edge Capture Status (PTP_GPIO_FE_STS[7:0])** This interrupt indicates that a falling event occurred and the 1588 Local Time Counter was captured. These bits can also be set due to a manual capture via PTP Manual Capture (PTP_MANUAL_CAPTURE).	RC	00h
7:0	**PTP GPIO Rising Edge Capture Status (PTP_GPIO_RE_STS[7:0])** This interrupt indicates that a rising event occurred and the 1588 Local Time Counter was captured. These bits can also be set due to a manual capture via PTP Manual Capture (PTP_MANUAL_CAPTURE).	RC	00h

2.1.123 PTP GPIO INTERRUPT CLEAR CONFIGURATION REGISTER (PTP_GPIO_INT_CLR_CFG)

Index (In decimal): EP 4.574 Size: 16 bits

Bits	Description	Type	Default
15:11	**GPIO PTP Timer Interrupt B Clear Select (GPIO_PTP_TIMER_INT_B_CLEAR_SEL[4:0])** These bits determine which GPIO is used to clear the PTP Timer Interrupt B (PTP_TIMER_INT_B) bit of the PTP Common Interrupt Status Register (PTP_COMMON_INT_STS). 00000 = GPIO 0 is used to clear the PTP Timer Interrupt B | 11111 = GPIO 31 is used to clear the PTP Timer Interrupt B	R/W	00000b
10	**RESERVED**	RO	—
9	**GPIO PTP Timer Interrupt B Clear Polarity (GPIO_PTP_TIMER_INT_B_CLEAR_POL)** This bit selects the polarity of the selected GPIO. 0 = Active low 1 = Active high	R/W	0b
8	**GPIO PTP Timer Interrupt B Clear Enable (GPIO_PTP_TIMER_INT_B_CLEAR_EN)** This bit enables the selected GPIO to clear the PTP Timer Interrupt B (PTP_TIMER_INT_B) bit of the PTP Common Interrupt Status Register (PTP_COMMON_INT_STS).	R/W	0b
7:3	**GPIO PTP Timer Interrupt A Clear Select (GPIO_PTP_TIMER_INT_A_CLEAR_SEL[4:0])** These bits determine which GPIO is used to clear the PTP Timer Interrupt A (PTP_TIMER_INT_A) bit of the PTP Common Interrupt Status Register (PTP_COMMON_INT_STS). 00000 = GPIO 0 is used to clear the PTP Timer Interrupt A | 11111 = GPIO 31 is used to clear the PTP Timer Interrupt A	R/W	00000b
2	**RESERVED**	RO	—
1	**GPIO PTP Timer Interrupt A Clear Polarity (GPIO_PTP_TIMER_INT_A_CLEAR_POL)** This bit selects the polarity of the selected GPIO. 0 = Active low 1 = Active high	R/W	0b
0	**GPIO PTP Timer Interrupt A Clear Enable (GPIO_PTP_TIMER_INT_A_CLEAR_EN)** This bit enables the selected GPIO to clear the PTP Timer Interrupt A (PTP_TIMER_INT_A) bit of the PTP Common Interrupt Status Register (PTP_COMMON_INT_STS).	R/W	0b

2.1.124 PTP LTC HARD RESET REGISTER

Index (In decimal): EP 4.575 Size: 16 bits

This register resets the PTP Local Time Counter (LTC) and sets all related configuration registers to their default state.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**PTP LTC Hard Reset** 1 = Reset the PTP LTC and set all configuration registers to their default state. Writing a zero has no effect.	W1S/SC	0b

2.1.125 PTP LTC SOFT RESET REGISTER

Index (In decimal): EP 4.576 Size: 16 bits

This register resets the PTP Local Time Counter (LTC) but does not reset any configuration registers.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**PTP LTC Soft Reset** 1 = Reset the PTP LTC except all configuration registers. Writing a zero has no effect.	W1S/SC	0b

2.1.126 PTP OPERATING MODE REGISTER

Index (In decimal): EP 4.577 Size: 16 bits

This register configures the PTP operating mode of the chip.

Bits	Description	Type	Default
15:2	**RESERVED**	RO	—
1:0	**PTP Operating Mode** Configures the PTP operating mode for all ports of the chip. 00 = PTP functions are disabled 01 = PTP Standalone Mode 10 = PTP PCH Mode (MCH support disabled) 11 = PTP PCH Mode (MCH support enabled) **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit is set.	R/W	00b

2.1.127 PTP REVISION REGISTER

Index (In decimal): EP 4.578 Size: 16 bits

This register provides the revision of the PTP design.

Bits	Description	Type	Default
15:0	**PTP_REVISION**	RO	Note 1

Note 1: The revision is set within chip TOP. The first version will be set to 0000h, subsequent revisions will increment this field.

2.1.128 PTP PCH SUBPORTID REGISTER

Index (In decimal): EP 4.579 Size: 16 bits

This register configures the PCH (MCH) SubPortID for each device Port. This is the value sent with each frame in the PCH (MCH) header toward the USGMII interface, and this value is checked in the PCH (MCH) header for each frame received from the USGMII interface. This value is associated with the device physical port numbers independent of QSGMII muxing order.

Bits	Description	Type	Default
3:0	**Port 3 SubPortID [3:0]**	R/W	0011b
3:0	**Port 2 SubPortID [3:0]**	R/W	0010b
3:0	**Port 1 SubPortID [3:0]**	R/W	0001b
3:0	**Port 0 SubPortID [3:0]**	R/W	0000b

2.1.129 PTP LATENCY CORRECTION CONTROL REGISTER

Index (In decimal): EP 4.580 Size: 16 bits

This register configures frame alignment and related timestamp correction for frames being sent toward QSGMII.

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7	**Rx Correction Add Subtract** 1 = Add the Rx Correction Value to the Rx Timestamp 0 = Subtract the Rx Correction Value from the Rx Timestamp	R/W	1b
6:4	**Rx Correction Value [2:0]** 000 = 0 nanoseconds 001 = 1 nanoseconds | 111 = 7 nanoseconds The default value 100 = 4 nanoseconds	R/W	100b
3:2	**RESERVED**	RO	—
1	**ABCD_0011_Correction_Disable** 1 = Correction disabled 0 = Correction enabled Disables lane alignment compensation for ABCD = 0011	R/W	0b
0	**Rx Predictor Disable** 1 = Rx Predictor disabled 0 = Rx Predictor enabled The Rx Predictor compensates Rx timestamps for GPHY lane alignment	R/W	0b

2.1.130 1588 STI CONFIGURATION REGISTER

Index (In decimal): EP 4.768 Size: 16 bits

This register configures the 1588 Serial Timestamp Interface (STI). The STI is only available in PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11	**1588 STI Clock Phase** 1 = 1588_STI_CLK rising edge changes 1588_STI_DO 0 = 1588_STI_CLK falling edge changes 1588_STI_DO	R/W	0b
10	**1588 STI Clock Polarity** 1 = 1588_STI_CLK starts and ends high 0 = 1588_STI_CLK starts and ends low	R/W	0b
9:7	**1588 STI Clock Frequency [2:0]** 000 = 62.5 MHz (system 125 MHz divided by 2) 001 = 41.67 MHz (system 125 MHz divided by 3) | 111 = 13.89 MHz (system 125 MHz divided by 9)	R/W	000b
6:4	**1588 STI CS_N Deselect Cycles [2:0]** Minimum number of 1588_STI_CLK cycles 1588_STI_CS_N is deasserted between outputs 000 = 1588_STI_CS_N deasserted at least 2 cycles 001 = 1588_STI_CS_N deasserted at least 3 cycles | 111 = 1588_STI_CS_N deasserted at least 8 cycles	R/W	000b
3:1	**1588 STI CS_N Assert Cycles [2:0]** Number of 1588_STI_CLK cycles between 1588_STI_CS_N assertion and first valid bit of 1588_STI_DO data out 000 = 1588_STI_CS_N asserted 2 cycles 001 = 1588_STI_CS_N asserted 3 cycles | 111 = 1588_STI_CS_N asserted 8 cycles	R/W	000b
0	**1588 STI Enable** 1 = Enable the 1588 Serial Timestamp Interface 0 = Disable the 1588 Serial Timestamp Interface **Note:** Tx Egress Time and SequenceID are not available for reading via MDIO when the 1588 STI is enabled.	R/W	0b

To use the 1588 Serial Timestamp Interface the appropriate pins must be enabled as GPIO Alternate Functions.

2.1.131 1588 STI TX COUNT REGISTER

Index (In decimal): EP 4.769 Size: 16 bits

This register provides a count of the number of timestamps transmitted across the STI. The STI is only available in PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**1588 STI Tx Counter [15:0]** Count of the number of timestamps transmitted across the STI. This counter is cleared to zero on read, and halts at FFFFh	RC	0000h

2.1.132 1588 STI HARD RESET REGISTER

Index (In decimal): EP 4.770 Size: 16 bits

This register resets the 1588 Serial Timestamp Interface and sets all related configuration registers to their default state.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**1588 STI Hard Reset** 1 = Reset the 1588 STI and set all configuration registers to their default state Writing a zero has no effect.	W1S/SC	0b

2.1.133 1588 STI SOFT RESET REGISTER

Index (In decimal): EP 4.771 Size: 16 bits

This register resets the 1588 Serial Timestamp Interface but does not reset any configuration registers.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**1588 STI Soft Reset** 1 = Reset the 1588 STI except all configuration registers Writing a zero has no effect.	W1S/SC	0b

2.2 Extended Page 5 Registers

Device Port-Specific Registers are mapped to EP5.

2.2.1 LED CONTROL REGISTER 1

Index (In decimal): EP 5.0 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**first_pulse_fix_disable** 0 = Enable 1 = Disable When enabled, the new activity will not overlap the previous activity and will give a smooth blinking, instead of elongated blinking.	R/W	0b
13	**LED 1 Buffer Type** 0 = Open Drain or Open Source (determined by LED 1 Polarity) 1 = Push-Pull	R/W	0b
12	**LED 2 Buffer Type** 0 = Open Drain or Open Source (determined by LED 2 Polarity) 1 = Push-Pull	R/W	0b
11	**DGT_eee_led_md_en** 0 = Disable 1 = Enable	R/W	0b
10	**Single LED** 1 = Individual-LED mode 0 = Tri-Color-LED mode By default, this bit reflects the value of the LED_MODE strapping pin. If written as a 1, the value of the LED_MODE strapping pin is overridden and Individual-LED mode is selected.	R/W	Note 1
9	**LED 1 Test Control** 0 = LED 1 active 1 = LED 1 inactive	R/W	0b
8	**LED 2 Test Control** 0 = LED 2 active 1 = LED 2 inactive	R/W	0b
7	**LED Test Enable** 1 = Enabled: LED Test Control bits drive the LED outputs 0 = Disabled	R/W	0b
6	**KSZ9031 LED Mode** 1 = KSZ9031 LED mode 0 = Extended LED mode For normal LED operation, this bit should always be written as a 1.	R/W	1b
5	**Reg_eco_dis** Dual LED logic selection	R/W	1b
4:3	**mr_led_sel[1:0]** Controls the LED operation during Individual-LED mode.	R/W	11b
2:1	**mr_led_ctrl_test[1:0]**	R/W	11b
0	**mr_f_ledctrl**	R/W	0b

Note 1: The default is set by the LED_MODE strapping pin. To use LEDs they must be enabled as GPIO Alternate Functions.

2.2.2 LED CONTROL REGISTER 2

Index (In decimal): EP 5.1 Size: 16 bits

This register selects the operating mode of the PHY LEDs when in extended mode. This register is only used when the KSZ9031 LED Mode bit in LED Control Register 1 is clear.

Bits	Description	Type	Default
15	**LED Activity Output Select**	R/W	0b
14	**LED Pulsing Enable**	R/W	1b
13:12	**LED Blink/Pulse-Stretch Rate [1:0]** 00 = 2.5 Hz Blink Rate/400 ms pulse-stretch 01 = 5 Hz Blink Rate/200 ms pulse-stretch 10 = 10 Hz Blink Rate/100 ms pulse-stretch 11 = 20 Hz Blink Rate/50 ms pulse-stretch	R/W	00b
11	**LED 2 Pulse Stretch Enable** 0 = LED 2 is configured to blink 1 = LED 2 is configured to pulse-stretch	R/W	0b
10	**LED 1 Pulse Stretch Enable** 0 = LED 1 is configured to blink 1 = LED 1 is configured to pulse-stretch	R/W	0b
9	**LED 2 Combination Disable** 0 = Combine link/activity and duplex/collision for LED 2 1 = Provide link-only and duplex-only for LED 2	R/W	0b
8	**LED 1 Combination Disable** 0 = Combine link/activity and duplex/collision for LED 1 1 = Provide link-only and duplex-only for LED 1	R/W	0b
7:4	**LED2 Configuration [3:0]** This field configures LED2 Enhanced Mode operation 0000 = Enhanced Mode 0 0001 = Enhanced Mode 1 | 1111 = Enhanced Mode 15 LED2 default value is Enhanced Mode 4 per Product Marketing request.	R/W	0100b
3:0	**LED1 Configuration [3:0]** This field configures LED1 Enhanced Mode operation 0000 = Enhanced Mode 0 0001 = Enhanced Mode 1 | 1111 = Enhanced Mode 15 LED1 default value is Enhanced Mode 5 per Product Marketing request.	R/W	0101b

Note: To use LEDs they must be enabled as GPIO Alternate Functions.

2.2.3 QSGMII PCS1G HARD RESET REGISTER

Index (In decimal): EP 5.16 Size: 16 bits

This register resets the QSGMII PCS1G, and sets PCS1G configuration registers to their default state.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**QSGMII PCS1G Hard Reset** 1 = Reset the QSGMII PCS1G block and set all configuration registers to their default state Writing a zero has no effect.	W1S/SC	0b

2.2.4 QSGMII PCS1G SOFT RESET REGISTER

Index (In decimal): EP 5.17 Size: 16 bits

This register resets the QSGMII PCS1G, but does not reset any configuration registers.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**QSGMII PCS1G Soft Reset** 1 = Reset the QSGMII PCS1G block but no configuration registers Writing a zero has no effect.	W1S/SC	0b

2.2.5 QSGMII PCS1G CONFIGURATION AND STATUS REGISTER

Index (In decimal): EP 5.18 Size: 16 bits

This register provides configuration and status for the QSGMII PCS1G.

Note: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11	**SAVE_PREAMBLE_ENA** Preserves preamble when using PCH/MCH or preemption. When SAVE_PREAMBLE_ENA = 0, the PCS1G may occasionally drop a preamble byte due to even/odd byte alignment requirements 0 = Preamble Preservation disabled 1 = Preamble Preservation enabled	R/W	1b
10	**LINK_STATUS_TYPE** Define type of QSGMII link status indication 1 = QSGMII Link Partner up/down indication from lp_adv_ability[15] 0 = Sync Status from QSGMII PCS1G state machine	R/W	0b

Bits	Description	Type	Default
9	**PCS_ENA** 1 = Enable QSGMII PCS1G 0 = Disable QSGMII PCS1G	R/W	1b
8	**RESERVED** (SD_SEL is hardwired to 0, selecting signal detect from QSGMII SerDes which is connected to PCS1G signal_detect_hm_i)	RO	—
7	**SD_POL** Selects the polarity of the signal_detect line 0 = A '0' on the signal_detect line indicates active signal 1 = A '1' on the signal_detect line indicates active signal	R/W	1b
6	**SD_ENA** Signal detect enable 0 = The signal_detect line is ignored. The QSGMII PCS1G assumes an active signal_detect at all times. 1 = The signal_detect line is used to determine if a signal is detected.	R/W	1b
5	**SIGNAL_DETECT** Provides the current status of the QSGMII SerDes signal detect. 0 = No signal is detected 1 = Signal is detected	RO	0b
4	**LINK_STATUS** Indicates whether the QSGMII PCS1G link is up or down. The QSGMII PCS1G link is up when the ANEG state machine is in either the LINK_OK state, or the ANEG_DISABLE_LINK_OK state. 0 = QSGMII PCS1G link is down 1 = QSGMII PCS1G is up	RO	0b
3	**SYNC_STATUS** Indicates if the QSGMII PCS1G has successfully synchronized 0 = QSGMII PCS1G is not synchronized 1 = QSGMII PCS1G is synchronized	RO	0b
2	**LT_TESTMODE** Enables test mode with link timer divided by 1024 1 = Enable link timer test mode 0 = Disable link timer test mode (normal operation)	R/W	0b
1	**LINK_STATUS_CHANGE** This bit indicates a change of QSGMII PCS1G Link status. 0 = No change of QSGMII PCS1G Link status 1 = QSGMII PCS1G Link status has changed	RC	0b
0	**SYNC_STATUS_CHANGE** This bit indicates a change of QSGMII PCS1G Sync status. 0 = No change of QSGMII PCS1G Sync status 1 = QSGMII PCS1G Sync status has changed	RC	0b

2.2.6 QSGMII PCS1G ANEG CONFIGURATION REGISTER

Index (In decimal): EP 5.19 Size: 16 bits

This register provides Auto-negotiation configuration and status for the QSGMII PCS1G.

Note: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6	**AN_COMPLETE** 0 = ANEG not complete 1 = ANEG complete	RO	0b
5	**SW_RESOLVE_PRIORITY** Resolve priority via software 0 = Software does not resolve priority 1 = Software resolves priority	R/W	1b
4	**ANEG_RESTART_ONE_SHOT** Initiates restart of Auto-negotiation with the QSGMII Link Partner 0 = No action 1 = Restart auto-negotiation	W1S/RC	0b
3	**ANEG_ENA** 0 = Disable Auto-negotiation with the QSGMII PCS1G Link Partner 1 = Enable Auto-negotiation with the QSGMII PCS1G Link Partner	R/W	1b
2	**NP_LOADED_ONE_SHOT** TX_NP[15:0] must first be written with the desired NP data, then assert NP_LOADED_ONE_SHOT for this data to be loaded (take effect). 0 = No action 1 = Load the contents of TX_NP[15:0]	W1S/RC	0b
1	**PRIORITY_RESOLVE** Indicates ANEG priority can now be resolved by software 0 = ANEG is in process 1 = ANEG is nearly completed and priority can be resolved by software	RO	0b
0	**NEW_PAGE_RX** 0 = No new page received from the QSGMII PCS1G Link Partner 1 = New page received from the QSGMII PCS1G Link Partner	RC	0b

2.2.7 QSGMII PCS1G ANEG TX ADVERTISED ABILITIES REGISTER

Index (In decimal): EP 5.20 Size: 16 bits

This register provides the ANEG Advertised Abilities to be sent to the QSGMII PCS1G Link Partner.

Bits	Description	Type	Default
15:0	**TX_ADV_ABILITY[15:0]** When QSGMII_AUTO_ANEG_ENA = 0, this register must be fully software-configured with the ANEG Abilities to be sent to the QSGMII PCS1G Link Partner. When QSGMII_AUTO_ANEG_ENA=1: • SPEED (bits 11:9) and DUPLEX (bit 12) are automatically configured by hardware based on GPHY settings. Writing to this bits has no effect, however the automatically-determined settings can be read here. • All other bits must be software-configured as normal. • EEE Capability (bit 8) and EEE Clock Stop Capability (bit 7) are both set to 1 (supported) by default. • Bit 0 (defined only as ‘1’ in the standard) is set to 1 by default.	R/W	0181h

2.2.8 QSGMII PCS1G ANEG TX NP DATA REGISTER

Index (In decimal): EP 5.21 Size: 16 bits

This register provides the ANEG NP data to be sent to the QSGMII PCS1G Link Partner.

Bits	Description	Type	Default
15:0	**NP_TX[15:0]** ANEG Next Page data to be sent to the QSGMII PCS1G Link Partner	R/W	0000h

2.2.9 QSGMII PCS1G ANEG LP ADVERTISED ABILITIES REGISTER

Index (In decimal): EP 5.22 Size: 16 bits

This register provides the ANEG Advertised Abilities from the QSGMII PCS1G Link Partner.

Bits	Description	Type	Default
15:0	**LP_ADV_ABILITY[15:0]** ANEG Abilities received from the QSGMII PCS1G Link Partner	RO	0000h

2.2.10 QSGMII PCS1G ANEG LP NP DATA REGISTER

Index (In decimal): EP 5.23 Size: 16 bits

This register provides the ANEG Next Page data from the QSGMII PCS1G Link Partner.

Bits	Description	Type	Default
15:0	**LP_NP_RX[15:0]** ANEG Next Page data received from the QSGMII PCS1G Link Partner	RO	0000h

2.2.11 QSGMII PCS1G DEBUG REGISTER

Index (In decimal): EP 5.24 Size: 16 bits

This register provides debug and loopback control for the QSGMII PCS1G.

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8	**QSGMII_RX_CAR_EXT_FILTER_ENA** 0 = Do not filter Carrier Extend symbols after end of packet (normal mode) 1 = Filter Carrier Extend symbols after end of packet If enabled, filtering is from QSGMII Rx toward the Tx media interface.	R/W	0b
7	**QSGMII_TX_CAR_EXT_FILTER_ENA** 0 = Do not filter Carrier Extend symbols after end of packet (normal mode) 1 = Filter Carrier Extend symbols after end of packet If enabled, filtering is from Rx media interface toward QSGMII Tx.	R/W	0b
6	**UNIDIR_MODE** Enables 802.3 Clause 66 Unidirectional Mode 0 = Unidirectional Mode disabled 1 = Unidirectional Mode enabled	R/W	0b
5	**EN_CDET** Enables Comma Detection in PCS1G. Comma Detection is normally performed by the QSGMII Extender. 0 = Comma Detection disabled 1 = Comma Detection enabled	R/W	1b
4	**RA_ENA** Enables Rate Adaptation in Rx direction, required when GMII_LB_ENA = 1 0 = Rate Adaptation disabled 1 = Rate Adaptation enabled	R/W	0b
3:2	**XMIT_MODE[1:0]** Indicates the current QSGMII PCS1G TBI mode 00 = Idle mode 01 = Configuration mode 10 = RESERVED 11 = Data mode	RO	00b
1	**TBI_HOST_LB_ENA** Enables QSGMII PCS1G TBI loopback (TBI Tx to TBI Rx direction) 0 = TBI loopback disabled 1 = TBI loopback enabled	R/W	0b

Bits	Description	Type	Default
0	**GMII_LB_ENA** Enables QSGMII PCS1G GMII loopback (GMIII Rx to GMII Tx direction) 0 = GMII loopback disabled 1 = GMII loopback enabled	R/W	0b

2.2.12 QSGMII PCS1G LPI CONFIGURATION AND STATUS REGISTER

Index (In decimal): EP 5.25 Size: 16 bits

This register provides Low Power Idle control and status for the QSGMII PCS1G.

Bits	Description	Type	Default
15:5	**RESERVED**	RO	—
4	**TX_ASSERT_LPIDL** Asserts Low Power Idle control toward the QSGMII Link Partner 0 = Disable LPI in the QSGMII transmit direction 1 = Enable LPI in the QSGMII transmit direction	R/W	0b
3	**RX_LPI_OUT_DIS** Disable LPI output from the QSGMII PCS1G toward the GPHY 0 = LPI output enabled 1 = LPI output disabled	R/W	0b
2	**LPI_TESTMODE** Enables LPI timer test mode (reduced test time) 0 = LPI timer test mode disabled (normal operation) 1 = LPI timer test mode enabled	R/W	0b
1	**RX_LPI_MODE** Indicates receiver is in low-power idle mode 0 = Receiver is not in low-power idle mode 1 = Receiver is in low-power idle mode	RO	0b
0	**TX_LPI_MODE** Indicates transmitter is in low-power idle mode 0 = Transmitter is not in low-power idle mode 1 = Transmitter is in low-power idle mode	RO	0b

2.2.13 QSGMII PCS1G TEST PATTERN CONFIGURATION AND STATUS REGISTER

Index (In decimal): EP 5.26 Size: 16 bits

This register provides Jitter test pattern control and status for the QSGMII PCS1G.

Bits	Description	Type	Default
15:8	**JTP Error Count[7:0]** Count of Jitter Test Pattern errors. Counter saturates at FFh and is cleared to zero upon read.	RC	00h
7:5	**RESERVED**	RO	—
4:2	**JTP_SEL[2:0]** Selects the jitter test pattern. Patterns are according to IEEE 802.3 Annex 36A. 000 = Disable transmission of test patterns 001 = High Frequency Test Pattern – repeated transmission of D21.5 code group 010 = Low Frequency Test Pattern – repeated transmission of K28.7 code group 011 = Mixed Frequency Test Pattern – repeated transmission of K28.5 code group 100 = Long Continuous Random Test Pattern – 1524 byte frames 101 = Short Continuous Random Test Pattern – 360 byte frames 110 = RESERVED 111 = RESERVED	R/W	000b
1	**RESERVED**	RO	—
0	**JTP_LOCK** Indicates jitter pattern checker is locked 0 = Jitter pattern checker is not locked 1 = Jitter pattern checker is locked	RO	0b

2.2.14 RX RA FIFO THRESHOLDS 1 REGISTER

Index (In decimal): EP 5.32 Size: 16 bits

This register provides configurable thresholds for the 32-entry QSGMII Rate Adaptation FIFO.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:8	**RX_ALMOST_EMPTY[5:0]** FIFO Almost_Empty Threshold	R/W	0Ch
7:6	**RESERVED**	RO	—
5:0	**RX_EMPTY[5:0]** FIFO Empty Threshold	R/W	00h

2.2.15 RX RA FIFO THRESHOLDS 2 REGISTER

Index (In decimal): EP 5.33 Size: 16 bits

This register provides configurable thresholds for the 32-entry QSGMII Rate Adaptation FIFO.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:8	**RX_HALF_FULL[5:0]** FIFO Half_Full Threshold	R/W	10h
7:6	**RESERVED**	RO	—
5:0	**RX_HALF_EMPTY[5:0]** FIFO Half_Empty Threshold	R/W	10h

2.2.16 RX RA FIFO THRESHOLDS 3 REGISTER

Index (In decimal): EP 5.34 Size: 16 bits

This register provides configurable thresholds for the 32-entry QSGMII Rate Adaptation FIFO.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:8	**RX_ALMOST_FULL[5:0]** FIFO Almost_Full Threshold	R/W	14h
7:6	**RESERVED**	RO	—
5:0	**RX_FULL[5:0]** FIFO Full Threshold	R/W	20h

2.2.17 RX RA FIFO READ COUNT CONFIGURATION REGISTER

Index (In decimal): EP 5.35 Size: 16 bits

This register controls the “sample location” used by the Rate adaption FIFO to pick 1 data byte out of 10 sample data bytes for 100M speed and in similar manner 1 out of 100 for 10M speed.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:8	**RX_100M_READ_COUNT[3:0]** Sample location for 100 Mbps operation	R/W	9h
7	**RESERVED**	RO	—
6:0	**RX_10M_READ_COUNT[6:0]** Sample location for 10 Mbps operation	R/W	63h

2.2.18 RX RA FIFO IFG COUNT REGISTER

Index (In decimal): EP 5.36 Size: 16 bits

When the RA FIFO reaches Almost_Full, the RA FIFO is recentered to the Half_Full level by removing IFG bytes. This register the controls the number of consecutive IFG bytes which must be observed before recentering the RA FIFO.

Bits	Description	Type	Default
15:6	**RESERVED**	RO	—
5:4	**RX_IDLE_REMOVAL_CNT[1:0]** The number of Idle bytes to remove to recenter the FIFO 0h = 1 Idle byte removed 1h = 2 Idle bytes removed 2h = 3 Idle bytes removed 3h = 4 Idle bytes removed	R/W	1h
3:0	**RX_IFG_COUNT[3:0]** The number of consecutive IFG bytes which must be observed before recentering the Rate Adaptation FIFO	R/W	7h

2.2.19 RX RA FIFO STATUS REGISTER

Index (In decimal): EP 5.37 Size: 16 bits

This register provides the status of the QSGMII Rate Adaptation FIFO.

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**RX_RA_FIFO_AFULL** 0 = Not Almost_Full 1 = Almost_Full Threshold is set using RX RA FIFO Thresholds registers.	RC	—
2	**RX_RA_FIFO_FULL** 0 = Not Full 1 = Full Threshold is set using RX RA FIFO Thresholds registers.	RC	—
1	**RX_RA_FIFO_AEMPTY** 0 = Not Almost_Empty 1 = Almost_Empty Threshold is set using RX RA FIFO Thresholds registers.	RC	—
0	**RX_RA_FIFO_EMPTY** 0 = Not Empty 1 = Empty Threshold is set using RX RA FIFO Thresholds registers.	RC	—

2.2.20 TX RA FIFO THRESHOLDS 1 REGISTER

Index (In decimal): EP 5.38 Size: 16 bits

This register provides configurable thresholds for the 32-entry QSGMII Rate Adaptation FIFO.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:8	**TX_ALMOST_EMPTY[5:0]** FIFO Almost_Empty Threshold	R/W	0Ch
7:6	**RESERVED**	RO	—
5:0	**TX_EMPTY[5:0]** FIFO Empty Threshold	R/W	00h

2.2.21 TX RA FIFO THRESHOLDS 2 REGISTER

Index (In decimal): EP 5.39 Size: 16 bits

This register provides configurable thresholds for the 32-entry QSGMII Rate Adaptation FIFO.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:8	**TX_HALF_FULL[5:0]** FIFO Half_Full Threshold	R/W	10h
7:6	**RESERVED**	RO	—
5:0	**TX_HALF_EMPTY[5:0]** FIFO Half_Empty Threshold	R/W	10h

2.2.22 TX RA FIFO THRESHOLDS 3 REGISTER

Index (In decimal): EP 5.40 Size: 16 bits

This register provides configurable thresholds for the 32-entry QSGMII Rate Adaptation FIFO.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:8	**TX_ALMOST_FULL[5:0]** FIFO Almost_Full Threshold	R/W	14h
7:6	**RESERVED**	RO	—
5:0	**TX_FULL[5:0]** FIFO Full Threshold	R/W	20h

2.2.23 TX RA FIFO WRITE COUNT CONFIGURATION REGISTER

Index (In decimal): EP 5.41 Size: 16 bits

This register controls the “sample location” used by the Rate adaption FIFO to pick 1 data byte out of 10 sample data bytes for 100M speed and in similar manner 1 out of 100 for 10M speed.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:8	**TX_100M_WRITE_COUNT[3:0]** Sample location to write for 100 Mbps operation	R/W	4h
7	**RESERVED**	RO	—
6:0	**TX_10M_WRITE_COUNT[6:0]** Sample location to write for 10 Mbps operation	R/W	31h

2.2.24 TX RA FIFO IFG COUNT REGISTER

Index (In decimal): EP 5.42 Size: 16 bits

When the RA FIFO reaches Almost_Full, the RA FIFO is recentered to the Half_Full level by removing IFG bytes. This register the controls the number of consecutive IFG bytes which must be observed before recentering the RA FIFO.

Bits	Description	Type	Default
15:6	**RESERVED**	RO	—
5:4	**TX_IDLE_REMOVAL_CNT[1:0]** The number of Idle bytes to remove to recenter the FIFO 0h = 1 Idle byte removed 1h = 2 Idle bytes removed 2h = 3 Idle bytes removed 3h = 4 Idle bytes removed	R/W	1h
3:0	**TX_IFG_COUNT[3:0]** The number of consecutive IFG bytes which must be observed before recentering the Rate Adaptation FIFO	R/W	7h

2.2.25 TX RA FIFO STATUS REGISTER

Index (In decimal): EP 5.43 Size: 16 bits

This register provides the status of the QSGMII Rate Adaptation FIFO.

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**TX_RA_FIFO_AFULL** 0 = Not Almost_Full 1 = Almost_Full Threshold is set using RX RA FIFO Thresholds registers	RC	—
2	**TX_RA_FIFO_FULL** 0 = Not Full 1 = Full Threshold is set using RX RA FIFO Thresholds registers	RC	—
1	**TX_RA_FIFO_AEMPTY** 0 = Not Almost_Empty 1 = Almost_Empty Threshold is set using RX RA FIFO Thresholds registers	RC	—
0	**TX_RA_FIFO_EMPTY** 0 = Not Empty 1 = Empty Threshold is set using RX RA FIFO Thresholds registers	RC	—

2.2.26 TX RA FIFO RESET REGISTER

Index (In decimal): EP 5.44 Size: 16 bits

This register resets the Tx Rate Adaptation FIFO.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Tx RA FIFO Reset** 1 = Reset the Tx Rate Adaptation FIFO Writing a zero has no effect.	W1S/SC	0b

2.2.27 RX RA FIFO RESET REGISTER

Index (In decimal): EP 5.45 Size: 16 bits

This register resets the Rx Rate Adaptation FIFO.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Rx RA FIFO Reset** 1 = Reset the Rx Rate Adaptation FIFO Writing a zero has no effect.	W1S/SC	0b

2.2.28 RX RA FIFO IN HIGH COUNT REGISTER

Index (In decimal): EP 5.47 Size: 16 bits

Counts the number of packets received to the RA module from the GPHY (MSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**RX_RA_FIFO_IN_COUNT[31:16]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.29 RX RA FIFO IN LOW COUNT REGISTER

Index (In decimal): EP 5.48 Size: 16 bits

Counts the number of packets received to the RA module from the GPHY (LSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**RX_RA_FIFO_IN_COUNT[15:0]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.30 RX RA FIFO OUT HIGH COUNT REGISTER

Index (In decimal): EP 5.49 Size: 16 bits

Counts the number of packets transmitted out of the RA module to SerDes (MSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**RX_RA_FIFO_OUT_COUNT[31:16]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.31 RX RA FIFO OUT LOW COUNT REGISTER

Index (In decimal): EP 5.50 Size: 16 bits

Counts the number of transmitted out of the RA module to SerDes (LSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**RX_RA_FIFO_OUT_COUNT[15:0]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.32 TX RA FIFO IN HIGH COUNT REGISTER

Index (In decimal): EP 5.51 Size: 16 bits

Counts the number of packets received to the RA module from the SerDes (MSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**TX_RA_FIFO_IN_COUNT[31:16]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.33 TX RA FIFO IN LOW COUNT REGISTER

Index (In decimal): EP 5.52 Size: 16 bits

Counts the number of packets received to the RA module from the SerDes (LSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**TX_RA_FIFO_IN_COUNT[15:0]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.34 TX RA FIFO OUT HIGH COUNT REGISTER

Index (In decimal): EP 5.53 Size: 16 bits

Counts the number of packets transmitted out of RA module to the GPHY (MSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**TX_RA_FIFO_OUT_COUNT[31:16]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.35 TX RA FIFO OUT LOW COUNT REGISTER

Index (In decimal): EP 5.54 Size: 16 bits

Counts the number of packets transmitted out of RA module to the GPHY (LSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**TX_RA_FIFO_OUT_COUNT[15:0]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.36 RX RA AEMPTY COUNT HIGH REGISTER

Index (In decimal): EP 5.55 Size: 16 bits

Counts the number times almost empty condition is hit in the GPHY receive and SerDes Tx direction (MSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**RX_RA_AEMPTY_COUNT[31:16]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.37 RX RA AEMPTY COUNT LOW REGISTER

Index (In decimal): EP 5.56 Size: 16 bits

Counts the number times almost empty condition is hit in the GPHY receive and SerDes Tx direction (LSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**RX_RA_AEMPTY_COUNT[15:0]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.38 RX RA AFULL COUNT HIGH REGISTER

Index (In decimal): EP 5.57 Size: 16 bits

Counts the number times almost full condition is hit in the GPHY receive and SerDes Tx direction (MSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**RX_RA_AFULL_COUNT[31:16]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.39 RX RA AFULL COUNT LOW REGISTER

Index (In decimal): EP 5.58 Size: 16 bits

Counts the number times almost full condition is hit in the GPHY receive and SerDes Tx direction (LSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**RX_RA_AFULL_COUNT[15:0]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.40 RX RA EMPTY COUNT REGISTER

Index (In decimal): EP 5.59 Size: 16 bits

Counts the number times empty condition is hit in the GPHY receive and SerDes Tx direction.

Bits	Description	Type	Default
15:0	**RX_RA_EMPTY_COUNT[15:0]**	RC	0000h

2.2.41 RX RA FULL COUNT REGISTER

Index (In decimal): EP 5.60 Size: 16 bits

Counts the number times full condition is hit in the GPHY receive and SerDes Tx direction.

Bits	Description	Type	Default
15:0	**RX_RA_FULL_COUNT[15:0]**	RC	0000h

2.2.42 TX RA AEMPTY COUNT HIGH REGISTER

Index (In decimal): EP 5.61 Size: 16 bits

Counts the number times almost empty condition is hit in the GPHY transmit and SerDes Rx direction (MSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**TX_RA_AEMPTY_COUNT[31:16]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.43 TX RA AEMPTY COUNT LOW REGISTER

Index (In decimal): EP 5.62 Size: 16 bits

Counts the number times almost empty condition is hit in the GPHY transmit and SerDes Rx direction (LSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**TX_RA_AEMPTY_COUNT[15:0]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.44 TX RA AFULL COUNT HIGH REGISTER

Index (In decimal): EP 5.63 Size: 16 bits

Counts the number times almost full condition is hit in the GPHY transmit and SerDes Rx direction (MSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**TX_RA_AFULL_COUNT[31:16]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.45 TX RA AFULL COUNT LOW REGISTER

Index (In decimal): EP 5.64 Size: 16 bits

Counts the number times almost full condition is hit in the GPHY transmit and SerDes Rx direction (LSB 16 bits are mapped here).

Bits	Description	Type	Default
15:0	**TX_RA_AFULL_COUNT[15:0]** **Note:** HI/LO registers will be cleared only when both the corresponding HIGH and LOW count registers are read.	RC	0000h

2.2.46 TX RA EMPTY COUNT REGISTER

Index (In decimal): EP 5.65 Size: 16 bits

Counts the number times empty condition is hit in the GPHY transmit and SerDes Rx direction.

Bits	Description	Type	Default
15:0	**TX_RA_EMPTY_COUNT[15:0]**	RC	0000h

2.2.47 TX RA FULL COUNT REGISTER

Index (In decimal): EP 5.66 Size: 16 bits

Counts the number times full condition is hit in the GPHY transmit and SerDes Rx direction.

Bits	Description	Type	Default
15:0	**TX_RA_FULL_COUNT[15:0]**	RC	0000h

2.2.48 PORT HARD RESET REGISTER

Index (In decimal): EP 5.80 Size: 16 bits

This register resets the Port including all port-specific logic blocks and macros, and sets all related configuration registers to their default state.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Port Hard Reset** 1 = Reset the Port except GPHY and set all Port configuration registers except GPHY to their default state. Writing a zero has no effect.	W1S/SC	0b

2.2.49 PORT SOFT RESET REGISTER

Index (In decimal): EP 5.81 Size: 16 bits

This register resets the Port including all port-specific logic blocks and macros, but does not reset the GPHY or any configuration registers. The GPHY may be soft-reset using the Software Soft Reset in the GPHY.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Port Soft Reset** 1 = Reset the Port but not the GPHY and no configuration registers Writing a zero has no effect.	W1S/SC	0b

2.2.50 PTP TSU INTERRUPT ENABLE REGISTER (PTP_TSU_INT_EN)

Index (In decimal): EP 5.512 Size: 16 bits

This register enables the corresponding bits in the PTP TSU Interrupt Status Register (PTP_TSU_INT_STS).

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**PTP TX Timestamp FIFO Overflow Interrupt Enable (PTP_TX_TS_OVRFL_EN)**	R/W	0b
2	**PTP TX Timestamp Interrupt Enable (PTP_TX_TS_EN)**	R/W	0b
1	**PTP RX Timestamp FIFO Overflow Interrupt Enable (PTP_RX_TS_OVRFL_EN)**	R/W	0b
0	**PTP RX Timestamp Interrupt Enable (PTP_RX_TS_EN)**	R/W	0b

2.2.51 PTP TSU INTERRUPT STATUS REGISTER (PTP_TSU_INT_STS)

Index (In decimal): EP 5.513 Size: 16 bits

This register contains the 1588 TSU interrupt status bits.

Reading this register clears the interrupt sources. RO sources must be cleared at their lower level register.

If enabled in the PTP TSU Interrupt Enable Register (PTP_TSU_INT_EN), these interrupt bits are cascaded into the 1588 TSU x Interrupt bit of the Chip-level Interrupt Status Register. Status bits will still reflect the status of the interrupt source regardless of whether the source is enabled as an interrupt. The 1588 Interrupt Enable bit of the Interrupt Enable Register must be set in order for an actual system level interrupt to occur.

Note: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**PTP TX Timestamp FIFO Overflow Interrupt (PTP_TX_TS_OVRFL_INT)** This interrupt indicates that a packet was transmitted but its egress time and associated data stored could not be stored.	RC	0b
2	**PTP TX Timestamp Interrupt (PTP_TX_TS_INT)** This interrupt indicates that the count of egress timestamps stored is equal to or greater than the Timestamp Count Threshold. This bit is read only and clears once the count falls below the threshold.	RO	0b
1	**PTP RX Timestamp FIFO Overflow Interrupt (PTP_RX_TS_OVRFL_INT)** This interrupt indicates that a packet was received but its ingress time and associated data stored could not be stored.	RC	0b
0	**PTP RX Timestamp Interrupt (PTP_RX_TS_INT)** This interrupt indicates that the count of ingress timestamps stored is equal to or greater than the Timestamp Count Threshold. This bit is read only and clears once the count falls below the threshold.	RO	0b

2.2.52 PTP MODIFICATION ERROR REGISTER (PTP_MOD_ERR)

Index (In decimal): EP 5.514 Size: 16 bits

This register contains packet modification error status. PTP offloads are not available in PTP PCH Mode, both with and without MCH support.

Note: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6	**Reserved Field Overwrite Error** This bit is set if the 4 byte reserved field was not zero when it was written with the ingress timestamp during Ingress Time Insertion into Packet or during Ingress Correction Field Residence Time Adjustment method A. This bit is also set if the 1 byte reserved field was not zero when it was written with the ingress timestamp during Ingress Time Insertion into Packet.	RC	0b
5	**Pdelay_Resp Overwrite Error** This bit is set if the Pdelay_Resp Egress timestamp registers are overwritten (Pdelay_Resp Timestamp Valid was already set) by another egress Pdelay_Resp message before the registers were used by the egress Pdelay_Resp_Follow_Up message. **Note:** If egress Pdelay_Resp_Follow_Up message offloading is not enabled, this bit can be safely ignored.	RC	0b
4	**Pdelay_Req Overwrite Error** This bit is set if the Pdelay_Req Ingress timestamp and correction registers are overwritten (Pdelay_Req Timestamp Valid was already set) by another ingress Pdelay_Req message before the registers were used by the egress Pdelay_Resp or Pdelay_Resp_Follow_Up message. **Note:** If egress Pdelay_Resp or Pdelay_Resp_Follow_Up message offloading is not enabled, this bit can be safely ignored.	RC	0b
3	**Sync Overwrite Error** This bit is set if the Sync Egress timestamp registers are overwritten (Sync Timestamp Valid was already set) by another egress Sync message before the registers were used by the egress Follow_Up message. **Note:** If egress Follow_Up message offloading is not enabled, this bit can be safely ignored.	RC	0b
2	**Pdelay_Resp_Follow_Up Egress Error** This bit is set if the Pdelay_Req Ingress timestamp and correction field registers and/or the Pdelay_Resp Egress timestamp registers are not valid when a Pdelay_Resp_Follow_Up message is transmitted with offloading enabled.	RC	0b
1	**Pdelay_Resp Egress Error** This bit is set if the Pdelay_Req Ingress timestamp and correction field registers are not valid when a Pdelay_Resp message is transmitted with offloading enabled.	RC	0b
0	**Follow_Up Egress Error** This bit is set if the Sync Egress timestamp registers are not valid when a Follow_Up message is transmitted with offloading enabled.	RC	0b

2.2.53 PTP RX USER MAC ADDRESS HIGH REGISTER (PTP_RX_USER_MAC_HI)

Index (In decimal): EP 5.515 Size: 16 bits

This read/write register combined with the PTP RX User MAC Address Mid/Low Registers (PTP_RX_USER_MAC_MID/LO) forms the 48-bit user defined MAC address. This register contains the upper 16 bits of the user MAC address.

The User MAC address can be enabled for each protocol via their respective User Defined MAC Address Enable bits (L2_USER_MAC_EN, IPV4_USER_MAC_EN or IPV6_USER_MAC_EN) in the corresponding Address Enable registers (PTP_RX_PARSE_L2_ADDR_EN, PTP_RX_PARSE_IP_ADDR_EN).

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**User MAC Address (USER_MAC[47:32])** This field contains the high 16 bits of the user defined MAC address used for PTP packet detection. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h

2.2.54 PTP RX USER MAC ADDRESS MID REGISTER (PTP_RX_USER_MAC_MID)

Index (In decimal): EP 5.516 Size: 16 bits

This register contains the middle 16 bits of the user MAC address.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**User MAC Address (USER_MAC[31:16]** This field contains the middle 16 bits of the user defined MAC address used for PTP packet detection. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h

2.2.55 PTP RX USER MAC ADDRESS LOW REGISTER (PTP_RX_USER_MAC_LO)

Index (In decimal): EP 5.517 Size: 16 bits

This register contains the lower 16 bits of the user MAC address.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**User MAC Address (USER_MAC[15:0]** This field contains the low 16 bits of the user defined MAC address used for PTP packet detection. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h

2.2.56 PTP RX USER IP ADDRESS REGISTERS (PTP_RX_USER_IP_ADDRX)

Index (In decimal): x = 0: EP 5.518
x = 1: EP 5.519
x = 2: EP 5.520
x = 3: EP 5.521
x = 4: EP 5.522
x = 5: EP 5.523
x = 6: EP 5.524
x = 7: EP 5.525

Size: 16 bits

These read/write registers provide the 32-bit (IPv4) or 128-bit (IPv6) user defined IP address. Each register contains 16 bits of the address.

The User IP address can be enabled for the IPv4 or IPv6 protocols via their respective User Defined IP Address Enable bits in the PTP RX Parsing IP Format Address Enable Register (PTP_RX_PARSE_IP_ADDR_EN).

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Register	Bits	Description	Type	Default
x = 7 x = 6 x = 5 x = 4	15:0	**IP Address[127:112]** **IP Address[111:96]** **IP Address[95:80]** **IP Address[79:64]** These fields contain the upper 64 bits of the 128 bit user defined IPv6 address and the entire 32 bits of the user defined IPv4 address used for PTP packet detection. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h 0000h 0000h 0000h

Register	Bits	Description	Type	Default
x = 3 x = 2 x = 1 x = 0	15:0	**IP Address[63:48]** **IP Address[47:32]** **IP Address[31:16]** **IP Address[15:0]** These fields contain the lower 64 bits of the 128 bit user defined IPv6 address used for PTP packet detection. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h 0000h 0000h 0000h

2.2.57 PTP RX USER IP MASK REGISTERS (PTP_RX_USER_IP_MASKX)

Index (In decimal): x = 0: EP 5.526
x = 1: EP 5.527
x = 2: EP 5.528
x = 3: EP 5.529
x = 4: EP 5.530
x = 5: EP 5.531
x = 6: EP 5.532
x = 7: EP 5.533

Size: 16 bits

These read/write registers provide a 32-bit (IPv4) or 128-bit (IPv6) mask for the user defined IP address. Each register contains 16 bits of the mask.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Register	Bits	Description	Type	Default
x = 7 x = 6 x = 5 x = 4	15:0	**IP Mask[127:112]** **IP Mask[111:96]** **IP Mask[95:80]** **IP Mask[79:64]** These fields contain the upper 64 bits of the 128 bit user defined IPv6 mask and the entire 32 bits of the user defined IPv4 mask used for PTP packet detection. 0 = Bit is ignored (considered a match) 1 = Bit is compared **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	FFFFh FFFFh FFFFh FFFFh
x = 3 x = 2 x = 1 x = 0	15:0	**IP Mask[63:48]** **IP Mask[47:32]** **IP Mask[31:16]** **IP Mask[15:0]** These fields contain the lower 64 bits of the 128 bit user defined IPv6 mask used for PTP packet detection. 0 = Bit is ignored (considered a match) 1 = Bit is compared **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	FFFFh FFFFh FFFFh FFFFh

2.2.58 VLAN ETHERNET TYPE ID REGISTER (VLAN_TYPE_ID)

Index (In decimal): EP 5.534 Size: 16 bits

This read/write register specifies an alternate VLAN type ID.

This register is common for the ingress and egress directions.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**VLAN Ethernet Type [15:0]** **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	8100h

2.2.59 VLAN 1 TYPE/ID REGISTER (VLAN1_TYPE_ID)

Index (In decimal): EP 5.535 Size: 16 bits

This read/write register configures the Ethernet type and VID for VLAN 1.

This register is common for the ingress and egress directions.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:12	**VLAN Ethernet Type Select [1:0]** When VLAN checking enabled, this field is used to select the Ethernet Type. 11 = The fixed value of 0x88a8 is used. 10 = The value in the VLAN Ethernet Type ID Register (VLAN_TYPE_ID) is used. 01 = The value in the VLAN Ethernet Type ID Register (VLAN_TYPE_ID) is used. 00 = The fixed value of 0x8100 is used. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00b
11:0	**VLAN ID Value [11:0]** This field contains the VLAN ID. Each bit may be masked using the VLAN ID Mask field. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000h

2.2.60 VLAN 1 ID MASK REGISTER (VLAN1_ID_MASK)

Index (In decimal): EP 5.536 Size: 16 bits

This read/write register configures the VID mask for VLAN 1.

This register is common for the ingress and egress directions.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:0	**VLAN ID Mask [11:0]** This field contains the VLAN ID Mask. 0 = bit is ignored (considered a match) 1 = bit is compared **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000h

2.2.61 VLAN 1 VID RANGE UPPER REGISTER (VLAN1_VID_RANGE_UP)

Index (In decimal): EP 5.537 Size: 16 bits

This read/write register configures VID range checking for VLAN 1.

This register is common for the ingress and egress directions.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:13	**RESERVED**	RO	—
12	**VLAN ID Range Enable** When set, this field enables VLAN ID range checking. When cleared, the VLAN ID Value is checked. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
11:0	**VLAN ID Upper Range [11:0]** This field contains the VLAN ID range upper limit. This field is used along with the VLAN ID range lower limit field. Values are inclusive. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000h

2.2.62 VLAN 1 VID RANGE LOWER REGISTER (VLAN1_VID_RANGE_LO)

Index (In decimal): EP 5.538 Size: 16 bits

This read/write register configures VID range checking for VLAN 1.

This register is common for the ingress and egress directions.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:0	**VLAN ID Lower Range [11:0]** This field contains the VLAN ID range lower limit. This field is used along with the VLAN ID range upper limit field. Values are inclusive. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000h

2.2.63 VLAN 2 TYPE/ID REGISTER (VLAN2_TYPE_ID)

Index (In decimal): EP 5.539 Size: 16 bits

This read/write register configures the Ethernet type and VID for VLAN 2.

This register is common for the ingress and egress directions.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:12	**VLAN Ethernet Type Select [1:0]** When VLAN checking enabled, this field is used to select the Ethernet Type. 11 = The fixed value of 0x88a8 is used. 10 = The value in the VLAN Ethernet Type ID Register (VLAN_TYPE_ID) is used. 01 = The value in the VLAN Ethernet Type ID Register (VLAN_TYPE_ID) is used. 00 = The fixed value of 0x8100 is used. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00b
11:0	**VLAN ID Value [11:0]** This field contains the VLAN ID. Each bit may be masked using the VLAN ID Mask field. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000h

2.2.64 VLAN 2 ID MASK REGISTER (VLAN2_ID_MASK)

Index (In decimal): EP 5.540 Size: 16 bits

This read/write register configures the VID mask for VLAN 2.

This register is common for the ingress and egress directions.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:0	**VLAN ID Mask [11:0]** This field contains the VLAN ID Mask. 0 = Bit is ignored (considered a match) 1 = Bit is compared **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000h

2.2.65 VLAN 2 VID RANGE UPPER REGISTER (VLAN2_VID_RANGE_UP)

Index (In decimal): EP 5.541 Size: 16 bits

This read/write register configures VID range checking for VLAN 2.

This register is common for the ingress and egress directions.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:13	**RESERVED**	RO	—
12	**VLAN ID Range Enable** When set, this field enables VLAN ID range checking. When cleared, the VLAN ID Value is checked. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
11:0	**VLAN ID Upper Range [11:0]** This field contains the VLAN ID range upper limit. This field is used along with the VLAN ID range lower limit field. Values are inclusive. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000h

2.2.66 VLAN 2 VID RANGE LOWER REGISTER (VLAN2_VID_RANGE_LO)

Index (In decimal): EP 5.542 Size: 16 bits

This read/write register configures VID range checking for VLAN 2.

This register is common for the ingress and egress directions.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:0	**VLAN ID Lower Range [11:0]** This field contains the VLAN ID range lower limit. This field is used along with the VLAN ID range upper limit field. Values are inclusive. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000h

2.2.67 LLC ETHERNET TYPE ID REGISTER (LLC_TYPE_ID)

Index (In decimal): EP 5.543 Size: 16 bits

This read/write register specifies the EtherType for LCC.

This register is common for the ingress and egress directions.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**LLC Ethernet Type [15:0]** **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	05DCh

2.2.68 PTP RX LATENCY 10MBPS REGISTER (PTP_RX_LATENCY_10)

Index (In decimal): EP 5.544 Size: 16 bits

Bits	Description	Type	Default
15:0	**RX Latency 10Mbps (RX_LATENCY_10[15:0])** This field specifies the ingress delay in nanoseconds between the network medium while operating at 10 Mbps and the PTP timestamp point. The setting is used to adjust the internally captured 1588 Local Time Counter value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. The typical value is 8874 ns. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	22AAh

2.2.69 PTP TX LATENCY 10MBPS REGISTER (PTP_TX_LATENCY_10)

Index (In decimal): EP 5.545 Size: 16 bits

Bits	Description	Type	Default
15:0	**TX Latency 10Mbps (TX_LATENCY_10[15:0])** This field specifies the egress delay in nanoseconds between the PTP timestamp point and the network medium while operating at 10 Mbps. The setting is used to adjust the internally captured 1588 Local Time Counter value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. The typical value is 11850 ns. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	2E4Ah

2.2.70 PTP RX LATENCY 100MBPS REGISTER (PTP_RX_LATENCY_100)

Index (In decimal): EP 5.546 Size: 16 bits

Bits	Description	Type	Default
15:0	**RX Latency 100Mbps (RX_LATENCY_100[15:0])** This field specifies the ingress delay in nanoseconds between the network medium while operating at 100 Mbps and the PTP timestamp point. The setting is used to adjust the internally captured 1588 Local Time Counter value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. The typical value is 2346 ns. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	092Ah

2.2.71 PTP TX LATENCY 100MBPS REGISTER (PTP_TX_LATENCY_100)

Index (In decimal): EP 5.547 Size: 16 bits

Bits	Description	Type	Default
15:0	**TX Latency 100Mbps (TX_LATENCY_100[15:0])** This field specifies the egress delay in nanoseconds between the PTP timestamp point and the network medium while operating at 100 Mbps. The setting is used to adjust the internally captured 1588 Local Time Counter value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. The typical value is 705 ns. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	02C1h

2.2.72 PTP RX LATENCY 1000MBPS REGISTER (PTP_RX_LATENCY_1000)

Index (In decimal): EP 5.548 Size: 16 bits

Bits	Description	Type	Default
15:0	**RX Latency 1000Mbps (RX_LATENCY_1000[15:0])** This field specifies the ingress delay in nanoseconds between the network medium while operating at 1000 Mbps and the PTP timestamp point. The setting is used to adjust the internally captured 1588 Local Time Counter value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. The typical value is 429 ns. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	01ADh

2.2.73 PTP TX LATENCY 1000MBPS REGISTER (PTP_TX_LATENCY_1000)

Index (In decimal): EP 5.549 Size: 16 bits

Bits	Description	Type	Default
15:0	**TX Latency 1000Mbps (TX_LATENCY_1000[15:0])** This field specifies the egress delay in nanoseconds between the PTP time-stamp point and the network medium while operating at 1000 Mbps. The setting is used to adjust the internally captured 1588 Local Time Counter value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. The typical value is 201 ns. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00C9

2.2.74 PTP ASYMMETRY DELAY HIGH REGISTER (PTP_ASYM_DLY_HI)

Index (In decimal): EP 5.550 Size: 16 bits

This register contains the upper 16 bits of the delay asymmetry.

When combined with the lower 16 bits, this forms a signed number.

The sub-nanoseconds portion of the delay asymmetry is fixed at 0.

Bits	Description	Type	Default
15:0	**Port Delay Asymmetry (DELAY_ASYM[31:16])** This field specifies the previously known delay asymmetry in nanoseconds. This is a signed 2's complement number. Positive values occur when the master-to-slave or responder-to-requestor propagation time is longer than the slave-to-master or requestor-to-responder propagation time. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h

2.2.75 PTP ASYMMETRY DELAY LOW REGISTER (PTP_ASYM_DLY_LO)

Index (In decimal): EP 5.551 Size: 16 bits

This register contains the lower 16 bits of the delay asymmetry.

Bits	Description	Type	Default
15:0	**Port Delay Asymmetry (DELAY_ASYM[15:0])** This field specifies the previously known delay asymmetry in nanoseconds. This is a signed 2's complement number. Positive values occur when the master-to-slave or responder-to-requestor propagation time is longer than the slave-to-master or requestor-to-responder propagation time. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h

2.2.76 PTP PEER DELAY HIGH REGISTER (PTP_PEERDLY_HI)

Index (In decimal): EP 5.552 Size: 16 bits

This register contains the upper 16 bits of the RX peer delay.

When combined with the lower 16 bits, this forms an unsigned number and is either zero or a positive value.

The sub-nanoseconds portion of the RX peer delay is fixed at 0.

Bits	Description	Type	Default
15:0	**RX Peer Delay (RX_PEER_DELAY[31:16])** This field specifies the measured peer delay in nanoseconds used during peer-to-peer mode.	R/W	0000h

2.2.77 PTP PEER DELAY LOW REGISTER (PTP_PEERDLY_LO)

Index (In decimal): EP 5.553 Size: 16 bits

This register contains the lower 16 bits of the RX peer delay.

Bits	Description	Type	Default
15:0	**RX Peer Delay (RX_PEER_DELAY[15:0])** This field specifies the measured peer delay in nanoseconds used during peer-to-peer mode.	R/W	0000h

2.2.78 PTP CAPTURE INFORMATION REGISTER (PTP_CAP_INFO)

Index (In decimal): EP 5.554 Size: 16 bits

This read only register provides information about transmit and receive capture buffers.

Bits	Description	Type	Default
15:12	**PTP TX Timestamp Count Threshold (PTP_TX_TS_CNT_THRES[3:0])** An interrupt is generated whenever the TX Timestamp Count equals or exceeds this field.	R/W	1h
11:8	**PTP TX Timestamp Count (PTP_TX_TS_CNT[3:0])** This field indicates how many transmit timestamps are available to be read. It is incremented when a PTP packet is transmitted and decremented when the PTP_TX_MSG_HEADER2 register is read.	RO	0h
7:4	**PTP RX Timestamp Count Threshold (PTP_RX_TS_CNT_THRES[3:0])** An interrupt is generated whenever the RX Timestamp Count equals or exceeds this field.	R/W	1h
3:0	**PTP RX Timestamp Count (PTP_RX_TS_CNT[3:0])** This field indicates how many receive timestamps are available to be read. It is incremented when a PTP packet is received and decremented when the PTP_RX_MSG_HEADER2 register is read.	RO	0h

2.2.79 PTP TX USER MAC ADDRESS HIGH REGISTER (PTP_TX_USER_MAC_HI)

Index (In decimal): EP 5.555 Size: 16 bits

This read/write register combined with the PTP TX User MAC Address Mid/Low Registers (PTP_TX_USER_MAC_MID/LO) forms the 48-bit user defined MAC address. This register contains the upper 16 bits of the user MAC address.

The User MAC address can be enabled for each protocol via their respective User Defined MAC Address Enable bits (L2_USER_MAC_EN, IPV4_USER_MAC_EN or IPV6_USER_MAC_EN) in the corresponding Address Enable registers (PTP_TX_PARSE_L2_ADDR_EN, PTP_TX_PARSE_IP_ADDR_EN).

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**User MAC Address (USER_MAC[47:32])** This field contains the high 16 bits of the user defined MAC address used for PTP packet detection. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h

2.2.80 PTP TX USER MAC ADDRESS MID REGISTER (PTP_TX_USER_MAC_MID)

Index (In decimal): EP 5.556 Size: 16 bits

This register contains the middle 16 bits of the user MAC address.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**User MAC Address (USER_MAC[31:16]** This field contains the middle 16 bits of the user defined MAC address used for PTP packet detection. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h

2.2.81 PTP TX USER MAC ADDRESS LOW REGISTER (PTP_TX_USER_MAC_LO)

Index (In decimal): EP 5.557 Size: 16 bits

This register contains the lower 16 bits of the user MAC address.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**User MAC Address (USER_MAC[15:0]** This field contains the low 16 bits of the user defined MAC address used for PTP packet detection. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h

2.2.82 PTP TX USER IP ADDRESS REGISTERS (PTP_TX_USER_IP_ADDRX)

Index (In decimal): x = 0: EP 5.558
x = 1: EP 5.559
x = 2: EP 5.560
x = 3: EP 5.561
x = 4: EP 5.562
x = 5: EP 5.563
x = 6: EP 5.564
x = 7: EP 5.565

Size: 16 bits

These read/write registers provide the 32-bit (IPv4) or 128-bit (IPv6) user defined IP address. Each register contains 16 bits of the address.

The User IP address can be enabled for the IPv4 or IPv6 protocols via their respective User Defined IP Address Enable bits in the PTP TX Parsing IP Format Address Enable Register (PTP_TX_PARSE_IP_ADDR_EN).

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Register	Bits	Description	Type	Default
x = 7 x = 6 x = 5 x = 4	15:0	**IP Address[127:112]** **IP Address[111:96]** **IP Address[95:80]** **IP Address[79:64]** These fields contain the upper 64 bits of the 128 bit user defined IPv6 address and the entire 32 bits of the user defined IPv4 address used for PTP packet detection. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h 0000h 0000h 0000h
x = 3 x = 2 x = 1 x = 0	15:0	**IP Address[63:48]** **IP Address[47:32]** **IP Address[31:16]** **IP Address[15:0]** These fields contain the lower 64 bits of the 128 bit user defined IPv6 address used for PTP packet detection. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h 0000h 0000h 0000h

2.2.83 PTP TX USER IP MASK REGISTERS (PTP_TX_USER_IP_MASKX)

Index (In decimal): x = 0: EP 5.566
x = 1: EP 5.567
x = 2: EP 5.568
x = 3: EP 5.569
x = 4: EP 5.570
x = 5: EP 5.571
x = 6: EP 5.572
x = 7: EP 5.573

Size: 16 bits

These read/write registers provide a 32-bit (IPv4) or 128-bit (IPv6) mask for the user defined IP address. Each register contains 16 bits of the mask.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Register	Bits	Description	Type	Default
x = 7 x = 6 x = 5 x = 4	15:0	**IP Mask[127:112]** **IP Mask[111:96]** **IP Mask[95:80]** **IP Mask[79:64]** These fields contain the upper 64 bits of the 128 bit user defined IPv6 mask and the entire 32 bits of the user defined IPv4 mask used for PTP packet detection. 0 = Bit is ignored (considered a match) 1 = Bit is compared **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	FFFFh FFFFh FFFFh FFFFh
x = 3 x = 2 x = 1 x = 0	15:0	**IP Mask[63:48]** **IP Mask[47:32]** **IP Mask[31:16]** **IP Mask[15:0]** These fields contain the lower 64 bits of the 128 bit user defined IPv6 mask used for PTP packet detection. 0 = Bit is ignored (considered a match) 1 = Bit is compared **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	FFFFh FFFFh FFFFh FFFFh

2.2.84 PTP RX PARSING CONFIGURATION REGISTER (PTP_RX_PARSE_CONFIG)

Index (In decimal): EP 5.578 Size: 16 bits

This register is used to configure the PTP receive message detection.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15	**IPv6 Fragments Enable** When enabled, IPv6 Fragments are considered eligible for matching. IPv6 Fragments are known by the presence of the Fragment Extension Header on all Fragments. This function must normally be Disabled. 1 = Enable 0 = Disabled (normal mode) **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0
14	**Peer/Non-peer MAC/IP DA Mixing** When cleared, the MAC and IP Destination Addresses for peer delay messages and non-peer delay messages must match those assigned by the PTP specification for peer delay messages and non-peer delay messages respectively. When set, either destination address may be used for either peer delay messages or non-peer delay messages. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
13	**User IP DA Peer/Non-peer** When the Peer/Non-peer MAC/IP DA Mixing bit is cleared, this bit specifies whether the user defined IP Destination Address is used for peer or non-peer IPv4 and IPv6 formatted messages. 0 = Peer messages 1 = Non-peer messages When the Peer/Non-peer MAC/IP DA Mixing bit is set, the user defined IP Destination Address is used for both peer and non-peer IPv4 and IPv6 formatted messages. **Note 1:** This bit does not affect the IP Source Address matching, which, if enabled, matches for Peer and Non-peer messages. **2:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

Bits	Description	Type	Default
12	**User MAC DA Peer/Non-peer** When the Peer/Non-peer MAC/IP DA Mixing bit is cleared, this bit specifies whether the user defined MAC Destination Address is used for peer or non-peer Layer2, IPv4 and IPv6 formatted PTP messages. 0 = Peer messages 1 = Non-peer messages When the Peer/Non-peer MAC/IP DA Mixing bit is set, the user defined MAC Destination Address is used for both peer and non-peer Layer2, IPv4 and IPv6 formatted PTP messages. **Note 1:** This bit does not affect the MAC Source Address matching, which, if enabled, matches for Peer and Non-peer messages. **2:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
11	**MAC Destination Address Enable (MAC_DA_EN)** This bit enables the checking of the MAC Destination Address in Layer2, IPv4 and IPv6 formatted PTP messages. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
10:8	**User MAC DA Mode** These three bits select the address match mode for the MAC Destination Address in Layer2, IPv4 and IPv6 formatted PTP messages. One or multiple bits can be set allowing any combination of match types. Bit 0: match the 48 bit address Bit 1: match any unicast address Bit 2: match any multicast address **Note 1:** These bits do not affect the MAC Source Address matching, which, if enabled, always matches against the 48 bit address. **2:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000b
7	**IPv4 Fragments Enable** When enabled, IPv4 Fragments are considered eligible for matching. IPv4 Fragments are known by the values of the Fragments Offset and MF fields in the IPv4 header on all Fragments. This function must normally be Disabled. 1 = Enable 0 = Disabled (normal mode) **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
6	**UDP Source Port Number Enable** When set, the UDP source port number specified in the PTP RX Parsing UDP Source Port Register (PTP_RX_PARSE_UDP_SRC_PORT) is checked. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

Bits	Description	Type	Default
5	**UDP Destination Port Number Enable** When set, the UDP destination port number specified in the PTP RX Parsing UDP Destination Port Register (PTP_RX_PARSE_UDP_DEST_PORT) is checked. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
4	**MAC/IP Address Consistency Checking** When cleared, the MAC and IP Destination Addresses are independently tested. When set, the MAC Destination Address must be consistent with the corresponding IP Destination Address. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
3	**Enable Other Routing Headers** This bit allows the usage of IPv6 Routing headers other than type 0 and 2 when validating the UDP checksum for PTP frame parsing. When cleared, IPv6 Routing headers other than type 0 and 2 are not supported and the checksum is not validated and the frame is not timestamped. When set, IPv6 Routing headers other than type 0 and 2 are skipped, if the Segments Left field in the header is zero, otherwise, the checksum is not validated and the frame is not timestamped. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
2	**IPv6 Enable (IPV6_EN)** This bit enables the detection of the UDP/IPv6 formatted PTP messages. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
1	**IPv4 Enable (IPV4_EN)** This bit enables the detection of the UDP/IPv4 formatted PTP messages. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
0	**Layer 2 Enable (LAYER2_EN)** This bit enables the detection of the Layer 2 formatted PTP messages. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b

2.2.85 PTP RX PARSING VLAN CONFIGURATION REGISTER (PTP_RX_PARSE_VLAN_CONFIG)

Index (In decimal): EP 5.579 Size: 16 bits

This register is used to configure the VLAN parsing for PTP receive messages.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6:4	**VLAN Tag Count** When VLAN checking is enabled, this field specifies the expected number of VLAN tags. 000 = No VLAN tags allowed 001 = Exactly one VLAN tag expected 010 = Exactly two VLAN tags expected 101 = At least one VLAN tags expected 110 = At least two VLAN tags expected 111 = Any amount of VLAN tags allowed Others = Reserved **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000b
3	**RESERVED**	RO	—
2	**VLAN Checking Enable** When set, the number and contents of the VLAN tags is checked. When cleared, VLAN tags are parsed but skipped. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
1	**VLAN 2 Checking Enable** When set, the EtherType and VID value of VLAN 2 is checked. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
0	**VLAN 1 Checking Enable** When set, the EtherType and VID value of VLAN 1 is checked. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

2.2.86 PTP RX PARSING LAYER2 FORMAT ADDRESS ENABLE REGISTER (PTP_RX_PARSE_L2_ADDR_EN)

Index (In decimal): EP 5.580 Size: 16 bits

This register is used to enable MAC addresses for Layer 2 formatted PTP receive messages.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**Layer 2 MAC Destination Address 1 Enable (L2_MAC_DA1_EN)** This bit enables the MAC Destination Address of 01:80:C2:00:00:0E for Layer 2 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
2	**Layer 2 MAC Destination Address 2 Enable (L2_MAC_DA2_EN)** This bit enables the MAC Destination Address of 01:1B:19:00:00:00 for Layer 2 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
1:0	**User Defined Layer 2 MAC Address Enable (L2_USER_MAC_EN)** These bits enable a user defined Layer 2 MAC address for Layer 2 PTP messages. The address is defined via the PTP RX User MAC Address High/Mid/Low Registers (PTP_RX_USER_MAC_HI/MID/LO). The user defined MAC address may be enabled for the destination or source address as follows: 11 = Source/Destination address 10 = Source address 01 = Destination address 00 = Neither **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00b

2.2.87 PTP RX PARSING IP FORMAT ADDRESS ENABLE REGISTER (PTP_RX_PARSE_IP_ADDR_EN)

Index (In decimal): EP 5.581 Size: 16 bits

This register is used to enable MAC and IP addresses for IPv4 and IPv6 formatted PTP receive messages.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13	**IP Destination Address Enable (IP_DA_EN)** This bit enables the checking of the IP Destination Address in PTP messages for both IPv4 and IPv6 formats. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
12	**IP Destination Address 1 Enable (IP_DA1_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:81 and the IPv4 Destination Address of 224.0.1.129 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:81 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:181 for IPv6 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
11	**IP Destination Address 2 Enable (IP_DA2_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:82 and the IPv4 Destination Address of 224.0.1.130 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:82 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:182 for IPv6 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
10	**IP Destination Address 3 Enable (IP_DA3_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:83 and the IPv4 Destination Address of 224.0.1.131 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:83 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:183 for IPv6 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
9	**IP Destination Address 4 Enable (IP_DA4_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:84 and the IPv4 Destination Address of 224.0.1.132 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:84 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:184 for IPv6 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

Bits	Description	Type	Default
8	**IP Destination Address 5 Enable (IP_DA5_EN)** This bit enables the MAC Destination Address of 01:00:5e:00:00:6B and the IPv4 Destination Address of 224.0.0.107 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:00:6B and the IPv6 Destination Address of FF02:0:0:0:0:0:0:6B for IPv6 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
7:6	**User Defined IPv6 MAC Address Enable (IPV6_USER_MAC_EN)** These bits enable a user defined MAC address for IPv6 PTP messages. The address is defined via the PTP RX User MAC Address High/Mid/Low Registers (PTP_RX_USER_MAC_HI/MID/LO). The user defined MAC address may be enabled for the destination or source address as follows: 11 = Source/Destination address 10 = Source address 01 = Destination address 00 = Neither **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00b
5:4	**User Defined IPv6 IP Address Enable (IPV6_USER_IP_EN)** These bits enable a user defined MAC IP address for IPv6 PTP messages. The address is defined via the PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) as masked by the PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx). The user defined IP address may be enabled for the destination or source address as follows: 11 = Source/Destination address 10 = Source address 01 = Destination address 00 = Neither **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00b
3:2	**User Defined IPv4 MAC Address Enable (IPV4_USER_MAC_EN)** These bits enable a user defined MAC address for IPv4 PTP messages. The address is defined via the PTP RX User MAC Address High/Mid/Low Registers (PTP_RX_USER_MAC_HI/MID/LO). The user defined MAC address may be enabled for the destination or source address as follows: 11 = Either source or destination address 10 = Source address 01 = Destination address 00 = Neither **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00b

Bits	Description	Type	Default
1:0	**User Defined IPv4 IP Address Enable (IPV4_USER_IP_EN)** These bits enable a user defined MAC IP address for IPv4 PTP messages. The address is defined via the PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) as masked by the PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx). The user defined IP address may be enabled for the destination or source address as follows: 11 = Either source or destination address 10 = Source address 01 = Destination address 00 = Neither **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00b

2.2.88 PTP RX PARSING UDP SOURCE PORT REGISTER (PTP_RX_PARSE_UDP_SRC_PORT)

Index (In decimal): EP 5.582 Size: 16 bits

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**UDP Source Port Number (UDP_SOURCE_PORT[15:0])** This field specifies the UDP source port number. If UDP Source Port Number Enable is set, the UDP source port number in the frame must match the value in this field in order for the frame to be considered a PTP frame. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h

2.2.89 PTP RX PARSING UDP DESTINATION PORT REGISTER (PTP_RX_PARSE_UDP_DEST_PORT)

Index (In decimal): EP 5.583 Size: 16 bits

This register is used to configure the PTP receive message detection.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**UDP Destination Port Number (UDP_DEST_PORT[15:0])** This field specifies the UDP destination port number. If UDP Destination Port Number Enable is set, the UDP destination port number in the frame must match the value in this field in order for the frame to be considered a PTP frame. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	319

2.2.90 PTP RX VERSION REGISTER (PTP_RX_VERSION)

Index (In decimal): EP 5.584 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:8	**PTP Version Upper Range (PTP_VERSION_UP[7:0])** This field contains the PTP version range upper limit. This field is used along with the PTP version range lower limit field. Values are inclusive. The upper four bits correspond to the versionPTP message field, while the lower four bits correspond to the minorVersionPTP message field. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	20h
7:0	**PTP Version Lower Range (PTP_VERSION_LO[7:0])** This field contains the PTP version range lower limit. This field is used along with the PTP version range upper limit field. Values are inclusive. The upper four bits correspond to the versionPTP message field, while the lower four bits correspond to the minorVersionPTP message field. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	20h

2.2.91 PTP RX DOMAIN/DOMAIN RANGE LOWER REGISTER (PTP_RX_DOMAIN_DOMAIN_LO)

Index (In decimal): EP 5.585 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15	**PTP Domain Range Enable (PTP_DOMAIN_RANGE_EN)** When this bit is cleared, the domainNumber in the PTP message is checked against the masked value in PTP Domain (PTP_DOMAIN[7:0]). When this bit is set, domainNumber range checking is used. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
14:8	**RESERVED**	RO	—
7:0	**PTP Domain (PTP_DOMAIN[7:0])** **PTP Domain Lower Range (PTP_DOMAIN_LO[7:0])** This field has two uses based on the PTP Domain Range Enable (PTP_DOMAIN_RANGE_EN). This field contains the PTP domain in use. Each bit may be masked using the PTP Domain Mask field. This field contains the PTP domain range lower limit. This field is used along with the PTP domain upper limit field. Values are inclusive. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00h

2.2.92 PTP RX DOMAIN MASK/DOMAIN RANGE UPPER REGISTER (PTP_RX_DOMAIN_MASK_DOMAIN_UP)

Index (In decimal): EP 5.586 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**PTP Domain Mask (PTP_DOMAIN_MASK)** **PTP Domain Upper Range (PTP_DOMAIN_UP[7:0])** This field has two uses based on the PTP Domain Range Enable (PTP_DOMAIN_RANGE_EN) This field contains the PTP Domain Mask. 0 = Bit is ignored (considered a match) 1 = Bit is compared This field contains the PTP domain range upper limit. This field is used along with the PTP domain range lower limit field. Values are inclusive. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00h

2.2.93 PTP RX SDOID/SDOID RANGE LOWER REGISTER (PTP_RX_SDOID_SDOID_LO)

Index (In decimal): EP 5.587 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15	**PTP SdoId Range Enable (PTP_SDOID_RANGE_EN)** When this bit is cleared, the majorSdoId and minorSdoId fields in the PTP message are checked against the masked value in PTP SdoId (PTP_SDOID[11:0]). When this bit is set, majorSdoId and minorSdoId range checking is used. The majorSdoId and minorSdoId fields are concatenate and treated as a 12 bit value. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
14:12	**RESERVED**	RO	—
11:0	**PTP SdoId (PTP_SDOID[11:0])** **PTP SdoId Lower Range (PTP_SDOID_LO[11:0])** This field has two uses based on the PTP SdoId Range Enable (PTP_SDOID_RANGE_EN). This field contains the PTP SdoId in use. Each bit may be masked using the PTP SdoId Mask field. This field contains the PTP SdoId range lower limit. This field is used along with the PTP SdoId upper limit field. Values are inclusive. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00h

2.2.94 PTP RX SDOID MASK/SDOID RANGE UPPER REGISTER (PTP_RX_SDOID_MASK_SDOID_UP)

Index (In decimal): EP 5.588 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:0	**PTP SdoId Mask (PTP_SDOID_MASK)** **PTP SdoId Upper Range (PTP_SDOID_UP[7:0])** This field has two uses based on the PTP SdoId Range Enable (PTP_SDOID_RANGE_EN) This field contains the PTP SdoId Mask. 0 = bit is ignored (considered a match) 1 = bit is compared This field contains the PTP SdoId range upper limit. This field is used along with the PTP SdoId range lower limit field. Values are inclusive. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00h

2.2.95 PTP RX TIMESTAMP ENABLE REGISTER (PTP_RX_TIMESTAMP_EN)

Index (In decimal): EP 5.589 Size: 16 bits

This register is used to enable PTP receive message timestamping.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**PTP Message Type Enable (PTP_MESSAGE_EN[15:0])** These bits individually enable timestamping of their respective message types. Bit 0 of this field corresponds to a message type value of 0 (Sync), bit 1 to message type value 1 (Delay_Req), etc. Typically Sync, Delay_Req, Pdelay_Req and Pdelay_Resp messages are enabled.	R/W	0000h

2.2.96 PTP RX TIMESTAMP CONFIGURATION REGISTER (PTP_RX_TIMESTAMP_CONFIG)

Index (In decimal): EP 5.590 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**PTP Allow UDPv6 Zero Checksum (PTP_UDPV6_ZERO_CHKSUM_EN)** When this bit is set, a zero checksum value for IPv6/UDP frames is considered valid.	R/W	0b
2	**PTP Alternate Master Enable (PTP_ALT_MASTER_EN)** When this bit is set, the alternateMasterFlag in the PTP message is checked for a zero value. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
1	**PTP UDP Checksum Check Disable (PTP_UDP_CHKSUM_DIS)** When this bit is cleared, ingress times are not saved if the frame has an invalid UDP checksum. When this bit is set, the UDP checksum check is bypassed and the ingress time is saved regardless. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
0	**PTP FCS Check Disable (PTP_FCS_DIS)** When this bit is cleared, ingress times are not saved if the frame has an invalid FCS. When this bit is set, the FCS check is bypassed. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

2.2.97 PTP RX MODIFICATION REGISTER (PTP_RX_MOD)

Index (In decimal): EP 5.591 Size: 16 bits

This register is used to configure PTP message timestamp insertion.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**PTP Bad UDPv4 Checksum Force FCS Disable (PTP_BAD_UDPV4_CHKSUM_FORCE_FCS_DIS)** When this bit is cleared, IPv4 ingress packets that have an invalid UDP checksum will have a bad FCS forced if the packet is modified for time-stamp or correction field reasons. When this bit is set, the UDP checksum check is bypassed. **Note:** The host S/W must not change this field while both the TSU_EN-ABLE and PTP_ENABLE bits are set. At least one (PTP_EN-ABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
2	**PTP Insert Timestamp Seconds Enable (PTP_INSERT_TS_SEC_EN)** When PTP_INSERT_TS_EN is set, this bit enables bits 3:0 of the seconds portion of the receive ingress time to be inserted into the PTP message. This bit has no affect if PTP_INSERT_TS_EN is a low.	R/W	0b
1	**PTP Insert Timestamp 32 Bit Mode (PTP_INSERT_TS_32BIT)** When timestamps are inserted into the received PTP message, this bit enables bits 1:0 of the seconds portion of the receive ingress time to be inserted into the upper two bits of the 4 byte reserved field in the PTP mes-sage. Otherwise the upper two bits of the 4 byte reserved field will contain 00b.	R/W	0b
0	**PTP Insert Timestamp Enable (PTP_INSERT_TS_EN)** When set, receive ingress times are inserted into the PTP message.	R/W	0b

2.2.98 PTP RX RESERVED BYTES CONFIGURATION REGISTER (PTP_RX_RSVD_BYTE_CFG)

Index (In decimal): EP 5.592 Size: 16 bits

This register is used to configure the location of the reserved bytes inside the RX PTP messages.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:6	**PTP 4 Reserved Bytes Offset (PTP_4_RSVD_OFFSET[5:0])** This field specifies the offset into the PTP header where the receive ingress time is inserted. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	010000b
5:0	**PTP 1 Reserved Byte Offset (PTP_1_RSVD_OFFSET[5:0])** This field specifies the offset into the PTP header where the seconds portion of the receive ingress time is inserted. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000101b

2.2.99 PTP RX TAIL TAG REGISTER (PTP_RX_TAIL_TAG)

Index (In decimal): EP 5.593 Size: 16 bits

This register is used to configure tail tagging.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8	**PTP Tail Tag RX_ER forward** Enabling this field prevents RX_ER being masked during preamble when PTP_TAIL_TAG_EN=1. 1 = Enable 0 = Disable	R/W	1b
7:4	**PTP Tail Tag Insert (PTP_TAIL_TAG_INSERT_IFG)** When the PTP_TAIL_TAG_EN and PTP_TAIL_TAG_INSERT bits are set, this field specifies the minimum IFG in bytes to enforces between resultant frames. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
3	**PTP Tail Tag Insert (PTP_TAIL_TAG_INSERT)** When the PTP_TAIL_TAG_EN bit is set, this bit, when set, indicates that the timestamp is inserted before a new FCS. Otherwise the timestamp replaces the existing FCS without a new FCS. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

Bits	Description	Type	Default
2	**PTP Tail Tag All (PTP_TAIL_TAG_ALL)** When the PTP_TAIL_TAG_EN bit is set, this bit, when set, indicates that all frames are to be tail tagged. Otherwise only 1588 messages are tail tagged. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
1	**PTP Tail Tag All 1588 (PTP_TAIL_TAG_ALL_1588)** When the PTP_TAIL_TAG_EN bit is set, this bit, when set, indicates that all 1588 frames are to be tail tagged. Otherwise only those messages enabled via the PTP_RX_TIMESTAMP_EN register are tail tagged. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
0	**PTP Tail Tag Timestamp Enable (PTP_TAIL_TAG_EN)** When this bit is set, the FCS will be replaced by the ingress timestamp. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

2.2.100 PTP RX CORRECTION FIELD MODIFICATION ENABLE REGISTER (PTP_RX_CF_MOD_EN)

Index (In decimal): EP 5.594 Size: 16 bits

This register is used to enable RX PTP message correction field modifications.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**PTP Correction Field Message Type Enable (PTP_CF_MSG_EN[15:0])** These bits individually enable correction field modification of their respective message types. Bit 0 of this field corresponds to a message type value of 0 (Sync), bit 1 to message type value 1 (Delay_Req), etc. Typically Sync, Delay_Req, Pdelay_Req and Pdelay_Resp messages are enabled.	R/W	0000h

2.2.101 PTP RX CORRECTION FIELD CONFIGURATION REGISTER (PTP_RX_CF_CFG)

Index (In decimal): EP 5.595 Size: 16 bits

This register is used to configure RX PTP message correction field modifications.

Bits	Description	Type	Default
15:2	**RESERVED**	RO	—
1	**PTP Correction Field Maximum Value Test Disable (PTP_MAX_CF_DIS)** This bit disables the checking for the maximum correction field value of 7FFF_FFFF_FFFF_FFFFh. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
0	**PTP Correction Field Method (PTP_CF_METHOD)** This bit determines the method of correction field modification. 0 = Method A - CF_RSVD_4 - ingress time stored in 4 reserved bytes 1 = Method B - CF_SUB_ADD_64 - ingress time subtracted from correction field **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

2.2.102 PTP RX INGRESS TIME NANOSECONDS HIGH REGISTER (PTP_RX_INGRESS_NS_HI)

Index (In decimal): EP 5.596 Size: 16 bits

This read only register combined with the PTP RX Ingress Time Seconds High/Low Registers (PTP_RX_INGRESS_SEC_HI/LO) and the PTP RX Ingress Time Nanoseconds Low Register (PTP_RX_INGRESS_NS_LO) contains the RX timestamp capture. Up to eight captures are buffered. This register contains the upper 14 bits of the timestamps nanoseconds.

Note: Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field or the PTP RX Timestamp Valid (PTP_RX_TS_VALID) field is set indicating that at least one timestamp is available.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15	**PTP RX Timestamp Valid (PTP_RX_TS_VALID)** This field indicates that the timestamp is valid (there is at least one timestamp available to be read).	RO	0b
14	**RESERVED**	RO	—
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the nanoseconds portion of the receive ingress time.	RO	0000h

2.2.103 PTP RX INGRESS TIME NANOSECONDS LOW REGISTER (PTP_RX_INGRESS_NS_LO)

Index (In decimal): EP 5.597 Size: 16 bits

This register contains the lower 16 bits of the timestamps nanoseconds.

Note:	Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field or the PTP RX Timestamp Valid (PTP_RX_TS_VALID) field is set indicating that at least one timestamp is available.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the nanoseconds portion of the receive ingress time.	RO	0000h

2.2.104 PTP RX INGRESS TIME SECONDS HIGH REGISTER (PTP_RX_INGRESS_SEC_HI)

Index (In decimal): EP 5.598 Size: 16 bits

This read only register combined with the PTP RX Ingress Time Seconds Low Register (PTP_RX_INGRESS_SEC_LO) and the PTP RX Ingress Time Nanoseconds High/Low Registers (PTP_RX_INGRESS_NS_HI/LO) contains the RX timestamp captures. Up to eight captures are buffered. This register contains the upper 16 bits of the timestamps seconds.

Note:	Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field or the PTP RX Timestamp Valid (PTP_RX_TS_VALID) field is set indicating that at least one timestamp is available.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the seconds portion of the receive ingress time.	RO	0000h

2.2.105 PTP RX INGRESS TIME SECONDS LOW REGISTER (PTP_RX_INGRESS_SEC_LO)

Index (In decimal): EP 5.599 Size: 16 bits

This register contains the lower 16 bits of the timestamps seconds.

Note:	Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field or the PTP RX Timestamp Valid (PTP_RX_TS_VALID) field is set indicating that at least one timestamp is available.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC15:0])** This field contains the seconds portion of the receive ingress time.	RO	0000h

2.2.106 PTP RX MESSAGE HEADER 1 REGISTER (PTP_RX_MSG_HEADER1)

Index (In decimal): EP 5.600 Size: 16 bits

This read only register contains the sourcePortIdentity and messageType of the RX message header. Up to eight captures are buffered.

Note:	Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field or the PTP RX Timestamp Valid (PTP_RX_TS_VALID) field is set indicating that at least one timestamp is available.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:4	**Source Port Identity CRC (SRC_PRT_CRC)** This field contains the 12-bit CRC of the sourcePortIdentity field of the received PTP packet.	RO	000h
3:0	**Message Type (MSG_TYPE)** This field contains the messageType field of the received PTP packet.	RO	0h

2.2.107 PTP RX MESSAGE HEADER 2 REGISTER (PTP_RX_MSG_HEADER2)

Index (In decimal): EP 5.601 Size: 16 bits

This read only register contains the sequenceId of the RX message header. Up to eight captures are buffered.

Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field or the PTP RX Timestamp Valid (PTP_RX_TS_VALID) field is set indicating that at least one timestamp is available.

Reading this register will pop the capture FIFO.

Note:	This register may be read without causing a FIFO underflow.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Sequence ID (SEQ_ID)** This field contains the sequenceId field of the received PTP packet.	RO	0000h

2.2.108 PTP RX PDELAY_REQ INGRESS TIME SECONDS HIGH REGISTER (PTP_RX_PDREQ_SEC_HI)

Index (In decimal): EP 5.602 Size: 16 bits

This register combined with the PTP RX Pdelay_Req Ingress Time Seconds Mid/Low Registers (PTP_RX_PDREQ_SEC_MID/LO) and the PTP RX Pdelay_Req Ingress Time Nanoseconds High/Low Registers (PTP_RX_PDREQ_NS_HI/LO) contains the ingress time of the last Pdelay_Req message. This register contains the upper 16 bits of the timestamps seconds.

This register is automatically updated if the Auto Update (AUTO) bit is set.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[47:32])** This field contains the seconds portion of the receive ingress time.	R/W	0000h

2.2.109 PTP RX PDELAY_REQ INGRESS TIME SECONDS MID REGISTER (PTP_RX_PDREQ_SEC_MID)

Index (In decimal): EP 5.603 Size: 16 bits

This register contains the middle 16 bits of the timestamps seconds.

This register is automatically updated if the Auto Update (AUTO) bit is set.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the seconds portion of the receive ingress time.	R/W	0000h

2.2.110 PTP RX PDELAY_REQ INGRESS TIME SECONDS LOW REGISTER (PTP_RX_PDREQ_SEC_LOW)

Index (In decimal): EP 5.604 Size: 16 bits

This register contains the lower 16 bits of the timestamps seconds.

This register is automatically updated if the Auto Update (AUTO) bit is set.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[15:0])** This field contains the seconds portion of the receive ingress time.	R/W	0000h

2.2.111 PTP RX PDELAY_REQ INGRESS TIME NANOSECONDS HIGH REGISTER (PTP_RX_PDREQ_NS_HI)

Index (In decimal): EP 5.605 Size: 16 bits

This register combined with the PTP RX Pdelay_Req Ingress Time Seconds High/Mid/Low Registers (PTP_RX_PDREQ_SEC_HI/MID/LO) and the PTP RX Pdelay_Req Ingress Time Nanoseconds Low Register (PTP_RX_PDREQ_NS_LO) contains the ingress time of the last Pdelay_Req message. This register contains the upper 14 bits of the timestamps nanoseconds.

This register is automatically updated if the Auto Update (AUTO) bit is set.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15	**Auto Update (AUTO)** If this bit is set, the TS_NS field in this register and PTP_RX_PDREQ_NS_LO, the TS_SEC field in PTP_RX_PDREQ_SEC_HI/MID/LO and the CF field in PTP_RX_PDREQ_CF_HI/MID/LO are updated when a Pdelay_Req message is received. When cleared, S/W is responsible to maintain those fields. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
14	**Pdelay_Req Timestamp Valid (PDREQ_TS_VLD)** This field indicates if the RX Pdelay_Req Ingress Time and Correction Field registers are valid. This bit should be set by software after programming the registers. It is automatically set when a Pdelay_Req message is received with the Auto Update (AUTO) bit set. Depending on the egress offload mode used, this bit is cleared once the Pdelay_Resp or Pdelay_Resp_Follow_Up is transmitted. It can also be cleared by software.	R/W/SC	0b
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the nanoseconds portion of the receive ingress time.	R/W	00000000h

2.2.112 PTP RX PDELAY_REQ INGRESS TIME NANOSECONDS LOW REGISTER (PTP_RX_PDREQ_NS_LO)

Index (In decimal): EP 5.606 Size: 16 bits

This register contains the lower 16 bits of the timestamps nanoseconds.

This register is automatically updated if the Auto Update (AUTO) bit is set.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the nanoseconds portion of the receive ingress time.	R/W	0000h

2.2.113 PTP RX RAW INGRESS TIME SECONDS REGISTER (PTP_RX_RAW_TS_SEC)

Index (In decimal): EP 5.607 Size: 16 bits

This register contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter captured at the start of each frame.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[15:0])** This field contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter.	RO	0000h

Note: This value is live.

2.2.114 PTP RX RAW INGRESS TIME NANOSECONDS HIGH REGISTER (PTP_RX_RAW_TS_NS_HI)

Index (In decimal): EP 5.608 Size: 16 bits

This register contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter captured at the start of each frame.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:0	**LTC Nanoseconds (PTP_LTC_NS[29:16])** This field contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

Note: This value is live.

2.2.115 PTP RX RAW INGRESS TIME NANOSECONDS LOW REGISTER (PTP_RX_RAW_TS_NS_LO)

Index (In decimal): EP 5.609 Size: 16 bits

This register contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter captured at the start of each frame.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**LTC Nanoseconds (PTP_LTC_NS[15:0])** This field contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

Note: This value is live.

2.2.116 PTP RX CHECKSUM DROPPED COUNT HIGH REGISTER (PTP_RX_CHKSUM_DROPPED_CNT_HI)

Index (In decimal): EP 5.610 Size: 16 bits

This register along with the PTP RX Checksum Dropped Count Low Register (PTP_RX_CHKSUM_-DROPPED_CNT_LO) counts the number of ingress packets forced to have an FCS error due to a bad original UDP checksum. This register contains the upper 16 bits of the count.

Note: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit (for single bit fields) or bit-or (for multi-bit fields), such that a bit (or field) is only cleared if it was read as active (or non-zero). This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active or non-zero).

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Bad Checksum Dropped Count (BAD_CHKSUM_DROPPED_CNT[31:16])** This field is a count of ingress packets forced to have an FCS error due to a bad original UDP checksum. **Note 1:** The counter will stop at its maximum value of FFFF_FFFFh. **2:** For test purposes, the contents of this counter can be set to any desired value via a write.	RC/W	0000h

2.2.117 PTP RX CHECKSUM DROPPED COUNT LOW REGISTER (PTP_RX_CHKSUM_DROPPED_CNT_LO)

Index (In decimal): EP 5.611 Size: 16 bits

This register contains the lower 16 bits of the count.

Note:	RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit (for single bit fields) or bit-or (for multi-bit fields), such that a bit (or field) is only cleared if it was read as active (or non-zero). This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active or non-zero).

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Bad Checksum Dropped Count (BAD_CHKSUM_DROPPED_CNT[15:0])** This field is a count of ingress packets forced to have an FCS error due to a bad original UDP checksum. **Note 1:** The counter will stop at its maximum value of FFFF_FFFFh. **2:** For test purposes, the contents of this counter can be set to any desired value via a write.	RC/W	0000h

2.2.118 PTP RX FRAMES MODIFIED COUNT HIGH REGISTER (PTP_RX_FRMS_MOD_CNT_HI)

Index (In decimal): EP 5.612 Size: 16 bits

This register along with the PTP RX Frames Modified Count Low Register (PTP_RX_FRMS_MOD_CNT_LO) counts the number of packets that were modified on ingress. This register contains the upper 16 bits of the count.

Note:	RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit (for single bit fields) or bit-or (for multi-bit fields), such that a bit (or field) is only cleared if it was read as active (or non-zero). This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active or non-zero).

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**RX Frames Modified Count (RX_FRMS_MOD_CNT[31:16])** **Note:** The counter will roll over its maximum value of FFFF_FFFFh.	RC	0000h

2.2.119 PTP RX FRAMES MODIFIED COUNT LOW REGISTER (PTP_RX_FRMS_MOD_CNT_LO)

Index (In decimal): EP 5.613 Size: 16 bits

This register contains the lower 16 bits of the count.

Note: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit (for single bit fields) or bit-or (for multi-bit fields), such that a bit (or field) is only cleared if it was read as active (or non-zero). This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active or non-zero).

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**RX Frames Modified Count (RX_FRMS_MOD_CNT[15:0])** **Note:** The counter will roll over its maximum value of FFFF_FFFFh.	RC	0000h

2.2.120 PTP TX PARSING CONFIGURATION REGISTER (PTP_TX_PARSE_CONFIG)

Index (In decimal): EP 5.642 Size: 16 bits

This register is used to configure the PTP transmit message detection.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15	**IPv6 Fragments Enable** When enabled, IPv6 Fragments are considered eligible for matching. IPv6 Fragments are known by the presence of the Fragment Extension Header on all Fragments. This function must normally be Disabled. 1 = Enable 0 = Disabled (normal mode) **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0
14	**Peer/Non-peer MAC/IP DA Mixing** When cleared, the MAC and IP Destination Addresses for peer delay messages and non-peer delay messages must match those assigned by the PTP specification for peer delay messages and non-peer delay messages, respectively. When set, either destination address may be used for either peer delay messages or non-peer delay messages. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

Bits	Description	Type	Default
13	**User IP DA Peer/Non-peer** When the Peer/Non-peer MAC/IP DA Mixing bit is cleared, this bit specifies whether the user defined IP Destination Address is used for peer or non-peer IPv4 and IPv6 formatted messages. 0 = peer messages 1 = Non-peer messages When the Peer/Non-peer MAC/IP DA Mixing bit is set, the user defined IP Destination Address is used for both peer and non-peer IPv4 and IPv6 formatted messages. **Note 1:** This bit does not affect the IP Source Address matching, which, if enabled, matches for Peer and Non-peer messages. **2:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
12	**User MAC DA Peer/Non-peer** When the Peer/Non-peer MAC/IP DA Mixing bit is cleared, this bit specifies whether the user defined MAC Destination Address is used for peer or non-peer Layer2, IPv4 and IPv6 formatted PTP messages. 0 = Peer messages 1 = Non-peer messages When the Peer/Non-peer MAC/IP DA Mixing bit is set, the user defined MAC Destination Address is used for both peer and non-peer Layer2, IPv4 and IPv6 formatted PTP messages. **Note 1:** This bit does not affect the MAC Source Address matching, which, if enabled, matches for Peer and Non-peer messages. **2:** The host S/W must not change this bit while the TSU Enable (TSU_ENABLE) bit is set.	R/W	0b
11	**MAC Destination Address Enable (MAC_DA_EN)** This bit enables the checking of the MAC Destination Address in Layer2, IPv4 and IPv6 formatted PTP messages. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
10:8	**User MAC DA Mode** These three bits select the address match mode for the MAC Destination Address in Layer2, IPv4 and IPv6 formatted PTP messages. One or multiple bits can be set allowing any combination of match types. Bit 0: match the 48 bit address Bit 1: match any unicast address Bit 2: match any multicast address **Note 1:** These bits do not affect the MAC Source Address matching, which, if enabled, always matches against the 48 bit address. **2:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000b

Bits	Description	Type	Default
7	**IPv4 Fragments Enable** When enabled, IPv4 Fragments are considered eligible for matching. IPv4 Fragments are known by the values of the Fragments Offset and MF fields in the IPv4 header on all Fragments. This function must normally be Disabled. 1 = Enable 0 = Disabled (normal mode) **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
6	**UDP Source Port Number Enable** When set, the UDP source port number specified in the PTP TX Parsing UDP Source Port Register (PTP_TX_PARSE_UDP_SRC_PORT) is checked. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
5	**UDP Destination Port Number Enable** When set, the UDP destination port number specified in the PTP TX Parsing UDP Destination Port Register (PTP_TX_PARSE_UDP_DEST_PORT) is checked. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
4	**MAC/IP Address Consistency Checking** When cleared, the MAC and IP Destination Addresses are independently tested. When set, the MAC Destination Address must be consistent with the corresponding IP Destination Address. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
3	**Enable Other Routing Headers** This bit allows the usage of IPv6 Routing headers other than type 0 and 2 when validating the UDP checksum for PTP frame parsing. • When cleared, IPv6 Routing headers other than type 0 and 2 are not supported and the checksum is not validated and the frame is not time-stamped. • When set, IPv6 Routing headers other than type 0 and 2 are skipped, if the Segments Left field in the header is zero, otherwise, the checksum is not validated and the frame is not timestamped. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
2	**IPv6 Enable (IPV6_EN)** This bit enables the detection of the UDP/IPv6 formatted PTP messages. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b

Bits	Description	Type	Default
1	**IPv4 Enable (IPV4_EN)** This bit enables the detection of the UDP/IPv4 formatted PTP messages. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
0	**Layer 2 Enable (LAYER2_EN)** This bit enables the detection of the Layer 2 formatted PTP messages. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b

2.2.121 PTP TX PARSING VLAN CONFIGURATION REGISTER (PTP_TX_PARSE_VLAN_CONFIG)

Index (In decimal): EP 5.643 Size: 16 bits

This register is used to configure the VLAN parsing for PTP transmit messages.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6:4	**VLAN Tag Count [2:0]** When VLAN checking is enabled, this field specifies the expected number of VLAN tags. 000 = No VLAN tags allowed 001 = Exactly one VLAN tag expected 010 = Exactly two VLAN tags expected 101 = At least one VLAN tags expected 110 = At least two VLAN tags expected 111 = Any amount of VLAN tags allowed Others = Reserved **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000b
3	**RESERVED**	RO	—
2	**VLAN Checking Enable** When set, the number and contents of the VLAN tags is checked. When cleared, VLAN tags are parsed but skipped. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
1	**VLAN 2 Checking Enable** When set, the EtherType and VID value of VLAN 2 is checked. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
0	**VLAN 1 Checking Enable** When set, the EtherType and VID value of VLAN 1 is checked. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

2.2.122 PTP TX PARSING LAYER2 FORMAT ADDRESS ENABLE REGISTER (PTP_TX_PARSE_L2_ADDR_EN)

Index (In decimal): EP 5.644 Size: 16 bits

This register is used to enable MAC addresses for Layer 2 formatted PTP transmit messages.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**Layer 2 MAC Destination Address 1 Enable (L2_MAC_DA1_EN)** This bit enables the MAC Destination Address of 01:80:C2:00:00:0E for Layer 2 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
2	**Layer 2 MAC Destination Address 2 Enable (L2_MAC_DA2_EN)** This bit enables the MAC Destination Address of 01:1B:19:00:00:00 for Layer 2 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
1:0	**User Defined Layer 2 MAC Address Enable (L2_USER_MAC_EN[1:0])** These bits enable a user defined Layer 2 MAC address for Layer 2 PTP messages. The address is defined via the PTP TX User MAC Address High/Mid/Low Registers (PTP_TX_USER_MAC_HI/MID/LO). The user defined MAC address may be enabled for the destination or source address as follows: 11 = source/destination address 10 = source address 01 = destination address 00 = neither **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00b

2.2.123 PTP TX PARSING IP FORMAT ADDRESS ENABLE REGISTER (PTP_TX_PARSE_IP_ADDR_EN)

Index (In decimal): EP 5.645 Size: 16 bits

This register is used to enable MAC and IP addresses for IPv4 and IPv6 formatted PTP transmit messages.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13	**IP Destination Address Enable (IP_DA_EN)** This bit enables the checking of the IP Destination Address in PTP messages for both IPv4 and IPv6 formats. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
12	**IP Destination Address 1 Enable (IP_DA1_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:81 and the IPv4 Destination Address of 224.0.1.129 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:81 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:181 for IPv6 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
11	**IP Destination Address 2 Enable (IP_DA2_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:82 and the IPv4 Destination Address of 224.0.1.130 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:82 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:182 for IPv6 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
10	**IP Destination Address 3 Enable (IP_DA3_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:83 and the IPv4 Destination Address of 224.0.1.131 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:83 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:183 for IPv6 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
9	**IP Destination Address 4 Enable (IP_DA4_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:84 and the IPv4 Destination Address of 224.0.1.132 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:84 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:184 for IPv6 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

Bits	Description	Type	Default
8	**IP Destination Address 5 Enable (IP_DA5_EN)** This bit enables the MAC Destination Address of 01:00:5e:00:00:6B and the IPv4 Destination Address of 224.0.0.107 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:00:6B and the IPv6 Destination Address of FF02:0:0:0:0:0:0:6B for IPv6 PTP packets. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	1b
7:6	**User Defined IPv6 MAC Address Enable (IPV6_USER_MAC_EN[1:0])** These bits enable a user defined MAC address for IPv6 PTP messages. The address is defined via the PTP TX User MAC Address High/Mid/Low Registers (PTP_TX_USER_MAC_HI/MID/LO). The user defined MAC address may be enabled for the destination or source address as follows: 11 = Source/Destination address 10 = Source address 01 = Destination address 00 = Neither **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00b
5:4	**User Defined IPv6 IP Address Enable (IPV6_USER_IP_EN[1:0])** These bits enable a user defined MAC IP address for IPv6 PTP messages. The address is defined via the PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) as masked by the PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx). The user defined IP address may be enabled for the destination or source address as follows: 11 = Source/Destination address 10 = Source address 01 = Destination address 00 = Neither **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00b
3:2	**User Defined IPv4 MAC Address Enable (IPV4_USER_MAC_EN[1:0])** These bits enable a user defined MAC address for IPv4 PTP messages. The address is defined via the PTP TX User MAC Address High/Mid/Low Registers (PTP_TX_USER_MAC_HI/MID/LO). The user defined MAC address may be enabled for the destination or source address as follows: 11 = Either source or destination address 10 = Source address 01 = Destination address 00 = Neither **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00b

Bits	Description	Type	Default
1:0	**User Defined IPv4 IP Address Enable (IPV4_USER_IP_EN[1:0])** These bits enable a user defined MAC IP address for IPv4 PTP messages. The address is defined via the PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) as masked by the PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx). The user defined IP address may be enabled for the destination or source address as follows: 11 = Either source or destination address 10 = Source address 01 = Destination address 00 = Neither **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00b

2.2.124 PTP TX PARSING UDP SOURCE PORT REGISTER (PTP_TX_PARSE_UDP_SRC_PORT)

Index (In decimal): EP 5.646 Size: 16 bits

This register is used to configure the PTP transmit message detection.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**UDP Source Port Number (UDP_SOURCE_PORT[15:0])** This field specifies the UDP source port number. If UDP Source Port Number Enable is set, the UDP source port number in the frame must match the value in this field in order for the frame to be considered a PTP frame. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0000h

2.2.125 PTP TX PARSING UDP DESTINATION PORT REGISTER (PTP_TX_PARSE_UDP_DEST_PORT)

Index (In decimal): EP 5.647 Size: 16 bits

This register is used to configure the PTP transmit message detection.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**UDP Destination Port Number (UDP_DEST_PORT[15:0])** This field specifies the UDP destination port number. If UDP Destination Port Number Enable is set, the UDP destination port number in the frame must match the value in this field in order for the frame to be considered a PTP frame. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	319

2.2.126 PTP TX VERSION REGISTER (PTP_TX_VERSION)

Index (In decimal): EP 5.648 Size: 16 bits

This register is used to configure PTP transmit message timestamping and modification.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:8	**PTP Version Upper Range (PTP_VERSION_UP[7:0])** This field contains the PTP version range upper limit. This field is used along with the PTP version range lower limit field. Values are inclusive. The upper four bits correspond to the versionPTP message field, while the lower four bits correspond to the minorVersionPTP message field. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	20h
7:0	**PTP Version Lower Range (PTP_VERSION_LO[7:0])** This field contains the PTP version range lower limit. This field is used along with the PTP version range upper limit field. Values are inclusive. The upper four bits correspond to the versionPTP message field, while the lower four bits correspond to the minorVersionPTP message field. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	20h

2.2.127 PTP TX DOMAIN/DOMAIN RANGE LOWER REGISTER (PTP_TX_DOMAIN_DOMAIN_LO)

Index (In decimal): EP 5.649 Size: 16 bits

This register is used to configure PTP transmit message timestamping and modification.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15	**PTP Domain Range Enable (PTP_DOMAIN_RANGE_EN)** When this bit is cleared, the domainNumber in the PTP message is checked against the masked value in PTP Domain (PTP_DOMAIN[7:0]). When this bit is set, domainNumber range checking is used. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
14:8	**RESERVED**	RO	—
7:0	**PTP Domain (PTP_DOMAIN[7:0])** **PTP Domain Lower Range (PTP_DOMAIN_LO[7:0])** This field has two uses based on the PTP Domain Range Enable (PTP_DOMAIN_RANGE_EN). This field contains the PTP domain in use. Each bit may be masked using the PTP Domain Mask field. This field contains the PTP domain range lower limit. This field is used along with the PTP domain upper limit field. Values are inclusive. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00h

2.2.128 PTP TX DOMAIN MASK/DOMAIN RANGE UPPER REGISTER (PTP_TX_DOMAIN_MASK_DOMAIN_UP)

Index (In decimal): EP 5.650 Size: 16 bits

This register is used to configure PTP transmit message timestamping and modification.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**PTP Domain Mask (PTP_DOMAIN_MASK[7:0])** **PTP Domain Upper Range (PTP_DOMAIN_UP[7:0])** This field has two uses based on the PTP Domain Range Enable (PTP_DOMAIN_RANGE_EN) This field contains the PTP Domain Mask. 0 = Bit is ignored (considered a match) 1 = Bit is compared This field contains the PTP domain range upper limit. This field is used along with the PTP domain range lower limit field. Values are inclusive. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00h

2.2.129 PTP TX SDOID/SDOID RANGE LOWER REGISTER (PTP_TX_SDOID_SDOID_LO)

Index (In decimal): EP 5.651 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15	**PTP SdoId Range Enable (PTP_SDOID_RANGE_EN)** When this bit is cleared, the majorSdoId and minorSdoId fields in the PTP message are checked against the masked value in PTP SdoId (PTP_SDOID[11:0]). When this bit is set, majorSdoId and minorSdoId range checking is used. The majorSdoId and minorSdoId fields are concatenate and treated as a 12 bit value. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
14:12	**RESERVED**	RO	—
11:0	**PTP SdoId (PTP_SDOID[11:0])** **PTP SdoId Lower Range (PTP_SDOID_LO[11:0])** This field has two uses based on the PTP SdoId Range Enable (PTP_SDOID_RANGE_EN). This field contains the PTP SdoId in use. Each bit may be masked using the PTP SdoId Mask field. This field contains the PTP SdoId range lower limit. This field is used along with the PTP SdoId upper limit field. Values are inclusive. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00h

2.2.130 PTP TX SDOID MASK/SDOID RANGE UPPER REGISTER (PTP_TX_SDOID_MASK_SDOID_UP)

Index (In decimal): EP 5.652 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:0	**PTP SdoId Mask (PTP_SDOID_MASK[11:0])** **PTP SdoId Upper Range (PTP_SDOID_UP[11:0])** This field has two uses based on the PTP SdoId Range Enable (PTP_SDOID_RANGE_EN) This field contains the PTP SdoId Mask. 0 = Bit is ignored (considered a match) 1 = Bit is compared This field contains the PTP SdoId range upper limit. This field is used along with the PTP SdoId range lower limit field. Values are inclusive. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	00h

2.2.131 PTP TX TIMESTAMP ENABLE REGISTER (PTP_TX_TIMESTAMP_EN)

Index (In decimal): EP 5.653 Size: 16 bits

This register is used to enable PTP transmit message timestamping.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**PTP Message Type Enable (PTP_MESSAGE_EN[15:0])** These bits individually enable timestamping of their respective message types. Bit 0 of this field corresponds to a message type value of 0 (Sync), bit 1 to message type value 1 (Delay_Req), etc. Typically Sync, Delay_Req, Pdelay_Req and Pdelay_Resp messages are enabled.	R/W	0000h

2.2.132 PTP TX TIMESTAMP CONFIGURATION REGISTER (PTP_TX_TIMESTAMP_CONFIG)

Index (In decimal): EP 5.654 Size: 16 bits

This register is used to configure PTP transmit message timestamping and modification.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**PTP Allow UDPv6 Zero Checksum (PTP_UDPV6_ZERO_CHKSUM_EN)** When this bit is set, a zero checksum value for IPv6/UDP frames is considered valid.	R/W	0b
2	**PTP Alternate Master Enable (PTP_ALT_MASTER_EN)** When this bit is set, the alternateMasterFlag in the PTP message is checked for a zero value. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
1	**PTP UDP Checksum Check Disable (PTP_UDP_CHKSUM_DIS)** When this bit is cleared, egress times are not saved if the frame has an invalid UDP checksum. When this bit is set, the UDP checksum check is bypassed and the egress time is saved regardless. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
0	**PTP FCS Check Disable (PTP_FCS_DIS)** When this bit is cleared, egress times are not saved if the frame has an invalid FCS. When this bit is set, the FCS check is bypassed. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

2.2.133 PTP TX MODIFICATION REGISTER (PTP_TX_MOD)

Index (In decimal): EP 5.655 Size: 16 bits

This register is used to configure TX PTP message modifications.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15	**PTP Clear One Byte Reserved Field (PTP_CLR_1_RSVRD)** This bit enables the clearing of the one byte reserved field.	R/W	0b
14	**PTP Clear Four Byte Reserved Field (PTP_CLR_4_RSVRD)** This bit enables the clearing of the four byte reserved field.	R/W	0b
13	**PTP Pdelay_Resp Message Turnaround Time Insertion (PTP_PDRESP_TA_INSERT)** This bit enables the turnaround time between the received Pdelay_Req and the transmitted Pdelay_Resp to be inserted into the correctionfield of the Pdelay_Resp message sent by the Host.	R/W	0b
12	**PTP Sync Message Egress Time Insertion (PTP_SYNC_TS_INSERT)** This bit enables the egress time to be inserted into the originTimestamp field of Sync messages sent by the Host.	R/W	0b
11	**PTP Follow_Up Message Egress Time Insertion (PTP_FOLLOWUP_TS_INSERT)** This bit enables the egress time of the preceding Sync message to be inserted into the preciseOriginTimestamp field of the Follow_Up message sent by the Host.	R/W	0b
10	**PTP Pdelay_Resp Message Egress Time Insertion (PTP_PDRESP_TS_INSERT)** This bit enables the ingress time of the preceding Pdelay_Req message to be inserted into the requestReceiptTimestamp field of the Pdelay_Resp message sent by the Host.	R/W	0b
9	**PTP Pdelay_Resp_Follow_Up Message Egress Time Insertion (PTP_PDRESPFOLLOWUP_TS_INSERT)** This bit enables the egress time of the preceding Pdelay_Resp message to be inserted into the responseOriginTimestamp field of the Pdelay_Resp_-Follow_Up message sent by the Host.	R/W	0b
8	**PTP Pdelay_Resp_Follow_Up Message Turnaround Time Insertion (PTP_PDRESPFOLLOWUP_TA_INSERT)** This bit enables the turnaround time between the received Pdelay_Req and the transmitted Pdelay_Resp to be inserted into the correctionfield of the Pdelay_Resp_Follow_Up message sent by the Host.	R/W	0b
7:4	**RESERVED**	RO	—
3	**PTP Bad UDPv4 Checksum Force FCS Disable (PTP_BAD_UDPV4_CHKSUM_FORCE_FCS_DIS)** When this bit is cleared, IPv4 egress packets that have an invalid UDP checksum will have a bad FCS forced if the packet is modified for time-stamp or correction field reasons. When this bit is set, the UDP checksum check is bypassed. **Note:** The host S/W must not change this field while both the TSU_EN-ABLE and PTP_ENABLE bits are set. At least one (PTP_EN-ABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
2:0	**RESERVED**	RO	—

2.2.134 PTP TX RESERVED BYTES CONFIGURATION REGISTER (PTP_TX_RSVD_BYTE_CFG)

Index (In decimal): EP 5.656 Size: 16 bits

This register is used to configure the location of the reserved bytes inside the TX PTP messages.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:6	**PTP 4 Reserved Bytes Offset (PTP_4_RSVD_OFFSET[5:0])** This field specifies the offset into the PTP header of the four reserved bytes which the transmitter would clear if enabled. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	010000b
5:0	**PTP 1 Reserved Byte Offset (PTP_1_RSVD_OFFSET[5:0])** This field specifies the offset into the PTP header where the transmitter can retrieve the seconds portion of the ingress time. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	000101b

2.2.135 PTP TX TAIL TAG REGISTER (PTP_TX_TAIL_TAG)

Index (In decimal): EP 5.657 Size: 16 bits

This register is used to configure tail tagging.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8	**PTP Tail Tag TX_ER forward** Enabling this field prevents TX_ER being masked during preamble when PTP_TAIL_TAG_EN=1. 1 = Enable 0 = Disable	R/W	0b
7:4	**PTP Tail Tag Insert (PTP_TAIL_TAG_INSERT_IFG[3:0])** When the PTP_TAIL_TAG_EN and PTP_TAIL_TAG_INSERT bits are set, this field specifies the minimum IFG in bytes to enforces between resultant frames. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	001b
3	**PTP Tail Tag Insert (PTP_TAIL_TAG_INSERT)** When the PTP_TAIL_TAG_EN bit is set, this bit, when set, indicates that the timestamp is inserted before a new FCS. Otherwise the timestamp replaces the existing FCS without a new FCS. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
2	**PTP Tail Tag All (PTP_TAIL_TAG_ALL)** When the PTP_TAIL_TAG_EN bit is set, this bit, when set, indicates that all frames are to be tail tagged. Otherwise only 1588 messages are tail tagged. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
1	**PTP Tail Tag All 1588 (PTP_TAIL_TAG_ALL_1588)** When the PTP_TAIL_TAG_EN bit is set, this bit, when set, indicates that all 1588 frames are to be tail tagged. Otherwise only those messages enabled via the PTP_TX_TIMESTAMP_EN register are tail tagged. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
0	**PTP Tail Tag Timestamp Enable (PTP_TAIL_TAG_EN)** When this bit is set, the FCS will be replaced by the egress timestamp. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

2.2.136 PTP TX CORRECTION FIELD MODIFICATION ENABLE REGISTER (PTP_TX_CF_MOD_EN)

Index (In decimal): EP 5.658 Size: 16 bits

This register is used to configure TX PTP message correction field modifications.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**PTP Correction Field Message Type Enable (PTP_CF_MSG_EN[15:0])** These bits individually enable correction field modification of their respective message types. Bit 0 of this field corresponds to a message type value of 0 (Sync), bit 1 to message type value 1 (Delay_Req), etc. Typically, Sync, Delay_Req, Pdelay_Req and Pdelay_Resp messages are enabled.	R/W	0000h

2.2.137 PTP TX CORRECTION FIELD CONFIGURATION REGISTER (PTP_TX_CF_CFG)

Index (In decimal): EP 5.659 Size: 16 bits

This register is used to configure TX PTP message correction field modifications.

Bits	Description	Type	Default
15:3	**RESERVED**	RO	—
2	**PTP CF 32 Bit Mode (PTP_CF_32BIT)** When residence time correction field adjustments are made using Method A, this bit enables 32 bit mode, where bits 1:0 of the seconds portion of the receive ingress are taken from the upper two bits of the 4 byte reserved field in the PTP message. Otherwise only 30 bits of nanoseconds are used.	R/W	0b
1	**PTP Correction Field Maximum Value Test Disable (PTP_MAX_CF_DIS)** This bit disables the checking for the maximum correction field value of 7FFF_FFFF_FFFF_FFFFh. **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b
0	**PTP Correction Field Method (PTP_CF_METHOD)** This bit determines the method of correction field modification. 0 = Method A - CF_RSVD_4 - ingress time retrieved from 4 reserved bytes 1 = Method B - CF_SUB_ADD_64 - ingress time presubtracted from correction field **Note:** The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.	R/W	0b

2.2.138 PTP TX EGRESS TIME NANOSECONDS HIGH REGISTER (PTP_TX_EGRESS_NS_HI)

Index (In decimal): EP 5.660 Size: 16 bits

This read only register combined with the PTP TX Egress Time Seconds High/Low Registers (PTP_TX-_EGRESS_SEC_HI/LO) and the PTP TX Egress Time Nanoseconds Low Register (PTP_TX_EGRESS_NS_LO) contains the TX timestamp capture. Up to eight captures are buffered. This register contains the upper 14 bits of the timestamps nanoseconds.

Note 1: Values are only valid if the PTP TX Timestamp Interrupt (PTP_TX_TS_INT) field or the PTP TX Timestamp Valid (PTP_TX_TS_VALID) field is set indicating that at least one timestamp is available.

2: This register is not available when the 1588 Serial Timestamp Interface is enabled.

In PCH or MCH two-step operation, this register is used in combination with the PTP_TX_MSG_HEADER2, PTP_TX-_EGRESS_NS_LO, PTP_TX_EGRESS_SEC_HI, and PTP_TX_EGRESS_SEC_LO registers to provide the frame signature and departing timestamp of frames as controlled by the PCH or MCH header.

Bits	Description	Type	Default
15	**PTP TX Timestamp Valid (PTP_TX_TS_VALID)** This field indicates that the timestamp is valid (there is at least one timestamp available to be read).	RO	0b
14	**RESERVED**	RO	—
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the nanoseconds portion of the transmit egress time.	RO	0000h

2.2.139 PTP TX EGRESS TIME NANOSECONDS LOW REGISTER (PTP_TX_EGRESS_NS_LO)

Index (In decimal): EP 5.661 Size: 16 bits

This register contains the lower 16 bits of the timestamps nanoseconds.

Note 1: Values are only valid if the PTP TX Timestamp Interrupt (PTP_TX_TS_INT) field or the PTP TX Timestamp Valid (PTP_TX_TS_VALID) field is set indicating that at least one timestamp is available.

2: This register is not available when the 1588 Serial Timestamp Interface is enabled.

In PCH or MCH two-step operation, this register is used in combination with the PTP_TX_MSG_HEADER2, PTP_TX-_EGRESS_NS_HI, PTP_TX_EGRESS_SEC_HI, and PTP_TX_EGRESS_SEC_LO registers to provide the frame signature and departing timestamp of frames as controlled by the PCH or MCH header.

Bits	Description	Type	Default
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the nanoseconds portion of the transmit egress time.	RO	0000h

2.2.140 PTP TX EGRESS TIME SECONDS HIGH REGISTER (PTP_TX_EGRESS_SEC_HI)

Index (In decimal): EP 5.662 Size: 16 bits

This read only register combined with the PTP TX Egress Time Seconds Low Register (PTP_TX_EGRESS_SEC_LO) and the PTP TX Egress Time Nanoseconds High/Low Registers (PTP_TX_EGRESS_NS_HI/LO) contains the TX timestamp captures. Up to eight captures are buffered. This register contains the upper 16 bits of the timestamps seconds.

Note 1: Values are only valid if the PTP TX Timestamp Interrupt (PTP_TX_TS_INT) field or the PTP TX Timestamp Valid (PTP_TX_TS_VALID) field is set indicating that at least one timestamp is available.

2: This register is not available when the 1588 Serial Timestamp Interface is enabled.

In PCH or MCH two-step operation, this register is used in combination with the PTP_TX_MSG_HEADER2, PTP_TX-_EGRESS_NS_LO, PTP_TX_EGRESS_NS_HI, and PTP_TX_EGRESS_SEC_LO registers to provide the frame signature and departing timestamp of frames as controlled by the PCH or MCH header.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the seconds portion of the transmit egress time.	RO	0000h

2.2.141 PTP TX EGRESS TIME SECONDS LOW REGISTER (PTP_TX_EGRESS_SEC_LO)

Index (In decimal): EP 5.663 Size: 16 bits

This register contains the lower 16 bits of the timestamps seconds.

Note: Values are only valid if the PTP TX Timestamp Interrupt (PTP_TX_TS_INT) field or the PTP TX Timestamp Valid (PTP_TX_TS_VALID) field is set indicating that at least one timestamp is available.

In PCH or MCH two-step operation, this register is used in combination with the PTP_TX_MSG_HEADER2, PTP_TX-_EGRESS_NS_LO, PTP_TX_EGRESS_NS_HI, and PTP_TX_EGRESS_SEC_HI registers to provide the frame signature and departing timestamp of frames as controlled by the PCH or MCH header.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[15:0])** This field contains the seconds portion of the transmit egress time.	RO	0000h

2.2.142 PTP TX MESSAGE HEADER 1 REGISTER (PTP_TX_MSG_HEADER1)

Index (In decimal): EP 5.664 Size: 16 bits

This read only register contains the sourcePortIdentity and messageType of the TX message header. Up to eight captures are buffered.

Note 1: Values are only valid if the PTP TX Timestamp Interrupt (PTP_TX_TS_INT) field or the PTP TX Timestamp Valid (PTP_TX_TS_VALID) field is set indicating that at least one timestamp is available.

2: This register is not available when the 1588 Serial Timestamp Interface is enabled.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:4	**Source Port Identity CRC (SRC_PRT_CRC[11:0])** This field contains the 12-bit CRC of the sourcePortIdentity field of the transmitted PTP packet.	RO	000h
3:0	**Message Type (MSG_TYPE[3:0])** This field contains the messageType field of the transmitted PTP packet.	RO	0h

2.2.143 PTP TX MESSAGE HEADER 2 REGISTER (PTP_TX_MSG_HEADER2)

Index (In decimal): EP 5.665 Size: 16 bits

This read only register contains the sequenceId of the TX message header. Up to eight captures are buffered.

Note: Values are only valid if the PTP TX Timestamp Interrupt (PTP_TX_TS_INT) field or the PTP TX Timestamp Valid (PTP_TX_TS_VALID) field is set indicating that at least one timestamp is available.

In PCH or MCH two-step operation, this register is used in combination with the PTP_TX_EGRESS_SEC_HI/LO and PTP_TX_EGRESS_NS_HI/LO registers to provide the frame signature and departing timestamp of frames as controlled by the PCH or MCH header. This register contains the PCH or MCH frame signature.

Note 1: This register is not available when the 1588 Serial Timestamp Interface is enabled.

2: Reading this register will pop the capture FIFO.

3: This register may be read without causing a FIFO underflow.

Bits	Description	Type	Default
15:0	**Sequence ID (SEQ_ID[15:0])** In Standalone Mode this field contains the sequenceId field of the transmitted PTP packet. In PCH Mode, this field contains the signature field from the PCH or MCH header of the transmitted PTP packet.	RO	0000h

2.2.144 PTP TX SYNC EGRESS TIME SECONDS HIGH REGISTER (PTP_TX_SYNC_SEC_HI)

Index (In decimal): EP 5.666 Size: 16 bits

This register combined with the PTP TX Sync Egress Time Seconds Mid/Low Registers (PTP_TX_SYNC_SEC_MID/LO) and the PTP TX Sync Egress Time Nanoseconds High/Low Registers (PTP_TX_SYNC_NS_HI/LO) contains the egress time of the last Sync message. This register contains the upper 16 bits of the timestamps seconds.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[47:32])** This field contains the seconds portion of the transmit egress time.	RO	0000h

2.2.145 PTP TX SYNC EGRESS TIME SECONDS MID REGISTER (PTP_TX_SYNC_SEC_MID)

Index (In decimal): EP 5.667 Size: 16 bits

This register contains the middle 16 bits of the timestamps seconds.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the seconds portion of the transmit egress time.	RO	0000h

2.2.146 PTP TX SYNC EGRESS TIME SECONDS LOW REGISTER (PTP_TX_SYNC_SEC_LOW)

Index (In decimal): EP 5.668 Size: 16 bits

This register contains the lower 16 bits of the timestamps seconds.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[15:0])** This field contains the seconds portion of the transmit egress time.	RO	0000h

2.2.147 PTP TX SYNC EGRESS TIME NANOSECONDS HIGH REGISTER (PTP_TX_SYNC_NS_HI)

Index (In decimal): EP 5.669 Size: 16 bits

This register combined with the PTP TX Sync Egress Time Seconds High/Mid/Low Registers (PTP_TX_SYNC_SEC_HI/MID/LO) and the PTP TX Sync Egress Time Nanoseconds Low Register (PTP_TX_SYNC_NS_LO) contains the egress time of the last Sync message. This register contains the upper 14 bits of the timestamps nanoseconds.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**Sync Timestamp Valid (SYNC_TS_VLD)** This field indicates if the TX Sync Egress Time registers are valid. It is automatically set when a Sync message is transmitted. If Follow_Up Message Egress Time Insertion (Two Step Offload) is used, this bit is cleared once the Follow_Up is transmitted.	RO	0b
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the nanoseconds portion of the transmit egress time.	RO	00000000h

2.2.148 PTP TX SYNC EGRESS TIME NANOSECONDS LOW REGISTER (PTP_TX_SYNC_NS_LO)

Index (In decimal): EP 5.670 Size: 16 bits

This register contains the lower 16 bits of the timestamps nanoseconds.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the nanoseconds portion of the transmit egress time.	RO	0000h

2.2.149 PTP TX PDELAY_RESP EGRESS TIME SECONDS HIGH REGISTER (PTP_TX_PDRESP_SEC_HI)

Index (In decimal): EP 5.671 Size: 16 bits

This register combined with the PTP TX Pdelay_Resp Egress Time Seconds Mid/Low Registers (PTP_TX_PDRESP_SEC_MID/LO) and the PTP TX Pdelay_Resp Egress Time Nanoseconds High/Low Registers (PTP_TX_PDRESP_NS_HI/LO) contains the egress time of the last Pdelay_Resp message. This register contains the upper 16 bits of the timestamps seconds.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[47:32])** This field contains the seconds portion of the transmit egress time.	RO	0000h

2.2.150 PTP TX PDELAY_RESP EGRESS TIME SECONDS MID REGISTER (PTP_TX_PDRESP_SEC_MID)

Index (In decimal): EP 5.672 Size: 16 bits

This register contains the middle 16 bits of the timestamps seconds.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the seconds portion of the transmit egress time.	RO	0000h

2.2.151 PTP TX PDELAY_RESP EGRESS TIME SECONDS LOW REGISTER (PTP_TX_PDRESP_SEC_LOW)

Index (In decimal): EP 5.673 Size: 16 bits

This register contains the lower 16 bits of the timestamps seconds.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[15:0])** This field contains the seconds portion of the transmit egress time.	RO	0000h

2.2.152 PTP TX PDELAY_RESP EGRESS TIME NANOSECONDS HIGH REGISTER (PTP_TX_PDRESP_NS_HI)

Index (In decimal): EP 5.674 Size: 16 bits

This register combined with the PTP TX Pdelay_Resp Egress Time Seconds High/Mid/Low Registers (PTP_TX_PDRESP_SEC_HI/MID/LO) and the PTP TX Pdelay_Resp Egress Time Nanoseconds Low Register (PTP_TX_PDRESP_NS_LO) contains the egress time of the last Pdelay_Resp message. This register contains the upper 14 bits of the timestamps nanoseconds.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**Pdelay_Resp Timestamp Valid (PDRESP_TS_VLD)** This field indicates if the TX Pdelay_Resp Egress Time registers are valid. It is automatically set when a Pdelay_Resp message is transmitted. If Pdelay_Resp_Follow_Up Message Egress Time Insertion (Two Step Offload) or Pdelay_Resp_Follow_Up Message Egress Correction Field Turnaround Time Adjustment (Two Step Offload) is used, this bit is cleared once the Pdelay_Resp_Follow_Up is transmitted.	RO	0b
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the nanoseconds portion of the transmit egress time.	RO	00000000h

2.2.153 PTP TX PDELAY_RESP EGRESS TIME NANOSECONDS LOW REGISTER (PTP_TX_PDRESP_NS_LO)

Index (In decimal): EP 5.675 Size: 16 bits

This register contains the lower 16 bits of the timestamps nanoseconds.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the nanoseconds portion of the transmit egress time.	RO	0000h

2.2.154 PTP TX RAW EGRESS TIME SECONDS REGISTER (PTP_TX_RAW_TS_SEC)

Index (In decimal): EP 5.676 Size: 16 bits

This register contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter captured at the start of each frame.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Note: This value is live.

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[15:0])** This field contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter.	RO	0000h

2.2.155 PTP TX RAW EGRESS TIME NANOSECONDS HIGH REGISTER (PTP_TX_RAW_TS_NS_HI)

Index (In decimal): EP 5.677 Size: 16 bits

This register contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter captured at the start of each frame.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Note: This value is live.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:0	**LTC Nanoseconds (PTP_LTC_NS[29:16])** This field contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

2.2.156 PTP TX RAW EGRESS TIME NANOSECONDS LOW REGISTER (PTP_TX_RAW_TS_NS_LO)

Index (In decimal): EP 5.678 Size: 16 bits

This register contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter captured at the start of each frame.

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Note:	This value is live.

Bits	Description	Type	Default
15:0	**LTC Nanoseconds (PTP_LTC_NS[15:0])** This field contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

2.2.157 PTP TX CHECKSUM DROPPED COUNT HIGH REGISTER (PTP_TX_CHKSUM_DROPPED_CNT_HI)

Index (In decimal): EP 5.679 Size: 16 bits

This register along with the PTP TX Checksum Dropped Count Low Register (PTP_TX_CHKSUM_-DROPPED_CNT_LO) counts the number of egress packets forced to have an FCS error due to a bad original UDP checksum. Since the packet was dropped by forcing an TX error, the packet will also be counted as an error by the receiving MAC. This register contains the upper 16 bits of the count.

Note:	RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit (for single bit fields) or bit-or (for multi-bit fields), such that a bit (or field) is only cleared if it was read as active (or non-zero). This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active or non-zero).

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	**Bad Checksum Dropped Count (BAD_CHKSUM_DROPPED_CNT[31:16])** This field is a count of egress packets forced to have an FCS error due to a bad original UDP checksum. **Note 1:** The counter will stop at its maximum value of FFFF_FFFFh. **2:** For test purposes, the contents of this counter can be set to any desired value via a write.	RC/W	0000h

2.2.158 PTP TX CHECKSUM DROPPED COUNT LOW REGISTER (PTP_TX_CHKSUM_DROPPED_CNT_LO)

Index (In decimal): EP 5.680 Size: 16 bits

This register contains the lower 16 bits of the count.

Note:	RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit (for single bit fields) or bit-or (for multi-bit fields), such that a bit (or field) is only cleared if it was read as active (or non-zero). This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active or non-zero).

This register is not applicable to PTP PCH Mode, both with and without MCH support.

Bits	Description	Type	Default
15:0	Bad Checksum Dropped Count (BAD_CHKSUM_DROPPED_CNT[15:0]) This field is a count of egress packets forced to have an FCS error due to a bad original UDP checksum. **Note 1:** The counter will stop at its maximum value of FFFF_FFFFh. **2:** For test purposes, the contents of this counter can be set to any desired value via a write.	RC/W	0000h

2.2.159 PTP TX FRAMES MODIFIED COUNT HIGH REGISTER (PTP_TX_FRMS_MOD_CNT_HI)

Index (In decimal): EP 5.681 Size: 16 bits

This register along with the PTP TX Frames Modified Count Low Register (PTP_TX_FRMS_MOD_CNT_LO) counts the number of packets that were modified on egress. This register contains the upper 16 bits of the count.

Note:	RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit (for single bit fields) or bit-or (for multi-bit fields), such that a bit (or field) is only cleared if it was read as active (or non-zero). This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active or non-zero).

Bits	Description	Type	Default
15:0	**TX Frames Modified Count (TX_FRMS_MOD_CNT[31:16])** **Note:** The counter will roll over its maximum value of FFFF_FFFFh.	RC	0000h

2.2.160 PTP TX FRAMES MODIFIED COUNT LOW REGISTER (PTP_TX_FRMS_MOD_CNT_LO)

Index (In decimal): EP 5.682 Size: 16 bits

This register contains the lower 16 bits of the count.

Note: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit (for single bit fields) or bit-or (for multi-bit fields), such that a bit (or field) is only cleared if it was read as active (or non-zero). This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active or non-zero).

Bits	Description	Type	Default
15:0	**TX Frames Modified Count (TX_FRMS_MOD_CNT[15:0])** **Note:** The counter will roll over its maximum value of FFFF_FFFFh.	RC	0000h

2.2.161 TSU GENERAL CONFIGURATION REGISTER (TSU_GENERAL_CONFIG)

Index (In decimal): EP 5.704 Size: 16 bits

This register provides general configuration for the 1588 TSU.

Bits	Description	Type	Default
15:3	**RESERVED**	RO	—
2	**Dis_ts_save_for_crc_fail_pkt** 1= Save TS from frames with CRC error 0 = Do not save TS from frames with CRC error This bit controls whether timestamps are saved for egress MCH/PCH two-step frames when the FCS is in error or GMII_TX_ER asserts during the non-preamble part of the frame.	R/W	0b
1	**Preemption Enable (PREEMPTION_ENABLE)** 1 = Frame Preemption enabled on this port 0 = Frame Preemption disabled on this port The host S/W must not change this bit while the TSU Enable (TSU_ENABLE) bit is set.	R/W	0b
0	**Time-Stamp Unit Enable (TSU_ENABLE)** This bit enables the receive and transmit functions of the time-stamp unit. The PTP Enable (PTP_ENABLE) bit must also be set. The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit is set. (moved from Pfeiffer MMD 2.257)	R/W	1b

2.2.162 TSU HARD RESET REGISTER

Index (In decimal): EP 5.705 Size: 16 bits

This register resets the PTP TSU and sets all related configuration registers to their default state.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**PTP TSU Hard Reset** 1 = Reset the PTP TSU and set all configuration registers to their default state. Writing a zero has no effect.	W1S/SC	0b

2.2.163 TSU SOFT RESET REGISTER

Index (In decimal): EP 5.706 Size: 16 bits

This register resets the PTP TSU but does not reset any configuration registers.

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**PTP TSU Soft Reset** 1 = Reset the PTP TSU except all configuration registers. Writing a zero has no effect.	W1S/SC	0b

2.2.164 PTP PCH FORMAT MISMATCH REGISTER

Index (In decimal): EP 5.707 Size: 16 bits

This register indicates if a frame was ever received over USGMII with an unexpected PCH or MCH format.

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**Packet Type Mismatch** 1 = Frame received over USGMII with unexpected Packet Type 0 = No mismatch detected	RC	—
2	**Extension Type Mismatch** 1 = Frame received over USGMII with unexpected Extension Type 0 = No mismatch detected	RC	—
1	**CRC Error Detected** 1 = Frame received over USGMII with PCH or MCH CRC Error 0 = No mismatch detected	RC	—
0	**SubPortID Mismatch** 1 = Frame received over USGMII with SubPortID not matching the value configured in the PTP PCH SubPortID Register. 0 = No mismatch detected	RC	—

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004284B (06-17-22)	Miscellaneous (refer to each entry)	• Updated Chip Hard Reset Register bit 0 description • Updated Chip Soft Reset Register bit 0 description • Updated QSGMII Hard Reset Register bit 0 description • Updated QSGMII SerDes Transmit General Control Register field 4:0 description • Removed QSGMII SerDes Receive General Control Register (EP 4.132) definition • Updated QSGMII SerDes Receive Equalization Control Register field 2:0 default value • Removed QSGMII SerDes MPLL Control and Status Register (EP 4.136) definition • Updated 1588 PLL Status Register note grammar • Updated AB PVT Hard Reset Register bit 0 description • Updated AB PVT Soft Reset Register bit 0 description • Updated PTP Command and Control Register (PTP_CMD_CTL) bit 2 description • Updated PTP Reference Clock Configuration Register (PTP_REF_CLK_CFG) bits 12:10, 9, and 8 notes • Updated PTP LTC Hard Reset Register bit 0 description • Updated PTP LTC Soft Reset Register bit 0 description • Updated PTP Operating Mode Register note • Updated 1588 STI Hard Reset Register bit 0 description • Updated 1588 STI Soft Reset Register bit 0 description • Updated QSGMII PCS1G Hard Reset Register bit 0 description • Updated QSGMII PCS1G Test Pattern Configuration and Status Register bit 1 description • Updated Port Hard Reset Register bit 0 description • In Section 2.2.53 through Section 2.2.137, replaced note “The host S/W must not change this field while the TSU Enable (TSU_ENABLE) bit is set.” with note “The host S/W must not change this field while both the TSU_ENABLE and PTP_ENABLE bits are set. At least one (PTP_ENABLE, TSU_ENABLE) must be cleared to update this field.”

TABLE A-1: REVISION HISTORY (CONTINUED)

Revision Level & Date	Section/Figure/Entry	Correction
DS00004284B (06-03-22) *(Continued)*	Miscellaneous (refer to each entry)	• Updated PTP Capture Information Register (PTP_CAP_INFO) description • Updated PTP TX Modification Register (PTP_TX_MOD) bit 3 definition to indicate IPv4 instead of IPv6 • Updated PTP TX Tail Tag Register (PTP_TX-_TAIL_TAG) bit 1 definition to indicate PTP_TX_TIMESTAMP instead of PTP_RX_-TIMESTAMP • Updated PTP TX Egress Time Seconds Low Register (PTP_TX_EGRESS_SEC_LO) note • Updated TSU Hard Reset Register bit 0 description • Updated TSU Soft Reset Register bit 0 description • Output Control Register description updated - reference to LED pins removed and note following table deleted.
DS00004284A (11-09-21)	Initial release	

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