AN4286

LAN8804/LAN8814 GPHY Register Definitions

1.0 INTRODUCTION

The LAN8804/LAN8814 GPHY Register Definitions application note provides a description of all Gigabit PHY registers within the LAN8804/LAN8814 and is meant for clarification of functionality during design and debugging. This document should be used in conjunction with the LAN8804/LAN8814 General Register Definitions application note.

1.1 Sections

This document includes the following topics:

1.2 References

Consult the following documents for additional device details:

- LAN8804 Datasheet, www.microchip.com
- LAN8814 Datasheet, www.microchip.com
- LAN8804/LAN8814 General Register Definitions, www.microchip.com

2.0 REGISTER MAP

TABLE 2-1: MAP OF DIRECT REGISTERS

MDIO Index (in decimal)	MDIO Index (in hex)	APB Address (in hex)	Register Name
IEEE-Defined GPHY Registers			
0	0	x100h	Basic Control Register
1	1	x102h	Basic Status Register
2	2	x104h	Device Identifier 1 Register
3	3	X106h	Device Identifier 2 Register
4	4	x108h	Auto-Negotiation Advertisement Register
5	5	x10Ah	Auto-Negotiation Link Partner Base Page Ability Register
6	6	x10Ch	Auto-Negotiation Expansion Register
7	7	x10Eh	Auto-Negotiation Next Page TX Register
8	8	x110h	Auto-Negotiation Next Page RX Register
9	9	x112h	Auto-Negotiation Master Slave Control Register
10	Ah	x114h	Auto-Negotiation Master Slave Status Register
11	Bh	x116h	RESERVED
12	Ch	x118h	RESERVED
13	Dh	x11Ah	MMD Access Control Register
14	Eh	x11Ch	MMD Access Address/Data Register
15	Fh	x11Eh	Extended Status Register
Vendor-Specific GPHY Registers			
16	10h	x120h	RESERVED
17	11h	x122h	PCS Loop-back Swap/Polarity Control Register
18	12h	x124h	Cable Diagnostic Register
19	13h	X126h	Digital PMA/PCS Status Register
20	14h	x128h	RESERVED
21	15h	x12Ah	RXER Counter Register
22	16h	x12Ch	EP Access Control Register
23	17h	x12Eh	EP Access Address/Data Register
24	18h	x130h	GPHY Interrupt Enable Register
25	19h	x132h	GPHY Revision Register
26	1Ah	x134h	RESERVED
27	1Bh	x136h	GPHY Interrupt Status Register
28	1Ch	x138h	Digital Debug Control 1 Register
29	1Dh	x13Ah	RESERVED
30	1Eh	x13Ch	Reserved Register
31	1Fh	x13Eh	Control Register

APB Address x = Port ID (0, 1, 2, or 3)

TABLE 2-2: MAP OF INDIRECT MMD REGISTERS

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
MMD 3	**IEEE-Defined EEE/PCS Registers**		
	See Table 2-4		
MMD 7	**IEEE-Defined EEE Auto-Negotiation Registers**		
	See Table 2-5		

TABLE 2-3: MAP OF INDIRECT EXTENDED PAGE REGISTERS

EP Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
EP 0	**PCS Registers**		
	See Table 2-6		
EP 1	**PMA Registers**		
	See Table 2-7		
EP 2	**Miscellaneous Control Registers**		
	See Table 2-8		
EP 3	**EEE and PCS Registers**		
	See Table 2-9		
EP 7	**Vendor-Specific EEE Auto-Negotiation Registers**		
	See Table 2-10		
EP 28	**Analog Control Registers**		
	See Table 2-11		
EP 29	**Device Common Analog Control Registers**		
	See Table 2-12		

TABLE 2-4: IEEE-DEFINED EEE / PCS REGISTERS (MMD 3)

Index (in decimal)	Index (in hex)	Register Name
0	0	RESERVED
1	1	PCS Status 1 Register
2-19	2-13h	RESERVED
20	14h	EEE Control and Capability Register
21	15h	RESERVED
22	16h	RESERVED
23-27	17h-1Bh	RESERVED

TABLE 2-5: IEEE-DEFINED EEE AUTO-NEGOTIATION REGISTERS (MMD 7)

Index (in decimal)	Index (in hex)	Register Name
0-59	0-3Bh	RESERVED
60	3Ch	EEE Advertisement Register
61	3Dh	EEE Link Partner Ability Register
62-63	3Eh-3Fh	RESERVED

TABLE 2-6: PCS REGISTERS (EP 0)

Index (in decimal)	Index (in hex)	Register Name
0	0	RESERVED
1	1	RESERVED
2	2	RESERVED
3	3	RESERVED
4	4	RESERVED
5	5	RESERVED
6	6	RESERVED
7	7	RESERVED
8	8	RESERVED
9	9	RESERVED
10	Ah	RESERVED
11	Bh	RESERVED
12	Ch	RESERVED
13	Dh	RESERVED
14	Eh	RESERVED
15	Fh	Fast Link Fail (FLF) Configuration and Status Register
16	10h	Link Partner Force FD Override Register
17	11h	RESERVED
18	12h	RESERVED

TABLE 2-7: PMA REGISTERS (EP 1)

Index (in decimal)	Index (in hex)	Register Name
0 - 118	0h - 76h	RESERVED
119	77h	DFE Init2 100 Register
120	78h	RESERVED
121	79h	PGA Table 1G, Entry 0 (Max Gain) Register
122	7Ah	PGA Table 1G, Entry 1 Register
123	7Bh	PGA Table 1G, Entry 2 Register
124	7Ch	PGA Table 1G, Entry 3 Register
125	7Dh	PGA Table 1G, Entry 4 Register
126	7Eh	PGA Table 1G, Entry 5 Register
127	7Fh	PGA Table 1G, Entry 6 Register
128	80h	PGA Table 1G, Entry 7 Register

TABLE 2-7: PMA REGISTERS (EP 1) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
129	81h	PGA Table 1G, Entry 8 Register
130	82h	PGA Table 1G, Entry 9 Register
131	83h	PGA Table 1G, Entry 10 Register
132	84h	PGA Table 1G, Entry 11 Register
133	85h	PGA Table 1G, Entry 12 Register
134	86h	PGA Table 1G, Entry 13 Register
135	87h	PGA Table 1G, Entry 14 Register
136	88h	PGA Table 1G, Entry 15 Register
137	89h	PGA Table 1G, Entry 16 Register
138	8Ah	PGA Table 1G, Entry 17 Register
139 - 156	8Bh - 9Ch	RESERVED
157	9Dh	PD Controls Register
158 - 238	9Eh - EEh	RESERVED

TABLE 2-8: MISCELLANEOUS CONTROL REGISTERS (EP 2)

Index (in decimal)	Index (in hex)	Register Name
0	0	Common Control Register
1	1	RESERVED
2	2	Operation Mode Strap Override Low Register
3	3	Operation Mode Strap Low Register
4-8	4-8	RESERVED
9	9	Self-Test Packet Count LO Register
10	Ah	Self-Test Packet Count HI Register
11	Bh	Self-Test Status Register
12	Ch	Self-Test Frame Count Enable Register
13	Dh	Self-Test PGEN Enable Register
14	Eh	Self-Test Enable Register
15	Fh	1000BT Fix Latency Enable Register
16-59	10h-3Bh	RESERVED
60	3Ch	Self-Test Correct Count LO Register
61	3Dh	Self-Test Correct Count HI Register
62	3Eh	Self-Test Error Count LO Register
63	3Fh	Self-Test Error Count HI Register
64	40h	SCR Wait Counter Register
65	41h	SCR Wait Counter Control Register
66-73	42h-49h	RESERVED
74	4Ah	EP2 Register 74
75	4Bh	EP2 Register 75
76	4Ch	RESERVED
77	4Dh	RESERVED
78	4Eh	Lane Alignment Predictor Register
79-80	4Fh-50h	RESERVED
81	51h	Operation Mode Strap Override High Register

TABLE 2-8: MISCELLANEOUS CONTROL REGISTERS (EP 2) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
82	52h	Operation Mode Strap High Register
83	53h	LPI Miscellaneous Register
84	54h	Rx Correct Counter Low Register
85	55h	Rx Correct Counter High Register
86	56h	Rx CRC Counter Low Register
87	57h	Rx CRC Counter High Register
88	58h	Rx Correct Counter HI Extended Register
89	59h	Self-Test Correct Counter HI Extended Register
90-91	5Ah-5Bh	RESERVED
92	5Ch	ST2 Correct Counter LO Register
93	5Dh	ST2 Correct Counter HI Register
94	5Eh	ST2 Correct Counter HI Extended Register
95	5Fh	ST2 Error Counter LO Register
96	60h	ST2 Error Counter HI Register
97	61h	SRC1 Frame Counter LO Register
98	62h	SRC1 Frame Counter HI Register
99	63h	SRC1 Frame Counter HI Extended Register
100	64h	SRC2 Frame Counter LO Register
101	65h	SRC2 Frame Counter HI Register
102	66h	SRC2 Frame Counter HI Extended Register
103	67h	Sleep Timer Counter Mask Register
104	68h	Frame Counter Mask Register
105	69h	Sleep Counter Minimum Register
106	6Ah	DES1/SRC1 Address Register
107	6Bh	DES2/SRC2 Address Register
108	6Ch	Write to Clear Register
109	6Dh	Multistream Control Register
110	6Eh	Multistream Start Register
111-127	6Fh-7Fh	RESERVED
128-136	80h-88h	RESERVED
137-255	89h-FFh	RESERVED
256-511	100h-1FFh	RESERVED

TABLE 2-9: EEE AND PCS REGISTERS (EP 3)

Index (in decimal)	Index (in hex)	Register Name
0	0	PCS Control 1 Register
1-7	1-7	RESERVED
8	8	EEE Quiet Timer Register
9	9	EEE Update Timer Register
10	Ah	EEE Link-Fail Timer Register
11	Bh	EEE Post-Update Timer Register

TABLE 2-9: EEE AND PCS REGISTERS (EP 3) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
12	Ch	EEE WaitWQ Timer Register
13	Dh	EEE Wake Timer Register
14	Eh	EEE WakeTX Timer Register
15	Fh	EEE WakeMz Timer Register
16-27	10h-1Bh	RESERVED

TABLE 2-10: VENDOR-SPECIFIC EEE AUTO-NEGOTIATION REGISTERS (EP 7)

Index (in decimal)	Index (in hex)	Register Name
0-58	0-3Ah	RESERVED
58	3Ah	EP7 Register 58
59	3Bh	EP7 Register 59
60	3Ch	RESERVED
61	3Dh	RESERVED
62	3Eh	EEE Link Partner Ability Override Register
63	3Fh	EEE Message Code Register

TABLE 2-11: ANALOG CONTROL REGISTERS (EP 28)

Index (in decimal)	Index (in hex)	Register Name
0-3	0h-3h	RESERVED
4	4	Analog Control Register 4
5-7	5h-7h	RESERVED
8	8	Analog Control Register 8
9	9	AFED Control Register
10-15	Ah-Fh	RESERVED
16	10h	Power Management Mode 0 Register (see Power Management Mode Registers)
17	11h	Power Management Mode 1 Register (see Power Management Mode Registers)
18	12h	Power Management Mode 2 Register (see Power Management Mode Registers)
19	13h	Power Management Mode 3 Register (see Power Management Mode Registers)
20	14h	Power Management Mode 4 Register (see Power Management Mode Registers)
21	15h	Power Management Mode 5 Register (see Power Management Mode Registers)
22	16h	Power Management Mode 6 Register (see Power Management Mode Registers)
23	17h	Power Management Mode 7 Register (see Power Management Mode Registers)
24	18h	Power Management Mode 8 Register (see Power Management Mode Registers)
25	19h	Power Management Mode 9 Register (see Power Management Mode Registers)
26	1Ah	Power Management Mode 10 Register (see Power Management Mode Registers)
27	1Bh	Power Management Mode 11 Register (see Power Management Mode Registers)
28	1Ch	Power Management Mode 12 Register (see Power Management Mode Registers)
29	1Dh	Power Management Mode 13 Register (see Power Management Mode Registers)

TABLE 2-11: ANALOG CONTROL REGISTERS (EP 28) (CONTINUED)

Index (in decimal)	Index (in hex)	Register Name
30	1Eh	Power Management Mode 14 Register (see Power Management Mode Registers)
31	1Fh	Power Management Mode 15 Register (see Power Management Mode Registers)
32	20h	Power Management Mode 16 (Master) Register (see Power Management Mode Registers)
33	21h	Power Management Mode 16 (Slave) Register (see Power Management Mode Registers)
34-35	22h	RESERVED
36	24h	EDPD Control Register
37-79	25h-4Fh	RESERVED

TABLE 2-12: DEVICE COMMON ANALOG CONTROL REGISTERS (EP 29)

Index (in decimal)	Index (in hex)	Register Name
0	0	RESERVED
1	1	Analog Control Register 1
2-13	2-Dh	RESERVED
14	Eh	Analog Control Register 11
15-55	Fh-37h	RESERVED
56	38h	EP29 Register 56
57	39h	EP29 Register 57
58	3Ah	EP29 Register 58
59	3Bh	EP29 Register 59
60	3Ch	EP29 Register 60
61	3Dh	EP29 Register 61
62	3Eh	RESERVED
63	3Fh	EP 29 Register 63
64-80	F0h-50h	RESERVED

3.0 DIRECT REGISTERS

Direct registers provide direct read/write access to a 32-register address space, as defined in Clause 22 of the IEEE 802.3 Specification.

- The first 16 registers [Registers 0 to 15 (Fh)] are defined according to 802.3.
- The remaining 16 registers [Registers 16 (10h) to 31 (1Fh)] are PHY vendor-specific.

3.1 Basic Control Register

Index (In decimal): 0 Size: 16 bits

This read/write register is used to configure the PHY.

Bits	Description	Type	Default
15	**PHY Software Hard Reset (RESET)** When set, this bit resets all the PHY and all its registers to their default state. This bit is self clearing. 1 = PHY software hard reset.	R/W1S/SC	0b
14	**Loopback (PHY_LOOPBACK)** This bit enables/disables the loopback mode. When enabled, transmissions are not sent to network. Instead, they are looped back into the PHY. 0 = Loopback mode disabled (normal operation) 1 = Loopback mode enabled	R/W	0b
13	**Speed Select[0]** Together with Speed Select[1], sets speed per the following table: [Speed Select1][Speed Select0] 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Reserved (customer cannot write 11) **Note 1:** Ignored if the Auto-Negotiation Enable bit of this register is 1. **2:** See EP 7.59 for UNH override	R/W	Note 1
12	**Auto-Negotiation Enable** This bit enables/disables Auto-Negotiation. 0 = Disable auto-negotiate process 1 = Enable auto-negotiate process (overrides the Speed Select[0], Speed Select[1] ,and Duplex Mode bits of this register)	R/W	Note 1
11	**Software Power Down** This bit controls the Software Power Down (SPD) mode of this PHY port. 0 = Normal operation 1 = Power down AFE port	R/W	Note 1
10	**Isolate (PHY_ISO)** This bit controls the isolation of the PHY from the MII interface. 0 = Non-Isolated (normal operation) 1 = Isolated	R/W	0b

Note 1: The default is set by the values in the Operation Mode Strap Override Low Register and the Operation Mode Strap Override High Register.

Bits	Description	Type	Default
9	**Restart Auto-Negotiation (PHY_RST_AN)** When set, this bit restarts the Auto-Negotiation process. This bit is self clearing. 1 = Auto-Negotiation restarted	R/W1S/SC	0b
8	**Duplex Mode** This bit is used to set the duplex. 0 = Half Duplex 1 = Full Duplex **Note:** Ignored if the Auto-Negotiation Enable bit of this register is 1.	R/W	Note 1
7	**Collision Test Mode (PHY_COL_TEST)** This bit enables/disables the collision test mode of the PHY. When set, the collision signal is active during transmission. It is recommended that this feature be used only in Loopback mode. 0 = Collision test mode disabled 1 = Collision test mode enabled	R/W	0b
6	**Speed Select[1]** See description for Speed Select[0] for details.	R/W	Note 1
5:0	RESERVED	RO	—

Note 1: The default is set by the values in the Operation Mode Strap Override Low Register and the Operation Mode Strap Override High Register.

3.2 Basic Status Register

Index (In decimal): 1 Size: 16 bits

This register is used to monitor the status of the PHY.

Note: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15	**100BASE-T4** This bit displays the status of 100BASE-T4 compatibility. 0 = PHY not able to perform 100BASE-T4 1 = PHY able to perform 100BASE-T4	RO	0b
14	**100BASE-X Full Duplex** This bit displays the status of 100BASE-X full duplex compatibility. 0 = PHY not able to perform 100BASE-X full duplex 1 = PHY able to perform 100BASE-X full duplex	RO	1b
13	**100BASE-X Half Duplex** This bit displays the status of 100BASE-X half duplex compatibility. 0 = PHY not able to perform 100BASE-X half duplex 1 = PHY able to perform 100BASE-X half duplex	RO	1b
12	**10BASE-T Full Duplex** This bit displays the status of 10BASE-T full duplex compatibility. 0 = PHY not able to perform 10BASE-T full duplex 1 = PHY able to perform 10BASE-T full duplex	RO	1b
11	**10BASE-T Half Duplex** This bit displays the status of 10BASE-T half duplex compatibility. 0 = PHY not able to perform 10BASE-T half duplex 1 = PHY able to perform 10BASE-T half duplex	RO	1b
10	**100BASE-T2 Full Duplex** This bit displays the status of 100BASE-T2 full duplex compatibility. 0 = PHY not able to perform 100BASE-T2 full duplex 1 = PHY able to perform 100BASE-T2 full duplex	RO	0b
9	**100BASE-T2 Half Duplex** This bit displays the status of 100BASE-T2 half duplex compatibility. 0 = PHY not able to perform 100BASE-T2 half duplex 1 = PHY able to perform 100BASE-T2 half duplex	RO	0b
8	**Extended Status** This bit displays whether extended status information is in register 15 (per IEEE 802.3 clause 22.2.4). 0 = No extended status information in Register 15 1 = Extended status information in Register 15	RO	1b

Bits	Description	Type	Default
7	**Unidirectional Ability** This bit indicates whether the PHY is able to transmit regardless of whether the PHY has determined that a valid link has been established. 0 = Can only transmit when a valid link has been established 1 = Can transmit regardless	RO	0b
6	**MF Preamble Suppression** This bit indicates whether the PHY accepts management frames with the preamble suppressed. 0 = Management frames with preamble suppressed not accepted 1 = Management frames with preamble suppressed accepted	RO	1b
5	**Auto-Negotiation Complete** This bit indicates the status of the Auto-Negotiation process. 0 = Auto-Negotiation process not completed 1 = Auto-Negotiation process completed	RO	0b
4	**Remote Fault** This bit indicates if a remote fault condition has been detected. 0 = No remote fault condition detected 1 = Remote fault condition detected	RO/LH	0b
3	**Auto-Negotiation Ability** This bit indicates the PHY's Auto-Negotiation ability. 0 = PHY is unable to perform Auto-Negotiation 1 = PHY is able to perform Auto-Negotiation	RO	1b
2	**Link Status** This bit indicates the status of the link. 0 = Link is down 1 = Link is up	RO/LL	0b
1	**Jabber Detect** This bit indicates the status of the jabber condition. 0 = No jabber condition detected 1 = Jabber condition detected	RO/LH	0b
0	**Extended Capability** This bit indicates whether extended register capability is supported. 0 = Basic register set capabilities only 1 = Extended register set capabilities	RO	1b

3.3 Device Identifier 1 Register

Index (In decimal): 2 Size: 16 bits

This register contains the MSB of the Organizationally Unique Identifier (OUI) for the PHY. The LSB of the PHY OUI is contained in the Device Identifier 2 Register.

Bits	Description	Type	Default
15:0	**PHY ID Number (MSB)** Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	Note 1

Note 1: This value is set by chip TOP.

3.4 Device Identifier 2 Register

Index (In decimal): 3 Size: 16 bits

This register contains the LSB of the Organizationally Unique Identifier (OUI) for the PHY. The MSB of the PHY OUI is contained in the Device Identifier 1 Register.

Bits	Description	Type	Default
15:10	**PHY ID Number (LSB)** Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	Note 1
9:4	**Model Number [5:0]** Six-bit manufacturer's model number.	RO	Note 1
3:0	**Revision Number [3:0]** Four-bit manufacturer's revision number.	RO	Note 1

Note 1: This value is set by chip TOP.

3.5 Auto-Negotiation Advertisement Register

Index (In decimal): 4 Size: 16 bits

This read/write register contains the advertised ability of the PHY and is used in the Auto-Negotiation process with the link partner.

Bits	Description	Type	Default
15	**Next Page** 0 = No next page ability 1 = Next page capable	R/W	0b
14	**RESERVED**	RO	—
13	**Remote Fault** This bit determines if remote fault indication will be advertised to the link partner. 0 = Remote fault indication not advertised 1 = Remote fault indication advertised	R/W	0b
12	**Extended Next Page** See EP 7.59 for UNH override.	RO	0b
11	**Asymmetric Pause** This bit determines the advertised asymmetric pause capability. 0 = No Asymmetric PAUSE toward link partner advertised 1 = Asymmetric PAUSE toward link partner advertised **Note:** The default is set based on the DGT_gb_flow_ctrl_en configuration input.	R/W	1b
10	**Symmetric Pause** This bit determines the advertised symmetric pause capability. 0 = No Symmetric PAUSE toward link partner advertised 1 = Symmetric PAUSE toward link partner advertised **Note:** The default is set based on the DGT_gb_flow_ctrl_en configuration input.	R/W	1b
9	**100BASE-T4** 0 = No T4 ability 1 = T4 able See EP 7.59 for UNH override.	RO	0
8	**100BASE-X Full Duplex** This bit determines the advertised 100BASE-X full duplex capability. 0 = 100BASE-X full duplex ability not advertised 1 = 100BASE-X full duplex ability advertised	R/W	Note 1
7	**100BASE-X Half Duplex** This bit determines the advertised 100BASE-X half duplex capability. 0 = 100BASE-X half duplex ability not advertised 1 = 100BASE-X half duplex ability advertised	R/W	Note 1

Note 1: The default is set by the values in the Operation Mode Strap Override Low Register and the Operation Mode Strap Override High Register.

Bits	Description	Type	Default
6	**10BASE-T Full Duplex** This bit determines the advertised 10BASE-T full duplex capability. 0 = 10BASE-T full duplex ability not advertised 1 = 10BASE-T full duplex ability advertised	R/W	Note 1
5	**10BASE-T Half Duplex** This bit determines the advertised 10BASE-T half duplex capability. 0 = 10BASE-T half duplex ability not advertised 1 = 10BASE-T half duplex ability advertised	R/W	Note 1
4:0	**Selector Field [4:0]** This field identifies the type of message being sent by Auto-Negotiation. 00001 = IEEE 802.3	R/W	00001b

Note 1: The default is set by the values in the Operation Mode Strap Override Low Register and the Operation Mode Strap Override High Register.

3.6 Auto-Negotiation Link Partner Base Page Ability Register

Index (In decimal): 5 Size: 16 bits

This read-only register contains the advertised ability of the link partner's PHY and is used in the Auto-Negotiation process between the link partner and the PHY.

Bits	Description	Type	Default
15	**Next Page** This bit indicates the link partner PHY page capability. 0 = Link partner PHY does not advertise next page capability 1 = Link partner PHY advertises next page capability	RO	0b
14	**Acknowledge** This bit indicates whether the link code word has been received from the partner. 0 = Link code word not yet received from partner 1 = Link code word received from partner	RO	0b
13	**Remote Fault** This bit indicates whether a remote fault has been detected. 0 = No remote fault 1 = Remote fault detected	RO	0b
12	**Extended Next Page** 0 = Link partner PHY does not advertise extended next page capability 1 = Link partner PHY advertises extended next page capability	RO	0b
11	**Asymmetric Pause** This bit indicates the link partner PHY asymmetric pause capability. 0 = No Asymmetric PAUSE toward link partner 1 = Asymmetric PAUSE toward link partner	RO	0b

Bits	Description	Type	Default
10	**Pause** This bit indicates the link partner PHY symmetric pause capability. 0 = No Symmetric PAUSE toward link partner 1 = Symmetric PAUSE toward link partner	RO	0b
9	**100BASE-T4** This bit indicates the link partner PHY 100BASE-T4 capability. 0 = 100BASE-T4 ability not supported 1 = 100BASE-T4 ability supported	RO	0b
8	**100BASE-X Full Duplex** This bit indicates the link partner PHY 100BASE-X full duplex capability. 0 = 100BASE-X full duplex ability not supported 1 = 100BASE-X full duplex ability supported	RO	0b
7	**100BASE-X Half Duplex** This bit indicates the link partner PHY 100BASE-X half duplex capability. 0 = 100BASE-X half duplex ability not supported 1 = 100BASE-X half duplex ability supported	RO	0b
6	**10BASE-T Full Duplex** This bit indicates the link partner PHY 10BASE-T full duplex capability. 0 = 10BASE-T full duplex ability not supported 1 = 10BASE-T full duplex ability supported	RO	0b
5	**10BASE-T Half Duplex** This bit indicates the link partner PHY 10BASE-T half duplex capability. 0 = 10BASE-T half duplex ability not supported 1 = 10BASE-T half duplex ability supported	RO	0b
4:0	**Selector Field [4:0]** This field identifies the type of message being sent by Auto-Negotiation. 00001 = IEEE 802.3	RO	00000b

3.7 Auto-Negotiation Expansion Register

Index (In decimal): 6 Size: 16 bits

This read/write register is used in the Auto-Negotiation process between the link partner and the PHY.

Note: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6	**Receive Next Page Location Able** 0 = Received next page storage location is not specified by bit 6.5 1 = Received next page storage location is specified by bit 6.5	RO	1b
5	**Received Next Page Storage Location** 0 = Link partner next pages are stored in the Auto-Negotiation Link Partner Base Page Ability Register (PHY register 5) 1 = Link partner next pages are stored in the Auto-Negotiation Next Page RX Register (PHY register 8)	RO	1b
4	**Parallel Detection Fault** This bit indicates whether a Parallel Detection Fault has been detected. 0 = A fault has not been detected via the Parallel Detection function 1 = A fault has been detected via the Parallel Detection function	RO/LH	0b
3	**Link Partner Next Page Able** This bit indicates whether the link partner has next page ability. 0 = Link partner does not contain next page capability 1 = Link partner contains next page capability	RO	0b
2	**Next Page Able** This bit indicates whether the local device has next page ability. 0 = Local device does not contain next page capability 1 = Local device contains next page capability	RO	1b
1	**Page Received** This bit indicates the reception of a new page. 0 = A new page has not been received 1 = A new page has been received	RO/LH	0b
0	**Link Partner Auto-Negotiation Able** This bit indicates the Auto-Negotiation ability of the link partner. 0 = Link partner is not Auto-Negotiation able 1 = Link partner is Auto-Negotiation able	RO	0b

3.8 Auto-Negotiation Next Page TX Register

Index (In decimal): 7 Size: 16 bits

Bits	Description	Type	Default
15	**Next Page** 0 = No next page ability 1 = Next page capable	R/W	0b
14	**RESERVED**	RO	—
13	**Message Page** 0 = Unformatted page 1 = Message page	R/W	1b
12	**Acknowledge 2** 0 = Device cannot comply with message. 1 = Device will comply with message.	R/W	0b
11	**Toggle** 0 = Previous value was HIGH. 1 = Previous value was LOW.	RO	0b
10:0	**Message Code [10:0]** Message/Unformatted Code Field	R/W	000 0000 0001b

3.9 Auto-Negotiation Next Page RX Register

Index (In decimal): 8 Size: 16 bits

Bits	Description	Type	Default
15	**Next Page** 0 = No next page ability 1 = Next page capable	RO	0b
14	**Acknowledge** This bit indicates whether the link code word has been received from the partner. 0 = Link code word not yet received from partner 1 = Link code word received from partner	RO	0
13	**Message Page** 0 = Unformatted page 1 = Message page	RO	0b
12	**Acknowledge 2** 0 = Device cannot comply with message. 1 = Device will comply with message.	RO	0b
11	**Toggle** 0 = Previous value was HIGH. 1 = Previous value was LOW.	RO	0b
10:0	**Message Code [10:0]** Message/Unformatted Code Field	RO	000 0000 0000b

3.10 Auto-Negotiation Master Slave Control Register

Index (In decimal): 9 Size: 16 bits

Bits	Description	Type	Default
15:13	**Test Mode [2:0]** IEEE 802.3 clause 40.6.1.1.2 transmitter test mode. 000 = Normal mode 001 = Test Mode 1 - Transmit waveform test 010 = Test Mode 2 - Transmit jitter test in Master mode 011 = Test Mode 3 - Transmit jitter test in Slave mode 100 = Test Mode 4 - Transmitter distortion test 101 = Reserved 110 = Reserved 111 = Reserved	R/W	000b
12	**Master/Slave Manual Configuration Enable** 0 = Disable MASTER-SLAVE manual configuration value 1 = Enable MASTER-SLAVE manual configuration value	R/W	Note 1
11	**Master/Slave Manual Configuration Value** Active only when the Master/Slave Manual Configuration Enable bit of this register is 1. 0 = Configure PHY as slave 1 = Configure PHY as master	R/W	Note 1
10	**Port Type** 0 = Single-port device 1 = Multi-port device	R/W	Note 1
9	**1000BASE-T Full Duplex** 0 = Advertise PHY is not 1000BASE-T full duplex capable 1 = Advertise PHY is 1000BASE-T full duplex capable	R/W	Note 1
8	**1000BASE-T Half Duplex** 0 = Advertise PHY is not 1000BASE-T half duplex capable 1 = Advertise PHY is 1000BASE-T half duplex capable The device does not support this mode and this bit should always be written as a 0.	R/W	Note 1
7:0	**RESERVED**	RO	—

Note 1: The default is set by the values in the Operation Mode Strap Override Low Register and the Operation Mode Strap Override High Register.

3.11 Auto-Negotiation Master Slave Status Register

Index (In decimal): 10 Size: 16 bits

Note: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit (for single bit fields) or bit-or (for multi-bit fields), such that a bit (or field) is only cleared if it was read as active (or non-zero). This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active or non-zero).

Bits	Description	Type	Default
15	**Master/Slave Configuration Fault** 0 = No MASTER-SLAVE configuration fault detected 1 = MASTER-SLAVE configuration fault detected	RO/LH	0b
14	**Master/Slave Configuration Resolution** 0 = Local PHY configuration resolved to SLAVE 1 = Local PHY configuration resolved to MASTER	RO	0b
13	**Local 1000BASE-T Receiver Status** 0 = Local Receiver not OK 1 = Local Receiver OK	RO	0b
12	**Remote (Link Partner) Receiver Status** 0 = Remote Receiver not OK 1 = Remote Receiver OK	RO	0b
11	**Link Partner Advertised 1000BASE-T Full Duplex Capability** 0 = Link Partner is not capable of 1000BASE-T full duplex 1 = Link Partner is capable of 1000BASE-T full duplex	RO	0b
10	**Link Partner Advertised 1000BASE-T Half Duplex Capability** 0 = Link Partner is not capable of 1000BASE-T half duplex 1 = Link Partner is capable of 1000BASE-T half duplex	RO	0b
9:8	**RESERVED**	RO	—
7:0	**1000BASE-T Idle Error Count [7:0]** Cumulative count of the errors detected when the receiver is receiving idles. This counter halts at a value of 0xFF.	RO/RC	00h

3.12 MMD Access Control Register

Index (In decimal): 13 Size: 16 bits

The MMD Access Control Register and the MMD Access Address/Data Register work together to support IEEE 802.3 Clause 45 MDIO Manageable Device (MMD) indirect access using Clause 22 registers.

Bits	Description	Type	Default
15:14	**MMD Function [1:0]** This field is used to select the desired MMD function: 00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only	R/W	00b
13:5	**RESERVED**	RO	—
4:0	**MMD Device Address (DEVAD) [4:0]** This field is used to select the desired MMD device address.	R/W	00000b

3.13 MMD Access Address/Data Register

Index (In decimal): 14 Size: 16 bits

The MMD Access Control Register and the MMD Access Address/Data Register work together to support IEEE 802.3 Clause 45 MDIO Manageable Device (MMD) indirect access using Clause 22 registers.

Bits	Description	Type	Default
15:0	**MMD Register Address/Data** If the MMD Function field of the MMD Access Control Register is “00”, this field is used to indicate the MMD register address to read/write of the device specified in the MMD Device Address (DEVAD) field. Otherwise, this register is used to read/write data from/to the previously specified MMD address.	R/W	0000h

3.14 Extended Status Register

Index (In decimal): 15 Size: 16 bits

This register is used to monitor the status of the PHY.

Bits	Description	Type	Default
15	**1000BASE-X Full Duplex** This bit displays the status of 1000BASE-X full duplex compatibility. 0 = PHY not able to perform 1000BASE-X full duplex 1 = PHY able to perform 1000BASE-X full duplex	RO	0b
14	**1000BASE-X Half Duplex** This bit displays the status of 1000BASE-X half duplex compatibility. 0 = PHY not able to perform 1000BASE-X half duplex 1 = PHY able to perform 1000BASE-X half duplex	RO	0b
13	**1000BASE-T Full Duplex** This bit displays the status of 1000BASE-T full duplex compatibility. 0 = PHY not able to perform 1000BASE-T full duplex 1 = PHY able to perform 1000BASE-T full duplex	RO	1b
12	**1000BASE-T Half Duplex** This bit displays the status of 1000BASE-T half duplex compatibility. 0 = PHY not able to perform 1000BASE-T half duplex 1 = PHY able to perform 1000BASE-T half duplex	RO	0b
11:0	**RESERVED**	RO	—

3.15 PCS Loop-back Swap/Polarity Control Register

Index (In decimal): 17 Size: 16 bits

Bits	Description	Type	Default
15	**CD Swap** Swap C/D in PCS loop-back	R/W	0b
14	**Polarity control D** D channel polarity control in PCS loop-back	R/W	0b
13	**Polarity control C** C channel polarity control in PCS loop-back	R/W	0b
12	**Polarity control B** B channel polarity control in PCS loop-back	R/W	0b
11	**Polarity control A** A channel polarity control in PCS loop-back	R/W	0b
10	**Idle_timer_en** Enable idle timer for MDC/MDIO	R/W	0b
9	**Disable_mdo_drv** 0 = Open drain 1 = Push-pull **Note:** Disable_mdo_drv must only be set to push-pull when the MDIO station manager is operating MDC as a frequency below 2.5 MHz in order for the setting to be updated reliably over the MDIO bus.	R/W	0b
8	**port_lpbk**	R/W	0b
7:3	**RESERVED/Not Used**	R/W	11110b
2	**en_bt_pream** Enable 10BT preamble	R/W	1b
1	**t10_en** LinkMD for 10BT test enable	R/W	0b
0	**t10_pass_r** LinkMD 10BT pass/fail indicator	RO	0b

3.16 Cable Diagnostic Register

Index (In decimal): 18 Size: 16 bits

Bits	Description	Type	Default
15	**Cable Diagnostics Test Enable (VCT_EN)** Writing a 1 enables the test. This bit is self-cleared when the test is complete. Writing a 0 will disable the test. Reading a 0 indicates the cable diagnostic test is completed and the status information is valid. Reading a 1 indicates the cable diagnostic test is in progress and the status information is NOT valid.	R/W/SC	0b
14	**Cable Diagnostic Disable Transmitter (VCT_DIS_TX)** [0] = The transmitter is enabled to start cable diagnostic. [1] = The transmitter is disabled and cable diagnostic is on hold to break down the link.	R/W	0b
13:12	**Cable Diagnostics Test Pair (VCT_PAIR[1:0])** This field defines which channel to be tested. 00 = Pair A 01 = Pair B 10 = Pair C 11 = Pair D	R/W	00b
11:10	**Bit[9:0] Definition (VCT_SEL[1:0])** Defines the meaning of bit[9:0] as: 00 = Bit[9:0] is VCT result, i.e., VCT_ST[1:0] and VCT_DATA[7:0]. 01 = Bit[9:0] is the threshold for generating high pulse from ADC2VCT[8:0]. Default value is 64. 10 = Bit[9:0] is the threshold for generating low pulse from ADC2VCT[8:0]. Default value is -64. 11 = Reserved	R/W	00b
9:8	**Cable Diagnostics Status (VCT_ST[1:0])** When VCT_SEL = 00, this is the status of cable diagnostics. Valid only when VCT_EN = 0. 00 = Normal, no fault has been detected 01 = Open Fault has been detected 10 = Short Fault has been detected 11 = Cable diagnostic test failed When VCT_SEL! = 00, see details in VCT_SEL.	RO	00b

Bits	Description	Type	Default
7:0	**Cable Diagnostics Data or Threshold (VCT_DATA[7:0])** When VCT_SEL! = 00, see details in VCT_SEL. When VCT_SEL = 00, this is the data of cable diagnostics. Valid only when VCT_EN = 0. (1) If cable is normal, i.e., VCT_ST = 00, VCT_DATA don't care. (2) If cable is open or short, i.e., VCT_ST = 01 or 10, the distance to fault is approximately 0.8 * (VCT_DATA - 22) (Meters) (see Section 7.17) (3) If cable diagnostics failed, i.e., VCT_ST = 11, Bit[7] = 1 means invalid reflected pulse width, i.e. equal or greater than 152ns, equal or less than 48 ns. Bit[6] = 1 means cable has signal for too long time during WAIT state. It is unusual and for debug only. Bit[5] = 1 means mask100 detected and no silent time window can be found for diagnostics. It means high frequency signal is found on the line. The link partner probably is in forced 100BT or 1000BT mode. Bit[4] = 1 means signals faster than NLP and FLP exists and no silent time window can be found for diagnostics. It's unusual and for debug only. Bit[3:2] = number of low pulses detected. If more than 3, stay at 3. Bit[1:0] = number of high pulses detected. If more than 3, stay at 3.	RO	00h

3.17 Digital PMA/PCS Status Register

Index (In decimal): 19 Size: 16 bits

Note: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15	**A channel FIFO error** Indicates ADC FIFO overflow or underflow	RC	0b
14	**B channel FIFO error** Indicates ADC FIFO overflow or underflow	RC	0b
13	**C channel FIFO error** Indicates ADC FIFO overflow or underflow	RC	0b
12	**D channel FIFO error** Indicates ADC FIFO overflow or underflow	RC	0b
11	**A killer pattern detected** Indicate BLW pattern detected in A	RC	0b
10	**B killer pattern detected** Indicate BLW pattern detected in B	RC	0b
9	**C killer pattern detected** Indicate BLW pattern detected in C	RC	0b
8	**D killer pattern detected** Indicate BLW pattern detected in D	RC	0b
7	**RESERVED**	RO	—
6	**A DSP error detected** Indicate a DSP error detected in A	RC	0b
5	**B DSP error detected** Indicates a DSP error detected in B	RC	0b
4	**C DSP error detected** Indicates a DSP error detected in C	RC	0b
3	**D DSP error detected** Indicates a DSP error detected in D	RC	0b
2	**Equalizer training completed** Channel equalizer training status 1 = Equalizer OK, ready to train scrambler 0 = Equalizer not OK	RO	0b
1	**1000BT link status** 1000 BT link status 1 = Link status OK 0 = Link status not OK	RO	0b
0	**100BT link status** 100 BT link status 1 = Link status OK 0 = Link status not OK	RO	0b

3.18 RXER Counter Register

Index (In decimal): 21 Size: 16 bits

Note:	RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit (for single bit fields) or bit-or (for multi-bit fields), such that a bit (or field) is only cleared if it was read as active (or non-zero). This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active or non-zero).

Bits	Description	Type	Default
15:0	**RXER Counter [15:0]** RX Error counter for the RX_ER signal **Note:** This counter halts at a value of 0xFFFF.	RC	0000h

3.19 EP Access Control Register

Index (In decimal): 22 Size: 16 bits

The EP Access Control Register and the EP Access Address/Data Register work together to support indirect access to vendor-specific Extended Page (EP) registers using Clause 22 registers.

Bits	Description	Type	Default
15:14	**EP Function [1:0]** This field is used to select the desired Extended Page function: 00 = EP Register Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only	R/W	00b
13:5	**RESERVED**	RO	—
4:0	**EP Index [4:0]** This field is used to select the desired Extended Page.	R/W	00000b

3.20 EP Access Address/Data Register

Index (In decimal): 23 Size: 16 bits

The EP Access Control Register and the EP Access Address/Data Register work together to support indirect access to vendor-specific Extended Page (EP) registers using Clause 22 registers.

Bits	Description	Type	Default
15:0	**EP Register Address/Data [15:0]** If the EP Function field of the EP Access Control Register is “00”, this field is used to indicate the EP register address to read/write of the Extended Page specified in the EP Index field. Otherwise, this register is used to read/write data from/to the previously specified EP register address.	R/W	0000h

3.21 GPHY Interrupt Enable Register

Index (In decimal): 24 Size: 16 bits

Bits	Description	Type	Default
15:13	**RESERVED**	RO	—
12	**FLF Interrupt Enable** 1 = Enable Fast Link Fail interrupt 0 = Disable Fast Link Fail interrupt	R/W	0b
11	**Energy Not Detected Interrupt Enable** 1 = Enable “energy not detected” interrupt 0 = Disable “energy not detected” interrupt	R/W	0b
10	**Energy Detected Interrupt Enable** 1 = Enable energy detected interrupt 0 = Disable energy detected interrupt	R/W	0b
9	**RESERVED**	RO	—
8	**RESERVED**	RO	—
7	**Jabber Interrupt Enable** 1 = Enable jabber interrupt 0 = Disable jabber interrupt	R/W	0b
6	**Receive Error Interrupt Enable** 1 = Enable receive error interrupt 0 = Disable receive error interrupt	R/W	0b
5	**Page Received Interrupt Enable** 1 = Enable page received interrupt 0 = Disable page received interrupt	R/W	0b
4	**Parallel Detect Fault Interrupt Enable** 1 = Enable parallel detection fault interrupt 0 = Disable parallel detection fault interrupt	R/W	0b
3	**Link Partner Acknowledge Interrupt Enable** 1 = Enable link partner acknowledge interrupt 0 = Disable link partner acknowledge interrupt	R/W	0b

Bits	Description	Type	Default
2	**Link Down Interrupt Enable** 1 = Enable link down interrupt 0 = Disable link down interrupt	R/W	0b
1	**Remote Fault Interrupt Enable** 1 = Enable remote fault interrupt 0 = Disable remote fault interrupt	R/W	0b
0	**Link Up Interrupt Enable** 1 = Enable link up interrupt 0 = Disable link up interrupt	R/W	0b

3.22 GPHY Revision Register

Index (In decimal): 25 Size: 16 bits

Bits	Description	Type	Default
15:0	**GPHY_HM_REVISION** This register provides the GPHY Hard Macro revision.	R/W	Note 1

Note 1: The revision is set within the GPHY Hard Macro. The first version will be set to 0000h, subsequent revisions will increment this field.

3.23 GPHY Interrupt Status Register

Index (In decimal): 27 Size: 16 bits

Reading this register clears the RC interrupt sources. RO sources must be cleared at their lower level register.

Interrupt status bits in this register reflect the state of the interrupt source regardless of the state of the corresponding enable.

ENGINEERING NOTE: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15:13	**RESERVED**	RO	—
12	**FLF Interrupt** 1 = FLF interrupt 0 = No FLF interrupt This bit is set when the 'FLF status' bit in the EP 0 FLF Configuration and Status Register changes from 0 to 1.	RC	0b
11	**Energy Not Detected Interrupt** 1 = "Energy not detected" interrupt 0 = No "energy not detected" interrupt This bit is set when the EDPD low power bit in the Analog Control Register 8 changes from 0 to 1.	RC	0b
10	**Energy Detected Interrupt** 1 = Energy detected interrupt 0 = No energy detected interrupt This bit is set when the EDPD low power bit in the Analog Control Register 8 changes from 1 to 0.	RC	0b
9	**RESERVED**	RO	—
8	**RESERVED**	RO	—
7	**Jabber Interrupt** 1 = Jabber interrupt 0 = No jabber interrupt	RC	0b
6	**Receive Error Interrupt** 1 = Receive error interrupt 0 = No receive error interrupt	RC	0b
5	**Page Receive Interrupt** 1 = Page receive interrupt 0 = No page receive interrupt	RC	0b
4	**Parallel Detect Fault Interrupt** 1 = Parallel detection fault interrupt 0 = No parallel detection fault interrupt	RC	0b
3	**Link Partner Acknowledge Interrupt** 1 = Link partner acknowledge interrupt 0 = No link partner acknowledge interrupt	RC	0b

Bits	Description	Type	Default
2	**Link Down Interrupt** 1 = Link down interrupt 0 = No link down interrupt	RC	0b
1	**Remote Fault Interrupt** 1 = Remote fault interrupt 0 = No remote fault interrupt	RC	0b
0	**Link Up Interrupt** 1 = Link up interrupt 0 = No link up interrupt	RC	0b

3.24 Digital Debug Control 1 Register

Index (In decimal): 28 Size: 16 bits

Bits	Description	Type	Default
15	**auto_swap_fastlink** 1 = Enable auto swap 0 = Disable	R/W	1b
14	**Select register clock speed** 0 = 125 MHz for mreg 1 = 25 Mhz **Note:** Since the DGT_MDC_sel configuration input is tied high, this bit is not used and the register clock speed is always 25 Mhz.	R/W	0b
13	**Force_lp_txfcable** **Note:** The default is set based on the DGT_gb_flow_ctrl_en configuration input.	R/W	1b
12	**adc_fifo_rsten** Enable ADC FIFO auto-reset mechanism	R/W	0b
11	**skew_debug** 1 = Turn on pcs1000 lane skew debug mode 0 = Turn off pcs1000 lane skew debug mode	R/W	0b
10	**Force_lp_rxfcable** **Note:** The default is set based on the DGT_gb_flow_ctrl_en configuration input.	R/W	1b
9:8	**td_depth_smu[1:0]** Trellis decoder depth mu parameter	R/W	00b
7	**mdi_set** mdi_set has no function when swapoff (reg28.6) is de-asserted. When swapoff is asserted, if mdi_set is asserted, chip will operate at MDI mode. When swapoff is asserted, if mdi_set is de-asserted, chip will operate at MDI-X mode.	R/W	Note 1
6	**swapoff** 1 = Disable auto crossover function. 0 = Enable auto crossover function.	R/W	Note 1
5	**td_use_st_info** 1 = Use the valid survival paths to select the next survival symbol. 0 = Default.	R/W	0b

Note 1: The default is set by the values in the Operation Mode Strap Override Low Register and the Operation Mode Strap Override High Register.

Bits	Description	Type	Default
4	**td_lowest_costN** 1 = Choose arbitrarily a symbol from available survival symbols. 0 = Default. Choose the survival symbol with the lowest cost.	R/W	0b
3	**td_init_state** 1 = Assume that the state is in state 0 when the trellis decoder is reset. 0 = Default.	R/W	0b
2	**turn_off_trellis** 1 = Trellis decoder off 0 = Trellis decoder on	R/W	0b
1	**disable_psa** 1 = pcs1000 pair swap off 0 = pcs1000 pair swap on	R/W	0b
0	**PCS Loop back** 1 = Turn off trellis decoder (reg28.2) 0 = Normal function	R/W	0b

Note 1: The default is set by the values in the Operation Mode Strap Override Low Register and the Operation Mode Strap Override High Register.

3.25 Reserved Register

Index (In decimal): 30 Size: 16 bits

Bits	Description	Type	Default
15:12	**Fixed 100BT latency[3:0]** bit 15 = Fixed latency mode enable bit 14 = Serial to parallel FIFO 5-bit code selection bit 13 = Bypass serial to parallel FIFO bit 12 = Receive load selection	R/W	1111b
11	**eee_scr_rst_en**	R/W	1b
10	**Fixed 10BT latency** 0 = Lower but variable 10BASE-T receive latency 1 = Higher but fixed 10BASE-T receive latency	R/W	1b
9	**RESERVED**	RO	—
8:6	**Ptl_clk125_skew[2:0]** Clock skew	R/W	000b
5	**Cr_eee_block** 0 = While in debug mode do not block txer, txen	R/W	0b
4	**Link_down_disable** Force link down when Register 0 bit 11 Software Power Down (SPD) = 1	R/W	0b
3	**Ext_lpbk**	R/W	0b
2	**UNH_NLP_test** Increase NLP_MAX to 55 ms	R/W	0b
1	**mr_disable_waveshap** Using in DSP to select TI coeff.	R/W	0b
0	**en_syncE_100_leaf_node** For last phy at 100BT	R/W	0b

3.26 Control Register

Index (In decimal): 31 Size: 16 bits

ENGINEERING NOTE: RC, LL, and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15	**Dis_geee_tx_state_ctrl** 1 = Disable 0 = Enable	R/W	0b
14	**RESERVED**	R/W	0b
13	**Repeater Mode** 1 = Enable repeater mode 0 = Disable	R/W	0b
12	**Force Link** 1 = Force link up 0 = Normal	R/W	0b
11	**txfifo_under** transmit FIFO underflow	RO/LH	0b
10	**txfifo_over** transmit FIFO overflow	RO/LH	0b
9	**Enable Jabber** 1 = Enable jabber counter 0 = Disable	R/W	1b
8	**Enable SQE Test** 1 = Enable SQE test 0 = Disable	R/W	1b
7	**No Cipher** 1 = Disable scrambler 0 = Enable scrambler	R/W	0b
6	**Speed status 1000T** Indicates speed is 1000T	RO	0b
5	**Speed status 100TX** Indicates speed is 100TX	RO	0b
4	**Speed status 10BT** Indicates speed is 10BT	RO	0b
3	**Duplex status** Indicates duplex status	RO	0b
2	**1000BASE-T Mater/Slave status** 1 = Indicates 1000BASE-T Master mode 0 = Indicates 1000BASE-T Slave mode	RO	0b
1	**Software Soft Reset** When set, this bit resets the PHY except all registers. This bit is self clearing. 1 = PHY software soft reset.	R/W1S/SC	0b

Bits	Description	Type	Default
0	**Link Status Check Fail** 1 = Fail 0 = Not Failing	RC	0b

4.0 MMD INDIRECT REGISTERS

MMD registers provide indirect read/write access to up to 32 MMD device addresses with each device supporting up to 65,536 16-bit registers, as defined in Clause 22 of the IEEE 802.3 Specification. This device, however, uses only two MMD devices.

The following two standard registers serve as the portal registers to access the indirect MMD registers.

- MMD Access Control Register
- MMD Access Address/Data Register

EXAMPLE 4-1: MMD REGISTER WRITE

Write 0001h to MMD 3 Register 00h.

1. Write 0003h to the MMD Access Control Register // Select Register Address for MMD 3.
2. Write 0000h to the MMD Access Address/Data Register // Set Register Address to 00h.
3. Write 4003h to the MMD Access Control Register // Select Data Value for MMD 3.
4. Write 0001h to the MMD Access Address/Data Register // Write 0001h to MMD 3 Register 00h.

EXAMPLE 4-2: MMD REGISTER READ

Read MMD 3 Register 00h.

1. Write 0003h to the MMD Access Control Register // Select Register Address for MMD 3.
2. Write 000h to the MMD Access Address/Data Register // Set Register Address to 00h.
3. Write 4003h to the MMD Access Control Register // Select Data Value for MMD 3.
4. Read the MMD Access Address/Data Register // Read Data Value from MMD 3 Register 00h.

4.1 MMD 3 Registers

4.1.1 PCS STATUS 1 REGISTER

Index (In decimal): MMD 3.1 Size: 16 bits

For the LL and LH bits, if the host reads this register as a new condition corresponding to the same bit occurs, the LL/LH bit will remain cleared/set. If a level event remains asserted, then the corresponding bit will remain cleared/set.

ENGINEERING NOTE: RC, LL ,and LH bits are updated at the end of the read command. Depending on the timing, a serial read can finish simultaneously with an event (start read, capture data, event and end read) or it can overlap an event (start read, capture data, event then end read). To ensure that an event is never missed, the clear on read logic is gated with the read data, bit for bit, such that a bit is only cleared if it was read as active. This has a natural consequence that in the event of a simultaneousness event and end read, the event will have priority (if the bit was not previously active).

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11	**TX LPI received** 1 = TX PCS has received LPI 0 = LPI not received	RO/LH	0b
10	**RX LPI received** 1 = RX PCS has received LPI 0 = LPI not received	RO/LH	0b
9	**TX LPI indication** 1 = TX PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO	0b
8	**RX LPI indication** 1 = RX PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO	0b
7	**Fault** 1 = Fault condition detected 0 = No fault condition detected	RO	0b
6	**RESERVED**	RO	—
5:3	**RESERVED**	RO	—
2	**PCS receive link status** 1 = PCS receive link up 0 = PCS receive link down **Note:** Per IEEE 802.3, this bit is supposed to be Latch Low	RO	0b
1	**Low-power ability** 1 = PCS supports low-power mode 0 = PCS does not support low-power mode	RO	Note 1
0	**RESERVED**	RO	—

Note 1: This bit is a 1 if either the 1000BASE-T EEE or 100BASE-TX EEE bit in the EEE Advertisement Register is set. Otherwise it is a 0.

4.1.2 EEE CONTROL AND CAPABILITY REGISTER

Index (In decimal): MMD 3.20 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13	**100GBASE-R deep sleep** 1 = EEE deep sleep is supported for 100GBASE-R 0 = EEE deep sleep is not supported for 100GBASE-R **Note:** The device does not support this mode.	RO	0b
12	**100GBASE-R fast wake** 1 = EEE fast wake is supported for 100GBASE-R 0 = EEE fast wake is not supported for 100GBASE-R **Note:** The device does not support this mode.	RO	0b
11:10	**RESERVED**	RO	—
9	**40GBASE-R deep sleep** 1 = EEE deep sleep is supported for 40GBASE-R **Note:** 0 = EEE deep sleep is not supported for 40GBASE-R The device does not support this mode.	RO	0b
8	**40GBASE-R fast wake** 1 = EEE fast wake is supported for 40GBASE-R 0 = EEE fast wake is not supported for 40GBASE-R **Note:** The device does not support this mode.	RO	0b
7	**RESERVED**	RO	—
6	**10GBASE-KR EEE** 0 = EEE is not supported for 10GBASE-KR. 1 = EEE is supported for 10GBASE-KR. **Note:** The device does not support this mode.	RO	0b
5	**10GBASE-KX4 EEE** 0 = EEE is not supported for 10GBASE-KX4. 1 = EEE is supported for 10GBASE-KX4. **3:** The device does not support this mode.	RO	0b
4	**10GBASE-KX EEE** 0 = EEE is not supported for 10GBASE-KX. 1 = EEE is supported for 10GBASE-KX. **Note:** The device does not support this mode.	RO	0b
3	**10GBASE-T EEE** 0 = EEE is not supported for 10GBASE-T. 1 = EEE is supported for 10GBASE-T. **Note:** The device does not support this mode.	RO	0b
2	**1000BASE-T EEE** 0 = EEE is not supported for 1000BASE-T. 1 = EEE is supported for 1000BASE-T.	RO	1b
1	**100BASE-TX EEE** 0 = EEE is not supported for 100BASE-TX. 1 = EEE is supported for 100BASE-TX.	RO	1b
0	**RESERVED**	RO	—

4.2 MMD 7 Registers

4.2.1 EEE ADVERTISEMENT REGISTER

Index (In decimal): MMD 7.60 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED** **Note:** Per IEEE 802.3, these bits are supposed to be read only.	RO	—
13	**100GBASE-CR4 EEE** 0 = Do not advertise EEE capability for 100GBASE-CR4 deep sleep 1 = Advertise EEE capability for 100GBASE-CR4 deep sleep **Note:** The device does not support this mode. This bit is not used.	R/W	0b
12	**100GBASE-KR4 EEE** 0 = Do not advertise EEE capability for 100GBASE-KR4 deep sleep 1 = Advertise EEE capability for 100GBASE-KR4 deep sleep **Note:** The device does not support this mode. This bit is not used.	R/W	0b
11	**100GBASE-KP4 EEE** 0 = Do not advertise EEE capability for 100GBASE-KP4 deep sleep 1 = Advertise EEE capability for 100GBASE-KP4 deep sleep **Note:** The device does not support this mode. This bit is not used.	R/W	0b
10	**100GBASE-CR10 EEE** 0 = Do not advertise EEE capability for 100GBASE-CR10 deep sleep 1 = Advertise EEE capability for 100GBASE-CR10 deep sleep **Note:** The device does not support this mode.	R/W	0b
9	**RESERVED** **Note:** Per IEEE 802.3, this bit is supposed to be read only	RO	—
8	**40GBASE-CR4 EEE** 0 = Do not advertise EEE capability for 40GBASE-CR4 deep sleep 1 = Advertise EEE capability for 40GBASE-CR4 deep sleep **Note:** The device does not support this mode.	R/W	0b
7	**40GBASE-KR4 EEE** 0 = Do not advertise EEE capability for 40GBASE-KR4 deep sleep 1 = Advertise EEE capability for 40GBASE-KR4 deep sleep **Note:** The device does not support this mode.	R/W	0b
6	**10GBASE-KR EEE** 0 = Do not advertise EEE capability for 10GBASE-KR 1 = Advertise EEE capability for 10GBASE-KR **Note:** The device does not support this mode.	R/W	0b
5	**10GBASE-KX4 EEE** 0 = Do not advertise EEE capability for 10GBASE-KX4 1 = Advertise EEE capability for 10GBASE-KX4 **Note:** The device does not support this mode.	R/W	0b

Note 1: The default is set by the values in the Operation Mode Strap Override Low Register and the Operation Mode Strap Override High Register.

Bits	Description	Type	Default
4	**10GBASE-KX EEE** 0 = Do not advertise EEE capability for 10GBASE-KX 1 = Advertise EEE capability for 10GBASE-KX **Note:** The device does not support this mode.	R/W	0b
3	**10GBASE-T EEE** 0 = Do not advertise EEE capability for 10GBASE-T 1 = Advertise EEE capability for 10GBASE-T **Note:** The device does not support this mode.	R/W	0b
2	**1000BASE-T EEE** 0 = Do not advertise EEE capability for 1000BASE-T 1 = Advertise EEE capability for 1000BASE-T	R/W	Note 1
1	**100BASE-TX EEE** 0 = Do not advertise EEE capability for 100BASE-TX. 1 = Advertise EEE capability for 100BASE-TX.	R/W	Note 1
0	**RESERVED** **Note:** Per IEEE 802.3, this bit is supposed to be read only	RO	—

Note 1: The default is set by the values in the Operation Mode Strap Override Low Register and the Operation Mode Strap Override High Register.

4.2.2 EEE LINK PARTNER ABILITY REGISTER

Index (In decimal): MMD 7.61 Size: 16 bits

Bits	Description	Type	Default
15:11	**RESERVED** **Note:** Per IEEE 802.3, these bits are supposed to be read only	RO	—
10	**100GBASE-CR10 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 100GBASE-CR10. 1 = Link partner advertises EEE deep sleep capability for 100GBASE-CR10. **Note:** This device does not support this mode.	RO	0b
9	**RESERVED**	RO	0b
8	**40GBASE-CR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-CR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-CR4. **Note:** This device does not support this mode.	RO	0b
7	**40GBASE-KR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-KR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-KR4. **Note:** This device does not support this mode.	RO	0b
6	**10GBASE-KR EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KR. 1 = Link partner advertises EEE capability for 10GBASE-KR. **Note:** This device does not support this mode.	RO	0b
5	**10GBASE-KX4 EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX4. 1 = Link partner advertises EEE capability for 10GBASE-KX4. **Note:** This device does not support this mode.	RO	0b
4	**10GBASE-KX EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX. 1 = Link partner advertises EEE capability for 10GBASE-KX. **Note:** This device does not support this mode.	RO	0b
3	**10GBASE-T EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-T. 1 = Link partner advertises EEE capability for 10GBASE-T. **Note:** This device does not support this mode.	RO	0b
2	**1000BASE-T EEE** 0 = Link partner does not advertise EEE capability for 1000BASE-T. 1 = Link partner advertises EEE capability for 1000BASE-T.	RO	0b
1	**100BASE-TX EEE** 0 = Link partner does not advertise EEE capability for 100BASE-TX. 1 = Link partner advertises EEE capability for 100BASE-TX.	RO	0b
0	**RESERVED**	RO	—

5.0 EXTENDED PAGE INDIRECT REGISTERS

Extended Page registers provide indirect read/write access to up to 32 EP device addresses with each device supporting up to 65,536 16-bit registers. This approach is purposefully similar to the MMD approach but is vendor-specific.

The following two registers serve as the portal registers to access the indirect EP registers.

- EP Access Control Register
- EP Access Address/Data Register

EXAMPLE 5-1: EP REGISTER WRITE

Write 001h to EP 3 Register 00h.

1. Write 0003h to the EP Access Control Register // Select Register Address for EP 3.
2. Write 0000h to the EP Access Address/Data Register // Set Register Address to 00h.
3. Write 4003h to the EP Access Control Register // Select Data Value for EP 3.
4. Write 0001h to the EP Access Address/Data Register // Write 0001h to EP 3 Register 00h.

EXAMPLE 5-2: EP REGISTER READ

Read EP 3 Register 00h.

1. Write 0003h to the EP Access Control Register // Select Register Address for EP 3.
2. Write 0000h to the EP Access Address/Data Register // Set Register Address to 00h.
3. Write 4003h to the EP Access Control Register // Select Dave Value for EP 3.
4. Read the EP Access Address/Data Register // Read Data Value from EP 3 Register 00h.

It is also possible to automatically increment the register address for reads and/or writes

EXAMPLE 5-3: EP REGISTER WRITES WITH POST INCREMENT

Write 0123_4567_89ABh to EP 5 Registers 22Ch – 22Eh (1588 TSU MAC address).

1. Write 0005h to the EP Access Control Register // Select Register Address for EP 5.
2. Write 022Ch to the EP Access Address/Data Register // Set Register Address to 22Ch.
3. Write 8005h or C005h to the EP Access Control Register // Select Data Value for EP 5, with post increment addressing.
4. Write 0123h to the EP Access Address/Data Register // Write 0123h to EP 5 Register 22Ch.
5. Write 4567h to the EP Access Address/Data Register // Write 4567h to EP 5 Register 22Dh.
6. Write 89ABh to the EP Access Address/Data Register // Write 89ABh to EP 5 Register 22Eh.

EXAMPLE 5-4: MMD REGISTER READS WITH POST INCREMENT

Read EP 5 Registers 22Ch – 22Eh (1588 TSU MAC address).

1. Write 0005h to the EP Access Control Register // Select Register Address for EP 5.
2. Write 022Ch to the EP Access Address/Data Register // Set Register Address to 22Ch.
3. Write 8005h to the EP Access Control Register // Select Data Value for EP 5, with post increment addressing.
4. Read the EP Access Address/Data Register // Read Data Value from EP 5 Register 22Ch.
5. Read the EP Access Address/Data Register // Read Data Value from EP 5 Register 22Dh.
6. Read the EP Access Address/Data Register // Read Data Value from EP 5 Register 22Eh.

5.1 Extended Page 0 Registers

5.1.1 FAST LINK FAIL (FLF) CONFIGURATION AND STATUS REGISTER

Index (In decimal): EP 0.15 Size: 16 bits

Bits	Description	Type	Default
15	**10BT_link_loss_100ms_enable** 1 = Enable (use 100 ms) 0 = Disable (use 50 ms)	R/W	0b
14:12	**10BT link loss timer** Configures 10BT FLF timer bits [19:17]. 011 = 50 ms.	R/W	011b
11:3	**RESERVED**	RO	—
2	**FLF Status** 0 = Link is not in FLF state 1 = Link is in FLF state	RO	0b
1	**FLF Enable** 0 = FLF is not enabled on this link 1 = FLF is enabled on this link	R/W	0b
0	**Enable FLF Link Down** 0 = FLF assertion does not directly trigger Link Down 1 = FLF assertion immediately triggers Link Down	R/W	0b

5.1.2 LINK PARTNER FORCE FD OVERRIDE REGISTER

Index (In decimal): EP 0.16 Size: 16 bits

Bits	Description	Type	Default
15:2	**RESERVED**	RO	—
1	**LP Force 100 FD Override** Per 802.3 when Link Partner is set to Force 100, this device will select 100 HD due to Parallel Detect. This bit provides a proprietary override so this device will select 100 FD in this case 0 = Standard operation, this device operates according to 802.3 1 = Proprietary operation, this device selects 100 FD when the Link Partner is set to Force 100	R/W	0b
0	**LP Force 10 FD Override** Per 802.3 when Link Partner is set to Force 10, this device will select 10 HD due to Parallel Detect. This bit provides a proprietary override so this device will select 10 FD in this case 0 = Standard operation, this device operates according to 802.3 1 = Proprietary operation, this device selects 10 FD when the Link Partner is set to Force 10	R/W	0b

5.2 Extended Page 1 Registers

5.2.1 DFE INIT2 100 REGISTER

Index (In decimal): EP 1.119 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14:9	**DEVICE_ere[5:0]** 1G Slave:30, else 0 Master and 100BT override the setting to 00h	R/W	0Eh
8:0	**dfe_init_2_100bt[8:0]**	R/W	030h

5.2.2 PGA TABLE 1G, ENTRY 0 (MAX GAIN) REGISTER

Index (In decimal): EP 1.121 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_0[8:0]**	RW	11Ah

5.2.3 PGA TABLE 1G, ENTRY 1 REGISTER

Index (In decimal): EP 1.122 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_1[8:0]**	RW	0FBh

5.2.4 PGA TABLE 1G, ENTRY 2 REGISTER

Index (In decimal): EP 1.123 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_2[8:0]**	RW	0E0h

5.2.5 PGA TABLE 1G, ENTRY 3 REGISTER

Index (In decimal): EP 1.124 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_3[8:0]**	RW	0C8h

5.2.6 PGA TABLE 1G, ENTRY 4 REGISTER

Index (In decimal): EP 1.125 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_4[8:0]**	RW	0B2h

5.2.7 PGA TABLE 1G, ENTRY 5 REGISTER

Index (In decimal): EP 1.126 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_5[8:0]**	RW	09Fh

5.2.8 PGA TABLE 1G, ENTRY 6 REGISTER

Index (In decimal): EP 1.127 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_6[8:0]**	RW	08Dh

5.2.9 PGA TABLE 1G, ENTRY 7 REGISTER

Index (In decimal): EP 1.128 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_7[8:0]**	RW	07Eh

5.2.10 PGA TABLE 1G, ENTRY 8 REGISTER

Index (In decimal): EP 1.129 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_8[8:0]**	RW	070h

5.2.11 PGA TABLE 1G, ENTRY 9 REGISTER

Index (In decimal): EP 1.130 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_9[8:0]**	RW	064h

5.2.12 PGA TABLE 1G, ENTRY 10 REGISTER

Index (In decimal): EP 1.131 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_10[8:0]**	RW	059h

5.2.13 PGA TABLE 1G, ENTRY 11 REGISTER

Index (In decimal): EP 1.132 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_11[8:0]**	RW	050h

5.2.14 PGA TABLE 1G, ENTRY 12 REGISTER

Index (In decimal): EP 1.133 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_12[8:0]**	RW	047h

5.2.15 PGA TABLE 1G, ENTRY 13 REGISTER

Index (In decimal): EP 1.134 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_13[8:0]**	RW	03Fh

5.2.16 PGA TABLE 1G, ENTRY 14 REGISTER

Index (In decimal): EP 1.135 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_14[8:0]**	RW	038h

5.2.17 PGA TABLE 1G, ENTRY 15 REGISTER

Index (In decimal): EP 1.136 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_15[8:0]**	RW	032h

5.2.18 PGA TABLE 1G, ENTRY 16 REGISTER

Index (In decimal): EP 1.137 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_16[8:0]**	RW	02Dh

5.2.19 PGA TABLE 1G, ENTRY 17 REGISTER

Index (In decimal): EP 1.138 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**pga_table_1G_17[8:0]**	RW	028h

5.2.20 PD CONTROLS REGISTER

Index (In decimal): EP 1.157 Size: 16 bits

Bits	Description	Type	Default
15:9	**level_th[6:0]**	R/W	12h
8:6	**log2_loop_count[2:0]**	R/W	2h
5	**pd_in**	R/W	0b
4	**pd_forced**	R/W	0b
3:0	**pd_measure_time[3:0]** fastmode override the setting to Ch	R/W	Ch

5.3 Extended Page 2 Registers

Note: Register values in this Extended Page 2 (EP2) are **not** reset by mr0 bit 15.

5.3.1 COMMON CONTROL REGISTER

Index (In decimal): EP 2.0 Size: 16 bits

Bits	Description	Type	Default
15	**Res: FastMode** 1 = Fast-Mode, for shorter timers 0 = Normal Mode	R/W	0b
14	**Cr_trans_dis** 1 = Disable trans 0 = Normal Operation	R/W	0b
13	**RESERVED**	RO	—
12	**Disable EEE_fast_mode** 0 = EEE fast mode 1 = Normal mode	R/W	0b
11	**Disable DSP_fast_mode** 0 = DSP fast mode 1 = Normal mode	R/W	0b
10	**Falling Catch** Catch data on Falling edge	R/W	0b
9	**Cr_tx_er disable** 1 = Disable TX ER signal 0 = Normal function	R/W	0b
8	**RESERVED**	RO	—
7:6	**PRBS order [1:0]**	R/W	00b
5	**PRBS inverse**	R/W	0b
4	**RESERVED/Not Used**	RO	—
3	**RESERVED**	RO	—
2	**Miib2b**	R/W	0b
1	**clk125 Enable** A 1 enables the 125 MHz clock output onto the CLK125_NDO pin.	R/W	Note 1
0	**All-PHYAD Enable** When this bit is set, the PHY will respond to PHY address 0 as well as its assigned PHY address.	R/W	Note 1

Note 1: clk125 default is set by the CLK125_EN strapping pin. All-PHYAD Enable default is set by the inverse of the ALLPHYAD strapping pin.

5.3.2 OPERATION MODE STRAP OVERRIDE LOW REGISTER

Index (In decimal): EP 2.2 Size: 16 bits

This register may be used to override the value of the MODE[4:0] configuration straps.

Following an update to this register, a PHY Software Hard Reset (RESET) should be issued for the new value to take effect.

Note: When setting a new value, it is the user's responsibility to ensure that conflicting assignments are not made.

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**Magjack Disable** 0 = Magjack Enable 1 = Magjack Disable	R/W	0b
13	**1000_FD_slave_mode** Forced 1000BASE-T full duplex slave mode 1 = Forced 1000BT FD slave mode	R/W	Note 1
12	**100_HD_mode** Forced 100BASE-TX half duplex mode 1 = Forced 100BT HD mode	R/W	Note 1
11	**100_FD_mode** Forced 100BASE-TX full duplex mode 1 = Forced 100BT FD mode	R/W	Note 1
10	**1000_FD_master_mode** Forced 1000BASE-T full duplex master mode 1 = Forced 1000BT FD master mode	R/W	Note 1
9	**spd_pll_dis_mode** Software Power Down (SPD) with PLL disabled mode 1 = SPD w/pll disabled mode	R/W	Note 1
8	**spd_pll_en_mode** Software Power Down (SPD) with PLL enabled mode 1 = SPD w/pll enable mode	R/W	Note 1
7:0	**RESERVED**	RO	—

Note 1: The default is set by the MODE4, MODE3, MODE2, MODE1, and MODE0 strapping pins as indicated by the corresponding bit in the Operation Mode Strap Low Register.

5.3.3 OPERATION MODE STRAP LOW REGISTER

Index (In decimal): EP 2.3 Size: 16 bits

This register indicates the value of the MODE[4:0] configuration straps that were latched into the device at reset.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13	**Strap_1000_FD_slave_mode** Forced 1000BASE-T full duplex slave Strap-In Status **1 = Forced 1000BT FD slave mode (MODE[4:0]='01101')**	RO	Note 1
12	**Strap_100_HD_mode** Forced 100BASE-TX half duplex Strap-In Status 1 = Forced 100BT HD mode (MODE[4:0]='01100')	RO	Note 1
11	**Strap_100_FD_mode** Forced 100BASE-TX full duplex Strap-In Status 1 = Forced 100BT FD mode (MODE[4:0]='01011')	RO	Note 1
10	**Strap_1000_FD_master_mode** Forced 1000BASE-T full duplex master Strap-In Status 1 = Forced 1000BT FD master mode (MODE[4:0]='01010')	RO	Note 1
9	**Strap_spd_pll_dis_mode** Software Power Down (SPD) with PLL disabled Strap-In Status 1 = SPD w/pll disabled mode (MODE[4:0]='01001')	RO	Note 1
8	**Strap_spd_pll_en_mode** Software Power Down (SPD) with PLL enabled Strap-In Status 1 = SPD w/pll enable mode (MODE[4:0]='01000')	RO	Note 1
7:0	**RESERVED**	RO	—

Note 1: Set by the MODE[4:0] strapping pins.

5.3.4 SELF-TEST PACKET COUNT LO REGISTER

Index (In decimal): EP 2.9 Size: 16 bits

Bits	Description	Type	Default
15:0	**Self_test_frame_cnt[15:0]**	R/W	0000h

5.3.5 SELF-TEST PACKET COUNT HI REGISTER

Index (In decimal): EP 2.10 Size: 16 bits

Bits	Description	Type	Default
15:0	**Self_test_frame_cnt[31:16]**	R/W	0001h

5.3.6 SELF-TEST STATUS REGISTER

Index (In decimal): EP 2.11 Size: 16 bits

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Self_test_done** 0 = Self test running 1 = Self test finished	RO	0b

5.3.7 SELF-TEST FRAME COUNT ENABLE REGISTER

Index (In decimal): EP 2.12 Size: 16 bits

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Self_test_frame_cnt_en** 0 = Disabled 1 = Enabled	R/W	0b

5.3.8 SELF-TEST PGEN ENABLE REGISTER

Index (In decimal): EP 2.13 Size: 16 bits

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Self_test_pgen_en** 0 = Disabled 1 = Enabled	R/W	0b

5.3.9 SELF-TEST ENABLE REGISTER

Index (In decimal): EP 2.14 Size: 16 bits

Bits	Description	Type	Default
15	**Self_test_external_clk_sel** When this bit is high, the self-test function requires a clock to be supplied onto the GTX_CLK input pin. When this bit is low, the self-test function does not require a clock to be supplied.	R/W	0b
14:13	**Self_test_packet_type[1:0]** 00 = Random data bit and SA/DA values 01 = All data bits and SA/DA are 0 10 = All data bits and SA/DA are 1 11 = Random	R/W	00b
12:9	**RESERVED**	RO	—
8	**Self_test_CRC_checker_enable** 1 = Enable 0 = Disable	R/W	0b
7:5	**RESERVED**	RO	—
4	**GMII_TX_CRC_check_en** Enables CRC_checker in Tx path (toward line) 0 = Disabled 1 = Enabled	R/W	0b
3:1	**RESERVED**	RO	—
0	**Self_test_en** 0 = Disabled 1 = Enabled	R/W	0b

5.3.10 1000BT FIX LATENCY ENABLE REGISTER

Index (In decimal): EP 2.15 Size: 16 bits

Bits	Description	Type	Default
15:5	**RESERVED**	RO	—
4	**Fix_lat_1000_type** 1 = 0 or 1 delay 0 = 0, 1, or 2 delay	R/W	0b
3:1	**RESERVED**	RO	—
0	**Fix_lat_1000_en** 1 = Enable fix latency for 1G 0 = Disable fix latency for 1G	R/W	0b

5.3.11 SELF-TEST CORRECT COUNT LO REGISTER

Index (In decimal): EP 2.60 Size: 16 bits

Following a self-test, this register along with Self-Test Correct Count HI Register indicate the count of frames with a correct FCS.

Bits	Description	Type	Default
15:0	**Self_test_correct_cnt[15:0]**	RO	—

5.3.12 SELF-TEST CORRECT COUNT HI REGISTER

Index (In decimal): EP 2.61 Size: 16 bits

Following a self-test, this register along with Self-Test Correct Count LO Register indicate the count of frames with a correct FCS.

Bits	Description	Type	Default
15:0	**Self_test_correct_cnt[31:16]**	RO	—

5.3.13 SELF-TEST ERROR COUNT LO REGISTER

Index (In decimal): EP 2.62 Size: 16 bits

Following a self-test, this register along with Self-Test Error Count HI Register indicate the count of frames with an incorrect FCS.

Bits	Description	Type	Default
15:0	**Self_test_error_cnt[15:0]**	RO	—

5.3.14 SELF-TEST ERROR COUNT HI REGISTER

Index (In decimal): EP 2.63 Size: 16 bits

Following a self-test, this register along with Self-Test Error Count LO Register indicate the count of frames with an incorrect FCS.

Bits	Description	Type	Default
15:0	**Self_test_error_cnt[31:16]**	RO	—

5.3.15 SCR WAIT COUNTER REGISTER

Index (In decimal): EP 2.64 Size: 16 bits

This register along with the SCR Wait Counter Control Register provide for a programmable PCS Symbol Lock Wait timer.

Bits	Description	Type	Default
15:0	**SCR_wait_cnt[15:0]** Lower 16 bits of 18-bit Symbol Lock Wait timer	R/W	FFFFh

5.3.16 SCR WAIT COUNTER CONTROL REGISTER

Index (In decimal): EP 2.65 Size: 16 bits

This register along with the SCR Wait Counter Register provide for a programmable PCS Symbol Lock Wait timer.

Bits	Description	Type	Default
15:6	**RESERVED**	RO	—
5:4	**SCR_wait_cnt[17:16]** Upper two bits of 18-bit Symbol Lock Wait timer	R/W	00b
3:2	**RESERVED**	RO	—
1	**en_counter_sel_EEE** 0 = Bug fix enabled – The PCS Symbol Lock Wait timer is configured using SCR_wait_cnt[17:0], with default setting of 512 µs. 1 = Bug fix disabled. The PCS Symbol Lock Wait timer is hard-wired to the standard value of 512 ns.	R/W	0b
0	**good_pol_ONLY** 0 = Bug fix enabled–check Idle 1 = Bug fix disabled–do not check Idle	R/W	0b

5.3.17 EP2 REGISTER 74

Index (In decimal): EP 2.74 Size: 16 bits

Bits	Description	Type	Default
15	**EP2_74_spare_sel** for alignment reduce to 2.8 µs	R/W	0b
14:2	**RESERVED**	RO	—
1:0	tx_pam swap[1:0] 00: No swap 01: A, B swap 10: A, B swap and C, D swap 11: No swap	R/W	01b

5.3.18 EP2 REGISTER 75

Index (In decimal): EP 2.75 Size: 16 bits

Bits	Description	Type	Default
15	**packet_load_sel**	R/W	0b
14	**Tx_FIFO_bypass** 0 = Tx FIFO not bypassed 1 = Tx FIFO bypassed	R/W	1b
13	**edpd_sd_en**	R/W	0b
12	**edpd_sd_st**	RC	—
11	**RESERVED**	RO	—
10	**leee_sfd_enable** 0 = Check for four or more bytes of 55h 1 = Check for exactly seven bytes of 55h	R/W	0b
9:8	**SOF_preemption_enable[1:0]** These bits enable 802.3br preemption SMD support for the SOF detection. 0x = SMD-E (0xD5/normal SFD) 10 = SMD-V (0x07), SMD-R (0x19), SMD-E (0xD5) and SMD-S[0,1,2,3] (0xE6. 0x4C, 0x7F or 0xB3) 11 = SMD-V (0x07), SMD-R (0x19), SMD-E (0xD5), SMD-S[0,1,2,3] (0xE6. 0x4C, 0x7F or 0xB3) and SMD-C[0,1,2,3] (0x61, 0x52, 0x9E or 0x2A)	R/W	00b
7:6	**RESERVED**	RO	—
5:2	**EP2_75_eee_sel[3:0]** For k31_pma_phyctrl_eee.v	R/W	0h
1	**ST 2-3-2 enable** 0 = Disable 1 = Enable	R/W	0b
0	**RESERVED**	RO	—

5.3.19 LANE ALIGNMENT PREDICTOR REGISTER

Index (In decimal): EP 2.78 Size: 16 bits

Bits	Description	Type	Default
15:0	**Lane_alignment_Predictor_A/B/C/D**	RO	0000h

5.3.20 OPERATION MODE STRAP OVERRIDE HIGH REGISTER

Index (In decimal): EP 2.81 Size: 16 bits

This register may be used to override the value of the MODE[4:0] configuration straps.

Following an update to this register, a PHY Software Hard Reset (RESET) should be issued in order for the new value to take effect.

Note: When setting a new value, it is the user's responsibility to ensure that conflicting assignments are not made.

Bits	Description	Type	Default
15	**AMDIX_enable** Auto MDIX enable mode 1 = Auto MDIX enabled	R/W	Note 1
14	**EEE_enable** EEE enable/10BASE-T cat5 mode 1 = EEE enabled	R/W	Note 1
13:8	**RESERVED**	RO	—
7	**an_10fh_100fh** 1 = Advertise 10BASE-T and 100BASE-TX full and half duplex only	R/W	Note 1
6	**an_100h** 1 = Advertise 100BASE-TX half duplex only	R/W	Note 1
5	**an_100f** 1 = Advertise 100BASE-TX full duplex only	R/W	Note 1
4	**an_100fh** 1 = Advertise 100BASE-TX full and half duplex only	R/W	Note 1
3	**an_1000f_mp** 1 = Advertise 1000BASE-T full duplex only - multiple port preferred	R/W	Note 1
2	**an_1000f_sp** 1 = Advertise 1000BASE-T full duplex only - single port preferred	R/W	Note 1
1	**an_10fh_100fh_1000f_mp** 1 = Advertise all capabilities except 1000BASE-T half duplex - multiple port preferred	R/W	Note 1
0	**an_10fh_100fh_1000f_sp** 1 = Advertise all capabilities except 1000BASE-T half duplex - single port preferred	R/W	Note 1

Note 1: The default is set by the MODE4, MODE3, MODE2, MODE1, and MODE0 strapping pins as indicated by the corresponding bit in Operation Mode Strap High Register.

5.3.21 OPERATION MODE STRAP HIGH REGISTER

Index (In decimal): EP 2.82 Size: 16 bits

This register indicates the value of the MODE[4:0] configuration straps that were latched into the device at reset.

Bits	Description	Type	Default
15	**Strap_AMDIX_enable** Auto MDIX enable Strap-In Status 1 = Auto MDIX enabled (MODE[4:0] =’10000’ through ‘11111’)	RO	Note 1
14	**Strap_EEE_enable** EEE enable/10BASE-T cat5 Strap-In Status 1 = EEE enabled (MODE[4:0] =’11000’ through ‘11111’)	RO	Note 1
13:8	**RESERVED**	RO	—
7	**Strap_an_10fh_100fh** 1 = Advertise 10BASE-T and 100BASE-TX full and half duplex only (MODE[4:0] =’10111’ and ‘11111’)	RO	Note 1
6	**Strap_an_100h** 1 = Advertise 100BASE-TX half duplex only (MODE[4:0] =’10110’)	RO	Note 1
5	**Strap_an_100f** 1 = Advertise 100BASE-TX full duplex only (MODE[4:0] =’10101’ and ‘11101’)	RO	Note 1
4	**Strap_an_100fh** 1 = Advertise 100BASE-TX full and half duplex only (MODE[4:0] =’10100’ and ‘11100’)	RO	Note 1
3	**Strap_an_1000f_mp** 1 = Advertise 1000BASE-T full duplex only - multiple port preferred (MODE[4:0] =’10011’ and ‘11011’)	RO	Note 1
2	**Strap_an_1000f_sp** 1 = Advertise 1000BASE-T full duplex only - single port preferred (MODE[4:0] =’10010’ and ‘11010’)	RO	Note 1
1	**Strap_an_10fh_100fh_1000f_mp** 1 = Advertise all capabilities except 1000BASE-T half duplex - multiple port preferred (MODE[4:0] =’10001’ and ‘11001’)	RO	Note 1
0	**Strap_an_10fh_100fh_1000f_sp** 1 = Advertise all capabilities except 1000BASE-T half duplex - single port preferred (MODE[4:0] =’10000’ and ‘11000’)	RO	Note 1

Note 1: Set by the MODE4, MODE3, MODE2, MODE1, and MODE0 strapping pins.

5.3.22 LPI MISCELLANEOUS REGISTER

Index (In decimal): EP 2.83 Size: 16 bits

Bits	Description	Type	Default
15:3	**RESERVED**	RO	—
2	**Rx_lpi_req**	RO	—
1	**Tx_lpi_req**	RO	—
0	**Lpi_mode**	RO	—

5.3.23 RX CORRECT COUNTER LOW REGISTER

Index (In decimal): EP 2.84 Size: 16 bits

Bits	Description	Type	Default
15:0	**Correct_cnt[15:0]**	RO/RC	0000h

5.3.24 RX CORRECT COUNTER HIGH REGISTER

Index (In decimal): EP 2.85 Size: 16 bits

Bits	Description	Type	Default
15:0	**Correct_cnt[31:16]**	RO/RC	0000h

5.3.25 RX CRC COUNTER LOW REGISTER

Index (In decimal): EP 2.86 Size: 16 bits

Bits	Description	Type	Default
15:0	**CRC_cnt[15:0]**	RO/RC	0000h

5.3.26 RX CRC COUNTER HIGH REGISTER

Index (In decimal): EP 2.87 Size: 16 bits

Bits	Description	Type	Default
15:0	**CRC_cnt[31:16]**	RO/RC	0000h

5.3.27 RX CORRECT COUNTER HI EXTENDED REGISTER

Index (In decimal): EP 2.88 Size: 16 bits

Bits	Description	Type	Default
15:0	**correct_cnt[47:32]**	RO/RC	0000h

5.3.28 SELF-TEST CORRECT COUNTER HI EXTENDED REGISTER

Index (In decimal): EP 2.89 Size: 16 bits

Bits	Description	Type	Default
15:0	**correct_cnt[15:0]**	RO/RC	0000h

5.3.29 ST2 CORRECT COUNTER LO REGISTER

Index (In decimal): EP 2.92 Size: 16 bits

Bits	Description	Type	Default
15:0	**ST2_correct_cnt[15:0]**	RO	0000h

5.3.30 ST2 CORRECT COUNTER HI REGISTER

Index (In decimal): EP 2.93 Size: 16 bits

Bits	Description	Type	Default
15:0	**ST2_correct_cnt[31:16]**	RO	0000h

5.3.31 ST2 CORRECT COUNTER HI EXTENDED REGISTER

Index (In decimal): EP 2.94 Size: 16 bits

Bits	Description	Type	Default
15:8	**Reserved**	RO	—
7:0	**ST2_correct_cnt[39:32]**	RO	00h

5.3.32 ST2 ERROR COUNTER LO REGISTER

Index (In decimal): EP 2.95 Size: 16 bits

Bits	Description	Type	Default
15:0	**ST2_error_cnt[15:0]**	RO	0000h

5.3.33 ST2 ERROR COUNTER HI REGISTER

Index (In decimal): EP 2.96 Size: 16 bits

Bits	Description	Type	Default
15:0	**ST2_error_cnt[31:16]**	RO	0000h

5.3.34 SRC1 FRAME COUNTER LO REGISTER

Index (In decimal): EP 2.97 Size: 16 bits

Bits	Description	Type	Default
15:0	**SRC1_frame_cnt[15:0]**	RO	0000h

5.3.35 SRC1 FRAME COUNTER HI REGISTER

Index (In decimal): EP 2.98 Size: 16 bits

Bits	Description	Type	Default
15:0	**SRC1_frame_cnt[31:16]**	RO	0000h

5.3.36 SRC1 FRAME COUNTER HI EXTENDED REGISTER

Index (In decimal): EP 2.99 Size: 16 bits

Bits	Description	Type	Default
15:8	**Reserved**	RO	—
7:0	**SRC1_frame_cnt[39:32]**	RO	00h

5.3.37 SRC2 FRAME COUNTER LO REGISTER

Index (In decimal): EP 2.100 Size: 16 bits

Bits	Description	Type	Default
15:0	**SRC2_frame_cnt[15:0]**	RO	0000h

5.3.38 SRC2 FRAME COUNTER HI REGISTER

Index (In decimal): EP 2.101 Size: 16 bits

Bits	Description	Type	Default
15:0	**SRC2_frame_cnt[31:16]**	RO	0000h

5.3.39 SRC2 FRAME COUNTER HI EXTENDED REGISTER

Index (In decimal): EP 2.102 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**SRC2_frame_cnt[39:32]**	RO	00h

5.3.40 SLEEP TIMER COUNTER MASK REGISTER

Index (In decimal): EP 2.103 Size: 16 bits

Bits	Description	Type	Default
15:0	**Slp_cnt_mask[15:0]**	R/W	FE00h

5.3.41 FRAME COUNTER MASK REGISTER

Index (In decimal): EP 2.104 Size: 16 bits

Bits	Description	Type	Default
15:0	**Frame_cnt_mask[15:0]**	R/W	FFC0h

5.3.42 SLEEP COUNTER MINIMUM REGISTER

Index (In decimal): EP 2.105 Size: 16 bits

Bits	Description	Type	Default
15:10	**Reserved**	RO	—
9:0	**Slp_cnt_min[9:0]**	R/W	004h

5.3.43 DES1/SRC1 ADDRESS REGISTER

Index (In decimal): EP 2.106 Size: 16 bits

Bits	Description	Type	Default
15:8	**Des_1_addr[7:0]**	R/W	01h
7:0	**Src_1_addr[7:0]**	R/W	23h

5.3.44 DES2/SRC2 ADDRESS REGISTER

Index (In decimal): EP 2.107 Size: 16 bits

Bits	Description	Type	Default
15:8	**Des_2_addr[7:0]**	R/W	45h
7:0	**Src_2_addr[7:0]**	R/W	67h

5.3.45 WRITE TO CLEAR REGISTER

Index (In decimal): EP 2.108 Size: 16 bits

Bits	Description	Type	Default
15:0	**Write_to_Clear** Write any value to clear Frame Counter registers 97-102 (decimal)	WAC	—

5.3.46 MULTISTREAM CONTROL REGISTER

Index (In decimal): EP 2.109 Size: 16 bits

Bits	Description	Type	Default
15:14	**Reserved**	RO	—
13	**Crs_use_timer** 1 = Use built-in timer 0 = CRS	R/W	1'b0
12	**St_no_lpi** 1 = Disable 0 = State machine sending LPI request	R/W	1'b0
11:10	**Reserved**	RO	—
9	**St2_trig_en** 1 = Enable CRC check of St2_correct_cnt and St2_error_cnt 0 = Disable check	R/W	1'b0
8	**St1_trig_en** 1 = Enable CRC check of St1_correct_cnt and St1_error_cnt 0 = Disable check	R/W	1'b0
7:5	**Reserved**	RO	—
4	**Ipef_en** 1 = Enable ipef pattern 0 = Disable	R/W	1'b0
3:1	**Reserved**	RO	—
0	**St_multi_stream_en** 1 = Enable 0 = Disable	R/W	1'b0

5.3.47 MULTISTREAM START REGISTER

Index (In decimal): EP 2.110 Size: 16 bits

Bits	Description	Type	Default
15:1	**Reserved**	RO	—
0	**St_frame_ctrl_en** 1 = Start multistream packet generation engine 0 = Stop multistream packet generation engine	R/W	1'b0

5.4 Extended Page 3 Registers

5.4.1 PCS CONTROL 1 REGISTER

Index (In decimal): EP 3.0 Size: 16 bits

Bits	Description	Type	Default
15:13	**RESERVED**	RO	—
12	**EEE100_idle_sel** 0 = 9031 1 = 8050	R/W	0b
11:10	**RESERVED**	RO	—
9:7	**TX FIFO threshold [2:0]**	R/W	111b
6:1	**RESERVED**	RO	—
0	**Dbg_pcs100_sel** 1 = Select eee100 RX signals 0 = Original	R/W	0b

5.4.2 EEE QUIET TIMER REGISTER

Index (In decimal): EP 3.8 Size: 16 bits

Bits	Description	Type	Default
15:0	**Quiet-Timer[15:0]** 1G-EEE quieter Timer Max Value	R/W	006Eh

5.4.3 EEE UPDATE TIMER REGISTER

Index (In decimal): EP 3.9 Size: 16 bits

Bits	Description	Type	Default
15:0	**Update-Timer[15:0]** 1G-EEE Update Timer Max Value	R/W	005Fh

5.4.4 EEE LINK-FAIL TIMER REGISTER

Index (In decimal): EP 3.10 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**Link-Fail-Timer[7:0]1G-EEE Link-Fail Timer Max Value**	R/W	5Ah

5.4.5 EEE POST-UPDATE TIMER REGISTER

Index (In decimal): EP 3.11 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**Post-Update-Timer[7:0]** 1G-EEE Post-Update Timer Max Value	R/W	50h

5.4.6 EEE WAITWQ TIMER REGISTER

Index (In decimal): EP 3.12 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**WaitWQ-Timer[7:0]** 1G-EEE WaitWQ Timer Max Value	R/W	5Bh

5.4.7 EEE WAKE TIMER REGISTER

Index (In decimal): EP 3.13 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**Wake-Timer[7:0]** 1G-EEE Wake Timer Max Value	R/W	89h

5.4.8 EEE WAKETX TIMER REGISTER

Index (In decimal): EP 3.14 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**WakeTX-Timer[7:0]** 1G-EEE WakeTX Timer Max Value	R/W	21h

5.4.9 EEE WAKEMZ TIMER REGISTER

Index (In decimal): EP 3.15 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**WakeMz-Timer[7:0]** 1G-EEE WakeMz Timer Max Value	R/W	6Eh

5.5 Extended Page 7 Registers

5.5.1 EP7 REGISTER 58

Index (In decimal): EP 7.58 Size: 16 bits

Bits	Description	Type	Default
15	**Register 4 RW Enable** This bit addresses a UNH Compliance issue with Direct Register 4 bits 9 and 12. 0 = Register 4 bits 9 and 12 are Read-Only (Normal) 1 = Register 4 bits 9 and 12 are Read/Write (UNH)	R/W	0b
14:0	**RESERVED**	RO	—

5.5.2 EP7 REGISTER 59

Index (In decimal): EP 7.59 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	RO	0b
14:9	**GIG AN RX Next Page Addon Options [5:0]** These bits are to revert various RX Next Page bug fixes (chicken bits) 0 = Bug fix enabled 1 = Bug fix disabled	R/W	00h
8	**GIG AN TX Next Page Addon Options** These bits are to revert various TX Next Page bug fixes (chicken bits) 0 = Bug fix enabled 1 = Bug fix disabled	R/W	0b
7	**Read on Clear Revert** This bit reverts the read on clear bug fix (chicken bit) 0 = Bug fix enabled 1 = Bug fix disabled	R/W	0b
6	**MDC Clock Rate Margin** This bit reverts the bypassing of one stage of flip flops on the read data (chicken bit) 0 = One stage of flip flops is bypassed 1 = One stage of flip flops is restored	R/W	0b
5	**Fix Arb_PF Clear on Reg4 Access** chicken bit 0 = Bug fix enabled. Direct Register 4 access has no effect on internal flag 1 = Bug fix disabled. Direct Register 4 access clears internal flag	R/W	0b
4:3	**RESERVED**	RO	00b
2	**Register 0 RW Enable** This bit addresses a UNH Compliance issue with Direct Register 0 bits 6 and 13. 0 = Register 0 bits 6 and 13 cannot set set to 2'b11 (Normal) 1 = Register 0 bits 6 and 13 can be set to 2'b11 (UNH)	R/W	0b
1:0	**GIG AN TX Next Page Addon Options [1:0]** These bits are to revert various TX Next Page bug fixes (chicken bits) 0 = Bug fix enabled 1 = Bug fix disabled	R/W	00b

5.5.3 EEE LINK PARTNER ABILITY OVERRIDE REGISTER

Index (In decimal): EP 7.62 Size: 16 bits

Bits	Description	Type	Default
15	**LP AN Override** 0 = Use Link partner AN results 1 = Use bits 10:0 as Link partner results	R/W	0b
14	**LP Force 100 FD Override** Per 802.3 when Link Partner is set to Force 100 and this device has been advertising HD and FD support, this device will select 100 HD due to parallel detect. If this device has not been advertising HD, the result will be PD fault. This bit provides a proprietary override so this device will select 100 FD in this case 0 = Standard operation, this device operates according to 802.3 1 = Proprietary operation, this device selects 100 FD when the Link Partner is set to Force 100 and this device has been advertising FD. If this device has not been advertising FD, the result will be PD fault.	R/W	0b
13:11	**RESERVED**	RO	—
10	**100GBASE-CR10 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 100GBASE-CR10. 1 = Link partner advertises EEE deep sleep capability for 100GBASE-CR10. **Note:** This device does not support this mode.	R/W	0b
9	**RESERVED**	RO	—
8	**40GBASE-CR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-CR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-CR4. **Note:** This device does not support this mode.	R/W	0b
7	**40GBASE-KR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-KR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-KR4. **Note:** This device does not support this mode.	R/W	0b
6	**10GBASE-KR EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KR. 1 = Link partner advertises EEE capability for 10GBASE-KR. **Note:** This device does not support this mode.	R/W	0b
5	**10GBASE-KX4 EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX4. 1 = Link partner advertises EEE capability for 10GBASE-KX4. **Note:** This device does not support this mode.	R/W	0b
4	**10GBASE-KX EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX. 1 = Link partner advertises EEE capability for 10GBASE-KX. **Note:** This device does not support this mode.	R/W	0b

Bits	Description	Type	Default
3	**10GBASE-T EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-T. 1 = Link partner advertises EEE capability for 10GBASE-T. **Note:** This device does not support this mode.	R/W	0b
2	**1000BASE-T EEE** 0 = Link partner does not advertise EEE capability for 1000BASE-T. 1 = Link partner advertises EEE capability for 1000BASE-T.	R/W	0b
1	**100BASE-TX EEE** 0 = Link partner does not advertise EEE capability for 100BASE-TX. 1 = Link partner advertises EEE capability for 100BASE-TX.	R/W	0b
0	**RESERVED**	RO	—

5.5.4 EEE MESSAGE CODE REGISTER

Index (In decimal): EP 7.63 Size: 16 bits

Bits	Description	Type	Default
15:11	**RESERVED**	RO	—
10:0	**EEE_message_code[10:0]** Programmable EEE specific message code for AN	R/W	00Ah

5.6 Extended Page 28 Registers

5.6.1 ANALOG CONTROL REGISTER 4

Index (In decimal): EP 28.4 Size: 16 bits

Bits	Description	Type	Default
15	**dgt1_tx_hii** Increase TX preamp bias current by 25%. 0 = Normal bias condition 1 = Bias increased by 25%	R/W	0b
14	**dgt1_dis_pas** 1 = Turn off passive termination at power-down mode	R/W	0b
13:10	**dgt1_v1gc[3:0]** TX driver mirror ratio	R/W	0h
9:8	**dgt1_vf_ctrl[1:0]** TX driver floating A/B bias control	R/W	00b
7:4	**dgt1_amp_10bt[3:0]** TX amplitude control for 10BT mode	R/W	0h
3:0	**dgt1_amp_100bt[3:0]** TX amplitude control for 100BT/1000BT modes	R/W	0h

5.6.2 ANALOG CONTROL REGISTER 8

Index (In decimal): EP 28.8 Size: 16 bits

Bits	Description	Type	Default
15	**EDPD low power** Indicates the link is in low power.	RO	0b
14:12	**EDPD Wire Pair Selection [2:0]** For cable diagnostic purposes, this field selects which wire pairs are monitored when EDPD is enabled and the speed forced to 1000 Mbps. 0xx = Pairs A, B, C and D (normal operation) 100 = Pair A 101 = Pair B 110 = Pair C 111 = Pair D	R/W	000b
11	**RESERVED**	R/W	0b
10	**exADCtest** when asserted, ch. A/C/D input 3 by pad input	R/W	0b
9:6	**TstPtSel[3:0]** one out of 15 pairs test points are selected to be monitored from ISET and LDO pins	R/W	0h
5:4	**BTRX trim [1:0]** Trim BTRX comparator threshold HIPLS, HIPLS2 threshold 00 = 400 mV, 200 mV 01 = 433 mV, 216 mV 10 = 466 mV, 233 mV 11 = 500 mV, 250 mV	R/W	00b
3	**BTRX LPF on** Turn on BTRX LPF to enhance 10BT immunity	R/W	0b
2	**ADCtestINL** unused	R/W	0b
1	**dgt_add_dly** Add clock delay to the ADC error correction logic clock.	R/W	0b
0	**ADCTEST1** choose 3rd input pair for ADC	R/W	0b

5.6.3 AFED CONTROL REGISTER

Index (In decimal): EP 28.9 Size: 16 bits

Bits	Description	Type	Default
15	**rd_block_en** 1 = Enable 0 = Disable	R/W	1b
14:12	**rd_block_cnt[2:0]** 110 = 4 µs 111 = 4.5 µs 100 = 2.56 µs	R/W	110b
11:10	**RESERVED**	RO	—
9	**p_cat3** 0 = cat5 parameter for 10 BASE-T TX 1 = cat3 parameter for 10 BASE-T TX	R/W	Note 1
8	**RESERVED**	RO	—
7	**disPR** Disable partial respond	R/W	0b
6	**bypass_nrzi** Bypass NRZI transform	R/W	0b
5:4	**sdstret_sel[1:0]**	R/W	01b
3:2	**sdext_sel[1:0]** Extension on signal detect from analog 00 = 3 µs 01 = 4 µs (default) 10 = 5 µs 11 = 6 µs	R/W	01b
1	**dis_powersave** Disable digital power save feature 1 = All AFE modules power on 0 = Power save depends on mode (default)	R/W	0b
0	**P_TX_Flip** Reverse the polarity of 10BASE-T TX signal	R/W	0b

Note 1: The default is set by the values of the EEE enable bit in the Operation Mode Strap Override High Register.

5.6.4 POWER MANAGEMENT MODE REGISTERS

Index (In decimal): EP 28.16-33 Size: 16 bits

These registers specify the power enables for each operating mode of the device.

Registers	Bits	Description	Type	Default
16	15:0	**Power Management Mode 0**	R/W	FFFFh
17	15:0	**Power Management Mode 1**	R/W	FFFFh
18	15:0	**Power Management Mode 2**	R/W	0000h
19	15:0	**Power Management Mode 3**	R/W	6EFFh
20	15:0	**Power Management Mode 4**	R/W	E6FFh
21	15:0	**Power Management Mode 5**	R/W	6EFFh
22	15:0	**Power Management Mode 6**	R/W	E6FFh
23	15:0	**Power Management Mode 7**	R/W	00FFh
24	15:0	**Power Management Mode 8**	R/W	43FFh
25	15:0	**Power Management Mode 9**	R/W	43FFh
26	15:0	**Power Management Mode 10**	R/W	67FFh
27	15:0	**Power Management Mode 11**	R/W	07FFh
28	15:0	**Power Management Mode 12**	R/W	07FFh
29	15:0	**Power Management Mode 13**	R/W	67FFh
30	15:0	**Power Management Mode 14**	R/W	67FFh
31	15:0	**Power Management Mode 15**	R/W	0000h
32	15:0	**Power Management Mode 16 (master)**	R/W	6666h
33	15:0	**Power Management Mode 16 (slave)**	R/W	6666h

5.6.5 EDPD CONTROL REGISTER

Index (In decimal): EP 28.36 Size: 16 bits

Bits	Description	Type	Default
15	**Lpf from DSP disable**	R/W	0b
14:6	**RESERVED**	RO	—
5:4	**p_edpd_mask_timer[1:0]** 00 = EDPD mask for 2.6 µs 01 = 3.2 µs 10 = 4.0 µs 11 = 5.0 µs	R/W	00b
3:2	**p_edpd_timer[1:0]** 00 = EDPD pulse separation for 1s 01 = 1.3s 10 = 1.6s 11 = 1.9s	R/W	00b
1	**p_EDPD_random_dis** 1 = Use edpd_timer value as EDPD pulse separation selection 0 = Use random seed value as EDPD pulse separation selection	R/W	0b
0	**p_edpd_en** 0 = EDPD mode disabled 1 = EDPD mode enabled	R/W	0b

5.7 Extended Page 29 Registers

Note:	Register values in this Extended Page 29 (EP29) are **not** reset by mr0 bit 15.

5.7.1 ANALOG CONTROL REGISTER 1

Index (In decimal): EP 29.1 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**ISET_R_SEL** select ISET resistor 1 = On-chip 0 = External	R/W	0b
13	**enXTALb** XTAL OSC enable_bar 0 = XTAL on 1 = Turn off	R/W	0b
12:8	**RESERVED**	RO	—
7	**PLL prop gain** proportional path current gain h, h0 combine with EP 29.13 <15:13>	R/W	0b
6:5	**PLL trim f[1:0]** PLL trim f bits	R/W	00b
4	**PLL Rp control** Select Rp resistance value 0 = 4k 1 = 2k	R/W	0b
3	**PLL div10** Enable PLL divided-by-10 on feedback	R/W	0b
2:0	**PLL LDO control[2:0]** Select LDO reference level 000 = 1.146V 001 = 1.097V 010 = 1.048V 011 = 0.998V 100 = 1.194V 101 = 1.242V 110 = 1.29V 111 = 1.337V	R/W	000b

5.7.2 ANALOG CONTROL REGISTER 11

Index (In decimal): EP 29.14 Size: 16 bits

Bits	Description	Type	Default
15	**LDO enable** turn off VDD regulator by software 1 = Off 0 = On	R/W	0b
14:12	**LDO reference tune[2:0]** Tune LDO output voltage @Iload = 200 mA 000 = 1.10V 001 = 1.14V 010 = 1.18V 011 = 1.22V 100 = 1.26V 101 = 1.30V 110 = 1.34V 111 = 1.39V	R/W	000b
11	**SWREF** 1 = Change LDO reference to local	R/W	0b
10	**Sel_low_freq** 0 = phy_xtalclk = 25 MHz from crystal 1 = phy_xtalclk = clk from slow osc	R/W	0b
9	**dis_detVDDAH** 1 = dis_detVDDAH	R/W	0b
8	**VDDAHsel** once dis_detVDDAH = 1, set VDDAHsel = 1 for 2.5V, VDDAHsel = 0 for 3.3V	R/W	0b
7:0	**RESERVED**	RO	—

5.7.3 EP29 REGISTER 56

Index (In decimal): EP 29.56 Size: 16 bits

Bits	Description	Type	Default
15	**Xtal_amp_ow**	R/W	0b
14:12	**RESERVED**	RO	—
11:8	**Xtal_amp_time_step[3:0]**	R/W	0001b
7:5	**Xtal_amp_ow_dinv[2:0]**	R/W	111b
4:0	**Xtal_amp_ow_dgm[4:0]**	R/W	00000b

5.7.4 EP29 REGISTER 57

Index (In decimal): EP 29.57 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:5	**Xtal_amp_ninv[2:0]**	RO	Note 1
4:0	**Xtal_amp_ngm[4:0]**	RO	Note 1

Note 1: The value reflects the current crystal amplifier operation and has no given default.

5.7.5 EP29 REGISTER 58

Index (In decimal): EP 29.58 Size: 16 bits

Bits	Description	Type	Default
15:12	**rcal_value_tx[3:0]**	RO	Note 1
11	**RESERVED**	RO	—
10	**rcal_1st_run**	RO	Note 1
9	**rcal_good_tx**	RO	Note 1
8	**rcal_done_tx**	RO	Note 1
7:4	**tx_rterm_ctrl[3:0]**	R/W	Note 1
3:0	**Tx_rterm_offset[3:0]**	RO	0000b

Note 1: The value depends on the calibration result and has no given default.

5.7.6 EP29 REGISTER 59

Index (In decimal): EP 29.59 Size: 16 bits

Bits	Description	Type	Default
15:12	**rcal_value_rx[3:0]**	RO	Note 1
11	**RESERVED**	RO	—
10	**rcal_1st_run**	RO	Note 1
9	**rcal_good_rx**	RO	Note 1
8	**rcal_done_rx**	RO	Note 1
7:4	**rx_rterm_ctrl[3:0]**	R/W	Note 1
3:0	**Rx_rterm_offset[3:0]**	RO	0000b

Note 1: The value depends on the calibration result and has no given default.

5.7.7 EP29 REGISTER 60

Index (In decimal): EP 29.60 Size: 16 bits

Bits	Description	Type	Default
15:0	**rcal_raw_tx[15:0]**	RO	Note 1

Note 1: The value depends on the calibration result and has no given default.

5.7.8 EP29 REGISTER 61

Index (In decimal): EP 29.61 Size: 16 bits

Bits	Description	Type	Default
15:0	**rcal_raw_rx[15:0]**	RO	Note 1

Note 1: The value depends on the calibration result and has no given default.

5.7.9 EP 29 REGISTER 63

Index (In decimal): EP 29.63 Size: 16 bits

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Rterm_calibration_restart_toggle** Write a 1 to toggle the value of this field.	R/W	0b

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004286B (06-27-22)	Misc.	• Updated 14:12 field in Analog Control Register 11. • Updated 2:0 field in Analog Control Register 1. • Updated Operation Mode Strap Override Low Register to add bit 14 definition. • Updated EP2 Register 75 to add bits 13, 12, 1, 0 definitions and updated bits 10, 5:2 definitions. • Updated Lane Alignment Predictor Register definition. • Added note to PCS Loop-back Swap/Polarity Control Register bit 9 related to enabling high-speed MDIO operation. • Corrected typo in EP2 Register 75 default column of EP2_75_eee_sel[3:0].
DS00004286A (11-01-21)	Initial release	

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