Application Note

Designing a Copper SFP using the VSC8221 10/100 /1000BASE-T PHY

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Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 was published in March 2005.

1.2 Revision 1.0

Revision 1.0 was the first release of this document. It was published in February 2005.

2 Introduction

In addition to a detailed description of the use of the VSC8221 10/100/1000BASE-T PHY for designing a copper SFP, this document also provides a brief description of different SFP types.

This is not a standalone document and references the VSC8221 Datasheet and the VSC8221HHEV Copper SFP Reference Design Kit.

In order to better understand this document it is recommended that the 'SFP MSA' and the 'Serial-GMII' specifications mentioned in the 'References' section be read before further reading this document.

2.1 Audience

The audience for this document is customers engaged in the design of copper SFPs or field application engineers, marketing and sales involved support and design of VSC8221 based copper SFPs.

2.2 References

Small Form-Factor Pluggable (SFP) Transceiver MultiSource Agreement (MSA)

This document describes a common specification for the Small Formfactor Pluggable (SFP) Transceivers developed by the Multiple Source Agreement (MSA) group. The MSA group is a group of companies that are engaged in the development of swappable optical interface for SONET/SDH, Fibre Channel, Gigabit Ethernet, and other applications. This document is an internal working document of the SFF Committee, an industry ad hoc group.

Serial-GMII (SGMII) Specification

This is a MAC-copper PHY interface specification developed by CISCO Systems that allows 10, 100, or 1000BASE-T communication over a copper cable. The signaling between the MAC and the PHY is always 1.25 GHz, 8b/10b encoded, irrespective of the link speed on the copper media. This MAC interface is a slight variant of the 1000BASE-X interface described in Clause 36 and Clause 37 of the IEEE802.3 specification.

Please contact your Vitesse Semiconductor representative for a copy of this specification.

IEEE 802.3 Specification

Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications.

VSC8221HHEV Reference Design Kit

This reference design kit contains the schematics, layout files, BOM, and user guide of a VSC8221PHY based copper SFP.

This design kit can be found on your Vitesse Semiconductor documentation website.

VSC8221 Datasheet

This document can be found on your Vitesse Semiconductor documentation website.

'Copper SFP PHY Performance Comparison' White paper

This document can be found on your Vitesse Semiconductor documentation website.

2.3 Terms and Abbreviations

- **SFP**: Small FormFactor Pluggable.
- **VSC8221**: Vitesse's single port 10/100/1000BASE-T PHY for Copper SFP applications.

- **MSA**: Multi-Source Agreement.
- **1000BASE-X**: 8b/10b encoded 1.25 Gbps differential signals compliant with Clause 36 and Clause 37 of the IEEE802.3 physical layer specification.
- **SerDes**: Serializer-Deserializer.
- **PHY**: Physical Layer transceiver. In this document, this is mainly used to refer to a copper 10/100 /1000BASE-T transceiver.
- **PCS**: Physical coding sublayer. The block inside the transceiver that converts the raw data to a format suitable for transmission over the physical media and vice-versa. For example, for a fiber optic media the 8 bit raw data is converted to 10 bit encoded data for transmission over the Media and therefore the PCS block is a 8b/10b converter. In case copper media, the 8bit data is converted to a 5-PAM (Pulse Amplitude Modulated) signal and therefore the PCS is 8b/5 PAM converter.
- **SGMII**: 1.25 GHz MAC-copper PHY Interface defined by CISCO systems.
- **802.3z SerDes**: Same as 1000BASE-X.
- **Clause 37 Autonegotiation**: The in-band auto-negotiation that occurs between the MAC and PHY over the SFP interface in order to establish a link.
- **Clause 28 Autonegotiation**: The auto-negotiation that occurs between two 10/100/1000BASE-T PHYs in order to establish a link over the copper media.
- **CAT5 Media**: CAT5 copper cable used for Ethernet connections with RJ45 connectors at either end.
- **Copper Media**: Same as CAT5 media.
- **Fiber Optic Media**: Multimode or single mode Fiber optic cable used for Ethernet connections.

Note: For the purposes of this document, the term "1000BASE-X" and "802.3z SerDes" are synonymous and have been used interchangeably.

3 SFP System Overview

Pluggable interfaces are small, hot-swappable, managed port interface modules that provide physical layer (copper or fiber) signaling for data, voice, storage and video transport networks.

The first implementations of pluggable interfaces of Ethernet started with Gigabit Interface Converter (GBIC) modules, which allowed Gigabit Ethernet devices to provide a generic, modular interface to optical transceivers. This capability allowed optical transceivers of various distances (10 km or 80 km for example) to be plugged into a switch-card slot without modifications to the card.

In the year 2000, the GBIC was upgraded to Small FormFactor Pluggable (SFP). SFP optical interfaces are less than ½ the size of GBIC interfaces. A SFP module can support various kinds of technologies such as Asynchronous Transfer Mode (ATM), FDDI, Fiber Channel, Fast Ethernet and Gigabit Ethernet, and Synchronous Optical Network (SONET)/Synchronous Digital Hierarchy (SDH) applications at speeds up to 2.5 Gbps full-duplex. The design requirements of a Fiber Optic SFP are mentioned in the SFP MSA specification.

The data throughput of a 1.25 Gbps Fiber Optic SFP is 1 Gbps since the data is actually 8b/10b encoded for transmission over the Fiber Optic media. This kind of an optical SFP is used in a Gigabit Ethernet network.

With the development of low-power transceivers such as the VSC8221 that can transmit Ethernet data at 1 Gbps over CAT5 cable, it is now possible to develop Gigabit Ethernet SFPs for the copper media.

Furthermore, CISCO has developed a MAC Interface protocol called the SGMII protocol, that enables data transfer at 10 Mbps and 100 Mbps (in addition to 1000 Mbps) on the CAT5 copper cable, while maintaining the signaling rate between the MAC and the PHY on the SFP at 1.25 GHz. The SGMII protocol is very similar to the 1000BASE-X protocol for fiber optic media defined in Clause 36 and Clause 37 of the IEEE 802.3 specification.

This enabled the design of Copper SFPs that will inter-operate with legacy 10/100BASE-T copper PHYs in addition to newer 1000BASE-T PHYs while using same 1.25GHz SerDes blocks in the MACs and PHYs for all three speeds.

3.1 Different Kinds of SFPs

3.1.1 Legacy 1000BASE-X Fiber Optic SFP

The following block diagram shows a legacy 1000BASE-X Fiber Optic SFP.

Figure 1 • 1000BASE-X Fiber Optic Gigabit Ethernet SFP
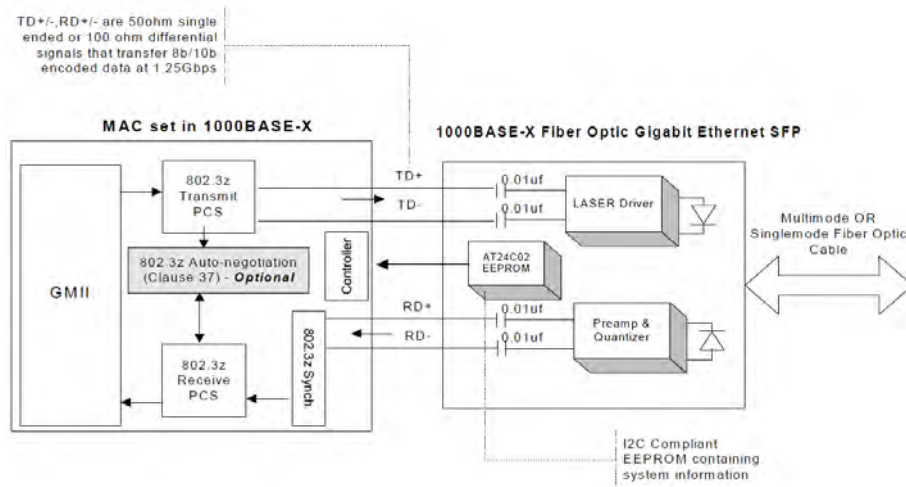
As seen in the previous figure, a fiber optic SFP is nothing but an electrical to optical signal converter and vice-versa. It does not perform any kind of data manipulation.

In a fiber optic SFP, the communication is between a local MAC and a link partner MAC. Unlike the copper PHYs, the 8b/10b encoding/decoding physical coding sublayer (PCS) blocks for the fiber media are part of the MAC ICs.

A 1000BASE-X MAC can operate with auto-negotiation or without auto-negotiation. It should be noted that a MAC with 1000BASE-X auto-negotiation can only interoperate with a MAC with 1000BASE-X auto-negotiation. Similarly, a MAC without 1000BASE-X auto-negotiation can only interoperate with a MAC without 1000BASE-X auto-negotiation.

The EEPROMs used in these systems are I2C-compliant 2-wire EEPROMs like Atmel's AT24 series. They have a page address of '0' and are either 128 or 256 bytes in size.

The contents in the EEPROM are vendor specific and follow the guidelines mentioned in Appendix B4 of the SFP MSA specification.

## 3.1.2   1000BASE-T Copper SFP with 1000BASE-X MAC Interface

The block diagram below shows a 1000BASE-T copper SFP with 1000BASE-X Interface. This kind of SFP for CAT5 copper media cable can be used in systems designed to support 1000BASE-X fiber optic SFPs.

As far as the MAC is concerned, it is driving a fiber optic SFP. The VSC8221 PHY in the copper SFP handles the 1000BASE-X to 1000BASE-T data translation in both transmit and receive directions.

In the transmit path, the PHY performs 10b/8b decoding of the 10b encoded data received from the 1000BASE-X interface of the MAC over the TD+/TD- pins. This decoded 8b data is now converted to 4 parallel channels (for 4 twisted pairs of the CAT5 cable) of PAM-5 encoded symbols at a symbol rate of 125 MHz, giving a total throughput of 1000 Mbps.

In the receive path, the PHY performs 1000BASE-T PAM-5 to 8b decoding. This decoded 8b data is again encoded using the 8b/10b encoder block (Transmit PCS) of the PHY. This 1.25 GHz 1000BASE-X format 10b encoded data is sent to the MAC over the RD+/RD- pins of the 1000BASE-X MAC interface.

Figure 2 • 1000BASE-T Copper SFP with 1000BASE-X MAC Interface
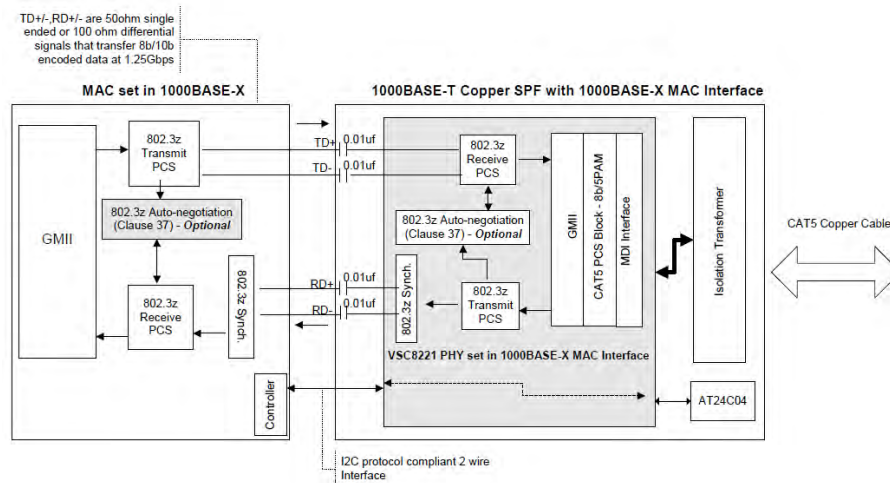
These SFPs are used in systems where the distance between the Local SFP and the link partner is less than 100 m. This saves system cost because CAT5 copper cable is cheaper than fiber optic cable.

The EEPROMs used in these SFPs are I2C-compliant 2-wire EEPROMs like Atmel's AT24 series. They must have a page address of '0' and must be of size 512 bytes or greater.

Address locations 0 through 255 are reserved for vendor-specific data and must follow the guidelines mentioned in Appendix B4 of the SFP MSA specification.

The contents in EEPROM locations 256 through 511 are specific to the Vitesse VS8221 10/100 /1000BASE-T PHY. The PHY uses this data to initialize itself during startup.The contents are mentioned in section Default PHY Initialization and must be copied to the EEPROM without any changes.

It should be noted that a Copper SFP can be set to operate in one of the following operating modes:

- 1000BASE-X MAC Interface Auto-negotiation enabled mode also called Clause 37 auto-negotiation enabled mode.
- 1000BASE-X MAC Interface Auto-negotiation disabled mode also called Clause 37 auto-negotiation disabled mode.

The MAC Interface must also be in the same auto-negotiation state (enable or disabled) as the PHY in the copper SFP for the system link to successfully transfer data. This will be described further in the following sections.

3.1.3   10/100/1000BASE-T Copper SFP with SGMII MAC Interface

The following block diagram shows a 10/100/1000BASE-T copper SFP with SGMII Interface. This kind of SFP for CAT5 copper media cable is used in newer systems that support the SGMII MAC Interface. It is recommended that the SFP's default operating mode not be a SGMII MAC Interface mode if there is any likelihood of the SFP being used in a legacy system that supports only the 1000BASE-X Interface.

These SFPs are used in systems where the distance between the Local SFP and the link partner is less than 100 m. This saves system cost because CAT5 copper cable is cheaper than fiber optic cable.

Figure 3 • 10/100/1000BASE-T Copper SFP with SGMII MAC Interface
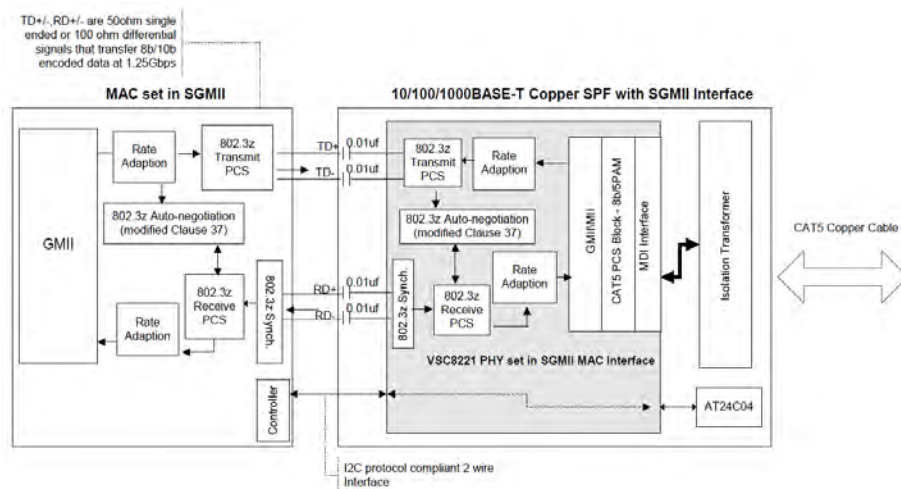
The EEPROMs used in these SFPs are I2C-compliant 2-wire EEPROMs like the Atmel AT24 series. They must have a page address of '0' and must be of size 512 bytes or greater.

Address locations 0 through 255 are reserved for vendor-specific data and must follow the guidelines mentioned in Appendix B4 of the SFP MSA specification.

The contents in EEPROM locations 256 through 511 are specific to the Vitesse VS8221 10/100 /1000BASE-T PHY. The PHY uses this data to initialize itself during startup. The contents are mentioned in section Default PHY Initialization and must be copied to the EEPROM without any changes.

It should be noted that the 1000BASE-T only and the 10/100/1000BASE-T SFPs are exactly the same in terms of schematic, layout, and the SFP mechanical dimensions. The only difference between the two is the VSC8221 PHY's operating mode.

The default operating mode can be setup by using different initialization for 1000BASE-T only SFP and the 10/100/1000BASE-T SFP in the EEPROM of the SFP, or by writing to the PHY registers via the I2C compliant interface after startup. This is described in greater detail in section Copper SFP Configuration.

It should be noted that a triple speed (SGMII) copper SFP can be set to operate in one of the following operating modes:

- SGMII MAC Interface Auto-negotiation enabled mode also called Modified Clause 37 auto-negotiation enabled mode.
- SGMII MAC Interface Auto-negotiation disabled mode also called Modified Clause 37 auto-negotiation disabled mode.

The MAC Interface must also be in the same auto-negotiation state (enable or disabled) as the PHY in the copper SFP for the system link to successfully transfer data. This will be described further in the following sections.

3.2 MAC Interfaces for Gigabit Ethernet SFPs

The MAC interfaces for Gigabit Ethernet SFPs can be in one of the following 4 modes. The SGMII Interface modes are applicable to copper SFPs only whereas the 1000BASE-X operating modes can be used with either fiber optic or copper SFPs.
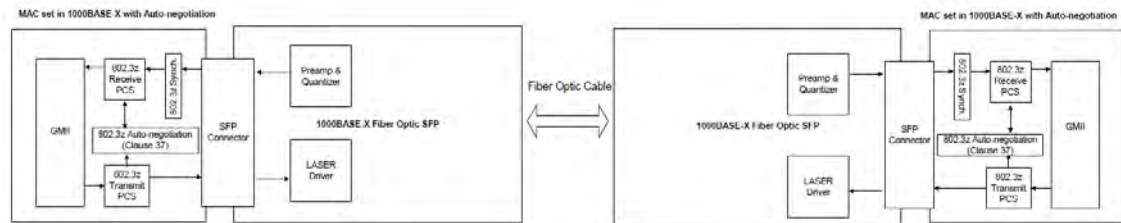
- 1000BASE-X with auto-negotiation
- 1000BASE-X without auto-negotiation
- SGMII with auto-negotiation
- SGMII without auto-negotiation

3.2.1   1000BASE-X with Auto-negotiation

The following block diagrams show the typical system implementations with MAC Interface set in this mode. It should be noted that only the two system implementations shown in this section will be able to successfully transfer bi-directional Gigabit traffic.

The System Scenario A block diagram shows the typical system implementation with MAC interface set as '1000BASE-X with Auto-negotiation'. As shown, the 1000BASE-X Auto-negotiation of both the local MAC and the link Partner MAC must be enabled.

Figure 4 • System Scenario A

The System Scenario B block diagram shows the typical system implementation with MAC interface set as '1000BASE-X with Auto-negotiation'. As shown, the 1000BASE-X Auto-negotiation of both the local MAC and the local PHY must be enabled.

Figure 5 • System Scenario B

3.2.2   1000BASE-X without Auto-negotiation

The following block diagrams show the typical system implementations with MAC Interface set in this mode. It should be noted that only the two system implementations shown in this section will be able to successfully transfer bi-directional Gigabit traffic.
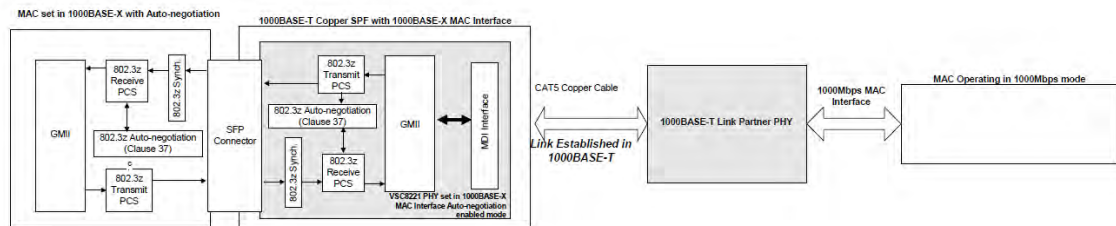
The System Scenario A block diagram shows the typical system implementation with MAC interface set as '1000BASE-X without Auto-negotiation'. As shown, the 1000BASE-X Auto-negotiation of both the local MAC and the link Partner MAC must be disabled.

Figure 6 • System Scenario A

The System Scenario B block diagram shows the typical system implementation with MAC interface set as '1000BASE-X without Auto-negotiation'. As shown, the 1000BASE-X Auto-negotiation of both the local MAC and the local PHY must be disabled.
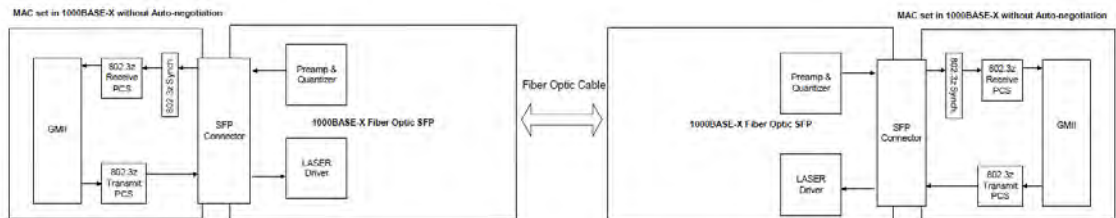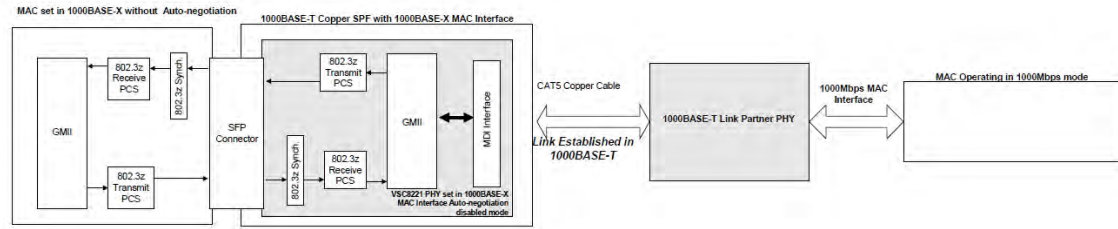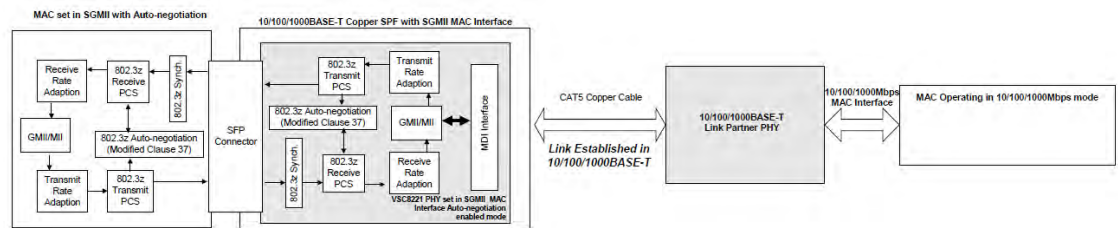
Figure 7 • System Scenario B

3.2.3 SGMII with Auto-negotiation

The System Scenario A block diagram shows the typical system implementation with MAC Interface set as 'SGMII with Auto-negotiation'. As shown, the SGMII Interface Auto-negotiation of both the local MAC and the local PHY must be enabled.

Figure 8 • System Scenario A

It should be noted that only the system implementation shown in this section will be able to successfully transfer bi-directional 10,100 or 1000 Mbps traffic.

Fiber optic SFPs cannot be used in SFP ports when the MAC is set in SGMII Interface mode.

3.2.4 SGMII without Auto-negotiation

This is not a standard operating mode. In this mode the MAC is not able to find out the link configuration i.e. link status, speed, duplex and flow control settings through the in-band auto-negotiation process between the MAC and PHY. Inband auto-negotiation means that auto-negotiation takes place over the data lines of the MAC-copper PHY interface, that is, over the TD+/TD- and RD+/RD-pins.

In order to configure the internal settings such as the rate adaption block setting or flow control setting, the MAC must know the link configuration of the SFP. Since in-band auto-negotiation is not enabled the MAC must query the PHY registers using the I2C-compliant interface using the MOD_DEF2 and MOD_DEF1 pins.

Refer to section Operating Mode 6 - SGMII SerDes to CAT5 Media, with Modified Clause 37 Autonegotiation Disabled on how to find the link configuration information from the PHY.

The System Scenario A block diagram shows the typical system implementation with MAC Interface set as 'SGMII without Auto-negotiation'. As shown, the SGMII Interface Auto-negotiation of both the local MAC and the local PHY must be disabled.

Figure 9 • System Scenario A
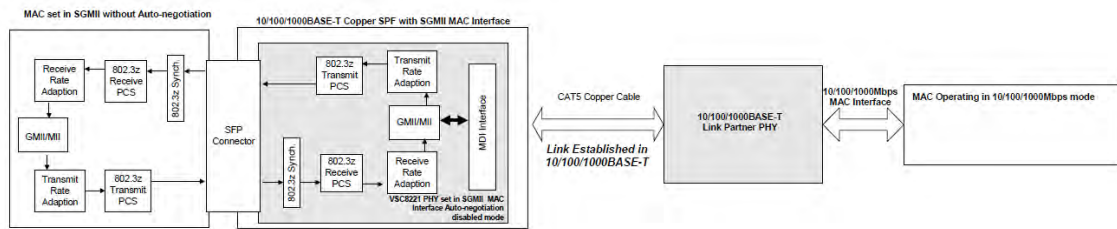
It should be noted that only the system implementation shown in this section will be able to successfully transfer bi-directional 10,100 or 1000 Mbps traffic.

Since this is a non-standard operating mode, it is unlikely that any MAC Interface of a switch system will operate in this mode.

Fiber optic SFPs cannot be used in SFP ports when the MAC is set in SGMII Interface mode.

4 Designing a Copper SFP Using the VSC8221 10/100/1000BASE-T PHY
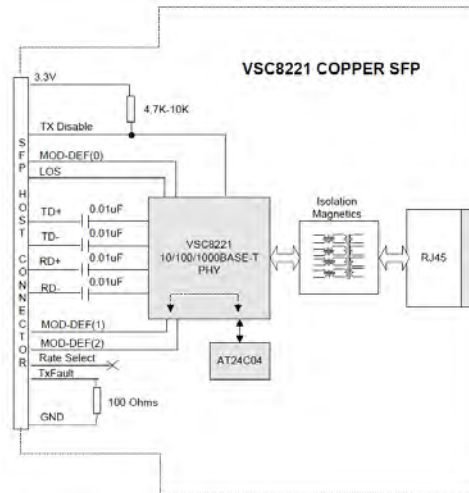
Irrespective of whether a copper SFP is 1000BASE-T only (with 1000BASE-X MAC Interface) or a 10/100/1000BASET triple speed SFP (with SGMII MAC Interface) the electrical schematics of the SFP are the same, that is, they are identical in all respects.

The following block diagram shows the copper SFP.

Figure 10 • Copper SFP Block Diagram

4.1 Important Design Considerations

- In a fiber optic SFP, the EEPROM on the SFP contains the system information as specified by the SFP MSA specification. In the fiber optic SFP, the EEPROM is directly connected to the MOD-DEF(1) and MOD-DEF(2) pins of the SFP Interfaces. However, in a VSC8221-based copper SFP, a single EEPROM is used to contain the system information as per the SFP MSA specification as well as to initialize the VSC8221 PHY on startup. So, the EEPROM is connected to the VSC8221 PHY. As shown in the previous block diagram, the system can access page '0' of the EEPROM, where the system information is stored using the MOD-DEF(1) and MOD-DEF(2) pins of the SFP Interface connector. To the system the EEPROM appears to be directly connected to the MOD-DEF(1)/(2) pins.
- In most fiber optic SFPs a 128-byte or 256-byte EEPROM (that is, an AT24C01 or a AT24C02) is used. However, in a VSC8221-based copper SFP an EEPROM of size greater than or equal to 512 bytes should be used, that is an AT24C04, AT24C08 or AT24C16 EEPROMs can be used but an AT24C01 and AT24C02 cannot be used.
- In a fiber optic SFP the MOD-DEF(0) pin of the SFP Interface is grounded. In the host system, the MODDEF(0) pin is pulled up. On insertion of a SFP this pin transitions to a low state and this indicates the presence of an SFP to the host system. However, because the startup of a 10/100/1000BASE-T PHY is slower than a fiber optic SFP, direct grounding of the MOD-DEF(0) pin on the SFP is not recommended. The MOD-DEF(0) pin on the SFP Interface should be connected to the MODDEF0 pin of the VSC8221 PHY. Once the SFP is inserted in a system, the PHY drives the MOD-DEF(0) pin low after it has initialized itself from the EEPROM.
- The LOS pin of the SFP interface should be connected to the RXLOS pin of the VSC8221 PHY. This pin is driven high when the copper media link drops. By default, a 20 ms pulse (low-high-low) will be driven on the LOS pin when the copper media link drop. The VSC8221 PHY provides control over the behavior of the LOS signal. Refer to section Changing the Default RxLOS Behavior Setting for more details.

- TxDisable pin of the SFP interface should be connected to the TXDISABLE pin of the PHY. When this signal is driven high by host system, the PHY immediately enters a low power state and drops the copper media link.

4.2 Copper SFP Schematic

A complete schematic of a VSC8221-based copper SFP is provided as part of the VSC8221HHEV reference design kit. It is recommended that the schematic be used without any changes.

- If it is required that the LOS signal always be low, then R18 must not be populated in the final board build.
- R7 can be left unpopulated. It is recommended that R11 always be populated on the final board build. This is because it eliminates the possibility of the host system detecting a SFP when the SFP is still in the initializing phase.
- Surface mount common mode chokes L3 ,L4, and a 4-core transformer T1 constitute the isolation transformer shown in the Copper SFP Block Diagram. Due to space constraints, the VSC8221HHEV design uses a miniature surface mount common mode choke by Murata (Part No: DPL31DN900ML4L) for EMI suppression and a custom 4-coil transformer by Delta (Part No: LF9231) for isolation. Please refer to Vitesse's Copper SFP PHY Performance comparison White Paper for EMI performance of VSC8221-based copper SFPs using this transformer configuration. Any standard 8-coil or 12-coil 10/100/1000BASE-T magnetics can be used in place of L3, L4, and T1. It is recommended that if this change is made, the customer send the schematics to Vitesse for review.
- The PHY provides 3 active low, direct drive LED pins namely LED2, LED1, LED0. Refer to section 14 LED Interface and section 26.2.28 LED Control Register of the VSC8221 datasheet before finalizing this part of the circuit. This is required to make sure that the connected LEDs provide the functions needed by the SFP design.

4.3 Copper SFP Layout

The VSC8221HHEV reference SFP's layout files are part of the VSC8221 reference design kit. This is a 4-layer layout and emphasis good layout practices for high speed circuits. These are:

- The MAC interface traces TD+/TD- and RD+/RD- should be routed as 100 Ω differential or 50 Ω single-ended traces.
- The copper media traces between the PHY and isolation transformer and between the isolation transformer and the RJ45 must be routed as controlled impedance traces. These are the traces originating from the TXVPA/TXVNA, TXVPB/TXVNB, TXVPC/TXVNC, TXVPD/TXVND pins of the VSC8221 PHY. These can be routed as 100 Ω differential pairs or as 50 Ω single-ended traces.
- The power supplies must be routed as planes as much as possible.
- The decoupling capacitors must be as close to the respective power supply pins of the PHY as possible.
- The resistor R3 connected to REFREXT and capacitor C16 connected to REFFILT must be as close to the PHY as possible and connected to ground through a common via.
- Switching Regulator filtering components L2 and C17 must be placed as close to REGOUT as possible.

4.4 Copper SFP Configuration

As mentioned previously in this document, the same copper SFP can be set to operate as a 1000BASE-T only (1000BASE-X MAC interface) or a triple speed 10/100/1000BASE-T SFP (SGMII MAC interface) by changing the operating mode of the PHY. The SFP's default operating mode is set by the initialization provided by the EEPROM. The operating mode can also be changed after the SFP has powered up by writing to the PHY registers. This will be described in greater detail in the following sections. However, before setting the operating mode of the SFP it is important to understand the various operating modes provided by the PHY. Please read section VSC8221 Operating Modes for Copper SFP Applications for more information on this topic.

4.4.1 Default PHY Initialization

The EEPROM (component U4 on the VSC8221HHEV reference SFP design) on the copper SFP serves two purposes:

- Stores system information in EEPROM address locations 0-255, according to the SFP MSA specification.
- Stores data for PHY initialization during startup.

Refer to section EEPROM Interface of the VSC8221 Datasheet for more information.

The PHY initialization data is stored in the EEPROM, starting from address location 256. This is shown in the following table.

Note: The following EEPROM content must be copied to the SFP's EEPROM without any changes to the EEPROM address locations, data values, or the sequence.

Table 1 • Default EEPROM Content

EEPROM Address (hexadecimal)	Data (hexadecimal)	Function
0x100	0xBD	Indicates presence of Initialization Sequence in the EEPROM.
0x101	0xBD	
0x102	0x01	EEPROM Address of Starting point of intialzation sequence.
0x103	0x04	
0x104	0x00	Length of Initialization sequence - Number of PHY register write * 3.
0x105	0x42	
0x106	0x1F	These EEPROM writes modify MII Register 23 to set the PHY operating mode.
0x107	0x00	The PHY operating mode set here is – Operating mode 1 – 802.3z SerDes to CAT5, with clause 37 auto-detection.
0x108	0x00	
0x109	0x17	
0x10A	0xEC	
0x10B	0x21	
0x10C	0x1F	Write to PHY Registers - Fix for interoperability issue with Intel 82547EI Gigabit Ethernet MAC+PHY IC.
0x10D	0x00	
0x10E	0x00	
0x10F	0x12	
0x110	0x00	
0x111	0x49	
0x112	0x1F	Write to internal PHY Registers (not mentioned in the datasheet) for optimal PHY performance.
0x113	0x2A	
0x114	0x30	
0x115	0x08	
0x116	0x02	
0x117	0x12	
0x118	0x1F	
0x119	0x52	
0x11A	0xB5	
0x11B	0x00	
0x11C	0xAF	
0x11D	0xA4	
0x11E	0x02	

EEPROM Address (hexadecimal)	Data (hexadecimal)	Function
0x11F	0x00	
0x120	0x0F	
0x121	0x01	
0x122	0x47	
0x123	0x2A	
0x124	0x00	
0x125	0x8F	
0x126	0xA4	
0x127	0x1F	
0x128	0x2A	
0x129	0x30	
0x12A	0x08	
0x12B	0x00	
0x12C	0x12	
0x12D	0x1F	Turn off CLKOUTMICRO clock output to save power and for better EMI performance.
0x12E	0x00	
0x12F	0x01	These EEPROM Writes modify Extended MII Register 17 to turn of the CLKOUTMICRO clock output.
0x130	0x11	
0x131	0xFF	
0x132	0xD0	
0x133	0x1F	Turn off CLKOUTMAC clock output to save power and for better EMI performance.
0x134	0x00	These EEPROM Writes modify MII Register 18 to turn of the CLKOUTMAC clock output.
0x135	0x00	
0x136	0x12	
0x137	0x00	
0x138	0x48	
0x139	0x1B	Setting LED behavior - LED2 = Duplex/Collision.
0x13A	0x06	LED1 = Link/Activity LED0 = Fault.
0x13B	0x80	These EEPROM Writes modify MII Register 27 to set the LED default functions output.
0x13C	0x1E	Setting RxLOS behavior – a 20ms wide pulse is driven on the RxLOS pin when the CAT5 link drops.
0x13D	0x00	
0x13E	0x01	These EEPROM Writes modify MII Register 30 to set the default RxLOS behavior.
0x13F	0x1F	Marvell Compatibility Feature – This feature is disabled by default. To enable this feature set address location 0x143 to 0xA3.
0x140	0x2A	
0x141	0x30	
0x142	0x10	
0x143	0x23	
0x144	0x4C	
0x145	0x1F	
0x146	0x00	

EEPROM Address (hexadecimal)	Data (hexadecimal)	Function
0x147	0x00	

4.4.1.1 Changing the Default PHY Operating Mode

The operating mode set by the initialization script shown previously is Operating mode 1 – 802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation detection. The default operating mode of the SFP can be changed by changing the values stored in EEPROM locations 10Ah and 10Bh. This is summarized in the following table.

Table 2 • Changing the Default PHY Operating Mode

	PHY Operating Mode	Auto-negotiation Category	MAC Interface Catergory	EEPROM Data Value at Address 0x10A	EEPROM Data Value at Address 0x10B
1	802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Detection	Clause 37 Autonegotiation Enabled	1000BASE-X – For 1000BASE-T only copper SFP	0xEC	0x21
2	802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Enabled			0xEC	0x23
3	802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Enabled, Media Convertor Mode			0xEC	0x25
4	802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Disabled	Clause 37 Auto-negotiation Disabled		0xFC	0x21
5	SGMII to CAT5 Media, with Modified Clause 37 Auto-negotiation Enabled	Modified Clause 37 Enabled	SGMII – For 10/100 /1000BASE-T triple speed SFP[1]	0xAC	0x23
6	SGMII to CAT5 Media, with Modified Clause 37 Auto-negotiation Disabled	Modified Clause 37 Disabled		0xBC	0x21

1. It is recommended that these operating modes should not be used as the default operating mode of the SFP, if the SFP may be used in a legacy system that supports only the 1000BASE-X MAC interface on its SFP ports.

4.4.1.2 Changing the Default RxLOS Behavior Setting

The PHY provides the flexibility to set the behavior of the RxLOS signal by setting the appropriate defaults in the PHY Register 30.1:0 at startup. The EEPROM initialization code shown above sets the behavior of the RxLOS as a 20ms high pulse when the copper link drops. The default behavior of the RxLOS signal can be changed by changing the values stored in EEPROM locations 0x13D and 0x13E. This summarized in the following table.

Table 3 • Changing the Default RxLOS Behavior

RxLOS Behavior	EEPROM Data Value at Address 0x13D	EEPROM Data Value at Address 0x13E
A 20 ms high pulse (low-high-low) is driven by the on the RxLOS pin when the copper media link goes down.	0x00	0x01
A 200 ms high pulse (low-high-low) is driven by the on the RxLOS pin when the copper media link goes down.	0x00	0x02
A 500 ms high pulse (low-high-low) is driven by the on the RxLOS pin when the copper media link goes down.	0x00	0x03
RxLOS is always driven low.	0x00	0x00

In Operating mode 5 - Operating Mode 5 - SGMII to CAT5 Media, with Modified Clause 37 Auto-negotiation Enabled the RxLOS is always driven low by the PHY.

4.4.1.3 Changing the Default LED Setting

The PHY provides three active low, direct drive LED pins namely LED2, LED1, LED0. Each of these LEDs can be assigned one of four possible LED functions. This is described in section LED Interface and section LED Control Register of the VSC8221 datasheet.

To set the required behavior of the LEDs, PHY register 27 must be initialized accordingly. This is done in EEPROM locations 0x13A and 0x13B. Location 0x13A contains bits 15:0 of the MII Register 27's value and Location 0x13B contains bits 7:0 of the MII Register 27's value. The EEPROM data shown in table Default EEPROM Content sets MII Register 27 as 0x0680 setting LED2 = Duplex/Collision, LED1 = Link /Activity and LED0 = Fault.

4.4.2 PHY Configuration After Initialization

Once the SFP is plugged into a system, the system can access the PHY registers via the MOD-DEF(2)/(1) pins using the I2C 2-wire protocol. Reading/Writing the PHY register is identical to reading/writing the an EEPROM address with page address '6' (or 0xAC for write and 0xAB for read). More details on accessing the PHY registers can be found in datasheet section PHY Register access with SMI in MSA mode.

4.4.2.1 Changing the PHY Operating Mode

This is the most common task that a system may need to perform on the SFP. For example a system may be SGMII capable whereas the SFP's default operating mode could be 1000BASE-X MAC interface. In this case, when the SFP is plugged into the system, the host system can change the operating mode of the SFP by writing to MII Register 23 of the PHY in the SFP, followed by a software reset (this is described in the next section). The following table summarizes the writes to MII Register 23 to set the operating mode of the PHY/SFP.

Table 4 • Changing the PHY Operating Mode After Initialization

	PHY Operating Mode	Auto-negotiation Category	MAC Interface Category	MII Register 23 Value (bits 15: 0)
1	802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Detection	Clause 37 Auto-negotiation Enabled	1000BASE-X – For 1000BASE-T only copper SFP	0XEC21
2	802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Enabled			0XEC23
3	802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Enabled, Media Convertor Mode			0XEC25
4	802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Disabled	Clause 37 Auto-negotiation Disabled		0XFC21
5	SGMII to CAT5 Media, with Modified Clause 37 Auto-negotiation Enabled	Modified Clause 37 Enabled	SGMII – For 10/100 /1000BASE-T triple speed SFP	0XAC23
6	SGMII to CAT5 Media, with Modified Clause 37 Auto-negotiation Disabled	Modified Clause 37 Disabled		0XBC21

4.4.2.2 Performing Software Reset

To perform software reset on the PHY in the SFP, do the following:

- Write 0x9040 to MII Register 0.
- Read EEPROM Address 0 (of page '0') of the EEPROM twice OR provide 70 clock cycles on the MODDEF1/MDC pin.

4.5 Copper SFP Testing

Once the first prototype of an SFP is built it should be tested in the following stages:

4.5.1 Stage 1 – Test the Board

Once the SFP is plugged into an SFP port and the 3.3v supply is up:

- All the power supplies (the 3.3v and 1.2v supply) must be checked near the respective local decoupling capacitors. It is recommended that an oscilloscope be used for this purpose, in order to check the supply noise.
- Check the voltage on the REFREXT pin. It should be 1.0v.
- Check the voltage on the REFFILT pin. It should be 1.2v.
- Check the clock on the XTAL1 or XTAL2 pin. It should be a 25 MHz sine wave. It is recommended that a frequency meter be used for this purpose to ensure that the clock is within +/-100ppm of 25 MHz.

4.5.2 Stage II – Check PHY Initialization

- Check if the EEPROM contains the initialization code – Read the EEPROM via the MOD-DEF(1)/(2) pin of the SFP interface. Locations 0x100 through 0x13E must contain the data as shown in 'Table 1Default EEPROM content'.
- Check if the PHY has initialized itself from the EEPROM – Read PHY MII Register 18. It should return a value of 0x0048.
- Check the default operating mode – Read MII Register 23. It should return the desired operating mode as set in EEPROM location 0x10A and 0x10B

### 4.5.3 Stage III – Test the PHY's/SFP's High-Speed Serial Interface

Figure 11 • Testing the High-Speed Serial Interface
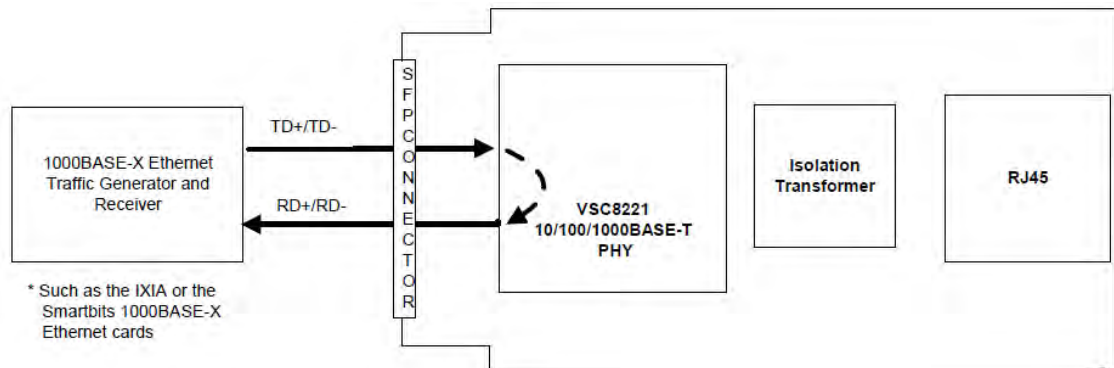
- Plug in the SFP.
- Set the PHY in operating mode 4 – 802.3z Serdes to CAT5, Clause 37 Auto-negotiation disabled mode by writing 0xFC21 to MII Register 23, followed by a software reset. Refer to section Performing Software Reset for information regarding software reset.
- Set the PHY in near-end Loopback by writing 0x4140 to MII register 0.
- Send 8b/10b encoded gigabit Ethernet traffic over the TD+/TD- pins of the SFP host connector. You should see the data reflect back on the RD+/RD- pins without any errors.

4.5.4 Stage IV – Test the PHY's/SFP's CAT5 Interface at 10 Mbps, 100 Mbps, and 1000 Mbps Speeds

Figure 12 • Testing the CAT5 Copper Media Interface
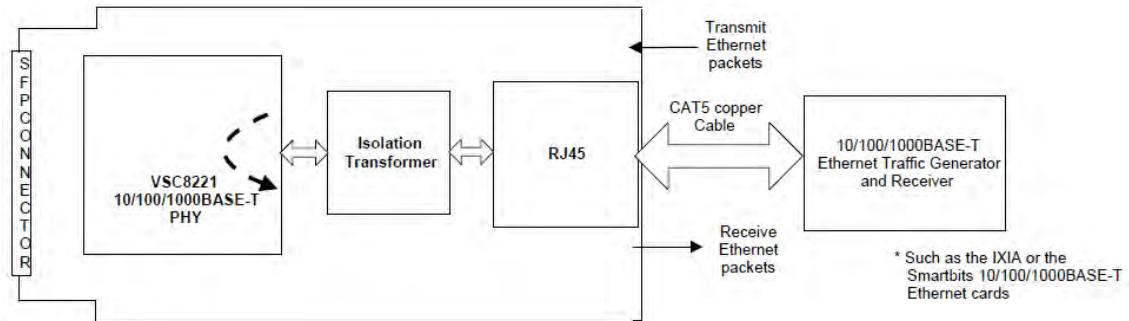
- Plug in the SFP.
- Set the PHY in operating mode 6 – SGMII to CAT5, Modified Clause 37 Auto-negotiation disabled mode by writing 0xBC21 to MII Register 23, followed by a software reset. Refer to section 3.4.2.2 Performing software reset for information regarding software reset.
- Set the PHY in far-end Loopback by writing 0xBC29 to MII register 0.
- Perform the steps mentioned the sections 3.9.1 through 3.9.3 to test 10BASE-T, 100BASE-TX, or 1000BASE-T interface.

4.5.4.1 10BASE-T Testing

- Set PHY's auto-negotiation advertisement setting to be 10BASE-T full duplex only.

  - Disable 1000FDX/HDX advertisement - Write 0x0000 to MII Register 9.
  - Disable 100FDX/HDX,10HDX advertisement - Write 0x0041 to MII Register 4.
  - Restart auto-negotiation - Write 0x1240 to MII Register 0.

- Connect the PHY to a copper link partner that has the capability to perform 10BASE-T FDX operation, for example, smartbits copper Ethernet test equipment.
- Make sure the copper link has been established by checking the Link LED of the PHY, the Link LED of the link partner or by reading MII Register 1. MII Register 1 should read 0x796D.
- Transmit 10BASE-T Ethernet traffic from the link partner. You should receive the transmitted data packets without any errors.

### 4.5.4.2 100BASE-T Testing

- Set PHY's auto-negotiation advertisement setting to be 100BASE-T full duplex only.

  - Disable 1000FDX/HDX advertisement - Write 0x0000 to MII Register 9.
  - Disable 10FDX/HDX,100HDX advertisement - Write 0x0101 to MII Register 4.
  - Restart auto-negotiation - Write 0x1240 to MII Register 0.

- Connect the PHY to a copper link partner that has the capability to perform 100BASE-T FDX operation, for example, smartbits copper Ethernet test equipment.
- Make sure the copper link has been established by checking the Link LED of the PHY, the Link LED of the link partner or by reading MII Register 1. MII Register 1 should read 0x796D.
- Transmit 100BASE-T Ethernet traffic from the link partner. You should receive the transmitted data packets without any errors.

4.5.4.3 1000BASE-T Testing

- Set PHY's auto-negotiation advertisement setting to be 1000BASE-T full duplex only.

    - Disable 1000HDX advertisement - Write 0x0600 to MII Register 9.
    - Disable 100FDX/HDX,10FDX/HDX advertisement - Write 0x0001 to MII Register 4.
    - Restart auto-negotiation - Write 0x1240 to MII Register 0.

- Connect the PHY to a copper link partner that has the capability to perform 1000BASE-T FDX operation, for example, smartbits copper Ethernet test equipment.
- Make sure the copper link has been established by check the Link LED of the PHY, the Link LED of the link partner or by reading MII Register 1. MII Register 1 should read 0x796D.
- Transmit 1000BASE-T Ethernet traffic from the link partner. You should see the data packets reflected back without any errors.

4.5.5 Stage V – Testing Full SFP Operation

Figure 13 • Testing the Full SFP Operation
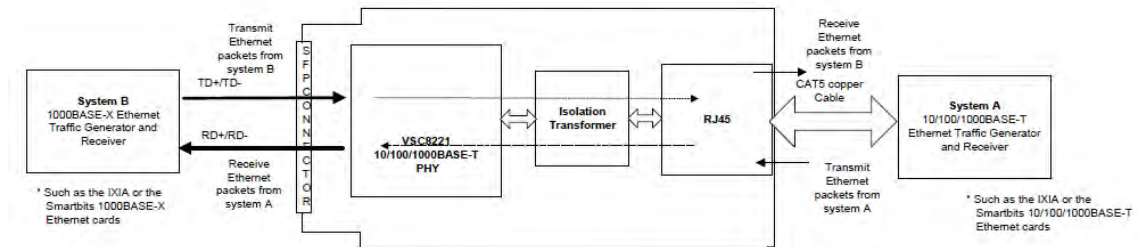
- Plug in the SFP.
- Set the PHY in operating mode 4 – 802.3z Serdes to CAT5, Clause 37 Auto-negotiation disabled mode by writing 0xFC21 to MII Register 23, followed by a software reset. Refer section Performing Software Reset on information regarding software reset.
- Connect the PHY to a copper link partner that has the capability to perform 1000BASE-T FDX operation, for example, smatbits copper Ethernet test equipment.
- Make sure the copper link has been established by checking the Link LED of the PHY, the Link LED of the link partner or by reading MII Register 1. MII Register 1 should read 0x796D.
- Send 8b/10b encoded gigabit Ethernet traffic over the TD+/TD- pins of the SFP host connector (System B). You should see the data received on the copper link partner (System A) without any errors.
- Send 1000BASE-T Ethernet traffic from the copper link partner (System A). You should see the data received on the MAC connected to the SFP (System B) through the RD+/RD- pins.
- Perform the previous 2 steps simultaneously to ensure that there are no errors due to power supply noise, signal coupling and so on during bi-directional data transfer.

At this stage the basic functionality of the SFP has been tested for 1000BASE-T only as well as triple speed 10/100/1000BASE-T versions of module.

Further system level testing may be performed on the production release of the SFP.

4.5.6 Common Testing Issues

4.5.6.1 Testing with a PRBS Pattern

A copper SFP is not like a fiber optic SFP. It performs more involved data conversions, that is, from 8b/10b to 5PAM and vice-versa, whereas a fiber optic SFP performs an electrical to optical signal conversion and vice-versa. For this reason:

- In order to test the high-speed serial interface,the copper SFP needs 8b/10b encoded data in the form of a Ethernet packet. A random bit pattern such as the '1010..' or the PRBS pattern from a BERT cannot be used. A 1000BASE-X compliant data pattern must be used.

4.5.6.2 Testing the CAT5 Interface

All the operating modes that have Clause 37 or Modified Clause 37 enabled must be receiving valid '1000BASE-X with auto-negotiation' traffic pattern or a valid SGMII (with modifieded Clause 37 auto-negotiation) traffic pattern on the TD+/TD- pins in order for the SFP to establish a copper link.

4.5.6.3 Accessing Other Slave EEPROMs on the Shared I2C-Compatible Bus

In the system configuration shown below, when the SFP is plugged in, the system's stations manager cannot access the other slave EEPROMs (EEPROMs 0xA4, 0xA6, 0xA8, 0xAA, 0xAE). This is because the VSC8221 PHY on the SFP drives the MODDEF2 (SDA) pin high, rather than tri-stating, when in idle state.

Figure 14 • Possible System Configuration
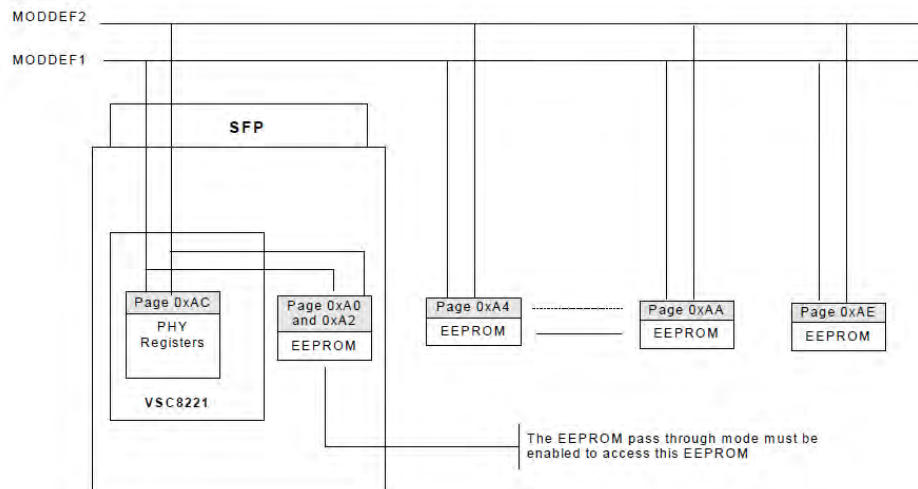
In order to access the other slave EEPROMs on the system the following steps must be performed:

- Disable the 'EEPROM pass-through' mode by performing the following steps:
  - Write 0x2a30 to MII register 31.
  - Write 0x300F to MII register 12.
  - Write 0x0000 to MII register 31.

By default the 'EEPROM pass-through' mode of the PHY is enabled, i.e. the EEPROM 0xA0 and 0xA2 on the SFP can be accessed.

- In this state the EEPROM pages 0xA0 and 0xA2 on the SFP cannot be accessed, but the other slave EEPROM on the I2C compatible bus can be accessed.
- To access the EEPROMs on the SFP the 'EEPROM pass-through' mode of the PHY must be re-enabled by performing the following steps:
  - Write 0x2a30 to MII register 31.
  - Write 0x200F to MII register 12. (Don't perform a read-back after this write.)
  - Read any location (for example, location 0) from EEPROM page 0xA0 twice, but ignore the return values; OR provide 18 clock cycles on MODDEF1 (with MODDEF2 static).
  - Write 0x0000 to MII register 31.

5 VSC8221 Operating Modes for Copper SFP Applications

The PHY supports six operating modes for copper SFP applications. Four of these four are for '1000BASE-T only' (1000BASE-X MAC Interface) copper SFPs and two are for 10/100/1000BASE-T triple speed (SGMII MAC Interfaces) copper SFPs. These modes are listed in the following table.

Table 5 • VSC8221 PHY Operating Modes

	PHY Operating Mode	Auto-negotiation Category	MAC Interface Category
1	802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Detection	Clause 37 Auto-negotiation Enabled	1000BASE-X – For 1000BASE-T only copper SFP
2	802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Enabled		
3	802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Enabled, Media Convertor Mode		
4	802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Disabled	Clause 37 Auto-negotiation Disabled	
5	SGMII to CAT5 Media, with Modified Clause 37 Auto-negotiation Enabled	Modified Clause 37 Enabled	SGMII – For 10/100 /1000BASE-T triple speed SFP
6	SGMII to CAT5 Media, with Modified Clause 37 Auto-negotiation Disabled	Modified Clause 37 Disabled	

The difference between the PHY operating modes in the above table is in the manner of interaction between the host (the switch that the SFP is inserted into) and the PHY. This interaction takes place over the SFP module's host interface (SFP connector).

5.1 PHY Operating Modes for 1000BASE-X MAC Interfaces

In case of a 1000BASE-T only copper SFP, that is, 1000BASE-X MAC interface, the auto-negotiation between the host and the PHY is the same as 1000BASE-X auto-negotiation and is called Clause 37 auto-negotiation. (The 'Clause 37' name comes from the IEEE 802.3z specification section, where this protocol is described.) The host can be in one of two modes:

- Clause 37 Auto-negotiation Enabled.
  OR
- Clause 37 Auto-negotiation Disabled.

Figure 15 • 1000BASE-X System Block Diagram
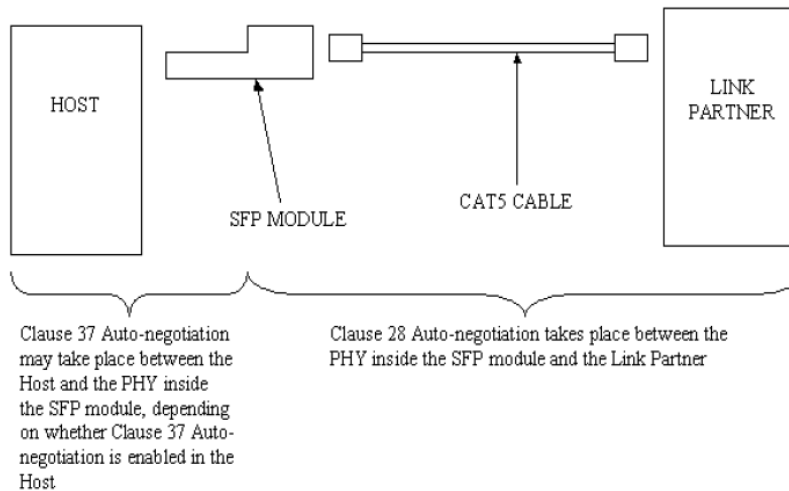
5.1.1 Clause 37 Auto-negotiation

If enabled, during auto-negotiation the host advertises some of the following capabilities:

- Full Duplex, Half Duplex.
- Flow control information.
- Remote Fault information (This is optional for Clause 37 implementation).

The speed of operation is always assumed to be 1000 Mbps. It is recommended in section 37.1.4.1 and 37.1.4.4 in the IEEE 802.3 standard that all 1000BASE-X devices use the Clause 37 auto-negotiation process to establish link.

5.1.2 Clause 28 Auto-negotiation

Although this auto-negotiation is used to establish a link at 10,100 or 1000 Mbps on the CAT5 Media, in 1000BASE-X MAC interface copper SFP applications it is used to establish a 1000BASE-T link only. The SFP advertises some of the following capabilities:

- 1000BASE-T Full duplex, 1000BASE-T Half duplex.
- Flow Control Information.

5.1.3 Description of Operating Modes (1000BASE-X MAC Interface)

Referring to table VSC8221 PHY Operating Modes, the VSC8221 PHY supports four 802.3z SerDes to CAT5 operating modes that can be used for 1000BASE-T only SFP applications.

In order to understand operating mode 1 '802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Detection' it is essential to understand operating modes 2 '802.3z SerDes to CAT5 Media, with Clause 37 Autonegotiation Enabled' and 4 '802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Disabled'. These modes are described in the following sections.

5.1.3.1 Operating Mode 2 - 802.3z SerDes to CAT5 Media, with Clause 37 Autonegotiation Enabled

Figure 16 • Clause 37 Auto-negotiation Enabled
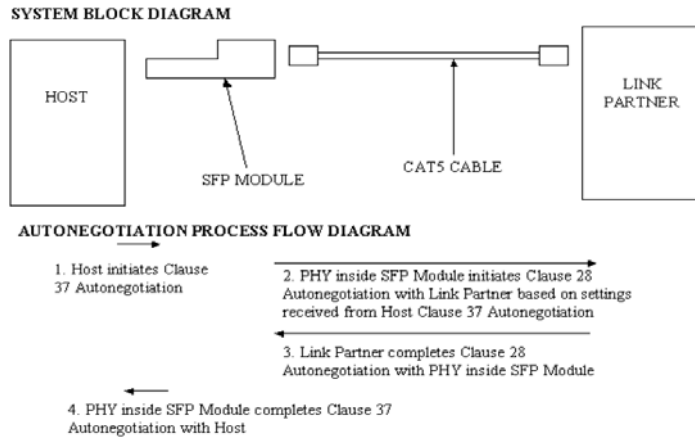
This operating mode is used when Clause 37 auto-negotiation is enabled on the host.

In this mode, the PHY uses the Clause 37 auto-negotiation information from the host MAC (that is, duplex and flow control information) to perform the Clause 28 CAT5 Media auto-negotiation. Once the Clause 28 CAT5 Media auto-negotiation completes, the PHY completes the Clause 37 auto-negotiation with the host MAC. After the Clause 37 auto-negotiation process is complete, the link has been established and data can be transferred.

In summary, in this mode the PHY performs a Clause 37 (information extraction from MAC)-Clause 28-Clause 37 (link establishment with MAC) sequence to establish a link and enter normal data transfer mode.

In this mode the SFP will not establish a CAT5 link if it does not receive Clause 37 compliant 8b/10b encoded traffic from the MAC.

5.1.3.2 Operating Mode 4 - 802.3z SerDes to CAT5 Media, with Clause 37 Autonegotiation Disabled

Figure 17 • Clause 37 Auto-negotiation Disabled
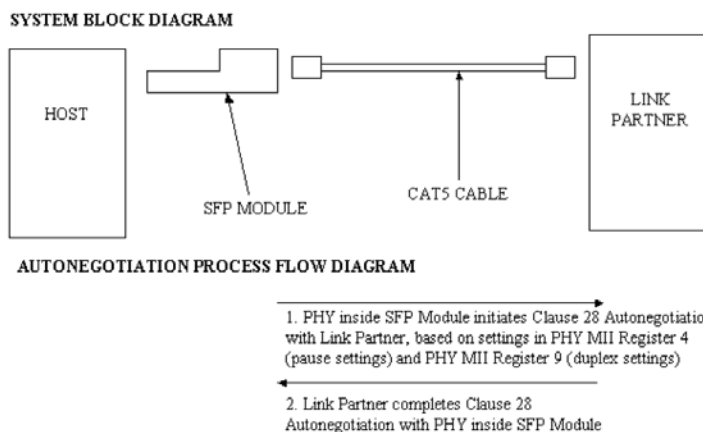
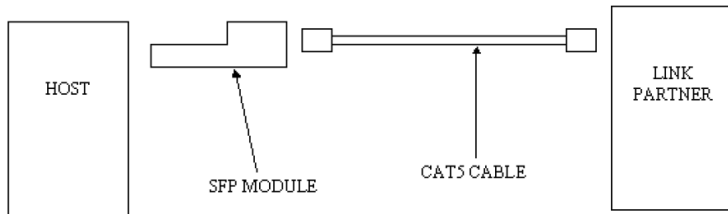This operating mode is used when Clause 37 auto-negotiation is disabled on the host.

In this mode, the PHY does not use any information from the host MAC, which should be in Clause 37 auto-negotiation disabled mode for normal data-transfer to happen after link establishment. The Clause 28 CAT5 Media autonegotiation is performed using the contents of PHY MII Register 4 (pause settings) and PHY MII Register 9 (duplex settings). By default, the PHY advertises 1000BASE-T Full duplex capability and therefore the link is always established in 1000Mbps Full duplex mode.

5.1.3.3 Operating Mode 1 - 802.3z SerDes to CAT5 Media, with Clause 37 Autonegotiation Detection

Figure 18 • Clause 37 Auto-negotiation Detection

A host can have Clause 37 auto-negotiation disabled or enabled. In order for data transfer to occur in a normal fashion after link is established, the Clause 37 state (that is, enabled or disabled) of the PHY and the host must be the same.

In systems where the host's Clause 37 capabilities are unknown, use of operating mode 1 is convenient.
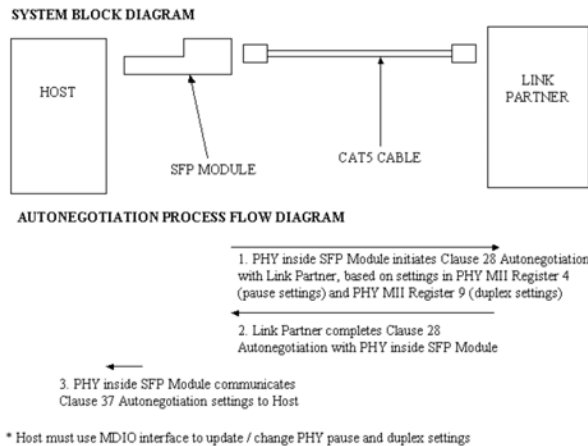
In this mode, the PHY detects the Clause 37 capabilities state of the host and sets the internal state of the PHY to operating mode 2 '802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Enabled' or 4 '802.3z SerDes to CAT5 Media, with Clause 37 Auto-negotiation Disabled'.

It should be noted that this detection of host's auto-negotiation capabilities happens only once after the SFP is plugged in. If the state of the host's auto-negotiation capability is changed after the SFP has been plugged into the system the SFP must be reset by pulling out and plugging back the SFP into the SFP port.

5.1.3.4 Operating Mode 3 - 802.3z SerDes to CAT5 Media, with Clause 37 Autonegotiation Enabled, Media Convertor Mode

Figure 19 • Clause 37 Auto-negotiation Enabled, Media Converter Mode

This operating mode is used when Clause 37 auto-negotiation is enabled on the host.

In this mode, the PHY does not use the Clause 37 auto-negotiation information from the MAC. The PHY uses the duplex information set in PHY MII Register 9 and Flow control information set in PHY MII Register 4 to perform the Clause 28 CAT5 Media auto-negotiation. Once the Clause 28 CAT5 Media auto-negotiation completes, the PHY completes the Clause 37 auto-negotiation with the MAC. It this stage, the link has been established and the data can be transferred.

In summary, in this mode the PHY performs a Clause 28 (information from PHY MII registers)-Clause 37 (link establishment with MAC) sequence to establish a link and enter normal data transfer mode.

In this mode the SFP will not establish a CAT5 link if it does not receive Clause 37 compliant 8b/10b encoded traffic from the MAC.

5.2 PHY Operating Modes for SGMII MAC Interfaces

In case of a triple speed 10/100/1000BASE-T copper SFPs, that is, SGMII MAC interface, the auto-negotiation between the host and the PHY is performed according to the SGMII specification by CISCO Systems and will be called Modified Clause 37 auto-negotiation (because this is very similar to the 1000BASE-X auto-negotiation mentioned in 'Clause 37' in the IEEE 802.3z specification section). A SGMII host can be in one of two modes:

- Modified Clause 37 Auto-negotiation Enabled.
  OR
- Modified Clause 37 Auto-negotiation Disabled.

The Modified Clause 37 Auto-negotiation disabled mode is not a standard operating mode and the SGMII specification does not cover this mode. It is unlikely that any system will be found operating in this mode.

5.2.1 Modified Clause 37 Auto-negotiation

If enabled, during auto-negotiation the PHY transfers the following information about its link configuration to the host MAC over the high speed serial Interface.

- Link Status
- Link Speed

- Full Duplex, Half Duplex
- Flow control information
- Remote Fault information (optional)

5.2.2 Clause 28 Auto-negotiation

This auto-negotiation is used to establish a link at 10,100 or 1000 Mbps on the CAT5 Media. In SGMII Interface mode the PHY uses the advertisement settings in MII Registers 4 and 9 of the PHY to establish a copper link with the 10/100/1000BASE-T link partner.
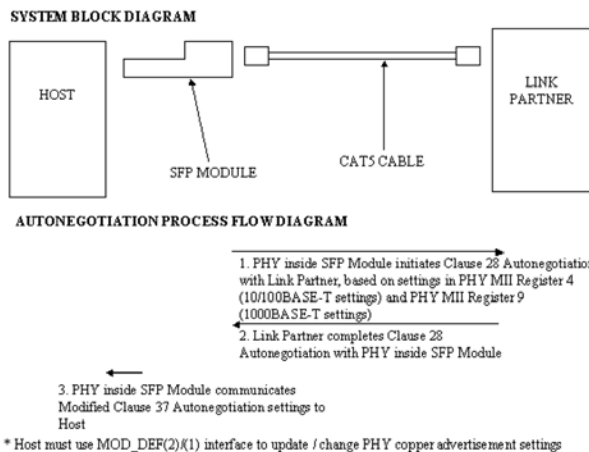
5.2.3 Description of Operating modes (SGMII MAC Interface)

Referring to table VSC8221 PHY Operating Modes, the VSC8221 PHY supports two SGMII to CAT5 operating modes that can be used for 10/100/1000BASE-T copper SFP applications. These modes are described in the following sections.

5.2.3.1 Operating Mode 5 - SGMII to CAT5 Media, with Modified Clause 37 Autonegotiation Enabled.

Figure 20 • SGMII, Modified Clause 37 Auto-negotiation Enabled

PHY MII Register 23.15:12,2:1 = 1010,01

SYSTEM BLOCK DIAGRAM

HOST — SFP MODULE — CAT5 CABLE — LINK PARTNER

AUTONEGOTIATION PROCESS FLOW DIAGRAM

1. PHY inside SFP Module initiates Clause 28 Autonegotiation with Link Partner, based on settings in PHY MII Register 4 (10/100BASE-T settings) and PHY MII Register 9 (1000BASE-T settings)

2. Link Partner completes Clause 28 Autonegotiation with PHY inside SFP Module

3. PHY inside SFP Module communicates Modified Clause 37 Autonegotiation settings to Host

* Host must use MOD_DEF(2)/(1) interface to update / change PHY copper advertisement settings

This operating mode is used when Modified Clause 37/SGMII auto-negotiation is enabled on the host.

In this mode, the PHY does not use the auto-negotiation information from the MAC. The PHY uses the speed and duplex information set in PHY MII Register 4 and 9 and Flow control information set in PHY MII Register 4 to perform the Clause 28 CAT5 Media auto-negotiation. Once the Clause 28 CAT5 Media auto-negotiation completes, the PHY completes the Modified Clause 37 auto-negotiation with the MAC according to the SGMII specification. At this stage, the link has been established and the data can be transferred.

In summary, in this mode the PHY performs a Clause 28 (information from PHY MII registers)- Modified Clause 37 (link establishment with MAC) sequence to establish a link and enter normal data transfer mode.
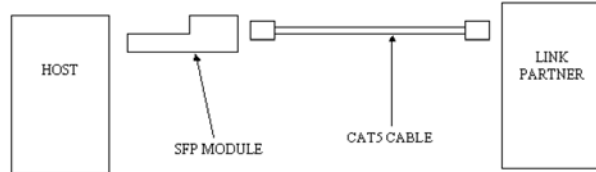
In this mode the SFP will not establish a CAT5 link if it does not receive SGMII protocol compliant 8b/10b encoded traffic from the MAC.

5.2.3.2 Operating Mode 6 - SGMII SerDes to CAT5 Media, with Modified Clause 37 Autonegotiation Disabled

Figure 21 • Clause 37 Auto-negotiation Disabled

PHY MII Register 23.15:12,2:1 = 1011,00

SYSTEM BLOCK DIAGRAM

HOST — SFP MODULE — CAT5 CABLE — LINK PARTNER

AUTONEGOTIATION PROCESS FLOW DIAGRAM

1. PHY inside SFP Module initiates Clause 28 Autonegotiation with Link Partner, based on settings in PHY MII Register 4 (10/100BASE-T settings) and PHY MII Register 9 (1000BASE-T settings)

2. Link Partner completes Clause 28 Autonegotiation with PHY inside SFP Module

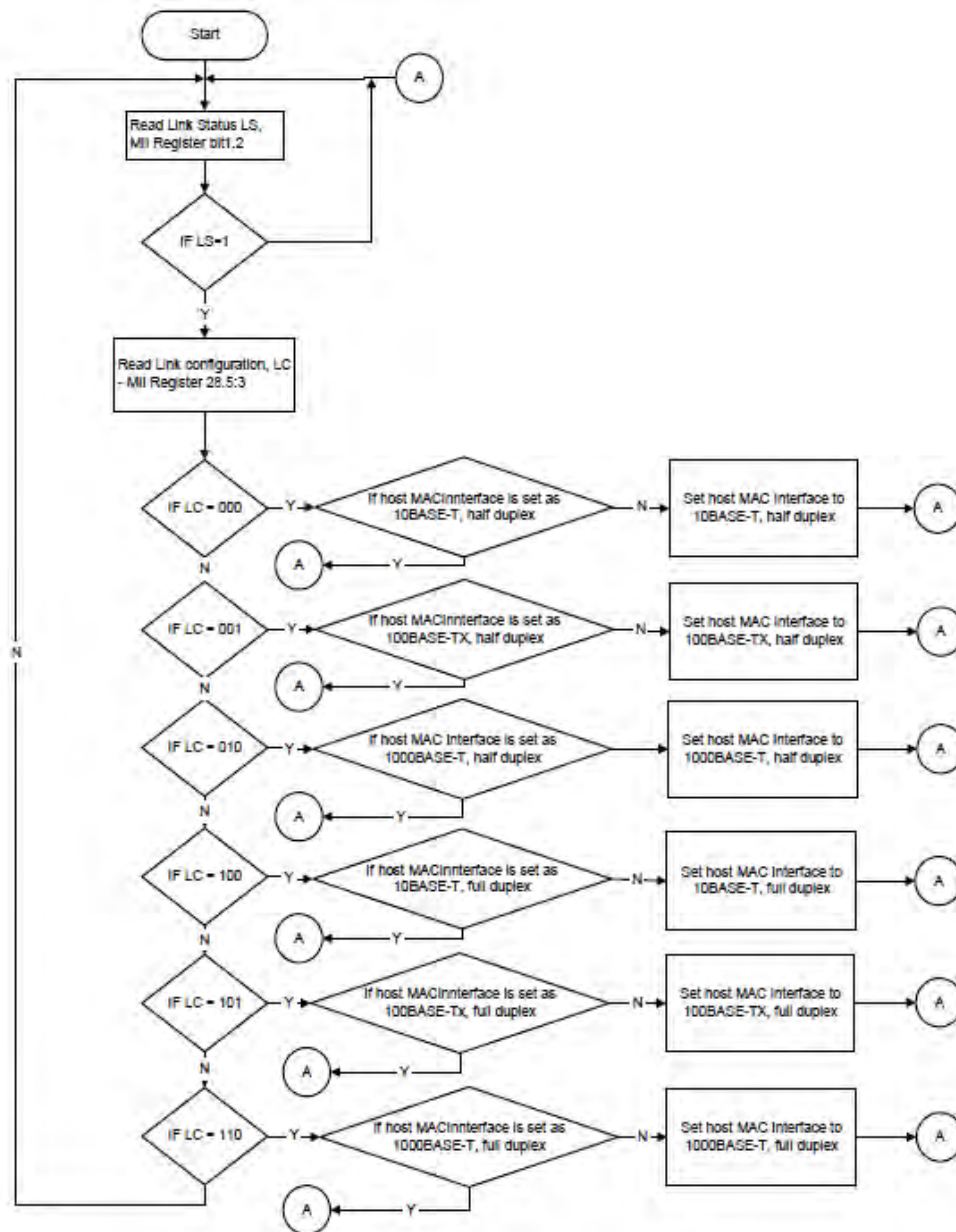•Host must use MOD_DEF(2)/(1) interface to update / change PHY copper advertisement settings.

•Host must also find the link status and configuration by querying the PHY registers in order to sets itself in the correct operating mode.

This operating mode is used when SGMII auto-negotiation is disabled on the host.

In this mode, the PHY uses the speed and duplex information set in PHY MII Register 4 and 9 and Flow control information set in PHY MII Register 4 to perform the Clause 28 CAT5 Media auto-negotiation. Once the link has been established and the data can be transferred for the local MAC to the link partner and vice-versa.

In this mode the host system needs to query the PHY's MII Registers using the MOD-DEF(2)/MOD-DEF(1) interface pins in order to find out the link status and link configuration. This procedure is identical to finding the link status and link configuration of a standard 10/100/1000BASE-T SFP using the standard MII Registers 0 through 15. The links status and configuration can also be found by using PHY register 28. The flowchart is shown as follows.

Figure 22 • Link Status and Link Configuration Check by Querying the PHY Registers via the MOD-DEF (2)/(1) Interface Pins

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