

Block diagram of VSC7512/VSC8514
unmanaged 8+2 port switch

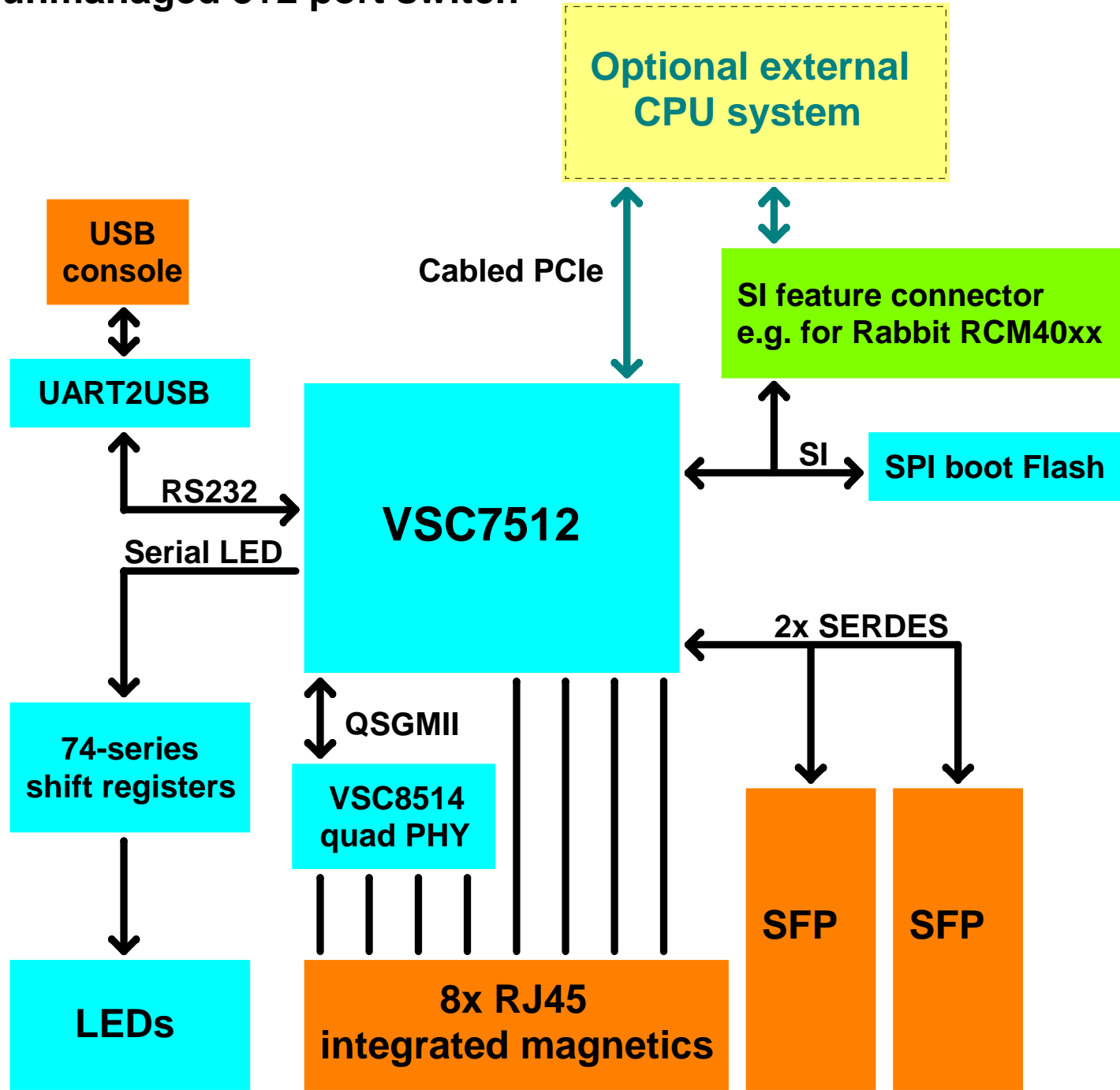


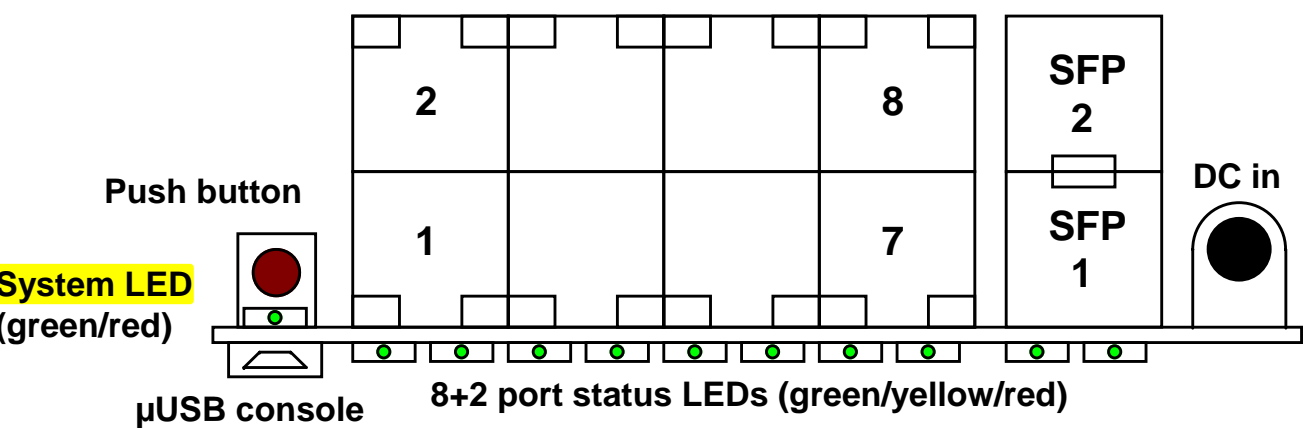
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Revision history

Version:	Date:	Author:	Main change(s):
01-00	2015-11-03	MAG	First release
01-01	2016-02-10	MAG	Swapped R1/R8 (2V5 LDO)
01-02	2016-02-12	MAG	J10,C149,C150,C151,C155,C165,C166,C167,C168 mounted (was not mounted)
01-03	2016-04-14	MAG	Changes to U10 3V3/RESET, swap U4 S4 Rx polarity
01-04	2016-04-20	MAG	Swapped RD/GR labels on LTST-S326 (LED) inputs etc.
01-05	2016-05-24	MAG	Added R87/R88, added R92
02-00	2016-08-11	MAG	Changed VSC7512 reference clock input circuit

Front layout



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Title
Block diagram

Size
A

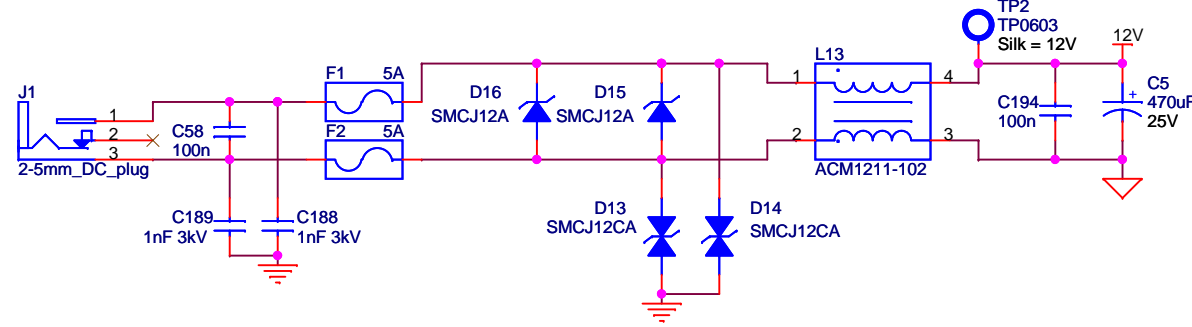
Document Number
PCB121

Rev
02-00

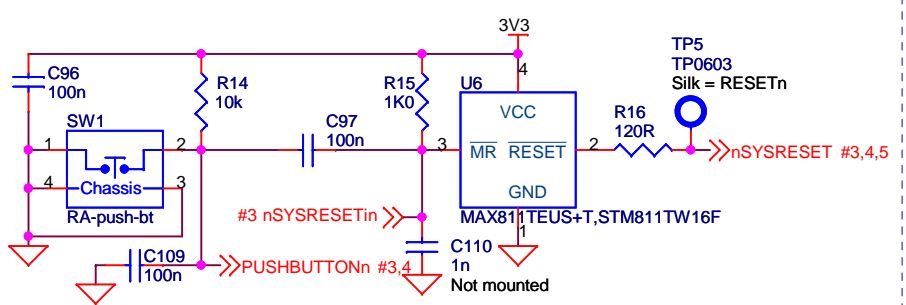
Date: Thursday, August 11, 2016

Sheet 1 of 6

2.5mm center pin DC jack for external PSU

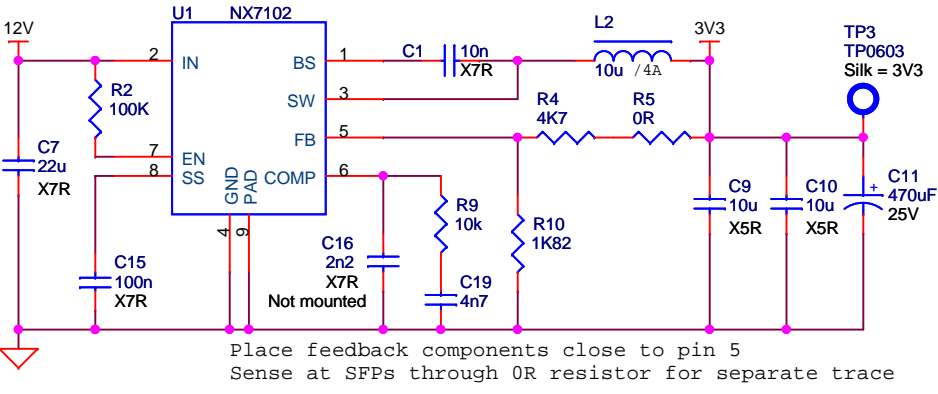


Reset generator



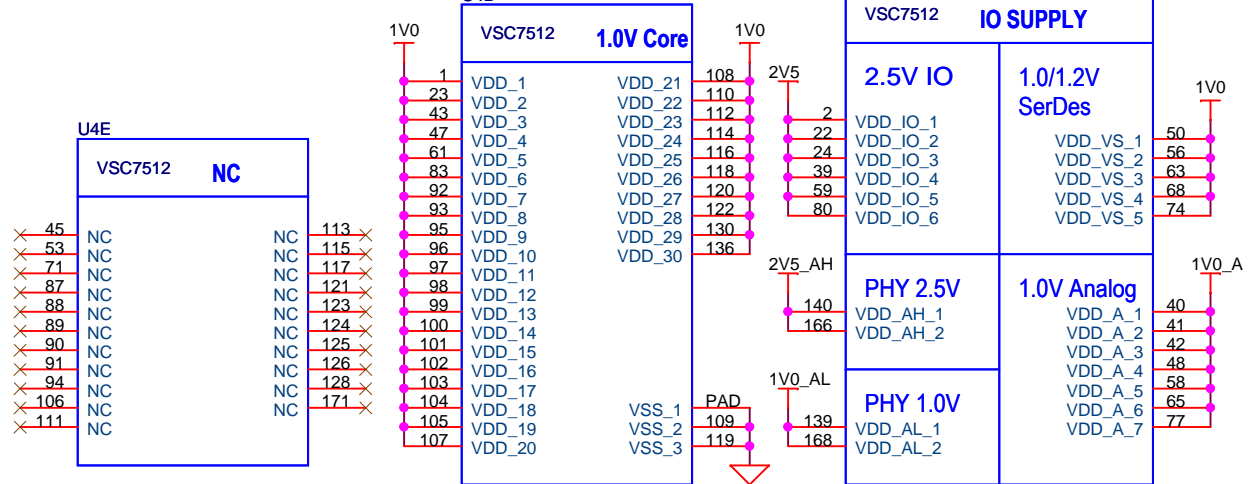
3V3 generation

Nominal output voltage = $(0.925V/1K82) * (1K82 + 4K7) = 3.31V$
Calculated current consumption on 3V3 = 2.2A

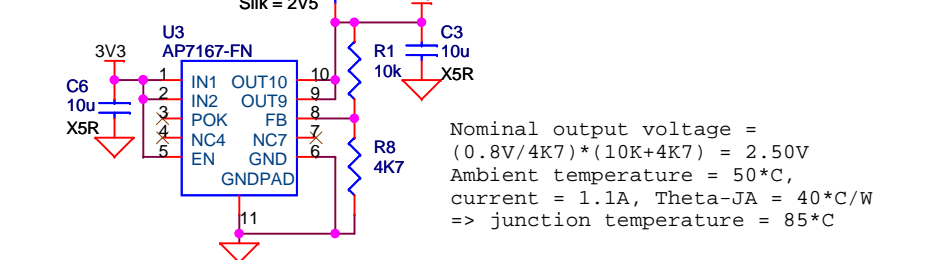


Place feedback components close to pin 5
Sense at SFPs through 0R resistor for separate trace

VSC7512 power/decoupling



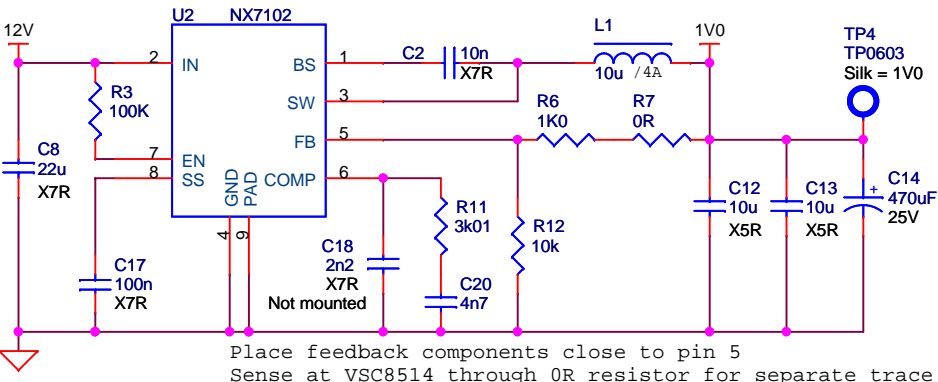
2V5 generation



Nominal output voltage = $(0.8V/4K7) * (10K + 4K7) = 2.50V$
Ambient temperature = 50°C,
current = 1.1A, Theta-JA = 40°C/W
=> junction temperature = 85°C

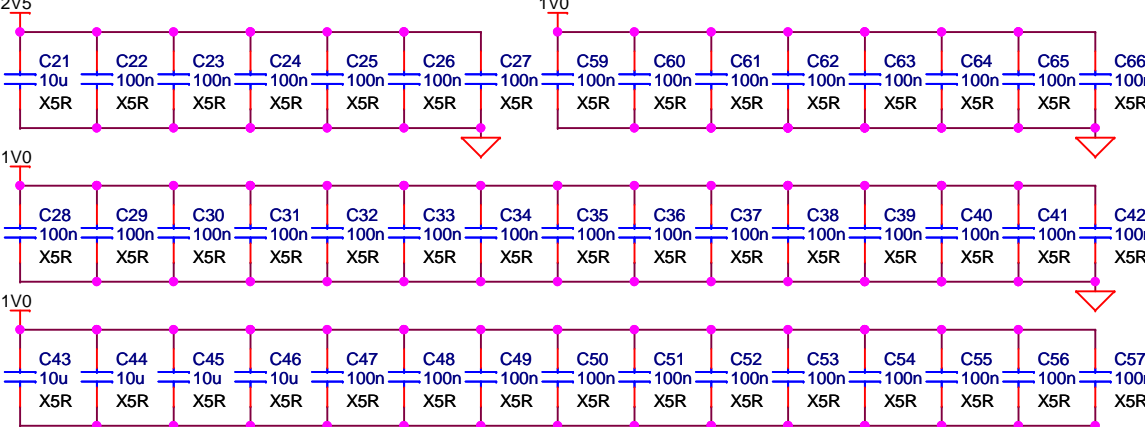
1V0 generation

Nominal output voltage = $(0.925V/10K) * (1K + 10K) = 1.02V$
Calculated current consumption on 1V0 = 3.0A

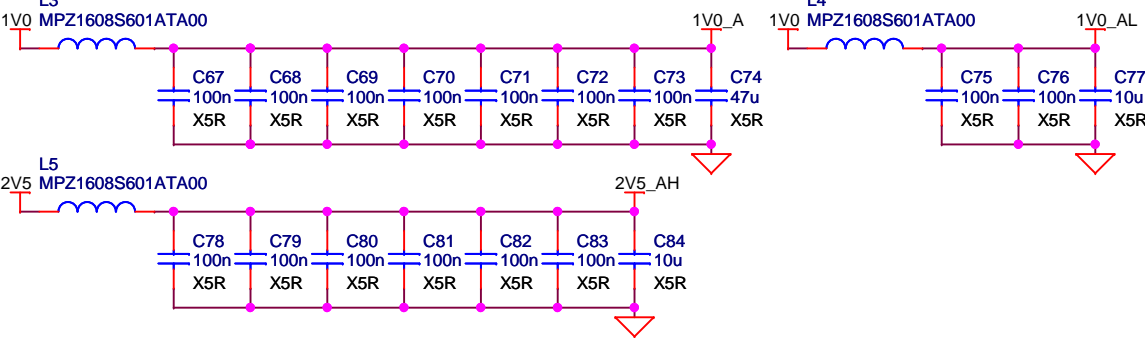


Place feedback components close to pin 5
Sense at VSC8514 through 0R resistor for separate trace

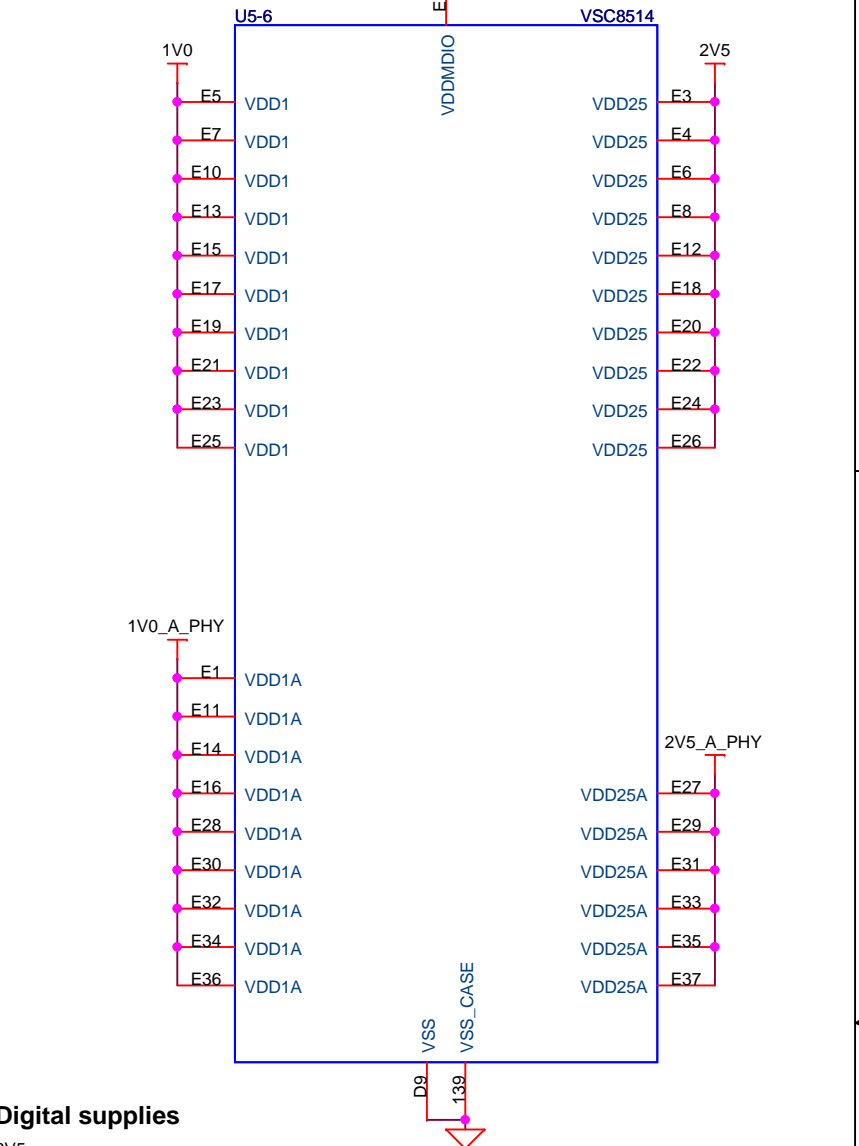
Digital supplies



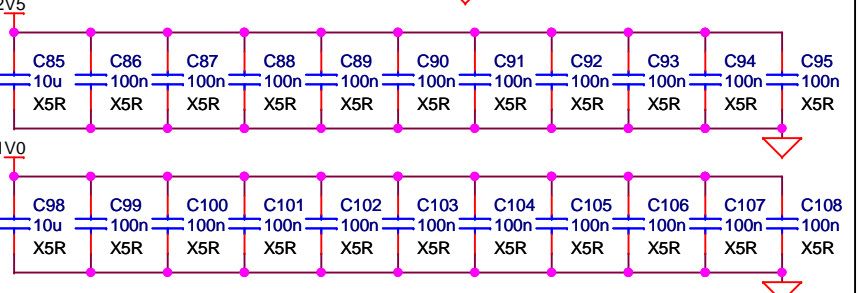
Filtered analog supplies



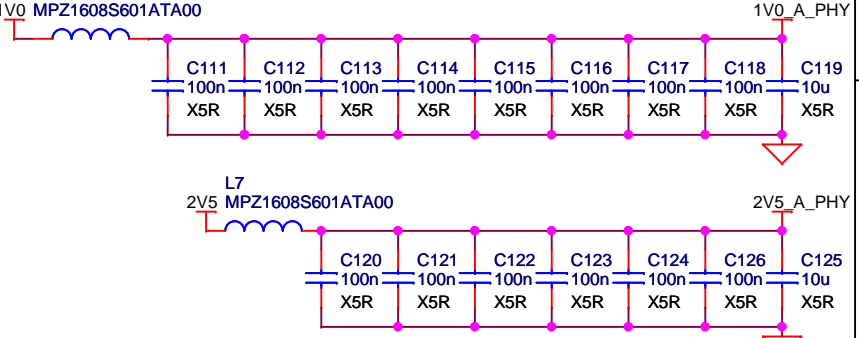
VSC8514 power/decoupling



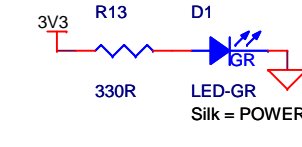
Digital supplies



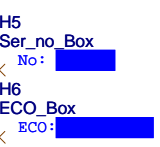
Filtered analog supplies



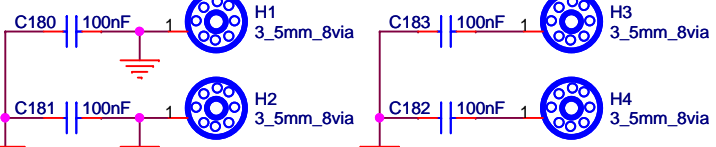
Power ON indicator



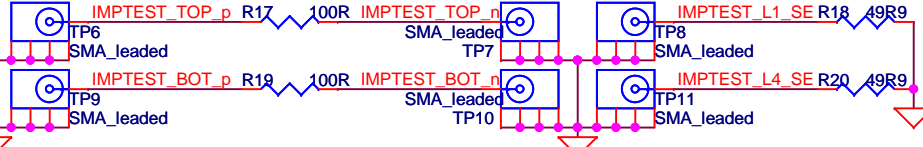
Silkscreen



Mounting holes



Impedance test traces



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Microsemi

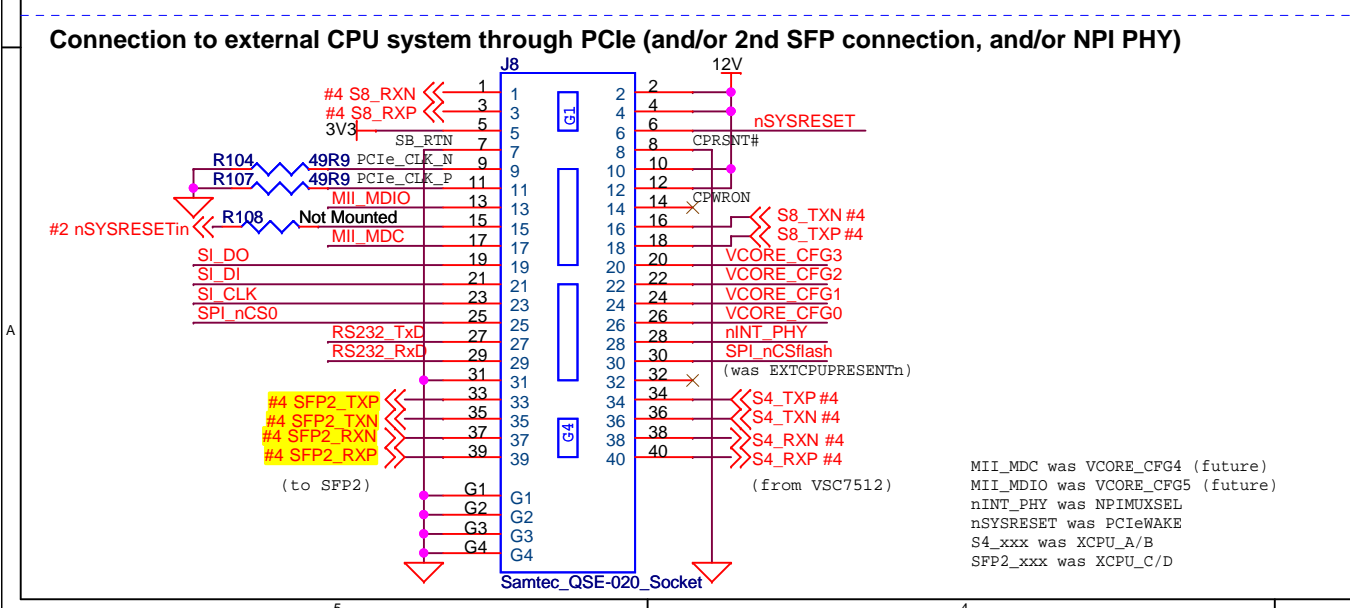
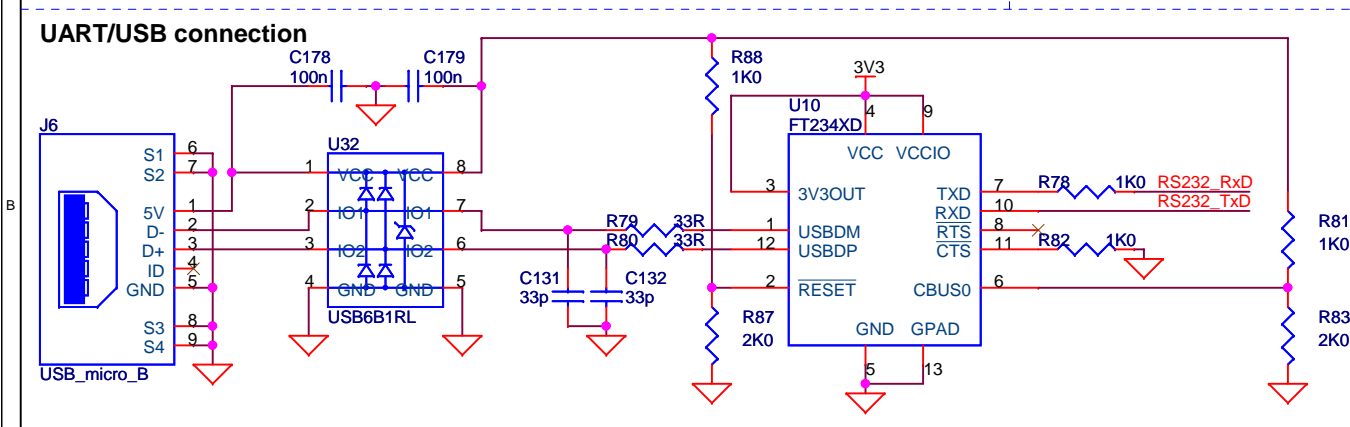
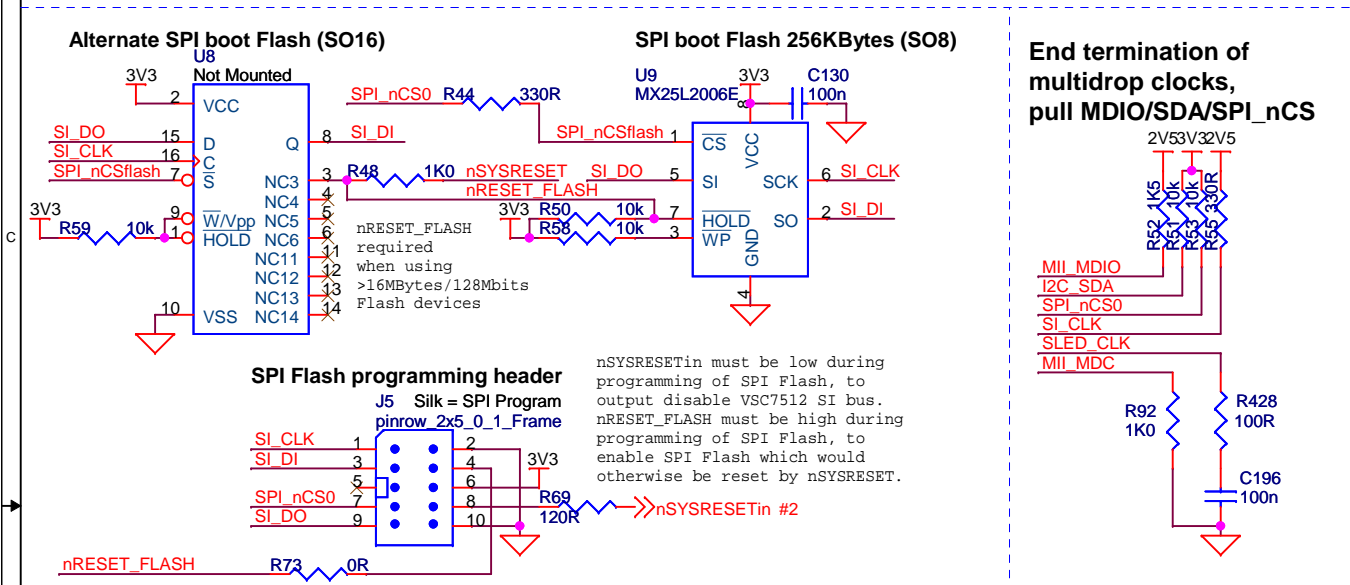
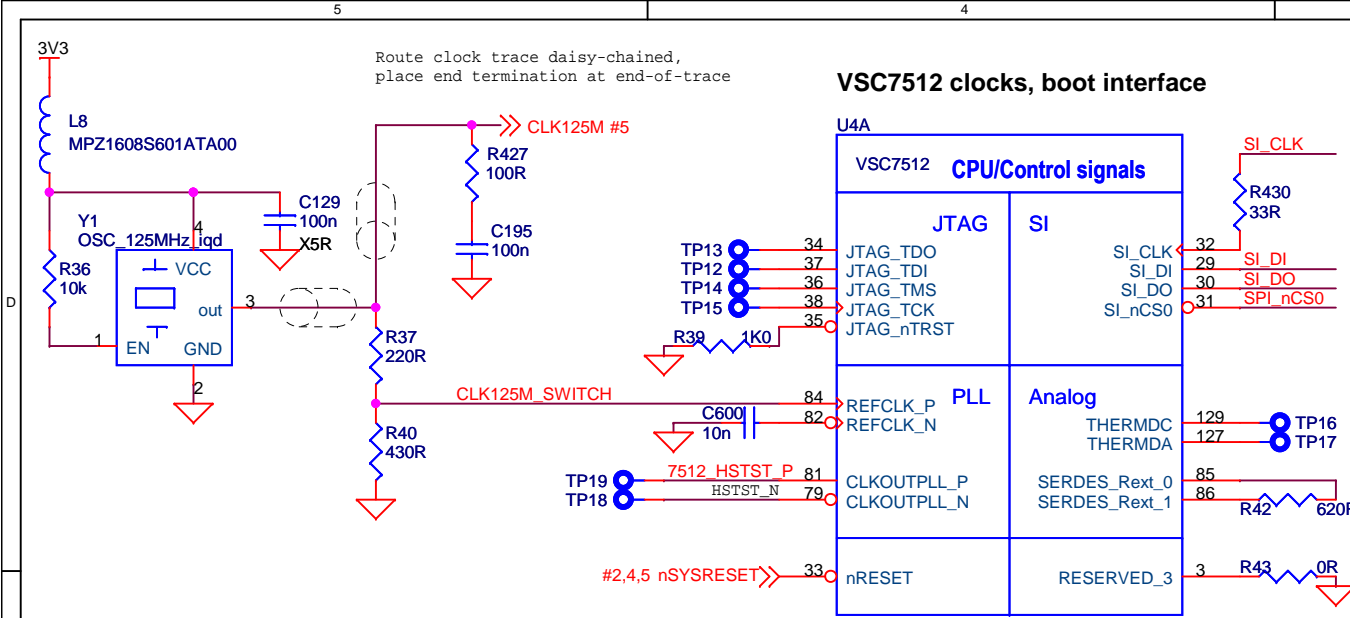
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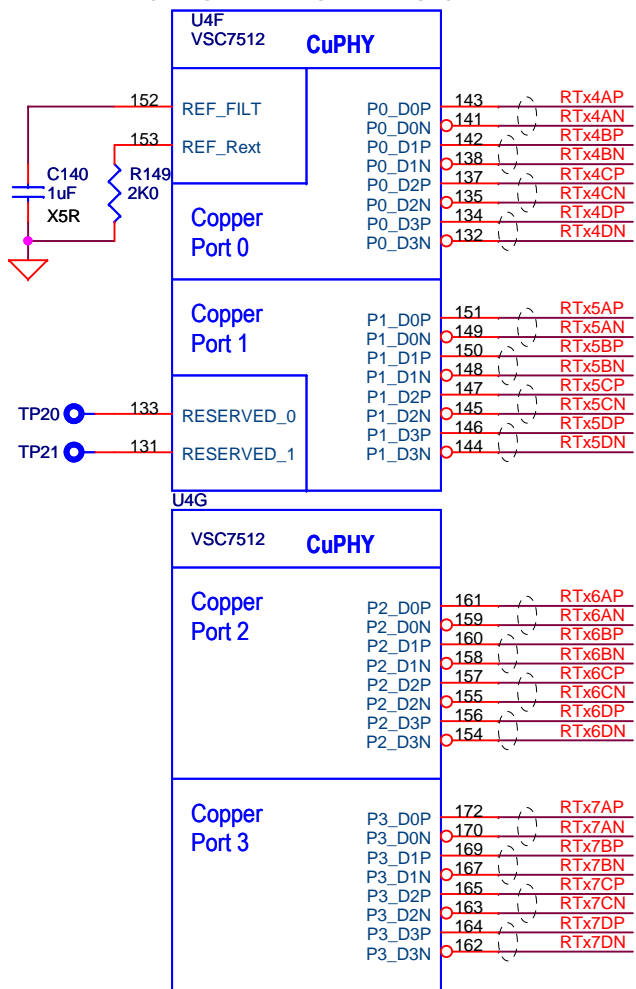
Title: Power inlet, voltage conversion, VSCxxxx power/decoup, reset

Size: A3 Document Number: PCB121 Rev: 02-00

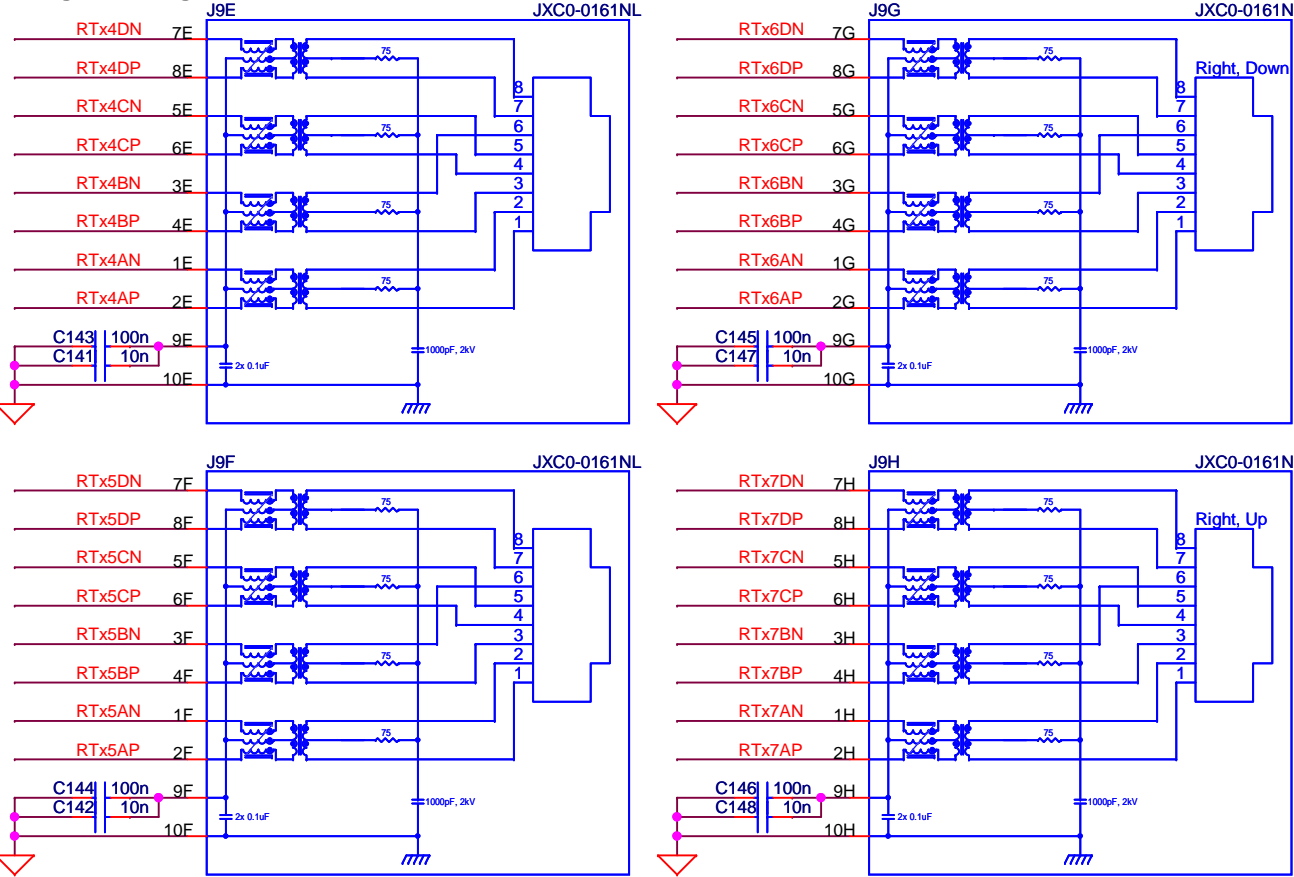
Date: Thursday, August 11, 2016 Sheet: 2 of 6



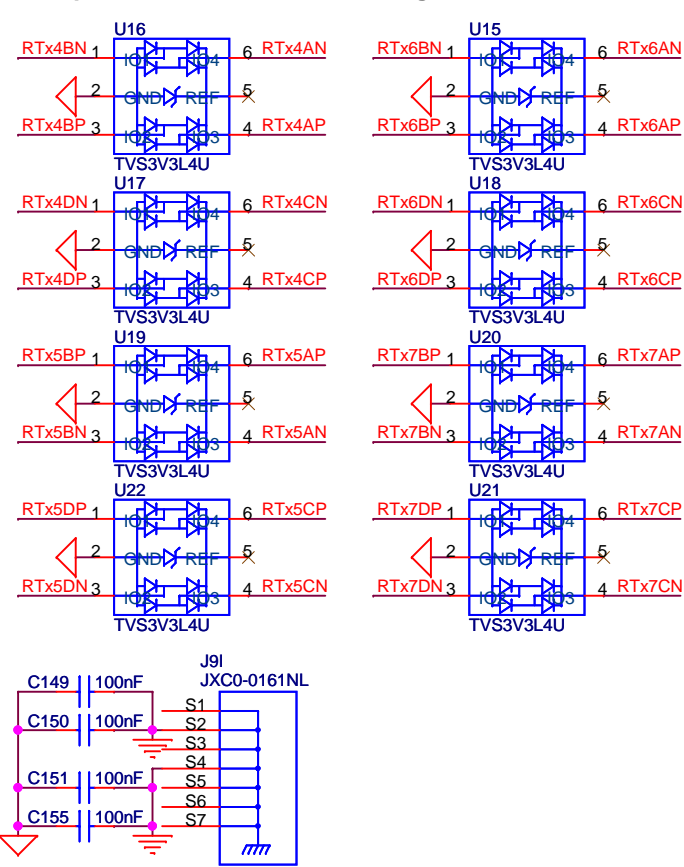
RJ45[8:5] (1Gbps/100Mbps/10Mbps)



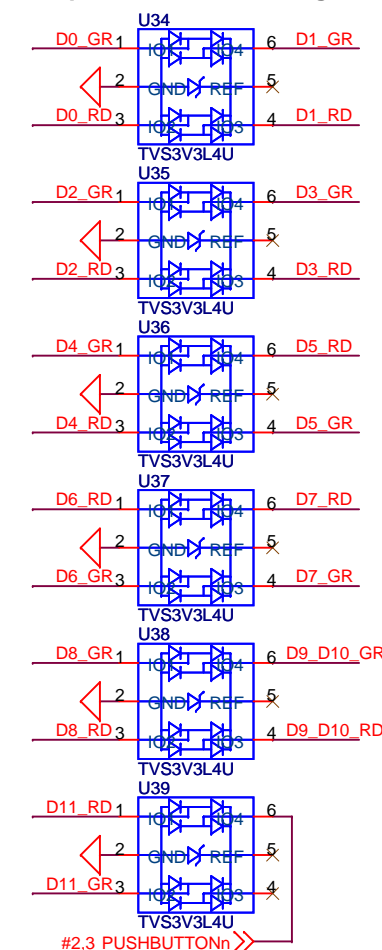
Integrated magnetics



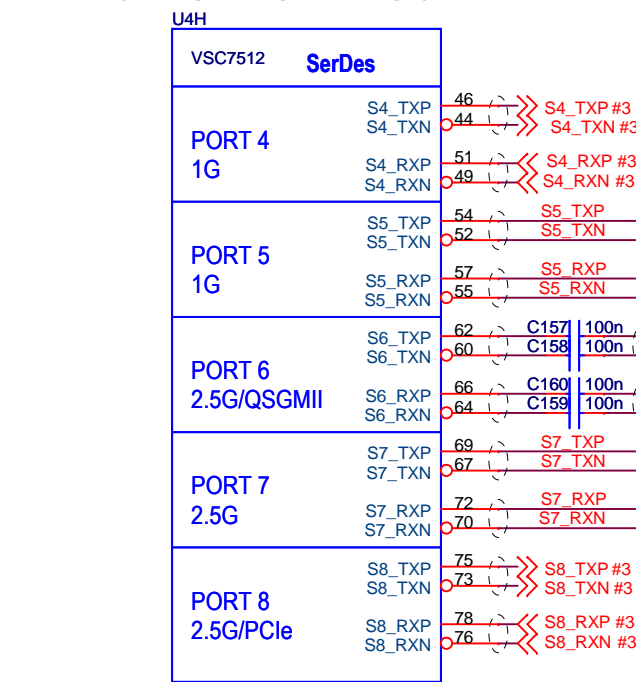
TVS protection on 1000BASE-T signals



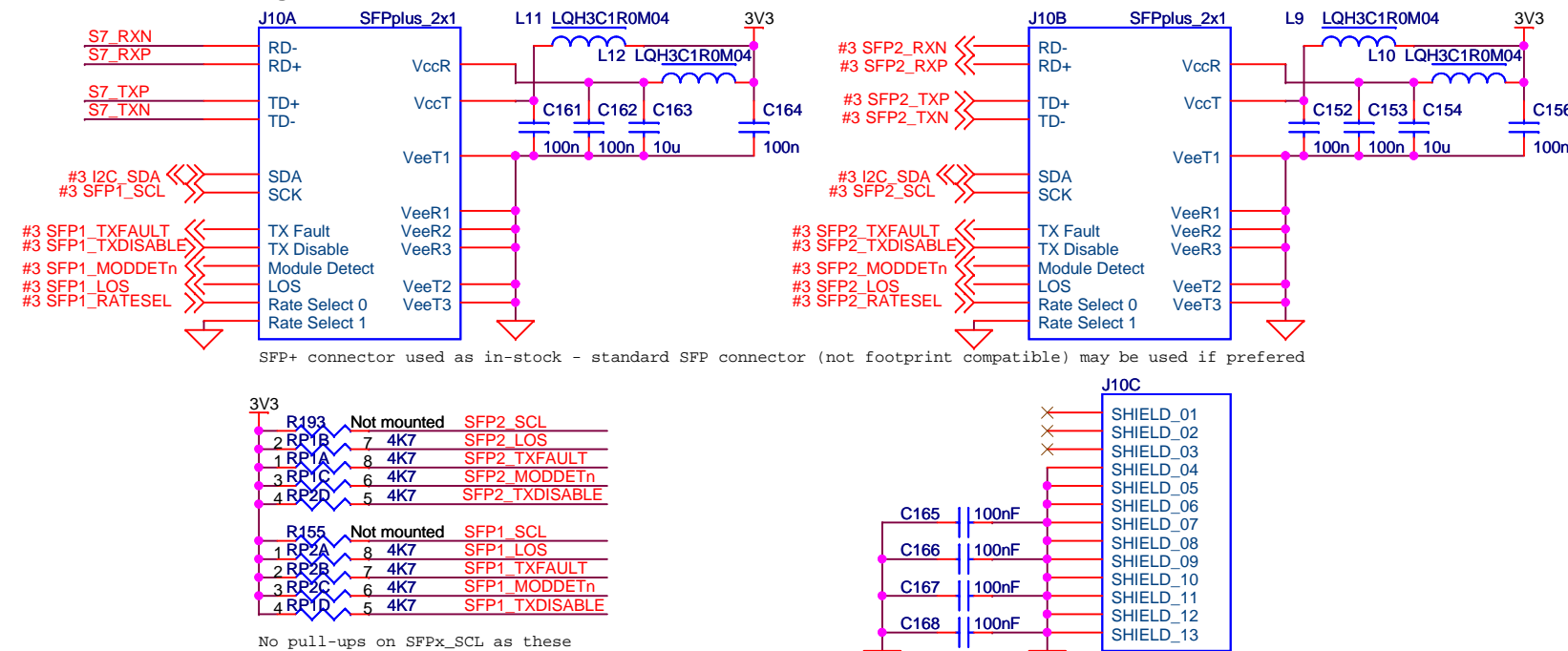
TVS protection on LED signals



SFP[2:1] (2.5Gbps/1Gbps/100Mbps)



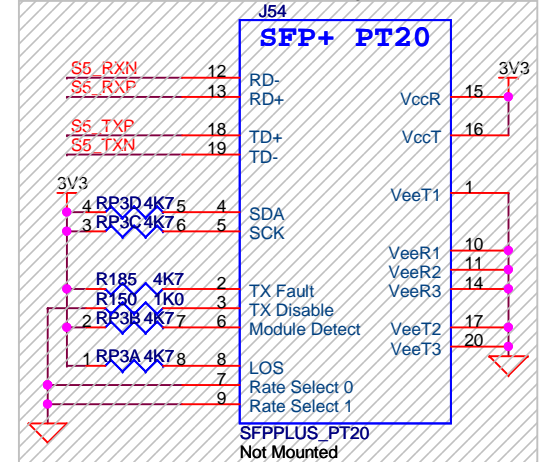
SFP connectors and cage



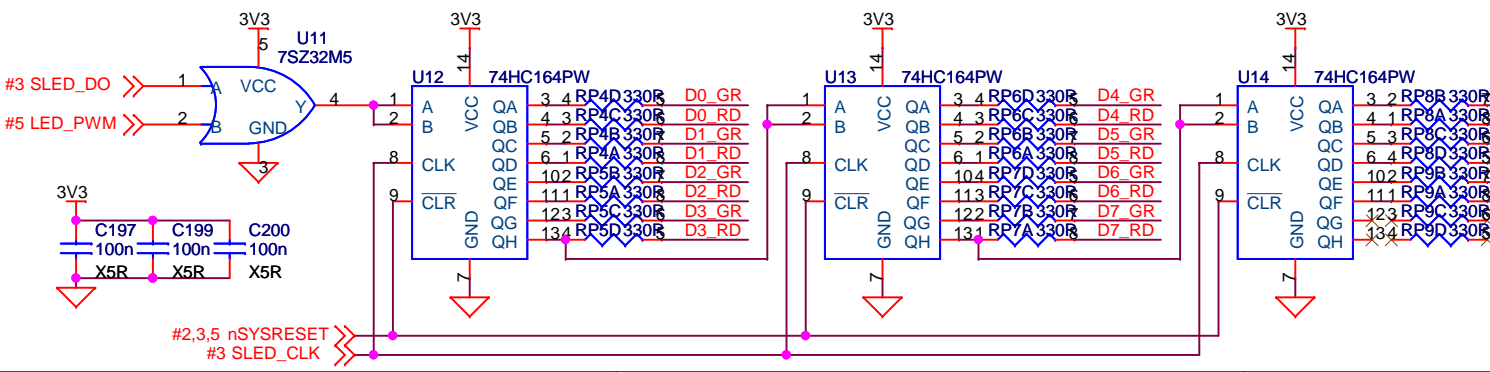
SERDES usage:

- S5 only used for test
- S6 connects to VSC8514 through QSGMII
- S7 (2.5Gbps) connects to SFP1
- Config 0: S4 (1Gbps) connects to NPI on breakoff and S8 (2.5Gbps) connects to SFP2 through breakoff
- Config c: S4 (1Gbps) connects to SFP2 through breakoff and S8 (2.5Gbps) connects to PCIe on breakoff board

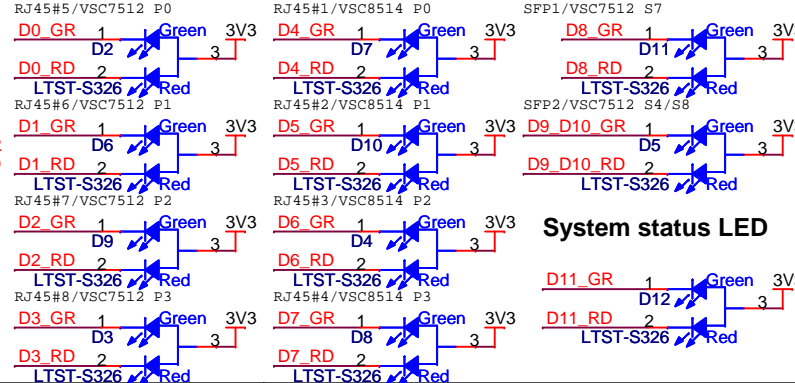
"SFP" connector for test only



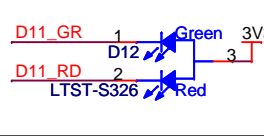
Serial LED outputs



Port status LEDs



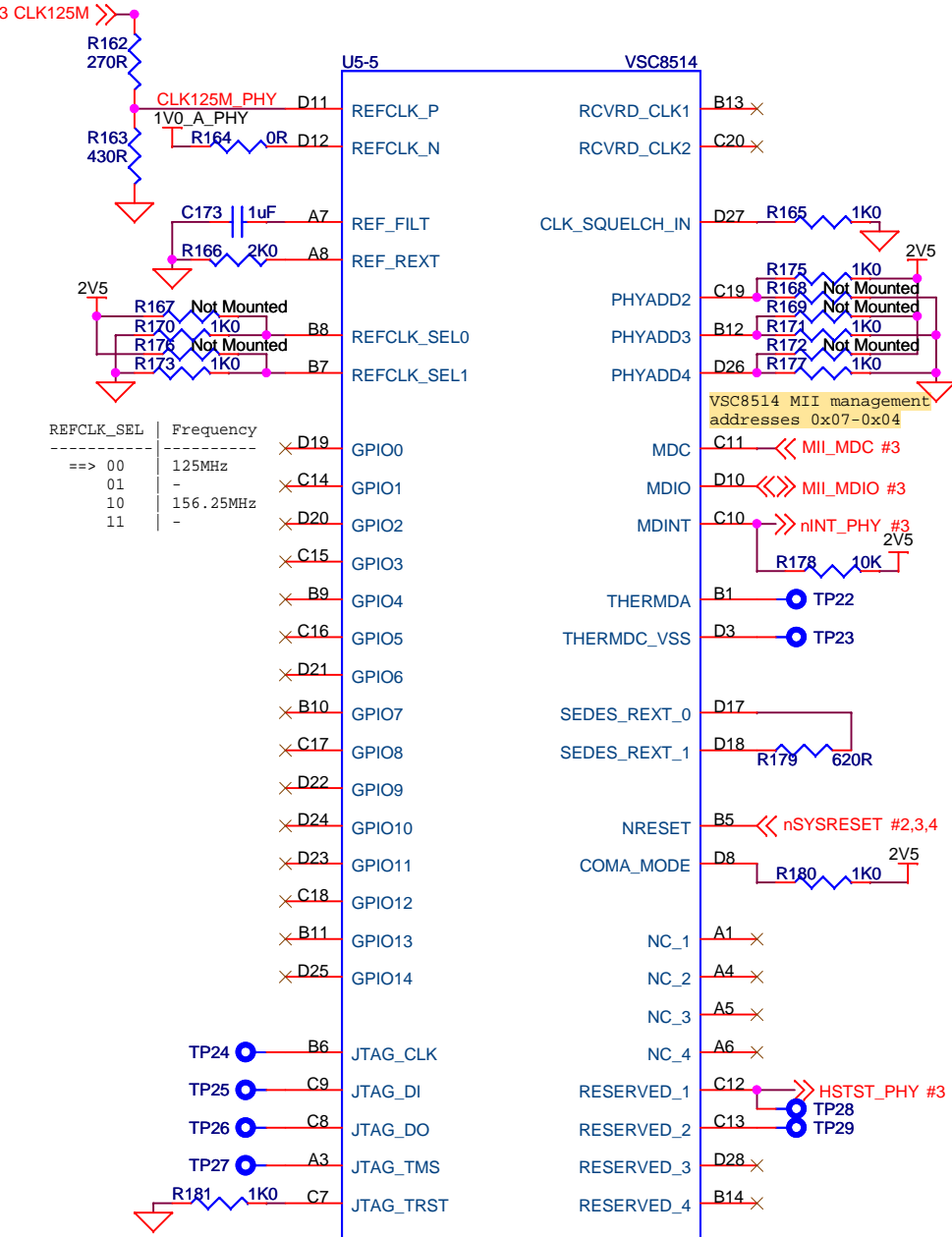
System status LED



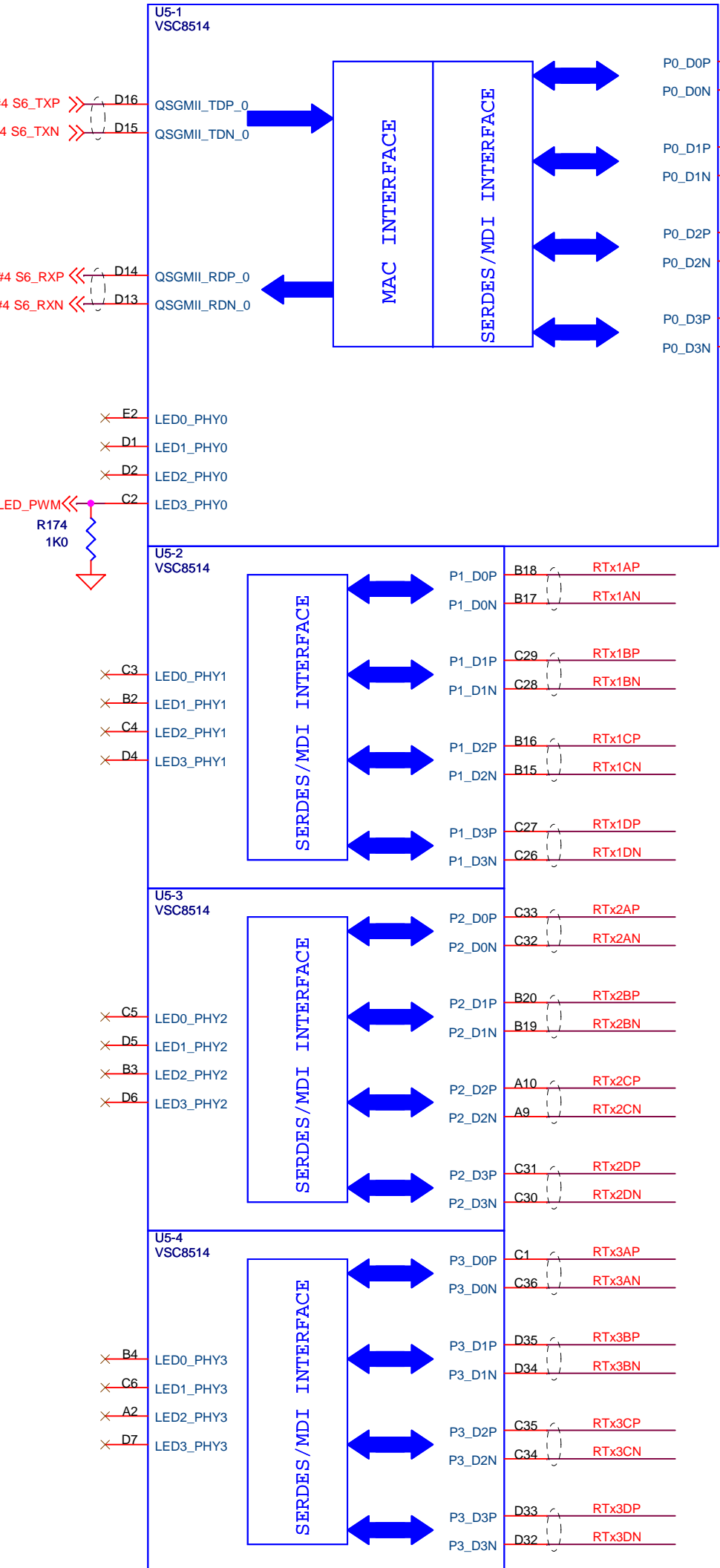
Enable SLED ports 7:0 as port status LEDs for 8x RJ45 ports (SLED port 0 is VSC7512 P0/RJ45#5, SLED port 4 is VSC8514 P0/RJ45#1, etc.). SLED port 8 as LED for SFP1 through S7, SLED port 9 as LED for 1G SFP2 through S4 (config c/PCIe only), SLED port 10 as LED for 2.5G SFP2 through S8 (config 0 only), SLED port 11 as system status LED

Enable two bits per port, bit[1:0]=00 => yellow, 01 => red, 10 => green, 11 => off.

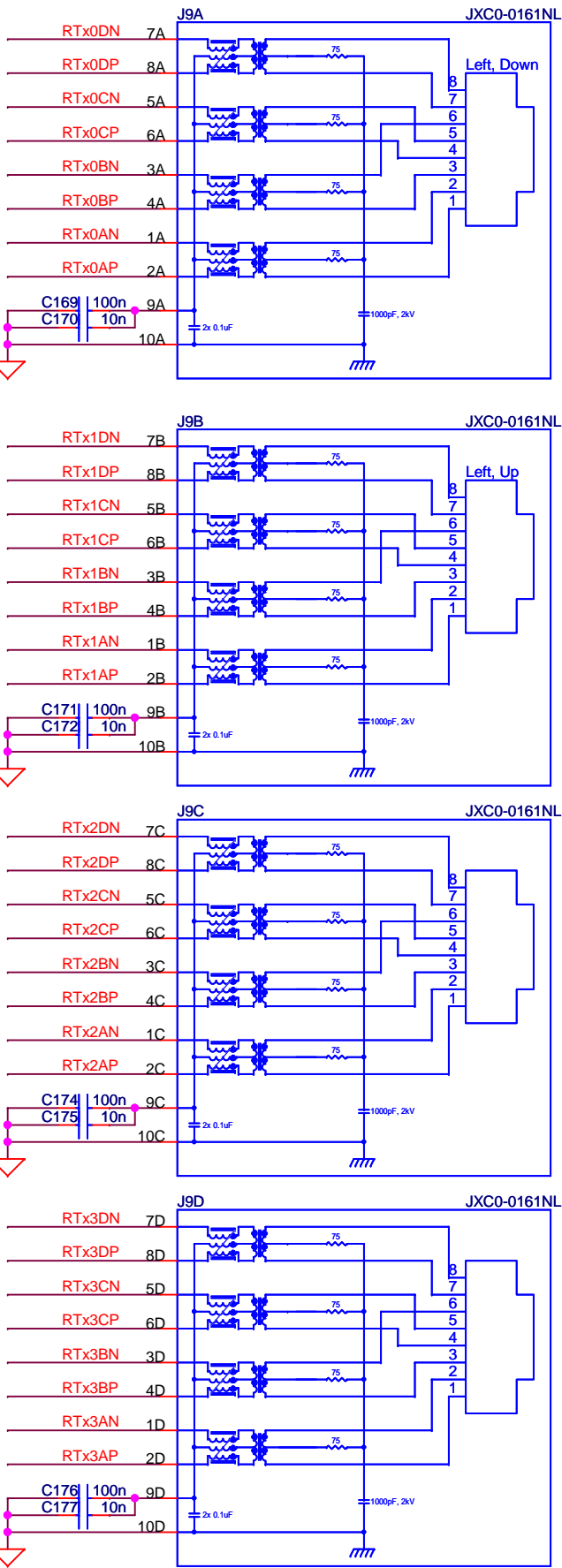
VSC8514 I/O and strapping



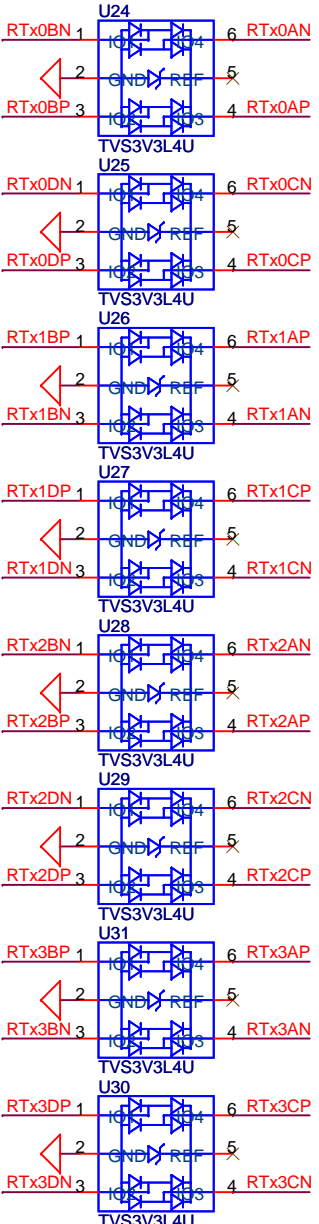
VSC8514 QSGMII/ports



Integrated magnetics

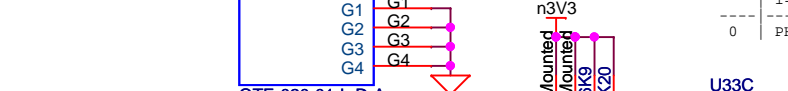
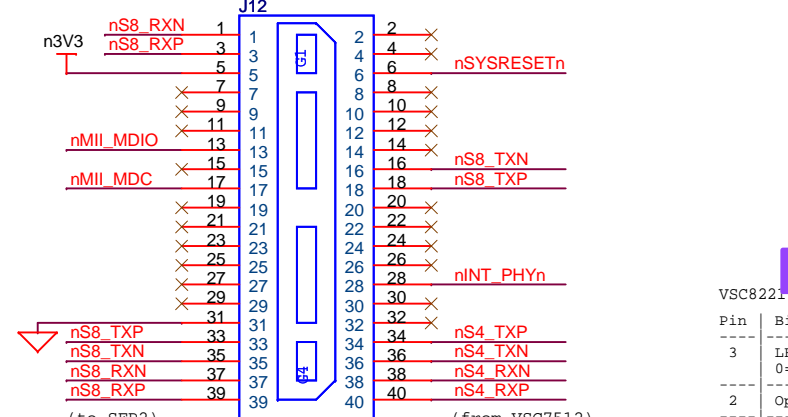


TVS protection

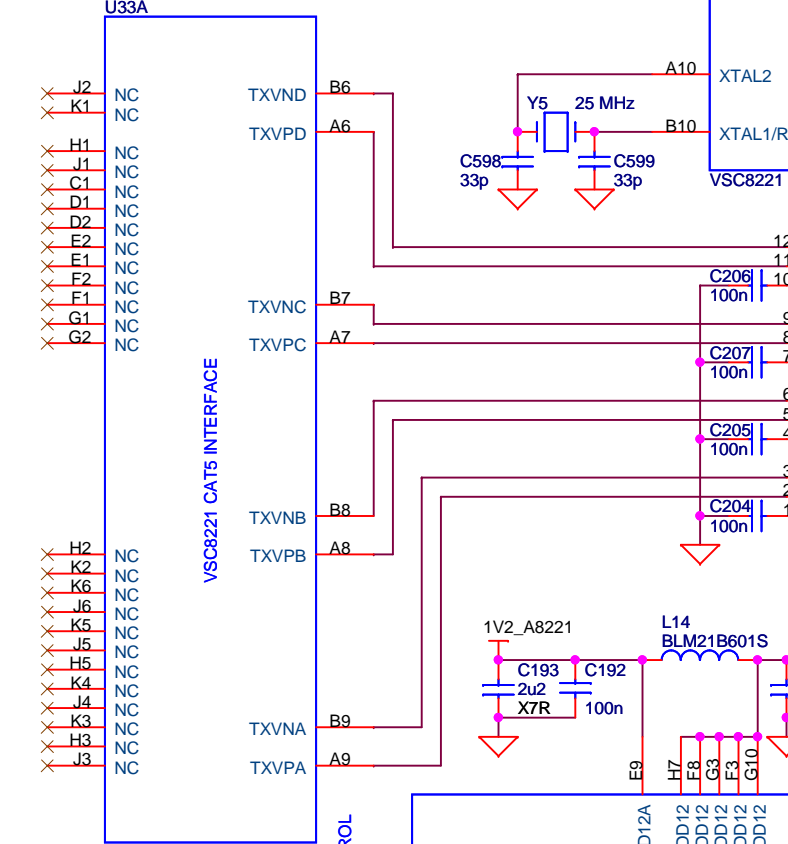
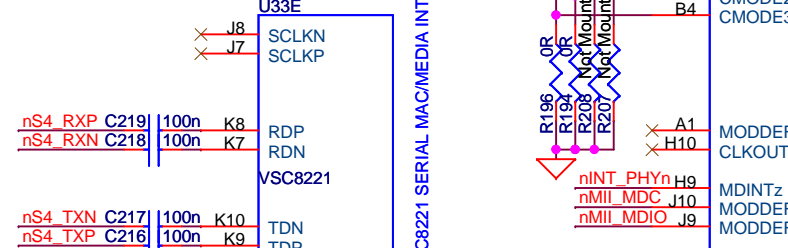


[illegible]

Samtec connector towards mainboard feedthrough of S8 to SFP2



USC9221 NDT single DIV 195 195 200 200 A5 34025

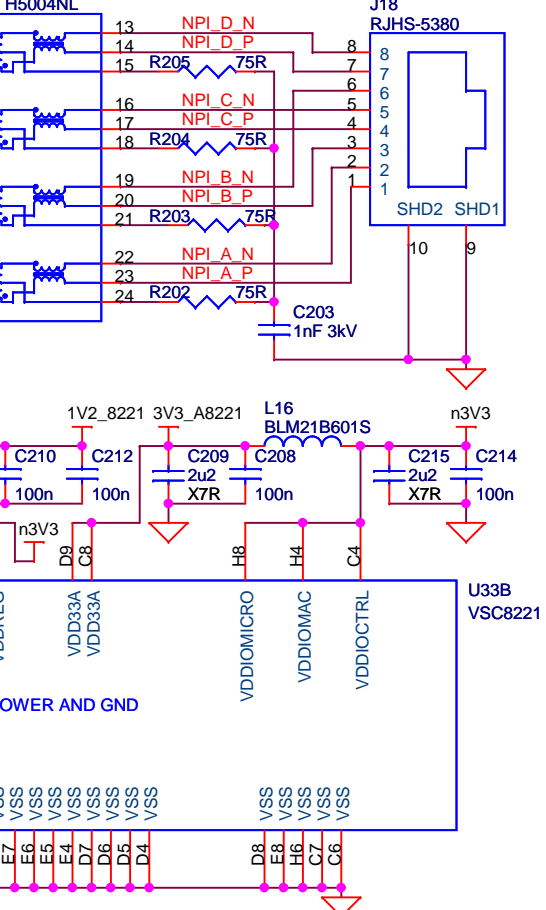
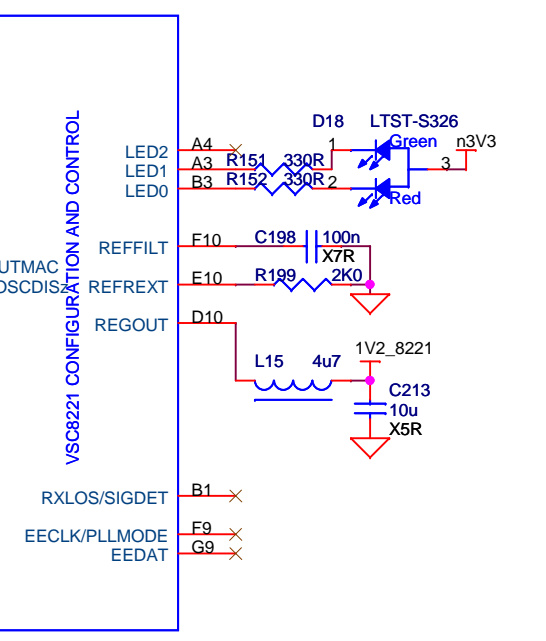


With CMODE	with 1%	Set bit	Set bit	Set bit	Set bit
0	0	0	0	0	0
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9
10	10	10	10	10	10
11	11	11	11	11	11
12	12	12	12	12	12
13	13	13	13	13	13
14	14	14	14	14	14
15	15	15	15	15	15

	GND	0	0	0	0	0
	GND	2.26k	0	0	0	1
	GND	4.02k	0	0	1	0
	GND	5.90k	0	0	1	1
	GND	8.25k	0	1	0	0
	GND	12.1k	0	1	0	1
	GND	16.9k	0	1	1	0
	GND	22.6k	0	1	1	1
	3V3	0	1	0	0	0
	3V3	2.26k	1	0	0	1
	3V3	4.02k	1	0	1	0
	3V3	5.90k	1	0	1	1
	3V3	8.25k	1	1	0	0
	3V3	12.1k	1	1	0	1
	3V3	16.9k	1	1	1	0

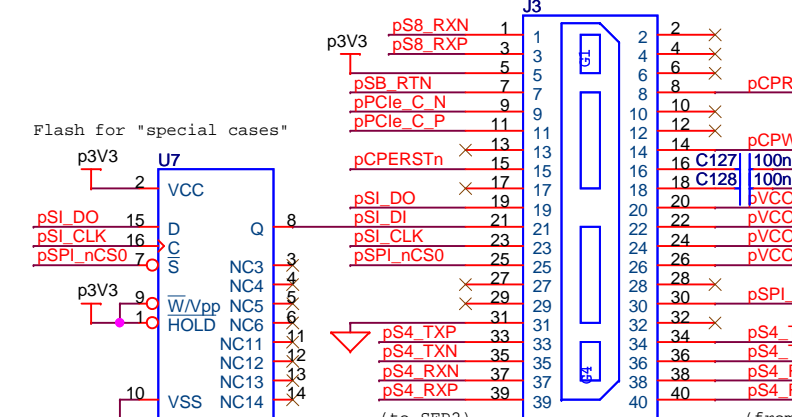
[illegible]

Bit 2 control	Bit 1 control	Bit 0 (LSB) control
SQE enable	Reserved	Autoneg ctrl[1]
0=>SQE disabled	-	0=>10/100/1000Base
mode	3:0], 0000=>SERDES to CAT5, SCLK	disabled
PHY address[4]	SIGDET direct	Line impedance
1	1=>Output	0=>50R

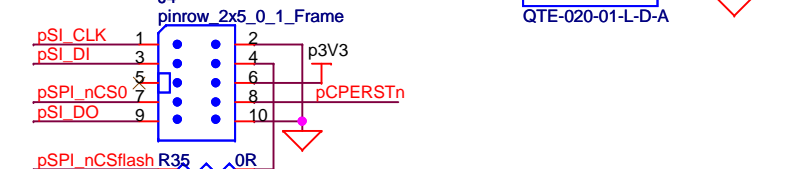


2	3
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Samtec connector towards mainboard feedthrough of S4 to



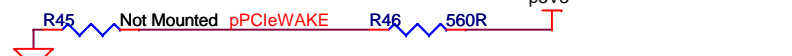
Programming header for Flash



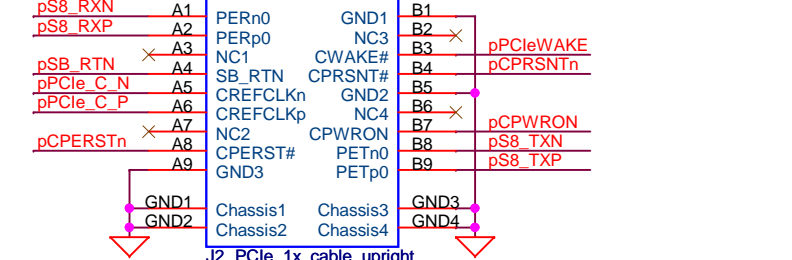
Override VCOFE GEC of mainboard for plug&play PCIe

R25	Not Mounted	pVCORE_CFG3	R26	560R
R27	560R	pVCORE_CFG2	R28	Not Mounted
R29	560R	pVCORE_CFG1	R30	Not Mounted
R31	Not Mounted	pVCORE_CFG0	R32	560R
R33	Not Mounted	pSPLnCFGnB	R34	Not Mounted

No PCIeWAKE from this mainboard (use in-band beacon instead)



PCIE 1x cable connector for S8 from mainboard



Note, PCIe interface for use in controlled lab environment, so

- (1) no power domain isolation,
- (2) high-impedance when powered off not guaranteed for CWAKE#, CPRSNT#, CPERST#
- (3) spread spectrum clocked PCIe hosts not supported

