KSZ9477 EVB/Demo Board with Atmel SAMA5D3 SoC

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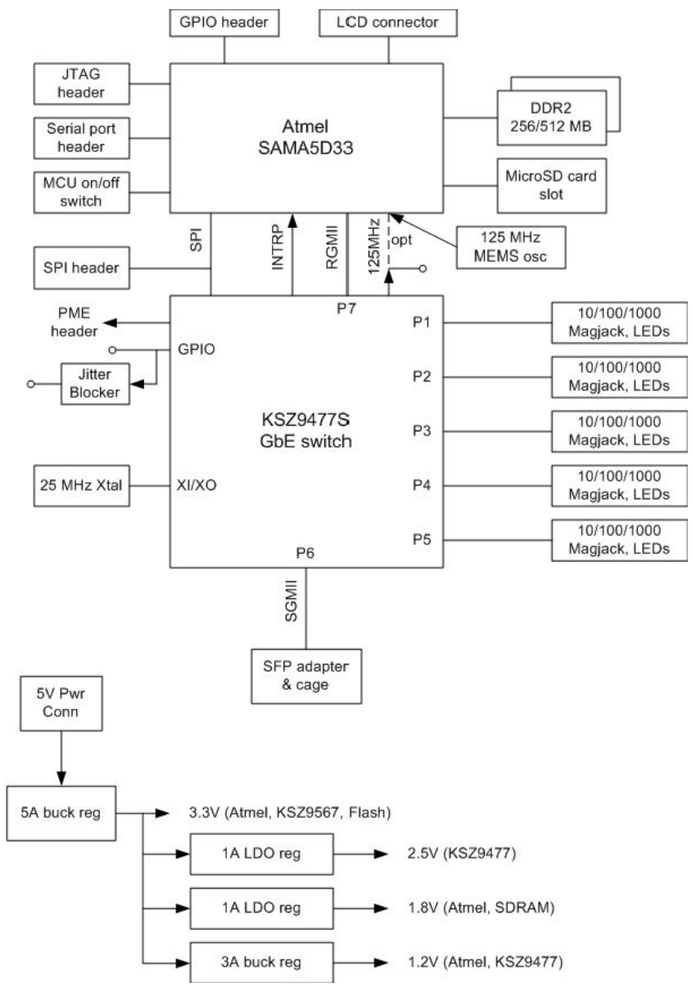
Revision History

Revision	Date	Revision Summary	Author
A00	6/23/2016	Pre-release	Kelly Maas
B	12/15/2016	Release	Kelly Maas
B1	3/9/2017	Update KSZ9477 SGMII pin names, update notes	Kelly Maas

Block Diagram



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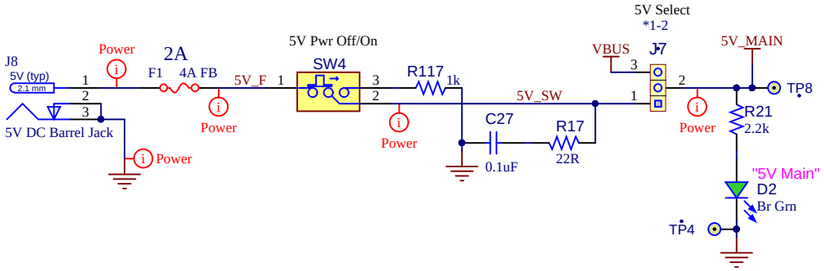
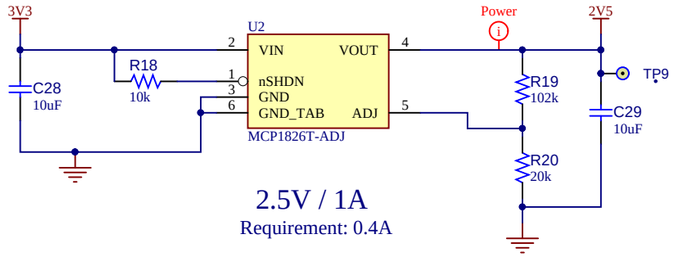
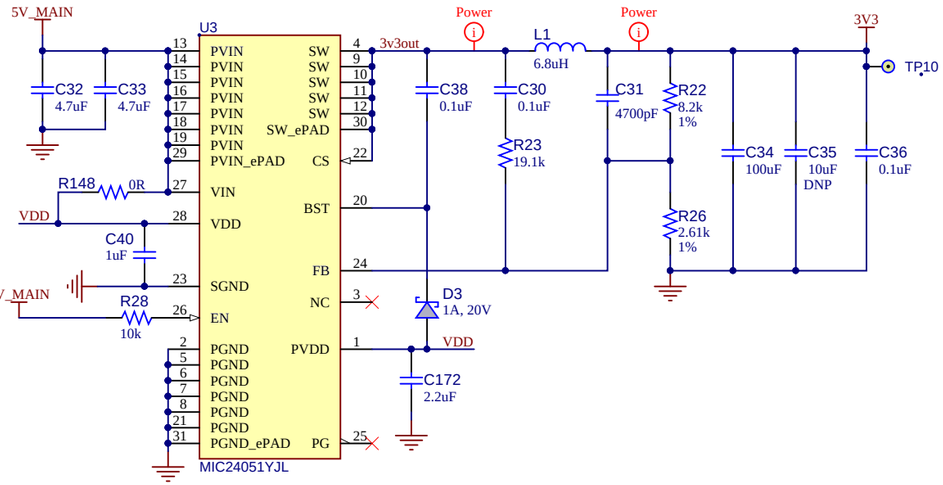
Description: KSZ9477 EVB_Demo Board with SAMA5D3 SoC			
Page Title: Title Page			
Project Name: KSZ9477 EVB_Demo		PN: UNG_8071	
Size: B	Date: 3/30/2017	Designer: Kelly Maas	Sheet 1 of 8	Rev B1

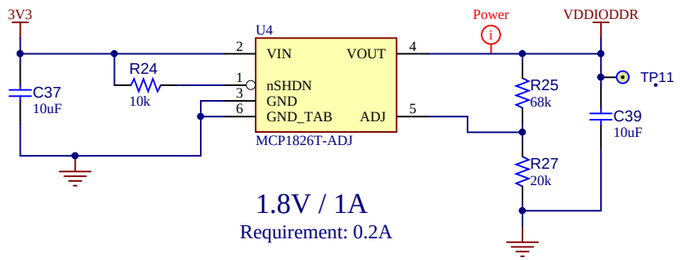




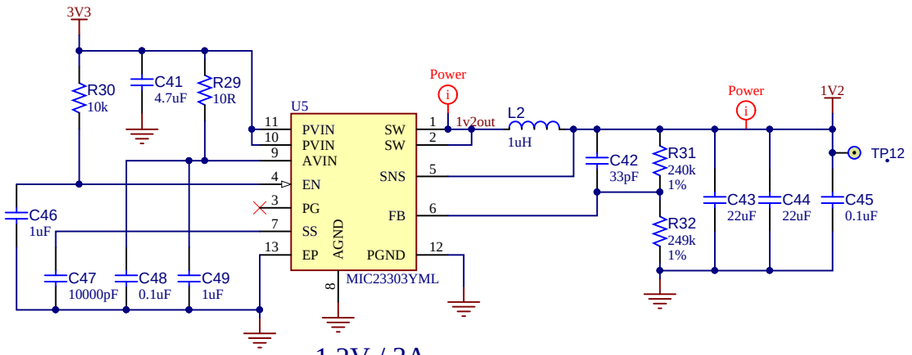
2.5V / 1A
Requirement: 0.4A



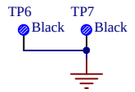
3.3V / 6A
Requirement: 2A



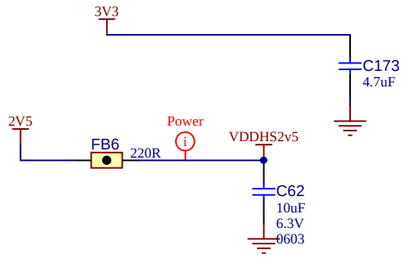
1.8V / 1A
Requirement: 0.2A

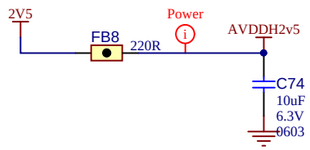


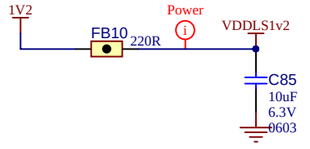
1.2V / 3A
Requirement: 1.6A

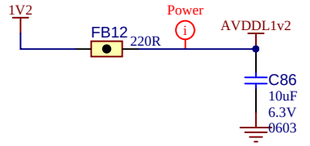


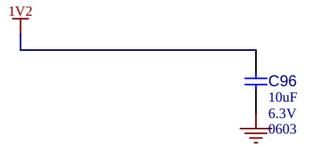
MICROCHIP	Microchip Technology, Inc. USB/Network Group - UNG www.Microchip.com	Designed with Altium Altium.com	
Description: KSZ9477 EVB_Demo Board with SAMA5D3 SoC			
Page Title: Board Power I/O and Regulators			
Project Name: KSZ9477 EVB_Demo		PN: UNG_8071	
Size: B	Date: 12/16/2016	Designer: Kelly Maas	Sheet 2 of 8	Rev B1

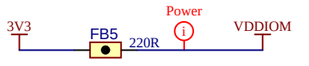


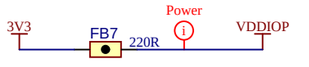


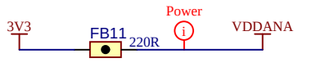


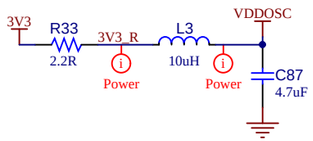


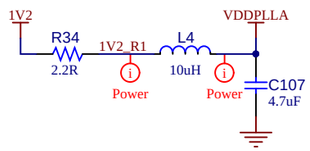


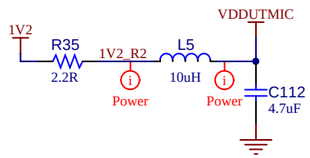


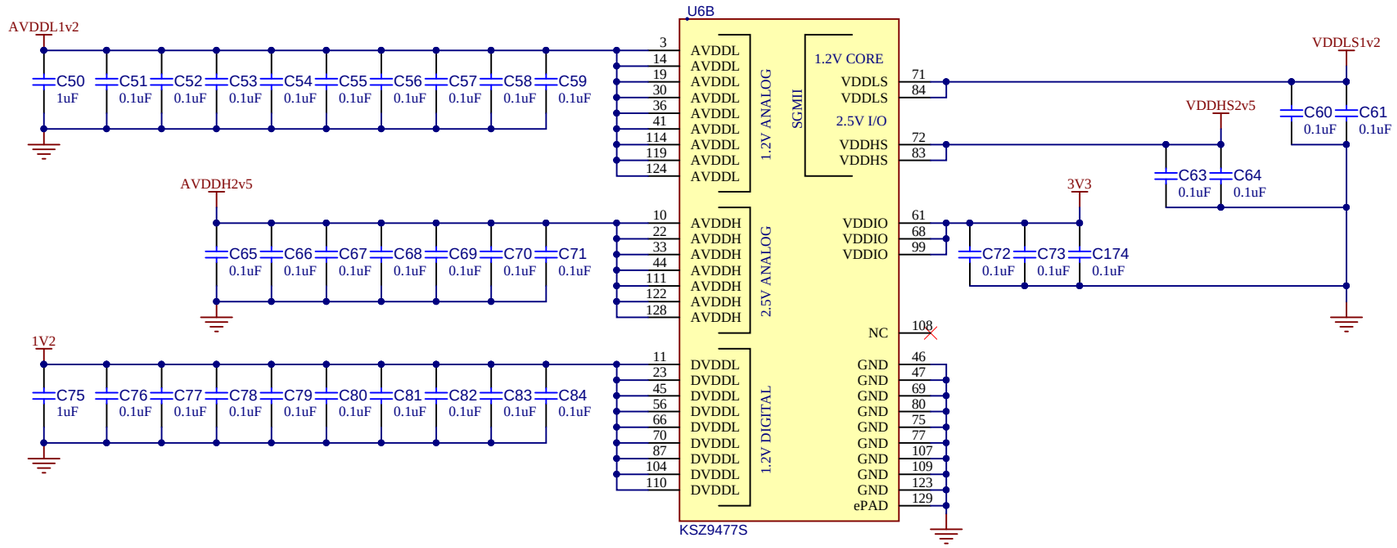


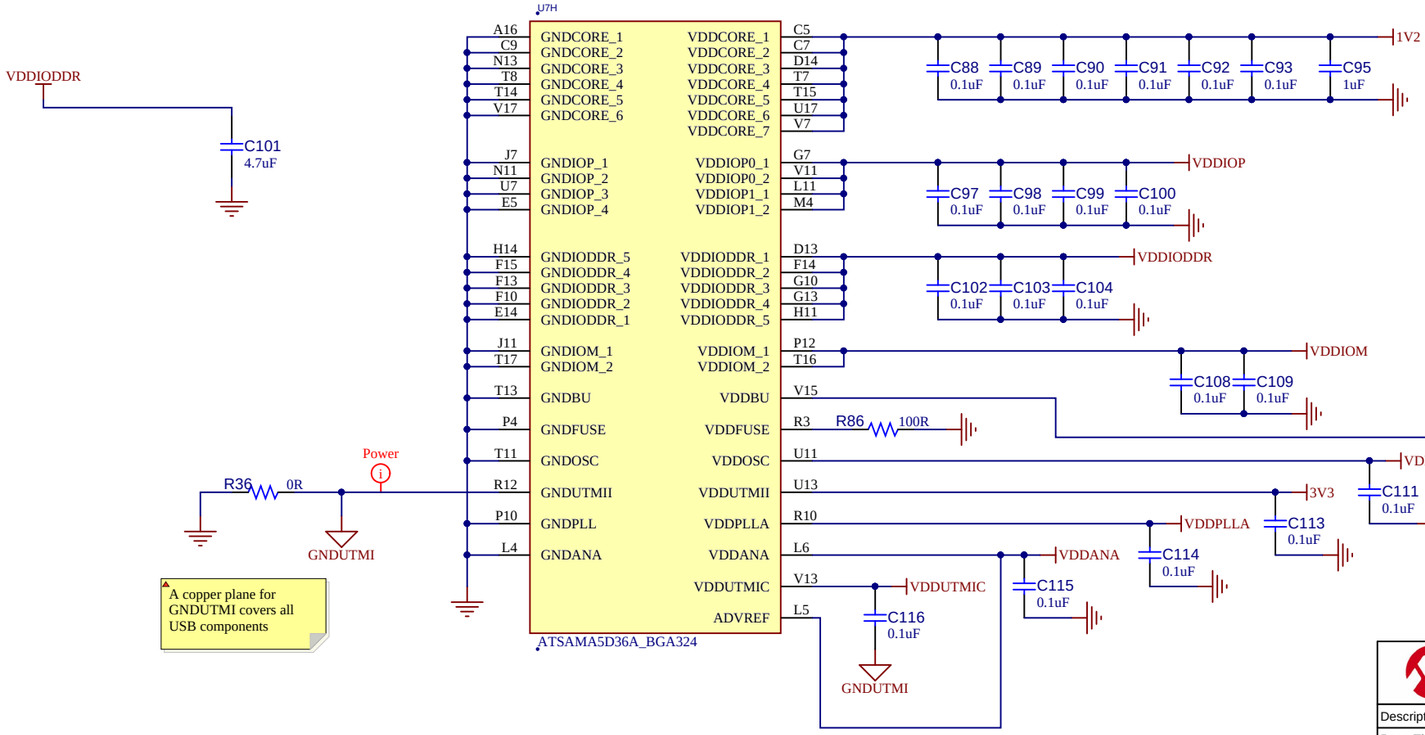












A copper plane for GNDUTMI covers all USB components

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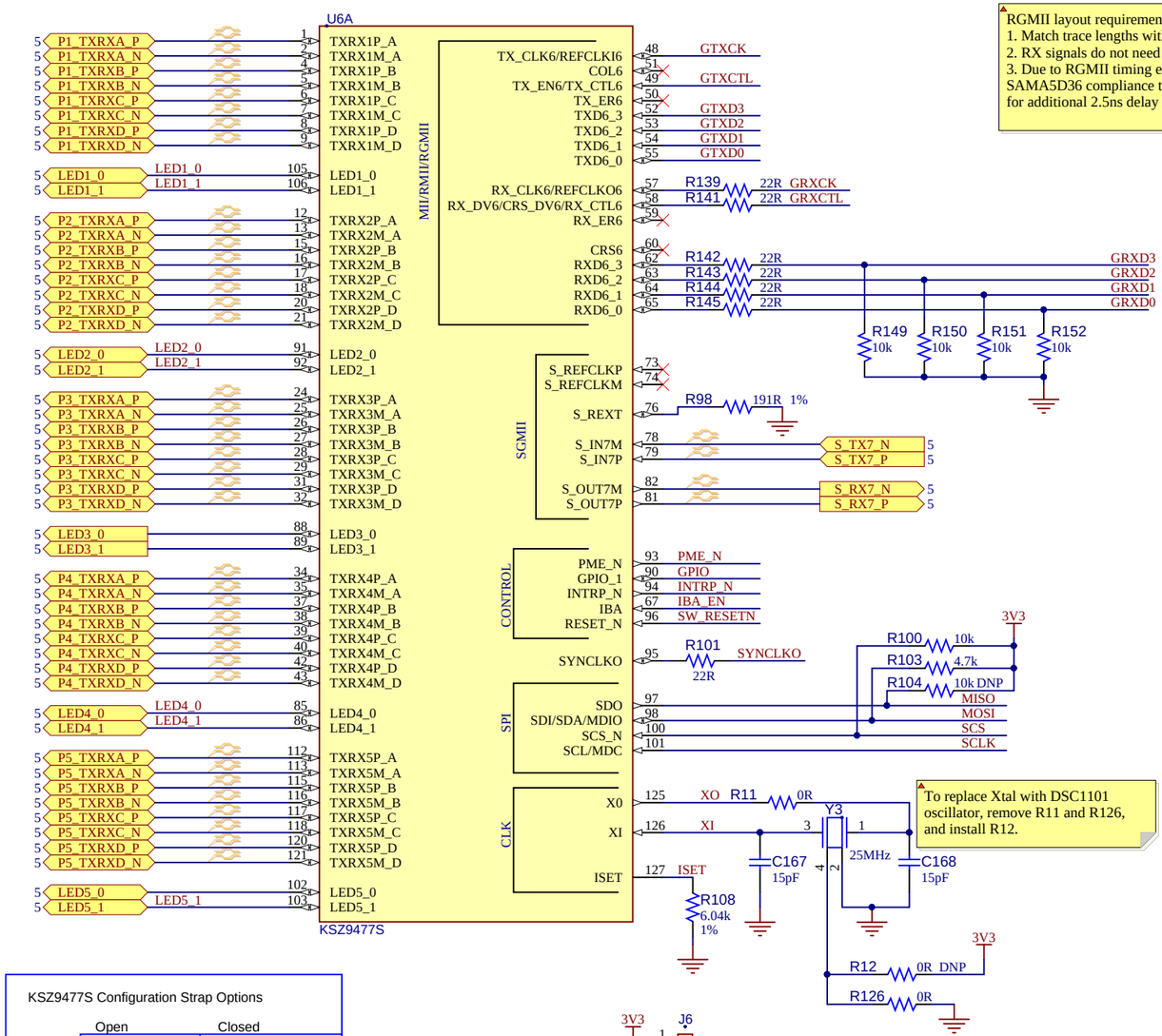
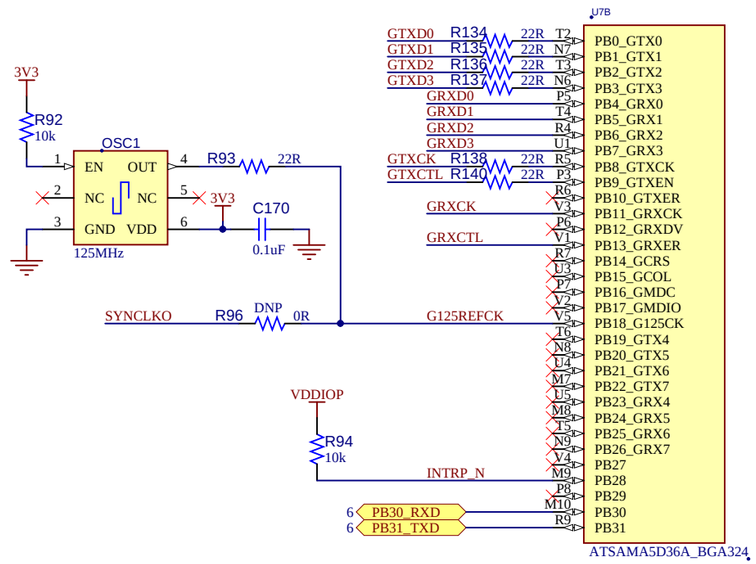
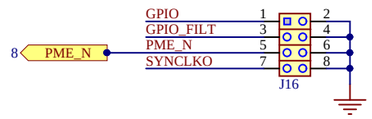
Page Title: Power connections for switch and SoC			
Project Name: KSZ9477 EVB_Demo		PN: UNG_8071	
Size: B	Date: 12/9/2016	Designer: Kelly Maas	Sheet 3 of 8 Rev B1

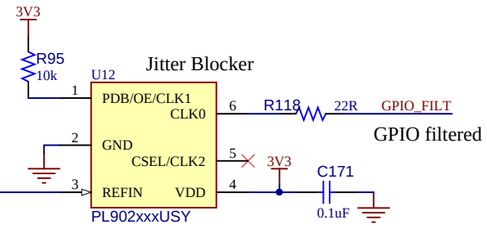


RGMII layout requirements
1. Match trace lengths within 10 to 100 mils.
2. RX signals do not need to be length match to TX signals.
3. Due to RGMII timing error in port 6 of KSZ9477, plus SAMA5D36 compliance to RGMII v1.3, GTXCK must be routed for additional 2.5ns delay relative to GTXD[3:0] and GTXCTL.

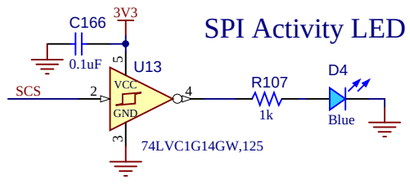


KSZ9477 Output Header

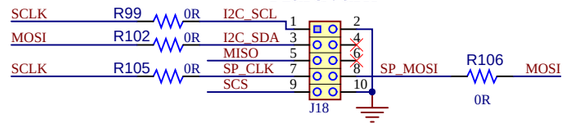




SPI Activity LED



SPI / I2C Aardvark

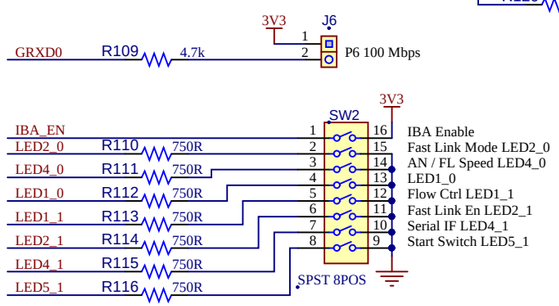


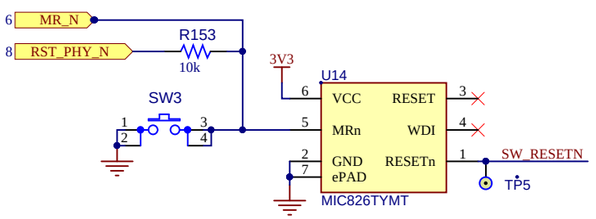
KSZ9477S Configuration Strap Options

	Open	Closed
GRXD0	RGMII: 1000 Mb/s	RGMII: 100 Mb/s
LED2_0	1000B-T master or 10/100 MDI	1000B-T slave or 10/100 MDI-X
LED4_0	Enable AN or 100B-TX	Disable AN or 1000B-T
LED1_0	Quiet-WIRE off	Quiet-WIRE on
LED1_1	Flow control on	Flow control off
LED2_1	Normal link up	Fast link up
LED4_1	SPI	I2C
LED5_1	Start switch	Don't start switch
IBA	IBA off	IBA enabled

No option:
LED3_1 No option for MDC/MDIO
RXD6_[3:2] Port 6 fixed as RGMII
RXD6_1 Not relevant when port is RGMII
SYNCLKO S_REFCLKP/M input clock not used

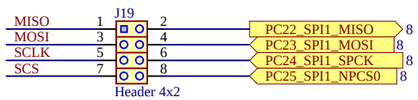
KSZ9477 Configuration Strap Options





KSZ9477 Reset
200ms delay

MCU SPI



Install all 4 jumpers at J19 for MCU to control KSZ9477 via SPI.
Remove all jumpers at J19 when connecting external SPI or I2C controller to header J18.

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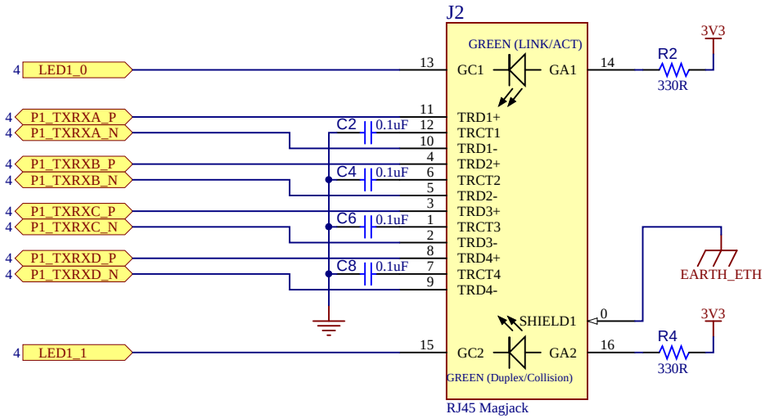
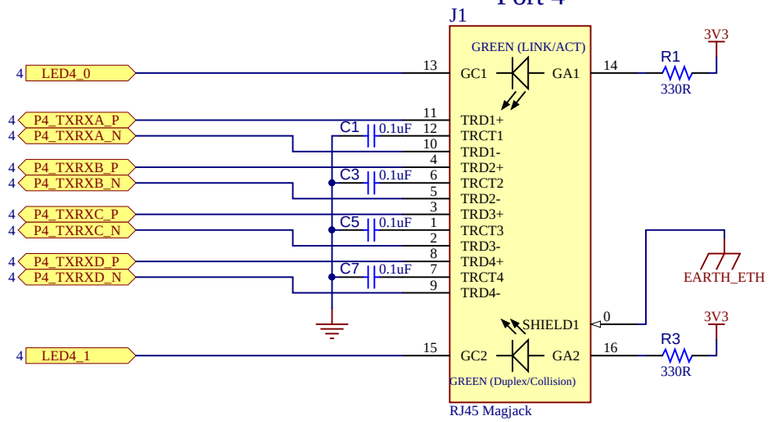
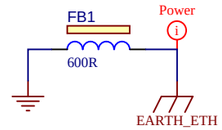
Page Title: KSZ9477, RGMII to SAMA5D3			
Project Name: KSZ9477 EVB_Demo		PN: UNG_8071	
Size: B	Date: 3/9/2017	Designer: Kelly Maas	Sheet 4 of 8 Rev B1

Port 1



Port 4





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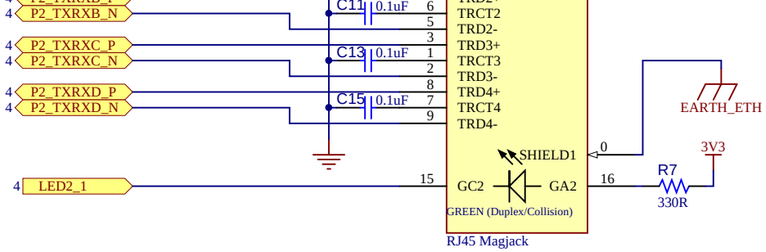
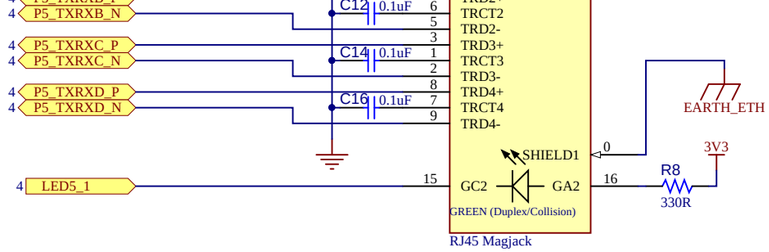
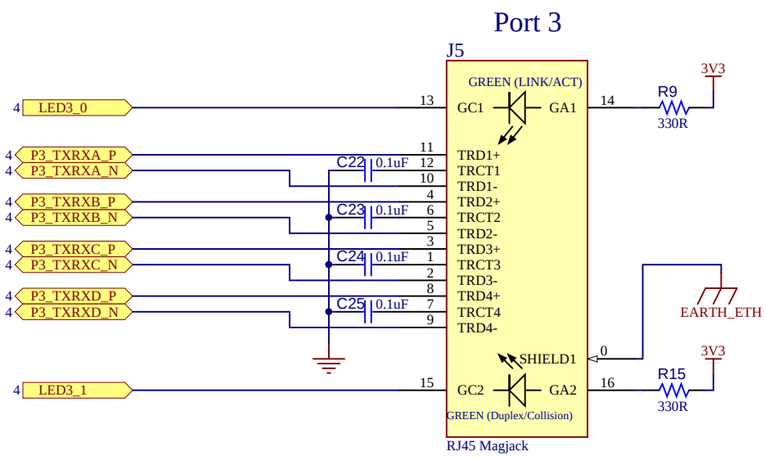
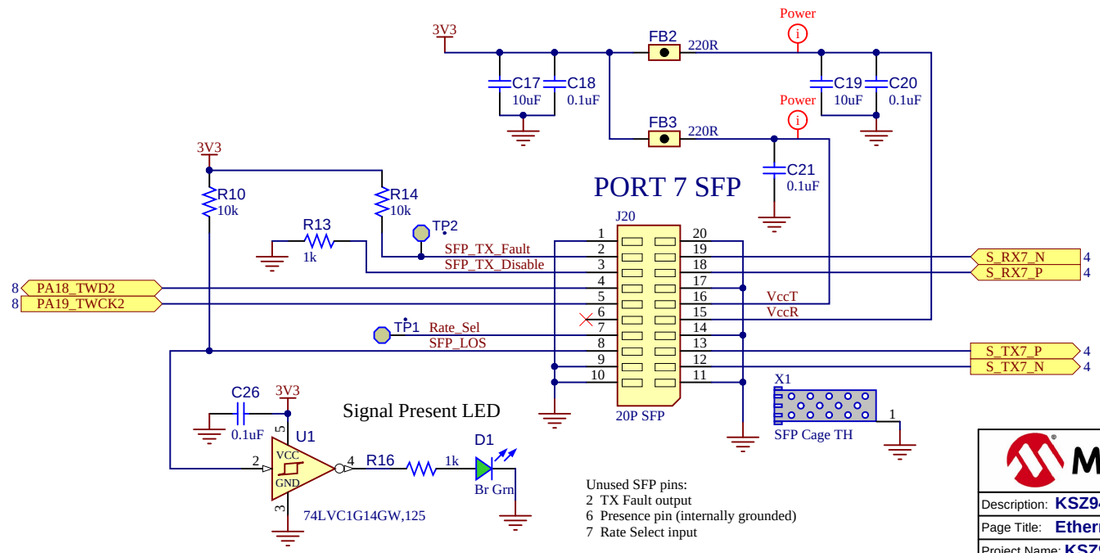


Port 5



Port 3





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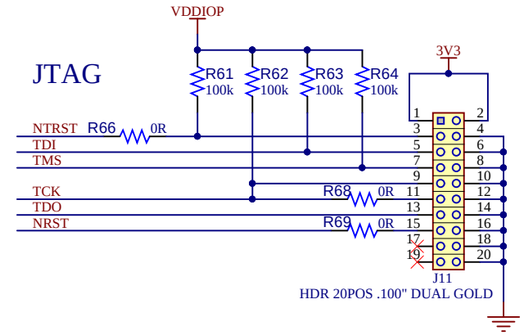
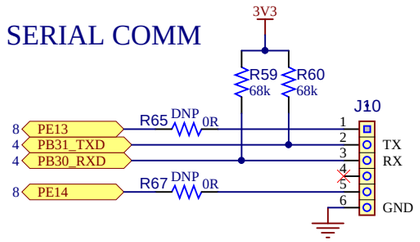
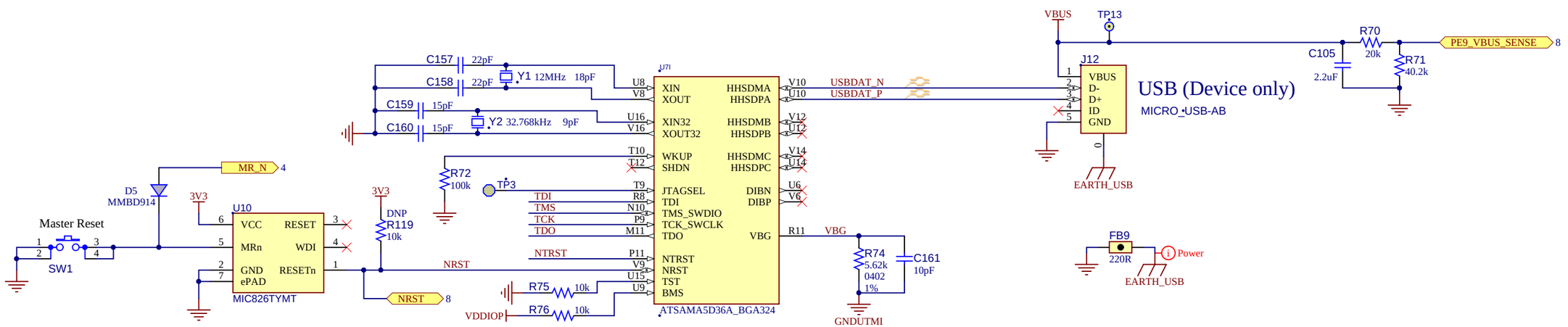
Description: KSZ9477 EVB_Demo Board with SAMA5D3 SoC			
Page Title: Ethernet ports and SGMII SFP			
Project Name: KSZ9477 EVB_Demo		PN: UNG_8071	
Size: B	Date: 2/16/2017	Designer: Kelly Maas	Sheet 5 of 8 Rev B1

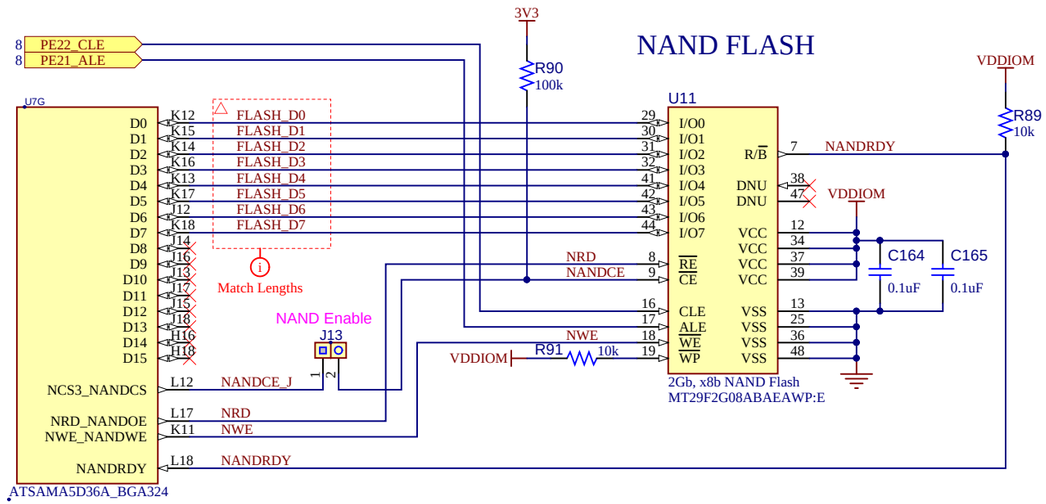


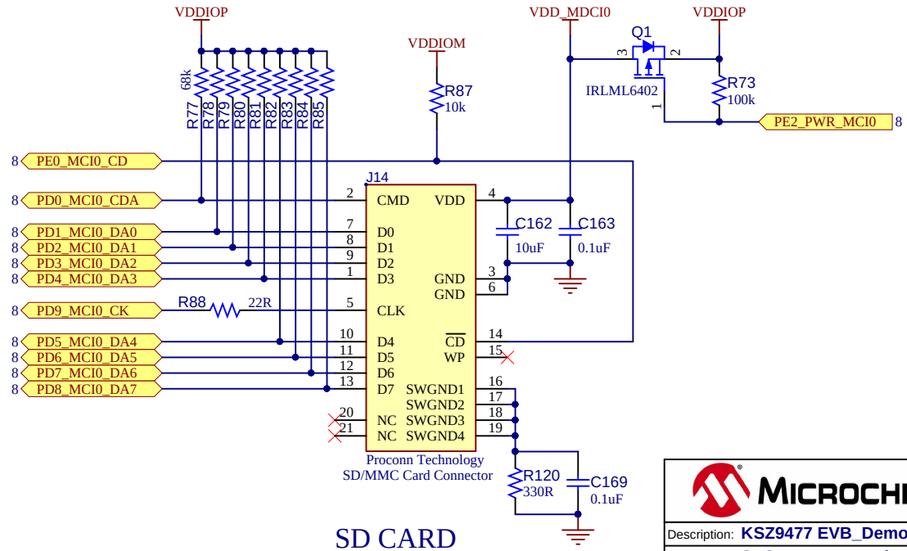


SAMA5D36 is not currently using pins 1 and 5 of J10



Reset / 200ms delay





SD CARD

Preferred location is bottom side of board

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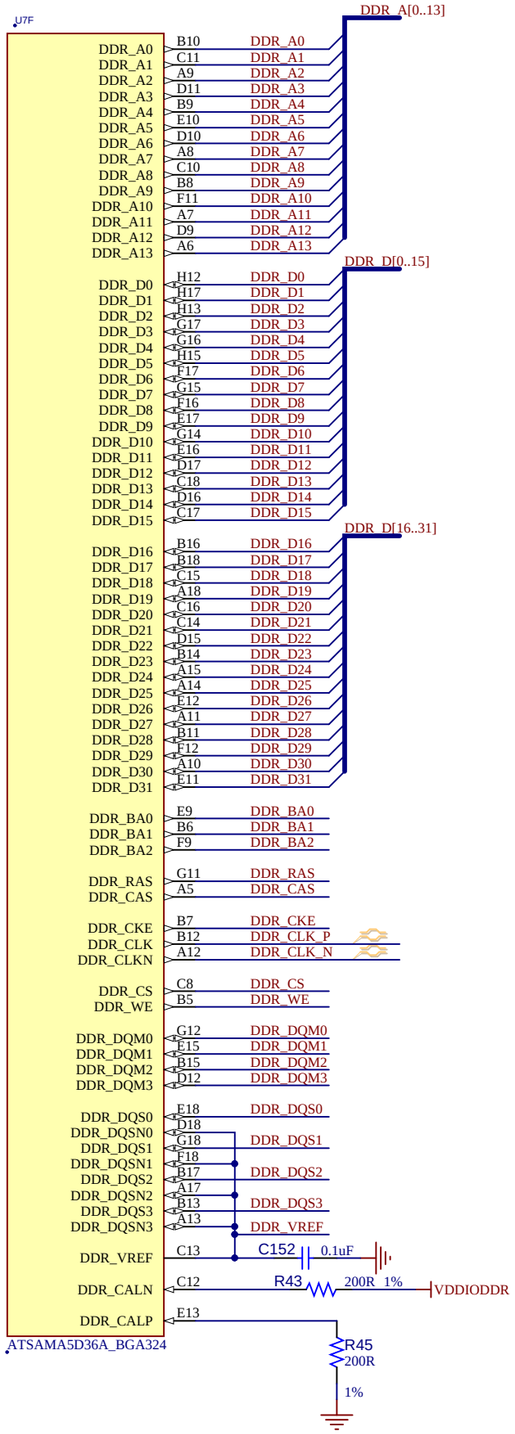
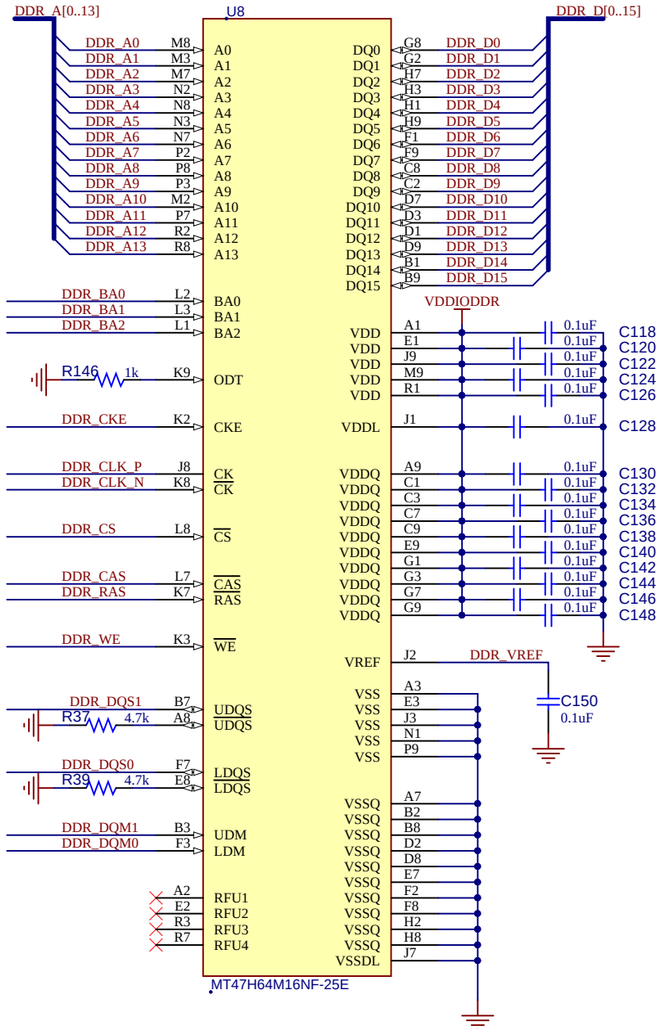
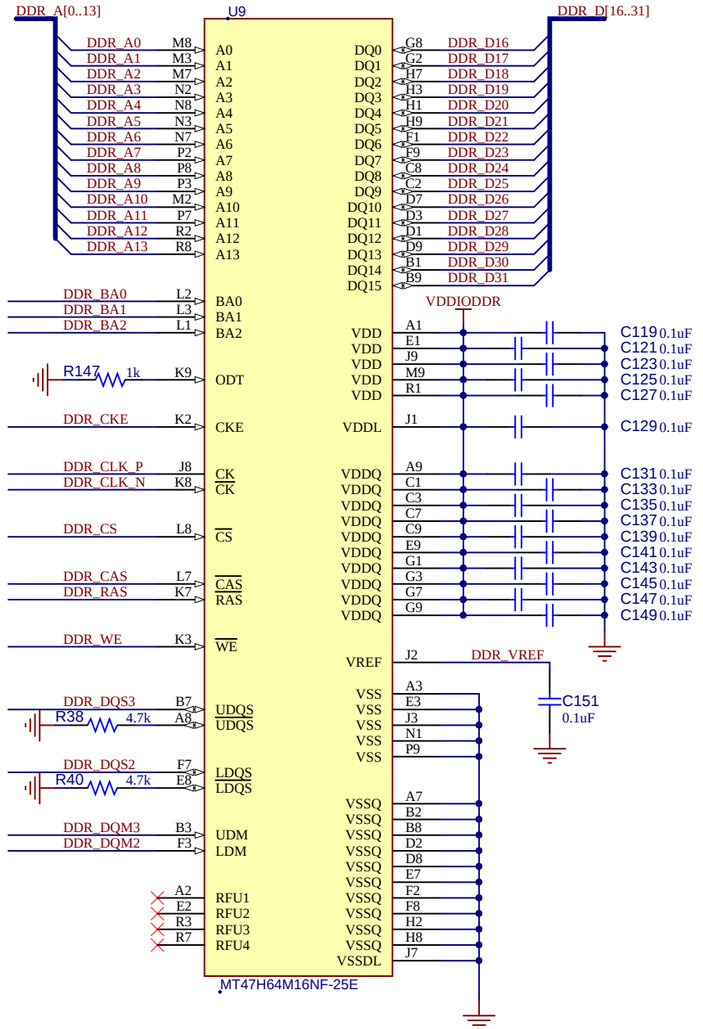
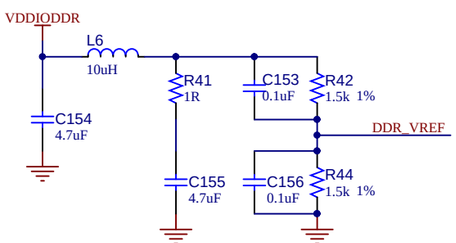
Page Title: SoC core connections, NAND Flash, SD Card	
Project Name: KSZ9477 EVB_Demo	PN: UNG_8071
Size: B Date: 3/9/2017 Designer: Kelly Maas	Sheet 6 of 8 Rev B1

DDR2 SDRAM









Keep nets as short as possible. Therefore DDR2 devices have to be placed as close as possible to SAMA5D3.
The layout EBI DDR2 should use controlled impedance traces of Z0= 50ohm.

Address, control and data traces may not exceed 1.3 inches (33mm).
Address, control and data traces must be length matched to within 0.1 inch (2.54mm).
Address, control and data traces must match the data group trace lengths to within 0.25 inch (6.35mm).

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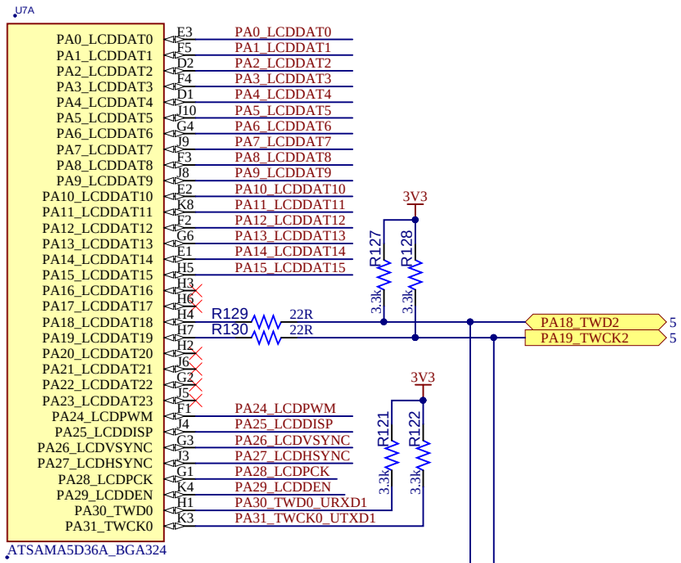
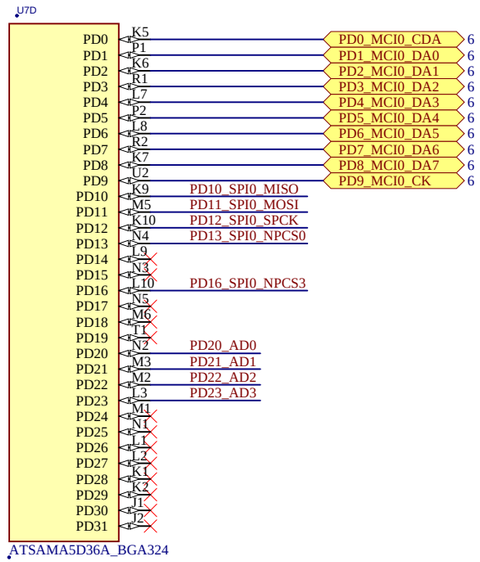
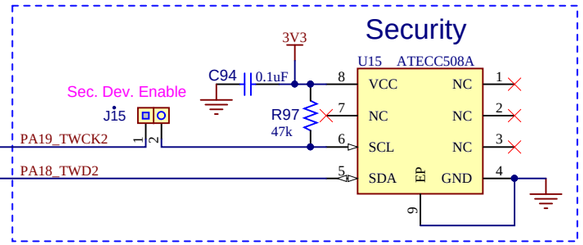
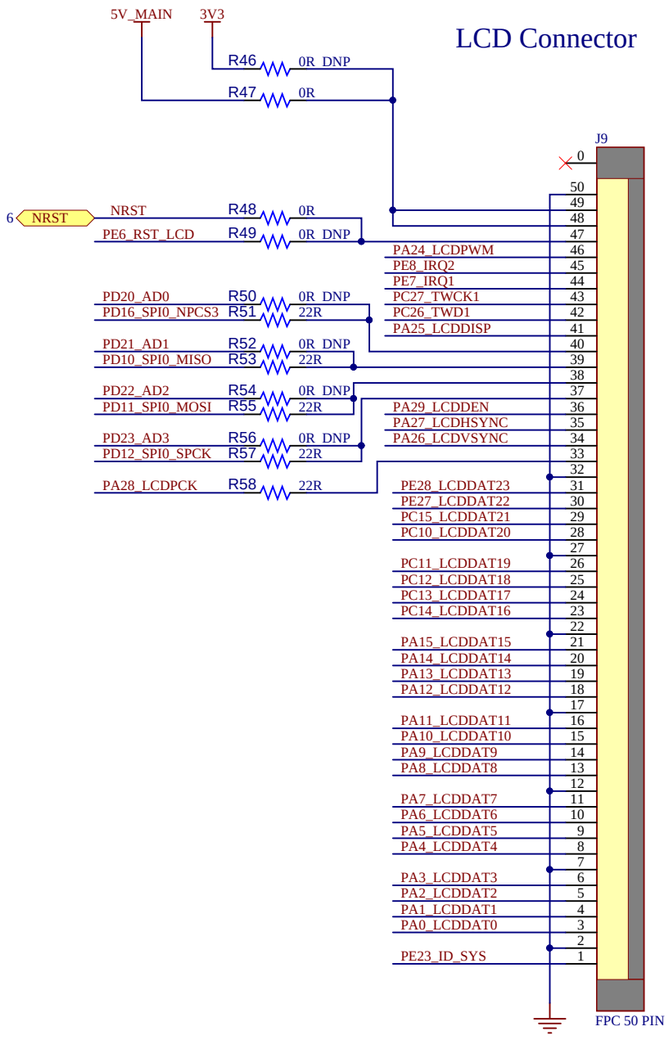
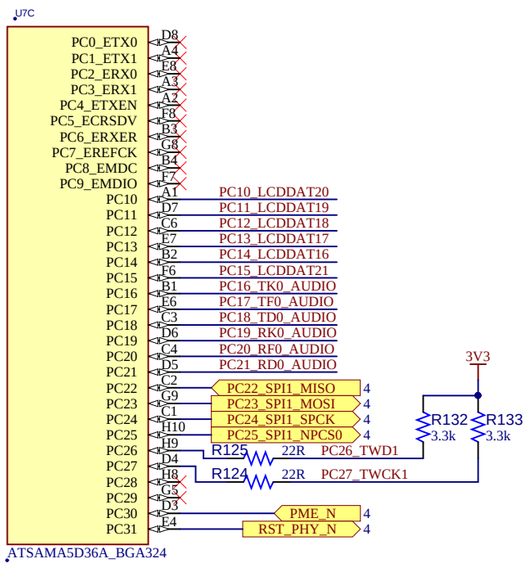
Project Name: KSZ9477 EVB_Demo		PN: UNG_8071	
Size: B	Date: 12/6/2016	Designer: Kelly Maas	Sheet 7 of 8	Rev B1

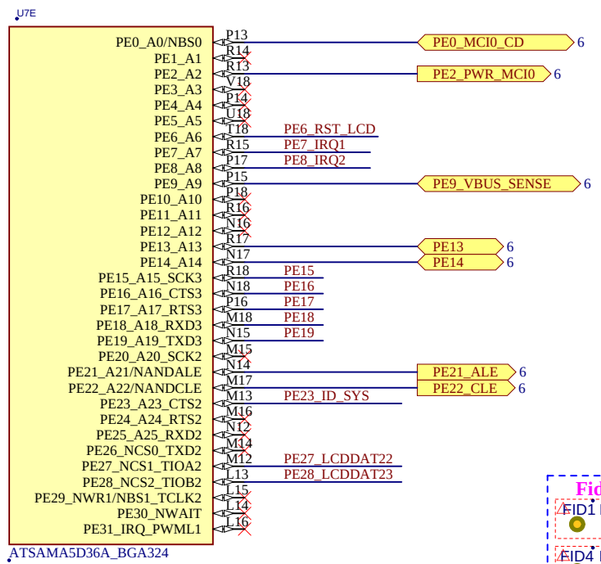


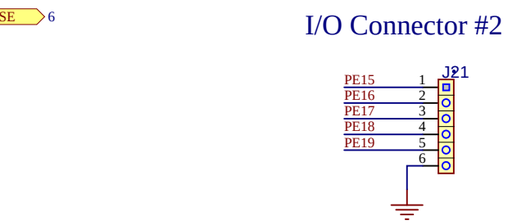


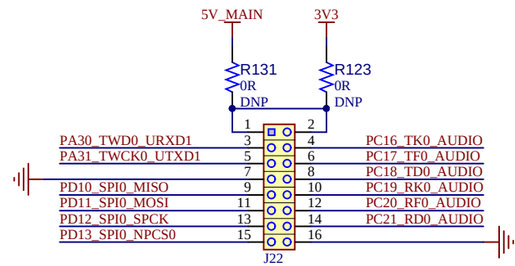


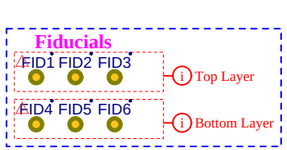


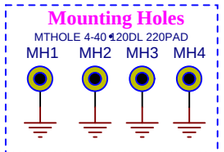












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Description:	KSZ9477 EVB_Demo Board with SAMA5D3 SoC		
Page Title:	SoC GPIO, LCD Connector, misc headers		
Project Name:	KSZ9477 EVB_Demo	PN:	UNG_8071
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