VSC7512

User Guide

VSC5634EV Hardware Manual

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Power Matters.™

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 01-02

Revision 01-02 updated chapter 8.5.

1.2 01-01

In revision 01-01 of this document, all references to Ferret (except in this line) have been changed to Ocelot.

1.3 01-00

Revision 01-00 was the first production-level publication of this document.

1.4 00-03

Revision 00-03 was the first publication of this document, for internal review.

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2 Introduction

This hardware manual describes the design of the VSC5634EV reference board, demonstrating the VSC7512 Ocelot Ethernet switch and VSC8514 Elise PHY devices.

2.1 Audience

The audience for this document is primarily hardware and software engineers that want to get an overview of designing products based on the VSC7512 device.

2.2 References

2.2.1 Microsemi documents

- VSC7512 product datasheet, http://www.microsemi.com/products/ethernet-solutions/ethernet-switches/vsc7512-10-port-layer-2-gigabit-ethernet-switch
- VSC8514 product datasheet, http://www.microsemi.com/products/ethernet-solutions/ethernet-phys/gigabit-ethernet-phys/vsc8514-quad-port-gigabit-copper-eee-phy-with-qsgmii-mac-to-phy-interface
- Serial GPIO user's guide, http://ethernet.microsemi.com/products/download.php?fid=4865&number=vsc7428
- VSC5634EV reference design hardware collateral, http://www.microsemi.com/products/ethernet-solutions/ethernet-switches/vsc7512-10-port-layer-2-gigabit-ethernet-switch

2.2.2 IEEE standards

- IEEE802.1D, Media Access Control Bridges
- IEEE802.1Q, Virtual Bridged Local Area Networks
- IEEE802.3, CSMA/CD Access Method and Physical Layer Specification
- IEEE1588-2008, Precision Clock Synchronization Protocol

2.2.3 Optical module standards

- SFP MSA, ftp://ftp.seagate.com/sff/INF-8074.PDF

2.3 Terms and abbreviations

The following table lists any special terms and abbreviations used in this document.

Table 1 Terms and abbreviations

Term	Description
AMS	Automatic Media-Sense
EMI	Electromagnetic Interference, emissions
JTAG	Joint Test Access Group, IEEE1149
LVDS	Low Voltage Differential Signaling

Term	Description
LVTTL	Low Voltage TTL
NPI	Node Processor Interface
PCS	Physical Coding Sublayer
PHY	Physical layer device
SFP	Small Form-factor Pluggable transceiver
SI	Serial Interface, SPI

3 Features

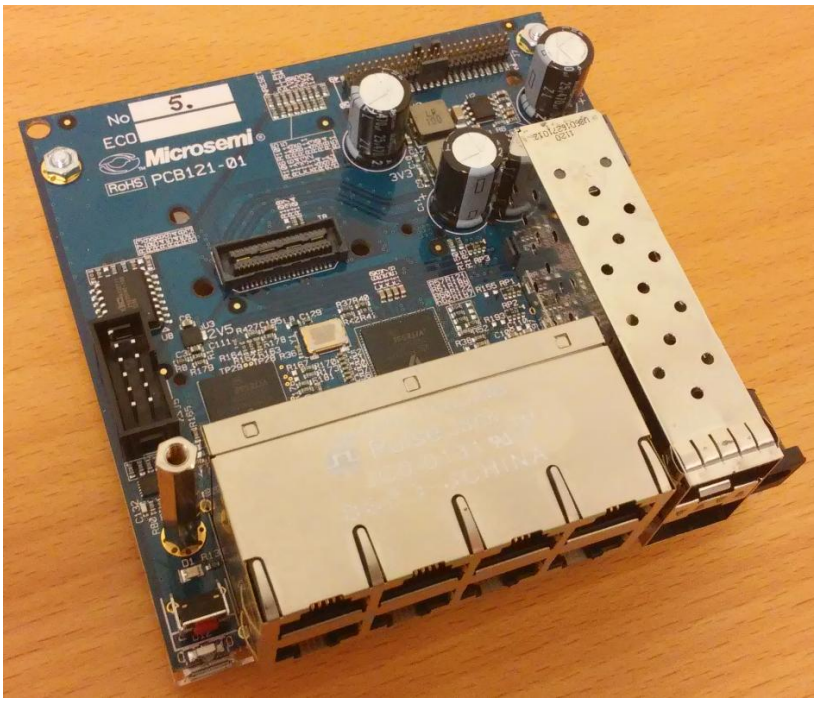
3.1 VSC5634EV

The VSC5634EV reference board's main use case is as an "unmanaged" switch, with the integrated CPU system in VSC7512 doing the initial setup of devices and whatever light duties required after setup.

Reference board feature summary below:

- Four 10/100/1000BASE-T (RJ45) Ethernet ports (PHYs integrated with VSC7512) …
- … and four more 10/100/1000BASE-T (RJ45) Ethernet ports (through VSC8514 PHY)
- Two 100M/1G/2.5Gbit/s Ethernet SFP ports (connected to VSC7512 through SERDES)
- One optional additional 10/100/1000BASE-T (RJ45) Ethernet port (VSC8221 PHY connected to VSC7512 through SGMII)
- Serial port for accessing the command line interface (CLI) software debugger, implemented through an on-board serial-to-USB converter (so connecting to a PC through a USB cable)
- Reset button with one-shot reset (so button state can be read by firmware after board reset, e.g. for a "reset to factory defaults" function)
- System status LED, port status LEDs
- 12Vdc power in socket

Figure 1 VSC5634EV



3.2 CPU system

3.2.1 Embedded VCore-I CPU system

- Embedded 8051 processor.
- Embedded RAM, external 256KBytes SPI boot Flash for basic setup.

3.2.2 Management and user I/O

- NPI port (extra LAN port) – the NPI port resides on a small add-on module
- Serial port converted to USB on-board, for accessing CLI debugger
- Reset button
- System status LED (tri-color green/yellow/red) and port status LED (tri-color green/yellow/red) per network port (e.g. for link and activity information), all LEDs controlled through the serial LED interface (using 74-series external shift registers)

3.3 Module slots and feature connectors

3.3.1 SFP module slots

VSC5634EV has two SFP slots for 100M/1G/2.5G SFP transceivers. The SFP slots connect to VSC7512 through SERDES.

VSC7512 port S7 (100M/1G/2.5G) connects directly to VSC5634EV SFP1.

VSC7512 ports S4 (100M/1G) and S8 (100M/1G/2.5G, PCIe capable) connects to an NPI/PCIe feature connector:

- When an NPI PHY module is mounted on this feature connector, S4 connects to a VSC8221 NPI PHY on the module, and the module feeds S8 back to the main VSC5634EV reference board for connection to SFP2 (100M/1G/2.5G capable in this case).
- When a PCIe module is mounted on this feature connector, S8 connects to a connector on the module for cabled PCIe, and the module feeds S4 back to the main VSC5634EV reference board for connection to SFP2 (100M/1G capable in this case).

3.3.2 SI (serial interface) feature connector

Interface to the VSC7512 SI (SPI) interface.

3.3.3 NPI/PCIe feature connector

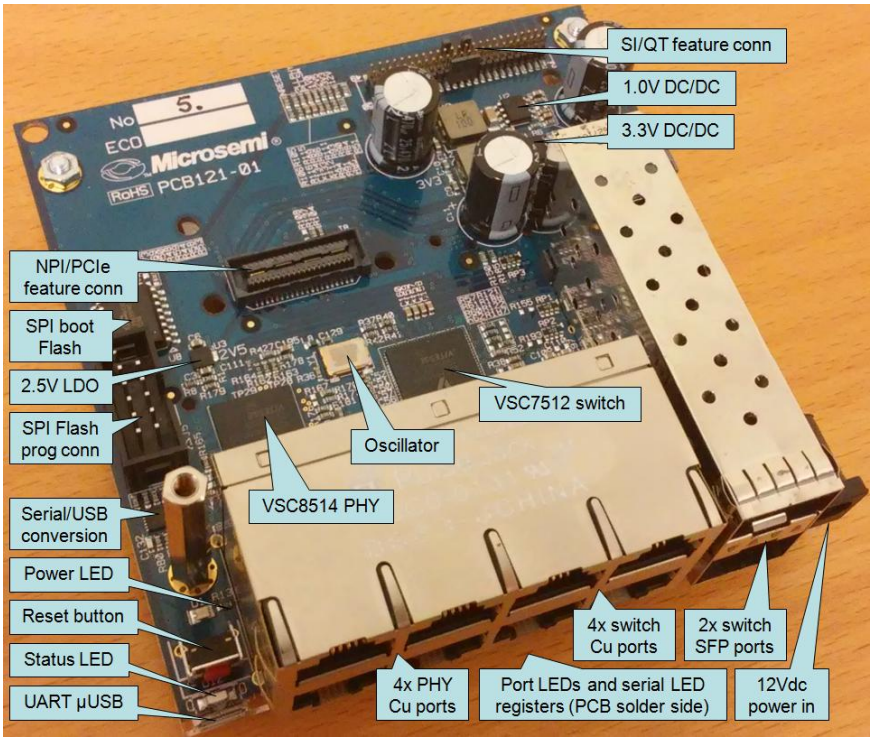
This feature connector primarily exposes the VSC7512 NPI port. If can also be used to connect an external PCIe master to the VSC7512 PCIe slave port.

Note that the add-on module connecting to the NPI/PCIe feature connector is responsible for feeding the VSC7512 SERDES port (S4 or S8) not used for NPI/PCIe duties on the module back to the main VSC5634EV reference board for connection to the mainboard's SFP2. If no module is added on the NPI/PCIe feature connector, the mainboard's SFP2 is thus left unconnected.

4 Quick start guide

4.1 Tour-de-board

Figure 2 Annotated photo of VSC5634



4.2 Connectors

4.2.1 Power input

12Vdc, 2.5 mm center pin power jack.

4.2.2 1x2 SFP ports

Connecting to VSC7512 SERDES ports.

4.2.3 4x2 RJ45 ports

Connecting to 4x VSC8514 PHY ports (in turn connecting to VSC7512 switch through QSGMII) and 4x VSC7512 switch ports.

4.2.4 µUSB (serial) port

The reference board can be connected directly to a PC USB port using the cable supplied with the system (or a standard USB-to-µUSB cable as used e.g. with many smartphones) to access the command line interface (CLI) debugger.

The reference board contains an on-board serial-to-USB converter, when connected to a PC the PC will detect this USB device and allow setup of e.g. baud rate - from there on the port will behave like a PC serial port e.g. including a COMx port number. On the PC, set the new COM port for 115200 baud, 8 data bits, no parity, 1 stop bit, no flow control, and point the terminal program of choice to the new COM port.

USB driver software (Windows, Mac, Linux) for the FTDI FT234XD serial-to-USB converter is available at http://www.ftdichip.com/Products/ICs/FT234XD.html.

4.2.5 SPI boot Flash programming

The SPI boot Flash can be programmed from an external programmer through a pin header.

4.2.6 NPI/PCIe feature connector

The NPI/PCIe feature connector is host to either the NPI PHY module or the PCIe module.

4.2.7 SI/QT feature connector

The SI (serial interface, SPI) bus of the VSC7512 is available in a 0.05" pitch pin header.

This feature connector has dual duty as connection point for the Microsemi QuickTest manufacturing test module, allowing for measurements of power supplies, resets etc.

4.3 Buttons

4.3.1 Reset

A reset button is available on the front of the reference board. When pressed it sinks an input of the voltage supervisor, creating a hard board reset. It functions as a one-shot, so pressing it causes a reset and it can afterwards be sampled by firmware to determine if it is still pressed during boot, e.g. causing a "reset to factory defaults".

4.4 LEDs

4.4.1 Power LED

A power LED is available, powered by the local 3.3V DC/DC converter (which is also the supply voltage monitored by the reset circuitry).

4.4.2 System status LED

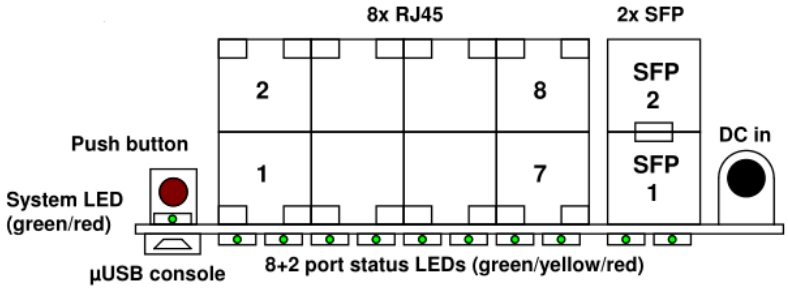
A tri-color (individual green/red controls, both on equals yellow) LED is available on the reference board front. It is controlled by switch firmware through the VSC7512 serial LED engine. It is yellow during reset.

4.4.3 Port status LEDs

The reference board has 8 ("2x4 RJ45") + 2 ("2x1 SFP") tri-color (individual green/red controls, both on equals yellow) port status LEDs available on the front.

The port status LEDs are controlled by firmware through the VSC7512 serial LED engine.

Figure 3 Front bracket layout for VSC5634EV



5 Hardware description

5.1 Block diagram

Figure 4 depicts the block diagram of the VSC5634EV reference board.

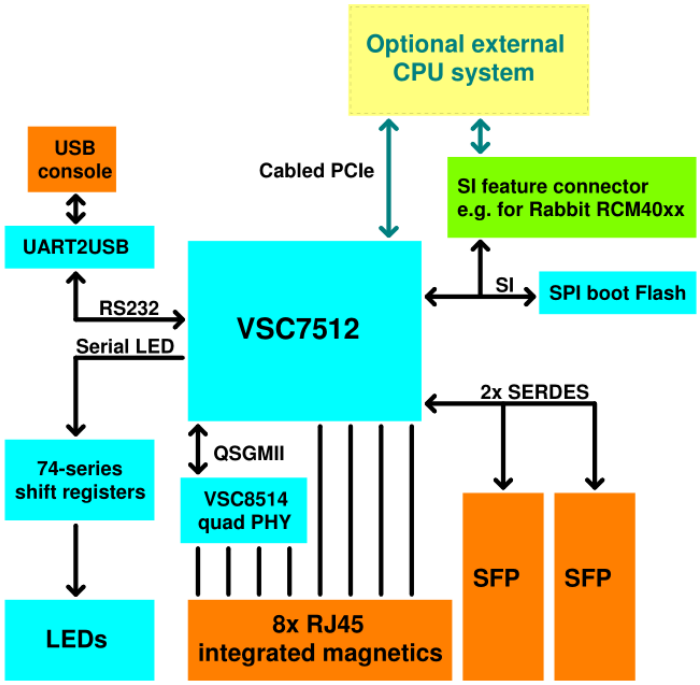
The design is based on the VSC7512 switch. It is complemented by a VSC8514 quad PHY providing four 1000Base-T ports in addition to the four 1000Base-T ports of VSC7512. Two VSC7512 network ports are made available as SFP module slots.

The VCore-I CPU of VSC7512 system is used for basic setup. It uses internal RAM and an external SPI Flash for booting the basic application firmware.

The VSC7512 serial GPIO/LED engine interfaces to external 74-series shift registers controlling system and port status LEDs.

The VSC7512 console port is exposed in a µUSB connector through a serial-to-USB converter.

Figure 4 System functional block diagram for VSC5634EV



5.2 CPU system

VSC7512 has an embedded VCore-I 8051-based CPU.

The VCore-I CPU is by default configured as master, booting from SPI Flash.

5.2.1 External memories

SPI boot NOR Flash

As default, the reference boards are equipped with 256KBytes of NOR SPI boot Flash. Other densities can easily be substituted, e.g. 64KBytes, depending on the application.

SPI boot Flash programming

The SPI boot Flash can be programmed from an external programmer through a 2x5 pin 0.1" pitch header. This includes a reset signal through which the programmer can keep VSC7512 in reset, in which state it will release control of its SI_DO output so that the programmer can take over while programming the SPI Flash. With the introduction of SPI Flash devices with a density above 128Mbit/16MBytes also comes a need for the SPI Flash to have a reset input – this SPI Flash reset input is exposed in the programming header allowing the programmer to (1) assert reset to the system to output disable VSC7512 SI signals and (2) deassert reset to the Flash to allow programming it.

Table 2 SPI boot Flash programming connector

Signal	Direction	Pin	Pin	Direction	Signal
SI_CLK - SPI clock signal	Switch<- Probe	1	2		Gnd
SI_DI - SPI data from SPI Flash	Switch-> Probe	3	4		nRESET_FLASH – reset signal from probe to Flash, keep high during Flash programming
n/c		5	6	Probe<- Switch	3V3
SI_nCS0 - SPI chipselect signal	Switch<- Probe	7	8	Probe-> Switch	nSYSRESETin - reset signal from probe to switch, keep low during Flash programming
SI_DO - SPI data to SPI Flash	Switch<- Probe	9	10		Gnd

5.2.2 NPI/PCIe

The NPI and PCIe interfaces of VSC7512 are exposed in a Samtec QSE-020 NPI/PCIe feature connector. A small add-on module exposes the VSC7512 S8 port in a standard PCIe cable connector, another small add-on module feeds the VSC7512 S4 port to a single PHY thus exposing the NPI interface as a 1000Base-T port. The VSC7512 port (S4/S8) not used on an add-on module must be fed back to the VSC5634EV mainboard for connection to the front SFP2.

The NPI/PCIe feature connector signal pins are detailed in Table 3.

Table 3 NPI/PCIe feature connector signal description

Description	Pin	Pin	Description
PCIe_R_N, extCPU->switch S8 (or fed back to reference board SFP2)	1	2	12V
PCIe_R_P, extCPU->switch S8 (or fed back to reference board SFP2)	3	4	12V
3V3	5	6	nSYSRESET, reference board reset signal

Description	Pin	Pin	Description
PCIe SB_RTN, grounded by reference board host	7	8	PCIe CPRSNT#, grounded by reference board host
PCIe_CLK_N, 50R terminated by reference board host	9	10	12V
PCIe_CLK_P, 50R terminated by reference board host	11	12	12V
MII_MDIO, management bus interface towards NPI PHY	13	14	PCIe CPWRON, n/c on reference board host
nSYSRESETin, allows extCPU to reset reference board host	15	16	PCIe_T_N, switch S8 ->extCPU (or fed back to reference board SFP2)
MII_MDC, management bus interface towards NPI PHY	17	18	PCIe_T_P, switch S8 ->extCPU (or fed back to reference board SFP2)
SI_DO	19	20	VCORE_CFG3
SI_DI	21	22	VCORE_CFG2
SI_CLK	23	24	VCORE_CFG1
SI_nCS0	25	26	VCORE_CFG0
RS232_TXD	27	28	nINT_PHY, interrupt signal towards reference board, open collector
RS232_RXD	29	30	SPI_nCSflash
GND	31	32	n/c
SFP2_T_P, reference board SFP2 transmit data (towards SFP)	33	34	NPI_T_P, switch S4 ->NPI PHY (or fed back to reference board SFP2)
SFP2_T_N, reference board SFP2 transmit data (towards SFP)	35	36	NPI_T_N, switch S4 ->NPI PHY (or fed back to reference board SFP2)
SFP2_R_N, reference board SFP2 receive data (towards VSC7512)	37	38	NPI_R_N, NPI PHY->switch (or fed back to reference board SFP2)
SFP2_R_P, reference board SFP2 receive data (towards VSC7512)	39	40	NPI_R_P, NPI PHY->switch (or fed back to reference board SFP2)

5.2.3 SI feature connector

The SI feature connector is a 2x25 pin 0.05” pitch boxed pin header. It can be used to connect to the VSC7512 SI bus.

The SI feature connector is also used for the QuickTest board diagnostics add-on module, monitoring a selection of signals useful in mainboard bring-up and manufacturing testing. The QuickTest related signals are simply labeled as such in Table 4.

Table 4 SI feature connector signal description

Description	Pin	Pin	Description
3V3	1	2	GND
QuickTest	3	4	QuickTest
QuickTest	5	6	QuickTest
GND	7	8	GND
QuickTest	9	10	QuickTest

Description	Pin	Pin	Description
QuickTest	11	12	QuickTest
QuickTest	13	14	QuickTest
QuickTest	15	16	QuickTest
QuickTest	17	18	QuickTest
QuickTest	19	20	QuickTest
QuickTest	21	22	QuickTest
QuickTest	23	24	RS232_RXD
RS232_TXD	25	26	SI_DI, input to VSC7512
SI_DO, output from VSC7512	27	28	nMODULE_INT
QuickTest	29	30	QuickTest
SI_CLK	31	32	QuickTest
QuickTest	33	34	nSYSRESET_IN
SI_nCS0	35	36	QuickTest
QuickTest	37	38	QuickTest
QuickTest	39	40	VCORE_CFG0
VCORE_CFG1	41	42	VCORE_CFG2
VCORE_CFG3	43	44	QuickTest
I2C_SCL	45	46	QuickTest
I2C_SDA	47	48	SPI_nCSflash
QuickTest	49	50	GND

5.3 Network ports

- Four 10/100/1000BASE-T RJ45 front ports are connected to VSC7512 1000Base-T ports.
- Four 10/100/1000BASE-T RJ45 front ports are connected to VSC8514 1000Base-T ports.
- One 10/100/1000BASE-T RJ45 port is available when using the NPI PHY module.
- Two 100M/1000M/2.5G SFP front ports are connected directly to the VSC7512 switch through SERDES.

Table 5 VSC5634EV physical port summary

VSC5634EV board physical port	VSC7512 physical pins	VSC7512 port number / device	Additional information
RJ45 #1	S6/QSGMII (VSC8514 port 1)	4	"External" MIIM address 4
RJ45 #2	S6/QSGMII (VSC8514 port 2)	5	"External" MIIM address 5
RJ45 #3	S6/QSGMII (VSC8514 port 3)	6	"External" MIIM address 6
RJ45 #4	S6/QSGMII (VSC8514 port 4)	7	"External" MIIM address 7
RJ45 #5	P0	0	"Internal" MIIM address DEVCPU_GCB:PHY:PHY_CFG.PHY_ADDR+0

VSC5634EV board physical port	VSC7512 physical pins	VSC7512 port number / device	Additional information
RJ45 #6	P1	1	"Internal" MIIM address DEVCPU_GCB:PHY:PHY_CFG.PHY_ADDR+1
RJ45 #7	P2	2	"Internal" MIIM address DEVCPU_GCB:PHY:PHY_CFG.PHY_ADDR+2
RJ45 #8	P3	3	"Internal" MIIM address DEVCPU_GCB:PHY:PHY_CFG.PHY_ADDR+3
SFP #1	S7	8	SCL=GPIO[20], LOS=GPIO[10], MODDETn=GPIO[8], TXFAULT=GPIO[12], TXDISABLE=GPIO[5], RATESEL=GPIO[18]
SFP2 (with NPI PHY module)	S8	10	SCL=GPIO[21], LOS=GPIO[11], MODDETn=GPIO[9], TXFAULT=GPIO[13], TXDISABLE=GPIO[17], RATESEL=GPIO[19]
SFP2 (with PCIe module)	S4	9	As above (so tied to SFP2 rather than S4/S8): SCL=GPIO[21], LOS=GPIO[11], MODDETn=GPIO[9], TXFAULT=GPIO[13], TXDISABLE=GPIO[17], RATESEL=GPIO[19]
NPI (only with NPI PHY module)	S4	9	"External" MIIM address 0x1C
PCIe (only with PCIe module)	S8	n/a	

5.3.1 PHYs

The twisted pair interfaces on the copper PHYs of VSC5634EV are fully compliant with the IEEE802.3 specification for CAT-5 media. The Microsemi PHYs, unlike other traditional Gigabit PHYs, integrate all passive components required to connect the PHYs' CAT-5 interface to an external 1:1 transformer and common mode choke. This reduces the number of components in a design and greatly simplifies the layout of this interface.

The ports support auto-negotiation and can automatically detect the speed and duplex mode of a link and provide the appropriate connection in 10BASE-T half-duplex, 10BASE-T full duplex, 100BASE-T half-duplex, 100BASE-T full duplex or 1000BASE-T full duplex.

The ports include Automatic Crossover Detection functionality for all three speeds (HP Auto MDI/MDI-X function). They also include the ability to detect and correct polarity errors on all MDI pairs. These functions are normally enabled, but can be disabled.

The ports support the IEEE standard range of 1m to 100m twisted pair cable.

1000Base-T mode requires Category 5 enhanced cable in accordance to the cabling specifications defined by IEEE802.3-2005.

100BASE-TX mode requires Category 5 cable and 10BASE-T requires Category 3 cable as specified in ISO/IEC 11801.

TVS diodes

The port-side signals (4 differential signals) comprising each of the 8 copper port interfaces of the mainboard can optionally be further protected from over-voltage events such as ESD, cable-discharge or lightning-induced transients by mounting TVS3V3L4U TVS diodes. Note that the

capacitance of protection devices such as TVS diodes will add to the capacitance of PCB traces and e.g. EMI caps, and that the accumulated capacitance may impact e.g. IEEE template compliance.

5.3.2 SFP interfaces

VSC5634EV has two front port SFP module slots connected directly to the VSC7512 switch. These can host 2.5Gbit/s, 1000BASE-X or 100BASE-FX SFP plugs, in this case PHY and SFP interface via a SERDES protocol - or copper SFP plugs via an SGMII protocol.

Note that the connection between VSC7512 and SFP2 is provided through the NPI/PCIe module, to allow for 2x 2.5G capable SFPs when using VSC5634EV in non-PCIe mode, and 1x1G+1x2.5G capable SFPs when using VSC5634EV in PCIe mode (where the PCIe port use the 2.5G capable VSC7512 SERDES port S8 otherwise used for SFP2 duties).

SFPs have the inherent “feature” of occupying a specific I2C slave address, which is an issue when several SFPs are to be connected to a single I2C master. VSC7512 offers an embedded I2C clock multiplexer as overlaid functions on GPIO pins. Through this multiplexer one SFP I2C slave at a time is connected to the VSC7512 I2C master.

The semi-static control signals (LossOfSignal, TxFault, TxDisable, ModuleDetect and RateSelect) of the SFPs are connected to VSC7512 GPIOs as detailed in Table 5 and Table 6.

5.4 GPIO

The reference board uses the VSC7512 GPIO pins as detailed in Table 6.

Table 6 VSC5634EV/VSC7512 GPIO

GPIO	Signal	Description
GPIO_0	SLED_CLK	Serial GPIO/LED controller clock
GPIO_1	SLED_DO	Serial GPIO/LED controller data output
GPIO_2	PUSHBUTTONn	Input from the reset push button, as the reset function has a one-shot the signal can be sampled by firmware e.g. during boot
GPIO_3	Not used	Not used
GPIO_4	nINT_PHY	Output from VSC8514 and VSC8221 PHYs
GPIO_5	SFP1_TXDISABLE	TX disable output towards SFP1 – 0=laser enabled, 1=laser disabled
GPIO_6	RS232_RXD	Data received from serial port
GPIO_7	RS232_TXD	Data transmitted to serial port
GPIO_8	SFP1_MODDETn	Module detect input from SFP1 – 0=module present, 1=module absent
GPIO_9	SFP2_MODDETn	Module detect input from SFP2 – 0=module present, 1=module absent
GPIO_10	SFP1_LOS	Loss of signal input from SFP1 – 0=optical signal present, 1=optical signal absent
GPIO_11	SFP2_LOS	Loss of signal input from SFP2 – 0=optical signal present, 1=optical signal absent
GPIO_12	SFP1_TXFAULT	TX fault input from SFP1 – 0=transmitter OK, 1=transmitter faulty
GPIO_13	SFP2_TXFAULT	TX fault input from SFP2 – 0=transmitter OK, 1=transmitter faulty
GPIO_14	MII_MDC	Management bus clock
GPIO_15	MII_MDIO	Management bus data
GPIO_16	I2C_SDA	Data line in the I2C serial interface

GPIO	Signal	Description
GPIO_17	SFP2_TXDISABLE	TX disable output towards SFP2 – 0=laser enabled, 1=laser disabled
GPIO_18	SFP1_RATESEL	Rate select output towards SFP1
GPIO_19	SFP2_RATESEL	Rate select output towards SFP2
GPIO_20	SFP1_SCL	Multiplexed (gated) clock line in the I2C serial interface, towards SFP1
GPIO_21	SFP2_SCL	Multiplexed (gated) clock line in the I2C serial interface, towards SFP1

5.5 Serial GPIO/LED

VSC7512 incorporates a novel serial GPIO mechanism.

Through four pins a serial GPIO controller interfaces to 74-series shift registers on the board to provide a flexible GPIO mechanism. It is documented in the Serial GPIO user's guide and in the VSC7512 datasheet.

Instead of 74-series shift registers, the external circuitry can of course be implemented in e.g. a central PLD, but the parallel inputs and outputs of this would then have to be routed across the board between the PLD and individual endpoints – using shift registers it is only the four VSC7512 serial GPIO signals which need to be routed "long distance", the shift registers can be distributed across the board as applicable.

On VSC5634EV the serial GPIO controller is used only to control port and system status LEDs, and thus only the clock and output data pins of the VSC7512 serial GPIO controller is required.

The port and system status LEDs are tri-color – one pin controls a green LED, another pin controls a red LED, when both green and red LED parts are turned on simultaneously the LED shows a yellowish color.

Serial GPIO controller setup: Enable ports 11 and [8:0] – if the NPI PHY add-on module is present on the NPI/PCIe feature connector also enable port 10 (used to output serial LED data for SFP2 when connected to VSC7512 port S8 through the NPI PHY module) – if the PCIe add-on module is present on the NPI/PCIe feature connector also enable port 9 (used to output serial LED data for SFP2 when connected to VSC7512 port S4 through the PCIe module). Enable bits 1:0. The individual bits in the serial GPIO output frame are used as detailed in Table 7.

Table 7 Serial GPIO/LED

Port/bit	Output used for
p0b0	RJ45#5 (VSC7512 P0) green LED (0=on, 1=off)
p0b1	RJ45#5 (VSC7512 P0) red LED (0=on, 1=off)
p1b0	RJ45#6 (VSC7512 P1) green LED (0=on, 1=off)
p1b1	RJ45#6 (VSC7512 P1) red LED (0=on, 1=off)
p2b0	RJ45#7 (VSC7512 P2) green LED (0=on, 1=off)
p2b1	RJ45#7 (VSC7512 P2) red LED (0=on, 1=off)
p3b0	RJ45#8 (VSC7512 P3) green LED (0=on, 1=off)
p3b1	RJ45#8 (VSC7512 P3) red LED (0=on, 1=off)
p4b0	RJ45#1 (VSC8514 P0) green LED (0=on, 1=off)
p4b1	RJ45#1 (VSC8514 P0) red LED (0=on, 1=off)
p5b0	RJ45#2 (VSC8514 P1) green LED (0=on, 1=off)

Port/bit	Output used for
p5b1	RJ45#2 (VSC8514 P1) red LED (0=on, 1=off)
p6b0	RJ45#3 (VSC8514 P2) green LED (0=on, 1=off)
p6b1	RJ45#3 (VSC8514 P2) red LED (0=on, 1=off)
p7b0	RJ45#4 (VSC8514 P3) green LED (0=on, 1=off)
p7b1	RJ45#4 (VSC8514 P3) red LED (0=on, 1=off)
p8b0	SFP#1 (VSC7512 S7) green LED (0=on, 1=off)
p8b1	SFP#1 (VSC7512 S7) red LED (0=on, 1=off)
p9b0	SFP#2 (VSC7512 S4) green LED (0=on, 1=off) - note, only with PCIe module added on NPI/PCIe feature connector
p9b1	SFP#2 (VSC7512 S4) red LED (0=on, 1=off) - note, only with PCIe module added on NPI/PCIe feature connector
p10b0	SFP#2 (VSC7512 S8) green LED (0=on, 1=off) - note, only with NPI PHY module added on NPI/PCIe feature connector
p10b1	SFP#2 (VSC7512 S8) red LED (0=on, 1=off) - note, only with NPI PHY module added on NPI/PCIe feature connector
p11b0	System status LED green (0=on, 1=off)
p11b1	System status LED red (0=on, 1=off)

5.6 UARTs

The VSC7512 VCore-I CPU has two on-chip serial UARTs, available as alternate functions on GPIO pins.

UART1 is used as console port and connected through an FTDI FT234XD serial-to-USB converter to a µUSB connector on the reference board front. The FTDI FT234XD is reset when USB bus power is not available, to ensure that it awakens smoothly when connected through a USB cable to e.g. a PC.

UART2 is not used in this reference design.

5.7 I2C

I2C addresses are allocated according to Table 8.

Table 8 I2C addresses

I2C address	Device
1010xxx	SFP transceiver

Other addresses can be used freely.

VSC7512 contains an I2C multiplexer targeted at accessing e.g. SFP plugs which need to be at separate I2C segments in order to avoid I2C address conflicts (all SFPs reside on the same I2C address). The VSC7512 I2C multiplexer uses separate I2C_SCL lines per I2C segment, and shares a single I2C_SDA signal among all I2C segments.

VSC7512 multiplexed I2C signals are available as alternate functions on GPIOs (as are the primary I2C signals, actually). See Table 6 for details.

5.8 Interrupts

VSC7512 has dedicated interrupt inputs as alternate functions on GPIOs. These are used as depicted in Table 9.

Table 9 Interrupt inputs

Interrupt	GPIO	Description
nINT_PHY	GPIO_4, IRQ0	Shared (open collector) interrupt, used by VSC8514 quad PHY and VSC8221 single PHY (the latter only when the NPI module is added to the NPI/PCIe feature connector)
-	GPIO_5, IRQ1	Not used in this reference design

5.9 Reset

A MAX811 power watchdog monitors the 3.3 V supply and generates reset when applicable. The other supply voltages are not monitored.

A reset can also be triggered by the reset button mounted on the front of the reference board, by the SPI boot Flash programming header, or by the SI and NPI/PCIe feature connectors.

The reset button triggers a one-shot circuit on its path to the power watchdog button input, hence it is possible to keep the button pressed through a reset and have firmware detect that it is still pressed during boot, e.g. to trigger a “restore factory defaults” firmware function.

5.10 Reference clock

A single 125MHz oscillator sources reference clock to both VSC7512 switch and VSC8514 PHY.

Signal level is LVCMOS33, with local resistor dividers at both consumers converting the signal to a pseudo-differential clock as required by the consumer devices’ REFCLK_p/n differential inputs.

The clock trace is short, less than 1”, and routed daisychained and with an RC destination termination.

Any changes to this should be thoroughly simulated on post-layout data – reference clock signal integrity is vital to the performance of the two clock signal consumers.

5.11 JTAG

JTAG signals from both VSC7512 and VSC8514 PHY are exposed on PCB test points, and JTAG_nTRST signals are pulled low. Apart from this JTAG is not used in this reference design, e.g. the two devices are not connected in a common JTAG chain as that would have added to PCB layout complexity.

5.12 Power supply

Table 10 lists a summary of the power consumption for VSC5634EV. Note that as VSC7512 characterization had not been concluded at the time this was written, the power consumption figures are estimated max values at specific operating conditions that are provided here only to dimension the power generation circuits. Consult the specific device datasheets for the most accurate power consumption figures.

Table 10 VSC5634EV power

	Supply	Max amps	Max watts
VSC7512			
VDD_CORE	1.0	1.677	1.68
VDD_A	1.0	0.236	0.24
VDD_AL	1.0	0.129	0.13
VDD_AH	2.5	0.500	1.25
VDD_H	2.5	0.025	0.06
VDD_IO	2.5	0.020	0.05
VDD_S	1.0	0.140	0.14
Total power for VSC7512			*3.54*
VSC8514			
VDD_CORE	1.0	0.605	0.61
VDD_A	1.0	0.245	0.25
VDD_25	2.5	0.570	1.43
Total power for VSC8514			*2.28*
Misc			
LEDs	3.3	0.033	0.11
Flash	3.3	0.025	0.08
2x SFP	3.3	0.606	2.00
NPI PHY	3.3	0.303	1.00
Oscillator, SGPIO, misc	3.3	0.070	0.23
Total power for misc			*3.42*
Supply summary			
1.0V supply from 12V	1.0	3.032	3.03
Power dissipation in supply (@80% efficiency)			0.61
2.5V supply from 3.3V	2.5	1.115	2.79
Power dissipation in supply (linear regulator, loss included in 3.3V supply)			0.56
3.3V supply from 12V	3.3	2.152	7.10
Power dissipation in supply (@80% efficiency)			1.42
12V from DC input	12.0	1.013	12.16

VSC5634EV contains regulators for:

- 1.0V@3.0A – VSC7512 core and QSGMII/SERDES, VSC8514 core and QSGMII
- 3.3V@2.2A – Flash, SFPs, LEDs, oscillator, source for 2.5V LDO
- 2.5V@1.1A – VSC7512 and VSC8514 digital IO and 1000Base-T

1.0V and 3.3V are generated by DC/DC converters from the 12Vdc input.

2.5V is generated by a linear regulator from the local 3.3V supply.

6 Environmental requirements

VSC5634EV is designed to operate within the following temperatures (case and airflow dependent):

- Operating temperature: -40° to +40°C
- Storage temperature: -40° to +70°C
- Operating humidity: 10 % to 95 % relative humidity, non condensing

7 Layout

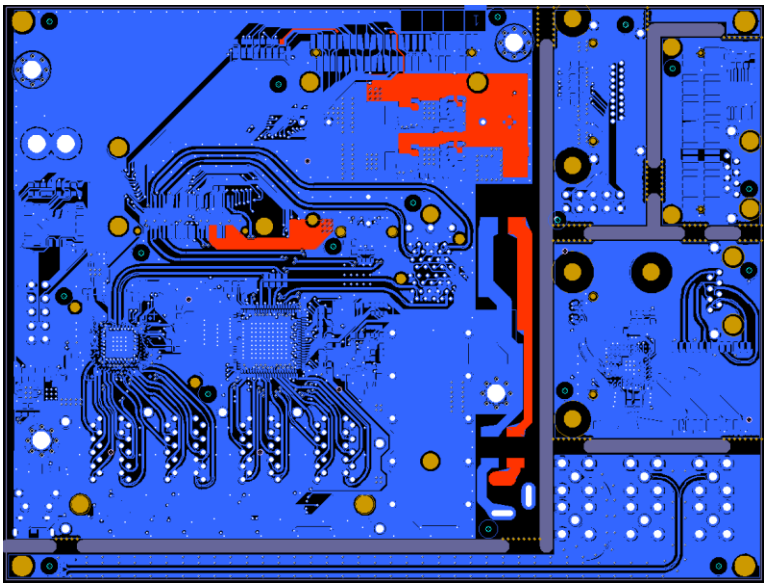
The VSC7512 device's package pinout is specifically optimized for low-cost PCB designs. As a result, the VSC5634EV reference board requires only four PCB layers. Layer 1 (top) contains signal traces as well as some power distribution planes, layer 2 is a solid ground plane, layer 3 contains power distribution, and layer 4 (bottom) additional routing and some power distribution planes. The solid ground plane layer is also used to remove heat from components and it must (also for this reason) be ensured that good connection between outer layer ground fills and the ground plane on layer 2 is established.

7.1 Power distribution

7.1.1 12V

The 12V power supply comes in from external PSU, passes over-voltage proteciong tranzorbers and through a common-mode choke, lives mostly on layer 4 for use by the 1.0V and 3.3V DC/DC supplies, carrying a calculated total current of 1A.

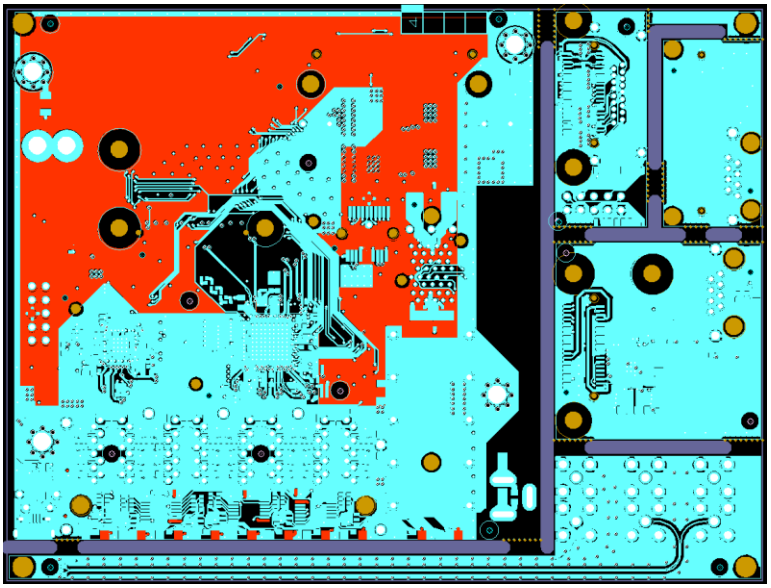
Figure 5 12V distribution, layer 1



7.1.2 3.3V

The 3.3V power supply is distributed mainly on layer 4 to devices as diverse as LEDs, Flash and SFP modules. At 2.2A current, this is one of the highest-current paths of the design, hence the distribution plane is as wide as possible. In order to compensate for the DC drop voltage in the plane, the DC/DC senses the voltage at the SFPs, through a 0 ohm resistor to ensure a discrete PCB trace.

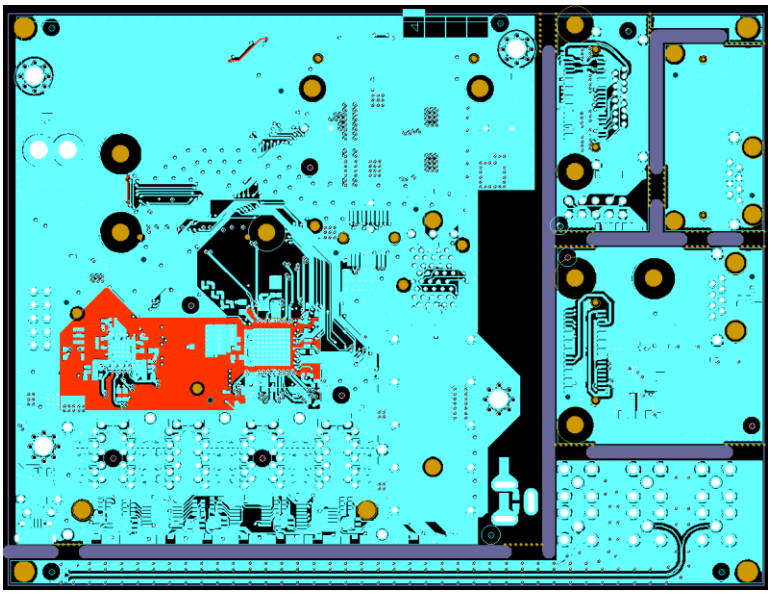
Figure 6 3.3V distribution, layer 4



7.1.3 2.5V

The 2.5V supply is led from the series regulator circuit to the VSC7512 switch and VSC8514 PHY. At 1.1A current, this is a fairly low-current path.

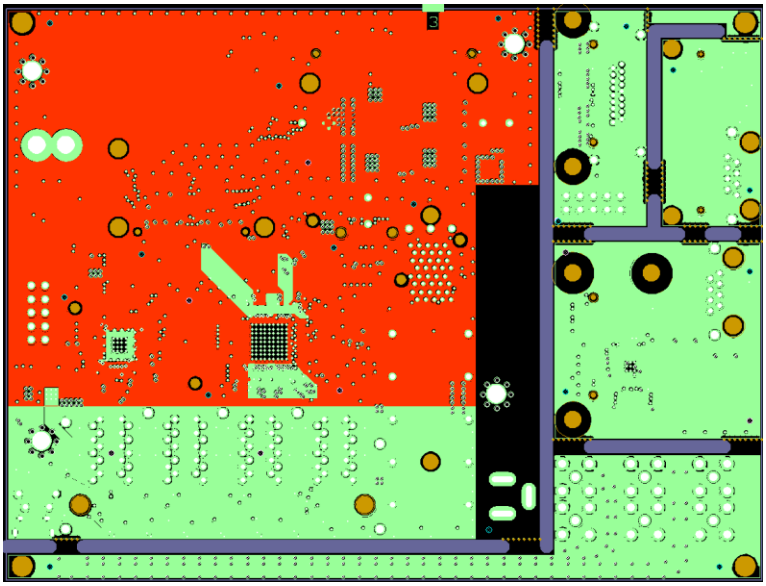
Figure 7 2.5V distribution, layer 4



7.1.4 1.0V

The 1.0V supply is led from the DC/DC circuit to the core and IO supplies of the VSC7512 switch and VSC8514 PHY. At 3A current, this is the highest-current path of the design, hence the distribution plane is as wide as possible. In order to compensate for the DC drop voltage in the plane, the DC/DC senses the voltage at the left of VSC8514, through a 0 ohm resistor to ensure a discrete PCB trace.

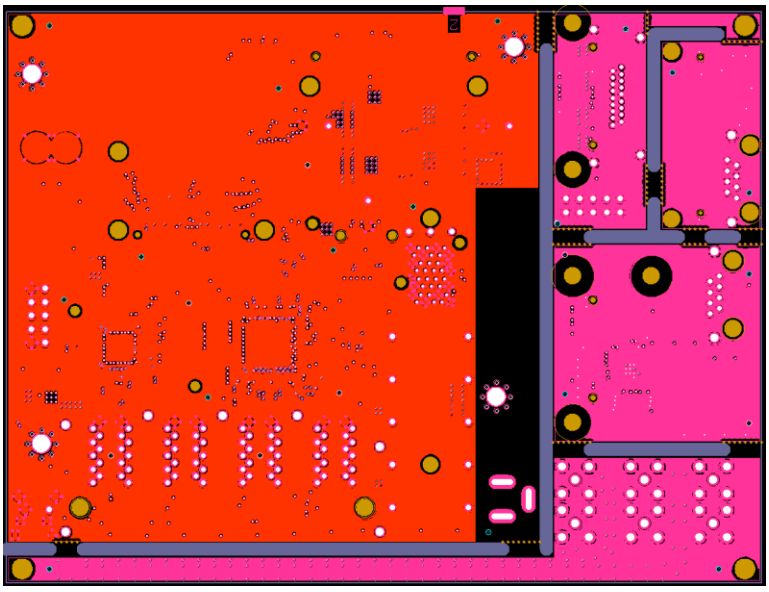
Figure 8 1.0V distribution, layer 3



7.1.5 Ground

A solid ground plane on layer 2 ensures that all signals on layer 1 have a good reference plane. In addition, the outer layers have ground fill areas for copper balancing purposes.

Figure 9 Ground distribution, layer 2



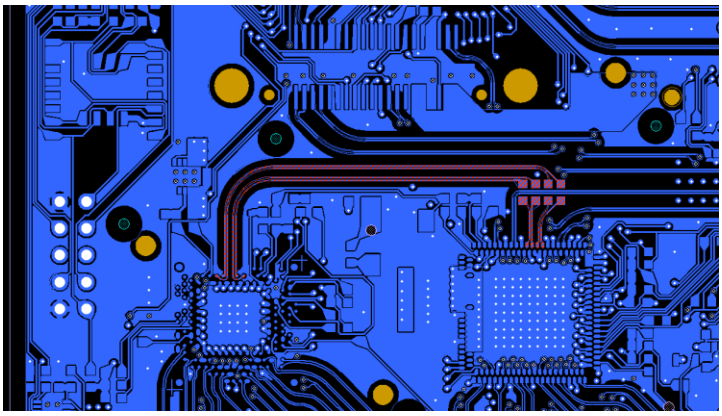
7.2 Critical nets' routing

Note that any net can be critical under the wrong circumstances – this is a minimum selection of nets that should be reviewed/simulated/measured thoroughly.

Also note the general PCB layout recommendations of chapter 9.

7.2.1 QSGMII

Figure 10 QSGMII routing, layer 1



The QSGMII signals are the highest bandwidth signals of the design, 5Gbit/s. They are routed as differential pairs between VSC7512 switch and VSC8514 PHY. Signal traces are kept as short as possible, and on a single layer to avoid impedance discontinuities of vias. Intra-pair skews (p/n differences) are kept as close to 0 as possible.

7.2.2 SERDES

Figure 11 SERDES routing, layer 1

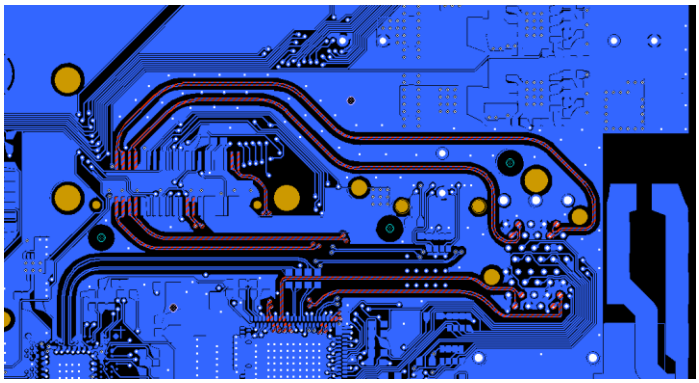
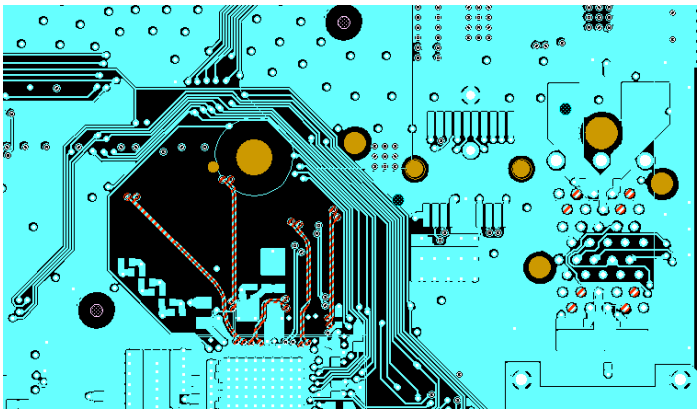


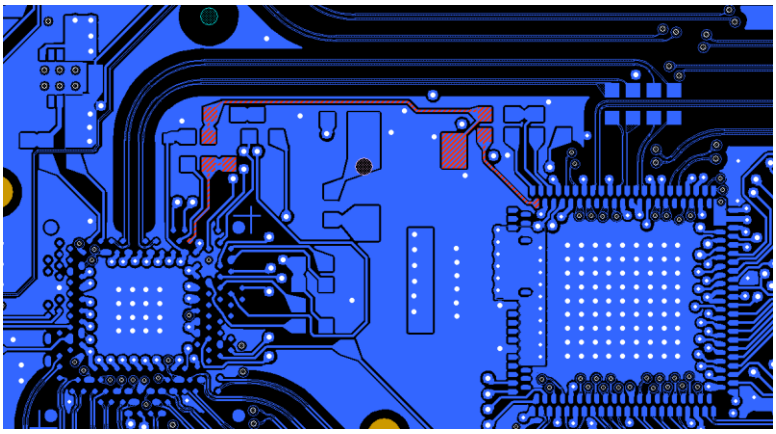
Figure 12 SERDES routing, layer 4



The SERDES signals are high bandwidth signals, up to 2.5Gbit/s. They are routed as differential pairs between VSC7512 switch and SFP connectors, for S4 and S8 with a detour to the NPI/PCIe feature connector. Signal traces are kept as short as possible, and intra-pair skews (p/n differences) are kept as close to 0 as possible.

7.2.3 Reference clock

Figure 13 Reference clock routing, layer 1



The reference clock signals are critical as e.g. clock jitter has a significant impact on device performance. The reference clock signal is routed daisychained from oscillator to VSC7512 switch and VSC8514 PHY, with an RC end termination at end-of-trace. Signal traces are kept as short as possible and without vias.

7.2.4 Other clocks

Other clock signals include SI_CLK, MDC, I2C_SCL and SLED_CLK. Though not necessarily high frequency, these clock signals have fast risetimes so should be treated with care.

7.3 Component locations

Figure 14 VSC5634EV component layout, top side

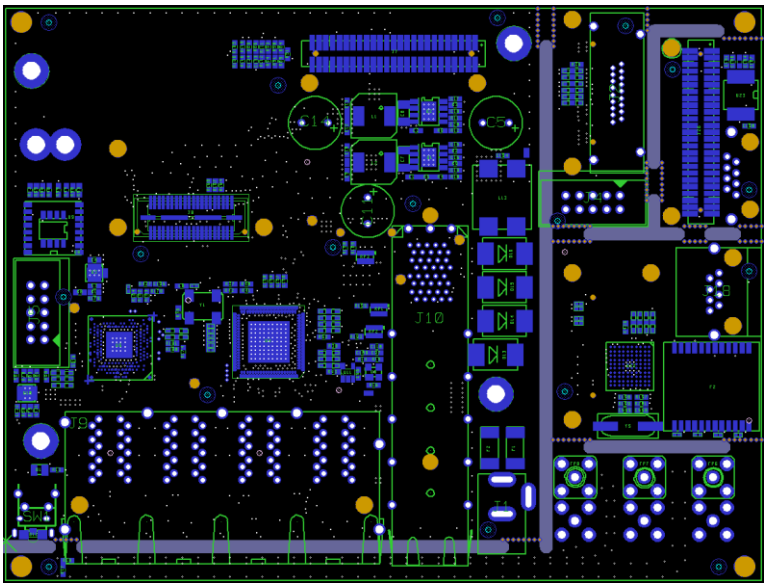
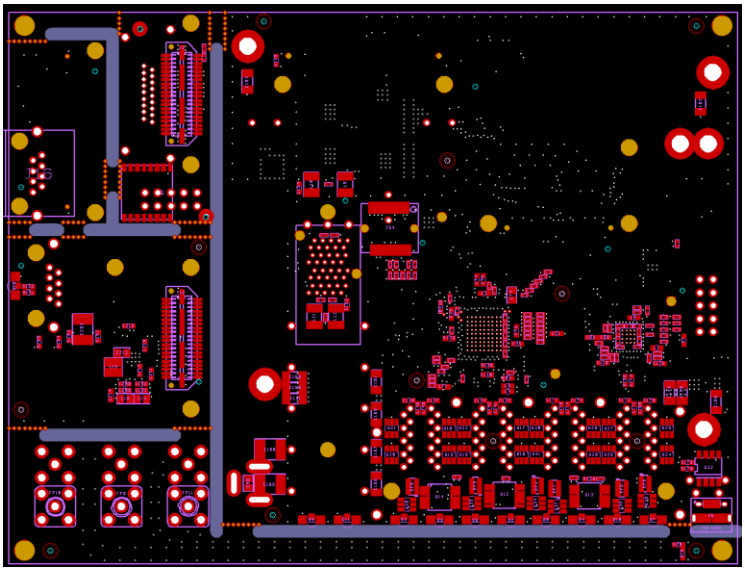
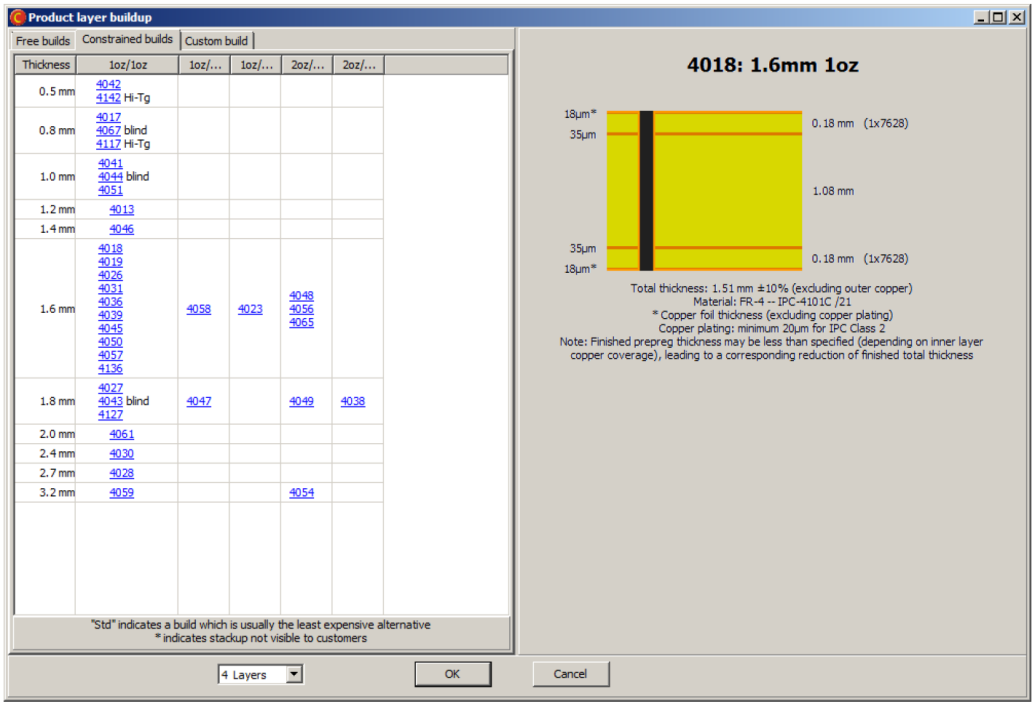


Figure 15 VSC5634EV component layout, bottom side



7.4 PCB stack-up

The board is a 4-layer impedance-controlled PCB. The stack-up of the layers is shown below.



7.5 PCB trace widths and clearance

Board thickness	1.6mm ± 10%
Characteristic impedance single ended	70 ohm
Characteristic impedance differential signals	100 ohm
Single ended trace width	125um
Single ended trace to trace clearance	125um
100ohm differential trace width	125um
100ohm differential trace to trace clearance	125um

Figure 16 Single-ended trace impedance calculations

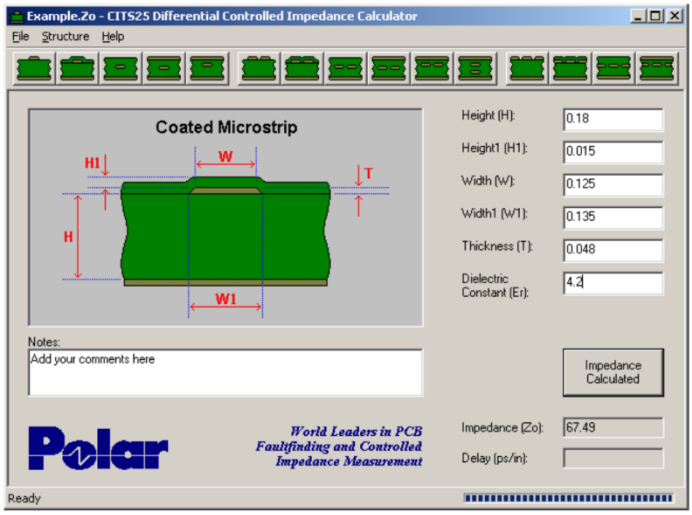
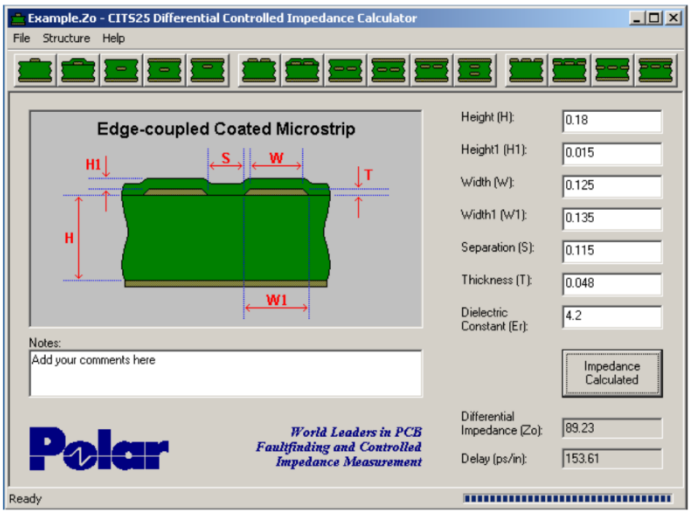


Figure 17 Differential trace (QSGMII etc.) impedance calculations



Our experience is that the Polar tool's calculation of differential impedance is approx 10 ohms off, so that this geometry results in a differential impedance close to 100 ohms.

8 Schematic review checklist

This section describes the things board designers should check extra carefully when making a schematic. Note that this section is meant only to supplement the Design Guidelines section in the devices' datasheets. Ask your friendly Microsemi FAE for updated datasheets, device errata and schematics checklists and study these carefully before committing a design.

8.1 Reset control checklist

nReset (active low) must be de-asserted no less than 20ms after the power supplies and the reference clock are valid. For this reason a POR/delay circuit must be used on the nReset pin. The MAX811 can be used to provide the POR delay after valid power supplies and clock.

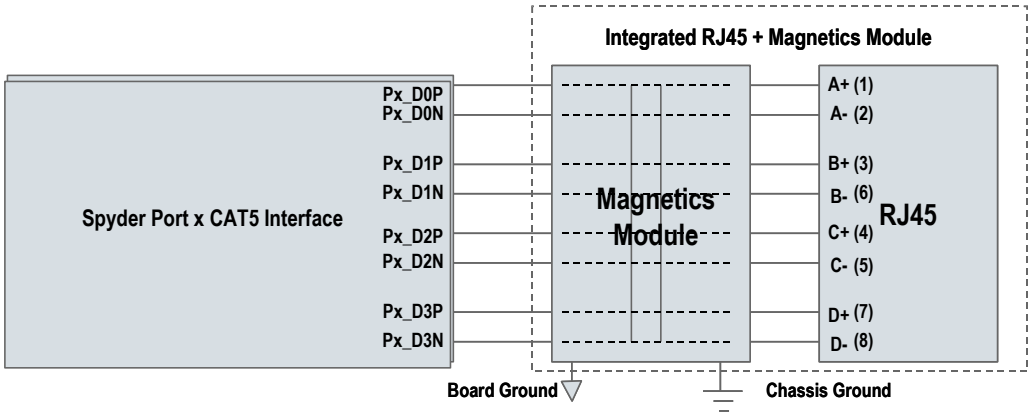
8.2 Reference clock checklist

The free-running reference clock can e.g. be a 125MHz +/-50 ppm clock source. Note the device datasheets' requirements for maximum clock jitter, which must be accounted for in board design when e.g. selecting clock source (oscillator) and clock distribution (buffer) components.

8.3 CAT5 media interface checklist

8 pins per port i.e. a total of 32 pins constitute the CAT5 media interface of VSC8584. These are named as Px_DyP and Px_DyN, where x is the port number 0-24 and y is the CAT5 cable pair 0-3.

Pairs 0-3 correspond to pairs A-D of the CAT5 cable respectively. Detailed connections of the CAT5 interface are shown below.



To pass the IEEE standard ESD tolerance tests it is important that the Board Ground and Chassis Ground be isolated across the Magnetic Module. However, it is recommended that a placeholder for a 0.1uf capacitor be included in the design for reducing EMI if needed. The magnetic module used is very important to ensure good EMI performance. Contact a Microsemi FAE to get the latest list of compatible magnetic modules.

Several different magnetic options exist, with different number of ferrite cores in the design, depending on the EMI performance needed. Microsemi recommends a magnetic module that includes one or more common mode chokes. The centre taps on the PHY side should be connected to board ground through 100nF capacitors.

8.4 Control signal checklist

- JTAG Interface
  - When JTAG is not being used, the JTAG_nTRST must be pulled down using a 1k resistor for normal operation.
- General Purpose I/Os
  - VSC7512 provides 22 GPIO pins, all with optional overlaid/alternate functions and some with additional strapping duties.
- Analog Bias Pins PHY (both VSC7512 and VSC8514)
  - Ref_Rext: The resistor connected to this pin sets the internal reference bias of the PHY. A 2k, 1% resistor must be used.
  - Ref_Filt: The capacitor connected to this pin filters the internal reference bias.

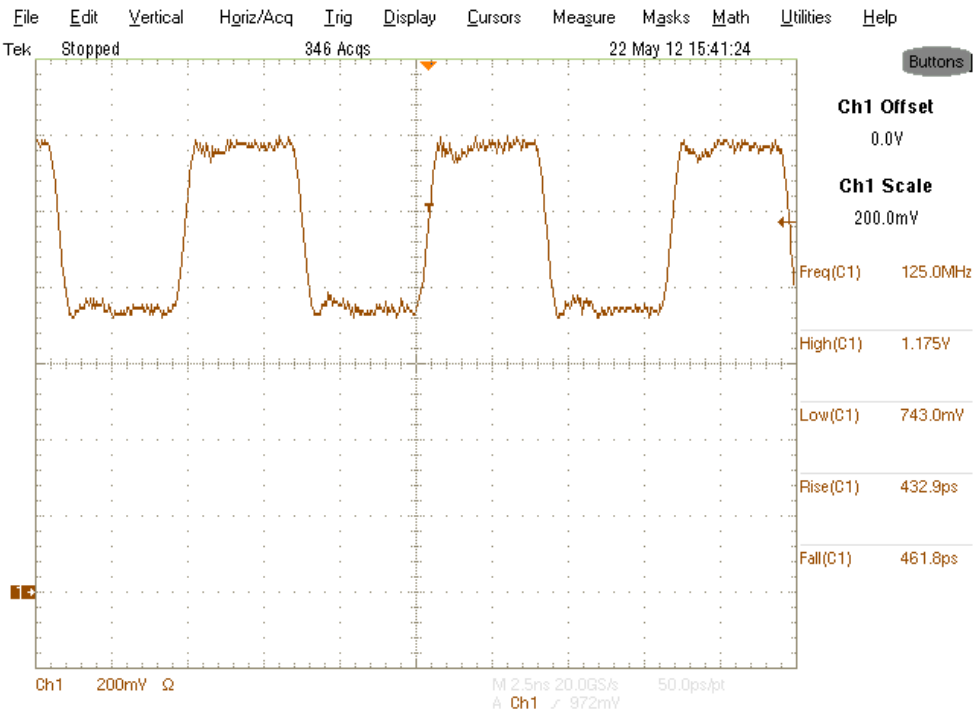
8.5 Using a single-ended signal to drive the differential reference clock input buffer

Though the VSC7512 reference clock input is differential with LVDS levels, it is possible to use it with a single-ended clock source. This is done by setting one differential input to a common-mode voltage and shaping the single-ended signal driving the other differential input so that it toggles around this common-mode voltage with a voltage swing comparable to LVDS. The reference clock differential input buffer will see this as a valid differential signal.

As the differential reference clock input has internal nominally 50R terminations to 1.0V (one 50R from REFCLK_P to 1.0V, one 50R from REFCLK_N to 1.0V), setting the REFCLK_N input to the common-mode voltage is achieved simply with a decoupling capacitor to ground – this ensures a 1.0V level on the REFCLK_N input.

Shaping the single-ended clock signal from an LVCMOS33 clock source to the levels required by the REFCLK_P input is achieved through a resistor divider. Note that because of the internal termination resistors in the reference clock input buffer, the 220R/430R external resistors proposed by the VSC7512 datasheet for dividing the clock signal do not simply decrease the voltage level on the REFCLK_P input to nominally 3.3V*430R/(220R+430R) = 2.2V – instead, the coltage level on the REFCLK_P input when voltage V is applied to the input of the 220R/430R resistor divider can be calculated as (Rbot*Rint*V+Rtop*Rbot*1.0V)/(Rtop*Rbot+Rbot*Rint+Rtop*Rint). With Rtop=220R, Rbot=430R and Rint=50R, then for V=3.3V the voltage level on the REFCLK_P input is calculated as 1.30V and for V=0V the voltage level on the REFCLK_P input is calculated as 0.74V, so a swing of approx ±250mV around the common-mode voltage 1.0V.

An actual measurement of a REFCLK_P input from a 3.3V single-ended source divided by 220R/430R resistors is shown below:



As the REFCLK_N input is set at 1.0V, the result seen by the reference clock input buffer is a pseudo-differential input with a peak-peak level of approx 250mV.

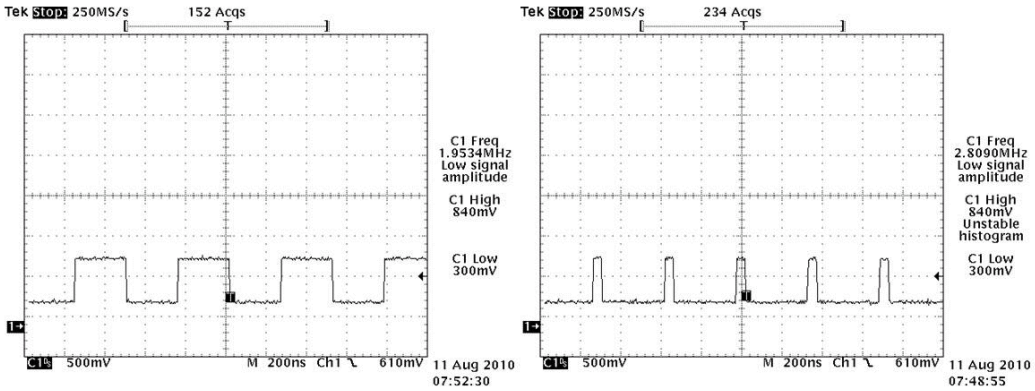
The voltage on any of the REFCLK pins should never exceed approx 1.25V, as that would trigger the input buffers' ESD protection diodes. Consult the devices' datasheets for exact values of this limit.

Note that differences in clock source output voltage levels, clock source output impedance, routing etc. may induce changes to the external voltage divider. The value of the dividing resistors is not important per se – what is important is the resulting signal as seen by the REFCLK_P input. This should be toggling around 1.0V with a swing as big as possible - a swing of ±200mV around the 1.0V common-mode voltage is safe regarding the ESD protection diode induced limits and also is big enough to offer reasonable noise margin.

Rise time of the signal presented to the REFCLK_P input is important. A decrease in rise time will result in less jitter seen by the REFCLK_P input. Consult the devices' datasheets for details and exact limits on rise time.

8.5.1 Monitoring PLL status

When debugging issues related to reference clock and PLL, the PLL's status can be monitored on a test signal output on the HS_TST_P pin. When the PLL is locked, implying that the reference clock input is sampled correctly, this test signal output toggles with a duty cycle of 50% - when the PLL is not locked it toggles with a duty cycle of 12.5%.



If the HS_TST_P signal is not available the health of the PLL can be induced from monitoring the MDC signal. When the PLL is locked this toggles with a frequency of 2.5MHz, when the PLL is not locked it toggles with a frequency of 4MHz. Note that after reset firmware can of course configure MDC for other frequencies.

9 Layout checklist

- Standard high-speed design layout techniques must be followed:
  - Minimize the number of signal vias.
  - No 90 deg bends - 45 deg bends or better curved traces can be used.
  - Traces must refer to a single power or ground plane, do not let high-speed traces pass plane splits on an adjacent layer.
  - In order to minimize crosstalk, the characteristic impedances of signals should be determined predominantly by the distance to the reference plane and not the distance to the neighboring traces.
  - Allow as much clearance between traces as possible, do not let two traces neighbor at a fixed low distance for extended lengths of trace.
  - Reduce trace length as much as possible, especially for high-speed single-ended signals (e.g. DDR) and very high-speed differential signals (e.g. QSGMII, XFI/SFI).
- Special care must be taken for the high-speed differential pairs (XFI/SFI/QSGMII/XAUI/SERDES/SGMII/PCIe etc.):
  - Must be routed as 100 ohms differential traces.
  - Allow as much clearance as possible between differential pairs, the well-known rule-of-thumb of “3*W” (W=width of trace) is absolute minimum, allow for 5*W or even 10*W clearance wherever possible to minimize crosstalk.
  - If guard traces or planes are used between individual pairs, use the same clearance constraints trace-to-plane as pair-to-pair (e.g. 3*W, 5*W or 10*W) to reduce the impact of the guard on the impedance of especially the trace (be that P or N) closest to the guard. Tie the guard to the inner layer ground plane frequently along the way – untied guards are good antennas.
  - Intra-pair skew (delta between lengths of P and N traces) must be as low as possible. E.g. for a 10Gbit/sec trace, an intra-pair skew of 3mm translates into 20ps or 20% of a bit, causing the differential receiver to read the signal with excessive jitter. “Nonchalance and high-speed don’t match”.
  - Inter-pair skew (delta between lengths of individual pairs) is typically less important. E.g. a XAUI interface can align lanes with up to 40 bits (12.8 ns / 2 meters) of inter-pair skew.
- 10/100/1000BASE-T signals are sensitive analog signals - that will be transmitted on up to 100 meters of UTP cable:
  - They must be routed from the PHY to magnetics, and from magnetics to the RJ45 connector, as four 100 ohm differential pairs for each port.
  - It is important to keep these signals away from noise sources. Differential (and some common mode) noise picked up by the signals between PHY and magnetics will end up as radiated emissions on the UTP cable. Differential as well as common mode noise picked up by the signals between magnetics and RJ45 connector will end up as radiated emissions on the UTP cable.

- It is also important to keep the two traces that make up a differential pair same length, as any difference in length will result in differential-to-common mode conversion of the signal and this will also end up as radiated emissions on the UTP cable.

- Low-bandwidth serial interfaces have fast edges too:
  - Even though the effective bandwidths of these interfaces are pretty low, it is important to avoid reflections on the multidrop clocks (MDC, I2C_SCL, SGPIO_CLK and SPI_CLK). Route the clock nets daisy-chained from the source to first consumer, then to the next consumer etc. and finally to the parallel termination network.
  - The pull-ups on MDIO and I2C_SDA must be present and can be placed where convenient.
- All power supplies must be routed as planes. Additional constraints:
  - Limit via sharing (where several power pins are connected to a single via) – ideally each power pin should be connected to its associated power plane through a dedicated via.
  - Surface mount local decoupling capacitors must be used and should be placed as close to the power supply pins as possible.
  - Analog supplies must be isolated from the remaining board supplies using ferrite beads.
  - Use a single ground point for the REF_REXT/REF_FILT resistor and capacitor.
- Simulate the completed design, and possibly selected signals during layout:
  - Simulate power integrity, e.g. power drops / current densities. Even though Microsemi devices are low power, small voltage drops on e.g. a 1.0V supply quickly add up to several percent of nominal voltage. If power integrity simulation shows issues, you can possibly solve them by using wider planes, or by using thicker planes (e.g. ½ oz -> 2 oz copper), or in some cases by using a remote sense point (located at the power consumer) for the DC/DC converter circuit.
  - Simulate signal integrity. DDR / SGMII / SERDES / XAUI / QSGMII / SFI / XFI signals are high speed, in some cases so high speed that it makes more sense to simulate on the layout file than to measure on the actual board. If a full simulation is not possible, then simulating e.g. a single lane of a multi-lane interface can still provide valuable insight. Microsemi supplies IBIS or IBIS-AMI models for its devices' high-speed inputs/outputs. Use the more accurate IBIS-AMI models when available, both for the target signal and for e.g. neighboring crosstalk aggressors.