Block diagram of VSC7512/VSC8514 unmanaged 8+2 port switch

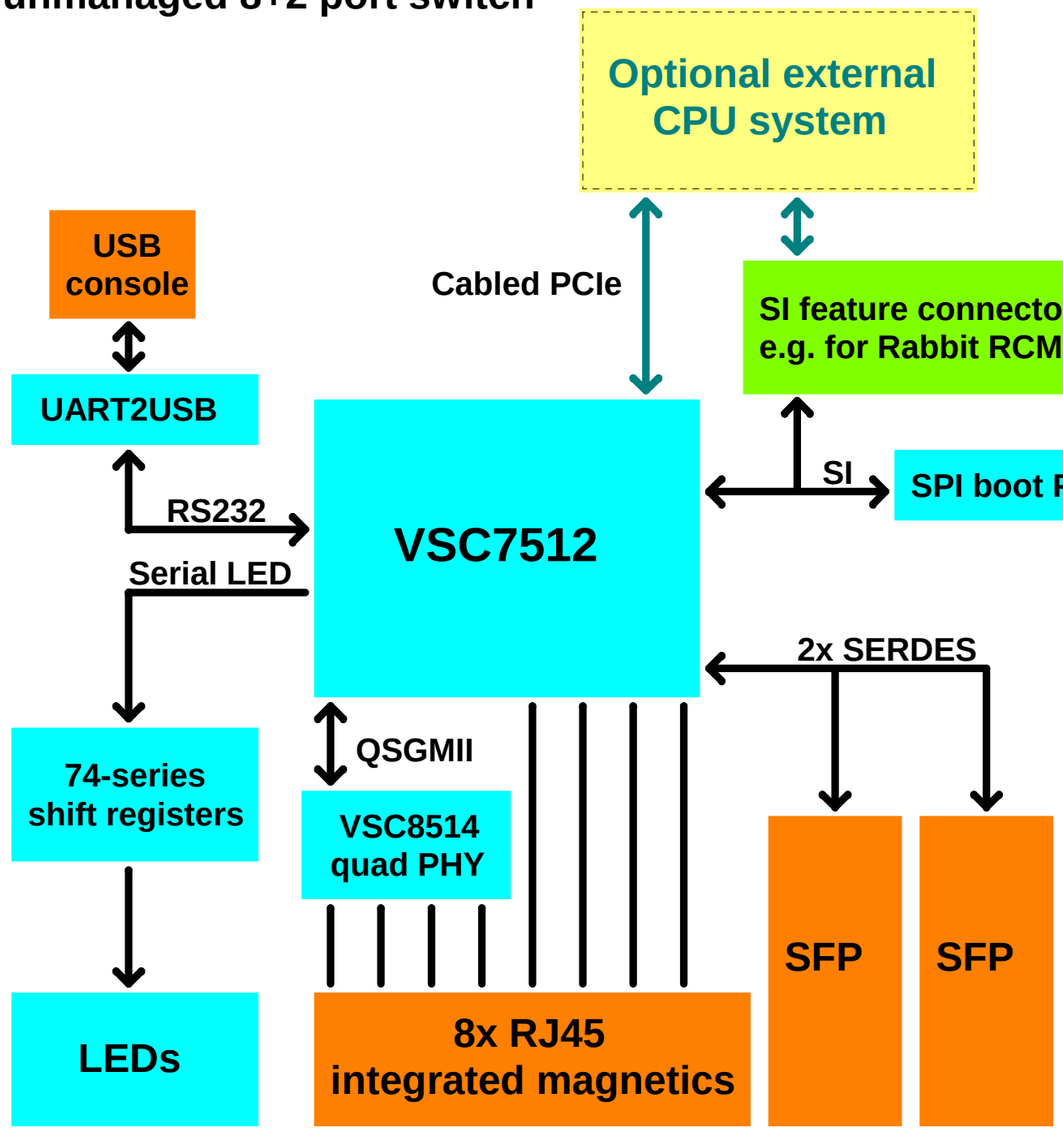
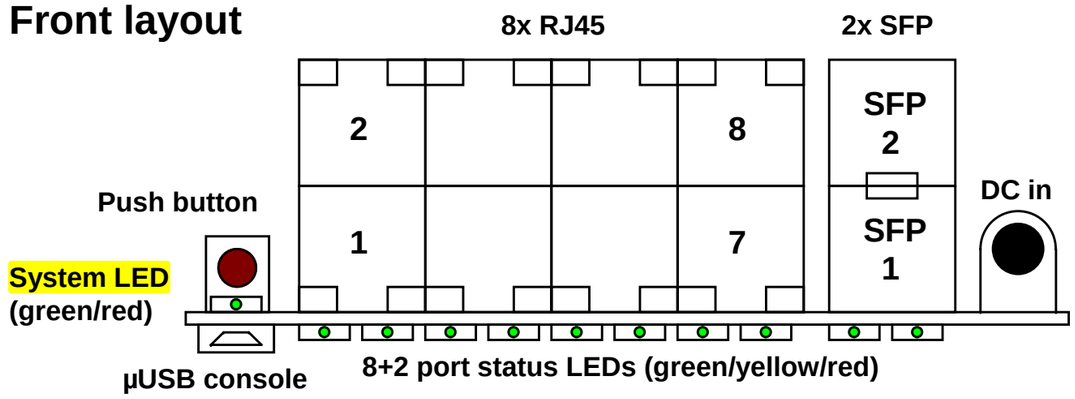


Table of contents

Revision history

Version:	Date:	Author:	Main change(s):
01-00	2015-11-03	MAG	First release
01-01	2016-02-10	MAG	Swapped R1/R8 (2V5 LDO)
01-02	2016-02-12	MAG	J10,C149,C150,C151,C155,C165,C166,C167,C168 mounted (was not mounted)
01-03	2016-04-14	MAG	Changes to U10 3V3/RESET, swap U4 S4 Rx polarity
01-04	2016-04-20	MAG	Swapped RD/GR labels on LTST-S326 (LED) inputs etc.
01-05	2016-05-24	MAG	Added R87/R88, added R92
02-00	2016-08-11	MAG	Changed VSC7512 reference clock input circuit

Front layout



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Title: Block diagram		
Size: A	Document Number: PCB121	Rev: 02-00
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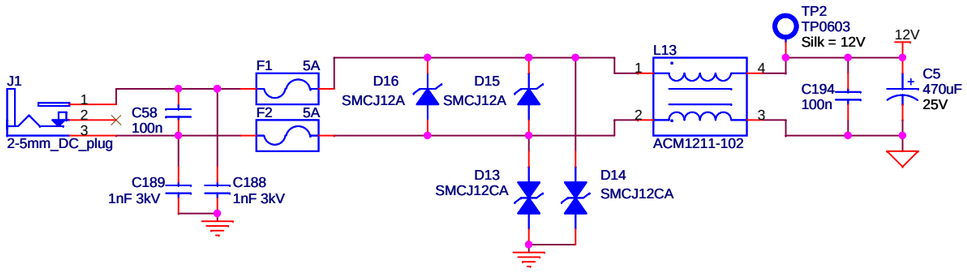
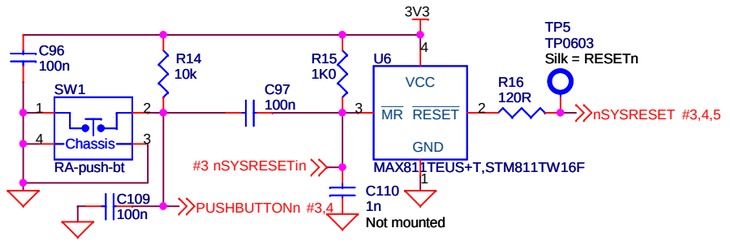
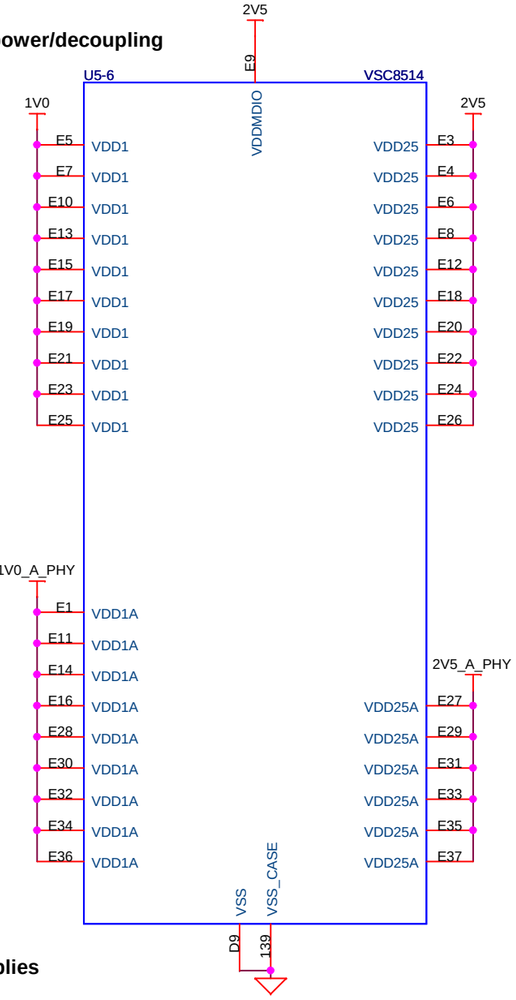
2.5mm center pin DC jack for external PSU



Reset generator

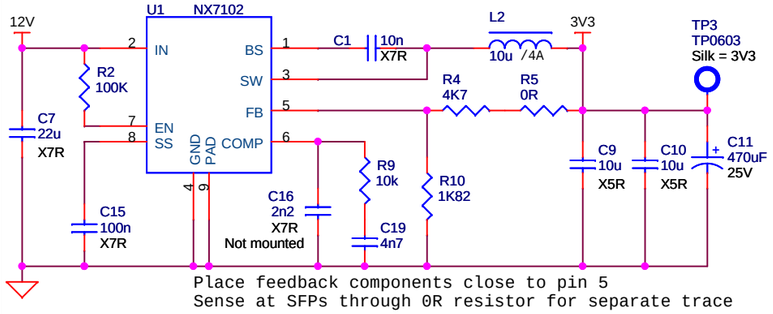


VSC8514 power/decoupling



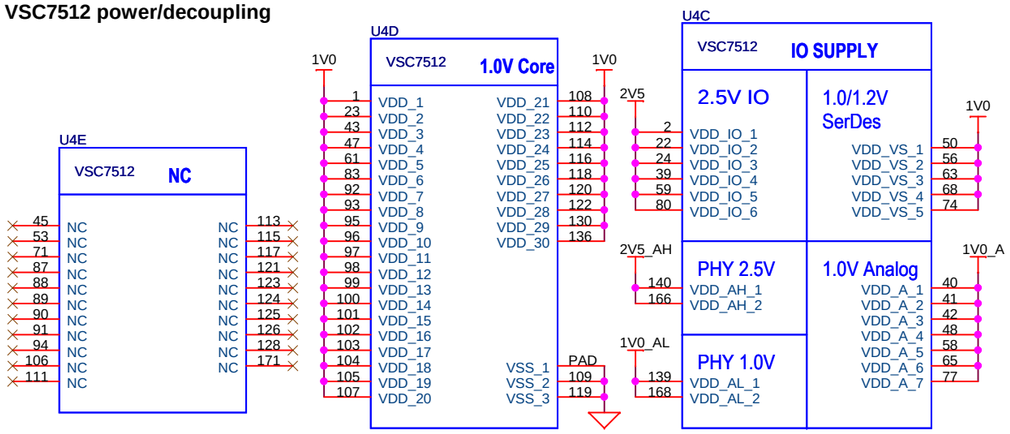
3V3 generation

Nominal output voltage = (0.925V/1K82)*(1K82+4K7) = 3.31V
Calculated current consumption on 3V3 = 2.2A

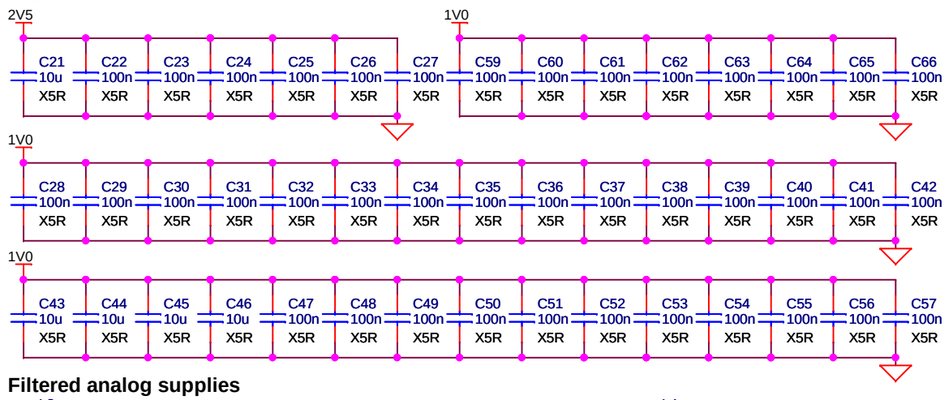


Place feedback components close to pin 5
Sense at SFPs through 0R resistor for separate trace

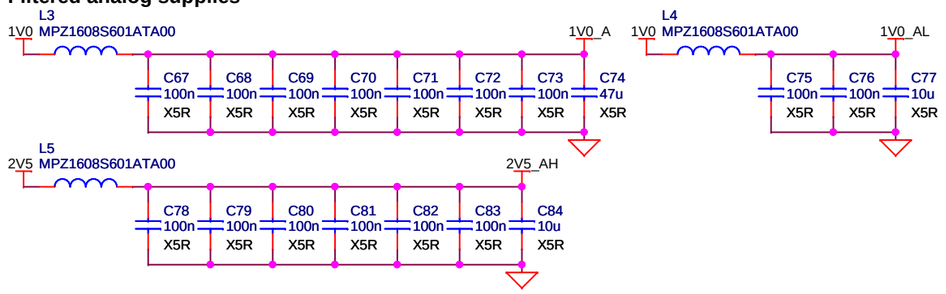
VSC7512 power/decoupling



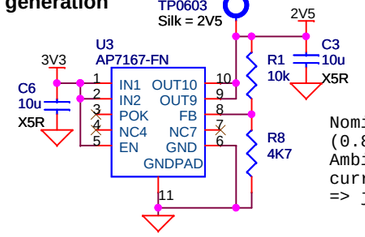
Digital supplies



Filtered analog supplies



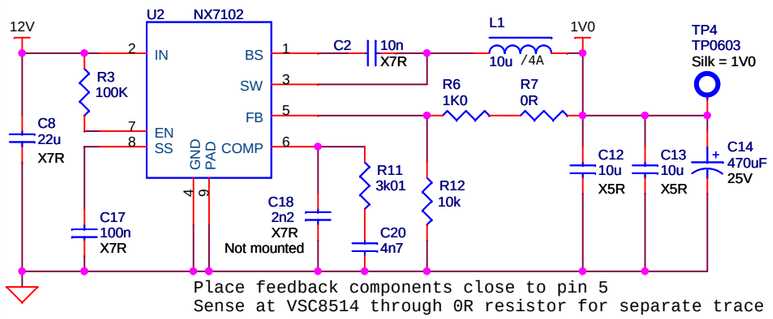
2V5 generation



Nominal output voltage =
(0.8V/4K7)*(10K+4K7) = 2.50V
Ambient temperature = 50*C,
current = 1.1A, Theta-JA = 40*C/W
=> junction temperature = 85*C

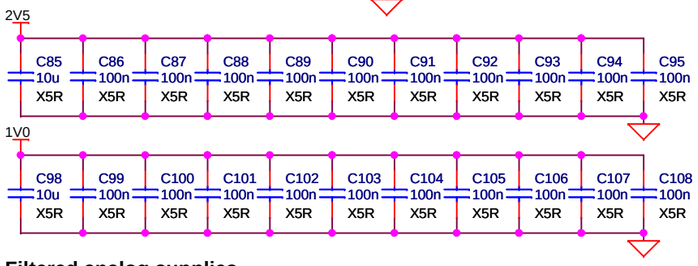
1V0 generation

Nominal output voltage = (0.925V/10K)*(1K+10K) = 1.02V
Calculated current consumption on 1V0 = 3.0A

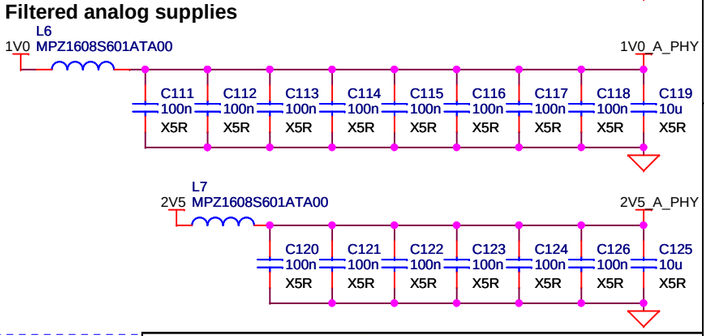


Place feedback components close to pin 5
Sense at VSC8514 through 0R resistor for separate trace

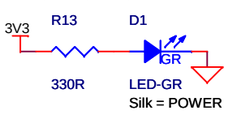
Digital supplies



Filtered analog supplies



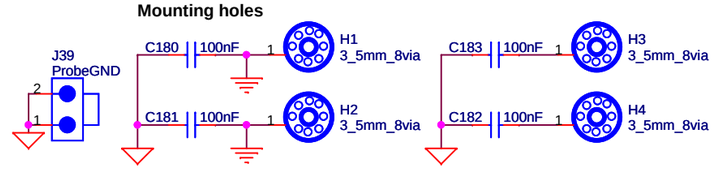
Power ON indicator



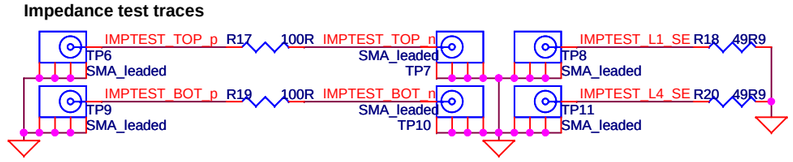
Silkscreen

H5 Ser_no_Box No:
H6 ECO_Box ECO:

Mounting holes



Impedance test traces



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Title	Power inlet, voltage conversion, VSCxxxx power/decoup, reset	
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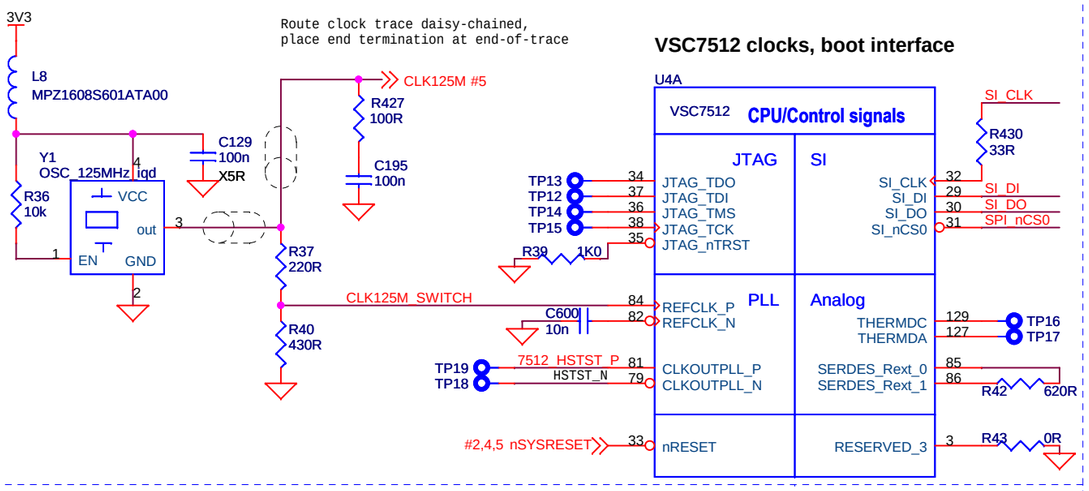
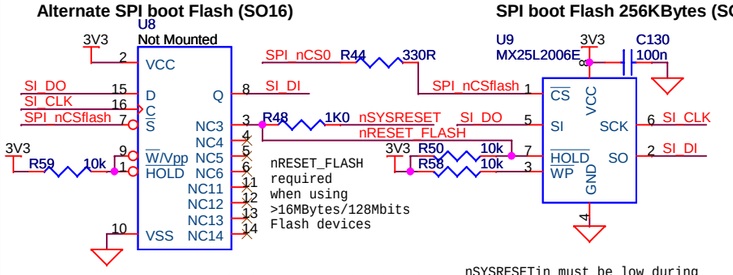
VSC7512 clocks, boot interface

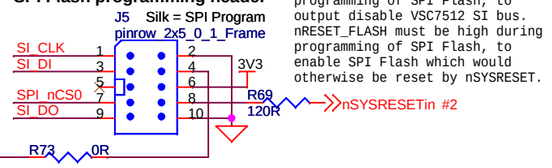


Alternate SPI boot Flash (SO16)



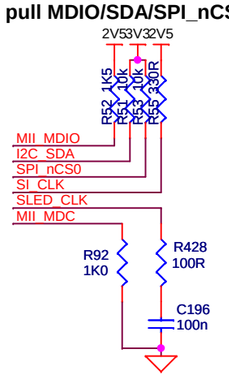
SPI boot Flash 256KBytes (SO8)

SPI Flash programming header

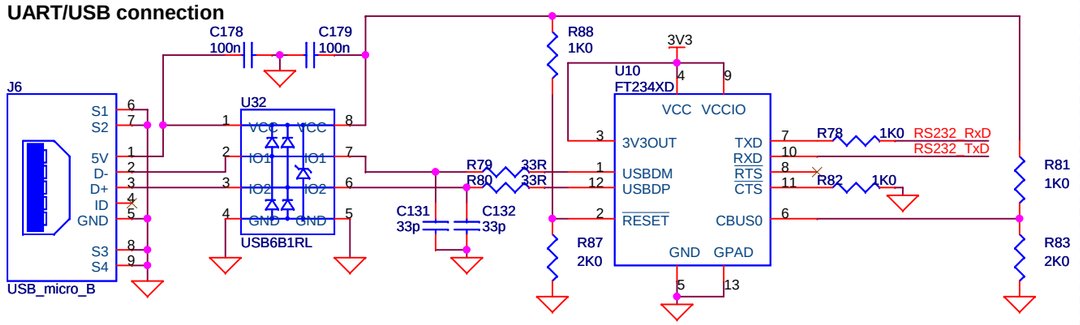


nSYSRESETin must be low during programming of SPI Flash, to output disable VSC7512 SI bus. nRESET_FLASH must be high during programming of SPI Flash, to enable SPI Flash which would otherwise be reset by nSYSRESET.

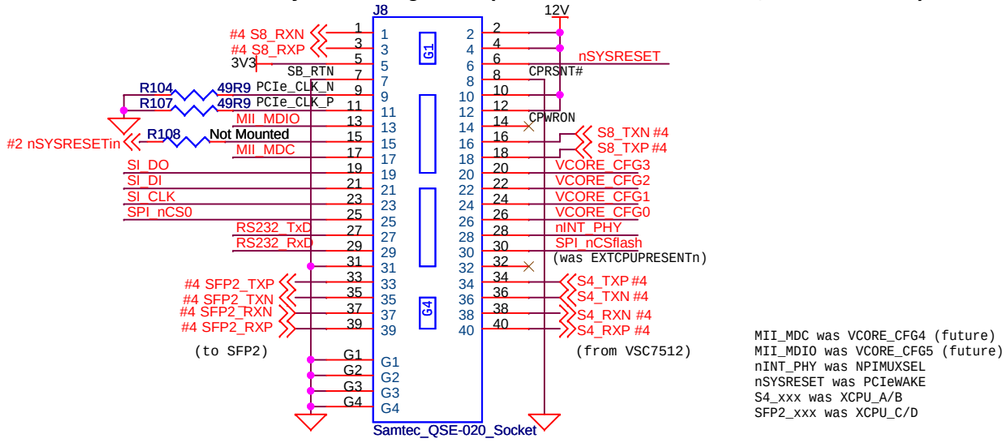
End termination of multidrop clocks, pull MDIO/SDA/SPI_nCS



UART/USB connection



Connection to external CPU system through PCIe (and/or 2nd SFP connection, and/or NPI PHY)



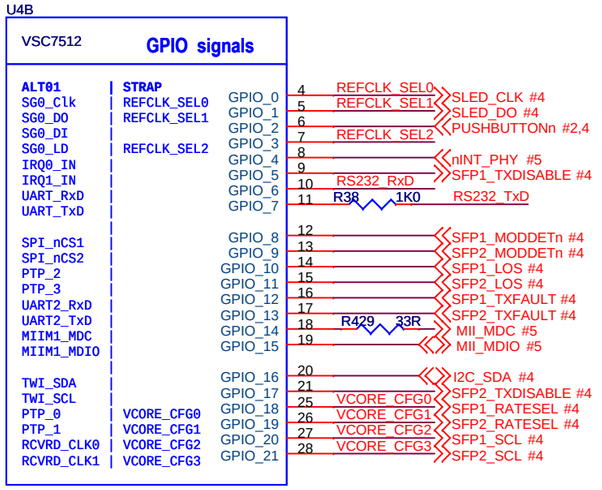
MII_MDC was VCORE_CFG4 (future)
MII_MDIO was VCORE_CFG5 (future)
nINT_PHY was NPIMUXSEL
nSYSRESET was PCIeWAKE
S4_xxx was XCPU_A/B
SFP2_xxx was XCPU_C/D

VSC7512 GPIO

VSC7512 GPIO alternate functions

GPIO #	ALT "10"	ALT "11"
0		
1		
2		
3		
4	IRQ0_OUT	TWI_SCL_MUX13
5	IRQ1_OUT	PCI_Wake
6	TWI_SCL_MUX0	
7	TWI_SCL_MUX1	
8	TWI_SCL_MUX2	IRQ0_OUT
9	TWI_SCL_MUX3	IRQ1_OUT
10	TWI_SCL_MUX4	SFP0_SD
11	TWI_SCL_MUX5	SFP1_SD
12	TWI_SCL_MUX6	SFP2_SD
13	TWI_SCL_MUX7	SFP3_SD
14	TWI_SCL_MUX8	SFP4_SD
15	TWI_SCL_MUX9	SFP5_SD
16		SPI_nCS3
17	TWI_SCL_MUX10	SPI_nCS4
18	TWI_SCL_MUX11_AD	
19	TWI_SCL_MUX12_AD	
20	TACHO	TWI_SCL_MUX14_AD
21	PWM	TWI_SCL_MUX15_AD

U4B

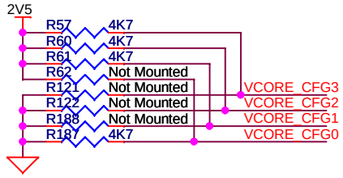


SFP signals on GPIOs:
- TXFAULT requires pullup (open drain)
- MODDETn requires pullup (open drain)
- RATESEL has no special requirements
- TXDISABLE requires pullup (TX init disabled)

Pullups are on SFP sheet

VSC7512 boot mode strapping

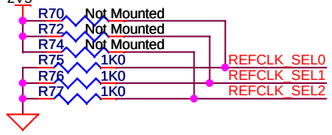
VCore_Cfg[3:0]	VCore-III CPU Behavior
0 0 0 0	Reserved.
0 0 0 1	8051 IROM boot. Reserved for port-bringup.
0 0 1 0	8051 IROM boot. Reserved for port-bringup.
0 0 1 1	8051 IROM boot. Reserved for port-bringup.
0 1 0 0	8051 IROM boot. Reserved for port-bringup.
0 1 0 1	8051 IROM boot. Reserved for port-bringup.
0 1 1 0	8051 IROM boot. Reserved for port-bringup.
0 1 1 1	8051 IROM boot. Reserved for port-bringup.
1 0 0 0	8051 IROM boot. NPI:1G FDX NoFC, VRAP.
1 0 0 1	8051 IROM boot. PCIe
1 0 1 0	No boot. SI slave and MIIM slave @ address 0 (GPIO alternative).
1 0 1 1	No boot. SI slave and MIIM slave @ address 31 (GPIO alternative).
1 1 0 0	Reserved.
1 1 0 1	Reserved.
==> 1 1 1 0	8051 boots from SI interface.
1 1 1 1	No boot. SI slave is enabled.



VSC7512 PLL strapping

REFCLK_SEL[2:0]	Frequency	Comment
==> 000	125MHz	The default mode. Normal operation mode with 125MHz
001	156.25MHz	Normal operation mode with 156.25MHz ref clock
010	250MHz	Normal operation mode with 250MHz ref clock
011	N/A	Reserved
100	25MHz	Normal operation mode with 25MHz ref clock
101	N/A	Reserved
110	N/A	Reserved
111	N/A	Reserved

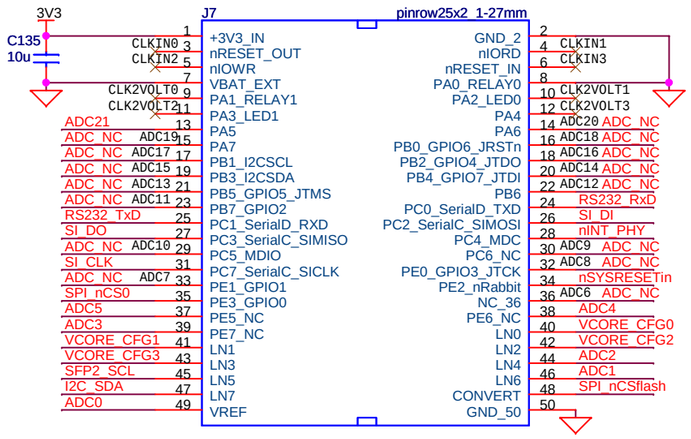
Due to VSC7512 jitter requirements, don't use 25MHz REFCLK as base for QSGMII



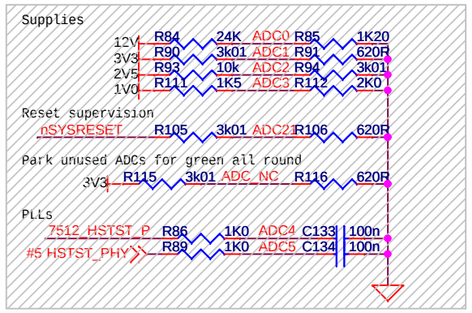
Board I2C address table

Address	I2C slave
1010xxx	SFP transceiver

Optional receptacle for Rabbit RCM40xx CPU module (for connecting external CPU to VSC7512 SI)



Rabbit connector has double duty as connector for Microsemi QuickTest module, enabling test of selected PCB signals (definitely optional!). ADC nominal input voltage 0.57V.



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Title: Switch memory (SPI boot Flash, GPIO, PCIe, clocks, strapping

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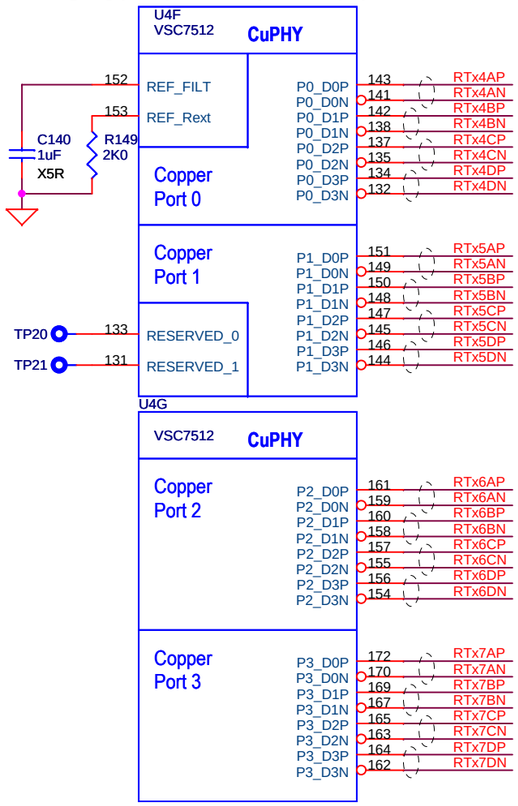
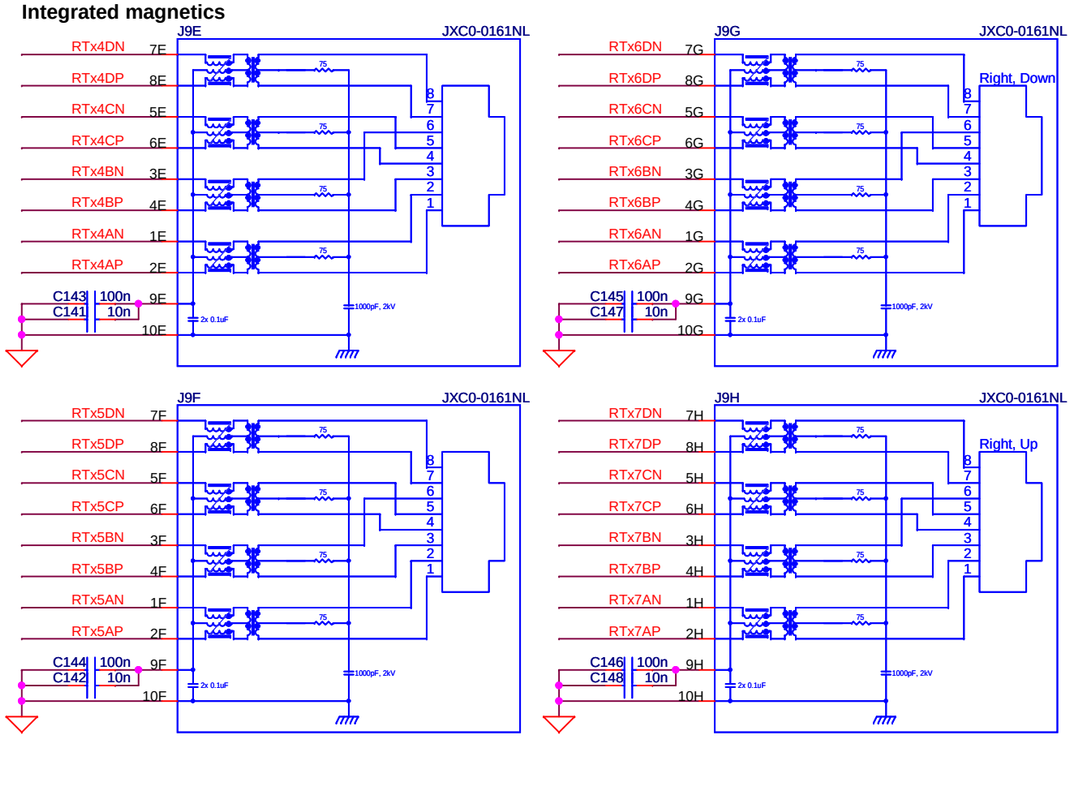
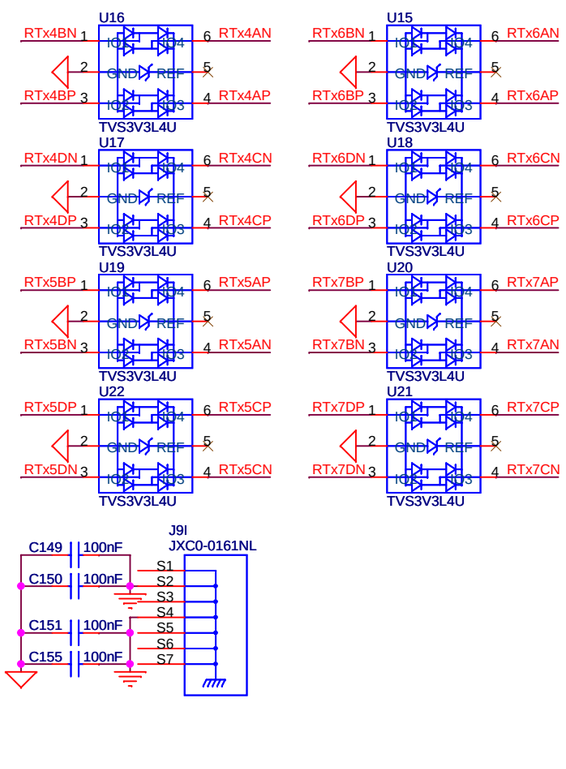
RJ45[8:5] (1Gbps/100Mbps/10Mbps)



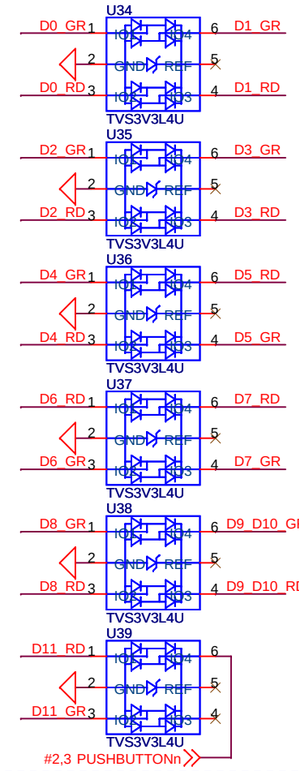
Integrated magnetics



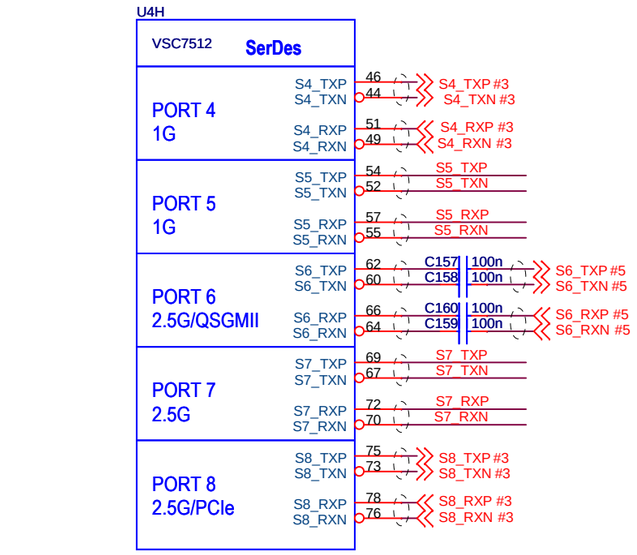
TVS protection on 1000BASE-T signals



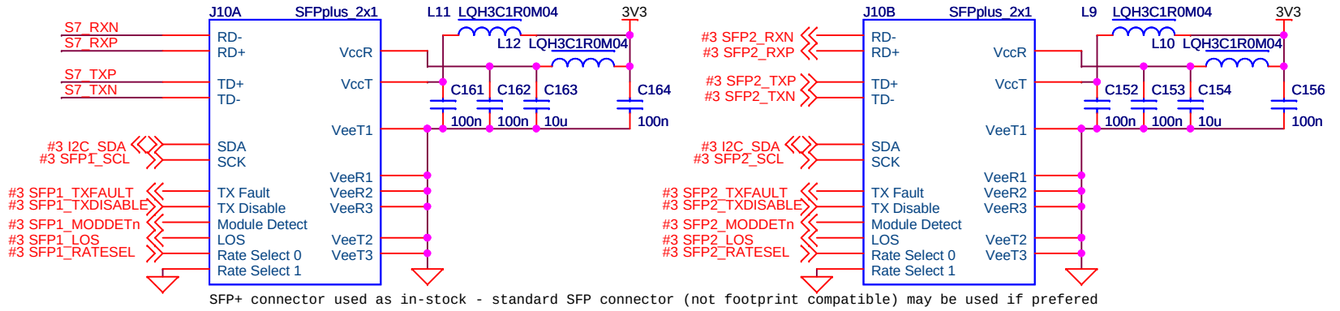
TVS protection on LED signals



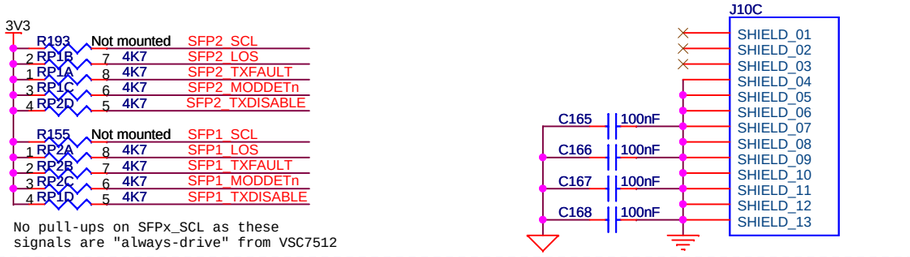
SFP[2:1] (2.5Gbps/1Gbps/100Mbps)



SFP connectors and cage



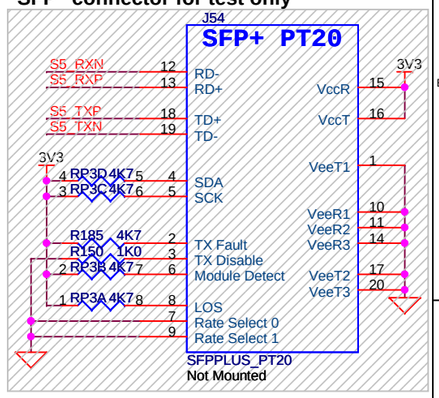
SFP+ connector used as in-stock - standard SFP connector (not footprint compatible) may be used if prefered



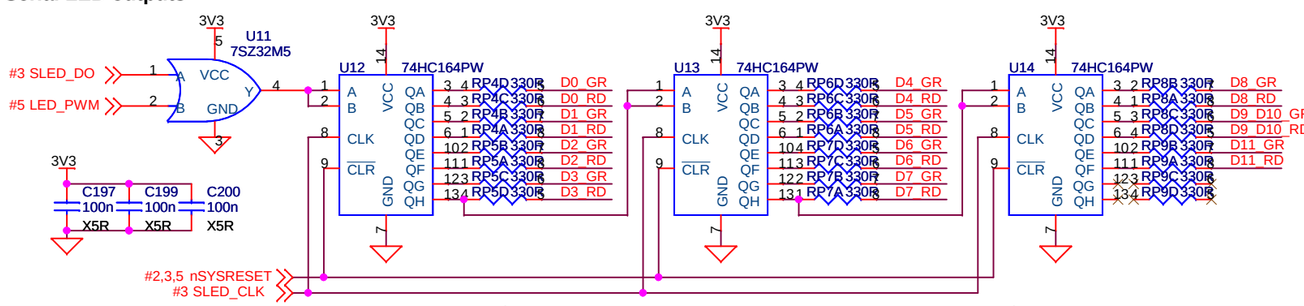
No pull-ups on SFPx_SCL as these signals are "always-drive" from VSC7512

SERDES usage:
- S5 only used for test
- S6 connects to VSC8514 through QSGMII
- S7 (2.5Gbps) connects to SFP1
- Config 0: S4 (1Gbps) connects to NPI on breakoff and S8 (2.5Gbps) connects to SFP2 through breakoff
- Config c: S4 (1Gbps) connects to SFP2 through breakoff and S8 (2.5Gbps) connects to PCIe on breakoff board

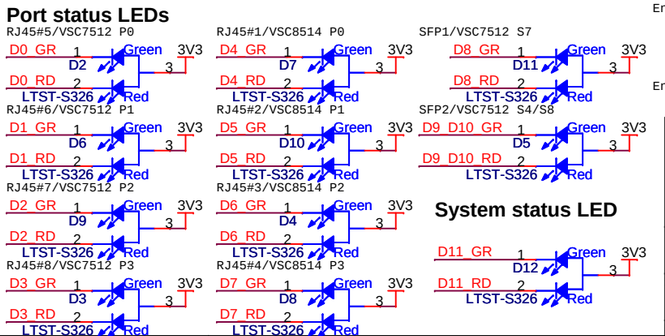
"SFP" connector for test only



Serial LED outputs



Port status LEDs



System status LED

Enable SLED ports 7:0 as port status LEDs for 8x RJ45 ports (SLED port 0 is VSC7512 P0/RJ45#5, SLED port 4 is VSC8514 P0/RJ45#1, etc.),
SLED port 8 as LED for SFP1 through S7,
SLED port 9 as LED for 1G SFP2 through S4 (config c/PCIe only),
SLED port 10 as LED for 2.5G SFP2 through S8 (config 0 only),
SLED port 11 as system status LED
Enable two bits per port,
bit[1:0]=00 => yellow, 01 => red, 10 => green, 11 => off.

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Title: VSC7512 ports, LEDs

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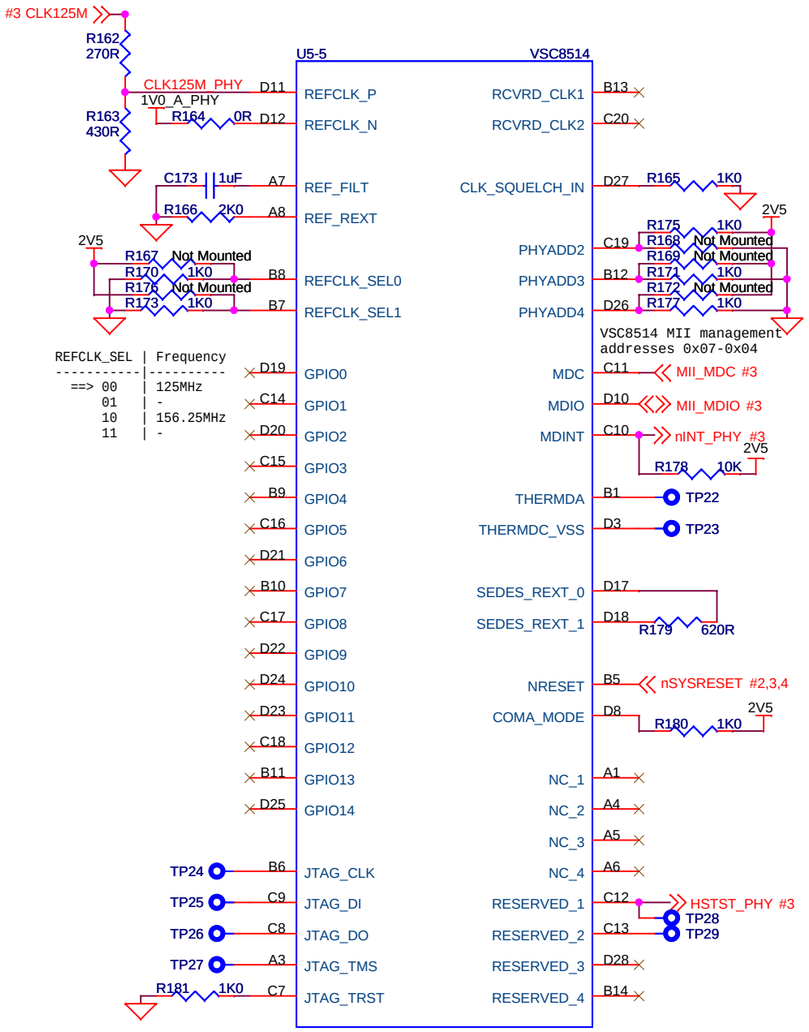
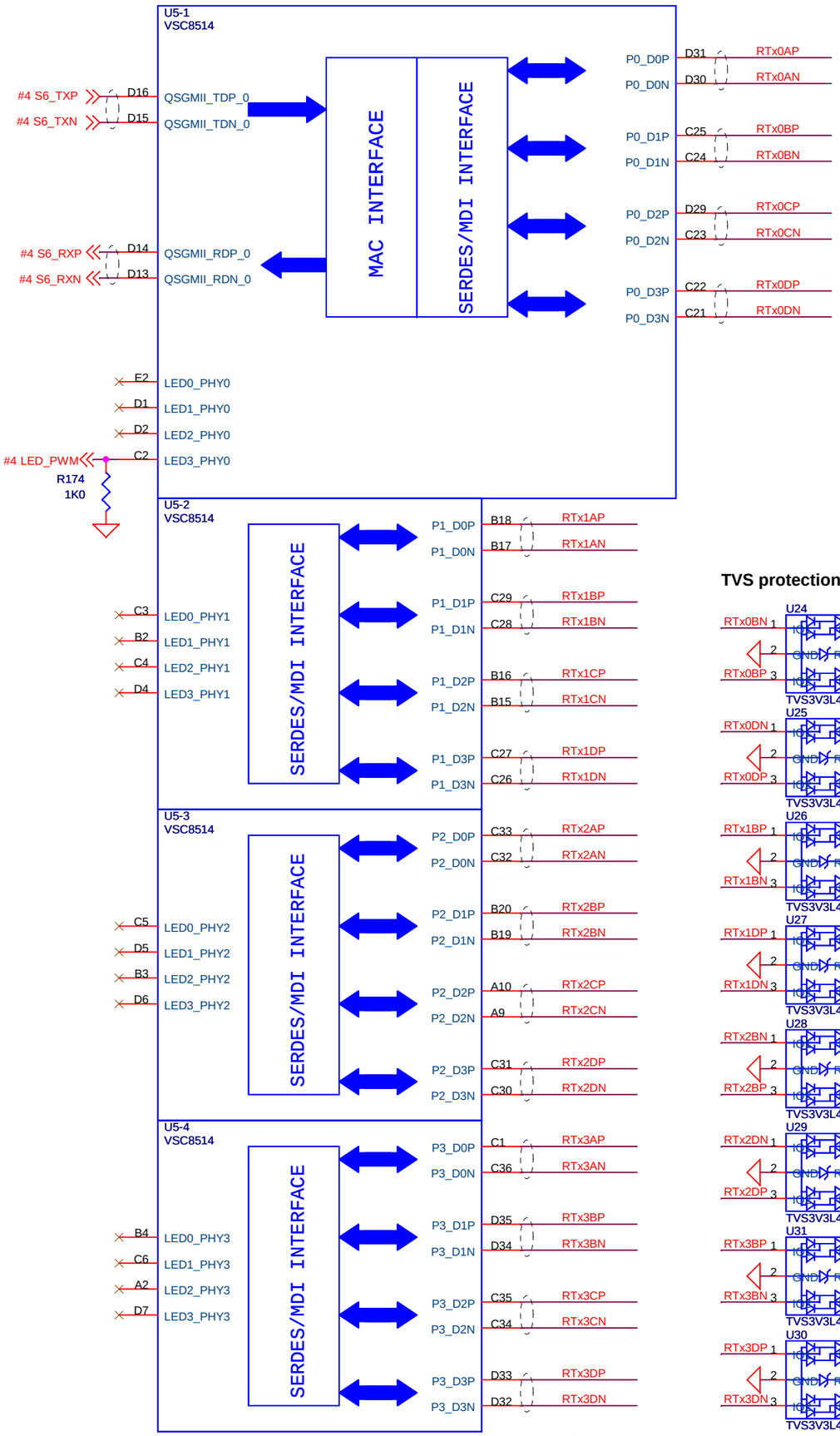
RJ45[4:1] (1Gbps/100Mbps/10Mbps)

VSC8514 I/O and strapping

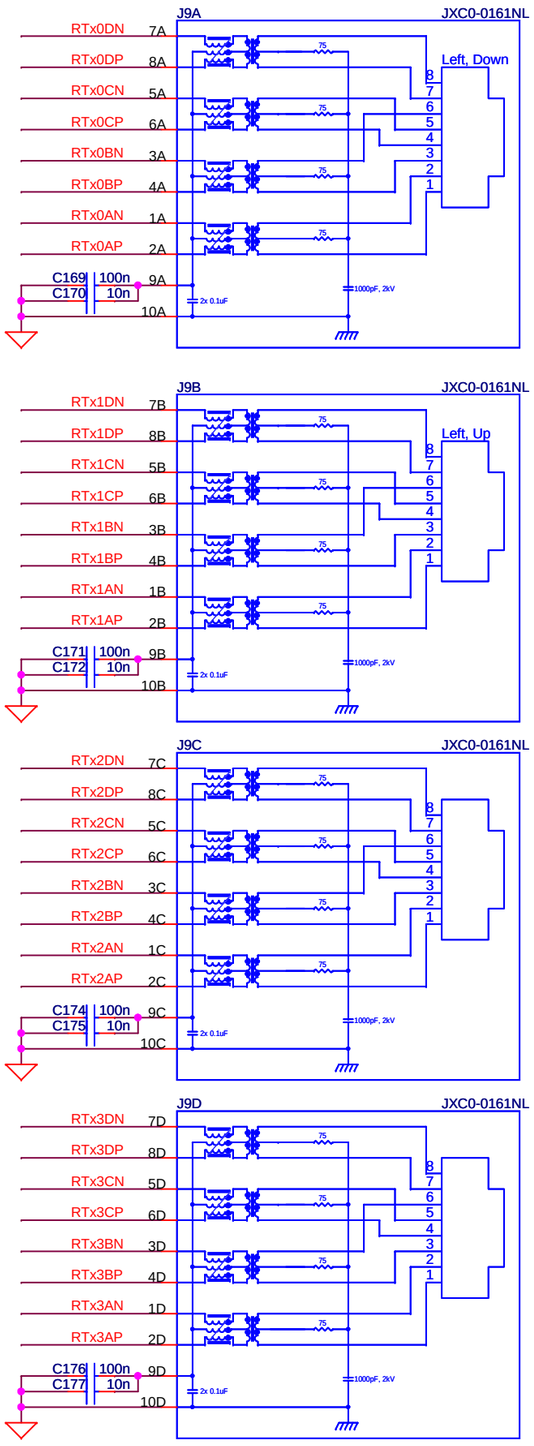


VSC8514 QSGMII/ports



TVS protection

Integrated magnetics



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Title: VSC8514		
Size: A3	Document Number: PCB121	Rev: 02-00
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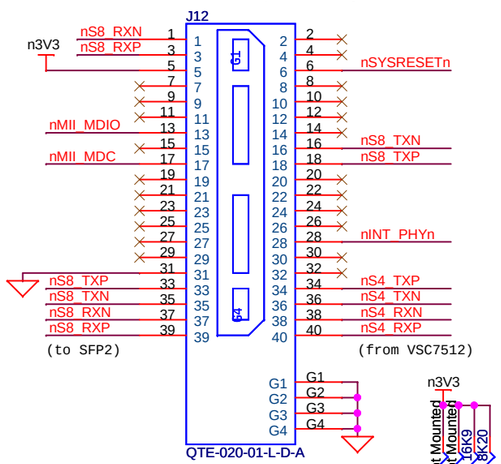
Breakoff board for connecting NPI PHY to mainboard S4 (SFP2 is 2.5Gbps S8)

Samtec connector towards mainboard, feedthrough of S8 to SFP2



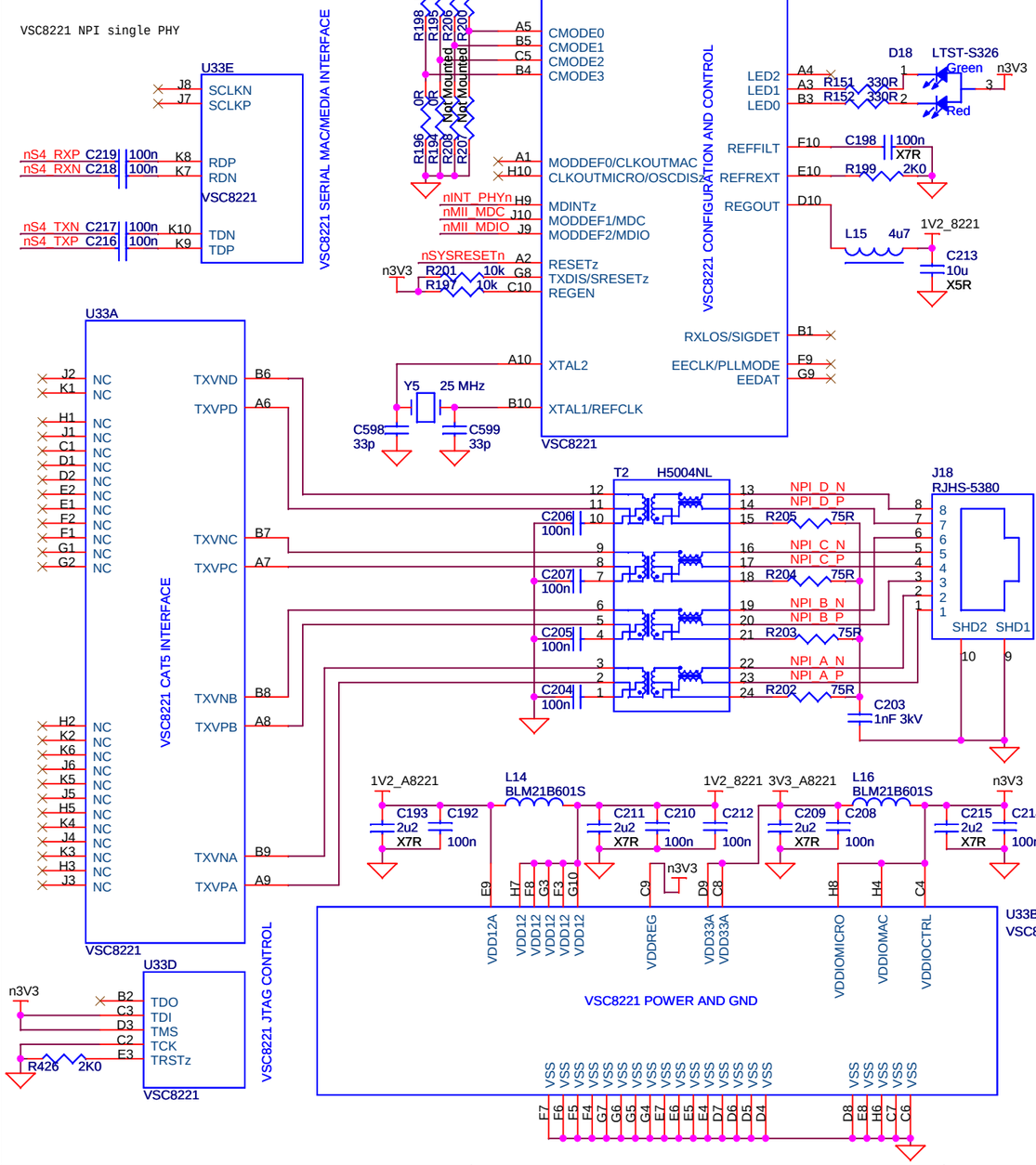
CMODE pull-up/pull-down to digital translation

With CMODE pin tied to	. with 1% . res val	Set bit 3 to:	Set bit 2 to:	Set bit 1 to:	Set bit 0 to:
GND	0	0	0	0	0
GND	2.26k	0	0	0	1
GND	4.02k	0	0	1	0
GND	5.90k	0	0	1	1
GND	8.25k	0	1	0	0
GND	12.1k	0	1	0	1
GND	16.9k	0	1	1	0
GND	22.6k	0	1	1	1
3V3	0	1	0	0	0
3V3	2.26k	1	0	0	1
3V3	4.02k	1	0	1	0
3V3	5.90k	1	0	1	1
3V3	8.25k	1	1	0	0
3V3	12.1k	1	1	0	1
3V3	16.9k	1	1	1	0
3V3	22.6k	1	1	1	1

VSC8221 CMODE strapping

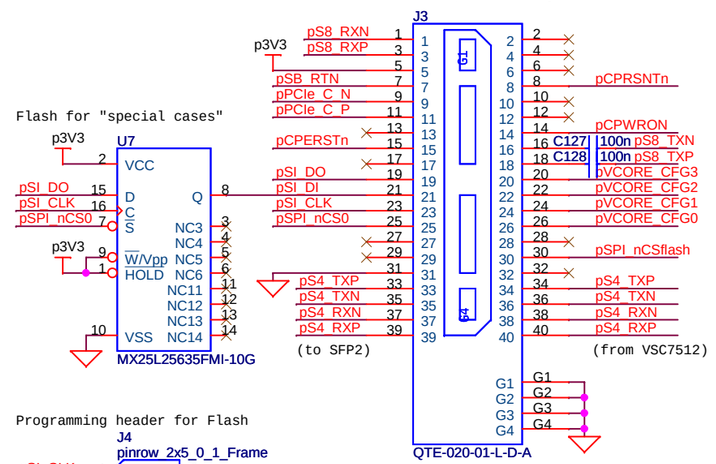
Pin	Bit 3 control	Bit 2 control	Bit 1 control	Bit 0 (LSB) control
3	LED control[1] 0=>link/act	SQE enable 0=>SQE disabled	Reserved -	Autoneg ctrl[1] 0=>10/100/1000Base
2	Operating mode[3:0], 0000=>SERDES to CAT5, SCLK disabled			
1	SFP mode 1=>SFP disable	PHY address[4] 1	SIGDET direct 1=>Output	Line impedance 0=>50R
0	PHY address[3:0], (1)1100=>0x1c, 28 dec			

VSC8221 NPI single PHY



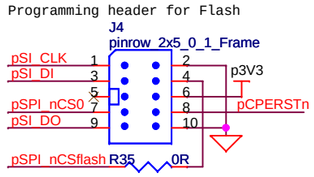
Breakoff board for connecting PCIe cable to mainboard S8 (SFP2 is 1Gbps S4)

Samtec connector towards mainboard, feedthrough of S4 to SFP2

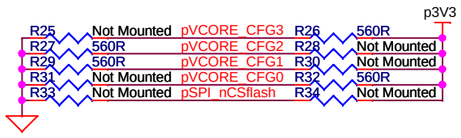


Flash for "special cases"

Programming header for Flash

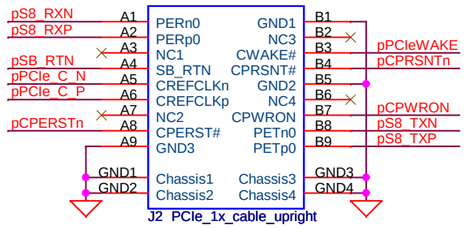


Override VCORE_CFG of mainboard, for plug&play PCIe



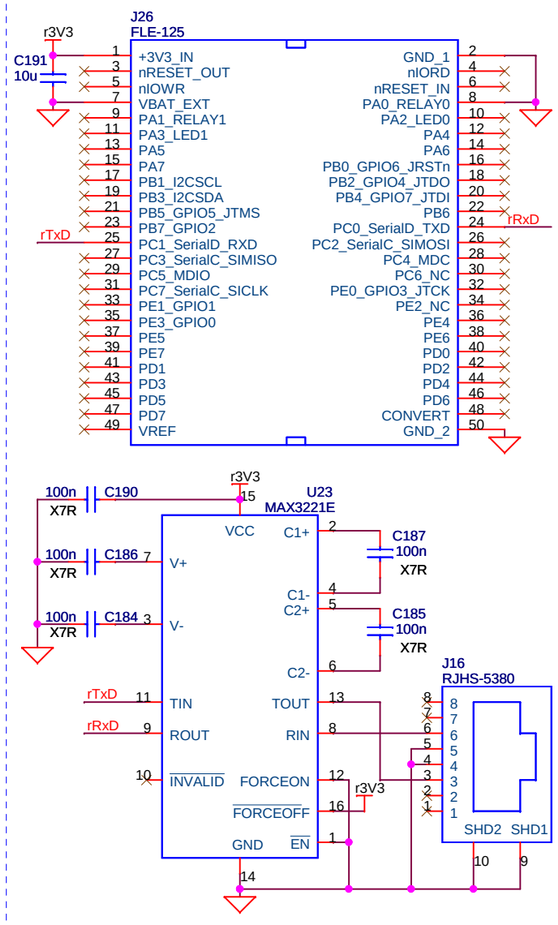
No PCIeWAKE from this mainboard (use in-band beacon instead)

PCIe 1x cable connector for S8 from mainboard



Note, PCIe interface for use in controlled lab environment, so
(1) no power domain isolation,
(2) high-impedance when powered off not guaranteed for CWAKE#, CPRSNT#, CPERST#,
(3) spread spectrum clocked PCIe hosts not supported

Breakoff board with RS232 port for old-school management



Hoerkaer 16
DK-2730 Herlev
Denmark

MAG

Microsemi

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Title	Breakoffs for PCIe, NPI PHY and 2nd SFP source selection - and RS232	
Size A3	Document Number PCB121	Rev 02-00
Date: Thursday, August 11, 2016	Sheet 6 of 6	