

Block diagram of VSC7512/VSC8514
unmanaged 8+2 port switch

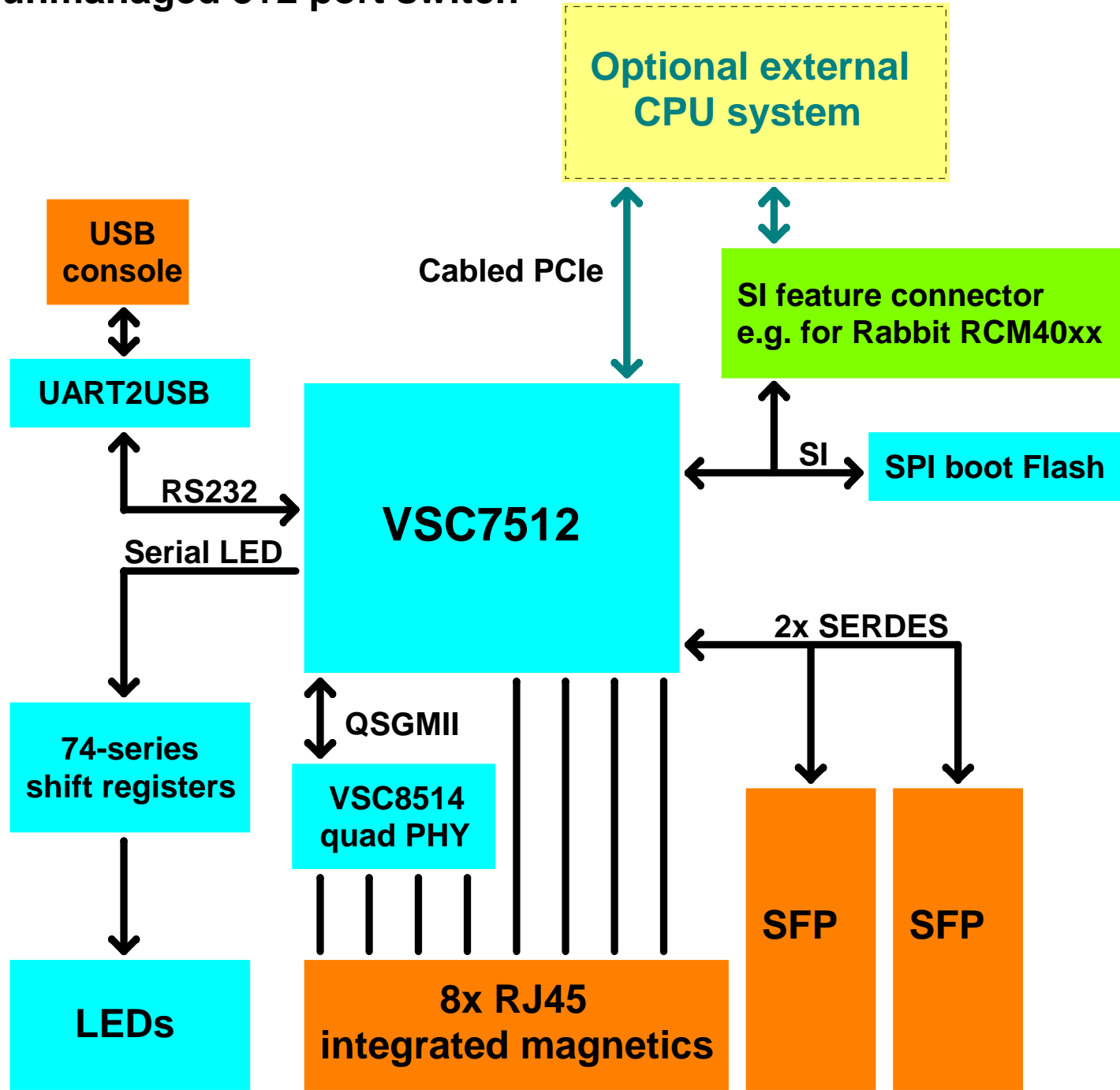


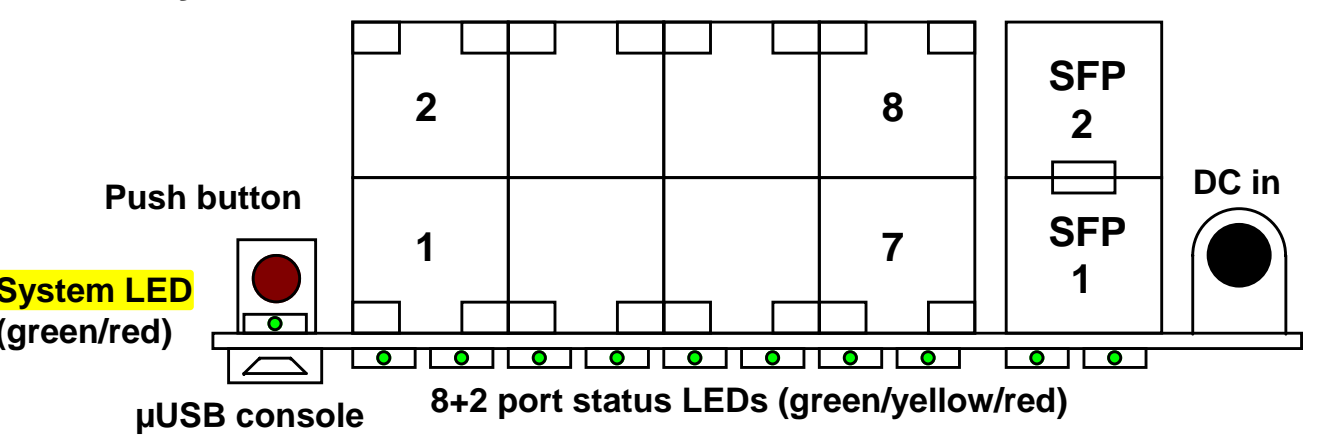
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Revision history

Version:	Date:	Author:	Main change(s):
01-00	2015-11-03	MAG	First release
01-01	2016-02-10	MAG	Swapped R1/R8 (2V5 LDO)
01-02	2016-02-12	MAG	J10,C149,C150,C151,C155,C165,C166,C167,C168 mounted (was not mounted)
01-03	2016-04-14	MAG	Changes to U10 3V3/RESET, swap U4 S4 Rx polarity
01-04	2016-04-20	MAG	Swapped RD/GR labels on LTST-S326 (LED) inputs etc.
01-05	2016-05-24	MAG	Added R87/R88, added R92
02-00	2016-08-11	MAG	Changed VSC7512 reference clock input circuit

Front layout



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MAG

Title
Block diagram

Size
A

Date:
Thursday, August 11, 2016

Microsemi

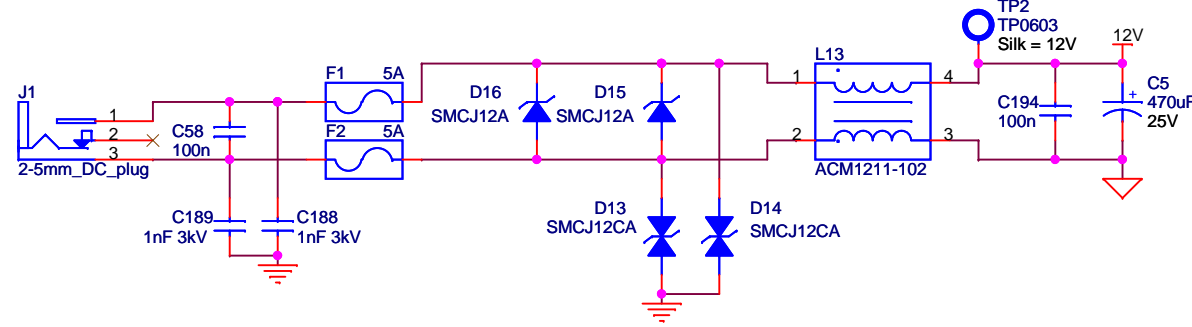
Company Confidential

Document Number
PCB121

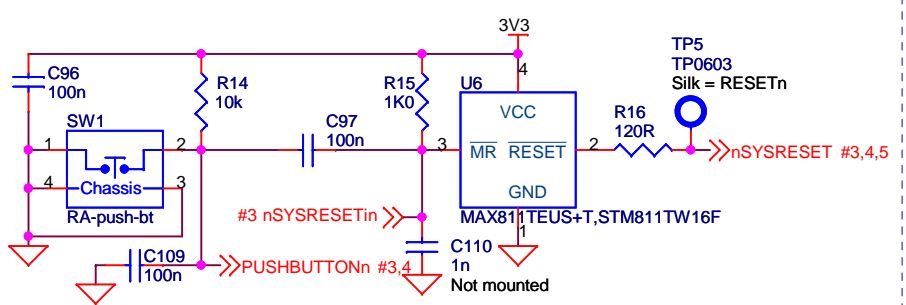
Rev
02-00

Sheet
1 of 6

2.5mm center pin DC jack for external PSU

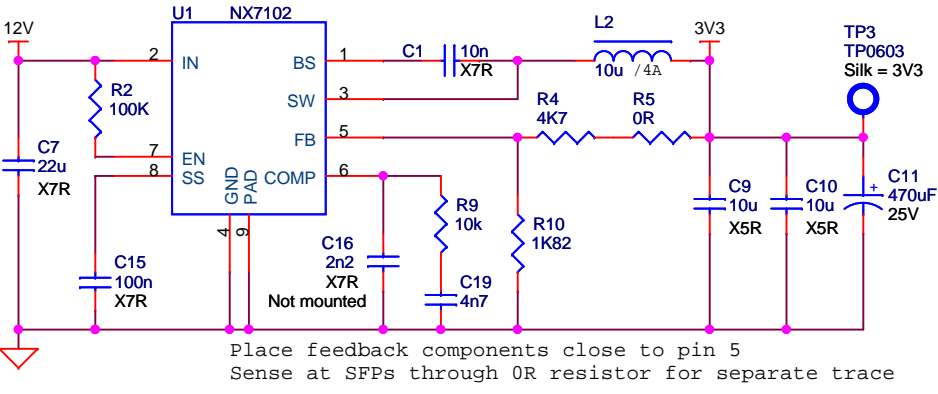


Reset generator

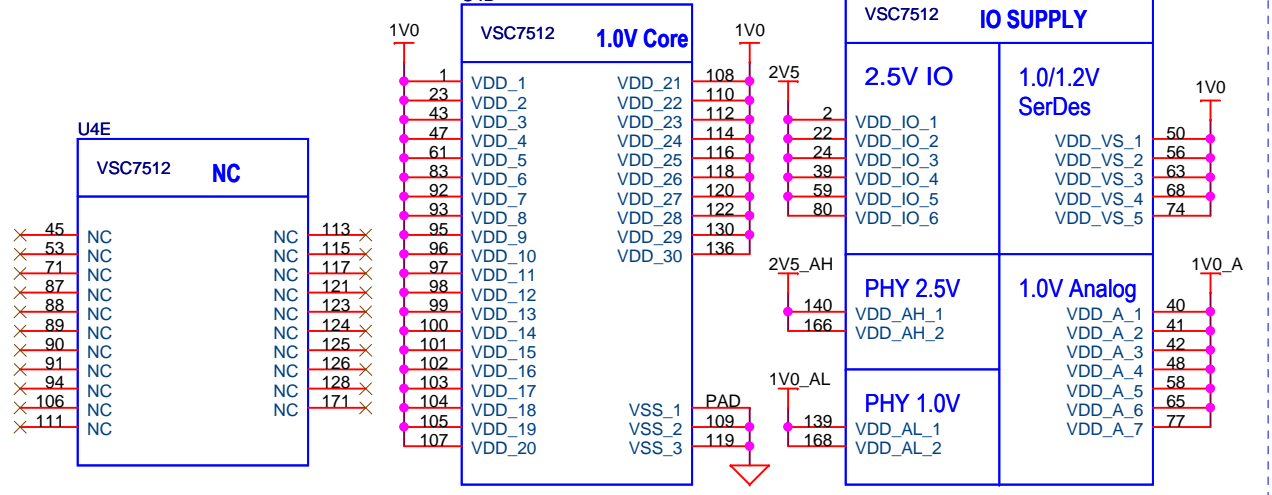


3V3 generation

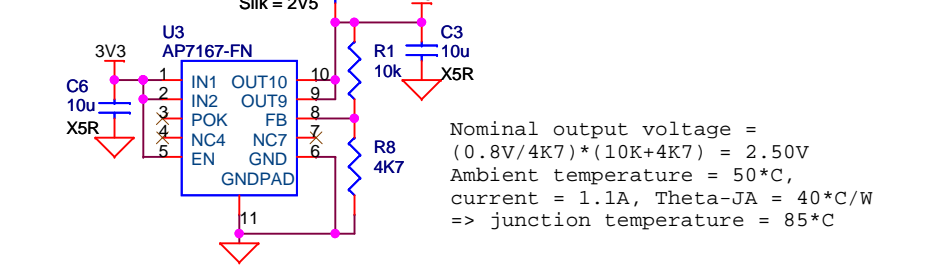
Nominal output voltage = $(0.925V/1K82) * (1K82 + 4K7) = 3.31V$
Calculated current consumption on 3V3 = 2.2A



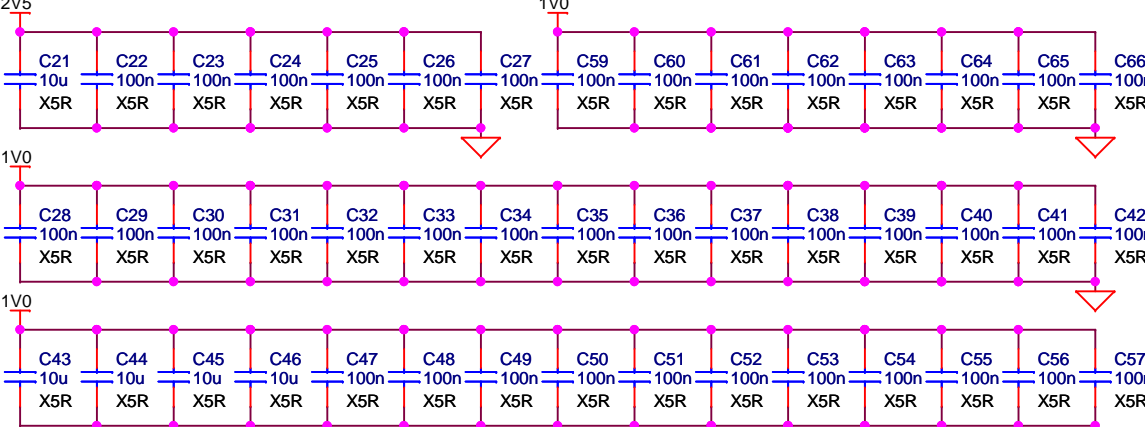
VSC7512 power/decoupling



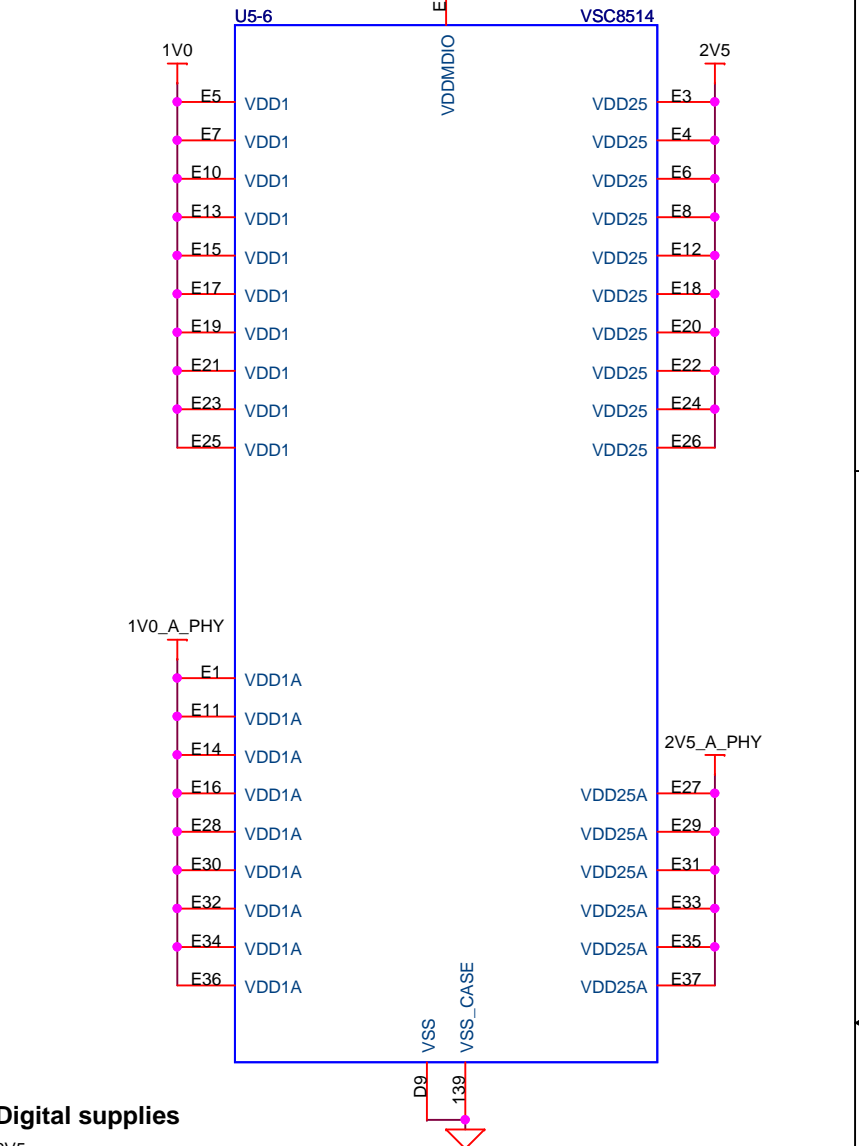
2V5 generation



Digital supplies

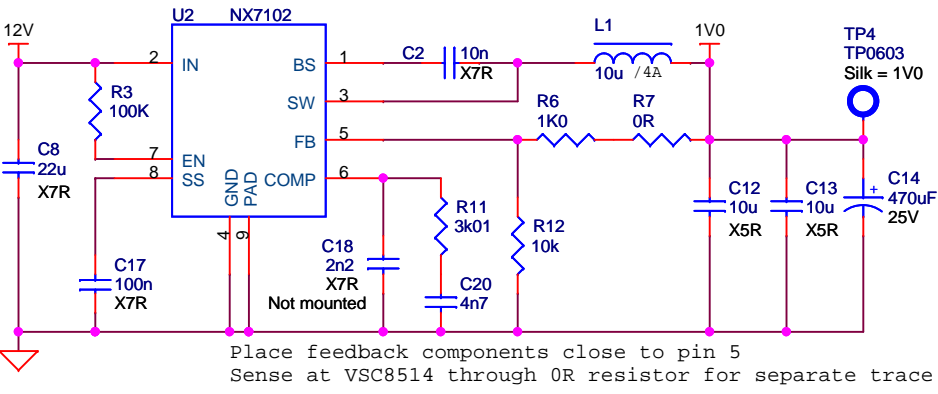


VSC8514 power/decoupling

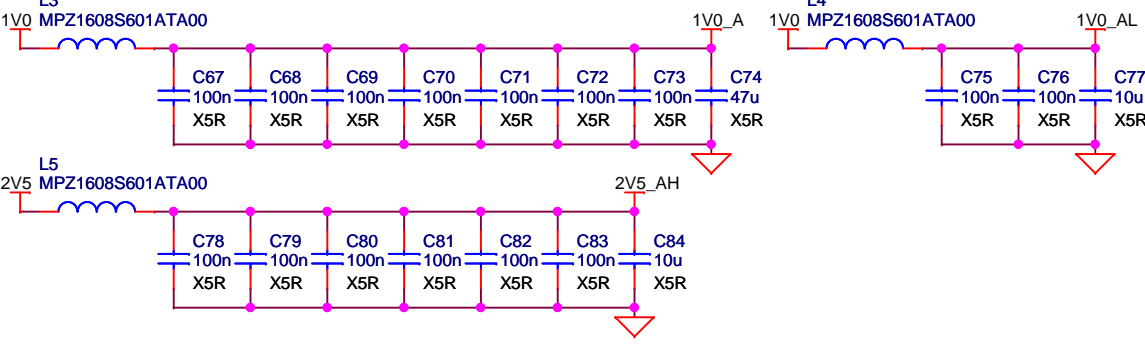


1V0 generation

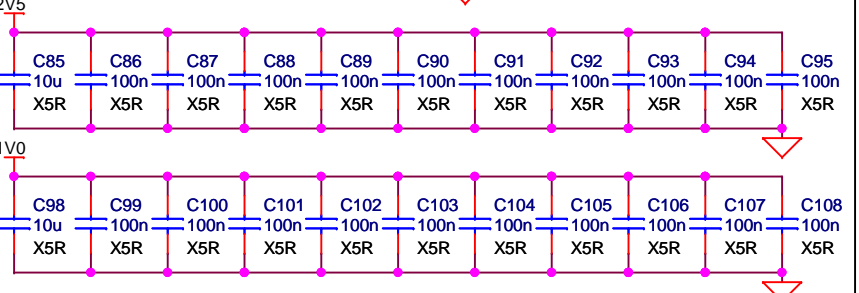
Nominal output voltage = $(0.925V/10K) * (1K + 10K) = 1.02V$
Calculated current consumption on 1V0 = 3.0A



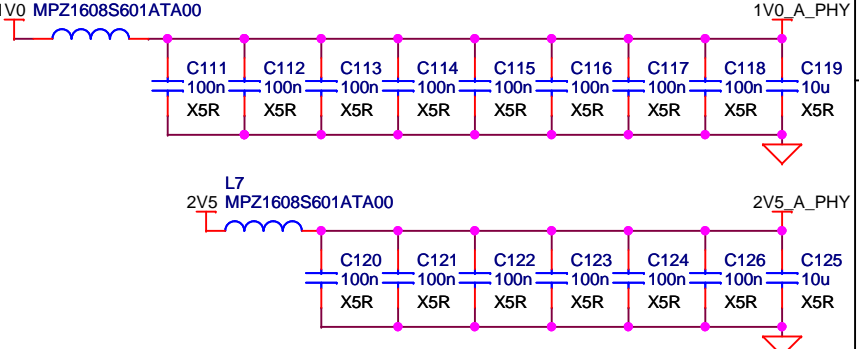
Filtered analog supplies



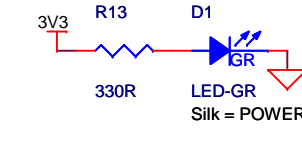
Digital supplies



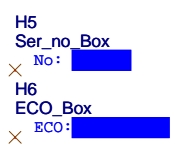
Filtered analog supplies



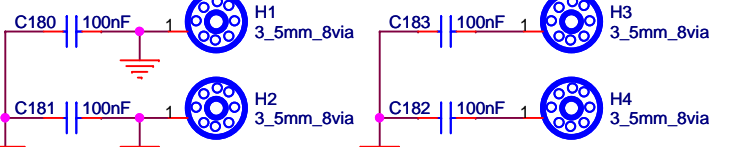
Power ON indicator



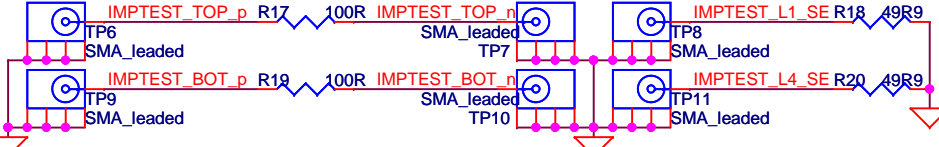
Silkscreen



Mounting holes



Impedance test traces



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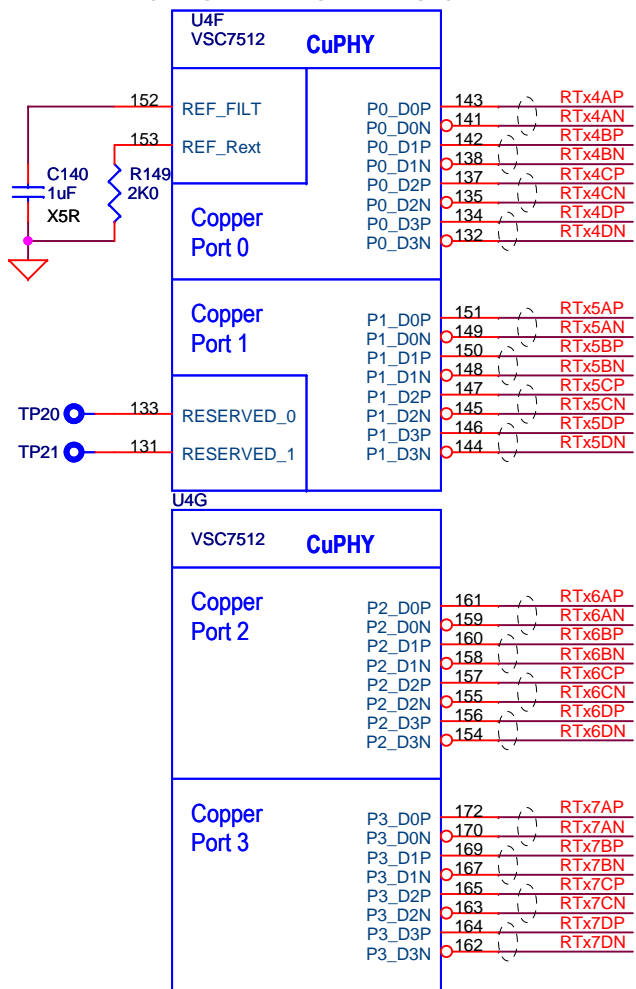
Microsemi

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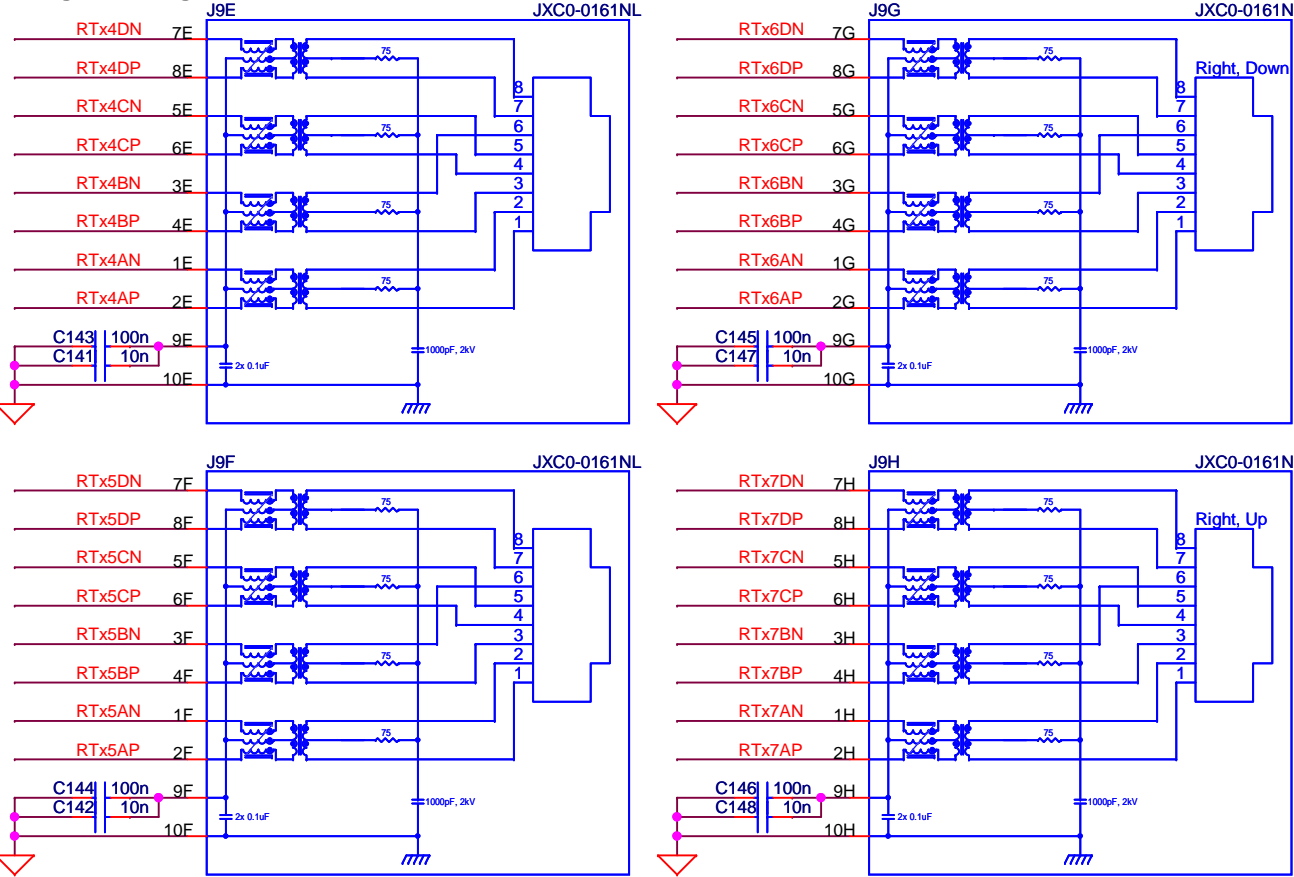
MAG
Title: Power inlet, voltage conversion, VSCxxxx power/decoup, reset

Size: A3	Document Number: PCB121	Rev: 02-00
Date: Thursday, August 11, 2016	Sheet: 2	of: 6

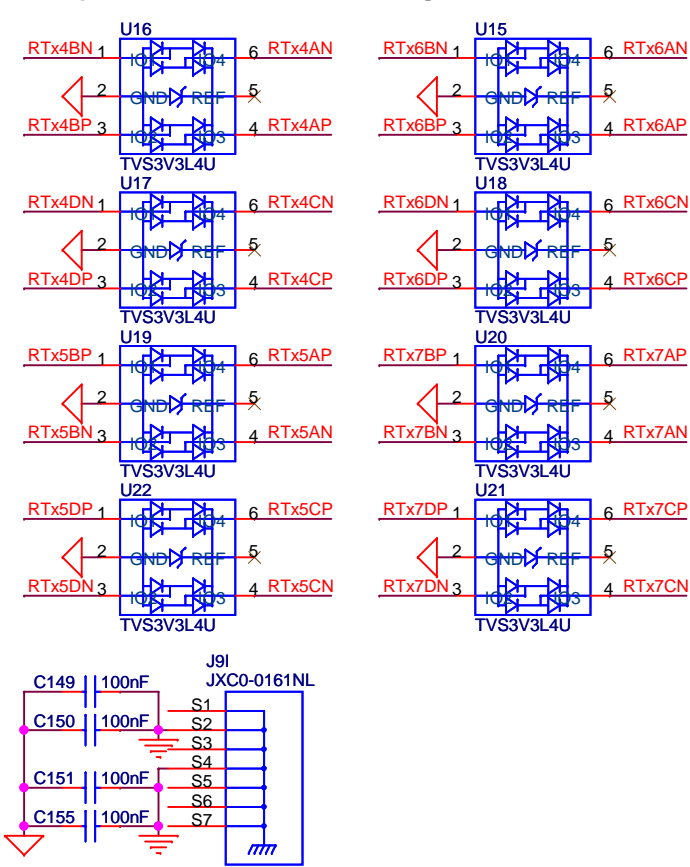
RJ45[8:5] (1Gbps/100Mbps/10Mbps)



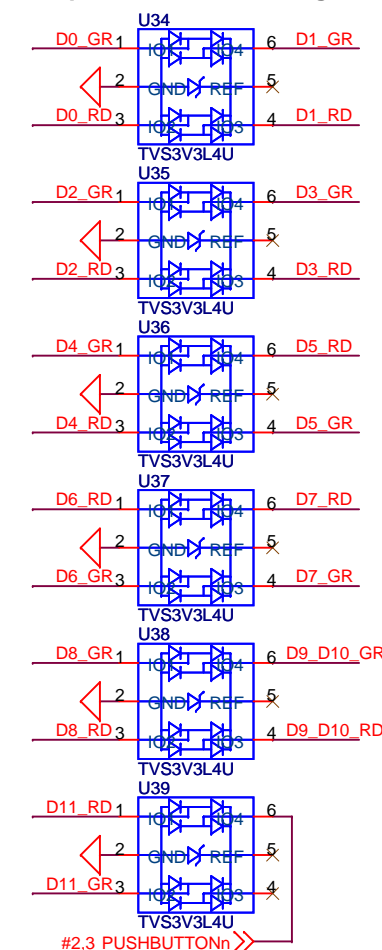
Integrated magnetics



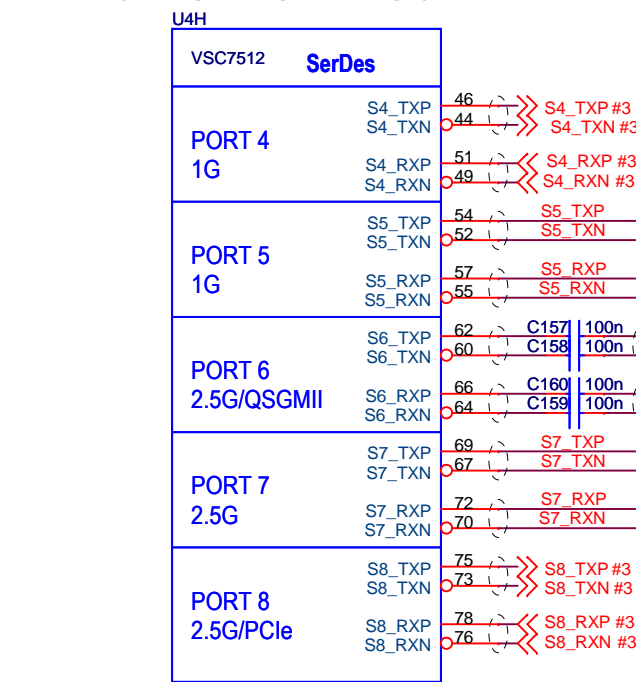
TVS protection on 1000BASE-T signals



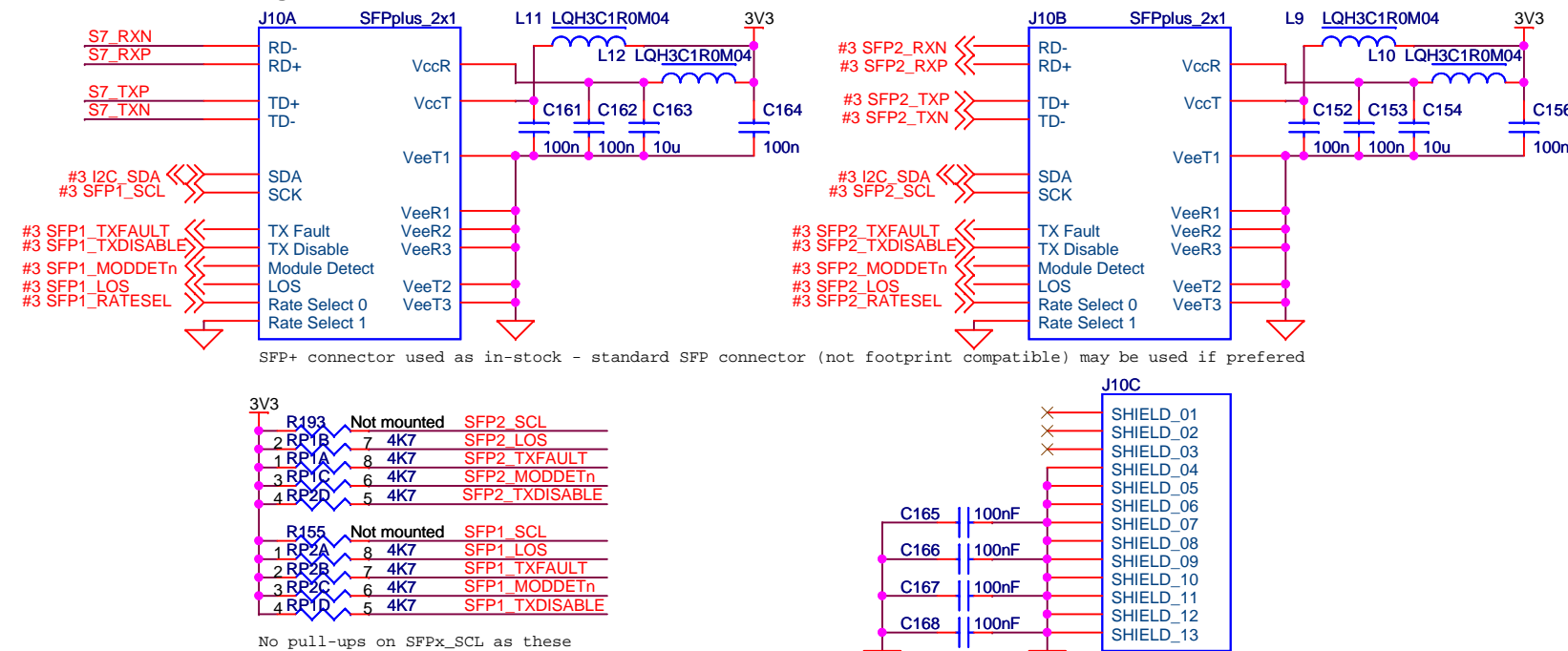
TVS protection on LED signals



SFP[2:1] (2.5Gbps/1Gbps/100Mbps)

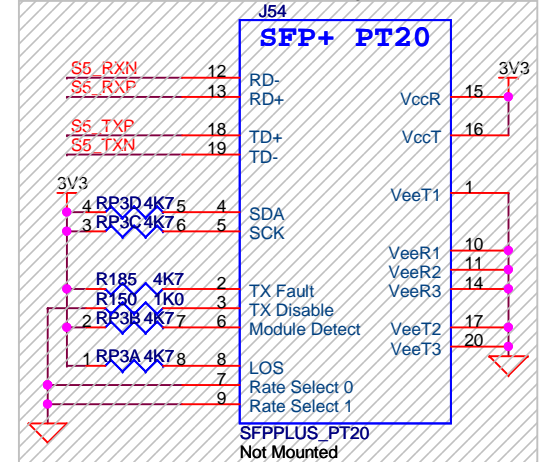


SFP connectors and cage

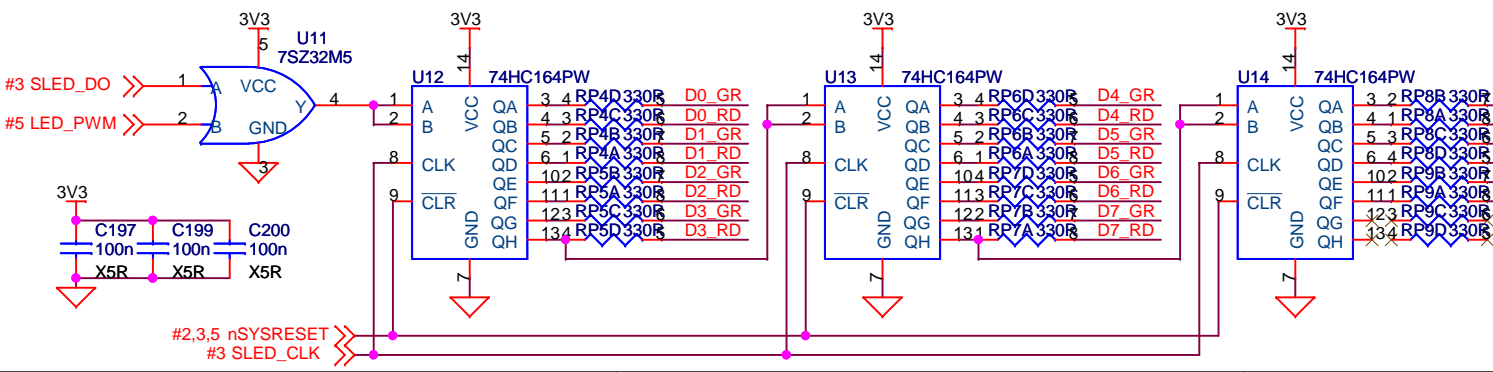


SERDES usage:
 - S5 only used for test
 - S6 connects to VSC8514 through QSGMII
 - S7 (2.5Gbps) connects to SFP1
 - Config 0: S4 (1Gbps) connects to NPI on breakoff and S8 (2.5Gbps) connects to SFP2 through breakoff
 - Config c: S4 (1Gbps) connects to SFP2 through breakoff and S8 (2.5Gbps) connects to PCIe on breakoff board

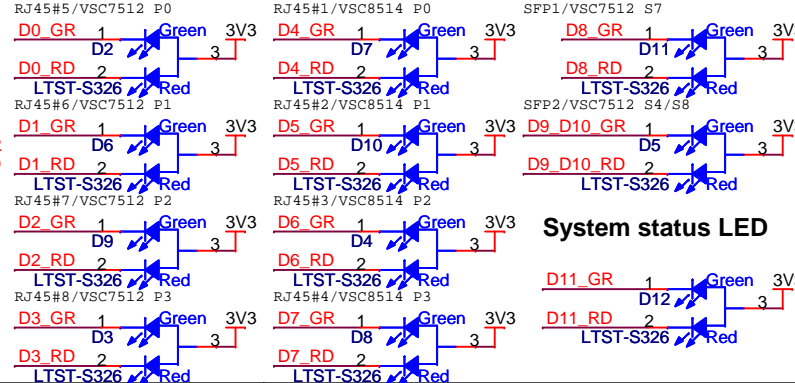
"SFP" connector for test only



Serial LED outputs

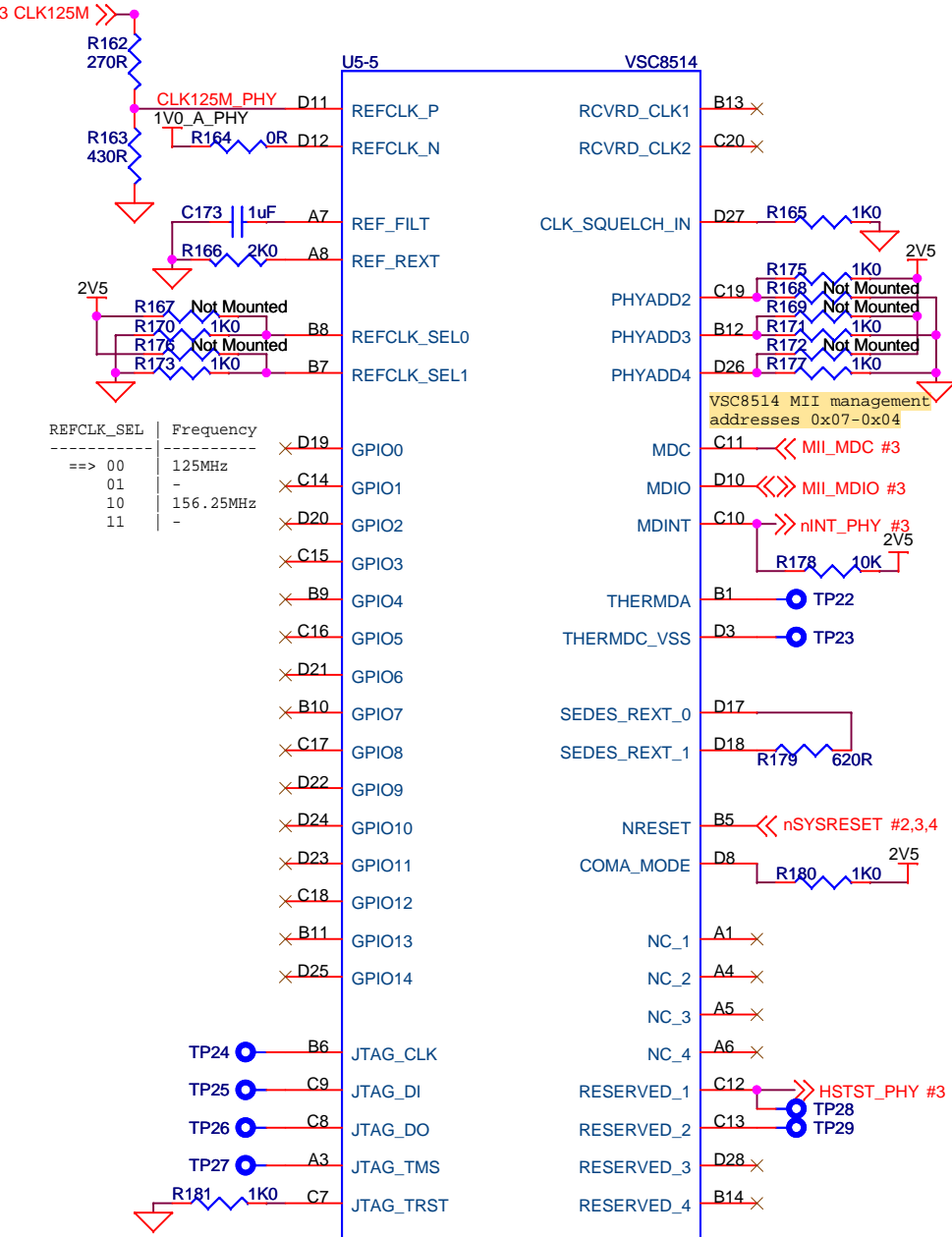


Port status LEDs

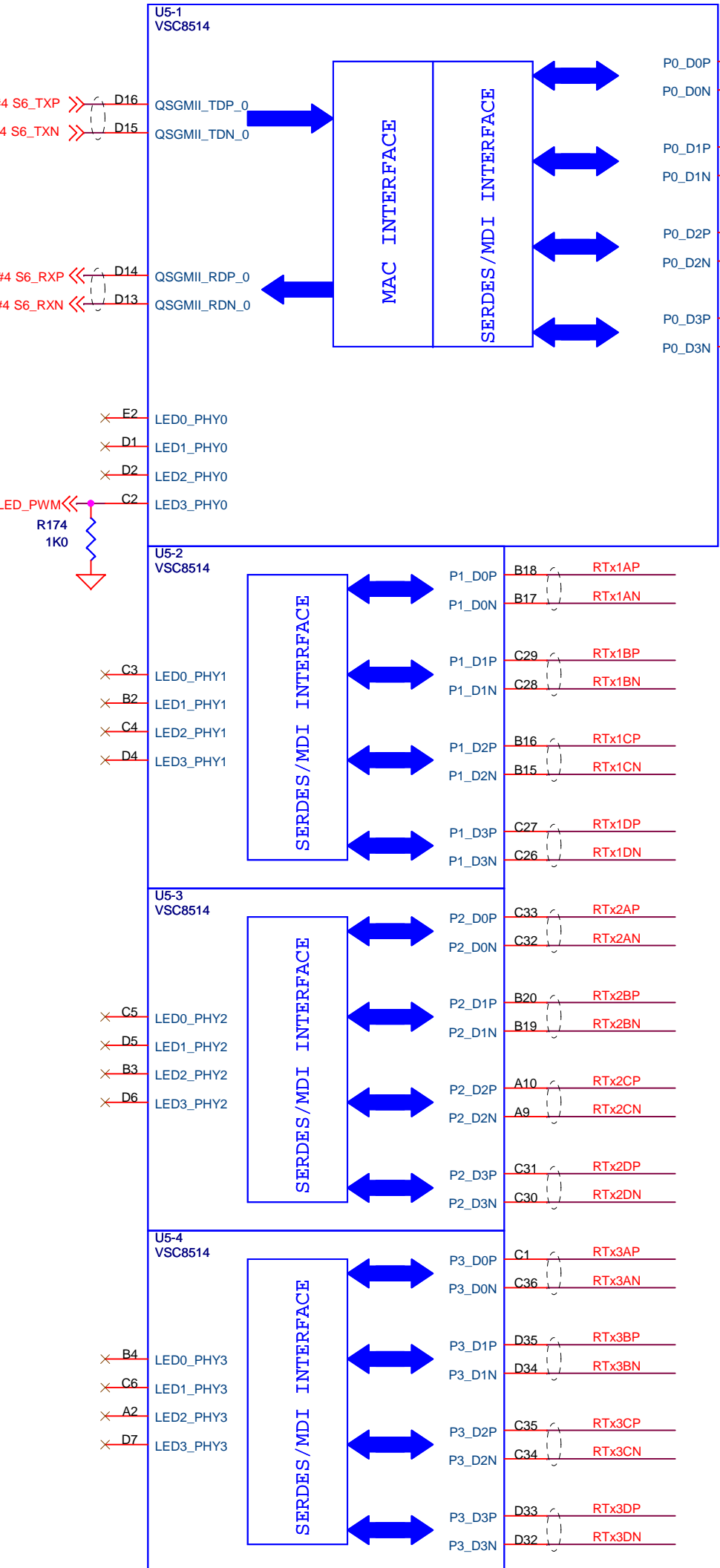


Enable SLED ports 7:0 as port status LEDs for 8x RJ45 ports (SLED port 0 is VSC7512 P0/RJ45#5, SLED port 4 is VSC8514 P0/RJ45#1, etc.).
 SLED port 8 as LED for SFP1 through S7,
 SLED port 9 as LED for 1G SFP2 through S4 (config c/PCIe only),
 SLED port 10 as LED for 2.5G SFP2 through S8 (config 0 only),
 SLED port 11 as system status LED
 Enable two bits per port,
 bit[1:0]=00 => yellow, 01 => red, 10 => green, 11 => off.

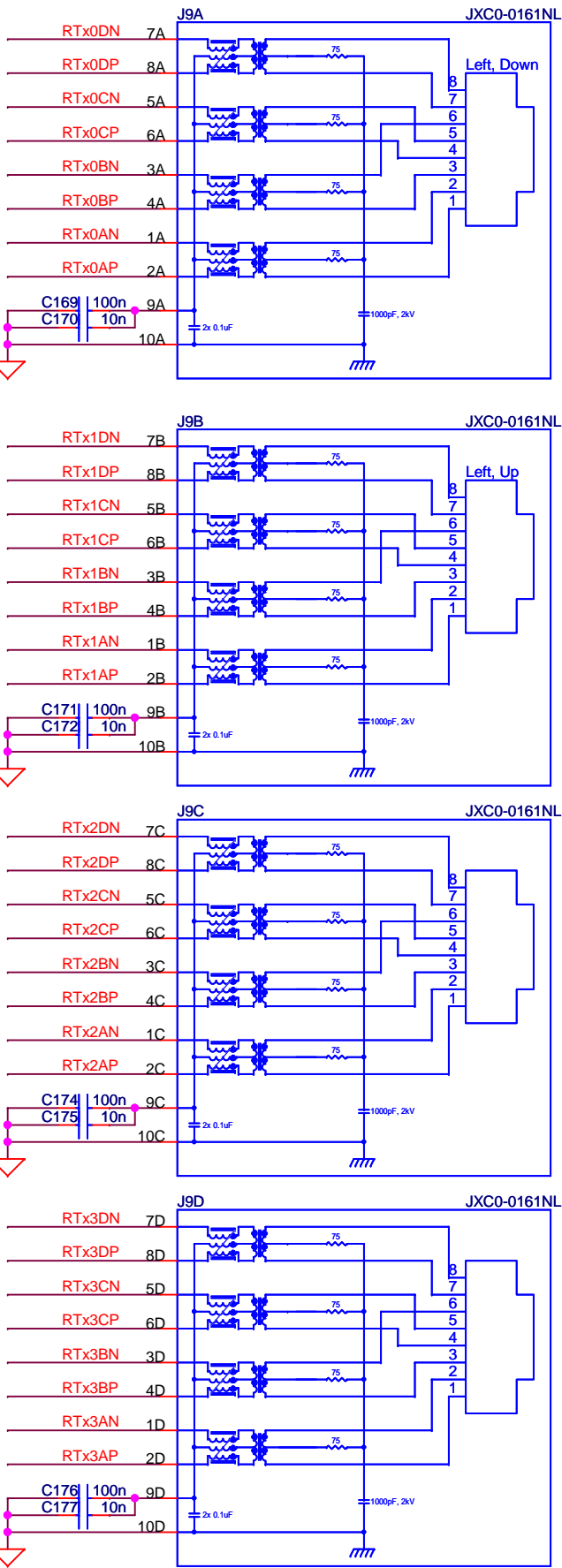
VSC8514 I/O and strapping



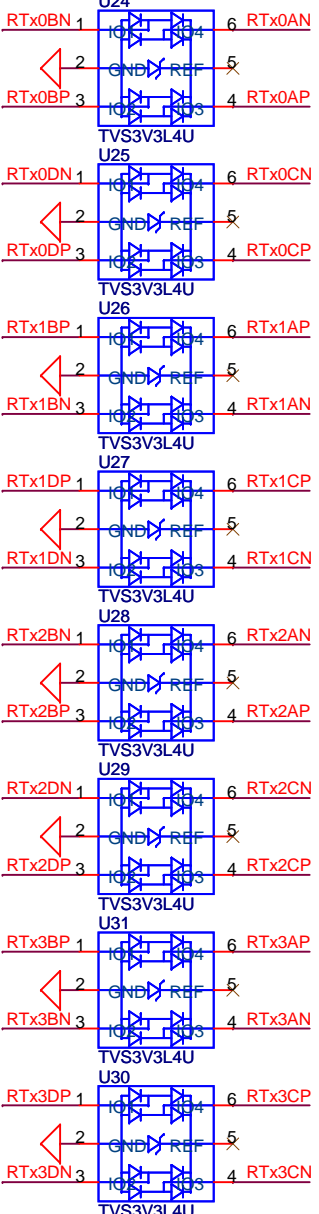
VSC8514 QSGMII/ports



Integrated magnetics

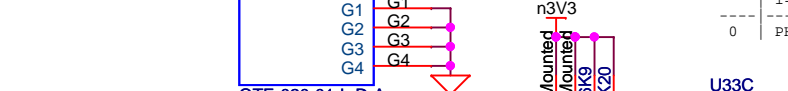
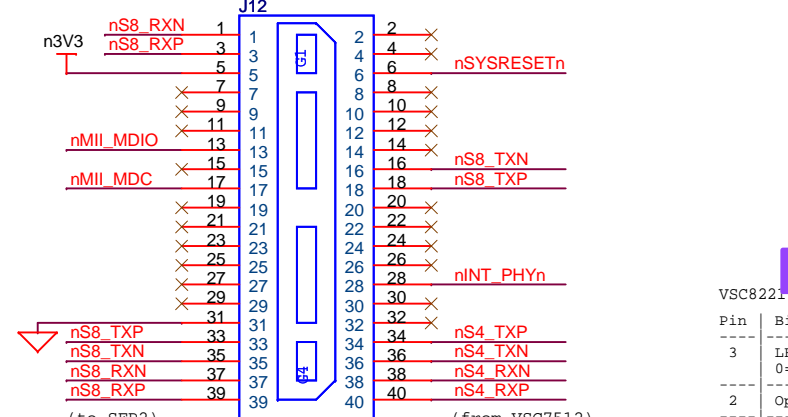


TVS protection

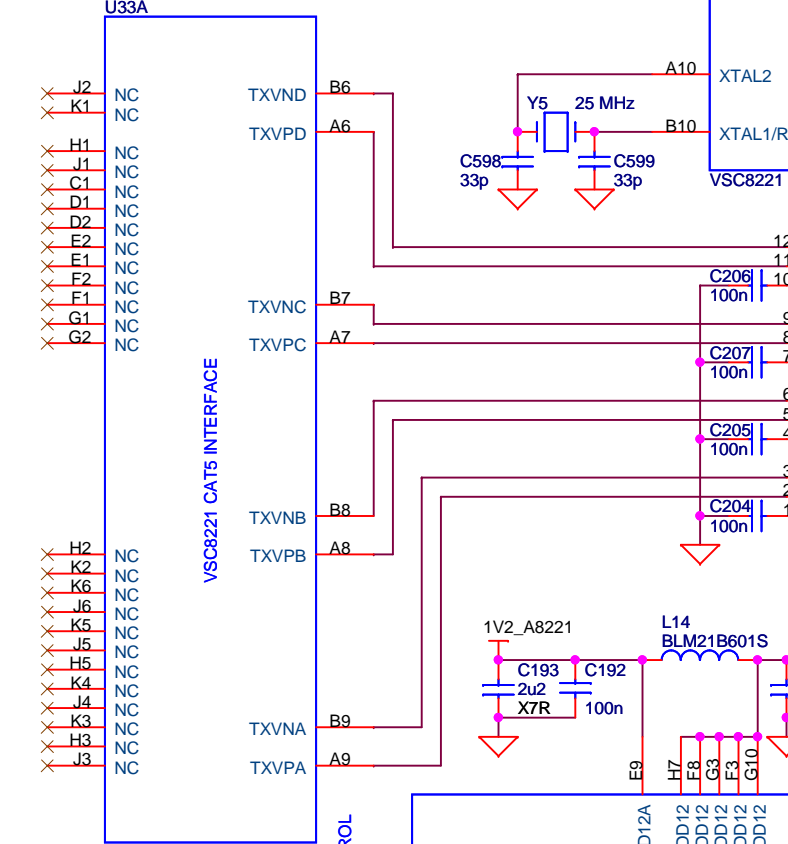
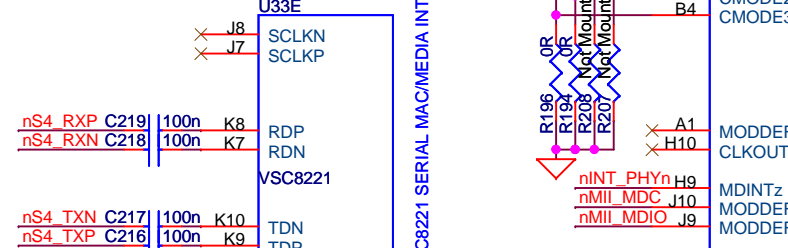


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Samtec connector towards mainboard feedthrough of S8 to SFP2



VSC8221 NPI single PHY

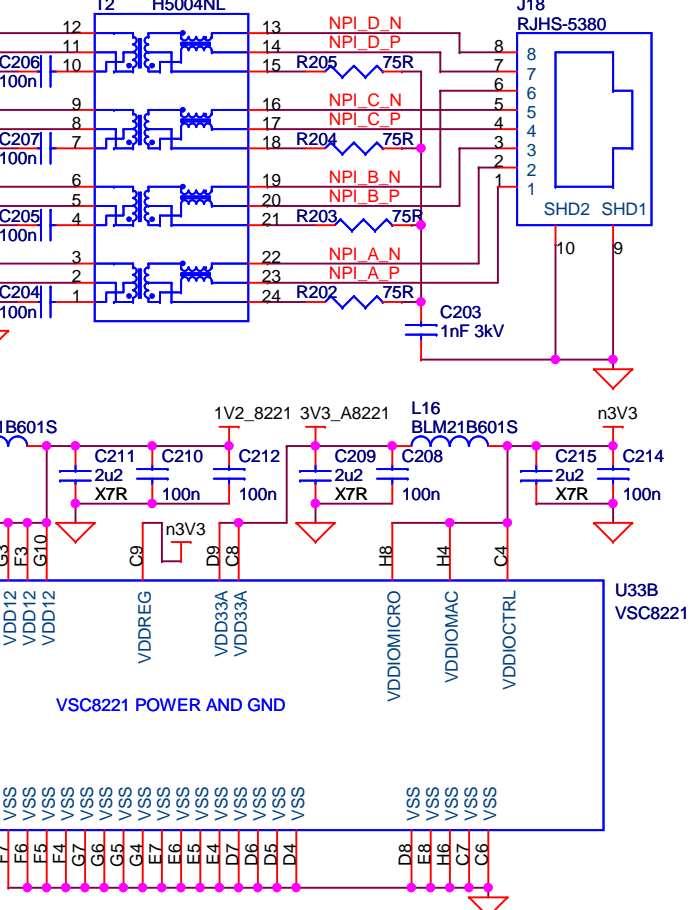
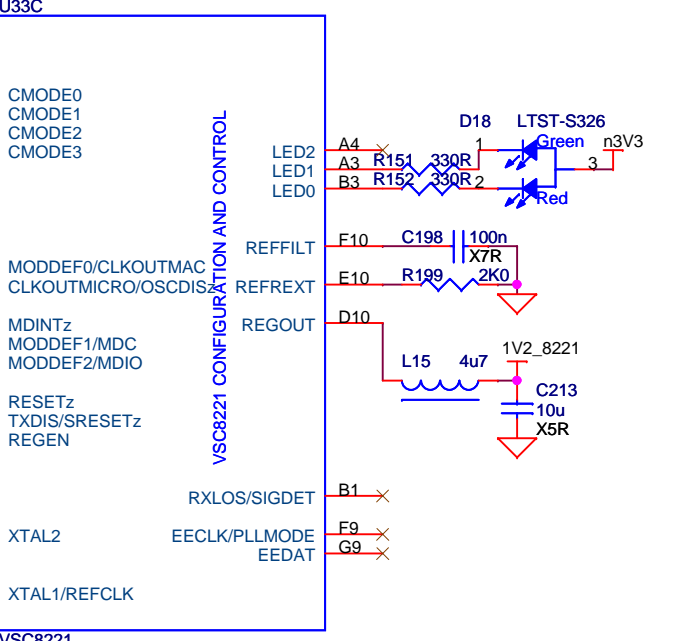
[illegible]

With CMODE	with 1%	Set bit	Set bit	Set bit	Set bit
1	1	1	1	1	1
2	2	2	2	2	2
3	3	3	3	3	3
4	4	4	4	4	4
5	5	5	5	5	5
6	6	6	6	6	6
7	7	7	7	7	7
8	8	8	8	8	8
9	9	9	9	9	9
10	10	10	10	10	10
11	11	11	11	11	11
12	12	12	12	12	12
13	13	13	13	13	13
14	14	14	14	14	14
15	15	15	15	15	15
16	16	16	16	16	16
17	17	17	17	17	17
18	18	18	18	18	18
19	19	19	19	19	19
20	20	20	20	20	20
21	21	21	21	21	21
22	22	22	22	22	22
23	23	23	23	23	23
24	24	24	24	24	24
25	25	25	25	25	25
26	26	26	26	26	26
27	27	27	27	27	27
28	28	28	28	28	28
29	29	29	29	29	29
30	30	30	30	30	30
31	31	31	31	31	31

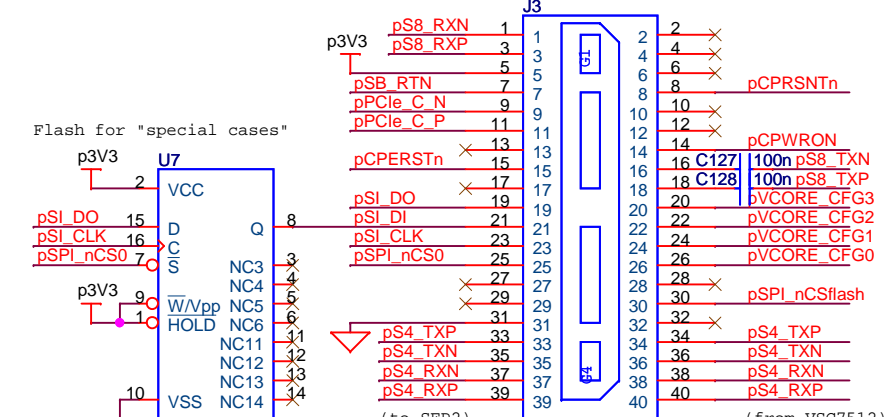
	GND	0	0	0	0	0
	GND	2.26k	0	0	0	1
	GND	4.02k	0	0	1	0
	GND	5.90k	0	0	1	1
	GND	8.25k	0	1	0	0
	GND	12.1k	0	1	0	1
	GND	16.9k	0	1	1	0
	GND	22.6k	0	1	1	1
	3V3	0	1	0	0	0
	3V3	2.26k	1	0	0	1
	3V3	4.02k	1	0	1	0
	3V3	5.90k	1	0	1	1
	3V3	8.25k	1	1	0	0
	3V3	12.1k	1	1	0	1
	3V3	16.9k	1	1	1	0

UCD0222 DE straining

Pin	Bit 3 control	Bit 2 control	Bit 1 control	Bit 0 (LSB) control
3	LED control[1] 0>=link/act	SQE enable 0>=SQE disabled	Reserved -	Autoneg ctrl[1] 0>=10/100/1000Base
2	Operating mode[3:0], 0000=>SERDES to CAT5, SCLK			disabled
1	SFP mode 1=>SFP disable	PHY address[4] 1	SIGDET direct 1=>Output	Line impedance 0=>50R

[illegible]

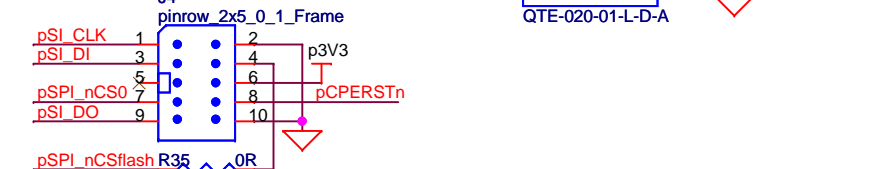
Samtec connector towards mainboard feedthrough of S4 to SFP2



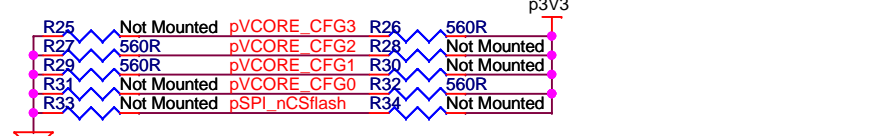
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Programming header for Flash

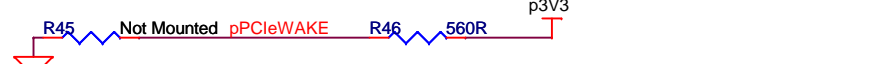
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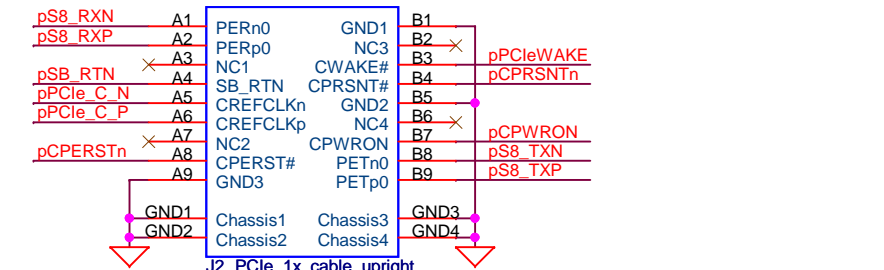
Override VCORE_CFG of mainboard, for plug&play PCIe



No PCIeWAKE from this mainboard (use in-band beacon instead)



PCIe 1x cable connector for S8 from mainboard



Note, PCIe interface for use in controlled lab environment, so

- (1) no power domain isolation,
- (2) high-impedance when powered off not guaranteed for CWAKE#, CPRSNT#, CPERST#,
- (3) spread spectrum clocked PCIe hosts not supported

