Register File for VSC7514

INTRODUCTION

This document provides information about the programming interface, register maps, register descriptions, and register tables of the device.

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1.0 REGISTERS

In writing to registers with reserved bits, use a read-modify-write technique, where the entire register is read, but with only the user bits to be chance are modified. Do not change the values of the register and bits marked as reserved. Their read state should not be considered static or unchanging. Unspecified registers and bits must be written to 0 and can be ignored when read.

The first-level table lists all register targets and associated base addresses. The second level table lists registers groups and offsets within targets, and the third-level tables list registers within the register groups.

Both register groups and registers may be replicated (repeated) a number of times. The repeat-count and the distance between two repetitions are listed in the Instances and Address Spacing column. Spacing is omitted if there is only one instance. The Offset within Target and the Offset within Register Group columns hold the offset of the first instance of the register group or register.

Use the following steps to calculate the absolute address of a given register.

1. Multiply the register group's replication number by the register group's address spacing.
2. Add the result to the register group's offset within the target.
3. Multiply the register's replication number with the register's address spacing.
4. Add the result to the register's offset within the register group.
5. Add these two numbers to the absolute address of the target in question.

TABLE 1-1: LIST OF TARGETS AND BASE ADDRESSES

Target Name	Base Address	Description	Details
ANA	0x71880000	Analyzer Configuration	Page 6
DEV[0]	0x711E0000	Port Configuration	Page 41
DEV[1]	0x711F0000	Port Configuration	Page 41
DEV[2]	0x71200000	Port Configuration	Page 41
DEV[3]	0x71210000	Port Configuration	Page 41
DEV[4]	0x71220000	Port Configuration	Page 41
DEV[5]	0x71230000	Port Configuration	Page 41
DEV[6]	0x71240000	Port Configuration	Page 41
DEV[7]	0x71250000	Port Configuration	Page 41
DEV[8]	0x71260000	Port Configuration	Page 41
DEV[9]	0x71270000	Port Configuration	Page 41
DEV[10]	0x71280000	Port Configuration	Page 41
DEVCPU_GCB	0x71070000	General configuration block.	Page 60
DEVCPU_ORG	0x71000000	CPU Device Origin	Page 87
DEVCPU_PTP	0x710E0000	DEVCPU Precision Timing Protocol Originator	Page 94
DEVCPU_QS	0x71080000	CPU Device Queue System	Page 101
ES0	0x71040000	Versatile Content Aware Processor	Page 186
HSIO	0x710D0000	Macro Control Register Collection	Page 107
ICPU_CFG	0x70000000	AMBA Top Level Settings	Page 139
S1	0x71050000	Versatile Content Aware Processor	Page 186
S2	0x71060000	Versatile Content Aware Processor	Page 186
PCIE_EP	0x70111000	PCIe Endpoint Configuration Space	Page 193
QSYS	0x71800000	Queue System Configuration	Page 212
REW	0x71030000	Rewriter Configuration	Page 228
SBA	0x70110000	Shared Bus Arbiter	Page 232
SIMC	0x70101000	SI Master Controller	Page 235
SYS	0x71010000	Switching Engine Configuration	Page 242

TABLE 1-1: LIST OF TARGETS AND BASE ADDRESSES (CONTINUED)

Target Name	Base Address	Description	Details
TWI	0x70100400	Two-Wire Interface Controller	Page 252
UART	0x70100000	UART Controller	Page 270
UART2	0x70100800	UART Controller	Page 270
PHY	0x71000000	PHY Configuration	Page 278

1.1 ANA

TABLE 1-2: REGISTER GROUPS IN ANA

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
ANA	0x00009000	1	Common analyzer registers	Page 6
PGID	0x00008C00	1	Port Group Identifier table	Page 15
ANA_TABLES	0x00008B00	1	Analyzer tables	Page 16
PORT	0x00007000	12 0x00000100	Classifier configuration per port	Page 21
PFC	0x00008800	11 0x00000040	Priority-based flow control configuration	Page 32
COMMON	0x000090B4	1	Common configurations for classifier	Page 33
POL	0x00004000	384 0x00000020	Policer configuration	Page 38
POL_MISC	0x00008B80	1	Policer flow control configuration	Page 40

1.1.1 ANA:ANA

Parent: ANA

Instances: 1

TABLE 1-3: REGISTERS IN ANA

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
ADVLEARN	0x00000000	1	Advanced learning setup	Page 7
VLANMASK	0x00000004	1	VLAN source port mask	Page 7
ANAGEFIL	0x0000000C	1	Aging filter	Page 7
ANEVENTS	0x00000010	1	Event sticky bits	Page 8
STORMLIMIT_BURST	0x00000014	1	Storm policer burst	Page 9
STORMLIMIT_CFG	0x00000018	4 0x00000004	Storm policer configuration per storm policer	Page 9
ISOLATED_PORTS	0x00000028	1	Private VLAN mask for isolated ports	Page 10
COMMUNITY_PORTS	0x0000002C	1	Private VLAN mask for community ports	Page 10
AUTOAGE	0x00000030	1	Auto-age timer	Page 11
MACTOPTIONS	0x00000034	1	MAC table options	Page 11

TABLE 1-3: REGISTERS IN ANA (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
LEARNDISC	0x00000038	1	Learn discard counter	Page 12
AGENCTRL	0x0000003C	1	Analyzer configuration	Page 12
MIRRORPORTS	0x00000040	1	Mirror target ports	Page 13
EMIRRORPORTS	0x00000044	1	Egress mirror mask	Page 13
FLOODING	0x00000048	1	Standard flooding configuration	Page 13
FLOODING_IPMC	0x0000004C	1	Flooding configuration for IP multicasts	Page 14
SFLOW_CFG	0x00000050	12 0x00000004	sFlow sampling configuration per switch port	Page 14
PORT_MODE	0x00000080	13 0x00000004	Port configuration per device port	Page 14

1.1.1.1 ANA:ANA:ADVLEARN

Parent: ANA:ANA

Instances: 1

TABLE 1-4: FIELDS IN ADVLEARN

Field Name	Bit	Access	Description	Default
VLAN_CHK	11	R/W	If this bit is set, a frame discarded because of VLAN ingress filtering is not subject to learning. VLAN ingress filtering is controlled by the VLAN_SRC_CHK flag in the VLAN table (see VLANACCESS register) or the VLANMASK register.	0x0
LEARN_MIRROR	10:0	R/W	Learn frames are also forwarded to ports marked in this mask.	0x000

1.1.1.2 ANA:ANA:VLANMASK

Parent: ANA:ANA

Instances: 1

TABLE 1-5: FIELDS IN VLANMASK

Field Name	Bit	Access	Description	Default
VLANMASK	11:0	R/W	Mask for requiring VLAN ingress filtering. If the bit for the frame's physical ingress port is set in this mask, then the port must be member of ingress frame's VLAN (VLANACCESS.VLAN_PORT_MASK), otherwise the frame is discarded.	0x000

1.1.1.3 ANA:ANA:ANAGEFIL

Parent: ANA:ANA

Instances: 1

This register sets up which entries are touched by an aging operation (manual as well as automatic aging).

In this way, it is possible to have different aging periods in each VLAN and to have quick removal of entries on specific ports.

The register also affects the GET_NEXT MAC table command. When using the register to control the behavior of GET_NEXT, it is recommended to disable automatic aging while executing the GET_NEXT command.

TABLE 1-6: FIELDS IN ANAGEFIL

Field Name	Bit	Access	Description	Default
AGE_LOCKED	20	R/W	Select entries to age. If cleared, unlocked entries are aged and potentially removed. If set, locked entries are aged but not removed.	0x0
PID_EN	19	R/W	If set, only MAC table entries with a destination index matching PID_VAL are aged or searched with GET_NEXT.	0x0
PID_VAL	18:14	R/W	Destination index used in selective aging or MAC table searching.	0x00
VID_EN	13	R/W	If set, only MAC table entries with a VID matching VID_VAL are aged or searched with GET_NEXT.	0x0
VID_VAL	12:0	R/W	VID used in selective aging or MAC table searching.	0x0000

1.1.1.4 ANA:ANA:ANEVENTS

Parent: ANA:ANA

Instances: 1

TABLE 1-7: FIELDS IN ANEVENTS

Field Name	Bit	Access	Description	Default
MSTI_DROP	27	Sticky	A frame was discarded due to blocking MSTI.	0x0
AUTOAGE	24	Sticky	An AUTOAGE run was performed.	0x0
STORM_DROP	22	Sticky	A frame was discarded, because it exceeded the flooding storm limitations configured in STORMLIMIT.	0x0
LEARN_DROP	21	Sticky	A frame was discarded, because it was subject to learning, and the DropMode flag was set in ADVLEARN.	0x0
AGED_ENTRY	20	Sticky	An entry was removed at CPU Learn, or CPU requested an aging process.	0x0
CPU_LEARN_FAILED	19	Sticky	A learn operation failed due to hash table depletion. CPU-based learning only.	0x0
AUTO_LEARN_FAILED	18	Sticky	A learn operation of incoming source MAC address failed due to hash table depletion. Hardware-based learning only.	0x0
LEARN_REMOVE	17	Sticky	An entry was removed when learning a new source MAC address.	0x0
AUTO_LEARNED	16	Sticky	An entry was learned from an incoming frame. Hardware-based learning only.	0x0
AUTO_MOVED	15	Sticky	A station was moved to another port.	0x0

TABLE 1-7: FIELDS IN ANEVENTS (CONTINUED)

Field Name	Bit	Access	Description	Default
CLASSIFIED_DROP	13	Sticky	A frame was not forwarded due to classification (such as BPDUs).	0x0
CLASSIFIED_COPY	12	Sticky	A frame was copied to the CPU due to classification.	0x0
VLAN_DISCARD	11	Sticky	A frame was discarded due to lack of VLAN membership on source port.	0x0
FWD_DISCARD	10	Sticky	A frame was discarded due to missing forwarding state on source port.	0x0
MULTICAST_FLOOD	9	Sticky	A frame was flooded with multicast flooding mask.	0x0
UNICAST_FLOOD	8	Sticky	A frame was flooded with unicast flooding mask.	0x0
DEST_KNOWN	7	Sticky	A frame was forwarded with known destination MAC address.	0x0
BUCKET3_MATCH	6	Sticky	A destination was found in hash table bucket 3.	0x0
BUCKET2_MATCH	5	Sticky	A destination was found in hash table bucket 2.	0x0
BUCKET1_MATCH	4	Sticky	A destination was found in hash table bucket 1.	0x0
BUCKET0_MATCH	3	Sticky	A destination was found in hash table bucket 0.	0x0
CPU_OPERATION	2	Sticky	A CPU-initiated operation on the MAC or VLAN table was processed. Default is 1 due to auto-initialization of the MAC and VLAN table.	0x1
DMAC_LOOKUP	1	Sticky	A destination address was looked up in the MAC table.	0x0
SMAC_LOOKUP	0	Sticky	A source address was looked up in the MAC table.	0x0

1.1.1.5 ANA:ANA:STORMLIMIT_BURST

Parent: ANA:ANA

Instances: 1

TABLE 1-8: FIELDS IN STORMLIMIT_BURST

Field Name	Bit	Access	Description	Default
STORM_BURST	3:0	R/W	Allowed number of frames in a burst is 2**STORM_BURST. The maximum allowed burst is 4096 frames, which corresponds to STORM_BURST = 12. The STORM_BURST is common for all storm policers.	0x0

1.1.1.6 ANA:ANA:STORMLIMIT_CFG

Parent: ANA:ANA

Instances: 4

0: UC storm policer

1: BC storm policer

2: MC policer

3: Learn policer

TABLE 1-9: FIELDS IN STORMLIMIT_CFG

Field Name	Bit	Access	Description	Default
STORM_RATE	6:3	R/W	Allowed rate of storm policer is 2**STORM_UNIT frames/sec or kiloframes/sec (see STORM_UNIT). The maximum allowed rate is 1024 kiloframes/sec, which corresponds to STORM_RATE = 10 with STORM_UNIT set to 0.	0x0
STORM_UNIT	2	R/W	If set, the base unit for the storm policer is 1 frame per second. If cleared, the base unit is 1 kiloframes per second.	0x0
STORM_MODE	1:0	R/W	Mode of operation for storm policer. 0: Disabled 1: Police CPU destination only. 2: Police front port destinations only. 3: Police both CPU and front port destinations.	0x0

1.1.1.7 ANA:ANA:ISOLATED_PORTS

Parent: ANA:ANA

Instances: 1

TABLE 1-10: FIELDS IN ISOLATED_PORTS

Field Name	Bit	Access	Description	Default
ISOL_PORTS	11:0	R/W	This mask is used in private VLANs applications. Promiscuous and community ports must be set and isolated ports must be cleared. For frames classified to a private VLAN (see the VLAN_PRIV_VLAN field in VLAN table), the resulting VLAN mask is calculated as follows: - Frames received on a promiscuous port use the VLAN mask directly. - Frames received on a community port use the VLAN mask AND'ed with the ISOL_PORTS. - Frames received on a isolated port use the VLAN mask AND'ed with the COMM_PORTS AND'ed with the ISOL_PORTS. For frames classified to a non-private VLAN, this mask is not used.	0xFFF

1.1.1.8 ANA:ANA:COMMUNITY_PORTS

Parent: ANA:ANA

Instances: 1

TABLE 1-11: FIELDS IN COMMUNITY_PORTS

Field Name	Bit	Access	Description	Default
COMM_PORTS	11:0	R/W	This mask is used in private VLANs applications. Promiscuous and isolated ports must be set and community ports must be cleared. See ISOLATED_PORTS.ISOL_PORTS for details.	0xFFF

1.1.1.9 ANA:ANA:AUTOAGE

Parent: ANA:ANA

Instances: 1

TABLE 1-12: FIELDS IN AUTOAGE

Field Name	Bit	Access	Description	Default
AGE_FAST	21	R/W	Sets the unit of AGE_PERIOD to 13.1 us. AGE_PERIOD must be a minimum of 3 when using the FAST option.	0x0
AGE_PERIOD	20:1	R/W	Time in seconds between automatic aging of a MAC table entry. Setting AGE_PERIOD to zero effectively disables automatic aging. An inactive unlocked MAC table entry is aged after 2*AGE_PERIOD.	0x00000
AUTOAGE_LOCKED	0	R/W	Enable setting of the AGED_FLAG for locked entries in the MAC table when doing an age scan. Locked entries are never removed but the AGED_FLAG can be used to indicate activity for the MAC address.	0x0

1.1.1.10 ANA:ANA:MACTOPTIONS

Parent: ANA:ANA

Instances: 1

TABLE 1-13: FIELDS IN MACTOPTIONS

Field Name	Bit	Access	Description	Default
REDUCED_TABLE	1	R/W	When set, the MAC table is reduced to 256 entries (64 rows of 4 entries).	0x0
SHADOW	0	R/W	Enable MAC table shadow registers. The SHADOW bit affects the behavior of the READ command in MACACCESS.MAC_TABLE_CMD: With the shadow bit set, reading bucket 0 causes the remaining 3 buckets in the row to be stored in "shadow registers". Following read accesses to bucket 1-3 return the content of the shadow registers. This is useful when reading a MAC table, which can change while being read.	0x0

1.1.1.11 ANA:ANA:LEARNDISC

Parent: ANA:ANA

Instances: 1

The total number of MAC table entries that have been or would have been learned, but have been discarded due to a lack of storage space.

TABLE 1-14: FIELDS IN LEARNDISC

Field Name	Bit	Access	Description	Default
LEARNDISC	31:0	R/W	Number of discarded learn requests due to MAC table overflow (collisions or MAC table entry limits).	0x00000000

1.1.1.12 ANA:ANA:AGENCTRL

Parent: ANA:ANA

Instances: 1

TABLE 1-15: FIELDS IN AGENCTRL

Field Name	Bit	Access	Description	Default
FID_MASK	23:12	R/W	Mask used to enable shared learning among multiple VLANs. The FID value used in learning and MAC table lookup is calculated as: FID = VID and (not FID_MASK) By default, FID_MASK is set to all-zeros, corresponding to independent VLAN learning. In this case FID becomes identical to VID.	0x000
IGNORE_DMAC_FLAGS	11	R/W	Do not react to flags found in the DMAC entry or the corresponding flags for flooded frames (FLOOD_IGNORE_VLAN).	0x0
IGNORE_SMAC_FLAGS	10	R/W	Do not react to flags found in the SMAC entry. Note, the IGNORE_VLAN flag is not checked for SMAC entries.	0x0
FLOOD_SPECIAL	9	R/W	Flood frames using the lowest 12 bits of DMAC as destination port mask. This is only added for testing purposes.	0x0
FLOOD_IGNORE_VLAN	8	R/W	VLAN mask is not applied to flooded frames.	0x0
MIRROR_CPU	7	R/W	Frames destined for the CPU extraction queues are also forwarded to the port set configured in MIRRORPORTS.	0x0
LEARN_CPU_COPY	6	R/W	If set, auto-learned stations get the CPU_-COPY flag set in the MAC table entry.	0x0
LEARN_SRC_KILL	5	R/W	If set, auto-learned stations get the SRC_KILL flag set in the MAC table entry.	0x0
LEARN_IGNORE_VLAN	4	R/W	If set, auto-learned stations get the IGNORE_VLAN flag set in the MAC table entry.	0x0
CPU_CPU_KILL_ENA	3	R/W	If set, CPU injected frames are never sent back to the CPU.	0x1

TABLE 1-15: FIELDS IN AGENCTRL (CONTINUED)

Field Name	Bit	Access	Description	Default
GREEN_COUNT_MODE	2	R/W	Counter mode for the Rx priority counters for green frames (C_RX_GREEN_PRIO_x) 0: Count octets 1: Count frames	0x1
YELLOW_COUNT_MODE	1	R/W	Counter mode for the Rx priority counters for yellow frames (C_RX_YELLOW_PRIO_x) 0: Count octets 1: Count frames	0x1
RED_COUNT_MODE	0	R/W	Counter mode for the Rx priority counters for red frames (C_RX_RED_PRIO_x) 0: Count octets 1: Count frames	0x1

1.1.1.13 ANA:ANA:MIRRORPORTS

Parent: ANA:ANA

Instances: 1

TABLE 1-16: FIELDS IN MIRRORPORTS

Field Name	Bit	Access	Description	Default
MIRRORPORTS	11:0	R/W	Ports set in this mask receive a mirror copy. If CPU is included in mask (most significant bit set), then the frame is copied to CPU extraction queue CPUQ_CFG.CPUQ_MIRROR.	0x000

1.1.1.14 ANA:ANA:EMIRRORPORTS

Parent: ANA:ANA

Instances: 1

TABLE 1-17: FIELDS IN EMIRRORPORTS

Field Name	Bit	Access	Description	Default
EMIRRORPORTS	11:0	R/W	Frames forwarded to ports in this mask are mirrored to the port set configured in MIRRORPORTS (i.e. egress port mirroring).	0x000

1.1.1.15 ANA:ANA:FLOODING

Parent: ANA:ANA

Instances: 1

TABLE 1-18: FIELDS IN FLOODING

Field Name	Bit	Access	Description	Default
FLD_UNICAST	17:12	R/W	Set the PGID mask to use when flooding unknown unicast frames.	0x3F
FLD_BROADCAST	11:6	R/W	Set the PGID mask to use when flooding unknown broadcast frames.	0x3F

TABLE 1-18: FIELDS IN FLOODING (CONTINUED)

Field Name	Bit	Access	Description	Default
FLD_MULTICAST	5:0	R/W	Set the PGID mask to use when flooding unknown multicast frames (except IP multicasts).	0x3F

1.1.1.16 ANA:ANA:FLOODING_IPMC

Parent: ANA:ANA

Instances: 1

TABLE 1-19: FIELDS IN FLOODING_IPMC

Field Name	Bit	Access	Description	Default
FLD_MC4_CTRL	23:18	R/W	Set the PGID mask to use when flooding unknown IPv4 Multicast Control frames.	0x3F
FLD_MC4_DATA	17:12	R/W	Set the PGID mask to use when flooding unknown IPv4 Multicast Data frames.	0x3F
FLD_MC6_CTRL	11:6	R/W	Set the PGID mask to use when flooding unknown IPv6 Multicast Control frames.	0x3F
FLD_MC6_DATA	5:0	R/W	Set the PGID mask to use when flooding unknown IPv6 Multicast Data frames.	0x3F

1.1.1.17 ANA:ANA:SFLOW_CFG

Parent: ANA:ANA

Instances: 12

TABLE 1-20: FIELDS IN SFLOW_CFG

Field Name	Bit	Access	Description	Default
SF_RATE	13:2	R/W	Probability of a frame being SFLOW sampled. Unit is 1/4096. A value of 0 makes 1/4096 of the candidates being forwarded to the SFLOW CPU extraction queue. A values of 4095 makes all candidates being forwarded.	0x000
SF_SAMPLE_RX	1	R/W	Enable SFLOW sampling of frames received on this port.	0x0
SF_SAMPLE_TX	0	R/W	Enable SFLOW sampling of frames transmitted on this port.	0x0

1.1.1.18 ANA:ANA:PORT_MODE

Parent: ANA:ANA

Instances: 13

These configurations exists per front port and for two CPU ports.

TABLE 1-21: FIELDS IN PORT_MODE

Field Name	Bit	Access	Description	Default
RESERVED	2:1	R/W	Must be set to its default.	0x2

TABLE 1-21: FIELDS IN PORT_MODE (CONTINUED)

Field Name	Bit	Access	Description	Default
L3_PARSE_CFG	0	R/W	Enable frame analysis on Layer-3 and Layer-4 protocol information. If cleared, all frames are seen as non-IP and are handled accordingly. This affects all blocks using IP information such as classification, TCAM lookups, IP flooding and forwarding, and DSCP rewriting.	0x1

1.1.2 ANA:PGID

Parent: ANA

Instances: 1

TABLE 1-22: REGISTERS IN PGID

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PGID	0x00000000	92 0x00000004	Port Group Identifiers	Page 15

1.1.2.1 ANA:PGID:PGID

Parent: ANA:PGID

Instances: 92

Three port masks are applied to all frames, allowing transmission to a port if the corresponding bit is set in all masks.

0-63: A mask is applied based on destination analysis

64-79: A mask is applied based on aggregation analysis

80-90: A mask is applied based on source port analysis

Destination analysis:

There are 64 destination masks in total. By default, the first 11 port masks only have the bit corresponding to their port number set. These masks should not be changed, except for aggregation.

The remaining destination masks are set to 0 by default and are available for use for Layer-2 multicasts and flooding (See FLOODING and FLOODING_IPMC).

Aggregation analysis:

The aggregation port masks are used to select only one port within each aggregation group. These 16 masks must be setup to select only one port in each aggregated port group.

For ports, which are not part of any aggregation group, the corresponding bits in all 16 masks must be set.

I.e. if no aggregation is configured, all masks must be set to all-ones.

The aggregation mask used for the forwarding of a given frame is selected by the frame's aggregation code (see AGGRCTRL).

Source port analysis:

The source port masks are used to prevent frames from being looped back to the ports on which they were received, and must be updated according to the

aggregation configuration. A frame that is received on port n, uses mask 80+n as a mask to filter out destination ports to avoid loopback, or to facilitate port grouping (port-based VLANs). The default values are that all bits are set except for the index number.

TABLE 1-23: FIELDS IN PGID

Field Name	Bit	Access	Description	Default
CPUQ_DST_PGID	29:27	R/W	CPU extraction queue used when CPU port is enabled in PGID. Only applicable for the destination analysis.	0x0
PGID	11:0	R/W	When a mask is chosen, bit N must be set for the frame to be transmitted on port N.	0xFFF

1.1.3 ANA:ANA_TABLES

Parent: ANA

Instances: 1

TABLE 1-24: REGISTERS IN ANA_TABLES

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
ANMOVED	0x00000030	1	Station move logger	Page 16
MACHDATA	0x00000034	1	MAC address high	Page 17
MACLDATA	0x00000038	1	MAC address low	Page 17
MACACCESS	0x0000003C	1	MAC table command	Page 17
MACTINDX	0x00000040	1	MAC table index	Page 19
VLANACCESS	0x00000044	1	VLAN table command	Page 19
VLANTIDX	0x00000048	1	VLAN table index	Page 20
ENTRYLIM	0x00000000	12 0x00000004	MAC table entry limits per switch port	Page 20
PTP_ID_HIGH	0x00000054	1	PTP identifiers 63-32	Page 21
PTP_ID_LOW	0x00000058	1	PTP identifiers 31-0	Page 21

1.1.3.1 ANA:ANA_TABLES:ANMOVED

Parent: ANA:ANA_TABLES

Instances: 1

TABLE 1-25: FIELDS IN ANMOVED

Field Name	Bit	Access	Description	Default
ANMOVED	11:0	R/W	This mask detects port moves in the MAC table. When a station is learned on a new port while already learned on another port, the bit corresponding to the new port is set in this mask. This mask can be used to detect topology problems in the network, where stations are learned on multiple ports repeatedly. If some bits in this register get asserted repeatedly, the ports can be shut down, or management warnings can be issued.	0x000

1.1.3.2 ANA:ANA_TABLES:MACHDATA

Parent: ANA:ANA_TABLES

Instances: 1

TABLE 1-26: FIELDS IN MACHDATA

Field Name	Bit	Access	Description	Default
VID	28:16	R/W	VID used in MAC table operations through MACACCESS. For read operations, the VID value is returned in this field.	0x0000
MACHDATA	15:0	R/W	Most significant 16 MAC address bits used in MAC table operations through MACACCESS.	0x0000

1.1.3.3 ANA:ANA_TABLES:MACLDATA

Parent: ANA:ANA_TABLES

Instances: 1

TABLE 1-27: FIELDS IN MACLDATA

Field Name	Bit	Access	Description	Default
MACLDATA	31:0	R/W	Lower 32 MAC address bits used in MAC table operations through MACACCESS.	0x00000000

1.1.3.4 ANA:ANA_TABLES:MACACCESS

Parent: ANA:ANA_TABLES

Instances: 1

This register is used for updating or reading the MAC table from the CPU.

The command (MAC_TABLE_CMD) selects between different operations and uses the following encoding:

000 - IDLE:

The previous operation has completed.

001 - LEARN:

Insert/learn new entry in MAC table. Position given by (MAC, VID) in MACHDATA and MACLDATA.

010 - FORGET:

Delete/unlearn entry given by (MAC, VID) in MACHDATA and MACLDATA.

Both locked and unlocked entries are deleted.

011 - AGE:

Start an age scan on the MAC table.

100 - GET_NEXT:

Get the smallest entry in the MAC table numerically larger than the (MAC, VID) specified in MACHDATA and MACLDATA. The VID and MAC are evaluated as a 60-bit number with the VID being most significant.

101 - INIT:

Table is initialized (completely cleared).

110 - READ:

The READ command is divided into two modes: Direct mode and indirect mode.

Direct mode (read):

With MACACCESS.VALID cleared, the entry pointed to by MACTINDX.M_INDEX (row) and MACTINDX.BUCKET (column) is read.

Indirect mode (lookup):

With MACACCESS.VALID set, the entry pointed to by (MAC, VID) in the MACHDATA and MACLDATA is read.

111 - WRITE

Write entry. Address of the entry is specified in MACTINDX.M_INDEX (row) and MACTINDX.BUCKET (column).

An existing entry (locked or unlocked) is overwritten.

The MAC_TABLE_CMD must be IDLE before a new command can be issued.

The AGE and CLEAR commands run for approximately 50 us. The other commands execute immediately.

The flags IGNORE_VLAN and MAC_CPU_COPY are ignored for DMAC lookup if AGENCTRL.IGNORE_DMAC_FLAGS is set.

The flags SRC_KILL and MAC_CPU_COPY are ignored for SMAC lookup if AGENCTRL.IGNORE_SMAC_FLAGS is set.

TABLE 1-28: FIELDS IN MACACCESS

Field Name	Bit	Access	Description	Default
MAC_CPU_COPY	15	R/W	Frames matching this entry are copied to the CPU extraction queue CPUQ_CFG.CPUQ_MAC_COPY. Applies to both SMAC and DMAC lookup.	0x0
SRC_KILL	14	R/W	Frames matching this entry are discarded. Applies only to the SMAC lookup. For discarding frames based on the DMAC lookup a NULL PGID mask can be used.	0x0
IGNORE_VLAN	13	R/W	The VLAN mask is ignored for this destination. Applies only to DMAC lookup.	0x0
AGED_FLAG	12	R/W	This flag is set on every aging run. Entry is removed if flag is already set. The flag is cleared when the entry is target for a SMAC lookup. Locked entries will not be removed. Bit is for IPv6 Multicast used for port 25.	0x0
VALID	11	R/W	Entry is valid.	0x0
ENTRY_TYPE	10:9	R/W	Type of entry: 0: Normal entry eligible for aging. 1: Locked entry. Entry is not removed by aging. 2: IPv4 Multicast entry. Entry is not removed by aging. 3: IPv6 Multicast entry. Entry is not removed by aging.	0x0

TABLE 1-28: FIELDS IN MACACCESS (CONTINUED)

Field Name	Bit	Access	Description	Default
DEST_IDX	8:3	R/W	Index for the destination masks table (PGID). For unicasts, this is a number from 0-EXB_PORT_CNT_MINUS_ONE.	0x00
MAC_TABLE_CMD	2:0	R/W	MAC Table Command. See below.	0x0

1.1.3.5 ANA:ANA_TABLES:MACTINDX

Parent: ANA:ANA_TABLES

Instances: 1

TABLE 1-29: FIELDS IN MACTINDX

Field Name	Bit	Access	Description	Default
BUCKET	11:10	R/W	Selects one of the four MAC table entries in a row. The row is addressed with the INDEX field.	0x0
M_INDEX	9:0	R/W	The index selects one of the 1024 MAC table rows. Within a row the entry is addressed by the BUCKET field	0x000

1.1.3.6 ANA:ANA_TABLES:VLANACCESS

Parent: ANA:ANA_TABLES

Instances: 1

The VLAN_TBL_CMD field of this register is used for updating and reading the VLAN table. The command (VLAN_TBL_CMD) selects between different operations and uses the following encoding:

00 - IDLE:

The previous operation has completed.

01 - READ:

The VLAN table entry set in VLANTIDX.V_INDEX is returned in VLANACCESS.VLAN_PORT_MASK and the VLAN flags in VLANTIDX.

10 - WRITE:

The VLAN table entry pointed to by VLANTIDX.V_INDEX is updated with VLANACCESS.VLAN_PORT_MASK and the VLAN flags in VLANTIDX.

11 - INIT:

The VLAN table is initialized to default values (all ports are members of all VLANs).

The VLAN_TBL_CMD must be IDLE before a new command can be issued. The INIT command run for approximately 50 us whereas the other commands execute immediately. When an operation has completed, VLAN_TBL_CMD changes to IDLE.

TABLE 1-30: FIELDS IN VLANACCESS

Field Name	Bit	Access	Description	Default
VLAN_PORT_MASK	13:2	R/W	Frames classified to this VLAN can only be sent to ports in this mask. Note that the CPU port module is always member of all VLANs and its VLAN membership can therefore not be configured through this mask.	0x7FF
VLAN_TBL_CMD	1:0	R/W	VLAN Table Command.	0x0

1.1.3.7 ANA:ANA_TABLES:VLANTIDX

Parent: ANA:ANA_TABLES

Instances: 1

TABLE 1-31: FIELDS IN VLANTIDX

Field Name	Bit	Access	Description	Default
VLAN_PRIV_VLAN	15	R/W	If set, a VLAN is a private VLAN. See ISOLATED_PORTS.ISOL_PORTS for details.	0x0
VLAN_LEARN_DISABLED	14	R/W	Disable learning for this VLAN.	0x0
VLAN_MIRROR	13	R/W	If set, all frames classified to this VLAN are mirrored to the port set configured in MIRRORPORTS.	0x0
VLAN_SRC_CHK	12	R/W	If set, VLAN ingress filtering is enabled for this VLAN. If set, a frame's ingress port must be member of the frame's VLAN, otherwise the frame is discarded.	0x0
V_INDEX	11:0	R/W	Index used to select VLAN table entry for read/write operations (see VLANACCESS). This value equals the VID.	0x000

1.1.3.8 ANA:ANA_TABLES:ENTRYLIM

Parent: ANA:ANA_TABLES

Instances: 12

TABLE 1-32: FIELDS IN ENTRYLIM

Field Name	Bit	Access	Description	Default
ENTRYLIM	17:14	R/W	Maximum number of unlocked entries in the MAC table learned on this port. Locked entries and IPMC entries do not obey this limit. Both auto-learned and unlocked CPU-learned entries obey this limit. 0: 1 entry 1: 2 entries n: 2**n entries >12: 8192 entries	0xD
ENTRYSTAT	13:0	R/W	Current number of unlocked MAC table entries learned on this port.	0x0000

1.1.3.9 ANA:ANA_TABLES:PTP_ID_HIGH

Parent: ANA:ANA_TABLES

Instances: 1

TABLE 1-33: FIELDS IN PTP_ID_HIGH

Field Name	Bit	Access	Description	Default
PTP_ID_HIGH	31:0	R/W	Bit vector with current use of PTP timestamp identifiers 32 through 63. Timestamp identifier is 63 is reserved for signaling that no identifiers are available. A timestamp identifier is released by setting the corresponding bit. Bit 0: Timestamp identifier 32 ... Bit 31: Timestamp identifier 63.	0x00000000

1.1.3.10 ANA:ANA_TABLES:PTP_ID_LOW

Parent: ANA:ANA_TABLES

Instances: 1

TABLE 1-34: FIELDS IN PTP_ID_LOW

Field Name	Bit	Access	Description	Default
PTP_ID_LOW	31:0	R/W	Bit vector with current use of PTP timestamp identifiers 0 through 31. A timestamp identifier is released by setting the corresponding bit. Bit 0: Timestamp identifier 0 ... Bit 31: Timestamp identifier 31.	0x0000000F

1.1.4 ANA:PORT

Parent: ANA

Instances: 12

TABLE 1-35: REGISTERS IN PORT

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
VLAN_CFG	0x00000000	1	Port VLAN configuration	Page 22
DROP_CFG	0x00000004	1	VLAN acceptance filtering	Page 23
QOS_CFG	0x00000008	1	QoS and DSCP configuration	Page 23
VCAP_CFG	0x0000000C	1	VCAP configuration	Page 24
VCAP_S1_KEY_CFG	0x00000010	3 0x00000004	VCAP S1 key configuration per S1 lookup	Page 24
VCAP_S2_CFG	0x0000001C	1	VCAP S2 configuration	Page 25
QOS_PCP_DEI_MAP_CFG	0x00000020	16 0x00000004	Mapping of DEI and PCP to QoS class and drop precedence level	Page 26

TABLE 1-35: REGISTERS IN PORT (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CPU_FWD_CFG	0x00000060	1	CPU forwarding of special protocols	Page 26
CPU_FWD_BPDU_CFG	0x00000064	1	CPU forwarding of BPDU frames	Page 27
CPU_FWD_GARP_CFG	0x00000068	1	CPU forwarding of GARP frames	Page 28
CPU_FWD_CCM_CFG	0x0000006C	1	CPU forwarding of CCM/Link trace frames	Page 28
PORT_CFG	0x00000070	1	Special port configuration	Page 29
POL_CFG	0x00000074	1	Policer selection	Page 30
PTP_CFG	0x00000078	1	Timing protocol configuration	Page 31
PTP_DLY1_CFG	0x0000007C	1	PTP ingress delay 1 configuration	Page 32
PTP_DLY2_CFG	0x00000080	1	PTP ingress delay 2 configuration	Page 32

1.1.4.1 ANA:PORT:VLAN_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-36: FIELDS IN VLAN_CFG

Field Name	Bit	Access	Description	Default
VLAN_AWARE_ENA	20	R/W	Enable VLAN awareness. If set, Q-tag headers are processed during the basic VLAN classification. If cleared, Q-tag headers are ignored during the basic VLAN classification.	0x0
VLAN_POP_CNT	19:18	R/W	Number of tag headers to remove from ingress frame. 0: Keep all tags. 1: Pop up to 1 tag (outer tag if available). 2: Pop up to 2 tags (outer and inner tag if available). 3: Disable rewriting of VLAN tags and DSCP value. The rewriter can still update the FCS.	0x0
VLAN_INNER_TAG_ENA	17	R/W	Set if the inner Q-tag must be used instead of the outer Q-tag. If the received frame is single tagged, the outer tag is used. This bit influences the VLAN acceptance filter (DROP_CFG), the basic VLAN classification (VLAN_CFG), and the basic QoS classification (QOS_CFG).	0x0
VLAN_TAG_TYPE	16	R/W	Tag Protocol Identifier type for port-based VLAN. 0: C-tag (EtherType = 0x8100) 1: S-tag (EtherType = 0x88A8 or configurable value (VLAN_ETYPE_CFG))	0x0
VLAN_DEI	15	R/W	DEI value for port-based VLAN.	0x0

TABLE 1-36: FIELDS IN VLAN_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
VLAN_PCP	14:12	R/W	PCP value for port-based VLAN.	0x0
VLAN_VID	11:0	R/W	VID value for port-based VLAN.	0x000

1.1.4.2 ANA:PORT:DROP_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-37: FIELDS IN DROP_CFG

Field Name	Bit	Access	Description	Default
DROP_UNTAGGED_ENA	6	R/W	Drop untagged frames.	0x0
DROP_S_TAGGED_ENA	5	R/W	Drop S-tagged frames (VID different from 0 and EtherType = 0x88A8 or configurable value (VLAN_ETYPE_CFG)).	0x0
DROP_C_TAGGED_ENA	4	R/W	Drop C-tagged frames (VID different from 0 and EtherType = 0x8100).	0x0
DROP_PRIO_S_TAGGED_ENA	3	R/W	Drop S-tagged frames (VID=0 and Ether-Type = 0x88A8 or configurable value (VLAN_ETYPE_CFG)).	0x0
DROP_PRIO_C_TAGGED_ENA	2	R/W	Drop priority C-tagged frames (VID=0 and EtherType = 0x8100).	0x0
DROP_NULL_MAC_ENA	1	R/W	Drop frames with source or destination MAC address equal to 0x000000000000.	0x0
DROP_MC_SMAC_ENA	0	R/W	Drop frames with multicast source MAC address.	0x0

1.1.4.3 ANA:PORT:QOS_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-38: FIELDS IN QOS_CFG

Field Name	Bit	Access	Description	Default
DP_DEFAULT_VAL	8	R/W	Default drop precedence level.	0x0
QOS_DEFAULT_VAL	7:5	R/W	Default QoS class.	0x0
QOS_DSCP_ENA	4	R/W	If set, the DP level and QoS class can be based on DSCP values.	0x0
QOS_PCP_ENA	3	R/W	If set, DP level and QoS class can be based on the PCP and DEI bits for tagged frames.	0x0
DSCP_TRANSLATE_ENA	2	R/W	Set if the DSCP value must be translated before using the DSCP value. If set, the translated DSCP value is given from DSCP_CFG[DSCP].DSCP_TRANS-LATE_VAL.	0x0

TABLE 1-38: FIELDS IN QOS_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
DSCP_REWR_CFG	1:0	R/W	Configure which DSCP values to rewrite based on DP level and QoS class. If the DSCP value is to be rewritten, then the new DSCP = DSCP_REWR_CFG[8*DP level + QoS class].DSCP_QOS_REWR_VAL. 0: Rewrite none. 1: Rewrite if DSCP=0 2: Rewrite for selected values configured in DSCP_CFG[DSCP].DSCP_REWR_ENA. 3: Rewrite all.	0x0

1.1.4.4 ANA:PORT:VCAP_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-39: FIELDS IN VCAP_CFG

Field Name	Bit	Access	Description	Default
S1_ENA	14	R/W	If S1 is enabled, each frame received on this port is processed and matched against the entries in the S1 TCAM. Each frame results in three lookups.	0x0
S1_DMAC_DIP_ENA	13:11	R/W	Set if the destination MAC address and the destination IP address must be used in S1 key instead of the source MAC address and the source IP address. One bit per lookup. Only applicable to S1 keys S1_NORMAL and S1_NORMAL_IP6.	0x0
S1_VLAN_INNER_TAG_ENA	10:8	R/W	Set if the inner Q-tag must be passed on to the S1 TCAM instead of the outer Q-tag. For single tagged frames, the outer tag is used. For untagged frames, the port VLAN is used. This bit influences the TPID, VID, PCP, and DEI input to the S1 key generation. One bit per lookup. Only applicable to S1_NORMAL.	0x0
PAG_VAL	7:0	R/W	Default PAG value used as input to S2. The PAG value can be changed by S1 actions.	0x00

1.1.4.5 ANA:PORT:VCAP_S1_KEY_CFG

Parent: ANA:PORT

Instances: 3

TABLE 1-40: FIELDS IN VCAP_S1_KEY_CFG

Field Name	Bit	Access	Description	Default
S1_KEY_IP6_CFG	6:4	R/W	Selects key per lookup in S1 for IPv6 frames. 0: Use key S1_NORMAL 1: Use key S1_7TUPLE 2: Use key S1_5TUPLE_IP4 3: Use key S1_NORMAL_IP6 4: Use key S1_5TUPLE_IP6 5: Use key S1_DBL_VID	0x0

TABLE 1-40: FIELDS IN VCAP_S1_KEY_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
S1_KEY_IP4_CFG	3:2	R/W	Selects key per lookup in S1 for IPv4 frames. 0: Use key S1_NORMAL 1: Use key S1_7TUPLE 2: Use key S1_5TUPLE_IP4 3: Use key S1_DBL_VID	0x0
S1_KEY_OTHER_CFG	1:0	R/W	Selects key per lookup in S1 for non-IP frames. 0: Use key S1_NORMAL 1: Use key S1_7TUPLE 2: Use key S1_DBL_VID	0x0

1.1.4.6 ANA:PORT:VCAP_S2_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-41: FIELDS IN VCAP_S2_CFG

Field Name	Bit	Access	Description	Default
S2_ENA	14	R/W	If S2 is enabled, each frame received on this port is processed and matched against the entries in the S2 TCAM. Each frame results in two lookups to determine both an ingress and an egress action.	0x0
S2_SNAP_DIS	13:12	R/W	If set, MAC_SNAP frames received on this port are treated as MAC_LLC frames when matching in S2. Bit 0 controls the first lookup and bit 1 controls the second lookup.	0x0
S2_ARP_DIS	11:10	R/W	If set, MAC_ARP frames received on this port are treated as MAC_ETYPE frames when matching in S2. Bit 0 controls the first lookup and bit 1 controls the second lookup.	0x0
S2_IP_TCPUDP_DIS	9:8	R/W	If set, IP_TCPUDP frames received on this port are treated as MAC_ETYPE frames when matching in S2. Bit 0 controls the first lookup and bit 1 controls the second lookup.	0x0
S2_IP_OTHER_DIS	7:6	R/W	If set, IP_OTHER frames received on this port are treated as MAC_ETYPE frames when matching in S2. Bit 0 controls the first lookup and bit 1 controls the second lookup.	0x0

TABLE 1-41: FIELDS IN VCAP_S2_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
S2_IP6_CFG	5:2	R/W	S2_IP6_CFG controls the key generation for IPv6 frames. Bits 1:0 control the first lookup and bits 3:2 control the second lookup. 0: IPv6 frames are matched against IP6_TCP_UDP or IP6_OTHER entries 1: IPv6 frames are matched against IP6_STD entries 2: IPv6 frames are matched against IP4_TCP_UDP or IP4_OTHER entries 3: IPv6 frames are matched against MAC_ETYPE entries	0x1
S2_OAM_DIS	1:0	R/W	If set, OAM frames received on this port are treated as MAC_ETYPE frames when matching in S2. Bit 0 controls the first lookup and bit 1 controls the second lookup.	0x0

1.1.4.7 ANA:PORT:QOS_PCP_DEI_MAP_CFG

Parent: ANA:PORT

Instances: 16

TABLE 1-42: FIELDS IN QOS_PCP_DEI_MAP_CFG

Field Name	Bit	Access	Description	Default
DP_PCP_DEI_VAL	3	R/W	Map the frame's PCP and DEI values to a drop precedence level. DP level = QOS_PCP_DEI_MAP_CFG[index].DP_PCP_DEI_VAL, where index = 8*DEI + PCP. Only applicable to tagged frames. The use of Inner or outer tag can be selected using VLAN_CFG.VLAN_INNER_TAG_ENA.	0x0
QOS_PCP_DEI_VAL	2:0	R/W	Map the frame's PCP and DEI values to a QoS class. QoS class = QOS_PCP_DEI_MAP_CFG[index].QOS_PCP_DEI_VAL, where index = 8*DEI + PCP. Only applicable to tagged frames. The use of inner or outer tag can be selected using VLAN_CFG.VLAN_INNER_TAG_ENA.	0x0

1.1.4.8 ANA:PORT:CPU_FWD_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-43: FIELDS IN CPU_FWD_CFG

Field Name	Bit	Access	Description	Default
CPU_VRAP_REDIR_ENA	7	R/W	If set, VRAP frames are redirected to the CPU extraction queue given by CPUQ_CFG2.CPUQ_VRAP.	0x0
CPU_MLD_REDIR_ENA	6	R/W	If set, MLD frames are redirected to the CPU.	0x0

TABLE 1-43: FIELDS IN CPU_FWD_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
CPU_IGMP_REDIR_ENA	5	R/W	If set, IGMP frames are redirected to the CPU.	0x0
CPU_IPMC_CTRL_COPY_ENA	4	R/W	If set, IPv4 multicast control frames (destination IP address in the range 224.0.0.x) are copied to the CPU.	0x0
CPU_SRC_COPY_ENA	3	R/W	If set, all frames received on this port are copied to the CPU extraction queue given by CPUQ_CFG.CPUQ_SRC_COPY.	0x0
CPU_ALLBRIDGE_DROP_ENA	2	R/W	If set, All LANs Bridge Management Group Address frames (DMAC = 01-80-C2-00-00-10) are not forwarded to any front ports. Together with CPU_ALLBRIDGE_REDIR_ENA, CPU_ALLBRIDGE_DROP_ENA controls the forwarding: CPU_ALLBRIDGE_DROP_ENA=0, CPU_ALLBRIDGE_REDIR_ENA=0: No action CPU_ALLBRIDGE_DROP_ENA=0, CPU_ALLBRIDGE_REDIR_ENA=1: Redirect to CPU CPU_ALLBRIDGE_DROP_ENA=1, CPU_ALLBRIDGE_REDIR_ENA=0: Discard CPU_ALLBRIDGE_DROP_ENA=1, CPU_ALLBRIDGE_REDIR_ENA=1: Copy to CPU	0x0
CPU_ALLBRIDGE_REDIR_ENA	1	R/W	If set, All LANs Bridge Management Group Address frames (DMAC = 01-80-C2-00-00-10) are redirected to the CPU. See also CPU_ALLBRIDGE_DROP_ENA.	0x0

1.1.4.9 ANA:PORT:CPU_FWD_BPDU_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-44: FIELDS IN CPU_FWD_BPDU_CFG

Field Name	Bit	Access	Description	Default
BPDU_DROP_ENA	31:16	R/W	If bit x is set, BPDU frame (DMAC = 01-80-C2-00-00-0x) is not forwarded to any front ports. Together with BPDU_REDIR_ENA, BPDU_-DROP_ENA controls the forwarding of BPDU frames: BPDU_DROP_ENA=0, BPDU_REDIR_ENA=0: No action BPDU_DROP_ENA=0, BPDU_REDIR_ENA=1: Redirect to CPU BPDU_DROP_ENA=1, BPDU_REDIR_ENA=0: Discard BPDU_DROP_ENA=1, BPDU_REDIR_ENA=1: Copy to CPU	0x0000
BPDU_REDIR_ENA	15:0	R/W	If bit x is set, BPDU frame (DMAC = 01-80-C2-00-00-0x) is redirected to the CPU. See also BPDU_DROP_ENA.	0x0000

1.1.4.10 ANA:PORT:CPU_FWD_GARP_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-45: FIELDS IN CPU_FWD_GARP_CFG

Field Name	Bit	Access	Description	Default
GARP_DROP_ENA	31:16	R/W	If bit x is set, GARP frame (DMAC = 01-80-C2-00-00-2x) is not forwarded to any front port. Together with GARP_REDIR_ENA, GARP_-DROP_ENA controls the forwarding of GARP frames: GARP_DROP_ENA=0, GARP_REDIR_ENA=0: No action GARP_DROP_ENA=0, GARP_REDIR_ENA=1: Redirect to CPU GARP_DROP_ENA=1, GARP_REDIR_ENA=0: Discard GARP_DROP_ENA=1, GARP_REDIR_ENA=1: Copy to CPU	0x0000
GARP_REDIR_ENA	15:0	R/W	If bit x is set, GARP frame (DMAC = 01-80-C2-00-00-2x) is redirected to the CPU. See also GARP_DROP_ENA.	0x0000

1.1.4.11 ANA:PORT:CPU_FWD_CCM_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-46: FIELDS IN CPU_FWD_CCM_CFG

Field Name	Bit	Access	Description	Default
CCM_DROP_ENA	31:16	R/W	If bit x is set, CCM/Link trace frame (DMAC = 01-80-C2-00-00-3x) is not forwarded to any front port. Together with CCM_REDIR_ENA, CCM_-DROP_ENA controls the forwarding of CCM/Link trace frames: CCM_DROP_ENA=0, CCM_REDIR_ENA=0: No action CCM_DROP_ENA=0, CCM_REDIR_ENA=1: Redirect to CPU CCM_DROP_ENA=1, CCM_REDIR_ENA=0: Discard CCM_DROP_ENA=1, CCM_REDIR_ENA=1: Copy to CPU	0x0000
CCM_REDIR_ENA	15:0	R/W	If bit x is set, CCM/Link trace frame (DMAC = 01-80-C2-00-00-3x) is redirected to the CPU. See also CCM_DROP_ENA.	0x0000

1.1.4.12 ANA:PORT:PORT_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-47: FIELDS IN PORT_CFG

Field Name	Bit	Access	Description	Default
SRC_MIRROR_ENA	15	R/W	If set, all frames received on this port are mirrored to the port set configured in MIR-RORPORTS (ie. ingress mirroring). For egress mirroring, see EMIRRORMASK.	0x0
LIMIT_DROP	14	R/W	If set, learn frames on an ingress port, which has exceeded the maximum number of MAC table entries are discarded. Forwarding to CPU is still allowed. Note that if LEARN_ENA is cleared, then the LIMIT_-DROP is ignored.	0x0
LIMIT_CPU	13	R/W	If set, learn frames on an ingress port, which has exceeded the maximum number of MAC table entries are copied to the CPU extraction queue specified in CPUQ_CFG.CPUQ_LRN. Note that if LEARN_ENA is cleared, then the LIM-IT_CPU is ignored.	0x0
LOCKED_PORTMOVE_DROP	12	R/W	If set, incoming frames triggering a port move for a locked entry in the MAC table received on this port are discarded. Forward-ing to CPU is still allowed. Note that if LEARN_ENA is cleared, then the LOCKED_PORTMOVE_DROP is ignored.	0x0

TABLE 1-47: FIELDS IN PORT_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
LOCKED_PORTMOVE_CPU	11	R/W	If set, incoming frames triggering a port move for a locked MAC table entry received on this port are copied to the CPU extraction queue specified in CPUQ_CFG.CPUQ_LOCKED_PORT-MOVE. Note that if LEARN_ENA is cleared, then the LOCKED_PORTMOVE_CPU is ignored.	0x0
LEARNDROP	10	R/W	If set, incoming learn frames received on this port are discarded. Forwarding to CPU is still allowed. Note that if LEARN_ENA is cleared, then the LEARNDROP is ignored.	0x0
LEARNCPU	9	R/W	If set, incoming learn frames received on this port are copied to the CPU extraction queue specified in CPUQ_CFG.CPUQ_LRN. Note that if LEARN_ENA is cleared, then the LEARNCPU is ignored.	0x0
LEARNAUTO	8	R/W	If set, incoming learn frames received on this port are auto learned. Note that if LEARN_ENA is cleared, then the LEAR-NAUTO is ignored.	0x1
LEARN_ENA	7	R/W	Enable learning for frames received on this port. If cleared, learning is skipped and any configuration settings in LEARNAUTO, LEARNCPU, LEARNDROP is ignored.	0x1
RECV_ENA	6	R/W	Enable forwarding from this port based on VLAN and destination MAC address. If cleared, the VLAN and MAC tables are not looked up and result is set to 0. Learning and CPU forwarding are still possible.	0x1
PORTID_VAL	5:2	R/W	Logical port number for front port. If port is not a member of a LLAG, then POR-TID must be set to the physical port number. If port is a member of a LLAG, then PORTID must be set to the common PORTID_VAL used for all member ports of the LLAG. The value must not exceed the number of physical ports on the device.	0x0

1.1.4.13 ANA:PORT:POL_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-48: FIELDS IN POL_CFG

Field Name	Bit	Access	Description	Default
POL_CPU_REDIR_8021	19	R/W	If set, frames with a DMAC = IEEE reserved addresses (BPDU, GARP, CCM, ALL-BRIGDE), which are copied to the CPU are not policed by any policers.	0x0

TABLE 1-48: FIELDS IN POL_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
POL_CPU_REDIR_IP	18	R/W	If set, IGMP and MLD frames, which are redirected to the CPU are not policed by any policers. The frames are still counted in the policers buckets.	0x0
PORT_POL_ENA	17	R/W	Enable port policing for frames on received on this port. Port policing on physical port P uses policer P.	0x0
QUEUE_POL_ENA	16:9	R/W	Bit mask, where bit<n>; enables policing of frames classified to QoS class n on this port. Policing of QoS class Q on physical port P uses policer 32+P*8+Q.	0x00
POL_ORDER	8:0	R/W	Each frame is checked against three policers: 1) port, 2) QoS, and 3) VCAP. In this register, a bit set makes updating of a policer dependant on the result from another. Bit<n+3*m> set means: Policer state <n> is checked before policer <m> is updated. Bit0: Port policer must be open in order to update port policer with frame Bit1: QoS policer must be open in order to update port policer with frame Bit2: VCAP policer must be open in order to update port policer with frame Bit3: Port policer must be open in order to update QoS policer with frame Bit4: QoS policer must be open in order to update QoS policer with frame Bit5: VCAP policer must be open in order to update QoS policer with frame Bit6: Port policer must be open in order to update VCAP policer with frame Bit7: QoS policer must be open in order to update VCAP policer with frame Bit8: VCAP policer must be open in order to update VCAP policer with frame	0x1FF

1.1.4.14 ANA:PORT:PTP_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-49: FIELDS IN PTP_CFG

Field Name	Bit	Access	Description	Default
PTP_BACKPLANE_MODE	0	R/W	Backplane mode for PTP. If set, the receive timestamp is read from the PTP header (4 reserved bytes at offset 16) instead of from the ingress timer. Ingress delays, PTP_DLY1_CFG and PTP_DLY2_CFG, are not applied in backplane mode.	0x0

1.1.4.15 ANA:PORT:PTP_DLY1_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-50: FIELDS IN PTP_DLY1_CFG

Field Name	Bit	Access	Description	Default
PTP_DLY1_VAL	31:0	R/W	Delay optionally subtracted from the frame's receive timestamp. This can for instance be a peer-to-peer link delay or a delay due to asymmetry. The subtraction is enabled through IS2 action REW_OP for one-step PTP. Unit is ns. Value is signed.	0x00000000

1.1.4.16 ANA:PORT:PTP_DLY2_CFG

Parent: ANA:PORT

Instances: 1

TABLE 1-51: FIELDS IN PTP_DLY2_CFG

Field Name	Bit	Access	Description	Default
PTP_DLY2_VAL	31:0	R/W	Delay optionally subtracted from the frame's receive timestamp. This can for instance be a peer-to-peer link delay or a delay due to asymmetry. The subtraction is enabled through IS2 action REW_OP for one-step PTP. This is not applicable if the ingress port is in backplane mode. Unit is ns. Value is signed.	0x00000000

1.1.5 ANA:PFC

Parent: ANA

Instances: 11

TABLE 1-52: REGISTERS IN PFC

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PFC_CFG	0x00000000	1	Priority-based flow control configuration	Page 32

1.1.5.1 ANA:PFC:PFC_CFG

Parent: ANA:PFC

Instances: 1

TABLE 1-53: FIELDS IN PFC_CFG

Field Name	Bit	Access	Description	Default
RX_PFC_ENA	9:2	R/W	Enable PFC per priority. Bit n enables PFC on priority n.	0x00

TABLE 1-53: FIELDS IN PFC_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
FC_LINK_SPEED	1:0	R/W	Configures the link speed. This is used to evaluate the time specifications in incoming pause frames. 0: 2500 Mbps 1: 1000 Mbps 2: 100 Mbps 3: 10 Mbps	0x1

1.1.6 ANA:COMMON

Parent: ANA

Instances: 1

TABLE 1-54: REGISTERS IN COMMON

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
AGGR_CFG	0x00000000	1	Aggregation code generation	Page 33
CPUQ_CFG	0x00000004	1	CPU extraction queue configuration	Page 34
CPUQ_CFG2	0x00000008	1	CPU extraction queue configuration 2	Page 34
CPUQ_8021_CFG	0x0000000C	16 0x00000004	CPU extraction queue per address of BPDU, GARP, and CCM frames.	Page 35
DSCP_CFG	0x0000004C	64 0x00000004	DSCP configuration per DSCP value.	Page 35
DSCP_REWR_CFG	0x0000014C	16 0x00000004	DSCP rewrite values per DP level and QoS class	Page 35
VCAP_RNG_TYPE_CFG	0x0000018C	8 0x00000004	VCAP range checkers	Page 36
VCAP_RNG_VAL_CFG	0x000001AC	8 0x00000004	Range configuration per range checker	Page 36
VRAP_CFG	0x000001CC	1	VRAP classifier configuration	Page 36
VRAP_HDR_DATA	0x000001D0	1	VRAP data	Page 37
VRAP_HDR_MASK	0x000001D4	1	VRAP mask	Page 37
DISCARD_CFG	0x000001D8	1	Various options for discard filters	Page 37
FID_CFG	0x000001DC	1	FID selector configuration	Page 37

1.1.6.1 ANA:COMMON:AGGR_CFG

Parent: ANA:COMMON

Instances: 1

TABLE 1-55: FIELDS IN AGGR_CFG

Field Name	Bit	Access	Description	Default
AC_RND_ENA	7	R/W	Use pseudo random number for aggregation code. Overrule other contributions.	0x0

TABLE 1-55: FIELDS IN AGGR_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
AC_DMAC_ENA	6	R/W	Use the lower 12 bits of the destination MAC address for aggregation code.	0x0
AC_SMAC_ENA	5	R/W	Use the lower 12 bits of the source MAC address for aggregation code.	0x0
AC_IP6_FLOW_LBL_ENA	4	R/W	Use the 20-bit IPv6 flow label for aggregation code.	0x0
AC_IP6_TCPUDP_ENA	3	R/W	Use least significant 8 bits of both source port and destination port of IPv6 frames for aggregation code.	0x0
AC_IP4_SIPDIP_ENA	2	R/W	Use least significant 8 bits of both source IP address and destination IP address of IPv4 frames for aggregation code.	0x0
AC_IP4_TCPUDP_ENA	1	R/W	Use least significant 8 bits of both source port and destination port of IPv4 frames for aggregation code.	0x0

1.1.6.2 ANA:COMMON:CPUQ_CFG

Parent: ANA:COMMON

Instances: 1

TABLE 1-56: FIELDS IN CPUQ_CFG

Field Name	Bit	Access	Description	Default
CPUQ_MLD	29:27	R/W	CPU extraction queue used for MLD frames.	0x0
CPUQ_IGMP	26:24	R/W	CPU extraction queue used for IGMP frames.	0x0
CPUQ_IPMC_CTRL	23:21	R/W	CPU extraction queue used for IPv4 multi-cast control frames.	0x0
CPUQ_ALLBRIDGE	20:18	R/W	CPU extraction queue used for All LANs Bridge Management Group Address frames (DMAC = 01-80-C2-00-00-10).	0x0
CPUQ_LOCKED_PORTMOVE	17:15	R/W	CPU extraction queue for frames triggering a port move for a locked MAC table entry.	0x0
CPUQ_SRC_COPY	14:12	R/W	CPU extraction queue for frames copied due to CPU_SRC_COPY_ENA	0x0
CPUQ_MAC_COPY	11:9	R/W	CPU extraction queue for frames copied due to CPU_COPY return by MAC table lookup	0x0
CPUQ_LRN	8:6	R/W	CPU extraction queue for frames copied due to learned or moved stations.	0x0
CPUQ_MIRROR	5:3	R/W	CPU extraction queue for frames copied due to mirroring to the CPU.	0x0
CPUQ_SFLOW	2:0	R/W	CPU extraction queue for frames copied due to SFLOW sampling.	0x0

1.1.6.3 ANA:COMMON:CPUQ_CFG2

Parent: ANA:COMMON

Instances: 1

TABLE 1-57: FIELDS IN CPUQ_CFG2

Field Name	Bit	Access	Description	Default
CPUQ_VRAP	2:0	R/W	CPU extraction queue used for VRAP frames.	0x0

1.1.6.4 ANA:COMMON:CPUQ_8021_CFG

Parent: ANA:COMMON

Instances: 16

The register instance number corresponds to the address of the extracted frame. For instance: CPUQ_8021_CFG[4].CPUQ_BPDU_VAL is the CPU extraction queue used for BPDU frames with address 01-80-C2-00-00-04.

TABLE 1-58: FIELDS IN CPUQ_8021_CFG

Field Name	Bit	Access	Description	Default
CPUQ_BPDU_VAL	8:6	R/W	CPU extraction queue used for BPDU frames.	0x0
CPUQ_GARP_VAL	5:3	R/W	CPU extraction queue used for GARP frames.	0x0
CPUQ_CCM_VAL	2:0	R/W	CPU extraction queue used for CCM/Link trace frames.	0x0

1.1.6.5 ANA:COMMON:DSCP_CFG

Parent: ANA:COMMON

Instances: 64

TABLE 1-59: FIELDS IN DSCP_CFG

Field Name	Bit	Access	Description	Default
DP_DSCP_VAL	11	R/W	Maps the frame's DSCP value to a drop precedence level. This is enabled in QOS_CFG.QOS_DSCP_ENA.	0x0
QOS_DSCP_VAL	10:8	R/W	Maps the frame's DSCP value to a QoS class. This is enabled in QOS_CFG.QOS_DSCP_ENA.	0x0
DSCP_TRANSLATE_VAL	7:2	R/W	Translated DSCP value triggered if DSCP translation is set for port (QOS_CFG[port].DSCP_TRANSLATE_ENA)	0x00
DSCP_TRUST_ENA	1	R/W	Must be set for a DSCP value if the DSCP value is to be used for QoS classification.	0x0
DSCP_REWR_ENA	0	R/W	Set if the DSCP value is selected to be rewritten. This is controlled in QOS_CFG.DSCP_REWR_CFG.	0x0

1.1.6.6 ANA:COMMON:DSCP_REWR_CFG

Parent: ANA:COMMON

Instances: 16

TABLE 1-60: FIELDS IN DSCP_REWR_CFG

Field Name	Bit	Access	Description	Default
DSCP_QOS_REWR_VAL	5:0	R/W	Map the frame's DP level and QoS class to a DSCP value. DSCP = DSCP_RE-WR_CFG[8*DP level + QoS class].DSCP_QOS_REWR_VAL. This is controlled in QOS_CFG.DSCP_REWR_CFG and DSCP_CFG.DSCP_REWR_ENA.	0x00

1.1.6.7 ANA:COMMON:VCAP_RNG_TYPE_CFG

Parent: ANA:COMMON

Instances: 8

TABLE 1-61: FIELDS IN VCAP_RNG_TYPE_CFG

Field Name	Bit	Access	Description	Default
VCAP_RNG_CFG	2:0	R/W	0: Idle 1: TCP/UDP destination port is matched against range 2: TCP/UDP source port is matched against range 3: TCP/UDP source and destination ports are matched against range. Match if either source or destination port is within range. 4: VID is matched against range (S1: VID in frame, S2: classified VID) 5: DSCP value is matched against range 6: Reserved 7: Reserved	0x0

1.1.6.8 ANA:COMMON:VCAP_RNG_VAL_CFG

Parent: ANA:COMMON

Instances: 8

TABLE 1-62: FIELDS IN VCAP_RNG_VAL_CFG

Field Name	Bit	Access	Description	Default
VCAP_RNG_MIN_VAL	31:16	R/W	Lower value. Value is included in range.	0x0000
VCAP_RNG_MAX_VAL	15:0	R/W	Upper value. Value is included in range.	0x0000

1.1.6.9 ANA:COMMON:VRAP_CFG

Parent: ANA:COMMON

Instances: 1

TABLE 1-63: FIELDS IN VRAP_CFG

Field Name	Bit	Access	Description	Default
VRAP_VLAN_AWARE_ENA	12	R/W	If set, VRAP frames must be single VLAN tagged and the frame's VID must match ANA::VRAP_CFG.VRAP_VID. If cleared, VRAP frames must be untagged.	0x0
VRAP_VID	11:0	R/W	VID value for VRAP frames.	0x000

1.1.6.10 ANA:COMMON:VRAP_HDR_DATA

Parent: ANA:COMMON

Instances: 1

TABLE 1-64: FIELDS IN VRAP_HDR_DATA

Field Name	Bit	Access	Description	Default
VRAP_HDR_DATA	31:0	R/W	The frame's VRAP header (4 bytes after EPID) is matched against VRAP_HDR_-DATA, except for bits don't cared by VRAP_HDR_MASK.	0x10000000

1.1.6.11 ANA:COMMON:VRAP_HDR_MASK

Parent: ANA:COMMON

Instances: 1

TABLE 1-65: FIELDS IN VRAP_HDR_MASK

Field Name	Bit	Access	Description	Default
VRAP_HDR_MASK	31:0	R/W	Bits set in VRAP_HDR_MASK don't care the equivalent bits in VRAP_HDR_DATA.	0x07FFFFFF

1.1.6.12 ANA:COMMON:DISCARD_CFG

Parent: ANA:COMMON

Instances: 1

TABLE 1-66: FIELDS IN DISCARD_CFG

Field Name	Bit	Access	Description	Default
RESERVED	3	R/W	Must be set to its default.	0x1
RESERVED	2	R/W	Must be set to its default.	0x1
DROP_TAGGING_S2_ENA	1	R/W	Frames discarded due to wrong tagging will still allow S2 lookup.	0x1
DROP_CTRLPROT_S2_ENA	0	R/W	Frames discarded with L2/L3 protocol filter will still allow S2 lookup.	0x1

1.1.6.13 ANA:COMMON:FID_CFG

Parent: ANA:COMMON

Instances: 1

TABLE 1-67: FIELDS IN FID_CFG

Field Name	Bit	Access	Description	Default
VID_MC_ENA	0	R/W	If set, the frame's classified VID is used instead of the FID for multicast frames when hashing into the MAC table for the DMAC lookup. The IS1 action FID_SEL can still overrule this setting. The SMAC lookup is unchanged by this configuration.	0x0

1.1.7 ANA:POL

Parent: ANA

Instances: 384

General purpose policers selected by port configuration and ACL actions

TABLE 1-68: REGISTERS IN POL

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
POL_PIR_CFG	0x00000000	1	Excess configuration	Page 38
POL_CIR_CFG	0x00000004	1	Committed configuration	Page 38
POL_MODE_CFG	0x00000008	1	Common configuration for this policer	Page 39
POL_PIR_STATE	0x0000000C	1	Excess state of the policer	Page 39
POL_CIR_STATE	0x00000010	1	Committed state of the policer	Page 39

1.1.7.1 ANA:POL:POL_PIR_CFG

Parent: ANA:POL

Instances: 1

TABLE 1-69: FIELDS IN POL_PIR_CFG

Field Name	Bit	Access	Description	Default
PIR_RATE	20:6	R/W	Excess information rate (EIR). Unit is 33 1/3 kbps.	0x0000
PIR_BURST	5:0	R/W	Excess burst size (EBS). Maximum allowed value is 60. Unit is 4 kilobytes.	0x00

1.1.7.2 ANA:POL:POL_CIR_CFG

Parent: ANA:POL

Instances: 1

TABLE 1-70: FIELDS IN POL_CIR_CFG

Field Name	Bit	Access	Description	Default
CIR_RATE	20:6	R/W	Committed information rate (CIR). Unit is 33 1/3 kbps.	0x0000

TABLE 1-70: FIELDS IN POL_CIR_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
CIR_BURST	5:0	R/W	Committed burst size (CBS). Maximum allowed value is 60. Unit is 4 kilobytes.	0x00

1.1.7.3 ANA:POL:POL_MODE_CFG

Parent: ANA:POL

Instances: 1

TABLE 1-71: FIELDS IN POL_MODE_CFG

Field Name	Bit	Access	Description	Default
IPG_SIZE	9:5	R/W	Size of interframe gap to add to each frame if line rate policing is chosen in FRM_MODE.	0x14
FRM_MODE	4:3	R/W	Accounting mode of the policer. 0: Line rate. Measure bytes in frames including IPG_SIZE. 1: Data rate. Measure bytes in frames excluding IPG. 2. Frame rate. Measure frames with rate unit = 33 1/3 frames per second and burst unit = 32.8 frames. 3: Frame rate. Measure frames with rate unit = 1/3 frame per second burst unit = 0.3 frames.	0x0
DLB_COUPLED	2	R/W	Coupling flag. If enabled, yellow frames are allowed to use CIR as well as EIR. If disabled, yellow frames are only allowed to use CIR. 0. Coupling is disabled. 1: Coupling is enabled.	0x0
CIR_ENA	1	R/W	Enable dual leaky bucket mode. If disabled, the policer operates as a single leaky bucket policer governed by POL_PIR_CFG. If enabled, the policer operates as a dual leaky bucket policer governed by POL_PIR_CFG and POL_CIR_CFG.	0x0
RESERVED	0	R/W	Must be set to its default.	0x1

1.1.7.4 ANA:POL:POL_PIR_STATE

Parent: ANA:POL

Instances: 1

TABLE 1-72: FIELDS IN POL_PIR_STATE

Field Name	Bit	Access	Description	Default
PIR_LVL	21:0	R/W	Current fill level of the excess bucket. Unit is 0.5 bits.	0x000000

1.1.7.5 ANA:POL:POL_CIR_STATE

Parent: ANA:POL

Instances: 1

TABLE 1-73: FIELDS IN POL_CIR_STATE

Field Name	Bit	Access	Description	Default
CIR_LVL	21:0	R/W	Current fill level of the committed bucket. Unit is 0.5 bits.	0x000000

1.1.8 ANA:POL_MISC

Parent: ANA

Instances: 1

TABLE 1-74: REGISTERS IN POL_MISC

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
POL_FLOWC	0x00000000	27 0x00000004	Flow control configuration per front port	Page 40
POL_HYST	0x0000006C	1	Set flow control hysteresis	Page 40

1.1.8.1 ANA:POL_MISC:POL_FLOWC

Parent: ANA:POL_MISC

Instances: 27

TABLE 1-75: FIELDS IN POL_FLOWC

Field Name	Bit	Access	Description	Default
POL_FLOWC	0	R/W	Use MAC flow control for lowering ingress rate 0: Standard policing. Frames are discarded when the rate is exceeded. 1: Flow control policing. Policer instructs the MAC to issue pause frames when the rate is exceeded.	0x0

1.1.8.2 ANA:POL_MISC:POL_HYST

Parent: ANA:POL_MISC

Instances: 1

TABLE 1-76: FIELDS IN POL_HYST

Field Name	Bit	Access	Description	Default
POL_FC_HYST	9:4	R/W	Set hysteresis for when to re-open a bucket after the burst capacity has been used. Unit is 1 kilobytes. This applies to policer in flow control mode (POL_FLOWC=1).	0x02
POL_DROP_HYST	3:0	R/W	Set hysteresis for when to re-open a bucket after the burst capacity has been used. Unit is 2 kilobytes. This applies to policer in drop mode (POL_FLOWC=0).	0x0

1.2 DEV

TABLE 1-77: REGISTER GROUPS IN DEV

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
PORT_MODE	0x00000000	1	Port configuration	Page 41
MAC_CFG_STATUS	0x0000001C	1	MAC configuration and status	Page 44
PCS1G_CFG_STATUS	0x00000048	1	PCS 1G Configuration Status Registers	Page 50
PCS1G_TSTPAT_CFG_STATUS	0x0000008C	1	PCS1G Testpattern Configuration and Status Registers	Page 57
PCS_FX100_CONFIGURATION	0x00000094	1	PCS FX100 Configuration Registers	Page 58
PCS_FX100_STATUS	0x00000098	1	PCS FX100 Status Registers	Page 59

1.2.1 DEV:PORT_MODE

Parent: DEV

Instances: 1

TABLE 1-78: REGISTERS IN PORT_MODE

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CLOCK_CFG	0x00000000	1	Clock and reset configuration	Page 41
PORT_MISC	0x00000004	1	Forwarding configuration of special frame types	Page 42
EEE_CFG	0x0000000C	1	Control Energy Efficient Ethernet operation.	Page 42
RX_PATH_DELAY	0x00000010	1	Local path delay compensation per front port	Page 43
TX_PATH_DELAY	0x00000014	1	Local path delay compensation per front port	Page 43
PTP_PREDICT_CFG	0x00000018	1	PTP Predictor Configuration per port	Page 43

1.2.1.1 DEV:PORT_MODE:CLOCK_CFG

Parent: DEV:PORT_MODE

Instances: 1

TABLE 1-79: FIELDS IN CLOCK_CFG

Field Name	Bit	Access	Description	Default
MAC_TX_RST	7	R/W	Reset the MAC Tx clock domain.	0x1
MAC_RX_RST	6	R/W	Reset the MAC Rx clock domain.	0x1
PCS_TX_RST	5	R/W	Reset the PCS Tx clock domain.	0x1
PCS_RX_RST	4	R/W	Reset the PCS Rx clock domain.	0x1
PORT_RST	3	R/W		0x1

TABLE 1-79: FIELDS IN CLOCK_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
RESERVED	2	R/W	Must be set to its default.	0x1
LINK_SPEED	1:0	R/W	Selects the link speed. 0: No link 1: 1000/2500 Mbps 2: 100 Mbps 3: 10 Mbps	0x0

1.2.1.2 DEV:PORT_MODE:PORT_MISC

Parent: DEV:PORT_MODE

Instances: 1

TABLE 1-80: FIELDS IN PORT_MISC

Field Name	Bit	Access	Description	Default
FWD_ERROR_ENA	4	R/W	Forward frames with errors signaled by the MAC.	0x0
FWD_PAUSE_ENA	3	R/W	Forward pause frames (EtherType = 0x8808, opcode = 0x0001). The reaction to incoming pause frames is controlled independently of FWD_PAUSE_ENA.	0x0
FWD_CTRL_ENA	2	R/W	Forward MAC control frames excluding pause frames (EtherType = 0x8808, opcode different from 0x0001).	0x0

1.2.1.3 DEV:PORT_MODE:EEE_CFG

Parent: DEV:PORT_MODE

Instances: 1

TABLE 1-81: FIELDS IN EEE_CFG

Field Name	Bit	Access	Description	Default
EEE_ENA	22	R/W	Enable EEE operation on the port. A port enters the low power mode when no egress queues have data ready. The port is activated when one of the following conditions is true: - A queue has been non-empty for EEE_TIMER_AGE. - A queue has more than EEE_HIGH_FRAMES frames pending. - A queue has more than EEE_HIGH_BYTES bytes pending. - A queue is marked as a fast queue, and has data pending.	0x0

TABLE 1-81: FIELDS IN EEE_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
EEE_TIMER_AGE	21:15	R/W	Maximum time frames in any queue must wait before the port is activated. The default value corresponds to 48 us. Time = 4**(EEE_TIMER_AGE/16) * (EEE_-TIMER_AGE mod 16) microseconds	0x23
EEE_TIMER_WAKEUP	14:8	R/W	Time from the egress port is activated until frame transmission is restarted. Default value corresponds to 16 us. Time = 4**(EEE_TIMER_WAKEUP/16) * (EEE_TIMER_WAKEUP mod 16) microseconds	0x14
EEE_TIMER_HOLDOFF	7:1	R/W	When all queues are empty, the port is kept active until this time has passed. Default value corresponds to 5 us. Time = 4**(EEE_TIMER_HOLDOFF/16) * (EEE_TIMER_HOLDOFF mod 16) microseconds	0x05
PORT_LPI	0	R/O	Status bit indicating whether port is in low-power-idle due to the LPI algorithm (EEE_CFG). If set, transmissions are held back.	0x0

1.2.1.4 DEV:PORT_MODE:RX_PATH_DELAY

Parent: DEV:PORT_MODE

Instances: 1

TABLE 1-82: FIELDS IN RX_PATH_DELAY

Field Name	Bit	Access	Description	Default
RX_PATH_DELAY	23:0	R/W	Delay through the local system receive path, which is added to the frame's receive time-stamp. The value is signed. Unit: Nanoseconds	0xFFFFD8

1.2.1.5 DEV:PORT_MODE:TX_PATH_DELAY

Parent: DEV:PORT_MODE

Instances: 1

TABLE 1-83: FIELDS IN TX_PATH_DELAY

Field Name	Bit	Access	Description	Default
TX_PATH_DELAY	23:0	R/W	Delay through the local system transmit path, which is added to the frame's transmit timestamp. The value is signed. Unit: Nanoseconds	0x000028

1.2.1.6 DEV:PORT_MODE:PTP_PREDICT_CFG

Parent: DEV:PORT_MODE

Instances: 1

TABLE 1-84: FIELDS IN PTP_PREDICT_CFG

Field Name	Bit	Access	Description	Default
PTP_PHY_PREDICT_CFG	11:4	R/W	Enables various informations from internal phy when finding the right ingress delayTime in ns to add to timestamper in the egress direction to compensate for static delay through the physical encoding layers. ffe1000, ffe100, rx_pkt, nibbl40, nibb400, add_delay200 xxxxxxx1: FFE1000 value will be added xxxxxx1x: FFE100 value will be added xxxxx1xx: Rx_Pkt delay x8 will be added xxxx1xxx: 40 ns will be added if nibble_inserted is set xxx1xxxx: 400 ns will be added if nibble inserted is set xx1xxxxx: 200 ns will be added if add_delay200 is set x1xxxxxx: Nibble inserted will be inverted 1xxxxxxx: RxPkt delay will be negated	0x00
PTP_PHASE_PREDICT_CFG	3:0	R/W	Enables increased accuracy in the time stamping logic, by finding the dynamic phase between port and 1588 clocks. This setting is used for both directions. 0001: 125 MHz port clock 0010: 25 MHz port clock 0011: 2.5 MHz port clock 0100: 161.13 MHz port clock 0101: 156.25 MHz port clock others: Disabled	0x0

1.2.2 DEV:MAC_CFG_STATUS

Parent: DEV

Instances: 1

The 1G/2.5G MAC module contains configuration and status registers related to the MAC module of the 1G and 2.5G ports.

TABLE 1-85: REGISTERS IN MAC_CFG_STATUS

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MAC_ENA_CFG	0x00000000	1	Mode Configuration Register	Page 45
MAC_MODE_CFG	0x00000004	1	Mode Configuration Register	Page 45
MAC_MAXLEN_CFG	0x00000008	1	Max Length Configuration Register	Page 45
MAC_TAGS_CFG	0x0000000C	1	VLAN / Service tag configuration register	Page 46
MAC_ADV_CHK_CFG	0x00000010	1	Advanced Check Feature Configuration Register	Page 46
MAC_IFG_CFG	0x00000014	1	Inter Frame Gap Configuration Register	Page 47

TABLE 1-85: REGISTERS IN MAC_CFG_STATUS (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MAC_HDX_CFG	0x00000018	1	Half-duplex Configuration Register	Page 47
MAC_FC_MAC_LOW_CFG	0x00000020	1	MAC Flow Control Configuration Register	Page 48
MAC_FC_MAC_HIGH_CFG	0x00000024	1	MAC Flow Control Configuration Register	Page 48
MAC_STICKY	0x00000028	1	Sticky Bit Register	Page 48

1.2.2.1 DEV:MAC_CFG_STATUS:MAC_ENA_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

TABLE 1-86: FIELDS IN MAC_ENA_CFG

Field Name	Bit	Access	Description	Default
RX_ENA	4	R/W	Receiver Module Enable. '0': Receiver Module Disabled '1': Receiver Module Enabled	0x0
TX_ENA	0	R/W	Transmitter Module Enable. '0': Transmitter Module Disabled '1': Transmitter Module Enabled	0x0

1.2.2.2 DEV:MAC_CFG_STATUS:MAC_MODE_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

TABLE 1-87: FIELDS IN MAC_MODE_CFG

Field Name	Bit	Access	Description	Default
GIGA_MODE_ENA	4	R/W	Enables 1 Gbps mode. '0': 10/100 Mbps mode '1': 1 Gbps mode. Note: FDX_ENA must also be set.	0x1
FDX_ENA	0	R/W	Enables full-duplex: '0': Half-duplex '1': Full-duplex. Note: Full-duplex MUST be selected if GIGA_MODE is enabled.	0x1

1.2.2.3 DEV:MAC_CFG_STATUS:MAC_MAXLEN_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

TABLE 1-88: FIELDS IN MAC_MAXLEN_CFG

Field Name	Bit	Access	Description	Default
MAX_LEN	15:0	R/W	Maximum frame length in bytes accepted by the MAC. Frames that are longer than the maximum length are discarded.	0x05EE

1.2.2.4 DEV:MAC_CFG_STATUS:MAC_TAGS_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

The MAC can be configured to accept 0, 1 and 2 tags and the TAG value can be user-defined.

TABLE 1-89: FIELDS IN MAC_TAGS_CFG

Field Name	Bit	Access	Description	Default
TAG_ID	31:16	R/W	This field defines which EtherTypes are recognized as a VLAN TPID - besides 0x8100. The value is used for all tag positions. I.e. a double tagged frame can have the following tag values: (TAG1,TAG2): (0x8100, 0x8100) (0x8100, TAG_ID) (TAG_ID, 0x8100) or (TAG_ID, TAG_ID) Single tagged frame can have the following TPID values: 0x8100 or TAG_ID.	0x8100
VLAN_LEN_AWR_ENA	2	R/W	When set, single tagged frames are allowed to be 4 bytes longer than the MAC_MAXLEN_CFG configuration and double tagged frames are allowed to be 8 bytes longer. Single tagged frames are adjusted if VLAN_AWR_ENA is also set. Double tagged frames are adjusted if both VLAN_AWR_ENA and VLAN_DBL_AWR_ENA are set.	0x1
VLAN_DBL_AWR_ENA	1	R/W	If set, double tagged frames are subject to length adjustments (VLAN_LEN_AWR_ENA). VLAN_AWR_ENA must be set when VLAN_DBL_AWR_ENA is set. '0': The MAC does not look for inner tags. '1': The MAC accepts inner tags with TPID=0x8100 or TAG_ID.	0x0
VLAN_AWR_ENA	0	R/W	If set, single tagged frames are subject to length adjustments (VLAN_LEN_AWR_ENA). '0': The MAC does not look for any tags. '1': The MAC accepts outer tags with TPID=0x8100 or TAG_ID.	0x0

1.2.2.5 DEV:MAC_CFG_STATUS:MAC_ADV_CHK_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

TABLE 1-90: FIELDS IN MAC_ADV_CHK_CFG

Field Name	Bit	Access	Description	Default
LEN_DROP_ENA	0	R/W	Length Drop Enable: Configures the Receive Module to drop frames in reference to in-range and out-of-range errors: '0': Length Drop Disabled '1': Length Drop Enabled.	0x0

1.2.2.6 DEV:MAC_CFG_STATUS:MAC_IFG_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

TABLE 1-91: FIELDS IN MAC_IFG_CFG

Field Name	Bit	Access	Description	Default
TX_IFG	12:8	R/W	Used to adjust the duration of the inter-frame gap in the Tx direction and must be set according to the speed and duplex settings. 10/100 Mbps, HDX, FDX 0x19, 0x13 1000 Mbps: 0x07.	0x07
RX_IFG2	7:4	R/W	Used to adjust the duration of the second part of the inter-frame gap in the Rx direction and must be set according to the speed and duplex settings. 10/100 Mbps, HDX, FDX: 0x8, 0xB 1000 Mbps: 0x1.	0x1
RX_IFG1	3:0	R/W	Used to adjust the duration of the first part of the inter-frame gap in the Rx direction and must be set according to the speed settings. 10/100 Mbps: 0x7 1000 Mbps: 0x5.	0x5

1.2.2.7 DEV:MAC_CFG_STATUS:MAC_HDX_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

TABLE 1-92: FIELDS IN MAC_HDX_CFG

Field Name	Bit	Access	Description	Default
WEXC_DIS	24	R/W	Determines whether the MAC backs off after an excessive collision has occurred. If set, back off is disabled after excessive collisions. '0': Back off after excessive collisions '1': Don't back off after excessive collisions	0x0
SEED	23:16	R/W	Seed value loaded into the PRBS of the MAC. Used to prevent excessive collision events.	0x00

TABLE 1-92: FIELDS IN MAC_HDX_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
SEED_LOAD	12	R/W	Load SEED value into PRNG register. A SEED value is loaded into the PRNG register of the MAC, when SEED_LOAD is asserted. After a load, the SEED_LOAD must be deasserted. '0': Do not load SEED value '1': Load SEED value.	0x0
RETRY_AFTER_EXC_COL_ENA	8	R/W	This bit is used to setup the MAC to retransmit a frame after an early collision even though 16 (or more) early collisions have occurred. '0': A frame is discarded and counted as an excessive collision if 16 collisions occur for this frame. '1': The MAC retransmits a frame after an early collision, regardless of the number of previous early collisions. The backoff sequence is reset after every 16 collisions.	0x0
LATE_COL_POS	6:0	R/W	Adjustment of early/late collision boundary: This bitgroup is used to adjust the MAC so that a collision on a shared transmission medium before bit 512 is handled as an early collision, whereas a collision after bit 512 is handled as a late collision, i.e. no retransmission is performed.	0x43

1.2.2.8 DEV:MAC_CFG_STATUS:MAC_FC_MAC_LOW_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

TABLE 1-93: FIELDS IN MAC_FC_MAC_LOW_CFG

Field Name	Bit	Access	Description	Default
MAC_LOW	23:0	R/W	Lower three bytes in the SMAC in generated flow control frames. 0xNNN: Lower three DMAC bytes	0x000000

1.2.2.9 DEV:MAC_CFG_STATUS:MAC_FC_MAC_HIGH_CFG

Parent: DEV:MAC_CFG_STATUS

Instances: 1

TABLE 1-94: FIELDS IN MAC_FC_MAC_HIGH_CFG

Field Name	Bit	Access	Description	Default
MAC_HIGH	23:0	R/W	Higher three bytes in the SMAC in generated flow control frames. 0xNNN: Higher three DMAC bytes	0x000000

1.2.2.10 DEV:MAC_CFG_STATUS:MAC_STICKY

Parent: DEV:MAC_CFG_STATUS

Instances: 1

Clear the sticky bits by writing a '0' in the relevant bitgroups (writing a '1' sets the bit)!.

TABLE 1-95: FIELDS IN MAC_STICKY

Field Name	Bit	Access	Description	Default
RX_IPG_SHRINK_STICKY	9	Sticky	Sticky bit indicating that an inter packet gap shrink was detected (IPG < 12 bytes).	0x0
RX_PREAM_SHRINK_STICKY	8	Sticky	Sticky bit indicating that a preamble shrink was detected (preamble < 8 bytes). '0': no preamble shrink was detected '1': a preamble shrink was detected one or more times Bit is cleared by writing a '1' to this position.	0x0
RX_CARRIER_EXT_STICKY	7	Sticky	Sticky bit indicating that a carrier extend was detected. '0': no carrier extend was detected '1': one or more carrier extends were detected Bit is cleared by writing a '1' to this position.	0x0
RX_CARRIER_EXT_ERR_-STICKY	6	Sticky	Sticky bit indicating that a carrier extend error was detected. '0': no carrier extend error was detected '1': one or more carrier extend errors were detected Bit is cleared by writing a '1' to this position.	0x0
RX_JUNK_STICKY	5	Sticky	Sticky bit indicating that junk was received (bytes not recognized as a frame). '0': no junk was received '1': junk was received one or more times Bit is cleared by writing a '1' to this position.	0x0
TX_RETRANSMIT_STICKY	4	Sticky	Sticky bit indicating that the transmit MAC asked the host for a frame retransmission. '0': no tx retransmission was initiated '1': one or more tx retransmissions were initiated Bit is cleared by writing a '1' to this position.	0x0
TX_JAM_STICKY	3	Sticky	Sticky bit indicating that the transmit host issued a jamming signal. '0': the transmit host issued no jamming signal '1': the transmit host issued one or more jamming signals Bit is cleared by writing a '1' to this position.	0x0
TX_FIFO_OFLW_STICKY	2	Sticky	Sticky bit indicating that the MAC transmit FIFO has overrun.	0x0
TX_FRM_LEN_OVR_STICKY	1	Sticky	Sticky bit indicating that the transmit frame length has overrun. I.e. a frame longer than 64K occurred. '0': no tx frame length error occurred '1': one or more tx frames length errors occurred Bit is cleared by writing a '1' to this position.	0x0
TX_ABORT_STICKY	0	Sticky	Sticky bit indicating that the transmit host initiated abort was executed.	0x0

1.2.3 DEV:PCS1G_CFG_STATUS

Parent: DEV

Instances: 1

Configuration and status register set for PCS1G

TABLE 1-96: REGISTERS IN PCS1G_CFG_STATUS

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PCS1G_CFG	0x00000000	1	PCS1G Configuration	Page 50
PCS1G_MODE_CFG	0x00000004	1	PCS1G Mode Configuration	Page 51
PCS1G_SD_CFG	0x00000008	1	PCS1G Signal Detect Configuration	Page 51
PCS1G_ANEG_CFG	0x0000000C	1	PCS1G Aneg Configuration	Page 51
PCS1G_ANEG_NP_CFG	0x00000010	1	PCS1G Aneg Next Page Configuration	Page 52
PCS1G_LB_CFG	0x00000014	1	PCS1G Loopback Configuration	Page 52
PCS1G_ANEG_STATUS	0x00000020	1	PCS1G ANEG Status Register	Page 53
PCS1G_ANEG_NP_STATUS	0x00000024	1	PCS1G Aneg Next Page Status Register	Page 53
PCS1G_LINK_STATUS	0x00000028	1	PCS1G link status	Page 53
PCS1G_LINK_DOWN_CNT	0x0000002C	1	PCS1G link down counter	Page 54
PCS1G_STICKY	0x00000030	1	PCS1G sticky register	Page 54
PCS1G_DEBUG_STATUS	0x00000034	1	PCS1G debug status	Page 55
PCS1G_LPI_CFG	0x00000038	1	PCS1G Low Power Idle Configuration	Page 55
PCS1G_LPI_WAKE_ERROR_CNT	0x0000003C	1	PCS1G wake error counter	Page 56
PCS1G_LPI_STATUS	0x00000040	1	PCS1G Low Power Idle Status	Page 56

1.2.3.1 DEV:PCS1G_CFG_STATUS:PCS1G_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G main configuration register

TABLE 1-97: FIELDS IN PCS1G_CFG

Field Name	Bit	Access	Description	Default
LINK_STATUS_TYPE	4	R/W	Set type of link_status indication at CPU-System 0: Sync_status (from PCS synchronization state machine) 1: Bit 15 of PCS1G_ANEG_STATUS.lp_adv_ability (Link up/down)	0x0

TABLE 1-97: FIELDS IN PCS1G_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
PCS_ENA	0	R/W	PCS enable 0: Disable PCS 1: Enable PCS	0x0

1.2.3.2 DEV:PCS1G_CFG_STATUS:PCS1G_MODE_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G mode configuration

TABLE 1-98: FIELDS IN PCS1G_MODE_CFG

Field Name	Bit	Access	Description	Default
UNIDIR_MODE_ENA	4	R/W	Unidirectional mode enable. Implementation of 802.3, Clause 66. When asserted, this enables MAC to transmit data independent of the state of the receive link. 0: Unidirectional mode disabled 1: Unidirectional mode enabled	0x0
SGMII_MODE_ENA	0	R/W	Selection of PCS operation 0: PCS is used in SERDES mode 1: PCS is used in SGMII mode	0x1

1.2.3.3 DEV:PCS1G_CFG_STATUS:PCS1G_SD_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G signal_detect configuration

TABLE 1-99: FIELDS IN PCS1G_SD_CFG

Field Name	Bit	Access	Description	Default
SD_SEL	8	R/W	Signal detect selection (select input for internal signal_detect line) 0: Select signal_detect line from hardmacro 1: Select external signal_detect line	0x0
SD_POL	4	R/W	Signal detect polarity: The signal level on signal_detect input pin must be equal to SD_POL to indicate signal detection (SD_ENA must be set) 0: Signal Detect input pin must be '0' to indicate a signal detection 1: Signal Detect input pin must be '1' to indicate a signal detection	0x1
SD_ENA	0	R/W	Signal Detect Enable 0: The Signal Detect input pin is ignored. The PCS assumes an active Signal Detect at all times 1: The Signal Detect input pin is used to determine if a signal is detected	0x1

1.2.3.4 DEV:PCS1G_CFG_STATUS:PCS1G_ANEG_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G Auto-negotiation configuration register

TABLE 1-100: FIELDS IN PCS1G_ANEG_CFG

Field Name	Bit	Access	Description	Default
ADV_ABILITY	31:16	R/W	Advertised Ability Register: Holds the capabilities of the device as described IEEE 802.3, Clause 37.	0x0000
SW_RESOLVE_ENA	8	R/W	Software Resolve Abilities 0: If Auto Negotiation fails (no matching HD or FD capabilities) the link is disabled. 1: The result of an Auto Negotiation is ignored - the link can be setup through software. This bit must be set in SGMII mode.	0x0
ANEG_RESTART_ONE_SHOT	1	One-shot	Auto Negotiation Restart 0: No action 1: Restart Auto Negotiation	0x0
ANEG_ENA	0	R/W	Auto Negotiation Enable 0: Auto Negotiation Disabled 1: Auto Negotiation Enabled	0x0

1.2.3.5 DEV:PCS1G_CFG_STATUS:PCS1G_ANEG_NP_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G Auto-negotiation configuration register for next-page function

TABLE 1-101: FIELDS IN PCS1G_ANEG_NP_CFG

Field Name	Bit	Access	Description	Default
NP_TX	31:16	R/W	Next page register: Holds the next-page information as described in IEEE 802.3, Clause 37	0x0000
NP_LOADED_ONE_SHOT	0	One-shot	Next page loaded 0: next page is free and can be loaded 1: next page register has been filled (to be set after np_tx has been filled)	0x0

1.2.3.6 DEV:PCS1G_CFG_STATUS:PCS1G_LB_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G loopback configuration register

TABLE 1-102: FIELDS IN PCS1G_LB_CFG

Field Name	Bit	Access	Description	Default
TBI_HOST_LB_ENA	0	R/W	Loops data in PCS (TBI side) from egress direction to ingress direction. The Rx clock is automatically set equal to the Tx clock 0: TBI Loopback Disabled 1:TBI Loopback Enabled	0x0

1.2.3.7 DEV:PCS1G_CFG_STATUS:PCS1G_ANEG_STATUS

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G Auto-negotiation status register

TABLE 1-103: FIELDS IN PCS1G_ANEG_STATUS

Field Name	Bit	Access	Description	Default
LP_ADV_ABILITY	31:16	R/O	Advertised abilities from link partner as described in IEEE 802.3, Clause 37	0x0000
PR	4	R/O	Resolve priority 0: ANEG is in progress 1: ANEG nearly finished - priority can be resolved (through software)	0x0
PAGE_RX_STICKY	3	Sticky	Status indicating whether a new page has been received. 0: No new page received 1: New page received Bit is cleared by writing a 1 to this position.	0x0
ANEG_COMPLETE	0	R/O	Auto Negotiation Complete 0: No Auto Negotiation has been completed 1: Indicates that an Auto Negotiation has completed successfully	0x0

1.2.3.8 DEV:PCS1G_CFG_STATUS:PCS1G_ANEG_NP_STATUS

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G Auto-negotiation next page status register

TABLE 1-104: FIELDS IN PCS1G_ANEG_NP_STATUS

Field Name	Bit	Access	Description	Default
LP_NP_RX	31:16	R/O	Next page ability register from link partner as described in IEEE 802.3, Clause 37	0x0000

1.2.3.9 DEV:PCS1G_CFG_STATUS:PCS1G_LINK_STATUS

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G link status register

TABLE 1-105: FIELDS IN PCS1G_LINK_STATUS

Field Name	Bit	Access	Description	Default
DELAY_VAR	15:12	R/O	Additional delay in rx-path; multiply the value of this field by the line-rate bit-period (800ps for 10/100/1000, 320ps for 2G5 mode.) This field is valid when the link is up, it remains constant for as long as the link is up, value may change on link-down event. This field shows the number of data bits that is stored in the rx comma-alignment block, values of 0-9 is possible.	0x0
SIGNAL_DETECT	8	R/O	Indicates whether or not the selected Signal Detect input line is asserted; does not consider the Polarity 0: No signal detected 1: Signal detected	0x0
LINK_STATUS	4	R/O	Indicates whether the link is up or down. A link is up when ANEG state machine is in state LINK_OK or AN_DISABLE_LINK_OK 0: Link down 1: Link up	0x0
SYNC_STATUS	0	R/O	Indicates if PCS has successfully synchronized 0: PCS is out of sync 1: PCS has synchronized	0x0

1.2.3.10 DEV:PCS1G_CFG_STATUS:PCS1G_LINK_DOWN_CNT

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G link down counter register

TABLE 1-106: FIELDS IN PCS1G_LINK_DOWN_CNT

Field Name	Bit	Access	Description	Default
LINK_DOWN_CNT	7:0	R/W	Link Down Counter. A counter that counts the number of times a link has been down. The counter does not saturate at 255 and is only cleared when writing 0 to the register	0x00

1.2.3.11 DEV:PCS1G_CFG_STATUS:PCS1G_STICKY

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G status register for sticky bits

TABLE 1-107: FIELDS IN PCS1G_STICKY

Field Name	Bit	Access	Description	Default
LINK_DOWN_STICKY	4	Sticky	The sticky bit is set when the link has been down - i.e. if the ANEG state machine has not been in the AN_DISABLE_LINK_OK or LINK_OK state for one or more clock cycles. This occurs if e.g. ANEG is restarted or for example if signal-detect or synchronization has been lost for more than 10 ms (1.6 ms in SGMII mode). By setting the UDLT bit, the required down time can be reduced to 9,77 us (1.56 us) 0: Link is up 1: Link has been down Bit is cleared by writing a 1 to this position.	0x0
OUT_OF_SYNC_STICKY	0	Sticky	Sticky bit indicating if PCS synchronization has been lost 0: Synchronization has not been lost at any time 1: Synchronization has been lost for one or more clock cycles Bit is cleared by writing a 1 to this position.	0x0

1.2.3.12 DEV:PCS1G_CFG_STATUS:PCS1G_DEBUG_STATUS

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G debug status register

TABLE 1-108: FIELDS IN PCS1G_DEBUG_STATUS

Field Name	Bit	Access	Description	Default
XMIT_MODE	13:12	R/O	Indicates the mode of the TBI 00: Idle mode 01: Configuration mode 10: Reserved 11: Data mode	0x0

1.2.3.13 DEV:PCS1G_CFG_STATUS:PCS1G_LPI_CFG

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

Configuration register for Low Power Idle (Energy Efficient Ethernet)

TABLE 1-109: FIELDS IN PCS1G_LPI_CFG

Field Name	Bit	Access	Description	Default
QSGMII_MS_SEL	20	R/W	QSGMII master/slave selection (only one master allowed per QSGMII). The master drives LPI timing on serdes 0: Slave 1: Master	0x1

TABLE 1-109: FIELDS IN PCS1G_LPI_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
LPI_RX_WTIM	5:4	R/W	Max wake-up time before link_fail 00: 10 us 01: 13 us 10: 17 us 11: 20 us	0x3
TX_ASSERT_LPIDLE	0	R/W	Assert Low-Power Idle (LPI) in transmit mode 0: Disable LPI transmission 1: Enable LPI transmission	0x0

1.2.3.14 DEV:PCS1G_CFG_STATUS:PCS1G_LPI_WAKE_ERROR_CNT

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

PCS1G Low Power Idle wake error counter (Energy Efficient Ethernet)

TABLE 1-110: FIELDS IN PCS1G_LPI_WAKE_ERROR_CNT

Field Name	Bit	Access	Description	Default
WAKE_ERROR_CNT	15:0	R/W	Wake Error Counter. A counter that is incremented when the link partner does not send wake-up burst in due time. The counter saturates at 65535 and is cleared when writing 0 to the register	0x0000

1.2.3.15 DEV:PCS1G_CFG_STATUS:PCS1G_LPI_STATUS

Parent: DEV:PCS1G_CFG_STATUS

Instances: 1

Status register for Low Power Idle (Energy Efficient Ethernet)

TABLE 1-111: FIELDS IN PCS1G_LPI_STATUS

Field Name	Bit	Access	Description	Default
RX_LPI_FAIL	16	R/O	Receiver has failed to recover from Low-Power Idle mode 0: No failure 1: Failed to recover from LPI mode	0x0
RX_LPI_EVENT_STICKY	12	Sticky	Receiver Low-Power idle occurrence 0: No LPI symbols received 1: Receiver has received LPI symbols Bit is cleared by writing a 1 to this position.	0x0
RX_QUIET	9	R/O	Receiver Low-Power Quiet mode 0: Receiver not in quiet mode 1: Receiver is in quiet mode	0x0
RX_LPI_MODE	8	R/O	Receiver Low-Power Idle mode 0: Receiver not in low power idle mode 1: Receiver is in low power idle mode	0x0
TX_LPI_EVENT_STICKY	4	Sticky	Transmitter Low-Power idle occurrence 0: No LPI symbols transmitted 1: Transmitter has transmitted LPI symbols Bit is cleared by writing a 1 to this position.	0x0

TABLE 1-111: FIELDS IN PCS1G_LPI_STATUS (CONTINUED)

Field Name	Bit	Access	Description	Default
TX_QUIET	1	R/O	Transmitter Low-Power Quiet mode 0: Transmitter not in quiet mode 1: Transmitter is in quiet mode	0x0
TX_LPI_MODE	0	R/O	Transmitter Low-Power Idle mode 0: Transmitter not in low power idle mode 1: Transmitter is in low power idle mode	0x0

1.2.4 DEV:PCS1G_TSTPAT_CFG_STATUS

Parent: DEV

Instances: 1

PCS1G testpattern configuration and status register set

TABLE 1-112: REGISTERS IN PCS1G_TSTPAT_CFG_STATUS

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PCS1G_TSTPAT_MODE_CFG	0x00000000	1	PCS1G TSTPAT MODE CFG	Page 57
PCS1G_TSTPAT_STATUS	0x00000004	1	PCS1G TSTPAT STATUS	Page 57

1.2.4.1 DEV:PCS1G_TSTPAT_CFG_STATUS:PCS1G_TSTPAT_MODE_CFG

Parent: DEV:PCS1G_TSTPAT_CFG_STATUS

Instances: 1

PCS1G testpattern mode configuration register (Frame based pattern 4 and 5 might be not available depending on chip type)

TABLE 1-113: FIELDS IN PCS1G_TSTPAT_MODE_CFG

Field Name	Bit	Access	Description	Default
JTP_SEL	2:0	R/W	Jitter Test Pattern Select: Enables and selects the jitter test pattern to be transmitted. The jitter test patterns are according to the IEEE 802.3, Annex 36A 0: Disable transmission of test patterns 1: High frequency test pattern - repeated transmission of D21.5 code group 2: Low frequency test pattern - repeated transmission of K28.7 code group 3: Mixed frequency test pattern - repeated transmission of K28.5 code group 4: Long continuous random test pattern (packet length is 1524 bytes) 5: Short continuous random test pattern (packet length is 360 bytes)	0x0

1.2.4.2 DEV:PCS1G_TSTPAT_CFG_STATUS:PCS1G_TSTPAT_STATUS

Parent: DEV:PCS1G_TSTPAT_CFG_STATUS

Instances: 1

PCS1G testpattern status register

TABLE 1-114: FIELDS IN PCS1G_TSTPAT_STATUS

Field Name	Bit	Access	Description	Default
JTP_ERR_CNT	15:8	R/W	Jitter Test Pattern Error Counter. Due to re-sync measures it might happen that single errors are not counted (applies for 2.5gpbs mode). The counter saturates at 255 and is only cleared when writing 0 to the register	0x00
JTP_ERR	4	R/O	Jitter Test Pattern Error 0: Jitter pattern checker has found no error 1: Jitter pattern checker has found an error	0x0
JTP_LOCK	0	R/O	Jitter Test Pattern Lock 0: Jitter pattern checker has not locked 1: Jitter pattern checker has locked	0x0

1.2.5 DEV:PCS_FX100_CONFIGURATION

Parent: DEV

Instances: 1

Configuration register set for PCS 100Base-FX logic

TABLE 1-115: REGISTERS IN PCS_FX100_CONFIGURATION

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PCS_FX100_CFG	0x00000000	1	PCS 100Base FX Configuration	Page 58

1.2.5.1 DEV:PCS_FX100_CONFIGURATION:PCS_FX100_CFG

Parent: DEV:PCS_FX100_CONFIGURATION

Instances: 1

Configuration bit groups for 100Base-FX PCS

TABLE 1-116: FIELDS IN PCS_FX100_CFG

Field Name	Bit	Access	Description	Default
SD_SEL	26	R/W	Signal detect selection (select input for internal signal_detect line) 0: Select signal_detect line from hardmacro 1: Select external signal_detect line	0x0
SD_POL	25	R/W	Signal detect polarity: The signal level on signal_detect input pin must be equal to SD_POL to indicate signal detection (SD_ENA must be set). Use '1' when SD_-SEL is set to hardmacro. 0: Signal Detect input pin must be '0' to indicate a signal detection 1: Signal Detect input pin must be '1' to indicate a signal detection	0x1

TABLE 1-116: FIELDS IN PCS_FX100_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
SD_ENA	24	R/W	Signal Detect Enable 0: The Signal Detect input pin is ignored. The PCS assumes an active Signal Detect at all times 1: The Signal Detect input pin is used to determine if a signal is detected	0x1
RESERVED	15:12	R/W	Must be set to its default.	0x4
LINKHYSTTIMER	7:4	R/W	Link hysteresis timer configuration. The hysteresis time lasts [linkhysttimer] * 65536 ns + 2320 ns. If linkhysttime is set to 5, the hysteresis lasts the minimum time of 330 us as specified in IEEE 802.3 - 24.3.3.4.	0x5
UNIDIR_MODE_ENA	3	R/W	Unidirectional mode enable. Implementation 0f 802.3 clause 66. When asserted, this enables MAC to transmit data independent of the state of the receive link. 0: Unidirectional mode disabled 1: Unidirectional mode enabled	0x0
FEFCHK_ENA	2	R/W	Far-End Fault (FEF) detection enable 0: Disable FEF detection 1 Enable FEF detection	0x1
FEFGEN_ENA	1	R/W	Far-End Fault (FEF) generation enable 0: Disable FEF generation 1 Enable FEF generation	0x1
PCS_ENA	0	R/W	PCS enable 0: Disable PCS 1: Enable PCS	0x0

1.2.6 DEV:PCS_FX100_STATUS

Parent: DEV

Instances: 1

Status register set for PCS 100Base-FX logic

TABLE 1-117: REGISTERS IN PCS_FX100_STATUS

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PCS_FX100_STATUS	0x00000000	1	PCS 100Base FX Status	Page 59

1.2.6.1 DEV:PCS_FX100_STATUS:PCS_FX100_STATUS

Parent: DEV:PCS_FX100_STATUS

Instances: 1

Status bit groups for 100Base-FX PCS. Note: If sigdet_cfg != "00" is selected status signal "signal_detect" shows the internal signal_detect value is gated with the status of rx toggle-rate control circuitry.

TABLE 1-118: FIELDS IN PCS_FX100_STATUS

Field Name	Bit	Access	Description	Default
EDGE_POS_PTP	11:8	R/O	Data change position in the 10bit words received. Must be used for adjusting PTP ingress delays.	0x0
PCS_ERROR_STICKY	7	Sticky	PCS error has occurred 1: RX_ER was high while RX_DV active 0: No RX_ER indication found while RX_DV active Bit is cleared by writing a 1 to this position.	0x0
FEF_FOUND_STICKY	6	Sticky	Far-end Fault state has occurred 1: A Far-End Fault has been detected 0: No Far-End Fault occurred Bit is cleared by writing a 1 to this position.	0x0
SSD_ERROR_STICKY	5	Sticky	Stream Start Delimiter error occurred 1: A Start-of-Stream Delimiter error has been detected 0: No SSD error occurred Bit is cleared by writing a 1 to this position.	0x0
SYNC_LOST_STICKY	4	Sticky	Synchronization lost 1: Synchronization lost 0: No sync lost occurred Bit is cleared by writing a 1 to this position.	0x0
FEF_STATUS	2	R/O	Current status of Far-end Fault detection state 1: Link currently in fault state 0: Link is in normal state	0x0
SIGNAL_DETECT	1	R/O	Current status of selected signal_detect input line 1: Proper signal detected 0: No proper signal found	0x0
SYNC_STATUS	0	R/O	Status of synchronization 1: Link established 0: No link found	0x0

1.3 DEVCPU_GCB

TABLE 1-119: REGISTER GROUPS IN DEVCPU_GCB

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
CHIP_REGS	0x00000000	1		Page 61
VCORE_ACCESS	0x00000020	1	Registers for accessing the VCore	Page 62
GPIO	0x00000034	1		Page 65
MIIM	0x0000009C	2 0x00000024		Page 69
MIIM_READ_SCAN	0x000000E4	1		Page 72
MIIM_SLAVE	0x000000EC	1		Page 73

TABLE 1-119: REGISTER GROUPS IN DEVCPU_GCB (CONTINUED)

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
PHY	0x000000F0	1	PHY configuration and status registers	Page 73
SIO_CTRL	0x000000F8	1	Serial IO control configuration	Page 74
FAN_CTRL	0x00000204	1	Fan controller configuration and status	Page 81
MEMITGR	0x00000210	1	Memory integrity monitor	Page 83
VRAP	0x00000228	1	VRAP controller	Page 87

1.3.1 DEVCPU_GCB:CHIP_REGS

Parent: DEVCPU_GCB

Instances: 1

TABLE 1-120: REGISTERS IN CHIP_REGS

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CHIP_ID	0x00000000	1	Chip ID register	Page 61
GPR	0x00000004	1	General purpose register	Page 61
SOFT_RST	0x00000008	1	Reset control register	Page 62
HW_STAT	0x00000010	1	Various status indications	Page 62

1.3.1.1 DEVCPU_GCB:CHIP_REGS:CHIP_ID

Parent: DEVCPU_GCB:CHIP_REGS

Instances: 1

TABLE 1-121: FIELDS IN CHIP_ID

Field Name	Bit	Access	Description	Default
REV_ID	31:28	R/O	Revision ID : Chip revision starting from 0.	0x0
PART_ID	27:12	R/O	Part ID: Part ID for identification of Microsemi Chips, contents of this field is updated when reset is released.	0x7514
MFG_ID	11:1	R/O	Manufacturer ID.	0x074
ONE	0	R/O	Always 1.	0x1

1.3.1.2 DEVCPU_GCB:CHIP_REGS:GPR

Parent: DEVCPU_GCB:CHIP_REGS

Instances: 1

TABLE 1-122: FIELDS IN GPR

Field Name	Bit	Access	Description	Default
GPR	31:0	R/W	General purpose register for software development.	0x00000000

1.3.1.3 DEVCPU_GCB:CHIP_REGS:SOFT_RST

Parent: DEVCPU_GCB:CHIP_REGS

Instances: 1

TABLE 1-123: FIELDS IN SOFT_RST

Field Name	Bit	Access	Description	Default
SOFT_SWC_RST	1	R/W	Set this field to reset the switch core (everything except the SERDES IO and PLL blocks.) This field is automatically cleared by the reset. Note: It is possible for the VCore to protect itself from this soft-reset, for more info see ICPU_CFG::RESET.CORE_RST_PROTECT inside the VCore register space.	0x0
SOFT_CHIP_RST	0	R/W	Set this field to reset the whole chip. This field is automatically cleared by the reset. Note: It is possible for the VCore to protect itself from this soft-reset, for more info see ICPU_CFG::RESET.CORE_RST_PROTECT inside the VCore register space.	0x0

1.3.1.4 DEVCPU_GCB:CHIP_REGS:HW_STAT

Parent: DEVCPU_GCB:CHIP_REGS

Instances: 1

TABLE 1-124: FIELDS IN HW_STAT

Field Name	Bit	Access	Description	Default
PLL0_CONF	3:1	R/O	PLL_CONF strapping value from GPIOs sampled after reset release.	0x0
MEM_FAIL	0	R/O	This field is set if a hardware fail has been detected in any of the memories during startup-initialization of the chip. This field is valid after release of reset.	0x0

1.3.2 DEVCPU_GCB:VCORE_ACCESS

Parent: DEVCPU_GCB

Instances: 1

TABLE 1-125: REGISTERS IN VCORE_ACCESS

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
VA_CTRL	0x00000000	1	Control register for VCore accesses	Page 63
VA_ADDR	0x00000004	1	Address register for VCore accesses	Page 63
VA_DATA	0x00000008	1	Data register for VCore accesses	Page 64

TABLE 1-125: REGISTERS IN VCORE_ACCESS (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
VA_DATA_INCR	0x0000000C	1	Data register for VCore accesses (w. auto increment of address)	Page 65
VA_DATA_INERT	0x00000010	1	Data register for VCore accesses (will not initiate access)	Page 65

1.3.2.1 DEVCPU_GCB:VCORE_ACCESS:VA_CTRL

Parent: DEVCPU_GCB:VCORE_ACCESS

Instances: 1

TABLE 1-126: FIELDS IN VA_CTRL

Field Name	Bit	Access	Description	Default
VA_ERR	3:2	R/O	If the VCore access logic detects an error this field is set based on the nature of the error. This is a read-only field which is cleared by the VCore access logic when a new access is (sucessfully) accepted. 0: No errors detected. 1: SBA not ready when accessed. 2: SBA reported error. 3: DATA or ADDR written during active access.	0x0
VA_BUSY_RD	1	R/O	This field is set to the value of VA_CTRL.VA_BUSY whenever one of the data registers VA_DATA, VA_DATA_INCR, or VA_DATA_INERT is read. By examining this field it is possible to determine if VA_BUSY was set at the time a read from one of these registers was performed.	0x0
VA_BUSY	0	R/O	This field is set by hardware when an access into VCore domain is started, and cleared when the access is done.	0x0

1.3.2.2 DEVCPU_GCB:VCORE_ACCESS:VA_ADDR

Parent: DEVCPU_GCB:VCORE_ACCESS

Instances: 1

TABLE 1-127: FIELDS IN VA_ADDR

Field Name	Bit	Access	Description	Default
VA_ADDR	31:0	R/W	The address to access in the VCore domain, all addresses must be 32-bit alligned (i.e. the two least significant bit must always be 0). When accesses are initiated using the VA_-DATA_INCR register, then this field is autoin-cremented by 4 at the end of the transfer. The memory region of the VCore that maps to switch-core registers may not be accessed by using these registers.	0x00000000

1.3.2.3 DEVCPU_GCB:VCORE_ACCESS:VA_DATA

Parent: DEVCPU_GCB:VCORE_ACCESS

Instances: 1

The VA_DATA, VA_DATA_INCR, and VA_DATA_INERT registers are used for indirect access into the VCore domain. The functionality of the VA_DATA_INCR and VA_DATA_INERT registers are similar to this register - but with minor exceptions. These exceptions are fleshed out in the description of the respective registers.

TABLE 1-128: FIELDS IN VA_DATA

Field Name	Bit	Access	Description	Default
VA_DATA	31:0	R/W	Reading or writing from/to this field initiates accesses into the VCore domain. While an access is ongoing (VA_CTRL.VA_BUSY is set) this field may not be written. It is possi-ble to read this field while an access is ongo-ing, but the data returned will be 0x80000000. When writing to this field; a write into the VCore domain is initiated to the address specified in the VA_ADDR register, with the data that was written to this field. Only 32-bit writes are supported. This field may not be written to until the VA_CTRL.VA_BUSY indi-cates that no accesses is ongoing. When reading from this field; a read from the VCore domain is initiated from the address specified in the VA_ADDR register. Import-ant: The data that is returned from reading this field (and stating an access) is not the result of the newly initiated read, instead the data from the last access is returned. The result of the newly initiated read access will be ready once the VA_CTRL.VA_BUSY field shows that the access is done. Note: When the result of a read-access is read from this field (the second read), a new access will automatically be intiated. This is desirable when reading a series of addresses from VCore domain. If a new access is not desirable, then the result should be read from the VA_DATA_INERT register instead of this field!	0x00000000

1.3.2.4 DEVCPU_GCB:VCORE_ACCESS:VA_DATA_INCR

Parent: DEVCPU_GCB:VCORE_ACCESS

Instances: 1

TABLE 1-129: FIELDS IN VA_DATA_INCR

Field Name	Bit	Access	Description	Default
VA_DATA_INCR	31:0	R/W	This field behaves in the same way as VA_-DATA. Except when an access is initiated by using this field (either read or write); the address register (VA_ADDR) is automatically incremented by 4 at the end of the access, i.e. when VA_CTRL.VA_BUSY is deasserted.	0x00000000

1.3.2.5 DEVCPU_GCB:VCORE_ACCESS:VA_DATA_INERT

Parent: DEVCPU_GCB:VCORE_ACCESS

Instances: 1

TABLE 1-130: FIELDS IN VA_DATA_INERT

Field Name	Bit	Access	Description	Default
VA_DATA_INERT	31:0	R/W	This field behaves in the same way as VA_-DATA. Except accesses (read or write) does not initiate VCore accesses. Writing to this register just overwrites the value currently held by all of the data registers (VA_DATA, VA_DATA_INCR, and VA_DATA_INERT).	0x00000000

1.3.3 DEVCPU_GCB:GPIO

Parent: DEVCPU_GCB

Instances: 1

General Purpose I/O Control configuration and status registers.

Each register in this group contains one field with one bit per GPIO pin. Bit 0 in each field correponds to GPIO0, bit 1 to GPIO1, and so on.

TABLE 1-131: REGISTERS IN GPIO

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
GPIO_OUT_SET	0x00000000	1	GPIO output set	Page 66
GPIO_OUT_CLR	0x00000004	1	GPIO output clear	Page 66
GPIO_OUT	0x00000008	1	GPIO output	Page 66
GPIO_IN	0x0000000C	1	GPIO input	Page 67
GPIO_OE	0x00000010	1	GPIO pin direction	Page 67
GPIO_INTR	0x00000014	1	GPIO interrupt	Page 67
GPIO_INTR_ENA	0x00000018	1	GPIO interrupt enable	Page 67
GPIO_INTR_IDENT	0x0000001C	1	GPIO interrupt identity	Page 67

TABLE 1-131: REGISTERS IN GPIO (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
GPIO_ALT	0x00000020	2 0x00000004	GPIO alternate functions	Page 68
GPIO_SD_MAP	0x00000028	16 0x00000004	GPIO Signal Detect Mapping	Page 68

1.3.3.1 DEVCPU_GCB:GPIO:GPIO_OUT_SET

Parent: DEVCPU_GCB:GPIO

Instances: 1

TABLE 1-132: FIELDS IN GPIO_OUT_SET

Field Name	Bit	Access	Description	Default
G_OUT_SET	21:0	One-shot	Setting a bit in this field will immediately set the corresponding bit in GPIO_OUT.G_OUT. Reading this register always return 0. '0': No change '1': Corresponding bit in GPIO_OUT.G_OUT is set.	0x000000

1.3.3.2 DEVCPU_GCB:GPIO:GPIO_OUT_CLR

Parent: DEVCPU_GCB:GPIO

Instances: 1

TABLE 1-133: FIELDS IN GPIO_OUT_CLR

Field Name	Bit	Access	Description	Default
G_OUT_CLR	21:0	One-shot	Setting a bit in this field will immediately clear the corresponding bit in GPIO_OUT.G_OUT. Reading this register always return 0. '0': No change '1': Corresponding bit in GPIO_OUT.G_OUT is cleared.	0x000000

1.3.3.3 DEVCPU_GCB:GPIO:GPIO_OUT

Parent: DEVCPU_GCB:GPIO

Instances: 1

In a multi-threaded software environment using the registers GPIO_OUT_SET and GPIO_OUT_CLR for modifying GPIO values removes the need for software-locked access.

TABLE 1-134: FIELDS IN GPIO_OUT

Field Name	Bit	Access	Description	Default
G_OUT	21:0	R/W	Controls the value on the GPIO pins enabled for output (via the GPIO_OE register). This field can be modified directly or by using the GPIO_O_SET and GPIO_O_CLR registers.	0x000000

1.3.3.4 DEVCPU_GCB:GPIO:GPIO_IN

Parent: DEVCPU_GCB:GPIO

Instances: 1

TABLE 1-135: FIELDS IN GPIO_IN

Field Name	Bit	Access	Description	Default
G_IN	21:0	R/O	GPIO input register. Reflects the current state of the corresponding GPIO pins.	0x000000

1.3.3.5 DEVCPU_GCB:GPIO:GPIO_OE

Parent: DEVCPU_GCB:GPIO

Instances: 1

TABLE 1-136: FIELDS IN GPIO_OE

Field Name	Bit	Access	Description	Default
G_OE	21:0	R/W	Configures the direction of the GPIO pins. '0': Input '1': Output	0x000000

1.3.3.6 DEVCPU_GCB:GPIO:GPIO_INTR

Parent: DEVCPU_GCB:GPIO

Instances: 1

TABLE 1-137: FIELDS IN GPIO_INTR

Field Name	Bit	Access	Description	Default
G_INTR	21:0	Sticky	Indicates whether a GPIO input has changed since last clear. '0': No change '1': GPIO has changed	0x000000

1.3.3.7 DEVCPU_GCB:GPIO:GPIO_INTR_ENA

Parent: DEVCPU_GCB:GPIO

Instances: 1

TABLE 1-138: FIELDS IN GPIO_INTR_ENA

Field Name	Bit	Access	Description	Default
G_INTR_ENA	21:0	R/W	Enables individual GPIO pins for interrupt.	0x000000

1.3.3.8 DEVCPU_GCB:GPIO:GPIO_INTR_IDENT

Parent: DEVCPU_GCB:GPIO

Instances: 1

TABLE 1-139: FIELDS IN GPIO_INTR_IDENT

Field Name	Bit	Access	Description	Default
G_INTR_IDENT	21:0	R/O	Shows which GPIO sources that are currently interrupting. This field is the result of an AND-operation between the GPIO_INTR and the GPIO_INTR_ENA registers.	0x000000

1.3.3.9 DEVCPU_GCB:GPIO:GPIO_ALT

Parent: DEVCPU_GCB:GPIO

Instances: 2

TABLE 1-140: FIELDS IN GPIO_ALT

Field Name	Bit	Access	Description	Default
G_ALT	21:0	R/W	Configures alternate functions for individual GPIOs. See datasheet for information on possible alternate functions. The LSB of the GPIO encoding is placed in replication 0, MSB is placed in replication 1. For example; to encode Alternate mode 2 for GPIO[n] write DEVCPU_GCB::GPIO_ALT[0][n] = 0, and DEVCPU_GCB::GPIO_ALT[1][n] = 1. Note: This register is only reset by the device's reset input, i.e. it is not affected by soft reset! 00: GPIO mode 01: Alternate mode 1 10: Alternate mode 2 11: Alternate mode 3	0x000000

1.3.3.10 DEVCPU_GCB:GPIO:GPIO_SD_MAP

Parent: DEVCPU_GCB:GPIO

Instances: 16

TABLE 1-141: FIELDS IN GPIO_SD_MAP

Field Name	Bit	Access	Description	Default
G_SD_MAP	5:0	R/W	Set to map a specific GPIO mapped signal detect input to specific front-port index. There is one replication for each GPIO mapped signal detect input. If multiple signal detects are enabled and map to same front-port index, then the higher replication index will take priority. For example to map 3'rd signal detect input asif it was provided by 2'nd SERDES; set DEVCPU_GCB::GPIO_SD_MAP[2].G_SD_MAP = 1 and enable SD2 via DEVCPU_GCB::GPIO_ALT registers.	0x00

1.3.4 DEVCPU_GCB:MIIM

Parent: DEVCPU_GCB

Instances: 2

TABLE 1-142: REGISTERS IN MIIM

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MII_STATUS	0x00000000	1	MIIM Status	Page 69
MII_CMD	0x00000008	1	MIIM Command	Page 70
MII_DATA	0x0000000C	1	MIIM Reply Data	Page 70
MII_CFG	0x00000010	1	MIIM Configuration	Page 71
MII_SCAN_0	0x00000014	1	MIIM Scan 0	Page 71
MII_SCAN_1	0x00000018	1	MIIM Scan 1	Page 71
MII_SCAN_LAST_RSLTS	0x0000001C	1	MIIM Results	Page 72
MII_SCAN_LAST_RSLTS_VLD	0x00000020	1	MIIM Results	Page 72

1.3.4.1 DEVCPU_GCB:MIIM:MII_STATUS

Parent: DEVCPU_GCB:MIIM

Instances: 1

TABLE 1-143: FIELDS IN MII_STATUS

Field Name	Bit	Access	Description	Default
MIIM_SCAN_COMPLETE	4	R/O	Signals if all PHYs have been scanned (with auto scan) at least once. 0 : Auto scan has not scanned all PHYs. 1 : Auto scan has scanned all PHY at least once.	0x0
MIIM_STAT_BUSY	3	R/O	Indicates the current state of the MIIM controller. When read operations are done (no longer busy), then read data is available via the DEVCPU_GCB::MII_DATA register. 0: MIIM controller is in idle state 1: MIIM controller is busy performing MIIM cmd (Either read or read cmd).	0x0
MIIM_STAT_OPR_PEND	2	R/O	The MIIM controller has a CMD fifo of depth one. When this field is 0, then it is safe to write another MIIM command to the MIIM controller. 0 : Read or write not pending 1 : Read or write pending.	0x0
MIIM_STAT_PENDING_RD	1	R/O	Indicates whether a read operation via the MIIM interface is in progress or not. 0 : Read not in progress 1 : Read in progress.	0x0
MIIM_STAT_PENDING_WR	0	R/O	Indicates whether a write operation via the MIIM interface is in progress or not. 0 : Write not in progress 1 : Write in progress.	0x0

1.3.4.2 DEVCPU_GCB:MIIM:MII_CMD

Parent: DEVCPU_GCB:MIIM

Instances: 1

TABLE 1-144: FIELDS IN MII_CMD

Field Name	Bit	Access	Description	Default
MIIM_CMD_VLD	31	One-shot	Must be set for starting a new PHY access. This bit is automatically cleared. 0 : Write to this register is ignored. 1 : Write to this register is processed.	0x0
MIIM_CMD_PHYAD	29:25	R/W	Indicates the addressed PHY number.	0x00
MIIM_CMD_REGAD	24:20	R/W	Indicates the addressed of the register within the PHY that shall be accessed.	0x00
MIIM_CMD_WRDATA	19:4	R/W	Data to be written in the PHY register.	0x0000
MIIM_CMD_SINGLE_SCAN	3	R/W	Select if scanning of the PHY shall be done once, or scanning should be done continuously. 0 : Do continuously PHY scanning 1 : Stop once all PHY have been scanned.	0x0
MIIM_CMD_OPR_FIELD	2:1	R/W	Indicates type of operation. Clause 22: 01 : Write 10 : Read Clause 45: 00 : Address 01 : Write 10 : Read inc. 11 : Read.	0x0
MIIM_CMD_SCAN	0	R/W	Indicates whether automatic scanning of PHY registers is enabled. When enabled, the PHY-number for each automatic read is continuously round-robined from PHY_ADDR_LOW through PHY_ADDR_HIGH. This function is started upon a read operation (ACCESS_TYPE). Scan MUST be disabled when doing any configuration of the MIIM controller. 0 : Disabled 1 : Enabled.	0x0

1.3.4.3 DEVCPU_GCB:MIIM:MII_DATA

Parent: DEVCPU_GCB:MIIM

Instances: 1

TABLE 1-145: FIELDS IN MII_DATA

Field Name	Bit	Access	Description	Default
MIIM_DATA_SUCCESS	17:16	R/O	Indicates whether a read operation failed or succeeded. 00 : OK 11 : Error	0x0
MIIM_DATA_RDDATA	15:0	R/O	Data read from PHY register.	0x0000

1.3.4.4 DEVCPU_GCB:MIIM:MII_CFG

Parent: DEVCPU_GCB:MIIM

Instances: 1

TABLE 1-146: FIELDS IN MII_CFG

Field Name	Bit	Access	Description	Default
MIIM_ST_CFG_FIELD	10:9	R/W	The ST (start-of-frame) field of the MIIM frame format adopts the value of this field. This must be configured for either clause 22 or 45 MIIM operation. "01": Clause 22 "00": Clause 45 Other values are reserved.	0x1
MIIM_CFG_PRESCALE	7:0	R/W	Configures the MIIM clock frequency. This is computed as system_clk/(2*(1+X)), where X is the value written to this register. Note : Setting X to 0 is invalid and will result in the same frequency as setting X to 1. Values less than 4 are reserved and must not be used.	0x32

1.3.4.5 DEVCPU_GCB:MIIM:MII_SCAN_0

Parent: DEVCPU_GCB:MIIM

Instances: 1

TABLE 1-147: FIELDS IN MII_SCAN_0

Field Name	Bit	Access	Description	Default
MIIM_SCAN_PHYADHI	9:5	R/W	Indicates the high PHY number to scan during automatic scanning.	0x00
MIIM_SCAN_PHYADLO	4:0	R/W	Indicates the low PHY number to scan during automatic scanning.	0x00

1.3.4.6 DEVCPU_GCB:MIIM:MII_SCAN_1

Parent: DEVCPU_GCB:MIIM

Instances: 1

TABLE 1-148: FIELDS IN MII_SCAN_1

Field Name	Bit	Access	Description	Default
MIIM_SCAN_MASK	31:16	R/W	Indicates the mask for comparing the PHY registers during automatic scan.	0x0000
MIIM_SCAN_EXPECT	15:0	R/W	Indicates the expected value for comparing the PHY registers during automatic scan.	0x0000

1.3.4.7 DEVCPU_GCB:MIIM:MII_SCAN_LAST_RSLTS

Parent: DEVCPU_GCB:MIIM

Instances: 1

TABLE 1-149: FIELDS IN MII_SCAN_LAST_RSLTS

Field Name	Bit	Access	Description	Default
MIIM_LAST_RSLT	31:0	R/O	Indicates for each PHY if a PHY register has matched the expected value (with mask). This register reflects the value of the last reading of the phy register. 0 : Mismatch. 1 : Match.	0xFFFFFFFF

1.3.4.8 DEVCPU_GCB:MIIM:MII_SCAN_LAST_RSLTS_VLD

Parent: DEVCPU_GCB:MIIM

Instances: 1

TABLE 1-150: FIELDS IN MII_SCAN_LAST_RSLTS_VLD

Field Name	Bit	Access	Description	Default
MIIM_LAST_RSLT_VLD	31:0	R/O	Indicates for each PHY if a PHY register matched are valid or not. 0 : Scan result not valid. 1 : Scan result valid.	0x00000000

1.3.5 DEVCPU_GCB:MIIM_READ_SCAN

Parent: DEVCPU_GCB

Instances: 1

TABLE 1-151: REGISTERS IN MIIM_READ_SCAN

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MII_SCAN_RSLTS_STICKY	0x00000000	2 0x00000004	MIIM Results	Page 72

1.3.5.1 DEVCPU_GCB:MIIM_READ_SCAN:MII_SCAN_RSLTS_STICKY

Parent: DEVCPU_GCB:MIIM_READ_SCAN

Instances: 2

TABLE 1-152: FIELDS IN MII_SCAN_RSLTS_STICKY

Field Name	Bit	Access	Description	Default
MIIM_SCAN_RSLTS_STICKY	31:0	R/O	Indicates for each PHY if a PHY register has had a mismatch of the expected value (with mask) since last reading of MIIM_S-CAN_RSLTS_STICKY. Result is sticky, and result will indicate if there has been a mismatch since the last reading of this register. Upon reading this register, all bits are reset to '1'. 0 : Mismatch 1 : Match.	0xFFFFFFFF

1.3.6 DEVCPU_GCB:MIIM_SLAVE

Parent: DEVCPU_GCB

Instances: 1

TABLE 1-153: REGISTERS IN MIIM_SLAVE

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MIIM_SLAVE_CFG	0x00000000	1	MIIM Configuration	Page 73

1.3.6.1 DEVCPU_GCB:MIIM_SLAVE:MIIM_SLAVE_CFG

Parent: DEVCPU_GCB:MIIM_SLAVE

Instances: 1

TABLE 1-154: FIELDS IN MIIM_SLAVE_CFG

Field Name	Bit	Access	Description	Default
SPIKE_FILTER_CFG	5:1	R/W	Configuration of the spike filter width on the MDC and MDIO inputs. Filters spikes with a width of (SPIKE_FIL-TER_CFG+1)*SYSTEM_CLK or less.	0x00
SPIKE_FILTER_ENA	0	R/W	Set this field to enable the spike filter on the MDC and MDIO inputs. When enabled the MIIM_SLAVE_CFG.SPIKE_FILTER_CFG field determines the width of the spike filter.	0x1

1.3.7 DEVCPU_GCB:PHY

Parent: DEVCPU_GCB

Instances: 1

TABLE 1-155: REGISTERS IN PHY

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_CFG	0x00000000	1	PHY configuration register	Page 74
PHY_STAT	0x00000004	1	PHY status register	Page 74

1.3.7.1 DEVCPU_GCB:PHY:PHY_CFG

Parent: DEVCPU_GCB:PHY

Instances: 1

TABLE 1-156: FIELDS IN PHY_CFG

Field Name	Bit	Access	Description	Default
PHY_RESET	8:5	R/W	Set to 1 to release reset.	0x0
PHY_COMMON_RESET	4	R/W	Set to 1 to release reset.	0x0
PHY_ENA	3:0	R/W	Enable PHY interface for Device 0 to 3	0x0

1.3.7.2 DEVCPU_GCB:PHY:PHY_STAT

Parent: DEVCPU_GCB:PHY

Instances: 1

TABLE 1-157: FIELDS IN PHY_STAT

Field Name	Bit	Access	Description	Default
FAST_LINK_STATUS	20:17	R/O		0x0
LINK_STAT_DUPLEX	16:13	R/O		0x0
LINK_STAT_SPEED_1000	12:9	R/O		0x0
LINK_STAT_SPEED_100	8:5	R/O		0x0
LINK_STAT_SPEED_10	4:1	R/O		0x0
SUPERVISOR_COMPLETE	0	R/O		0x0

1.3.8 DEVCPU_GCB:SIO_CTRL

Parent: DEVCPU_GCB

Instances: 1

TABLE 1-158: REGISTERS IN SIO_CTRL

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SIO_INPUT_DATA	0x00000000	4 0x00000004	Last value at SGPIO pins	Page 75
SIO_CFG	0x00000010	1	General configurations	Page 75
SIO_CLOCK	0x00000014	1	SGPIO shift clock frequency	Page 77

TABLE 1-158: REGISTERS IN SIO_CTRL (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SIO_PORT_CFG	0x00000018	32 0x00000004	Output configuration	Page 77
SIO_PORT_ENA	0x00000098	1	Port enable	Page 78
SIO_PWM_CFG	0x0000009C	3 0x00000004	Pulse-width modulation configuration	Page 78
SIO_INTR_POL	0x000000A8	4 0x00000004	SGPIO interrupt polarity	Page 79
SIO_INTR_RAW	0x000000B8	4 0x00000004	Interrupt raw status	Page 79
SIO_INTR_TRIGGER0	0x000000C8	4 0x00000004	Interrupt trigger mode 0	Page 79
SIO_INTR_TRIGGER1	0x000000D8	4 0x00000004	Interrupt trigger mode 1	Page 80
SIO_INTR	0x000000E8	4 0x00000004	Currently interrupting SGPIOs	Page 80
SIO_INTR_ENA	0x000000F8	1	SGPIO interrupt enable per port	Page 81
SIO_INTR_IDENT	0x000000FC	4 0x00000004	Currently active interrupts	Page 81

1.3.8.1 DEVCPU_GCB:SIO_CTRL:SIO_INPUT_DATA

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 4

TABLE 1-159: FIELDS IN SIO_INPUT_DATA

Field Name	Bit	Access	Description	Default
SIO_INPUT_DATA	31:0	R/O	Serial input data. Each replication, N, holds bit N from all ports - bit N from port M is mapped to replication N bit M. Values of disabled gpios are undefined.	0x00000000

1.3.8.2 DEVCPU_GCB:SIO_CTRL:SIO_CFG

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 1

TABLE 1-160: FIELDS IN SIO_CFG

Field Name	Bit	Access	Description	Default
SIO_PWM_WINDOW	31:24	R/W	Configure the size of the PWM window. 0 : 255 cycles 1-254 : 2-255 cycles 255 : Reserved.	0x00
SIO_REDUCED_GAP	23	R/W	When set, the SIO_BURST_GAP is divided by 32.	0x0

TABLE 1-160: FIELDS IN SIO_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
SIO_BMODE_1	22:21	R/W	Configuration for blink mode 1. Supports three different blink modes and a "burst toggle" mode in which blink mode 1 will alternate for each burst. 0: Blink freq appr. 20Hz 1: Blink freq appr. 10Hz 2: Blink freq appr. 5Hz 3: Burst toggle	0x0
SIO_BMODE_0	20:19	R/W	Configuration of blink mode 0. Supports four different blink modes. 0 : Blink freq appr. 5Hz. 1 : Blink freq appr. 2.5Hz. 2 : Blink freq appr. 1.25Hz. 3 : Blink freq appr. 0.625Hz.	0x0
SIO_BLINK_RESET	18	R/W	Reset the blink counters. Used to synchronize the blink modes between different chips. 0: Blink counter is running 1: Blink counter is reset until sio_blink_reset is unset again	0x0
SIO_BURST_GAP_DIS	17	R/W	Set to disable burst gap.	0x0
SIO_BURST_GAP	16:12	R/W	Configures the length of burst gap in steps of approx. 1.68 ms. Burst gap can be disabled by setting DEVCPU_GCB::SIO_CFG.SIO_BURST_GAP_DIS. For smaller burst gap set DEVCPU_GCB::SIO_CFG.SIO_REDUCED_GAP. The gap is calculated by (Value+1) * (2^18) * (system clock period). 0: 1.68 ms burst gap 1: 3.36 ms burst gap ... 31: 53.69 ms burst gap	0x00
SIO_SINGLE_SHOT	11	One-shot	Use this to output a single burst. Will be cleared by hardware when the burst has finished.	0x0
SIO_AUTO_REPEAT	10	R/W	Use this to output repeated bursts interleaved with burst gaps. Must be manually reset again to stop output of bursts.	0x0
SIO_LD_POLARITY	9	R/W	Polarity of the "Ld" signal 0: load signal is active low 1: load signal is active high	0x0
SIO_PORT_WIDTH	8:7	R/W	Number of SGPIOs pr. port. 0: 1 gpio pr. port 1: 2 gpios pr. port 2: 3 gpios pr. port 3: 4 gpios pr. port	0x0

TABLE 1-160: FIELDS IN SIO_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
SIO_REVERSE_OUTPUT	6	R/W	Reverse the output bitstream. The default order of the output bit stream is (displayed in transmitted order): (portN bit3, portN bit2, ..., port0 bit1, port0 bit0) The reverse order of the output bit stream is (displayed in transmitted order): (port0 bit0, port0 bit1, ..., portN bit2, portN bit3) 0: Do not reverse 1: Reverse	0x0
SIO_REVERSE_INPUT	5	R/W	Reverse the input bitstream. The default order of the input bit stream is (displayed in received order): (port0 bit0, port0 bit1, ..., portN bit2, portN bit3) The reverse order of the input bit stream is (displayed in received order): (portN bit3, portN bit2, ..., port0 bit1, port0 bit0) 0: Do not reverse 1: Reverse	0x0
SIO_GPIO_INTR_ENA	4:1	R/W	Bit interrupt enable. Enables interrupts for the four gpios in a port. Is applied to all ports. 0: Interrupt is disabled for bit n for all ports 1: Interrupt is enabled for bit n for all ports	0x0
SIO_MASTER_INTR_ENA	0	R/W	Master interrupt enable. Enables interrupts. Is applied to all gpios on all ports. This field only has effect on the interrupt output signal of the sio_ctrl block. It has no effect on the interrupt registers. 0: Interrupt is disabled for all bits for all ports 1: Interrupt is enabled for all bits for all ports	0x1

1.3.8.3 DEVCPU_GCB:SIO_CTRL:SIO_CLOCK

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 1

TABLE 1-161: FIELDS IN SIO_CLOCK

Field Name	Bit	Access	Description	Default
SIO_CLK_FREQ	19:8	R/W	SIO controller clock frequency. Divides the 250 MHz system clk with the value of this field. E.g. field is set to 10, the output frequency will be 25 MHz. 0: Disable clock 1: Reserved, do not use Others : Clock divider value.	0x000
SYS_CLK_PERIOD	7:0	R/W	The system clock period given in the clock period in PS divided by 100.	0x40

1.3.8.4 DEVCPU_GCB:SIO_CTRL:SIO_PORT_CFG

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 32

TABLE 1-162: FIELDS IN SIO_PORT_CFG

Field Name	Bit	Access	Description	Default
BIT_SOURCE	23:12	R/W	Output source select for the four outputs from each port.The source select is encoded using three bits for each output bit: Output bit0 is defined by (2 down to 0), output bit1 is defined by (5 down to 3), output bit2 is defined by (8 down to 6), and output bit3 is defined by (11 down to 9). 0: Forced 0 1: Forced 1 2: Blink mode 0 3: Blink mode 1 4: Link activity blink mode 0 5: Link activity blink mode 1 6: Reserved 7: Reserved	0x000
PWM_SOURCE	11:4	R/W	PWM source select for the four outputs from each port.The PWM source select is encoded using two bits for each output bit: Output bit0 is defined by (1 down to 0), output bit1 is defined by (3 down to 2), output bit2 is defined by (5 down to 4), and output bit3 is defined by (7 down to 6). 0: PWM disabled 1: PWM 0 used 2: PWM 1 used 3: PWM 2 used	0x00
BIT_POLARITY	3:0	R/W	Output polarity select for the four outputs from each port.The polarity select is encoded using one bit for each output bit. 0: Normal polarity 1: Inversed polarity	0x0

1.3.8.5 DEVCPU_GCB:SIO_CTRL:SIO_PORT_ENA

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 1

TABLE 1-163: FIELDS IN SIO_PORT_ENA

Field Name	Bit	Access	Description	Default
SIO_PORT_ENA	31:0	R/W	Port enable vector with one enable bit for each port. Port order: (portN down to port0) 0: Port is disabled 1: Port is enabled	0x00000000

1.3.8.6 DEVCPU_GCB:SIO_CTRL:SIO_PWM_CFG

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 3

TABLE 1-164: FIELDS IN SIO_PWM_CFG

Field Name	Bit	Access	Description	Default
PWM_DUTY_CYCLE	7:0	R/W	Define the duty cycle for the PWMs. 0x00: Always "off" 0xFF: Always "on"	0x00

1.3.8.7 DEVCPU_GCB:SIO_CTRL:SIO_INTR_POL

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 4

TABLE 1-165: FIELDS IN SIO_INTR_POL

Field Name	Bit	Access	Description	Default
SIO_INTR_POL	31:0	R/W	Interrupt polarity. This register defines at which logic value an interrupt is generated. For bit0 this register is also used to define the polarity of the "loss of signal" output. 0: interrupt and "loss of signal" is active high 1: interrupt and "loss of signal" is active low	0x00000000

1.3.8.8 DEVCPU_GCB:SIO_CTRL:SIO_INTR_RAW

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 4

TABLE 1-166: FIELDS IN SIO_INTR_RAW

Field Name	Bit	Access	Description	Default
SIO_INTR_RAW	31:0	R/O	Shows the current value of individual interrupts. All interrupts are active high (but has been corrected for polarity as configured in SIO_INTR_POL).	0x00000000

1.3.8.9 DEVCPU_GCB:SIO_CTRL:SIO_INTR_TRIGGER0

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 4

TABLE 1-167: FIELDS IN SIO_INTR_TRIGGER0

Field Name	Bit	Access	Description	Default
SIO_INTR_TRIGGER0	31:0	R/W	Configure trigger mode of individual interrupts. The trigger mode determines how the value of the SIO_INTR_RAW register is transfered to the SIO_INTR register. This register is the LSB of the encoding. Register SIO_INTR_TRIGGER1 is the MSB of the encoding. For level-triggered interrupts SIO_INTR is set when an input is received that results in a high corresponding bit in SIO_INTR_RAW. For edge-triggered interrupts SIO_INTR is set when an input is received that results in a change of the corresponding bit in SIO_INTR_RAW. For falling-edge-triggered interrupts SIO_INTR is set when an input is received that results in a change from '1' to '0' of the corresponding bit in SIO_INTR_RAW. For rising-edge-triggered interrupts SIO_INTR is set when an input is received that results in a change from '0' to '1' of the corresponding bit in SIO_INTR_RAW. 00: Interrupt is level-activated 01: Interrupt is edge-triggered 10: Interrupt is falling-edge-triggered 11: Interrupt is rising-edge-triggered	0x00000000

1.3.8.10 DEVCPU_GCB:SIO_CTRL:SIO_INTR_TRIGGER1

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 4

TABLE 1-168: FIELDS IN SIO_INTR_TRIGGER1

Field Name	Bit	Access	Description	Default
SIO_INTR_TRIGGER1	31:0	R/W	See description of SIO_INTR_TRIGGER0.	0x00000000

1.3.8.11 DEVCPU_GCB:SIO_CTRL:SIO_INTR

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 4

TABLE 1-169: FIELDS IN SIO_INTR

Field Name	Bit	Access	Description	Default
SIO_INTR	31:0	Sticky	Interrupt register. These sticky bits are set when an input is received that are triggered by the corresponding SIO_INTR_TRIGGER configuration. 0: No interrupt for given gpio 1: Interrupt for given gpio	0x00000000

1.3.8.12 DEVCPU_GCB:SIO_CTRL:SIO_INTR_ENA

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 1

TABLE 1-170: FIELDS IN SIO_INTR_ENA

Field Name	Bit	Access	Description	Default
SIO_INTR_ENA	31:0	R/W	Interrupt enable vector with one enable bit for each port. Port order: (portN down to port0) 0: Interrupt is disabled for the port 1: Interrupt is enabled for the port	0x00000000

1.3.8.13 DEVCPU_GCB:SIO_CTRL:SIO_INTR_IDENT

Parent: DEVCPU_GCB:SIO_CTRL

Instances: 4

TABLE 1-171: FIELDS IN SIO_INTR_IDENT

Field Name	Bit	Access	Description	Default
SIO_INTR_IDENT	31:0	R/O	Shows the currently active interrupts. This register is the result of the SIO_INTR interrupts with the disabled interrupts (from SIO_INTR_ENA and SIO_GPIO_INTR_ENA) removed. 0: No active interrupt for given gpio 1: Active interrupt for given gpio	0x00000000

1.3.9 DEVCPU_GCB:FAN_CTRL

Parent: DEVCPU_GCB

Instances: 1

TABLE 1-172: REGISTERS IN FAN_CTRL

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
FAN_CFG	0x00000000	1	Fan controller configuration	Page 82
PWM_FREQ	0x00000004	1	Configuration of the PWM frequency.	Page 82

TABLE 1-172: REGISTERS IN FAN_CTRL (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
FAN_CNT	0x00000008	1	TACH counter	Page 82

1.3.9.1 DEVCPU_GCB:FAN_CTRL:FAN_CFG

Parent: DEVCPU_GCB:FAN_CTRL

Instances: 1

TABLE 1-173: FIELDS IN FAN_CFG

Field Name	Bit	Access	Description	Default
DUTY_CYCLE	23:16	R/W	Define the duty cycle 0x00: Always "off" 0xFF: Always "on"	0x00
CLK_CYCLES_10US	15:4	R/W	The number of system clock cycles that fit in 10 us.	0x61B
INV_POL	3	R/W	Define the polarity of the PWM output. 0: PWM is logic 1 when "on" 1: PWM is logic 0 when "on"	0x0
GATE_ENA	2	R/W	Enable gating of the TACH input by the PWM output so that only TACH pulses received when PWM is "on" are counted. 0: Disabled 1: Enabled	0x0
PWM_OPEN_COL_ENA	1	R/W	Configure the PWM output to be open collector	0x0
FAN_STAT_CFG	0	R/W	Configure behavior of TACH input tick counter, see DEVCPU_GCB::FAN_CNT for more infromation.	0x0

1.3.9.2 DEVCPU_GCB:FAN_CTRL:PWM_FREQ

Parent: DEVCPU_GCB:FAN_CTRL

Instances: 1

TABLE 1-174: FIELDS IN PWM_FREQ

Field Name	Bit	Access	Description	Default
PWM_FREQ	16:0	R/W	Set the frequency of the PWM output. The value of this field must be (System clock frequency)/(PWM frequency)/256.	0x00018

1.3.9.3 DEVCPU_GCB:FAN_CTRL:FAN_CNT

Parent: DEVCPU_GCB:FAN_CTRL

Instances: 1

TABLE 1-175: FIELDS IN FAN_CNT

Field Name	Bit	Access	Description	Default
FAN_CNT	15:0	R/O	Counts the number of TACH input ticks. If DEVCPU_GCB::FAN_CFG.FAN_STAT_CFG is set then this is a wrapping counter that shows the total number of registered TACH ticks. If DEVCPU_GCB::FAN_CFG.FAN_STAT_CFG is cleared then this counter is updated once every second with the number of TACH ticks registered during the last second.	0x0000

1.3.10 DEVCPU_GCB:MEMITGR

Parent: DEVCPU_GCB

Instances: 1

TABLE 1-176: REGISTERS IN MEMITGR

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MEMITGR_CTRL	0x00000000	1	Monitor control	Page 83
MEMITGR_STAT	0x00000004	1	Monitor status	Page 84
MEMITGR_INFO	0x00000008	1	Memory indication	Page 85
MEMITGR_IDX	0x0000000C	1	Memory index	Page 86
MEMITGR_DIV	0x00000010	1	Monitor speed	Page 86

1.3.10.1 DEVCPU_GCB:MEMITGR:MEMITGR_CTRL

Parent: DEVCPU_GCB:MEMITGR

Instances: 1

TABLE 1-177: FIELDS IN MEMITGR_CTRL

Field Name	Bit	Access	Description	Default
ACTIVATE	0	One-shot	Setting this field transitions the integrity monitor between operating modes. Transitioning between modes takes time, this field remains set until the new mode is reached. During this time the monitor also reports busy DEVCPU_GCB::MEMITGR_STAT.MODE_BUSY is set). From IDLE (DEVCPU_GCB::MEMITGR_STAT.MODE_IDLE is set) the monitor can transition into either DETECT or LISTEN mode, the DETECT mode is entered if a memory reports an indication - the LISTEN mode is entered if no indications are reported. The first time after reset the monitor will not detect indications, that is; it will transition directly from IDLE to LISTEN mode. From DETECT (DEVCPU_GCB::MEMITGR_STAT.MODE_DETECT is set) the monitor can transition into either DETECT or LISTEN mode, the DETECT mode is entered if more indications are reported - the LISTEN mode is entered if no more indications are reported. From LISTEN (DEVCPU_GCB::MEMITGR_STAT.MODE_LISTEN is set) the monitor can transition into IDLE mode. Software shall not set this field when the monitor is BUSY (when DEVCPU_GCB::MEMITGR_STAT.MODE_BUSY is set.)	0x0

1.3.10.2 DEVCPU_GCB:MEMITGR:MEMITGR_STAT

Parent: DEVCPU_GCB:MEMITGR

Instances: 1

TABLE 1-178: FIELDS IN MEMITGR_STAT

Field Name	Bit	Access	Description	Default
INDICATION	4	R/O	If this field is set then there is an indication from one of the memories that needs to be analyzed. An indication is either a parity detection or an error correction. This field is only set when the monitor is in LISTEN mode (DEVCPU_GCB::MEMITGR_STAT.MODE_LISTEN is set), in all other states (including BUSY) this field returns 0.	0x0
MODE_LISTEN	3	R/O	This field is set when the monitor is in LISTEN mode, during listen mode the monitor continually check for parity/correction indications from the memories.	0x0

TABLE 1-178: FIELDS IN MEMITGR_STAT (CONTINUED)

Field Name	Bit	Access	Description	Default
MODE_DETECT	2	R/O	This field is set when the monitor is in DETECT mode, during detect mode the DEVCPU_GCB::MEMITGR_INFO and DEVCPU_GCB::MEMITGR_IDX registers contains valid information about one indication.	0x0
MODE_IDLE	1	R/O	This field is set when the monitor is in IDLE mode.	0x1
MODE_BUSY	0	R/O	The busy signal is a copy of the DEVCPU_GCB::MEMITGR_CTRL.ACTIVATE field, see description of that field for more information about the different states/modes of the monitor.	0x0

1.3.10.3 DEVCPU_GCB:MEMITGR:MEMITGR_INFO

Parent: DEVCPU_GCB:MEMITGR

Instances: 1

This field is only valid when the monitor is in the DETECT (DEVCPU_GCB::MEMITGR_STAT.MODE_DETECT is set) mode.

TABLE 1-179: FIELDS IN MEMITGR_INFO

Field Name	Bit	Access	Description	Default
MEM_ERR	31	R/O	This field is set if the monitor has detected a parity indication (or an unrecoverable correction).	0x0
MEM_COR	30	R/O	This field is set if the monitor has detected a correction.	0x0
MEM_ERR_OVF	29	R/O	This field is set if the monitor has detected a parity indication (or an unrecoverable correction) for which the address has not been recorded. If DEVCPU_GCB::MEMITGR_INFO.MEM_ERR is set then there has been more than one indication, then only the address of the newest indication has been kept. If DEVCPU_GCB::MEMITGR_INFO.MEM_ERR is cleared then an indication has occurred for which the address could not be stored, this is a very rare situation that can only happen if an indication is detected just as the memory is talking to the monitor.	0x0

TABLE 1-179: FIELDS IN MEMITGR_INFO (CONTINUED)

Field Name	Bit	Access	Description	Default
MEM_COR_OVF	28	R/O	This field is set if the monitor has correction indication for which the address has not been recorded. If DEVCPU_GCB::MEMITGR_INFO.MEM_ERR is set then there has also been a parity indication (or an unrecoverable correction) which takes priority over correction indications. If DEVCPU_GCB::MEMITGR_INFO.MEM_ERR is cleared and DEVCPU_GCB::MEMITGR_INFO.MEM_COR is set then there has been more than one correction indication, then only the address of the newest correction indication has been kept. If DEVCPU_GCB::MEMITGR_INFO.MEM_ERR and DEVCPU_GCB::MEMITGR_INFO.MEM_COR is both cleared then a correction indication has occurred for which the address could not be stored, this is a very rare situation that can only happen if an indication is detected just as the memory is talking to the monitor.	0x0
MEM_ADDR	27:0	R/O	This field is valid only when DEVCPU_GCB::MEMITGR_INFO.MEM_ERR or DEVCPU_GCB::MEMITGR_INFO.MEM_COR is set.	0x0000000

1.3.10.4 DEVCPU_GCB:MEMITGR:MEMITGR_IDX

Parent: DEVCPU_GCB:MEMITGR

Instances: 1

This field is only valid when the monitor is in the DETECT (DEVCPU_GCB::MEMITGR_STAT.MODE_DETECT is set) mode.

TABLE 1-180: FIELDS IN MEMITGR_IDX

Field Name	Bit	Access	Description	Default
MEM_IDX	15:0	R/O	This field contains a unique index for the memory for which info is currently provided in DEVCPU_GCB::MEMITGR_INFO. Indexes are counted from 1 (not 0).	0x0000

1.3.10.5 DEVCPU_GCB:MEMITGR:MEMITGR_DIV

Parent: DEVCPU_GCB:MEMITGR

Instances: 1

TABLE 1-181: FIELDS IN MEMITGR_DIV

Field Name	Bit	Access	Description	Default
MEM_DIV	15:0	R/W	Configure divider for generating the sync-pulse to memories (controls the speed at which the monitor talks to the memories). The lower this is set the faster indications can be read out of the memories. See datasheet for appropriate value.	0x00FF

1.3.11 DEVCPU_GCB:VRAP

Parent: DEVCPU_GCB

Instances: 1

TABLE 1-182: REGISTERS IN VRAP

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
VRAP_ACCESS_STAT	0x00000000	1	VRAP events	Page 87

1.3.11.1 DEVCPU_GCB:VRAP:VRAP_ACCESS_STAT

Parent: DEVCPU_GCB:VRAP

Instances: 1

TABLE 1-183: FIELDS IN VRAP_ACCESS_STAT

Field Name	Bit	Access	Description	Default
FRM_RECV_STICKY	3	Sticky	This field is set if a valid VRAP frame has been received.	0x0
CMD_INVALID_STICKY	2	Sticky	This field is set if an invalid command inside a valid VRAP frame has been received. The VRAP engine has ignored the command.	0x0
FRM_INVALID_STICKY	1	Sticky	This field is set if an invalid VRAP frame has been received and discarded by the VRAP-engine. Frames with a VRAP header different from V1 are considered invalid.	0x0
REPLY_ABORT_STICKY	0	Sticky	This field is set if a VRAP reply frame has been aborted. This my happen if a protocol violation is detected during VRAP request frame processing.	0x0

1.4 DEVCPU_ORG

TABLE 1-184: REGISTER GROUPS IN DEVCPU_ORG

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
DEVCPU_ORG	0x00000000	1	Origin registers	Page 88

1.4.1 DEVCPU_ORG:DEVCPU_ORG

Parent: DEVCPU_ORG

Instances: 1

TABLE 1-185: REGISTERS IN DEVCPU_ORG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
IF_CTRL	0x00000000	1	Physical interface control	Page 88
IF_CFGSTAT	0x00000004	1	Physical interface configuration and status	Page 89
ORG_CFG	0x00000008	1	Origin configuration	Page 89
ERR_CNTS	0x0000000C	1	Error counters	Page 90
TIMEOUT_CFG	0x00000010	1	Timeout configuration	Page 90
GPR	0x00000014	1	General purpose register	Page 91
MAILBOX_SET	0x00000018	1	Atomic set of mailbox	Page 91
MAILBOX_CLR	0x0000001C	1	Atomic clear of mailbox	Page 91
MAILBOX	0x00000020	1	Mailbox	Page 92
SEMA_CFG	0x00000024	1	Semaphore configuration	Page 92
SEMA0	0x00000028	1	Semaphore 0	Page 92
SEMA0_OWNER	0x0000002C	1	Semaphore 0 owner	Page 93
SEMA1	0x00000030	1	Semaphore 1	Page 93
SEMA1_OWNER	0x00000034	1	Semaphore 1 owner	Page 93

1.4.1.1 DEVCPU_ORG:DEVCPU_ORG:IF_CTRL

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

TABLE 1-186: FIELDS IN IF_CTRL

Field Name	Bit	Access	Description	Default
IF_CTRL	3:0	R/W	This register configures critical interface parameters, it is constructed so that it can always be written correctly no matter the current state of the interface. When initializing a physical interface, then this is the first register that must be written, the state of the interface at that point may be unknown and therefore the following scheme is required to bring the interface to a known state: When writing a 4-bit value to this field construct a 32-bit data-word as follows: a) copy the 4-bit value into bits 3:0, 11:8, 19:16, and 27:24. b) reverse the 4-bit value and copy into bits 7:4, 15:12, 23:20, and 31:28. Example: To write the value 2 to this field; the 32-bit data-word to write is "0x42424242". Bit 0 configures endianness (when applicable), 0:Little-Endian, 1:Big-Endian. Bit 1 configures bit-order (when applicable), 0:MSB-first, 1:LSB-first. Bit 2,3 are reserved and should be kept 0. For the SI interface the default value of this field is 0x1. For all other interfaces the default value is 0x0.	0x0

1.4.1.2 DEVCPU_ORG:DEVCPU_ORG:IF_CFGSTAT

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

TABLE 1-187: FIELDS IN IF_CFGSTAT

Field Name	Bit	Access	Description	Default
IF_NUM	31:24	R/O	Interface number; software can use this field to determine which interface that is currently used for accessing the device. 0: VCore System 1: VRAP 2: SI 3: MIIM	0x00
IF_STAT	16	Sticky	SI interface: This field is set if the SI interface has read data from device before it was ready (this can happen if the SI frequency is too high or when too few padding bytes has been specified).	0x0
IF_CFG	3:0	R/W	SI interface: This is the number of padding bytes to insert before read-data is shifted out of the device.This is needed when using high serial interface frequencies.	0x0

1.4.1.3 DEVCPU_ORG:DEVCPU_ORG:ORG_CFG

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

TABLE 1-188: FIELDS IN ORG_CFG

Field Name	Bit	Access	Description	Default
FAST_WR	0	R/W	Clear this field to make write accesses return status. By default write operations return status OK because they are finished before status of the access is known. All non-OK responses will be logged in DEVCPU_ORG::ERR_CNTS no matter the value of this field.	0x1

1.4.1.4 DEVCPU_ORG:DEVCPU_ORG:ERR_CNTS

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

TABLE 1-189: FIELDS IN ERR_CNTS

Field Name	Bit	Access	Description	Default
ERR_TGT_BUSY	19:16	R/W	The "Target Busy" indication is triggered when an interface tries to access a target which is currently reset or if another interface is using the target.	0x0
ERR_WD_DROP_ORG	15:12	R/W	The "Watch Dog Drop Origin" indication is triggered when the origin does not receive reply from the CSR ring within a given amount of time. This cannot happen during normal operation.	0x0
ERR_WD_DROP	11:8	R/W	The "Watch Dog Drop" indication is triggered when a target is too long about processing a request. Usually requests are processed immediately but some accesses requires interaction with the core-logic, when this logic is in reset or during very heavy traffic load there is a chance of timing out in the target.	0x0
ERR_NO_ACTION	7:4	R/W	The "No Action" indication is triggered when a target is accessed with a non-existing address. In other words, the target did not contain a register at the requested address.	0x0
ERR_UTM	3:0	R/W	The "Unknown Target Module" indication is triggered when a non-existing target is requested. In other words there was no target with the requested target-id.	0x0

1.4.1.5 DEVCPU_ORG:DEVCPU_ORG:TIMEOUT_CFG

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

This register is shared between all interfaces on the Origin.

TABLE 1-190: FIELDS IN TIMEOUT_CFG

Field Name	Bit	Access	Description	Default
TIMEOUT_CFG	11:0	R/W	The contents of this field controls the timeout delay for the CSR system. Setting this field to 0 disables timeout. Timeout is handled as follows: A counter that decrements continually, when reaching 0 it will wrap to the value specified by this field. When a target has been processing a request for three "wraps" the target time-out and generate a WD_-DROP indication. In the origin an Interface that has been processing a request for four "wraps" will time out and generate a WD_-DROP_ORG indication.	0xFFF

1.4.1.6 DEVCPU_ORG:DEVCPU_ORG:GPR

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

This register is shared between all interfaces on the Origin.

TABLE 1-191: FIELDS IN GPR

Field Name	Bit	Access	Description	Default
GPR	31:0	R/W	General purpose 32-bit registers for debug and software development. The contents of this register can always (safely) be read. However write operations from different masters (to this register), which occur at (exactly) the same time, will fail.	0x00000000

1.4.1.7 DEVCPU_ORG:DEVCPU_ORG:MAILBOX_SET

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

TABLE 1-192: FIELDS IN MAILBOX_SET

Field Name	Bit	Access	Description	Default
MAILBOX_SET	31:0	One-shot	Set bits in this register to atomically set corresponding bits in the DEVCPU_ORG::MAILBOX register. This register return 0 on read.	0x00000000

1.4.1.8 DEVCPU_ORG:DEVCPU_ORG:MAILBOX_CLR

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

TABLE 1-193: FIELDS IN MAILBOX_CLR

Field Name	Bit	Access	Description	Default
MAILBOX_CLR	31:0	One-shot	Set bits in this register to atomically clear corresponding bits in the DEVCPU_ORG::MAILBOX register. This register return 0 on read.	0x00000000

1.4.1.9 DEVCPU_ORG:DEVCPU_ORG:MAILBOX

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

This register is shared between all interfaces on the Origin.

TABLE 1-194: FIELDS IN MAILBOX

Field Name	Bit	Access	Description	Default
MAILBOX	31:0	R/W	Mailbox register which is shared between all interfaces on the Origin. Atomic (safe) modifications to the contents of this register can be performed by using the DEVCPU_ORG::MAILBOX_CLR and DEVCPU_ORG::MAILBOX_SET registers.	0x00000000

1.4.1.10 DEVCPU_ORG:DEVCPU_ORG:SEMA_CFG

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

This register is shared between all interfaces on the Origin.

TABLE 1-195: FIELDS IN SEMA_CFG

Field Name	Bit	Access	Description	Default
SEMA_INTR_POL	1:0	R/W	By default semaphore-interrupt is generated when a semaphore is free. By setting this field interrupt is generated when semaphore is taken, bit 0 corresponds to semaphore 0, bit 1 to semaphore 1. 0: Interrupt on taken semaphore 1: Interrupt on free semaphore	0x0

1.4.1.11 DEVCPU_ORG:DEVCPU_ORG:SEMA0

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

TABLE 1-196: FIELDS IN SEMA0

Field Name	Bit	Access	Description	Default
SEMA0	0	R/W	General Semaphore.The first interface to read this field will be granted the semaphore (reading this field returns 0x1). Once the semaphore has been granted, all reads return '0' from this field (until the semaphore has been released). Any interface can release the semaphore by writing (any value) to this field. 0: Semaphore ownership denied. 1: Semaphore has been granted.	0x1

1.4.1.12 DEVCPU_ORG:DEVCPU_ORG:SEMA0_OWNER

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

TABLE 1-197: FIELDS IN SEMA0_OWNER

Field Name	Bit	Access	Description	Default
SEMA0_OWNER	31:0	R/O	Current owner of the semaphore. This field is a one-hot encoded vector, each bit in this vector correspond to an interface on the origin. If this field return 0, then the semaphore was free at the time of reading the register. 0: Semaphore is free. 1: VCore System owns semaphore 2: VRAP owns semaphore 4: SI owns smaphore 8: MIIM owns semaphore	0x00000000

1.4.1.13 DEVCPU_ORG:DEVCPU_ORG:SEMA1

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

TABLE 1-198: FIELDS IN SEMA1

Field Name	Bit	Access	Description	Default
SEMA1	0	R/W	General Semaphore.The first interface to read this field will be granted the semaphore (reading this field returns 0x1). Once the semaphore has been granted, all reads return '0' from this field (until the semaphore has been released). Any interface can release the semaphore by writing (any value) to this field. 0: Semaphore ownership denied. 1: Semaphore has been granted.	0x1

1.4.1.14 DEVCPU_ORG:DEVCPU_ORG:SEMA1_OWNER

Parent: DEVCPU_ORG:DEVCPU_ORG

Instances: 1

TABLE 1-199: FIELDS IN SEMA1_OWNER

Field Name	Bit	Access	Description	Default
SEMA1_OWNER	31:0	R/O	Current owner of the semaphore. This field is a one-hot encoded vector, each bit in this vector correspond to an interface on the origin. If this field return 0, then the semaphore was free at the time of reading the register. 0: Semaphore is free. 1: VCore System owns semaphore 2: VRAP owns semaphore 4: SI owns smaphore 8: MIIM owns semaphore	0x00000000

1.5 DEVCPU_PTP

TABLE 1-200: REGISTER GROUPS IN DEVCPU_PTP

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
PTP_CFG	0x000000A0	1	PTP controller configuration and status	Page 94
PTP_STATUS	0x000000BC	1	Status of PTP timers	Page 96
PTP_PINS	0x00000000	5 0x00000020	Timing synchronization	Page 98

1.5.1 DEVCPU_PTP:PTP_CFG

Parent: DEVCPU_PTP

Instances: 1

TABLE 1-201: REGISTERS IN PTP_CFG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PTP_MISC_CFG	0x00000000	1	Misc PTP configurations	Page 94
CLK_ADJ_CFG	0x00000004	1	Generated clock adjustment configuration	Page 95
CLK_ADJ_FRQ	0x00000008	1	Generated clock frequency adjustment	Page 95
PTP_PIN_INTR	0x0000000C	1	Pending interrupt mask	Page 96
PTP_PIN_INTR_ENA	0x00000010	1	Enable interrupts per pin	Page 96
PTP_INTR_IDENT	0x00000014	1	Current interrupt status	Page 96
PTP_SYS_CLK_CFG	0x00000018	1	System clock configuration	Page 96

1.5.1.1 DEVCPU_PTP:PTP_CFG:PTP_MISC_CFG

Parent: DEVCPU_PTP:PTP_CFG

Instances: 1

TABLE 1-202: FIELDS IN PTP_MISC_CFG

Field Name	Bit	Access	Description	Default
PTP_ENA	2	R/W	Enable master counter. 0: Master counter disabled and reset 1: Master counter enabled	0x0
PTP_HOLD	1	R/W	Hold master counter. 0: Master counter counts if enabled 1: Master counter will stay at the reached value	0x0
PTP_TOD_FREEZE	0	R/W	The PTP_CUR timers will be frozen when this field is set for a domain, in order to return concurrent values.	0x0

1.5.1.2 DEVCPU_PTP:PTP_CFG:CLK_ADJ_CFG

Parent: DEVCPU_PTP:PTP_CFG

Instances: 1

One replication exsists per time domain

TABLE 1-203: FIELDS IN CLK_ADJ_CFG

Field Name	Bit	Access	Description	Default
CLK_ADJ_DIR	1	R/W	Clock frequency adjustment direction. 0: Positive adjustment. Every adjustment adds 1ns to the counter. => clock period is decreased, clock frequency is increased 1: Negative adjustment. Every adjustment subtracts 1ns from the counter. => clock period is increased, clock frequency is decreased	0x0
CLK_ADJ_ENA	0	R/W	Clock frequency adjust enable. 0: Adjustment Disabled 1: Adjustment Enabled	0x0

1.5.1.3 DEVCPU_PTP:PTP_CFG:CLK_ADJ_FRQ

Parent: DEVCPU_PTP:PTP_CFG

Instances: 1

Adjust master timer acording to detected PPB error. Ex: 1PBB: Adjust every 1ns. 50.006PBB: Adjust every 19.997.600ps

TABLE 1-204: FIELDS IN CLK_ADJ_FRQ

Field Name	Bit	Access	Description	Default
CLK_ADJ_UNIT	30	R/W	Clock frequency adjust unit./ 0: Adjustment made every CLK_ADJ pico-seconds. 1: Adjustment made every CLK_ADJ nano-seconds.	0x0
CLK_ADJ	29:0	R/W	Clock frequency adjust./ N: Number of unadjusted CLK_ADJ_UNIT after which the counter for the clock must be adjusted.	0x00000000

1.5.1.4 DEVCPU_PTP:PTP_CFG:PTP_PIN_INTR

Parent: DEVCPU_PTP:PTP_CFG

Instances: 1

TABLE 1-205: FIELDS IN PTP_PIN_INTR

Field Name	Bit	Access	Description	Default
INTR_PTP	4:0	Sticky	One bit per pin set when an active edge is seen.	0x00

1.5.1.5 DEVCPU_PTP:PTP_CFG:PTP_PIN_INTR_ENA

Parent: DEVCPU_PTP:PTP_CFG

Instances: 1

TABLE 1-206: FIELDS IN PTP_PIN_INTR_ENA

Field Name	Bit	Access	Description	Default
INTR_PTP_ENA	4:0	R/W	Enable interrupt per ptp pin.	0x00

1.5.1.6 DEVCPU_PTP:PTP_CFG:PTP_INTR_IDENT

Parent: DEVCPU_PTP:PTP_CFG

Instances: 1

TABLE 1-207: FIELDS IN PTP_INTR_IDENT

Field Name	Bit	Access	Description	Default
INTR_PTP_IDENT	4:0	R/O	Bit n will be high if an interrupt is currently pending for pin <n>.	0x00

1.5.1.7 DEVCPU_PTP:PTP_CFG:PTP_SYS_CLK_CFG

Parent: DEVCPU_PTP:PTP_CFG

Instances: 1

TABLE 1-208: FIELDS IN PTP_SYS_CLK_CFG

Field Name	Bit	Access	Description	Default
PTP_SYS_CLK_PER_NS	8:4	R/W	Must be configured to running system clock period, rounded down to closest interger nanoseconds value.	0x06
PTP_SYS_CLK_PER_PS100	3:0	R/W	Must be configured to number of 100ps to add on top of the PTP_SYS_CLK_PER_NS value to get to the correct clock period.	0x4

1.5.2 DEVCPU_PTP:PTP_STATUS

Parent: DEVCPU_PTP

Instances: 1

TABLE 1-209: REGISTERS IN PTP_STATUS

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PTP_CUR_NSF	0x00000000	1	Current timestamping value	Page 97
PTP_CUR_NSEC	0x00000004	1	Current time of day	Page 97
PTP_CUR_SEC_LSB	0x00000008	1	Current time of day	Page 97
PTP_CUR_SEC_MSB	0x0000000C	1	Current time of day	Page 97

1.5.2.1 DEVCPU_PTP:PTP_STATUS:PTP_CUR_NSF

Parent: DEVCPU_PTP:PTP_STATUS

Instances: 1

TABLE 1-210: FIELDS IN PTP_CUR_NSF

Field Name	Bit	Access	Description	Default
PTP_CUR_NSF	31:0	R/O	Returns the current value of the timestamping clock. The time of day registers will be latched when this register is read.	0x00000000

1.5.2.2 DEVCPU_PTP:PTP_STATUS:PTP_CUR_NSEC

Parent: DEVCPU_PTP:PTP_STATUS

Instances: 1

Current time of day, nanoseconds part.

TABLE 1-211: FIELDS IN PTP_CUR_NSEC

Field Name	Bit	Access	Description	Default
PTP_CUR_NSEC	29:0	R/O	Time of day naoseconds, latched when NSF was read.	0x00000000

1.5.2.3 DEVCPU_PTP:PTP_STATUS:PTP_CUR_SEC_LSB

Parent: DEVCPU_PTP:PTP_STATUS

Instances: 1

TABLE 1-212: FIELDS IN PTP_CUR_SEC_LSB

Field Name	Bit	Access	Description	Default
PTP_CUR_SEC_LSB	31:0	R/O	Value of current tod secs, latched when NSF was read.	0x00000000

1.5.2.4 DEVCPU_PTP:PTP_STATUS:PTP_CUR_SEC_MSB

Parent: DEVCPU_PTP:PTP_STATUS

Instances: 1

TABLE 1-213: FIELDS IN PTP_CUR_SEC_MSB

Field Name	Bit	Access	Description	Default
PTP_CUR_SEC_MSB	15:0	R/O	Current time of day, seconds part, latched when NSF was read	0x0000

1.5.3 DEVCPU_PTP:PTP_PINS

Parent: DEVCPU_PTP

Instances: 5

TABLE 1-214: REGISTERS IN PTP_PINS

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PTP_PIN_CFG	0x00000000	1	Configuration of use of the register group	Page 98
PTP_TOD_SEC_MSB	0x00000004	1	Time Of Day MSB	Page 99
PTP_TOD_SEC_LSB	0x00000008	1	Time Of Day LSB	Page 99
PTP_TOD_NSEC	0x0000000C	1	Time Of Day nanosecs part	Page 100
PTP_NSF	0x00000010	1	Stamper clock	Page 100
PIN_WF_HIGH_PERIOD	0x00000014	1	Waveform programming	Page 100
PIN_WF_LOW_PERIOD	0x00000018	1	Waveform programming	Page 101

1.5.3.1 DEVCPU_PTP:PTP_PINS:PTP_PIN_CFG

Parent: DEVCPU_PTP:PTP_PINS

Instances: 1

Select use of the ptp i/o pin. Ptp pin 4 is not attached to any physical I/O.

TABLE 1-215: FIELDS IN PTP_PIN_CFG

Field Name	Bit	Access	Description	Default
PTP_PIN_ACTION	5:3	R/W	Defined actions are: IDLE: No operation LOAD: Load TimeOfDay with configured values STORE: Store TimeOfDay and NSF of selected time domain CLOCK: Generate a clock output DELTA: Add PTP_TOD_NSEC field as a signed integer to TimeOfDay When the sync option is set, the action will be done when the pin sees an active edge. The action will automatically return to IDLE when complete. 0: IDLE 1: LOAD 2: STORE 3: CLOCK 4: DELTA 5-7: reserved	0x0
PTP_PIN_SYNC	2	R/W	For LOAD/STORE/DELTA actions, setting this option will suspend the action until an active edge is seen on the pin. Otherwise it will be done immediately. For the CLOCK action, the sync option makes the pin generate a single pulse, <WAFEFORM_LOW> nanoseconds after the time of day has increased the seconds. The pulse will get a width of <WAVE-FORM_HIGH> nanoseconds.	0x0
PTP_PIN_INV_POL	1	R/W	Polarity of the PTP pin. 0: Active high 1: Active low	0x0
PTP_PIN_DOM	0	R/W	Configures the time domain the pin is con-nected to.	0x0

1.5.3.2 DEVCPU_PTP:PTP_PINS:PTP_TOD_SEC_MSB

Parent: DEVCPU_PTP:PTP_PINS

Instances: 1

TABLE 1-216: FIELDS IN PTP_TOD_SEC_MSB

Field Name	Bit	Access	Description	Default
PTP_TOD_SEC_MSB	15:0	R/W	Bits 47:32 of the time-of-day seconds	0x0000

1.5.3.3 DEVCPU_PTP:PTP_PINS:PTP_TOD_SEC_LSB

Parent: DEVCPU_PTP:PTP_PINS

Instances: 1

TABLE 1-217: FIELDS IN PTP_TOD_SEC_LSB

Field Name	Bit	Access	Description	Default
PTP_TOD_SEC_LSB	31:0	R/W	Bits 31:0 of the time-of-day seconds	0x00000000

1.5.3.4 DEVCPU_PTP:PTP_PINS:PTP_TOD_NSEC

Parent: DEVCPU_PTP:PTP_PINS

Instances: 1

TABLE 1-218: FIELDS IN PTP_TOD_NSEC

Field Name	Bit	Access	Description	Default
PTP_TOD_NSEC	29:0	R/W	Time Of Day nanoseconds loaded or stored into TimeOfDay. A synced store operation may return a value between -2 and 999.999.999 in this field. To normalize the complete TOD, in case field is read 0x3ffffffe/f, software must subtract one from the SEC part, and add 1.000.000.000 to the NSEC part.	0x00000000

1.5.3.5 DEVCPU_PTP:PTP_PINS:PTP_NSF

Parent: DEVCPU_PTP:PTP_PINS

Instances: 1

TABLE 1-219: FIELDS IN PTP_NSF

Field Name	Bit	Access	Description	Default
PTP_NSF	31:0	R/O	Value of NSF counter when load/save action was executed. This value will not be loaded into the timers upon a LOAD operation.	0x00000000

1.5.3.6 DEVCPU_PTP:PTP_PINS:PIN_WF_HIGH_PERIOD

Parent: DEVCPU_PTP:PTP_PINS

Instances: 1

TABLE 1-220: FIELDS IN PIN_WF_HIGH_PERIOD

Field Name	Bit	Access	Description	Default
PIN_WFH	29:0	R/W	Configure waveform. Unit is nanoseconds. EX. 25MHz 60/40 clock: PIN_ACTION=CLOCK, PIN_SYNC=0, PIN_WFH=24, PIN_WFL=16 EX. 1 us pulse after 150 ns PIN_ACTION=CLOCK, PIN_SYNC=1, PIN_WFH=1000, PIN_WFL=150	0x00000000

1.5.3.7 DEVCPU_PTP:PTP_PINS:PIN_WF_LOW_PERIOD

Parent: DEVCPU_PTP:PTP_PINS

Instances: 1

TABLE 1-221: FIELDS IN PIN_WF_LOW_PERIOD

Field Name	Bit	Access	Description	Default
PIN_WFL	29:0	R/W	Configure waveform	0x00000000

1.6 DEVCPU_QS

TABLE 1-222: REGISTER GROUPS IN DEVCPU_QS

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
XTR	0x00000000	1	Frame extraction	Page 101
INJ	0x00000024	1	Frame injection	Page 104

1.6.1 DEVCPU_QS:XTR

Parent: DEVCPU_QS

Instances: 1

The DEVCPU_QS::XTR_GRP_CFG, DEVCPU_QS::XTR_RD, and DEVCPU_QS::XTR_FRM_PRUNING registers are replicated once per extraction group. Replication index n corresponds to extraction group number n.

TABLE 1-223: REGISTERS IN XTR

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
XTR_GRP_CFG	0x00000000	2 0x00000004	Extraction group configuration	Page 101
XTR_RD	0x00000008	2 0x00000004	Manual extraction data	Page 102
XTR_FRM_PRUNING	0x00000010	2 0x00000004	Extraction frame pruning	Page 103
XTR_FLUSH	0x00000018	1	Extraction group flush	Page 103
XTR_DATA_PRESENT	0x0000001C	1	Extraction status	Page 104

1.6.1.1 DEVCPU_QS:XTR:XTR_GRP_CFG

Parent: DEVCPU_QS:XTR

Instances: 2

TABLE 1-224: FIELDS IN XTR_GRP_CFG

Field Name	Bit	Access	Description	Default
MODE	3:2	R/W	Configures mode of the extraction group. Each extraction group can be assigned to one of three owners. Note: The VRAP block support only one context, if more than one extraction group is assigned the lowest group-number will be used. 0: VRAP block 1: Manual extraction (via DEVCPU_QS registers) 2: FDMA extraction and manual extraction via SBA registers	0x0
STATUS_WORD_POS	1	R/W	Select order of last data and status words. This field only applies to manual extraction mode (see DEVCPU_QS::XTR_GRP_CFG.MODE). 0: Status just before last data 1: Status just after last data	0x1
BYTE_SWAP	0	R/W	This field allows swapping the endianness of DEVCPU_QS::XTR_RD. Most software will want to read extraction data in network order (big-endian mode), i.e. the first byte of the destiantion MAC address to be placed on byte-address 0 of DEVCPU_QS::XTR_RD. In order to do this a little endian CPU must set this field, a big endian CPU must clear this field. This field only applies to manual extraction mode (see DEVCPU_QS::XTR_GRP_CFG.MODE). 0: Same endianness 1: Swap endianness	0x1

1.6.1.2 DEVCPU_QS:XTR:XTR_RD

Parent: DEVCPU_QS:XTR

Instances: 2

TABLE 1-225: FIELDS IN XTR_RD

Field Name	Bit	Access	Description	Default
DATA	31:0	R/O	Frame Data. Read from this register to obtain the next 32 bits of the frame data currently stored in the CPU queue system. Each read must check for the special values "0x8000000n", 0<=n<=7, as described by the encoding. Note: The encoding is presented in little endian format, if swapping is used (see DEVCPU_QS::XTR_GRP_CFG.BYTE_SWAP), then the special values are swapped as well. I.e. a little endian CPU using BYTE_SWAP=1 has to look for "0x0n000080" instead of "0x8000000n". The position of the unused/valid bytes follows the endianness encoding and swapping. n=0-3: EOF. Unused bytes in end-of-frame word is 'n' n=4 : EOF, but truncated n=5 : EOF Aborted. Frame invalid n=6 : Escape. Next read is packet data n=7 : Data not ready for reading out	0x07000080

1.6.1.3 DEVCPU_QS:XTR:XTR_FRM_PRUNING

Parent: DEVCPU_QS:XTR

Instances: 2

TABLE 1-226: FIELDS IN XTR_FRM_PRUNING

Field Name	Bit	Access	Description	Default
PRUNE_SIZE	7:0	R/W	Extracted frames for the corresponding queue are pruned to (PRUNE_SIZE+1) 32-bit words. Note : PRUNE_SIZE includes the IFH when this present in the frame. 0 : No pruning 1: Frames extracted are pruned to 8 bytes 2: Frames extracted are pruned to 12 bytes ... 255: Frames extracted are pruned to 1024 bytes	0x00

1.6.1.4 DEVCPU_QS:XTR:XTR_FLUSH

Parent: DEVCPU_QS:XTR

Instances: 1

TABLE 1-227: FIELDS IN XTR_FLUSH

Field Name	Bit	Access	Description	Default
FLUSH	1:0	R/W	Enable software flushing of a CPU queue. Note the queue will continue to be flushed until this field is cleared by SW. The flushing will automatically stop on frame boundary so OQS is allowed to transmit to the CPU queue during flushing. 0: No action 1: Do CPU queue flushing	0x0

1.6.1.5 DEVCPU_QS:XTR:XTR_DATA_PRESENT

Parent: DEVCPU_QS:XTR

Instances: 1

TABLE 1-228: FIELDS IN XTR_DATA_PRESENT

Field Name	Bit	Access	Description	Default
DATA_PRESENT	1:0	R/O	Shows if data is available for a specific group. It remains set until all frame data have been extracted. This field is only set if the mode of the group is set to manual extraction via DEVCPU_QS registers. 0: No frames available for this CPU queue group 1: At least one frame is available for this CPU queue group	0x0

1.6.2 DEVCPU_QS:INJ

Parent: DEVCPU_QS

Instances: 1

The DEVCPU_QS::INJ_GRP_CFG, DEVCPU_QS::INJ_WR, DEVCPU_QS::INJ_CTRL, and DEVCPU_QS::INJ_ERR registers are replicated once per injection group. Replication index n corresponds to injection group number n.

TABLE 1-229: REGISTERS IN INJ

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
INJ_GRP_CFG	0x00000000	2 0x00000004	Injection group configuration	Page 104
INJ_WR	0x00000008	2 0x00000004	Manual injection data	Page 105
INJ_CTRL	0x00000010	2 0x00000004	Injection control	Page 105
INJ_STATUS	0x00000018	1	Injection status	Page 106
INJ_ERR	0x0000001C	2 0x00000004	Injection errors	Page 107

1.6.2.1 DEVCPU_QS:INJ:INJ_GRP_CFG

Parent: DEVCPU_QS:INJ

Instances: 2

TABLE 1-230: FIELDS IN INJ_GRP_CFG

Field Name	Bit	Access	Description	Default
MODE	3:2	R/W	Configures mode of the injection group. Each injection group can be assigned to one of three owners. Note: The VRAP block support only one context, if more than one injection group is assigned the lowest group-number will be used. 0: VRAP block 1: Manual injection (via DEVCPU_QS registers) 2: FDMA injection and manual injection via SBA registers	0x0
BYTE_SWAP	0	R/W	This field allows swapping the endianness of the DEVCPU_QS::INJ_WR register. Most software will want to write injection data in network order (big-endian mode), i.e. the first byte of the destiantion MAC address to be placed on byte-address 0 of DEVCPU_QS::INJ_WR. In order to do this a little endian CPU must set this field, a big endian CPU must clear this field. This field only applies to manual extraction mode (see DEVCPU_QS::INJ_GRP_CFG.MODE). 0: Same endianness as CPU 1: Swap endianness	0x1

1.6.2.2 DEVCPU_QS:INJ:INJ_WR

Parent: DEVCPU_QS:INJ

Instances: 2

TABLE 1-231: FIELDS IN INJ_WR

Field Name	Bit	Access	Description	Default
DATA	31:0	R/W	Frame Write. Write to this register inject the next 32 bits of the frame data currently injected into the chip. Reading from this register returns 0.	0x00000000

1.6.2.3 DEVCPU_QS:INJ:INJ_CTRL

Parent: DEVCPU_QS:INJ

Instances: 2

TABLE 1-232: FIELDS IN INJ_CTRL

Field Name	Bit	Access	Description	Default
GAP_SIZE	24:21	R/W	Controls the min-spacing from EOF to SOF on injected frames, the default value emulates the delay of standard preamble/IFG setting on a front-port. Set this field to zero when injecting with IFH.	0x5
ABORT	20	One-shot	Set to abort the current frame.	0x0
EOF	19	One-shot	Set to indicate that the next data written to DEVCPU_Qs::INJ_WR is end-of-frame. At the same time as setting this field, also set DEVCPU_QS::INJ_CTRL.VLD_BYTES to indicate the number of valid data bytes in the end-of-frame word.	0x0
SOF	18	One-shot	Set to indicate that the next data written to DEVCPU_QS::INJ_WR is start-of-frame.	0x0
VLD_BYTES	17:16	R/W	Set to indicate how many bytes of the next data written to DEVCPU_QS::INJ_WR which are valid. This field is only used during end-of-frame words (see DEVCPU_QS::INJ_CTRL.EOF for more information). The position of the valid bytes follows the endianness encoding and swapping. 0: All bytes are valid n: 'n' byte are valid	0x0

1.6.2.4 DEVCPU_QS:INJ:INJ_STATUS

Parent: DEVCPU_QS:INJ

Instances: 1

TABLE 1-233: FIELDS IN INJ_STATUS

Field Name	Bit	Access	Description	Default
WMARK_REACHED	5:4	R/O	Before the CPU injects a frame, software may check if the input queue has reached high watermark. If wathermark in the IQS has been reached this bit will be set. 0: Input queue has not reached high watermark 1: Input queue has reached high watermark, and frames injected may be dropped due to buffer overflow	0x0
FIFO_RDY	3:2	R/O	When '1' the injector group's FIFO is ready for additional data written through the DEVCPU_QS::INJ_WR register. 0: The injector group cannot accept additional data 1: The injector group is able to accept additional data	0x3

TABLE 1-233: FIELDS IN INJ_STATUS (CONTINUED)

Field Name	Bit	Access	Description	Default
INJ_IN_PROGRESS	1:0	R/O	When '1' the injector group is in the process of receiving a frame, and at least one write to INJ_WR remains before the frame is forwarded to the front ports. When '0' the injector group is waiting for an initiation of a frame injection. 0: A frame injection is not in progress 1: A frame injection is in progress	0x0

1.6.2.5 DEVCPU_QS:INJ:INJ_ERR

Parent: DEVCPU_QS:INJ

Instances: 2

TABLE 1-234: FIELDS IN INJ_ERR

Field Name	Bit	Access	Description	Default
ABORT_ERR_STICKY	1	Sticky	Set if a frame has been aborted because of double-SOF injection (missing EOF).	0x0
WR_ERR_STICKY	0	Sticky	Set in case of overflow as a result of not obeying FIFO-ready	0x0

1.7 HSIO

Register Collection for Control of Macros (SERDES1G, SERDES6G, LCPLL)

TABLE 1-235: REGISTER GROUPS IN HSIO

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
PLL5G_CFG	0x00000000	1	PLL5G Configuration Registers	Page 108
PLL5G_STATUS	0x0000001C	1	PLL5G Status Registers	Page 109
RCOMP_STATUS	0x0000003C	1	RCOMP Status Registers	Page 110
SYNC_ETH_CFG	0x00000040	1	SYNC_ETH Configuration Registers	Page 110
SERDES1G_ANA_CFG	0x0000004C	1	SERDES1G Analog Configuration Registers	Page 111
SERDES1G_DIG_CFG	0x00000068	1	SERDES1G Digital Configuration Register	Page 116
SERDES1G_DIG_STATUS	0x00000080	1	SERDES1G Digital Status Register	Page 117
MCB_SERDES1G_CFG	0x00000088	1	MCB SERDES1G Configuration Register	Page 118
SERDES6G_DIG_CFG	0x0000008C	1	SERDES6G Digital Configuration Registers	Page 118
SERDES6G_ANA_CFG	0x000000BC	1	SERDES6G Analog Config-Status Registers	Page 120
SERDES6G_ANA_STATUS	0x000000F4	1	SERDES6G Analog Status Registers	Page 132

TABLE 1-235: REGISTER GROUPS IN HSIO (CONTINUED)

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
MCB_SERDES6G_CFG	0x00000108	1	MCB SERDES6G Configuration Register	Page 134
HW_CFGSTAT	0x0000010C	1	General high-speed IO configuration and status	Page 135
TEMP_SENSOR	0x0000011C	1	Temperature sensor control	Page 138

1.7.1 HSIO:PLL5G_CFG

Parent: HSIO

Instances: 1

Configuration register set for PLL5G.

TABLE 1-236: REGISTERS IN PLL5G_CFG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PLL5G_CFG4	0x00000010	1	PLL5G Configuration 4	Page 108
PLL5G_CFG6	0x00000018	1	PLL5G Configuration 6	Page 108

1.7.1.1 HSIO:PLL5G_CFG:PLL5G_CFG4

Parent: HSIO:PLL5G_CFG

Instances: 1

Configuration register 4 for PLL5G

TABLE 1-237: FIELDS IN PLL5G_CFG4

Field Name	Bit	Access	Description	Default
RESERVED	23:16	R/W	Must be set to its default.	0x08
IB_CTRL	15:0	R/W	settings for reference clock input buffer [1:0]: sel_vref490m [9]: ena_cmv_term [10]: ena_ib (not supported in ES6512) [15:12]: r_adj all other bits reserved	0x7600

1.7.1.2 HSIO:PLL5G_CFG:PLL5G_CFG6

Parent: HSIO:PLL5G_CFG

Instances: 1

Configuration register 6 for PLL5G

TABLE 1-238: FIELDS IN PLL5G_CFG6

Field Name	Bit	Access	Description	Default
REFCLK_SEL_SRC	23	R/W	Set to enable refclk_sel from PLL5G_CFG6.REFCLK_SEL instead of using external input. By default external pins are used for configuring reference clock frequency.	0x0
REFCLK_SEL	22:20	R/W	select ref.clk frequency, 0: 125MHz 1: 156.25MHz 2: 250MHz 3: 312.5MHz 4: 25MHz	0x0
REFCLK_SRC	19	R/W	select internal ref.clk input buffer or external input	0x0
POR_DEL_SEL	17:16	R/W	select POR delay 0: 500us 1: 1ms 2: 4ms 3: 64ms	0x0
RESERVED	15:8	R/W	Must be set to its default.	0x14
RESERVED	7	R/W	Must be set to its default.	0x1
RESERVED	6	R/W	Must be set to its default.	0x1
RESERVED	5:0	R/W	Must be set to its default.	0x0E

1.7.2 HSIO:PLL5G_STATUS

Parent: HSIO

Instances: 1

Status register set for PLL5G.

TABLE 1-239: REGISTERS IN PLL5G_STATUS

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PLL5G_STATUS0	0x00000000	1	PLL5G Status 0	Page 109

1.7.2.1 HSIO:PLL5G_STATUS:PLL5G_STATUS0

Parent: HSIO:PLL5G_STATUS

Instances: 1

Status register 0 for the PLL5G

TABLE 1-240: FIELDS IN PLL5G_STATUS0

Field Name	Bit	Access	Description	Default
RANGE_LIM	12	R/O	RCPLL Flag range limiter signaling	0x0
OUT_OF_RANGE_ERR	11	R/O	RCPLL Flag that indicates a out of range condition while NOT in calibration mode.	0x0
CALIBRATION_ERR	10	R/O	RCPLL Flag that indicates errors that may occur during the calibration procedure.	0x0
CALIBRATION_DONE	9	R/O	RCPLL Flag that indicates that the calibration procedure has finished.	0x0

TABLE 1-240: FIELDS IN PLL5G_STATUS0 (CONTINUED)

Field Name	Bit	Access	Description	Default
READBACK_DATA	8:1	R/O	RCPLL Interface to read back internal data of the FSM.	0x00
LOCK_STATUS	0	R/O	PLL lock status 0: not locked, 1: locked	0x0

1.7.3 HSIO:RCOMP_STATUS

Parent: HSIO

Instances: 1

Status register set for RCOMP.

TABLE 1-241: REGISTERS IN RCOMP_STATUS

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
RCOMP_STATUS	0x00000000	1	RCOMP Status	Page 110

1.7.3.1 HSIO:RCOMP_STATUS:RCOMP_STATUS

Parent: HSIO:RCOMP_STATUS

Instances: 1

Status register bits for the RCOMP

TABLE 1-242: FIELDS IN RCOMP_STATUS

Field Name	Bit	Access	Description	Default
BUSY	12	R/O	Resistor comparison activity 0: resistor measurement finished or inactive 1: resistor measurement in progress	0x0
DELTA_ALERT	7	R/O	Alarm signal if rcomp isn't best choice anymore 0: inactive 1: active	0x0
RCOMP	3:0	R/O	Measured resistor value 0: maximum resistance value 15: minimum resistance value	0x0

1.7.4 HSIO:SYNC_ETH_CFG

Parent: HSIO

Instances: 1

TABLE 1-243: REGISTERS IN SYNC_ETH_CFG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SYNC_ETH_CFG	0x00000000	2 0x00000004	Recovered Clock Configuration	Page 111
SYNC_ETH_PLL_CFG	0x00000008	1	PLL Recovered Clock Configuration	Page 111

1.7.4.1 HSIO:SYNC_ETH_CFG:SYNC_ETH_CFG

Parent: HSIO:SYNC_ETH_CFG

Instances: 2

This register is replicated once per GPIO mapped recovered clock destination.

TABLE 1-244: FIELDS IN SYNC_ETH_CFG

Field Name	Bit	Access	Description	Default
SEL_RCVRD_CLK_SRC	7:4	R/W	Select recovered clock source. 0-1: Select recovered CuPHY clock 0 through 1 2-7: Select SD1G 0 through 5 8-10: Select SD6G 0 through 2 11: Select PLL#0 reference Other values are reserved.	0x0
SEL_RCVRD_CLK_DIV	3:1	R/W	Select recovered clock divider. 0: Divide clock by 2 1: Divide clock by 4 2: Divide clock by 8 3: Divide clock by 16 4: Divide clock by 5 5: Divide clock by 25 6: No clock dividing 7: Reserved	0x0
RCVRD_CLK_ENA	0	R/W	Set to enable recovered clock output. This field only applies to GPIO mapped clock outputs. 0: Disable (high-impedance) 1: Enable (output recovered clock)	0x0

1.7.4.2 HSIO:SYNC_ETH_CFG:SYNC_ETH_PLL_CFG

Parent: HSIO:SYNC_ETH_CFG

Instances: 1

TABLE 1-245: FIELDS IN SYNC_ETH_PLL_CFG

Field Name	Bit	Access	Description	Default
PLL_AUTO_SQUELCH_ENA	0	R/W	Enable auto-squelching for sync. ethernet clock output: when set the clock output will stop toggling (keep its last value constantly) when PLL is out of lock.	0x0

1.7.5 HSIO:SERDES1G_ANA_CFG

Parent: HSIO

Instances: 1

Configuration register set for SERDES1G (analog parts)

TABLE 1-246: REGISTERS IN SERDES1G_ANA_CFG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SERDES1G_DES_CFG	0x00000000	1	SERDES1G Deserializer Cfg	Page 112
SERDES1G_IB_CFG	0x00000004	1	SERDES1G Input Buffer Cfg	Page 113
SERDES1G_OB_CFG	0x00000008	1	SERDES1G Output Buffer Cfg	Page 114
SERDES1G_SER_CFG	0x0000000C	1	SERDES1G Serializer Cfg	Page 115
SERDES1G_COMMON_CFG	0x00000010	1	SERDES1G Common Cfg	Page 115
SERDES1G_PLL_CFG	0x00000014	1	SERDES1G Pll Cfg	Page 116

1.7.5.1 HSIO:SERDES1G_ANA_CFG:SERDES1G_DES_CFG

Parent: HSIO:SERDES1G_ANA_CFG

Instances: 1

Configuration register for SERDES1G deserializer

TABLE 1-247: FIELDS IN SERDES1G_DES_CFG

Field Name	Bit	Access	Description	Default
DES_PHS_CTRL	16:13	R/W	Control of phase regulator logic. Bit 3 must be set to 0. 0: Disabled 1: Enabled with 99 ppm limit 2: Enabled with 202 ppm limit 3: Enabled with 485 ppm limit 4: Enabled if corresponding PCS is in sync with 50 ppm limit 5: Enabled if corresponding PCS is in sync with 99 ppm limit 6: Enabled if corresponding PCS is in sync with 202 ppm limit 7: Enabled if corresponding PCS is in sync with 485 ppm limit	0x6
DES_CPMD_SEL	12:11	R/W	Deserializer phase control, main CP/MD select 0: Directly from DES 1: Through hysteresis stage from DES 2: From core 3: Disabled	0x0
DES_MBTR_CTRL	10:8	R/W	Des phase control for 180 degrees deadlock block mode of operation 0: Depending on density of input pattern 1: Active until PCS has synchronized 2: Depending on density of input pattern until PCS has synchronized 3: Never 4: Always 5-7: Reserved	0x2

TABLE 1-247: FIELDS IN SERDES1G_DES_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
DES_BW_ANA	7:5	R/W	Bandwidth selection for proportional path of CDR loop. 0: No division 1: Divide by 2 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32 6: Divide by 64 7: Divide by 128	0x6
DES_BW_HYST	3:1	R/W	Selection of time constant for integrative path of CDR loop. 0: Divide by 2 1: Divide by 4 2: Divide by 8 3: Divide by 16 4: Divide by 32 5: Divide by 64 6: Divide by 128 7: Divide by 256	0x7

1.7.5.2 HSIO:SERDES1G_ANA_CFG:SERDES1G_IB_CFG

Parent: HSIO:SERDES1G_ANA_CFG

Instances: 1

Configuration register for SERDES1G input buffer

TABLE 1-248: FIELDS IN SERDES1G_IB_CFG

Field Name	Bit	Access	Description	Default
IB_FX100_ENA	27	R/W	Switches signal detect circuit into low frequency mode, must be used in FX100 mode	0x0
RESERVED	26:24	R/W	Must be set to its default.	0x1
IB_DET_LEV	21:19	R/W	Detect thresholds: 0: 159-189mVppd 1: 138-164mVppd 2: 109-124mVppd 3: 74-89mVppd	0x3
IB_HYST_LEV	14	R/W	Input buffer hysteresis levels: 0: 59-79mV 1: 81-124mV	0x0
IB_ENA_CMV_TERM	13	R/W	Enable common mode voltage termination 0: Low termination (VDD_A x 0.7) 1: High termination (VDD_A)	0x1
IB_ENA_DC_COUPLING	12	R/W	Enable dc-coupling of input signal 0: Disable 1: Enable	0x0
IB_ENA_DETLEV	11	R/W	Enable detect level circuit 0: Disable 1: Enable	0x1

TABLE 1-248: FIELDS IN SERDES1G_IB_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
IB_ENA_HYST	10	R/W	Enable hysteresis for input signal. Hysteresis can only be enabled if DC offset compensation is disabled. 0: Disable 1: Enable	0x0
IB_ENA_OFFSET_COMP	9	R/W	Enable offset compensation of input stage. This bit must be disabled to enable hysteresis (IB_ENA_HYST). 0: Disable 1: Enable	0x1
IB_EQ_GAIN	8:6	R/W	Selects weighting between AC and DC input path: 0: Reserved 1: Reserved 2: 0dB (recommended value) 3: 1.5dB 4: 3dB 5: 6dB 6: 9dB 12.5dB	0x2
IB_SEL_CORNER_FREQ	5:4	R/W	Corner frequencies of AC path: 0: 1.3GHz 1: 1.5GHz 2: 1.6GHz 3: 1.8GHz	0x0
RESERVED	3:0	R/W	Must be set to its default.	0xB

1.7.5.3 HSIO:SERDES1G_ANA_CFG:SERDES1G_OB_CFG

Parent: HSIO:SERDES1G_ANA_CFG

Instances: 1

Configuration register for SERDES1G output buffer

TABLE 1-249: FIELDS IN SERDES1G_OB_CFG

Field Name	Bit	Access	Description	Default
OB_SLP	18:17	R/W	Slope / slew rate control: 0: 45ps 1: 85ps 2: 105ps 3: 115ps	0x3
OB_AMP_CTRL	16:13	R/W	Amplitude control in steps of 50mVppd. 0: 0.4Vppd 15: 1.1Vppd	0xC
RESERVED	12:10	R/W	Must be set to its default.	0x2

TABLE 1-249: FIELDS IN SERDES1G_OB_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
OB_VCM_CTRL	7:4	R/W	Common mode voltage control: 0: Reserved 1: 440mV 2: 480mV 3: 460mV 4: 530mV 5: 500mV 6: 570mV 7: 550mV	0x4
RESERVED	3:0	R/W	Must be set to its default.	0x1

1.7.5.4 HSIO:SERDES1G_ANA_CFG:SERDES1G_SER_CFG

Parent: HSIO:SERDES1G_ANA_CFG

Instances: 1

Configuration register for SERDES1G serializer

TABLE 1-250: FIELDS IN SERDES1G_SER_CFG

Field Name	Bit	Access	Description	Default
SER_IDLE	9	R/W	Invert output D0b for idle-mode of OB 0: Non-inverting 1. Inverting	0x0
SER_DEEMPH	8	R/W	Invert and delays (one clk cycle) output D1 for de-emphasis of OB 0: Non-inverting and non-delaying 1: Inverting and delaying	0x0
SER_ENHYS	3	R/W	Enable hysteresis for phase alignment 0: Disable hysteresis 1: Enable hysteresis	0x0
SER_BIG_WIN	2	R/W	Use wider window for phase alignment 0: Use small window for low jitter (100 to 200ps) 1: Use wide window for higher jitter (150 to 300 ps)	0x0
SER_EN_WIN	1	R/W	Enable window for phase alignment 0: Disable window 1: Enable window	0x0
SER_ENALI	0	R/W	Enable phase alignment 0: Disable phase alignment 1: Enable phase alignment	0x0

1.7.5.5 HSIO:SERDES1G_ANA_CFG:SERDES1G_COMMON_CFG

Parent: HSIO:SERDES1G_ANA_CFG

Instances: 1

Configuration register for common SERDES1G functions Note: When enabling the facility loop (ena_floop) also the phase alignment in the serializer has to be enabled and configured adequate.

TABLE 1-251: FIELDS IN SERDES1G_COMMON_CFG

Field Name	Bit	Access	Description	Default
SYS_RST	31	R/W	System reset (low active) 0: Apply reset (not self-clearing) 1: Reset released	0x0
SE_AUTO_SQUELCH_ENA	21	R/W	Enable auto-squelching for sync. ethernet clock output: when set the clock output will stop toggling (keep its last value constantly) when PCS looses link synchrony. 0: Disable 1: Enable	0x0
ENA_LANE	18	R/W	Enable lane 0: Disable lane 1: Enable line	0x0
ENA_ELOOP	11	R/W	Enable equipment loop 0: Disable 1: Enable	0x0
ENA_FLOOP	10	R/W	Enable facility loop 0: Disable 1: Enable	0x0
RESERVED	0	R/W	Must be set to its default.	0x1

1.7.5.6 HSIO:SERDES1G_ANA_CFG:SERDES1G_PLL_CFG

Parent: HSIO:SERDES1G_ANA_CFG

Instances: 1

Configuration register for SERDES1G RCPLL

TABLE 1-252: FIELDS IN SERDES1G_PLL_CFG

Field Name	Bit	Access	Description	Default
RESERVED	21	R/W	Must be set to its default.	0x1
PLL_FSM_CTRL_DATA	15:8	R/W	Control data for FSM	0xC8
PLL_FSM_ENA	7	R/W	Enable FSM	0x0

1.7.6 HSIO:SERDES1G_DIG_CFG

Parent: HSIO

Instances: 1

Configuration register set for SERDES1G digital BIST and DFT functions.

TABLE 1-253: REGISTERS IN SERDES1G_DIG_CFG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SERDES1G_MISC_CFG	0x00000014	1	SERDES1G Misc Configuration	Page 116

1.7.6.1 HSIO:SERDES1G_DIG_CFG:SERDES1G_MISC_CFG

Parent: HSIO:SERDES1G_DIG_CFG

Instances: 1

Configuration register for miscellaneous functions

TABLE 1-254: FIELDS IN SERDES1G_MISC_CFG

Field Name	Bit	Access	Description	Default
DES_100FX_CPMD_ENA	8	R/W	Enable deserializer cp/md handling for 100fx mode 0: Disable 1: Enable	0x0
RX_LPI_MODE_ENA	5	R/W	Enable RX-Low-Power feature (Power control by LPI-FSM in connected PCS) 0: Disable 1: Enable	0x0
TX_LPI_MODE_ENA	4	R/W	Enable TX-Low-Power feature (Power control by LPI-FSM in connected PCS) 0: Disable 1: Enable	0x0
RX_DATA_INV_ENA	3	R/W	Enable data inversion received from Deserializer 0: Disable 1: Enable	0x0
TX_DATA_INV_ENA	2	R/W	Enable data inversion sent to Serializer 0: Disable 1: Enable	0x0
LANE_RST	0	R/W	Lane Reset 0: No reset 1: Reset (not self-clearing)	0x0

1.7.7 HSIO:SERDES1G_DIG_STATUS

Parent: HSIO

Instances: 1

Status register set for SERDES1G digital BIST and DFT functions.

TABLE 1-255: REGISTERS IN SERDES1G_DIG_STATUS

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SERDES1G_DFT_STATUS	0x00000000	1	SERDES1G DFT Status	Page 117

1.7.7.1 HSIO:SERDES1G_DIG_STATUS:SERDES1G_DFT_STATUS

Parent: HSIO:SERDES1G_DIG_STATUS

Instances: 1

Status register of SERDES1G DFT functions

TABLE 1-256: FIELDS IN SERDES1G_DFT_STATUS

Field Name	Bit	Access	Description	Default
BIST_NOSYNC	2	R/O	BIST sync result 0: Synchronization successful 1: Synchronization on BIST data failed	0x0

1.7.8 HSIO:MCB_SERDES1G_CFG

Parent: HSIO

Instances: 1

All SERDES1G macros are accessed via the serial Macro Configuration Bus (MCB). Each macro is configured by one MCB slave. All MCB slaves are connected in a daisy-chain loop.

TABLE 1-257: REGISTERS IN MCB_SERDES1G_CFG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MCB_SERDES1G_ADDR_CFG	0x00000000	1	MCB SERDES1G Address Cfg	Page 118

1.7.8.1 HSIO:MCB_SERDES1G_CFG:MCB_SERDES1G_ADDR_CFG

Parent: HSIO:MCB_SERDES1G_CFG

Instances: 1

Configuration of SERDES1G MCB slaves to be accessed

TABLE 1-258: FIELDS IN MCB_SERDES1G_ADDR_CFG

Field Name	Bit	Access	Description	Default
SERDES1G_WR_ONE_SHOT	31	One-shot	Initiate a write access to marked SERDES1G slaves 0: No write operation pending 1: Initiate write to slaves (kept 1 until write operation has finished)	0x0
SERDES1G_RD_ONE_SHOT	30	One-shot	Initiate a read access to marked SERDES1G slaves 0: No read operation pending (read op finished after bit has been set) 1: Initiate a read access (kept 1 until read operation has finished)	0x0
SERDES1G_ADDR	8:0	R/W	Activation vector for SERDES1G-Slaves, one-hot coded, each bit is related to one macro, e.g. bit 0 enables/disables access to macro no. 0. 0: Disable macro access via MCB 1: Enable macro access via MCB	0x1FF

1.7.9 HSIO:SERDES6G_DIG_CFG

Parent: HSIO

Instances: 1

Configuration register set for SERDES6G digital BIST and DFT functions.

TABLE 1-259: REGISTERS IN SERDES6G_DIG_CFG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SERDES6G_DIG_CFG	0x00000000	1	SERDES6G Digital Configuration register	Page 119

TABLE 1-259: REGISTERS IN SERDES6G_DIG_CFG (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SERDES6G_MISC_CFG	0x0000001C	1	SERDES6G Misc Configuration	Page 119

1.7.9.1 HSIO:SERDES6G_DIG_CFG:SERDES6G_DIG_CFG

Parent: HSIO:SERDES6G_DIG_CFG

Instances: 1

Configuration register for SERDES6G digital functions

TABLE 1-260: FIELDS IN SERDES6G_DIG_CFG

Field Name	Bit	Access	Description	Default
SIGDET_AST	5:3	R/W	Signal detect assertion time 0: 0 us 1: 35 us 2: 70 us 3: 105 us 4: 140 us 5..7: reserved	0x0
SIGDET_DST	2:0	R/W	Signal detect deassertion time 0: 0 us 1: 250 us 2: 350 us 3: 450 us 4: 550 us 5..7: reserved	0x0

1.7.9.2 HSIO:SERDES6G_DIG_CFG:SERDES6G_MISC_CFG

Parent: HSIO:SERDES6G_DIG_CFG

Instances: 1

Configuration register for miscellaneous functions

TABLE 1-261: FIELDS IN SERDES6G_MISC_CFG

Field Name	Bit	Access	Description	Default
SEL_RECO_CLK	14:13	R/W	Select recovered clock divider 0: No clock dividing 1: Divide clock by 5 2: Divide clock by 4 3: Reserved	0x0
DES_100FX_CPMD_ENA	8	R/W	Enable deserializer cp/md handling for 100fx mode 0: Disable 1: Enable	0x0
RX_BUS_FLIP_ENA	7	R/W	Enable flipping rx databus (MSB - LSB)	0x0
TX_BUS_FLIP_ENA	6	R/W	Enable flipping tx databus (MSB - LSB)	0x0

TABLE 1-261: FIELDS IN SERDES6G_MISC_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
RX_LPI_MODE_ENA	5	R/W	Enable RX-Low-Power feature (Power control by LPI-FSM in connected PCS) 0: Disable 1: Enable	0x0
TX_LPI_MODE_ENA	4	R/W	Enable TX-Low-Power feature (Power control by LPI-FSM in connected PCS) 0: Disable 1: Enable	0x0
RX_DATA_INV_ENA	3	R/W	Enable data inversion received from Deserializer 0: Disable 1: Enable	0x0
TX_DATA_INV_ENA	2	R/W	Enable data inversion sent to Serializer 0: Disable 1: Enable	0x0
LANE_RST	0	R/W	Lane Reset 0: No reset 1: Reset (not self-clearing)	0x0

1.7.10 HSIO:SERDES6G_ANA_CFG

Parent: HSIO

Instances: 1

Configuration register set for SERDES6G (analog parts)

TABLE 1-262: REGISTERS IN SERDES6G_ANA_CFG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SERDES6G_DES_CFG	0x00000000	1	SERDES6G Deserializer Cfg	Page 121
SERDES6G_IB_CFG	0x00000004	1	SERDES6G IB Configuration register 0	Page 122
SERDES6G_IB_CFG1	0x00000008	1	SERDES6G IB Configuration register 1	Page 124
SERDES6G_IB_CFG2	0x0000000C	1	SERDES6G IB Configuration register 2	Page 125
SERDES6G_IB_CFG3	0x00000010	1	SERDES6G IB Configuration register 3	Page 126
SERDES6G_IB_CFG4	0x00000014	1	SERDES6G IB Configuration register 4	Page 126
SERDES6G_IB_CFG5	0x00000018	1	SERDES6G IB Configuration register 5	Page 126
SERDES6G_OB_CFG	0x0000001C	1	SERDES6G Output Buffer Cfg 0	Page 127
SERDES6G_OB_CFG1	0x00000020	1	SERDES6G Output Buffer Cfg1	Page 128
SERDES6G_SER_CFG	0x00000024	1	SERDES6G Serializer Cfg	Page 128
SERDES6G_COMMON_CFG	0x00000028	1	SERDES6G Common Cfg	Page 128
SERDES6G_PLL_CFG	0x0000002C	1	SERDES6G Pll Cfg	Page 130
SERDES6G_ACJTAG_CFG	0x00000030	1	SERDES6G ACJTAG Cfg	Page 131

1.7.10.1 HSIO:SERDES6G_ANA_CFG:SERDES6G_DES_CFG

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register for SERDES6G deserializer

TABLE 1-263: FIELDS IN SERDES6G_DES_CFG

Field Name	Bit	Access	Description	Default
DES_PHS_CTRL	16:13	R/W	Control of phase regulator logic (bit 3 selects input to integrator block - 0: cp/md from DES, 1: cp/md from core) 0: Disabled 1: Enabled with 99 ppm limit 2: Enabled with 202 ppm limit 3: Enabled with 485 ppm limit 4: Enabled if corresponding PCS is in sync with 50 ppm limit 5: Enabled if corresponding PCS is in sync with 99 ppm limit 6: Enabled if corresponding PCS is in sync with 202 ppm limit 7: Enabled if corresponding PCS is in sync with 485 ppm limit	0x6
DES_MBTR_CTRL	12:10	R/W	Des phase control for 180 degrees deadlock block mode of operation 000: Depending on density of input pattern 001: Active until PCS has synchronized 010: Depending on density of input pattern until PCS has synchronized 011: Never 100: Always 111: Debug feature: Add cp/md of DES and cp/md from core	0x2
DES_CPMD_SEL	9:8	R/W	DES phase control, main cp/md select 00: Directly from DES 01: Through hysteresis stage from DES 10: From core 11: Disabled	0x0
DES_BW_HYST	7:5	R/W	Bandwidth selection. Selects dividing factor for hysteresis CP/MD outputs. 0: Divide by 2 1: Divide by 4 2: Divide by 8 3: Divide by 16 4: Divide by 32 5: Divide by 64 6: Divide by 128 7: Divide by 256	0x5

TABLE 1-263: FIELDS IN SERDES6G_DES_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
DES_BW_ANA	3:1	R/W	Bandwidth selection. Selects dividing factor for non-hysteresis CP/MD outputs. 0: No division 1: Divide by 2 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32 6: Divide by 64 7: Divide by 128	0x5

1.7.10.2 HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration settings 0

TABLE 1-264: FIELDS IN SERDES6G_IB_CFG

Field Name	Bit	Access	Description	Default
IB_SOFSI	30:29	R/W	Select location of offset correction inside equalizer 0: No offset correction 1: First stage (preferred) 2: Last stage 3: First and last stage	0x1
IB_VBULK_SEL	28	R/W	Controls Bulk Voltage of High Speed Cells 0: Reserved 1: Low (mission mode)	0x1
IB_RTRM_ADJ	27:24	R/W	Resistance adjustment for termination and CML cell regulation. This configuration defines an offset (2-complement) to the RCOMP value. The effective value is limited between 0 to 15. 7: RCOMP+7 1: RCOMP+1 0: RCOMP 15: RCOMP-1 8: RCOMP -8	0xD
IB_ICML_ADJ	23:20	R/W	Current adjustment for CML cells 0: low current 1: high current	0x5
IB_TERM_MODE_SEL	19:18	R/W	Select common mode termination voltage. 0: Open - recommended mission mode for DC-coupling 1: VCM ref - recommended mission mode for AC-coupling 2: VDD - used to increase amplitude in certain DC-coupled modes 3: capacitance only - Reserved for debug test purpose	0x1

TABLE 1-264: FIELDS IN SERDES6G_IB_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
IB_SIG_DET_CLK_SEL	17:15	R/W	Select signal detect clock: Frequency = 125 MHz / 2**n Set to 0 for ATE testing (reduces test-time) Set to 7 for optimized performance in mission mode	0x0
IB_REG_PAT_SEL_HP	14:13	R/W	Selects pattern detection for regulation of high-pass-gain 0: Only regulation assessment if basic pattern is detected 1: Regulation assessment if basic and simplified pattern are detected 2: Regulation assessment if basic and critical pattern are detected 3: Regulation assessment if simplified basic and critical pattern are detected.	0x1
IB_REG_PAT_SEL_MID	12:11	R/W	Selects pattern detection for regulation of mid-pass-gain 0: Only regulation assessment if basic pattern is detected 1: Regulation assessment if basic and simplified pattern are detected 2: Regulation assessment if basic and critical pattern are detected 3: Regulation assessment if simplified basic and critical pattern are detected.	0x1
IB_REG_PAT_SEL_LP	10:9	R/W	Selects pattern detection for regulation of low-pass-gain 0: Only regulation assessment if basic pattern is detected 1: Regulation assessment if basic and simplified pattern are detected 2: Regulation assessment if basic and critical pattern are detected 3: Regulation assessment if simplified basic and critical pattern are detected.	0x2
IB_REG_PAT_SEL_OFFSET	8:7	R/W	Selects pattern detection for regulation of offset 0: Only regulation assessment if basic pattern is detected 1: Regulation assessment if basic and simplified pattern are detected 2: Regulation assessment if basic and critical pattern are detected 3: Regulation assessment if simplified basic and critical pattern are detected.	0x1
IB_ANA_TEST_ENA	6	R/W	Enable analog test output. 0: Disable 1: Enable	0x0
IB_SIG_DET_ENA	5	R/W	Enable signal detection. 0: Disable 1: Enable	0x1

TABLE 1-264: FIELDS IN SERDES6G_IB_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
IB_CONCUR	4	R/W	Selection between constant current and constant resistor mode for CML cells 0: Constant resistor mode 1: Constant current mode	0x1
IB_CAL_ENA	3	R/W	Enable calibration IB calibration should be started after SERDES6G_COMMON_CFG.ENA_LANE was set to '1'. Calibration procedure takes up to 1sec depending on configuration of SERDES6G_IB_CFG.IB_SIG_DET_CLK_SEL. Max.- calibration time is for SERDES6G_IB_CFG.IB_SIG_DET_CLK_SEL set to 7. 0: Disable 1: Enable (mission mode)	0x0
IB_SAM_ENA	2	R/W	Enable SAMpling stage 0: Disable 1: Enable (mission mode)	0x1
IB_EQZ_ENA	1	R/W	Enable EQualiZation-Stage 0: Disable 1: Enable (mission mode)	0x1
IB_REG_ENA	0	R/W	Enable equalizer REGulation stage 0: Disable 1: Enable (mission mode)	0x1

1.7.10.3 HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG1

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration settings 1

TABLE 1-265: FIELDS IN SERDES6G_IB_CFG1

Field Name	Bit	Access	Description	Default
IB_TJTAG	21:17	R/W	Selects threshold voltage for ac-jtag. Voltage = (n + 1) * 20 mV.	0x08
IB_TSDET	16:12	R/W	Selects threshold voltage for signal detect. Voltage = (n + 1) * 20 mV.	0x10
IB_SCALY	11:8	R/W	Selects number of calibration cycles for equalizer, sampling stage, signal-detect and AC-JTAG comparator, BIAS. 0: no calibration --> neutral values are used.	0xF
IB_FILT_HP	7	R/W	Selects doubled filtering of high-pass-gain regulation or set it to hold if ib_frc_hp = 1	0x1
IB_FILT_MID	6	R/W	Selects doubled filtering of mid-pass-gain regulation or set it to hold if ib_frc_mid = 1	0x1
IB_FILT_LP	5	R/W	Selects doubled filtering of low-pass-gain regulation or set it to hold if ib_frc_lp = 1	0x1
IB_FILT_OFFSET	4	R/W	Selects doubled filtering of offset regulation or set it to hold if ib_frc_offset = 1	0x1

TABLE 1-265: FIELDS IN SERDES6G_IB_CFG1 (CONTINUED)

Field Name	Bit	Access	Description	Default
IB_FRC_HP	3	R/W	Selects manual control for high-pass-gain regulation if enabled	0x0
IB_FRC_MID	2	R/W	Selects manual control for mid-pass-gain regulation if enabled	0x0
IB_FRC_LP	1	R/W	Selects manual control for low-pass-gain regulation if enabled	0x0
IB_FRC_OFFSET	0	R/W	Selects manual control for offset regulation if enabled	0x0

1.7.10.4 HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG2

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration settings 2

TABLE 1-266: FIELDS IN SERDES6G_IB_CFG2

Field Name	Bit	Access	Description	Default
IB_TINFV	29:27	R/W	Selects maximum threshold influence for threshold calibration of VScope samplers. 0: 40mV 1: 80mV ...	0x3
IB_OINFI	26:22	R/W	Selects maximum offset influence for offset regulation. 0: 10mV 1: 20mV ...	0x1F
IB_OINFS	18:16	R/W	Selects maximum offset influence for offset calibration of main samplers. 0: 40mV 1: 80mV ...	0x7
IB_OCALS	15:10	R/W	Selects offset voltage for main sampler calibration. 0: -70mV ... 31: -0mV 32: +0mV ... 63: 70mV	0x20
IB_TCALV	9:5	R/W	Selects threshold voltage for VScope sampler calibration. 0: 10mV 1: 20mV ...	0x0C
IB_UMAX	4:3	R/W	Tunes common mode voltage to adapt to max. voltage of input signal. 0: 320mVppd 1: 480mVppd 2: 640mVppd (recommended for mission mode) 3: 800mVppd	0x2

TABLE 1-266: FIELDS IN SERDES6G_IB_CFG2 (CONTINUED)

Field Name	Bit	Access	Description	Default
IB_UREG	2:0	R/W	0dB regulation voltage for high-speed-cells. 0: 160mV 1: 180mV 2: 200mV 3: 220mV 4: 240mV (recommended for mission mode) 5: 260mV 6: 280mV 7: 300mV	0x4

1.7.10.5 HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG3

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration settings 3

TABLE 1-267: FIELDS IN SERDES6G_IB_CFG3

Field Name	Bit	Access	Description	Default
IB_INI_HP	23:18	R/W	Init force value for high-pass gain regulation	0x00
IB_INI_MID	17:12	R/W	Init force value for mid-pass gain regulation	0x1F
IB_INI_LP	11:6	R/W	Init force value for low-pass gain regulation	0x01
IB_INI_OFFSET	5:0	R/W	Init force value for offset gain regulation	0x1F

1.7.10.6 HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG4

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration settings 4

TABLE 1-268: FIELDS IN SERDES6G_IB_CFG4

Field Name	Bit	Access	Description	Default
IB_MAX_HP	23:18	R/W	Max value for high-pass gain regulation	0x3F
IB_MAX_MID	17:12	R/W	Max value for mid-pass gain regulation	0x3F
IB_MAX_LP	11:6	R/W	Max value for low-pass gain regulation	0x02
IB_MAX_OFFSET	5:0	R/W	Max value for offset gain regulation	0x3F

1.7.10.7 HSIO:SERDES6G_ANA_CFG:SERDES6G_IB_CFG5

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration settings 5

TABLE 1-269: FIELDS IN SERDES6G_IB_CFG5

Field Name	Bit	Access	Description	Default
IB_MIN_HP	23:18	R/W	Min value for high-pass gain regulation	0x00
IB_MIN_MID	17:12	R/W	Min value for mid-pass gain regulation	0x00

TABLE 1-269: FIELDS IN SERDES6G_IB_CFG5 (CONTINUED)

Field Name	Bit	Access	Description	Default
IB_MIN_LP	11:6	R/W	Min value for low-pass gain regulation	0x00
IB_MIN_OFFSET	5:0	R/W	Min value for offset gain regulation	0x00

1.7.10.8 HSIO:SERDES6G_ANA_CFG:SERDES6G_OB_CFG

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register 0 for SERDES6G output buffer

TABLE 1-270: FIELDS IN SERDES6G_OB_CFG

Field Name	Bit	Access	Description	Default
OB_IDLE	31	R/W	PCIe support 1: idle - force to 0V differential 0: Normal mode	0x0
OB_ENA1V_MODE	30	R/W	Output buffer supply voltage 1: Set to nominal 1V 0: Set to higher voltage	0x0
OB_POL	29	R/W	Polarity of output signal 0: Normal 1: Inverted	0x1
OB_POST0	28:23	R/W	Coefficients for 1st Post Cursor (MSB is sign)	0x00
OB_PREC	22:18	R/W	Coefficients for Pre Cursor (MSB is sign)	0x00
OB_POST1	15:11	R/W	Coefficients for 2nd Post Cursor (MSB is sign)	0x00
OB_SR_H	8	R/W	Half the predriver speed, use for slew rate control 0: Disable - slew rate < 60 ps 1: Enable - slew rate > 60 ps	0x1
OB_SR	7:4	R/W	Driver speed, fine adjustment of slew rate 30-60ps (if OB_SR_H = 0), 60-140ps (if OB_SR_H = 1). LSB is not used. 000x: ~30ps/60ps ... 111x: ~60ps/140ps	0x7
OB_RESISTOR_CTRL	3:0	R/W	Resistance adjustment for termination and CML cell regulation. This configuration defines an offset (2-complement) to the RCOMP value. The effective value is limited between 0 to 15. 7: RCOMP+7 1: RCOMP+1 0: RCOMP 15: RCOMP-1 8: RCOMP -8	0x1

1.7.10.9 HSIO:SERDES6G_ANA_CFG:SERDES6G_OB_CFG1

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register 1 for SERDES6G output buffer

TABLE 1-271: FIELDS IN SERDES6G_OB_CFG1

Field Name	Bit	Access	Description	Default
OB_ENA_CAS	8:6	R/W	Output skew, used for skew adjustment in SGMII mode - 1bit-hot-coded 000: Non-SGMII/1Gbps modes 001: Lowest skew 010: SGMII/1Gbps mode 100: Highest skew All other settings: Reserved	0x0
OB_LEV	5:0	R/W	Level of output amplitude for 1V mode: max: ~48 for 1.2V mode: max: 63 0: lowest level 63: highest level	0x30

1.7.10.10 HSIO:SERDES6G_ANA_CFG:SERDES6G_SER_CFG

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register for SERDES6G serializer

TABLE 1-272: FIELDS IN SERDES6G_SER_CFG

Field Name	Bit	Access	Description	Default
SER_ALISEL	5:4	R/W	Select reference clock source for phase alignment 00: RXCLKP (for facility loop mode) 01: RefClk15MHz (for XAUI/RXAUI) 10: RXCLKN (debug) 11: ext. ALICLK (debug)	0x0
SER_ENHYS	3	R/W	Enable hysteresis for phase alignment 0: Disable hysteresis 1: Enable hysteresis	0x0
SER_EN_WIN	1	R/W	Enable window for phase alignment 0: Disable window 1: Enable window	0x0
SER_ENALI	0	R/W	Enable phase alignment 0: Disable phase alignment 1: Enable phase alignment (required for MLD-modes - XAUI/RXAUI - and facility loop mode)	0x0

1.7.10.11 HSIO:SERDES6G_ANA_CFG:SERDES6G_COMMON_CFG

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register for common SERDES6G functions

TABLE 1-273: FIELDS IN SERDES6G_COMMON_CFG

Field Name	Bit	Access	Description	Default
SYS_RST	17	R/W	System reset (low active) Should be set after SERDES6G_COMMON_CFG.ENA_LANE was set to 1. 0: Apply reset (not self-clearing) 1: Reset released (mission mode)	0x0
SE_DIV2_ENA	16	R/W	Set to enable local divide-by-2 for sync. ethernet clock output.	0x0
SE_AUTO_SQUELCH_ENA	15	R/W	Enable auto-squelching for sync. ethernet clock output: when set the clock output will stop toggling (keep its last value constantly) when PCS looses link synchrony. 0: Disable 1: Enable	0x0
ENA_LANE	14	R/W	Enable lane 0: Disable lane 1: Enable line	0x0
ENA_ELOOP	7	R/W	Enable equipment loop 0: Disable 1: Enable	0x0
ENA_FLOOP	6	R/W	Enable facility loop SERDES6G_SER_CFG.SER_ENALI must be set to 1 SERDES6G_SER_CFG.SER_ALISEL must be set to 0 0: Disable 1: Enable	0x0
HRATE	3	R/W	Enable half rate Baudrate configuration is controlled by: SERDES6G_PLL_CFG.PLL_DIV4 SERDES6G_PLL_CFG.PLL_ROT_FRQ SERDES6G_PLL_CFG.PLL_ROT_DIR SERDES6G_PLL_CFG.PLL_ENA_ROT SERDES6G_COMMON_CFG.IF_MODE SERDES6G_COMMON_CFG.HRATE SERDES6G_COMMON_CFG.QRATE 0: Disable 1: Enable	0x0

TABLE 1-273: FIELDS IN SERDES6G_COMMON_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
QRATE	2	R/W	Enable quarter rate Baudrate configuration is controlled by: SERDES6G_PLL_CFG.PLL_DIV4 SERDES6G_PLL_CFG.PLL_ROT_FRQ SERDES6G_PLL_CFG.PLL_ROT_DIR SERDES6G_PLL_CFG.PLL_ENA_ROT SERDES6G_COMMON_CFG.IF_MODE SERDES6G_COMMON_CFG.HRATE SERDES6G_COMMON_CFG.QRATE 0: Disable 1: Enable	0x1
IF_MODE	1:0	R/W	Interface mode Baudrate configuration is controlled by: SERDES6G_PLL_CFG.PLL_DIV4 SERDES6G_PLL_CFG.PLL_ROT_FRQ SERDES6G_PLL_CFG.PLL_ROT_DIR SERDES6G_PLL_CFG.PLL_ENA_ROT SERDES6G_COMMON_CFG.IF_MODE SERDES6G_COMMON_CFG.HRATE SERDES6G_COMMON_CFG.QRATE 0: 8-bit mode 1: 10-bit mode 2: 16-bit mode 3: 20-bit mode	0x1

1.7.10.12 HSIO:SERDES6G_ANA_CFG:SERDES6G_PLL_CFG

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register for SERDES6G RCPLL

TABLE 1-274: FIELDS IN SERDES6G_PLL_CFG

Field Name	Bit	Access	Description	Default
PLL_ENA_OFFS	17:16	R/W	Enable offset compensation B1: Feedback path; B0: VCO.	0x3
PLL_DIV4	15	R/W	Enable div4 mode Baudrate configuration is controlled by: SERDES6G_PLL_CFG.PLL_DIV4 SERDES6G_PLL_CFG.PLL_ROT_FRQ SERDES6G_PLL_CFG.PLL_ROT_DIR SERDES6G_PLL_CFG.PLL_ENA_ROT SERDES6G_COMMON_CFG.IF_MODE SERDES6G_COMMON_CFG.HRATE SERDES6G_COMMON_CFG.QRATE	0x0

TABLE 1-274: FIELDS IN SERDES6G_PLL_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
PLL_ENA_ROT	14	R/W	Enable rotation Baudrate configuration is controlled by: SERDES6G_PLL_CFG.PLL_DIV4 SERDES6G_PLL_CFG.PLL_ROT_FRQ SERDES6G_PLL_CFG.PLL_ROT_DIR SERDES6G_PLL_CFG.PLL_ENA_ROT SERDES6G_COMMON_CFG.IF_MODE SERDES6G_COMMON_CFG.HRATE SERDES6G_COMMON_CFG.QRATE	0x0
PLL_FSM_CTRL_DATA	13:6	R/W	Control data for PLL-FSM Encoding below are only examples for some modes. Baudrate configuration is controlled by: SERDES6G_PLL_CFG.PLL_DIV4 SERDES6G_PLL_CFG.PLL_ROT_FRQ SERDES6G_PLL_CFG.PLL_ROT_DIR SERDES6G_PLL_CFG.PLL_ENA_ROT SERDES6G_COMMON_CFG.IF_MODE SERDES6G_COMMON_CFG.HRATE SERDES6G_COMMON_CFG.QRATE 60: SGMII/1G-Modes 48: XAUI/2.5Gbps 96: RXAUI 120: QSGMII	0x3C
PLL_FSM_ENA	5	R/W	Enable FSM	0x0
PLL_ROT_DIR	1	R/W	Select rotation direction Baudrate configuration is controlled by: SERDES6G_PLL_CFG.PLL_DIV4 SERDES6G_PLL_CFG.PLL_ROT_FRQ SERDES6G_PLL_CFG.PLL_ROT_DIR SERDES6G_PLL_CFG.PLL_ENA_ROT SERDES6G_COMMON_CFG.IF_MODE SERDES6G_COMMON_CFG.HRATE SERDES6G_COMMON_CFG.QRATE	0x0
PLL_ROT_FRQ	0	R/W	Select rotation frequency Baudrate configuration is controlled by: SERDES6G_PLL_CFG.PLL_DIV4 SERDES6G_PLL_CFG.PLL_ROT_FRQ SERDES6G_PLL_CFG.PLL_ROT_DIR SERDES6G_PLL_CFG.PLL_ENA_ROT SERDES6G_COMMON_CFG.IF_MODE SERDES6G_COMMON_CFG.HRATE SERDES6G_COMMON_CFG.QRATE	0x0

1.7.10.13 HSIO:SERDES6G_ANA_CFG:SERDES6G_ACJTAG_CFG

Parent: HSIO:SERDES6G_ANA_CFG

Instances: 1

Configuration register for (AC)JTAG debug capability

TABLE 1-275: FIELDS IN SERDES6G_ACJTAG_CFG

Field Name	Bit	Access	Description	Default
ACJTAG_INIT_DATA_N	5	R/W	ACJTAG init data for n leg	0x0
ACJTAG_INIT_DATA_P	4	R/W	ACJTAG init data for p leg	0x0
ACJTAG_INIT_CLK	3	R/W	ACJTAG clock line	0x0
OB_DIRECT	2	R/W	JTAG direct output (directly driven)	0x0
ACJTAG_ENA	1	R/W	ACJTAG enable (ac_mode)	0x0
JTAG_CTRL_ENA	0	R/W	Enable JTAG control via CSR 0: External controlled 1: CSR controlled	0x0

1.7.11 HSIO:SERDES6G_ANA_STATUS

Parent: HSIO

Instances: 1

Status register set for SERDES6G (analog parts)

TABLE 1-276: REGISTERS IN SERDES6G_ANA_STATUS

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SERDES6G_IB_STATUS0	0x00000000	1	SERDES6G IB Status register 0	Page 132
SERDES6G_IB_STATUS1	0x00000004	1	SERDES6G IB Status register 1	Page 133
SERDES6G_ACJTAG_STATUS	0x00000008	1	SERDES6G ACJTAG Status	Page 133
SERDES6G_PLL_STATUS	0x0000000C	1	SERDES6G Pll Status	Page 133
SERDES6G_REVID	0x00000010	1	SERDES6G REVID	Page 134

1.7.11.1 HSIO:SERDES6G_ANA_STATUS:SERDES6G_IB_STATUS0

Parent: HSIO:SERDES6G_ANA_STATUS

Instances: 1

Status register for Signal Detect

TABLE 1-277: FIELDS IN SERDES6G_IB_STATUS0

Field Name	Bit	Access	Description	Default
IB_CAL_DONE	8	R/O	Signals mission mode after calibration was done.	0x0
IB_HP_GAIN_ACT	7	R/O	Flag high-pass-gain regulation activity. Caution: currently this signal is generated with a clock of datarate/16 and NOT captured (sticky).	0x0
IB_MID_GAIN_ACT	6	R/O	Flag mid-pass-gain regulation activity. Caution: currently this signal is generated with a clock of datarate/16 and NOT captured (sticky).	0x0

TABLE 1-277: FIELDS IN SERDES6G_IB_STATUS0 (CONTINUED)

Field Name	Bit	Access	Description	Default
IB_LP_GAIN_ACT	5	R/O	Flag low-pass-gain regulation activity. Caution: currently this signal is generated with a clock of datarate/16 and NOT captured (sticky).	0x0
IB_OFFSET_ACT	4	R/O	Flag offset regulation activity. Caution: currently this signal is generated with a clock of datarate/16 and NOT captured (sticky).	0x0
IB_OFFSET_VLD	3	R/O	Valid average data of calibration process at ib_offset_stat available.	0x0
IB_OFFSET_ERR	2	R/O	Overflow error during calibration process. Value at ib_offset_stat not valid.	0x0
IB_OFFSDIR	1	R/O	Detection of offset direction in selected (ib_offsx) sampling channels	0x0
IB_SIG_DET	0	R/O	Detection of toggling signal at PADP and PADN	0x0

1.7.11.2 HSIO:SERDES6G_ANA_STATUS:SERDES6G_IB_STATUS1

Parent: HSIO:SERDES6G_ANA_STATUS

Instances: 1

Regulation stage status register

TABLE 1-278: FIELDS IN SERDES6G_IB_STATUS1

Field Name	Bit	Access	Description	Default
IB_HP_GAIN_STAT	23:18	R/O	Current high-pass-gain regulation value	0x00
IB_MID_GAIN_STAT	17:12	R/O	Current mid-pass-gain regulation value	0x00
IB_LP_GAIN_STAT	11:6	R/O	Current low-pass-gain regulation value	0x00
IB_OFFSET_STAT	5:0	R/O	Current offset regulation value	0x00

1.7.11.3 HSIO:SERDES6G_ANA_STATUS:SERDES6G_ACJTAG_STATUS

Parent: HSIO:SERDES6G_ANA_STATUS

Instances: 1

Status register of (AC)JTAG debug capability

TABLE 1-279: FIELDS IN SERDES6G_ACJTAG_STATUS

Field Name	Bit	Access	Description	Default
ACJTAG_CAPT_DATA_N	2	R/O	ACJTAG captured data for n leg	0x0
ACJTAG_CAPT_DATA_P	1	R/O	ACJTAG captured data for p leg	0x0
IB_DIRECT	0	R/O	JTAG direct input (directly driven)	0x0

1.7.11.4 HSIO:SERDES6G_ANA_STATUS:SERDES6G_PLL_STATUS

Parent: HSIO:SERDES6G_ANA_STATUS

Instances: 1

Status register of SERDES6G RCPLL

TABLE 1-280: FIELDS IN SERDES6G_PLL_STATUS

Field Name	Bit	Access	Description	Default
PLL_CAL_NOT_DONE	10	R/O	Calibration status 0: Calibration not started or ongoing 1: Calibration finished	0x0
PLL_CAL_ERR	9	R/O	Calibration error 0: No error during calibration 1: Errors occurred during calibration	0x0
PLL_OUT_OF_RANGE_ERR	8	R/O	Out of range error 0: No out of range condition detected 1: Out of range condition since last calibration detected	0x0
PLL_RB_DATA	7:0	R/O	PLL read-back data, depending on "pll_rb_data_sel" either the calibrated setting or the measured period	0x00

1.7.11.5 HSIO:SERDES6G_ANA_STATUS:SERDES6G_REVID

Parent: HSIO:SERDES6G_ANA_STATUS

Instances: 1

Revision ID register

TABLE 1-281: FIELDS IN SERDES6G_REVID

Field Name	Bit	Access	Description	Default
SERDES_REV	31:26	R/O	Serdes revision	0x00
RCPLL_REV	25:21	R/O	RCPLL revision	0x00
SER_REV	20:16	R/O	SER revision	0x00
DES_REV	15:10	R/O	DES revision	0x00
OB_REV	9:5	R/O	OB revision	0x00
IB_REV	4:0	R/O	IB revision	0x00

1.7.12 HSIO:MCB_SERDES6G_CFG

Parent: HSIO

Instances: 1

All SERDES6G macros are accessed via the serial Macro Configuration Bus (MCB). Each macro is configured by one MCB Slave. All MCB Slaves are connected in a daisy-chain loop.

TABLE 1-282: REGISTERS IN MCB_SERDES6G_CFG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MCB_SERDES6G_ADDR_CFG	0x00000000	1	MCB SERDES6G Address Cfg	Page 134

1.7.12.1 HSIO:MCB_SERDES6G_CFG:MCB_SERDES6G_ADDR_CFG

Parent: HSIO:MCB_SERDES6G_CFG

Instances: 1

Configuration of SERDES6G MCB Slaves to be accessed

TABLE 1-283: FIELDS IN MCB_SERDES6G_ADDR_CFG

Field Name	Bit	Access	Description	Default
SERDES6G_WR_ONE_SHOT	31	One-shot	Initiate a write access to marked SERDES6G Slaves 0: No write operation pending 1: Initiate write to slaves (kept 1 until write operation has finished)	0x0
SERDES6G_RD_ONE_SHOT	30	One-shot	Initiate a read access to marked SERDES6G Slaves 0: No read operation pending (read op finished after bit has been set) 1: Initiate a read access (kept 1 until read operation has finished)	0x0
SERDES6G_ADDR	24:0	R/W	Activation vector for SERDES6G-Slaves, one-hot coded, each bit is related to one macro, e.g. bit 0 enables/disables access to macro no. 0. 0: Disable macro access via MCB 1: Enable macro access via MCB	0x1FFFFFF

1.7.13 HSIO:HW_CFGSTAT

Parent: HSIO

Instances: 1

TABLE 1-284: REGISTERS IN HW_CFGSTAT

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
HW_CFG	0x00000000	1	Various configration	Page 135
HW_QSGMII_CFG	0x00000004	1	Additional configuration for QSGMII channels	Page 137
HW_QSGMII_STAT	0x00000008	1	Additional status from QSGMII channels	Page 137

1.7.13.1 HSIO:HW_CFGSTAT:HW_CFG

Parent: HSIO:HW_CFGSTAT

Instances: 1

TABLE 1-285: FIELDS IN HW_CFG

Field Name	Bit	Access	Description	Default
DEV2G5_10_MODE	6	R/W	Configure mode of device DEV2G5_10. This can be connected to SerDes1G_5 or SerDes6G_2 Setting PCIE_ENA prevents that DEV2G5_10 can be connected to SerDes6G_2 0: DEV2G5_10 is connected to Serdes6G_2 1: DEV2G5_10 is connected to SerDes1G_5	0x0
DEV1G_9_MODE	5	R/W	Configure mode of device DEV1G_9. This can be connected to SerDes1G_4 or be disconnected 0: DEV1G_9 is disconnected 1: DEV1G_9 is connected to SerDes1G_4	0x0
DEV1G_6_MODE	4	R/W	Configure mode of device DEV1G_6. This can be connected to SerDes1G_3 or SerDes6G_0 when QSGMII mode is enabled. Setting HW_CFG.QSGMII_ENA will force QSGMII mode and the DEV1G_6_MODE setting is ignored. 0: DEV1G_6 is disconnected 1: DEV1G_6 is connected to SerDes1G_3	0x0
DEV1G_5_MODE	3	R/W	Configure mode of device DEV1G_5. This can be connected to SerDes1G_5, SerDes1G_1 or SerDes6G_0 when QSGMII mode is enabled. Setting HW_CFG.QSGMII_ENA will force QSGMII mode and the DEV1G_5_MODE setting is ignored. 0: DEV1G_5 is connected to SerDes1G_5 1: DEV1G_5 is connected to SerDes1G_1	0x0
DEV1G_4_MODE	2	R/W	Configure mode of device DEV1G_4. This can be connected to SerDes1G_4, SerDes1G_2 or SerDes6G_0 when QSGMII mode is enabled. Setting HW_CFG.QSGMII_ENA will force QSGMII mode and the DEV1G_4_MODE setting is ignored. 0: DEV1G_4 is connected to SerDes1G_4 1: DEV1G_4 is connected to SerDes1G_2	0x0
PCIE_ENA	1	R/W	Set to enable PCIe mode for SerDes6G_2. 0: Disable PCIE 1: Enable PCIE	0x0

TABLE 1-285: FIELDS IN HW_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
QSGMII_ENA	0	R/W	Set bit 0 to enable QSGMII mode for devices DEV1G_4, DEV1G_5, DEV1G_6, and DEV1G_7 via SerDes6G_0. 0: Disable QSGMII 1: Enable QSGMII	0x0

1.7.13.2 HSIO:HW_CFGSTAT:HW_QSGMII_CFG

Parent: HSIO:HW_CFGSTAT

Instances: 1

TABLE 1-286: FIELDS IN HW_QSGMII_CFG

Field Name	Bit	Access	Description	Default
SHYST_DIS	3	R/W	Set to disable hysteresis of receive synchronization state machine. This setting applies to all QSGMII channels.	0x0
E_DET_ENA	2	R/W	Set to enable 8b10b receive error propagation; 8b10b error code-groups are replaced by K70.7 error symbols. This setting applies to all QSGMII channels.	0x0
USE_I1_ENA	1	R/W	Set to transmit I1 during idle sequencing only. This setting applies to all QSGMII channels.	0x0
FLIP_LANES	0	R/W	Set to flip QSGMII lanes: Lane 0 is interchanged with 3, and 1 is interchanged with 2 for both receie and transmit directions. Each bit in this field correspond to a QSGMII channel, bit 0 configures QSGMII#0, bit 1 configures QSGMII#1, etc.	0x0

1.7.13.3 HSIO:HW_CFGSTAT:HW_QSGMII_STAT

Parent: HSIO:HW_CFGSTAT

Instances: 1

TABLE 1-287: FIELDS IN HW_QSGMII_STAT

Field Name	Bit	Access	Description	Default
DELAY_VAR_X200PS	6:1	R/O	Variable delay in QSGMII ingress path provided in steps of 200ps, values 0 though 39 is possible allowing a span from 0ns to 7.8ns. Each replication of this register correspond to a QSGMII channel, replication 0 is from QSGMII#0, replication 1 is from QSGMII#1, etc. The value for a QSGMII channel is valid when it has synchronized to an incoming QSGMII signal, and will remain constant while the channel stays in sync.	0x00

TABLE 1-287: FIELDS IN HW_QSGMII_STAT (CONTINUED)

Field Name	Bit	Access	Description	Default
SYNC	0	R/O	Set when QSGMII channel has successfully synchronized on K28.1 code-group, this field is only valid when HSIO::HW_QSGMII_CFG.SHYST_DIS is 0.	0x0

1.7.14 HSIO:TEMP_SENSOR

Parent: HSIO

Instances: 1

Controls the temperature sensor readout

TABLE 1-288: REGISTERS IN TEMP_SENSOR

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
TEMP_SENSOR_CTRL	0x00000000	1	Temperature Sensor Control	Page 138
TEMP_SENSOR_STAT	0x00000008	1	Temperature Sensor Status	Page 138

1.7.14.1 HSIO:TEMP_SENSOR:TEMP_SENSOR_CTRL

Parent: HSIO:TEMP_SENSOR

Instances: 1

TABLE 1-289: FIELDS IN TEMP_SENSOR_CTRL

Field Name	Bit	Access	Description	Default
SAMPLE_ENA	0	R/W	Set this field to enable sampling of temperature. Approximately 200us after setting this field HSIO::TEMP_SENSOR_STAT.TEMP_VALID will be set together with a valid temperature value. After this the temperature will be updated every 500us for as long as this field remains set. Clear to disable temperature sensor.	0x0

1.7.14.2 HSIO:TEMP_SENSOR:TEMP_SENSOR_STAT

Parent: HSIO:TEMP_SENSOR

Instances: 1

TABLE 1-290: FIELDS IN TEMP_SENSOR_STAT

Field Name	Bit	Access	Description	Default
TEMP_VALID	8	R/O	This fied is set when valid temperature data is available in HSIO::TEMP_SENSOR_STAT.TEMP.	0x0

TABLE 1-290: FIELDS IN TEMP_SENSOR_STAT (CONTINUED)

Field Name	Bit	Access	Description	Default
TEMP	7:0	R/O	Temperature data readout, this field is valid when HSIO::TEMP_SENSOR_STAT.TEMP_VALID is set. This field is continually updated while the termperature sensor is enabled, see HSIO::TEMP_SENSOR_CTRL.SAMPLE_ENA for more information. Temperature(C)=177.4 - 0.8777*DATA	0x00

1.8 ICPU_CFG

TABLE 1-291: REGISTER GROUPS IN ICPU_CFG

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
CPU_SYSTEM_CTRL	0x00000000	1	Configurations for the CPU system.	Page 139
SPI_MST	0x0000003C	1	SPI boot master	Page 142
MPU8051	0x00000054	1	Configuration/status for the 8051	Page 144
INTR	0x00000070	1	Interrupt controller	Page 147
TIMERS	0x000000E4	1	Timers	Page 154
MEMCTRL	0x00000110	1	DDR2/3 memory controller	Page 157
TWI_DELAY	0x00000198	1	TWI hold time configuration	Page 167
TWI_SPIKE_FILTER	0x0000019C	1	TWI spike filter configuration	Page 168
FDMA	0x000001A0	1	Frame DMA	Page 168
PCIE	0x00000364	1	PCIe endpoint	Page 179
MANUAL_XTRINJ	0x00004000	1	Manual extraction and injection via FDMA	Page 184

1.8.1 ICPU_CFG:CPU_SYSTEM_CTRL

Parent: ICPU_CFG

Instances: 1

TABLE 1-292: REGISTERS IN CPU_SYSTEM_CTRL

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
GPR	0x00000000	8 0x00000004	General Purpose Register	Page 139
RESET	0x00000020	1	Reset Settings	Page 140
GENERAL_CTRL	0x00000024	1	General control	Page 140
GENERAL_STAT	0x00000028	1	General status	Page 141

1.8.1.1 ICPU_CFG:CPU_SYSTEM_CTRL:GPR

Parent: ICPU_CFG:CPU_SYSTEM_CTRL

Instances: 8

TABLE 1-293: FIELDS IN GPR

Field Name	Bit	Access	Description	Default
GPR	31:0	R/W	General purpose 8 times 32-bit registers for software development and debug. Note: This register is only reset by the device's reset input, i.e. it is not affected by soft reset!	0x00000000

1.8.1.2 ICPU_CFG:CPU_SYSTEM_CTRL:RESET

Parent: ICPU_CFG:CPU_SYSTEM_CTRL

Instances: 1

TABLE 1-294: FIELDS IN RESET

Field Name	Bit	Access	Description	Default
CORE_RST_CPU_ONLY	3	R/W	Set this field to enable VCore System reset protection. It is possible to protect the VCore System from soft-reset (issued via RESET.CORE_RST_FORCE) and watch-dog-timeout. When this field is set the afore-mentioned resets only reset the VCore CPU, not the VCore System. 0: Soft-reset and WDT-event and reset entire VCore 1: Soft-reset and WDT-event only reset the VCore CPU	0x0
CORE_RST_PROTECT	2	R/W	Set this field to enable VCore reset protec-tion. It is possible to protect the entire VCore from chip-level soft-reset (issued via DEVCPU_GCB::SOFT_RST.SOFT_-CHIP_RST). Setting this field does not pro-tect agains hard-reset of the chip (by asserting the reset pin). 0: No reset protection 1: VCore is protected from chip-level-soft-reset	0x0
CORE_RST_FORCE	1	One-shot	Set this field to generate a soft reset for the VCore. This field will be cleared when the reset has taken effect. It is possible to protect the VCore system (everything else than the VCore CPU) from reset via RESET.CORE_RST_CPU_ONLY. 0: VCore is not reset 1: Initiate soft reset of the VCore	0x0
MEM_RST_FORCE	0	R/W	Clear this field to release the DDR2/3 con-troller from reset. 0: Memory controller is not reset 1: Memory controller is forced in reset	0x1

1.8.1.3 ICPU_CFG:CPU_SYSTEM_CTRL:GENERAL_CTRL

Parent: ICPU_CFG:CPU_SYSTEM_CTRL

Instances: 1

TABLE 1-295: FIELDS IN GENERAL_CTRL

Field Name	Bit	Access	Description	Default
CPU_MIPS_DIS	11	R/W	Set this field to disable the MIPS core (and instead enable 8051).	0x0
IF_MIIM_SLV_ADDR_SEL	10	R/W	MIIM slave address when MIIM slave interface is enabled. 0: Address 0 1: Address 31	0x0
IF_MIIM_SLV_ENA	9	R/W	The default value of this field depends on strapping of the VCore. Set this field to enable the MIIM slave-interface on the GPIOs.	0x0
IF_SI_OWNER	5:4	R/W	The default value of this field depends on strapping of the VCore. Select the owner of the dedicated SI interface. Note, if the SI slave is not owner of this interface, it is not possible for an external CPU to access registers in the chip via the dedicated SI interface. It is possible for VCore CPU to boot via SI and then change overship to either SI Slave or SI Master Controller. 00 : SI Slave 01 : SI Boot Master 10 : SI Master Controller	0x0
SIMC_SSP_ENA	3	R/W	Hooked up to the master contention input (ss_in_n) of the SPI Master block.	0x0
CPU_BE_ENA	2	R/W	The default value of this field depends on strapping of the VCore. Set this field to force the MIPS VCore CPU into Big-Endian mode.	0x0
CPU_DIS	1	R/W	The default value of this field depends on strapping of the VCore. Clear this field to allow booting of the VCore CPU, while this field is set the VCore CPU is held in reset. 0: VCore CPU is allowed to boot 1: VCore CPU is forced in reset	0x1
BOOT_MODE_ENA	0	R/W	Use this field to change from Boot mode to Normal mode. In Boot mode, the reset vector of the VCore CPU maps to CS0 on the FLASH interface. When in Normal mode, this address maps instead to the DRAM Controller. The DRAM Controller must be operational before disabling Boot mode. After setting Boot mode, this register must be read back. The change in Boot mode takes effect during read. 0: The VCore memory map is in Normal mode. 1: The VCore memory map is in Boot mode.	0x1

1.8.1.4 ICPU_CFG:CPU_SYSTEM_CTRL:GENERAL_STAT

Parent: ICPU_CFG:CPU_SYSTEM_CTRL

Instances: 1

TABLE 1-296: FIELDS IN GENERAL_STAT

Field Name	Bit	Access	Description	Default
VCORE_CFG	7:4	R/O	Shows the value of the VCore Cfg strapping inputs.	0x0
REG_IF_ERR	3:1	R/O	Debug information for checking register read/write problems. This is a read-only field which can only be cleared by reset of the VCore System. 0: No errors detected. 1: Non-32bit access to VCore or SwC registers, access has been discarded, read returns 0x8888 or 0x88. 2: SwC registers not ready when accessed, access has been discarded, read returns 0x88888888. 3: SwC registers reported error, check DEVCPU_ORG::ERR_CNTS for error, read returns 0x88888888. 4: Unimplemented VCore register, access has been discarded, read returns 0x88888888.	0x0
CPU_SLEEP	0	R/O	This field is set if the VCore CPU has entered sleep mode.	0x0

1.8.2 ICPU_CFG:SPI_MST

Parent: ICPU_CFG

Instances: 1

TABLE 1-297: REGISTERS IN SPI_MST

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SPI_MST_CFG	0x00000000	1	SPI boot master configuration	Page 142
SW_MODE	0x00000014	1	Manual control of the SPI interface	Page 143

1.8.2.1 ICPU_CFG:SPI_MST:SPI_MST_CFG

Parent: ICPU_CFG:SPI_MST

Instances: 1

TABLE 1-298: FIELDS IN SPI_MST_CFG

Field Name	Bit	Access	Description	Default
A32B_ENA	11	R/W	Set to enable 32bit address mode. In 32bit addressing mode only CS0 is used, the SPI address region is limited to 256MByte reserved for the SI interface. 0: Use 24bit addressing with 4 different CS. 1: Use 32bit addressing on CS0, max 256MByte	0x0
FAST_READ_ENA	10	R/W	The type of read-instruction that the SPI Controller generates for reads. 0: READ (slow read - Instruction code - 0x03) 1: FAST READ (fast read - Instruction code - 0x0B)	0x0
CS_DESELECT_TIME	9:5	R/W	The minimum number of SPI clock cycles for which the SPI chip select (SI_nEn) must be deasserted in between transfers. Typical value of this is 100 ns. Setting this field to 0 is illegal.	0x1F
CLK_DIV	4:0	R/W	Controls the clock frequency for the SPI interface (SI_Clk). The clock frequency is VCore system clock divided by the value of this field. Setting this field to 0 or 1 value is illegal. The SPI interface frequency is: 250MHz/ CLK_DIV.	0x1F

1.8.2.2 ICPU_CFG:SPI_MST:SW_MODE

Parent: ICPU_CFG:SPI_MST

Instances: 1

Note: There are 4 chip selects in total, but only chip select 0 is mapped to IO-pin (SI_nEn). The rest of the SPI chip selects are available as alternate functions on GPIOs, these must be enabled in the GPIO controller before they can be controlled via this register.

TABLE 1-299: FIELDS IN SW_MODE

Field Name	Bit	Access	Description	Default
SW_PIN_CTRL_MODE	13	R/W	Set to enable software pin control mode (Bit banging), when set software has direct control of the SPI interface. This mode is used for writing into flash.	0x0
SW_SPI_SCK	12	R/W	Value to drive on SI_Clk output. This field is only used if SW_MODE.SW_PIN_CTRL_-MODE is set.	0x0
SW_SPI_SCK_OE	11	R/W	Set to enable drive of SI_Clk output. This field is only used if SW_MODE.SW_PIN_CTRL_MODE is set.	0x0
SW_SPI_SDO	10	R/W	Value to drive on SI_DO output. This field is only used if SW_MODE.SW_PIN_CTRL_-MODE is set.	0x0

TABLE 1-299: FIELDS IN SW_MODE (CONTINUED)

Field Name	Bit	Access	Description	Default
SW_SPI_SDO_OE	9	R/W	Set to enable drive of SI_DO output. This field is only used if SW_MODE.SW_PIN_CTRL_MODE is set.	0x0
SW_SPI_CS	8:5	R/W	Value to drive on SI_nEn outputs, each bit in this field maps to a corresponding chip-select (0 though 3). This field is only used if SW_MODE.SW_PIN_CTRL_MODE is set. Note: Chip selects 1 though 3 are available as alternate GPIO functions.	0x0
SW_SPI_CS_OE	4:1	R/W	Set to enable drive of SI_nEn outputs, each bit in this field maps to a corresponding chip-select (0 though 3). This field is only used if SW_MODE.SW_PIN_CTRL_MODE is set. Note: Chip selects 1 though 3 are available as alternate GPIO functions.	0x0
SW_SPI_SDI	0	R/O	Current value of the SI_DI input.	0x0

1.8.3 ICPU_CFG:MPU8051

Parent: ICPU_CFG

Instances: 1

TABLE 1-300: REGISTERS IN MPU8051

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MPU8051_STAT	0x00000004	1	8051 status	Page 144
MPU8051_MMAP	0x00000008	1	8051 memory mapping mechanism	Page 145
MEMACC_CTRL	0x0000000C	1	8051 memory load/examine configuration/status	Page 145
MEMACC	0x00000010	1	8051 memory offset configuration	Page 146
MEMACC_SBA	0x00000014	1	SBA memory offset configuration	Page 146

1.8.3.1 ICPU_CFG:MPU8051:MPU8051_STAT

Parent: ICPU_CFG:MPU8051

Instances: 1

These read only fields can be used for debugging 8051 programs.

TABLE 1-301: FIELDS IN MPU8051_STAT

Field Name	Bit	Access	Description	Default
MPU8051_STOP	8	R/O	Set when the 8051 has stopped itself by setting bit 2 in the PCON SFR register.	0x0
MPU8051_GPR	7:0	R/O	A read-only copy of the 8051 GPR register at SFR address 0xF0.	0x00

1.8.3.2 ICPU_CFG:MPU8051:MPU8051_MMAP

Parent: ICPU_CFG:MPU8051

Instances: 1

The MAP_* and MSADDR_* fields in this register is similar to the corresponding 8051 SFR register for control mapping the on-chip memory into the 8051 memory space. These fields must be used to configure 8051 memory mapping if the 8051 on-chip memory is loaded manually via an external processor. If the 8051 program itself does loading of on-chip memory then it must instead use the SFR equivalents.

TABLE 1-302: FIELDS IN MPU8051_MMAP

Field Name	Bit	Access	Description	Default
MSADDR_CODE_HIGH	7	R/W	Configure which half of the on-chip memory an 8051 data-accesses in the low 32KByte memory range (when mapped to on-chip memory) actually use. When set to 0, the low half of the on-chip 64KByte is accessed, when set to 1 the high half is accessed.	0x0
MSADDR_CODE_LOW	6	R/W	Configure which half of the on-chip memory an 8051 code-accesses in the low 32KByte memory range (when mapped to on-chip memory) actually use. When set to 0, the low half of the on-chip 64KByte is accessed, when set to 1 the high half is accessed.	0x0
MSADDR_DATA_HIGH	5	R/W	Configure which half of the on-chip memory an 8051 data-accesses in the high 32KByte memory range (when mapped to on-chip memory) actually use. When set to 0, the low half of the on-chip 64KByte is accessed, when set to 1 the high half is accessed.	0x0
MSADDR_DATA_LOW	4	R/W	Configure which half of the on-chip memory an 8051 data-accesses in the low 32KByte memory range (when mapped to on-chip memory) actually use. When set to 0, the low half of the on-chip 64KByte is accessed, when set to 1 the high half is accessed.	0x0
MAP_CODE_HIGH	3	R/W	Set to map 8051 code-accesses in the high 32KByte memory range to on-chip memory instead of FLASH.	0x0
MAP_CODE_LOW	2	R/W	Set to map 8051 code-accesses in the low 32KByte memory range to on-chip memory instead of FLASH.	0x0
MAP_DATA_HIGH	1	R/W	Set to map 8051 data-accesses in the high 32KByte memory range to on-chip memory instead of FLASH.	0x0
MAP_DATA_LOW	0	R/W	Set to map 8051 data-accesses in the low 32KByte memory range to on-chip memory instead of FLASH.	0x0

1.8.3.3 ICPU_CFG:MPU8051:MEMACC_CTRL

Parent: ICPU_CFG:MPU8051

Instances: 1

TABLE 1-303: FIELDS IN MEMACC_CTRL

Field Name	Bit	Access	Description	Default
MEMACC_EXAMINE	1	R/W	This field controls if the onchip 8051 memory is either loaded (written) or examined (read). 0: Load data from SBA to onchip memory. 1: Examine data from onchip memory to SBA.	0x0
MEMACC_DO	0	One-shot	Set this field to start an access with the parameters specified by MEMACC_CTRL.MEMACC_EXAMINE, MEMACC.MEMACC_START, MEMACC.MEMACC_STOP, and MEMACC_SBA.MEMACC_SBA_START. This field is cleared when the requested number of 32-bit words has been transfered.	0x0

1.8.3.4 ICPU_CFG:MPU8051:MEMACC

Parent: ICPU_CFG:MPU8051

Instances: 1

When loading (or examining) onchip 8051 memory, then it is only possible to move 32-bit words. This is why bits [17:16] and [1:0] of this register is not implemented. Setting START and STOP addresses determines how many words that are loaded (or examined). For example, when loading programs of less than 64KBytes, decreasing the stop address will speed up the load time.

When manually loading or examining the onchip 8051 memory via an external CPU the data has to be put somewhere in SBA memory space on its way into or out-of the onchip 8051 memory, for this the 8 x 32-bit general purpose registers starting at 0x70000000 is a good choice. By using all (or some) of these registers it is possible to move up to 8 32-bit words to/from the onchip memory per access.

TABLE 1-304: FIELDS IN MEMACC

Field Name	Bit	Access	Description	Default
MEMACC_STOP	31:18	R/W	Ending 32-bit word address when loading or examining the onchip 8051 memory, the value of this field must be equal to or higher than the MEMACC.MEMACC_START field.	0x3FFF
MEMACC_START	15:2	R/W	Starting 32-bit word address when loading or examining the onchip 8051 memory.	0x0000

1.8.3.5 ICPU_CFG:MPU8051:MEMACC_SBA

Parent: ICPU_CFG:MPU8051

Instances: 1

There is no stop address in the SBA address space. The number of 32-bit words which is moved per access is determined by the MEMACC.MEMACC_START and MEMACC.MEMACC_STOP.

TABLE 1-305: FIELDS IN MEMACC_SBA

Field Name	Bit	Access	Description	Default
MEMACC_SBA_START	31:2	R/W	This field determines where in the SBA memory space (32-bit alligned) the automatic load/examine mechanims reads/writes data to/from the onchip 8051 memory.	0x10000000

1.8.4 ICPU_CFG:INTR

Parent: ICPU_CFG

Instances: 1

These are the VCore interrupt controller registers. The controller has 25 interrupt sources (inputs) which can each be mapped to one of 4 interrupt destinations (outputs). The controller has a dedicated block for handling 15 device interrupts; the handling of device interrupts can be considered a small interrupt controller located before the interrupt controller.

TABLE 1-306: REGISTERS IN INTR

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
INTR_RAW	0x00000000	1	Interrupt raw status	Page 147
INTR_TRIGGER	0x00000004	2 0x00000004	Interrupt trigger mode	Page 148
INTR_FORCE	0x0000000C	1	Interrupt force sticky event	Page 148
INTR_STICKY	0x00000010	1	Interrupt sticky status	Page 149
INTR_BYPASS	0x00000014	1	Interrupt bypass enable	Page 149
INTR_ENA	0x00000018	1	Interrupt enable	Page 149
INTR_ENA_CLR	0x0000001C	1	Atomic clear of interrupt enable	Page 150
INTR_ENA_SET	0x00000020	1	Atomic set of interrupt	Page 150
INTR_IDENT	0x00000024	1	Currently active interrupt sources	Page 150
DST_INTR_MAP	0x00000028	4 0x00000004	Mapping of source to destination interrupts	Page 150
DST_INTR_IDENT	0x00000038	4 0x00000004	Currently active interrupt sources per destination	Page 151
EXT_SRC_INTR_POL	0x00000048	1	External source interrupt polarity	Page 151
EXT_DST_INTR_POL	0x0000004C	1	External destination interrupt polarity	Page 151
EXT_DST_INTR_DRV	0x00000050	1	External interrupt destination output drive mode	Page 152
DEV_INTR_POL	0x00000054	1	Device interrupt polarity	Page 152
DEV_INTR_RAW	0x00000058	1	Device interrupt raw status	Page 152
DEV_INTR_TRIGGER	0x0000005C	2 0x00000004	Device interrupt trigger mode	Page 152
DEV_INTR_STICKY	0x00000064	1	Device interrupt sticky status	Page 153
DEV_INTR_BYPASS	0x00000068	1	Device interrupt bypass enable	Page 154
DEV_INTR_ENA	0x0000006C	1	Device interrupt enable	Page 154
DEV_INTR_IDENT	0x00000070	1	Currently active device interrupts	Page 154

1.8.4.1 ICPU_CFG:INTR:INTR_RAW

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-307: FIELDS IN INTR_RAW

Field Name	Bit	Access	Description	Default
INTR_RAW	24:0	R/O	Shows the current value of individual interrupt sources. All sources are active high (the external interrupts has been corrected for polarity as configured in ICPU_CFG::EXT_SRC_INTR_POL).	0x0000000

1.8.4.2 ICPU_CFG:INTR:INTR_TRIGGER

Parent: ICPU_CFG:INTR

Instances: 2

TABLE 1-308: FIELDS IN INTR_TRIGGER

Field Name	Bit	Access	Description	Default
INTR_TRIGGER	24:0	R/W	Configure trigger mode of individual interrupt sources. The trigger mode determines how the value of the ICPU_CFG::INTR_RAW register is transfered to the ICPU_CFG::INTR_STICKY register. This register is replicated, the first replication controls bit 0 in the encoding, the second replication controls bit 1 in the encoding. I.e. to configure falling-edge-triggered interrupt for interrupt source 5; set ICPU_CFG::INTR_TRIGGER[0][5]='0' and ICPU_CFG::INTR_TRIGGER[1][5]='1'. For level-triggered interrupts ICPU_CFG::INTR_STICKY is set for as long as the corresponding bit in ICPU_CFG::INTR_RAW is high - i.e. is not possible to clear a bit in ICPU_CFG::INTR_STICKY until the corresponding ICPU_CFG::INTR_RAW is zero. For edge-triggeded interrupts ICPU_CFG::INTR_STICKY is set when the corresponding bit in ICPU_CFG::INTR_RAW changes value. For falling-edge-triggeded interrupts ICPU_CFG::INTR_STICKY is set when the corresponding bit in ICPU_CFG::INTR_RAW changes from '1' to '0'. For rising-edge-triggeded interrupts ICPU_CFG::INTR_STICKY is set when the corresponding bit in ICPU_CFG::INTR_RAW changes from '0' to '1'. 0: Interrupt is level-activated 1: Interrupt is edge-triggered 2: Interrupt is falling-edge-triggered 3: Interrupt is rising-edge-triggered	0x0000000

1.8.4.3 ICPU_CFG:INTR:INTR_FORCE

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-309: FIELDS IN INTR_FORCE

Field Name	Bit	Access	Description	Default
INTR_FORCE	24:0	One-shot	Set to force corresponding ICPU_CFG::INTR_STICKY bits. This field may be useful during development of software interrupt handler functions.	0x0000000

1.8.4.4 ICPU_CFG:INTR:INTR_STICKY

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-310: FIELDS IN INTR_STICKY

Field Name	Bit	Access	Description	Default
INTR_STICKY	24:0	Sticky	This register is set based on source interrupt events or by debug-force. See ICPU_CFG::INTR_TRIGGER and ICPU_CFG::INTR_FORCE for more information. Bits in this register remains set until cleared by software.	0x0000000

1.8.4.5 ICPU_CFG:INTR:INTR_BYPASS

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-311: FIELDS IN INTR_BYPASS

Field Name	Bit	Access	Description	Default
INTR_BYPASS	24:0	R/W	This register allows bypass of ICPU_CFG::INTR_STICKY for individual interrupt sources. When an interrupt source is in bypass mode then ICPU_CFG::INTR_RAW is used instead of ICPU_CFG::INTR_STICKY. Note: Enabling bypass does not make sense for all interrupt sources. It should only be used when the corresponding interrupt is sticky at the source. For example manual extraction data available interrupts can be configured to bypass, because the interrupt will remain asserted until the available data has been extracted. Note: The device interrupt is bypassed per default, "stickyness" is already implemented by ICPU_CFG::DEV_INTR_STICKY.	0x0000001

1.8.4.6 ICPU_CFG:INTR:INTR_ENA

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-312: FIELDS IN INTR_ENA

Field Name	Bit	Access	Description	Default
INTR_ENA	24:0	R/W	Set to enable propagation of individual interrupt sources to destinations. Atomic access to this register (needed in a multithreaded system) can be implemented by the ICPU_CFG::INTR_ENA_CLR and ICPU_CFG::INTR_ENA_SET registers.	0x0000000

1.8.4.7 ICPU_CFG:INTR:INTR_ENA_CLR

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-313: FIELDS IN INTR_ENA_CLR

Field Name	Bit	Access	Description	Default
INTR_ENA_CLR	24:0	One-shot	Set bit(s) in this register to clear the corresponding bits in ICPU_CFG::INTR_ENA. This register can be used for atomic access to ICPU_CFG::INTR_ENA register.	0x0000000

1.8.4.8 ICPU_CFG:INTR:INTR_ENA_SET

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-314: FIELDS IN INTR_ENA_SET

Field Name	Bit	Access	Description	Default
INTR_ENA_SET	24:0	One-shot	Set bit(s) in this register to set the corresponding bits in ICPU_CFG::INTR_ENA. This register can be used for atomic access to ICPU_CFG::INTR_ENA register.	0x0000000

1.8.4.9 ICPU_CFG:INTR:INTR_IDENT

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-315: FIELDS IN INTR_IDENT

Field Name	Bit	Access	Description	Default
INTR_IDENT	24:0	R/O	Shows the currently active interrupt sources. For interrupt sources that are not bypassed this register is a result of AND'ing ICPU_CFG::INTR_STICKY with ICPU_CFG::INTR_ENA.	0x0000000

1.8.4.10 ICPU_CFG:INTR:DST_INTR_MAP

Parent: ICPU_CFG:INTR

Instances: 4

Replicated per destination interrupt.

TABLE 1-316: FIELDS IN DST_INTR_MAP

Field Name	Bit	Access	Description	Default
DST_INTR_MAP	24:0	R/W	Set to enable mapping of individual interrupt sources to interrupt destinations. This register is replicated once for each destination interrupt.	0x0000000

1.8.4.11 ICPU_CFG:INTR:DST_INTR_IDENT

Parent: ICPU_CFG:INTR

Instances: 4

Replicated per destination interrupt.

TABLE 1-317: FIELDS IN DST_INTR_IDENT

Field Name	Bit	Access	Description	Default
DST_INTR_IDENT	24:0	R/O	Shows the currently active interrupt sources per destination interrupt. The contents of this register is equal to ICPU_CFG::INTR_IDENT AND'ed with the corresponding ICPU_CFG::DST_INTR_MAP. If any bit is set in this register the corresponding destination interrupt is asserted.	0x0000000

1.8.4.12 ICPU_CFG:INTR:EXT_SRC_INTR_POL

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-318: FIELDS IN EXT_SRC_INTR_POL

Field Name	Bit	Access	Description	Default
EXT_SRC_INTR_POL	1:0	R/W	Set individual bits in this register to configure polarity of the corresponding external source interrupt. 0: External interrupt input is active low 1: External interrupt input is active high	0x0

1.8.4.13 ICPU_CFG:INTR:EXT_DST_INTR_POL

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-319: FIELDS IN EXT_DST_INTR_POL

Field Name	Bit	Access	Description	Default
EXT_DST_INTR_POL	1:0	R/W	Set individual bits in this register to configure polarity of the corresponding external destination interrupt. 0: External interrupt output is active low 1: External interrupt output is active high	0x0

1.8.4.14 ICPU_CFG:INTR:EXT_DST_INTR_DRV

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-320: FIELDS IN EXT_DST_INTR_DRV

Field Name	Bit	Access	Description	Default
EXT_DST_INTR_DRV	1:0	R/W	This register configures drive mode of the corresponding external destination interrupt. 0: Only drive external interrupt output when asserted (tristate when inactive) 1: External interrupt output is always driven	0x0

1.8.4.15 ICPU_CFG:INTR:DEV_INTR_POL

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-321: FIELDS IN DEV_INTR_POL

Field Name	Bit	Access	Description	Default
DEV_INTR_POL	14:0	R/W	Set individual bits in this register to configure polarity of the corresponding device interrupt. 0: Device interrupt is active low 1: Device interrupt is active high	0x7FFF

1.8.4.16 ICPU_CFG:INTR:DEV_INTR_RAW

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-322: FIELDS IN DEV_INTR_RAW

Field Name	Bit	Access	Description	Default
DEV_INTR_RAW	14:0	R/O	Shows the current value of individual device interrupt sources. All sources are active high (sources have been corrected for polarity as configured in ICPU_CFG::DEV_INTR_POL).	0x0000

1.8.4.17 ICPU_CFG:INTR:DEV_INTR_TRIGGER

Parent: ICPU_CFG:INTR

Instances: 2

TABLE 1-323: FIELDS IN DEV_INTR_TRIGGER

Field Name	Bit	Access	Description	Default
DEV_INTR_TRIGGER	14:0	R/W	Configure trigger mode of individual device interrupt sources. The trigger mode determines how the value of the ICPU_CFG::DEV_INTR_RAW register is transfered to the ICPU_CFG::DEV_INTR_STICKY register. This register is replicated, the first replication controls bit 0 in the encoding, the second replication controls bit 1 in the encoding. I.e. to configure edge-triggered interrupt for device 3; set ICPU_CFG::DEV_INTR_TRIGGER[0][3]='1' and ICPU_CFG::DEV_INTR_TRIGGER[1][3]='0'. For level-triggered interrupts ICPU_CFG::DEV_INTR_STICKY is set for as long as the corresponding bit in ICPU_CFG::DEV_INTR_RAW is high - i.e. is not possible to clear a bit in ICPU_CFG::DEV_INTR_STICKY until the corresponding ICPU_CFG::DEV_INTR_RAW is zero. For edge-triggeded interrupts ICPU_CFG::DEV_INTR_STICKY is set when the corresponding bit in ICPU_CFG::DEV_INTR_RAW changes value. For falling-edge-triggeded interrupts ICPU_CFG::DEV_INTR_STICKY is set when the corresponding bit in ICPU_CFG::DEV_INTR_RAW changes from '1' to '0'. For rising-edge-triggeded interrupts ICPU_CFG::DEV_INTR_STICKY is set when the corresponding bit in ICPU_CFG::DEV_INTR_RAW changes from '0' to '1'. 0: Interrupt is level-activated 1: Interrupt is edge-triggered 2: Interrupt is falling-edge-triggered 3: Interrupt is rising-edge-triggered	0x0000

1.8.4.18 ICPU_CFG:INTR:DEV_INTR_STICKY

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-324: FIELDS IN DEV_INTR_STICKY

Field Name	Bit	Access	Description	Default
DEV_INTR_STICKY	14:0	Sticky	This register is set based on device interrupt sourec events. See ICPU_CFG::DEV_INTR_TRIGGER for more information. Bits in this register remains set until cleared by software.	0x0000

1.8.4.19 ICPU_CFG:INTR:DEV_INTR_BYPASS

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-325: FIELDS IN DEV_INTR_BYPASS

Field Name	Bit	Access	Description	Default
DEV_INTR_BYPASS	14:0	R/W	This register allows bypass of ICPU_CFG::DEV_INTR_STICKY for individual device interrupt sources. When a device interrupt source is in bypass mode then ICPU_CFG::DEV_INTR_RAW is used instead of ICPU_CFG::DEV_INTR_STICKY. See note on bypass in ICPU_CFG::INTR_BYPASS.	0x0000

1.8.4.20 ICPU_CFG:INTR:DEV_INTR_ENA

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-326: FIELDS IN DEV_INTR_ENA

Field Name	Bit	Access	Description	Default
DEV_INTR_ENA	14:0	R/W	Set to enable propagation of individual device interrupt sources to the main interrupt controller.	0x0000

1.8.4.21 ICPU_CFG:INTR:DEV_INTR_IDENT

Parent: ICPU_CFG:INTR

Instances: 1

TABLE 1-327: FIELDS IN DEV_INTR_IDENT

Field Name	Bit	Access	Description	Default
DEV_INTR_IDENT	14:0	R/O	Shows the currently active interrupt sources. For interrupt sources that are not bypassed this register is a result of AND'ing ICPU_CFG::DEV_INTR_STICKY with ICPU_CFG::DEV_INTR_ENA.	0x0000

1.8.5 ICPU_CFG:TIMERS

Parent: ICPU_CFG

Instances: 1

TABLE 1-328: REGISTERS IN TIMERS

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
WDT	0x00000000	1	Watchdog timer	Page 155
TIMER_TICK_DIV	0x00000004	1	Timer tick divider	Page 155
TIMER_VALUE	0x00000008	3 0x00000004	Timer value	Page 156
TIMER_RELOAD_VALUE	0x00000014	3 0x00000004	Timer reload value	Page 156
TIMER_CTRL	0x00000020	3 0x00000004	Timer control	Page 157

1.8.5.1 ICPU_CFG:TIMERS:WDT

Parent: ICPU_CFG:TIMERS

Instances: 1

TABLE 1-329: FIELDS IN WDT

Field Name	Bit	Access	Description	Default
WDT_STATUS	9	R/O	Shows whether the last reset was caused by a watchdog timer reset. This field is updated during reset, therefore it is always valid. 0: Reset was not caused by WDT 1: Reset was caused by WDT timeout	0x0
WDT_ENABLE	8	R/W	Use this field to enable or disable the watchdog timer. When the WDT is enabled, it causes a reset after 2 seconds if it is not periodically reset. This field is only read by the WDT after a sucessful lock sequence (see ICPU_CFG::WDT.WDT_LOCK). 0: WDT is disabled 1: WDT is enabled	0x0
WDT_LOCK	7:0	R/W	Use this field to configure and reset the WDT. When writing 0xBE to this field immediately followed by writing 0xEF, the WDT resets and configurations are read from this register (as provided when the 0xEF is written). When the WDT is enabled, writing any value other than 0xBE or 0xEF after 0xBE is written, causes a WDT reset as if the timer had run out.	0x00

1.8.5.2 ICPU_CFG:TIMERS:TIMER_TICK_DIV

Parent: ICPU_CFG:TIMERS

Instances: 1

TABLE 1-330: FIELDS IN TIMER_TICK_DIV

Field Name	Bit	Access	Description	Default
TIMER_TICK_DIV	17:0	R/W	The timer tick generator runs from the VCore System frequency. By default, the divider value generates a timer tick every 100 us (10KHz). The timer tick is used for all of the timers (except the WDT). This field must not be set to generate a timer tick of less than 0.1 us (higher than 10MHz). If this field is changed, it may take up to 2ms before the timers are running stable at the new frequency. The timer tick frequency is: 250MHz/(TIMER_TICK_DIV+1).	0x061A7

1.8.5.3 ICPU_CFG:TIMERS:TIMER_VALUE

Parent: ICPU_CFG:TIMERS

Instances: 3

TABLE 1-331: FIELDS IN TIMER_VALUE

Field Name	Bit	Access	Description	Default
TIMER_VAL	31:0	R/W	The current value of the timer. When enabled via TIMER_CTRL.TIMER_ENA the timer decrements at every timer tick (see TIMER_TICK_DIV for more info on timer tick frequency). When the timer has reached 0, and a timer-tick is received, then an interrupt is generated. For example; If a periodic interrupt is needed every 1ms, and the timer tick is generated every 100us then the TIMER_VALUE (and TIMER_RELOAD_VALUE) must be configured to 9. By default the timer will reload from the TIMER_RELOAD_VALUE when interrupt is generated, and then continue decrementing from the reloaded value. It is possible to make the timer stop after generating interrupt by setting TIMER_CTRL.ONE_SHOT_ENA.	0x00000000

1.8.5.4 ICPU_CFG:TIMERS:TIMER_RELOAD_VALUE

Parent: ICPU_CFG:TIMERS

Instances: 3

TABLE 1-332: FIELDS IN TIMER_RELOAD_VALUE

Field Name	Bit	Access	Description	Default
RELOAD_VAL	31:0	R/W	The contents of this field are loaded into the corresponding timer (TIMER_VALUE) when it wraps (decrements a zero).	0x00000000

1.8.5.5 ICPU_CFG:TIMERS:TIMER_CTRL

Parent: ICPU_CFG:TIMERS

Instances: 3

TABLE 1-333: FIELDS IN TIMER_CTRL

Field Name	Bit	Access	Description	Default
ONE_SHOT_ENA	2	R/W	When set the timer will automatically disable itself after it has generated interrupt.	0x0
TIMER_ENA	1	R/W	When enabled, the correponding timer decrements at each timer-tick. If TIMER_CTRL.ONE_SHOT_ENA is set this field is cleared when the timer reach 0 and interrupt is generated. 0: Timer is disabled 1: Timer is enabled	0x0
FORCE_RELOAD	0	One-shot	Set this field to force the reload of the timer, this will set the TIMER_VALUE to TIMER_RELOAD_VALUE for the corresponding timer. This field can be set at the same time as enabeling the counter, in that case the counter will be reloaded and then enabled for counting.	0x0

1.8.6 ICPU_CFG:MEMCTRL

Parent: ICPU_CFG

Instances: 1

TABLE 1-334: REGISTERS IN MEMCTRL

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MEMCTRL_CTRL	0x00000000	1	DDR2/3 control	Page 158
MEMCTRL_CFG	0x00000004	1	DDR2/3 configuration	Page 159
MEMCTRL_STAT	0x00000008	1	DDR2/3 status	Page 160
MEMCTRL_REF_PERIOD	0x0000000C	1	Refresh configuration	Page 161
MEMCTRL_ZQCAL	0x00000010	1	DDR3 ZQ-calibration	Page 161
MEMCTRL_TIMING0	0x00000014	1	Timing configuration	Page 161
MEMCTRL_TIMING1	0x00000018	1	Timing configuration	Page 163
MEMCTRL_TIMING2	0x0000001C	1	Timing configuration	Page 163
MEMCTRL_TIMING3	0x00000020	1	Timing configuration	Page 164
MEMCTRL_MR0_VAL	0x00000028	1	Mode register 0 value	Page 164
MEMCTRL_MR1_VAL	0x0000002C	1	Mode register 1 value	Page 164
MEMCTRL_MR2_VAL	0x00000030	1	Mode register 2 value	Page 165
MEMCTRL_MR3_VAL	0x00000034	1	Mode register 3 value	Page 165
MEMCTRL_TERMRES_CTRL	0x00000038	1	On-die-termination configuration	Page 165
MEMCTRL_DQS_DLY	0x00000040	2 0x00000004	DQS window configuration	Page 166
MEMPHY_CFG	0x00000050	1	SSTL configuration	Page 166

TABLE 1-334: REGISTERS IN MEMCTRL (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MEMPHY_ZCAL	0x00000078	1	SSTL drive-strength calibration	Page 167

1.8.6.1 ICPU_CFG:MEMCTRL:MEMCTRL_CTRL

Parent: ICPU_CFG:MEMCTRL

Instances: 1

TABLE 1-335: FIELDS IN MEMCTRL_CTRL

Field Name	Bit	Access	Description	Default
PWR_DOWN	3	R/W	Set this field to force the memory module into low power self refresh mode. The ICPU_CFG::MEMCTRL_STAT.PWR_DOWN_ACK is set when the controller has executed the command. Clear this field to bring the controller back to normal operation. Note: Before using power-down the ICPU_CFG::MEMCTRL_TIMING2.INIT_DLY must be reconfigured, see field description for more information.	0x0
MDSET	2	One-shot	Set this field to do memory register write command. The register to write is defined by ICPU_CFG::MEMCTRL_MR0_VAL[15:14], the data to write is defined by ICPU_CFG::MEMCTRL_MR0_VAL[15:0].	0x0
STALL_REF_ENA	1	R/W	Set this field to temporarily give software unhindered access to memory; two things changes in the controller: a) Refreshes are postponed until ICPU_CFG::MEMCTRL_REF_PERIOD.MAX_PEND_REF is exceeded. b) Only a single refresh will be issued when exceeding ICPU_CFG::MEMCTRL_REF_PERIOD.MAX_PEND_REF. When this field is NOT set (the normal case) the memory controller try to do refreshes during controller idle periods, also once refresh has started - all pending refreshes will be performed. Note: Interrupt routines and other high-priority tasks can use this field to ensure uninterrupted access to the memory, such routines must clear this field when memory access is no longer critical.	0x0

TABLE 1-335: FIELDS IN MEMCTRL_CTRL (CONTINUED)

Field Name	Bit	Access	Description	Default
INITIALIZE	0	One-shot	Set this field to force the memory controller to initialize the SDRAM. This field is automatically cleared after the controller has started initialization of the SDRAM. Wait for ICPU_CFG::MEMCTRL_STAT.INIT_DONE before performing read/write operations on the controller. Note: The ICPU_CFG::MEMCTRL_CFG, ICPU_CFG::MEMCTRL_REF_PERIOD, ICPU_CFG::MEMCTRL_TIMING*, and ICPU_CFG::MEMCTRL_MR* registers must be configured appropriately before setting this field.	0x0

1.8.6.2 ICPU_CFG:MEMCTRL:MEMCTRL_CFG

Parent: ICPU_CFG:MEMCTRL

Instances: 1

TABLE 1-336: FIELDS IN MEMCTRL_CFG

Field Name	Bit	Access	Description	Default
DDR_512MBYTE_PLUS	16	R/W	Set this field to enable support for more than 512MByte SDRAM.	0x0
DDR_ECC_ERR_ENA	15	R/W	Set this field to enable propagation of ECC errors to SBA by generating bus-error event when ECC error is detected. This field may not be set unless ICPU_CFG::MEMCTRL_CFG.DDR_ECC_ENA is also set.	0x0
DDR_ECC_COR_ENA	14	R/W	Set this field to enable propagation of ECC corrections to SBA by generating bus-error event when ECC correction is detected. This field may not be set unless ICPU_CFG::MEMCTRL_CFG.DDR_ECC_ENA is also set.	0x0
DDR_ECC_ENA	13	R/W	This field enables ECC mode of the SDRAM controller. This field may only be set when ICPU_CFG::MEMCTRL_CFG.DDR_WIDTH is configured for 16bit. In ECC mode byte lane 1 is used for ECC information and byte lane 0 is used for data. When using ECC mode, then the amount of random-access memory available to an application is half of the physically attached memory.	0x0
DDR_WIDTH	12	R/W	This field configures the interface width of the SDRAM controller. If 8bit is selected then byte lane 0 must be populated by external SDRAM memory. 0: 8bit 1: 16bit	0x0

TABLE 1-336: FIELDS IN MEMCTRL_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
DDR_MODE	11	R/W	This field configures the operating mode of the SDRAM controller. 0: DDR2 1: DDR3	0x0
BURST_SIZE	10	R/W	The number of data-bytes that is transmitted during one burst (of the defined burst length: ICPU_CFG::MEMC-TRL_CFG.BURST_LEN). 0: 8 data-bytes per burst. 1: 16 data-bytes per burst.	0x0
BURST_LEN	9	R/W	The burst size that is used by the SDRAM controller. The SDRAM must be configured with the corresponding burst size (through the ICPU_CFG::MEMCTRL_MR0_VAL register.) Note: The number of data-bytes that is transmitted during one burst must be encoded in the ICPU_CFG::MEMCTRL_CFG.BURST_-SIZE field. 0 : BURST4 1 : BURST8	0x0
BANK_CNT	8	R/W	Number of banks in the SDRAM configuration being used. 0 : 4 banks 1 : 8 banks	0x0
MSB_ROW_ADDR	7:4	R/W	Set to 1 less than the number of row address bits for the SDRAM configuration in use.	0x0
MSB_COL_ADDR	3:0	R/W	Set to 1 less than the number of column address bits for the SDRAM configuration in use. For example; for a memory that is using column addresses {A11, A9-A0} this field must be set to 10.	0x0

1.8.6.3 ICPU_CFG:MEMCTRL:MEMCTRL_STAT

Parent: ICPU_CFG:MEMCTRL

Instances: 1

TABLE 1-337: FIELDS IN MEMCTRL_STAT

Field Name	Bit	Access	Description	Default
RDATA_MASKED	5	Sticky	Set if the controller has masked a data-set towards the SBA (too many data words received from SDRAM). This field may be set during training. If this event occurs during normal operation then the DQS window may be wrongly configured.	0x0
RDATA_DUMMY	4	Sticky	Set if the controller has inserted missing data-set towards the SBA (too few data words received from SDRAM). This field may be set during training. If this event occurs during normal operation then the DQS window may be wrongly configured.	0x0

TABLE 1-337: FIELDS IN MEMCTRL_STAT (CONTINUED)

Field Name	Bit	Access	Description	Default
RDATA_ECC_ERR	3	Sticky	Set if the controller is enabled for ECC and an uncorrectable error has been detected.	0x0
RDATA_ECC_COR	2	Sticky	Set if the controller is enabled for ECC and a dataset has been corrected (a correctable error has been corrected).	0x0
PWR_DOWN_ACK	1	R/O	Is set once the memory controller has put the SDRAM in low power self refresh mode (result of setting ICPU_CFG::MEMCTRL_CTRL.PWR_DOWN). When this field is set SDRAM interface signal may turned off (all signals except the CKE and ODT) may be left floating.	0x0
INIT_DONE	0	R/O	This field is set after initialization of the SDRAM is done. When this field is set then read/write operations can be performed.	0x0

1.8.6.4 ICPU_CFG:MEMCTRL:MEMCTRL_REF_PERIOD

Parent: ICPU_CFG:MEMCTRL

Instances: 1

TABLE 1-338: FIELDS IN MEMCTRL_REF_PERIOD

Field Name	Bit	Access	Description	Default
MAX_PEND_REF	19:16	R/W	Maximum number of refreshes that are allowed to be outstanding at any time. If the number of outstanding refreshes exceeds this value, the memory controller will stop data accesses, and issue refreshes. If no outstanding refreshes is allowed then set this field to 0.	0x8
REF_PERIOD	15:0	R/W	Refresh interval of the SDRAM expressed in number of clock cycles. This value is calculated by dividing the average periodic refresh interval (tREFI) by the clock period.	0x0100

1.8.6.5 ICPU_CFG:MEMCTRL:MEMCTRL_ZQCAL

Parent: ICPU_CFG:MEMCTRL

Instances: 1

TABLE 1-339: FIELDS IN MEMCTRL_ZQCAL

Field Name	Bit	Access	Description	Default
ZQCAL_LONG	1	One-shot	Set this field to issue long ZQ calibration command. This field is cleared when calibration has been performed.	0x0
ZQCAL_SHORT	0	One-shot	Set this field to issue short ZQ calibration command. This field is cleared when calibration has been performed.	0x0

1.8.6.6 ICPU_CFG:MEMCTRL:MEMCTRL_TIMING0

Parent: ICPU_CFG:MEMCTRL

Instances: 1

The Following parameters are needed for configuration of the ICPU_CFG::MEMCTRL_TIMING* registers. All asynchronous delays should be converted (round up) to the corresponding number of DDR controller clock cycles. Note that DDR modules may specify a minimum number of clock cycles for some parameters:

RL=CL

BL=2 for burst4, 4 for burst8

Additional for DDR2 memories:

WL=RL-1

MD=tMRD

ID=400ns

SD=tXSRD

OW=WL-2

OR=RL-3

RP=tRP for 4-bank modules, tRPA for 8-bank modules

FAW=1 for 4-bank modules, tFAW for 8-bank modules

Additional for DDR3 memories:

WL=CWL

MD=tMOD

ID=tXPR

SD=tDLLK

OW=2

OR=2

RP=tRP

FAW=tFAW

TABLE 1-340: FIELDS IN MEMCTRL_TIMING0

Field Name	Bit	Access	Description	Default
RD_TO_WR_DLY	31:28	R/W	Delay from read to write on same chip select. RL+BL+1-WL	0x4
WR_CS_CHANGE_DLY	27:24	R/W	Delay from write to write on different chip selects. If ICPU_CFG::MEMCTRL_TERMRES_CTRL.ODT_WR_ENA==9 then increase this field by 2 (to allow ODT handover between destination devices). BL-1	0x3
RD_CS_CHANGE_DLY	23:20	R/W	Delay from read to read on different chip selects. BL	0x2
RAS_TO_PRECH_DLY	19:16	R/W	Delay from RAS to precharge. tRAS_min-1	0x0
WR_TO_PRECH_DLY	15:12	R/W	Delay from write to precharge. WL+BL+tWR-1	0x0

TABLE 1-340: FIELDS IN MEMCTRL_TIMING0 (CONTINUED)

Field Name	Bit	Access	Description	Default
RD_TO_PRECH_DLY	11:8	R/W	Delay from read to precharge. BL-1	0x0
WR_DATA_XFR_DLY	7:4	R/W	Delay from write command to data. WL-1	0x0
RD_DATA_XFR_DLY	3:0	R/W	Delay from read command to data. Important; this delay is further increased by the DQS delay logic - see ICPU_CFG::MEMCTRL_DQS_DLY for more information. RL-3	0x0

1.8.6.7 ICPU_CFG:MEMCTRL:MEMCTRL_TIMING1

Parent: ICPU_CFG:MEMCTRL

Instances: 1

See ICPU_CFG::MEMCTRL_TIMING0 for description of important parameters.

TABLE 1-341: FIELDS IN MEMCTRL_TIMING1

Field Name	Bit	Access	Description	Default
RAS_TO_RAS_SAME_BANK_DLY	31:24	R/W	Delay from RAS to RAS within same bank. tRC-1	0x00
BANK8_FAW_DLY	23:16	R/W	Four bank activate period. FAW-1	0x00
PRECH_TO_RAS_DLY	15:12	R/W	Delay from precharge to RAS. tRP-1	0x0
RAS_TO_RAS_DLY	11:8	R/W	Delay from RAS to RAS. tRRD-1	0x0
RAS_TO_CAS_DLY	7:4	R/W	Delay from RAS to CAS. tRCD-1	0x0
WR_TO_RD_DLY	3:0	R/W	Delay from write to read. WL+BL+tWTR-1	0x0

1.8.6.8 ICPU_CFG:MEMCTRL:MEMCTRL_TIMING2

Parent: ICPU_CFG:MEMCTRL

Instances: 1

See ICPU_CFG::MEMCTRL_TIMING0 for description of important parameters.

TABLE 1-342: FIELDS IN MEMCTRL_TIMING2

Field Name	Bit	Access	Description	Default
PRECH_ALL_DLY	31:28	R/W	Delay after precharge all. RP-1	0x0
MDSET_DLY	27:24	R/W	Delay after register-write. MD-1	0x0
REF_DLY	23:16	R/W	Delay after refresh. tRFC-1	0x00
INIT_DLY	15:0	R/W	Delay for initialization (see ICPU_CFG::MEMCTRL_CTRL.INITIALIZE). Before initialization: ID-1 After initialization: SD-1	0x0000

1.8.6.9 ICPU_CFG:MEMCTRL:MEMCTRL_TIMING3

Parent: ICPU_CFG:MEMCTRL

Instances: 1

See ICPU_CFG::MEMCTRL_TIMING0 for description of important parameters.

TABLE 1-343: FIELDS IN MEMCTRL_TIMING3

Field Name	Bit	Access	Description	Default
ODT_RD_DLY	15:12	R/W	Delay from read to ODT assert. External ODT assert for read commands is enabled by ICPU_CFG::MEMCTRL_TERMRES_CTRL.ODT_RD_ENA. OR-1	0x0
ODT_WR_DLY	11:8	R/W	Delay from write to ODT assert. External ODT assert for write commands is enabled by ICPU_CFG::MEMCTRL_TERMRES_CTRL.ODT_WR_ENA. OW-1	0x0
LOCAL_ODT_RD_DLY	7:4	R/W	Delay from read to local read-termination activate. Important; this delay is further increased by the DQS delay logic - see ICPU_CFG::MEMCTRL_DQS_DLY for more information. Local read-termination is enabled by ICPU_CFG::MEMCTRL_TERMRES_CTRL.LOCAL_ODT_RD_ENA. RL-3	0x0
WR_TO_RD_CS_CHANGE_DLY	3:0	R/W	Delay from write to write on different chip selects. WL+tWTR-1	0x0

1.8.6.10 ICPU_CFG:MEMCTRL:MEMCTRL_MR0_VAL

Parent: ICPU_CFG:MEMCTRL

Instances: 1

TABLE 1-344: FIELDS IN MEMCTRL_MR0_VAL

Field Name	Bit	Access	Description	Default
MR0_VAL	15:0	R/W	Value to be programmed into the mode register (0) during SDRAM initialization. During initialization bit 8 (DLL Reset) of this register must be set to 0, the memory controller automatically sets this bit when required during the initialization procedure. After initialization this field is used for sending custom MDSET commands. If ICPU_CFG::MEMCTRL_CTRL.MDSET is set then the value of this field is written to the register defined by bit [15:14].	0x0000

1.8.6.11 ICPU_CFG:MEMCTRL:MEMCTRL_MR1_VAL

Parent: ICPU_CFG:MEMCTRL

Instances: 1

TABLE 1-345: FIELDS IN MEMCTRL_MR1_VAL

Field Name	Bit	Access	Description	Default
MR1_VAL	15:0	R/W	Value to be programmed into mode register 1 / extended mode register during SDRAM initialization. Bits 7 through 9 (OCD Calibration Program) of this register must be set to 0x7, the memory controller sets this field when required during the initialization procedure.	0x0000

1.8.6.12 ICPU_CFG:MEMCTRL:MEMCTRL_MR2_VAL

Parent: ICPU_CFG:MEMCTRL

Instances: 1

TABLE 1-346: FIELDS IN MEMCTRL_MR2_VAL

Field Name	Bit	Access	Description	Default
MR2_VAL	15:0	R/W	Value to be programmed into mode register 2 / extended mode register 2 during SDRAM initialization.	0x0000

1.8.6.13 ICPU_CFG:MEMCTRL:MEMCTRL_MR3_VAL

Parent: ICPU_CFG:MEMCTRL

Instances: 1

TABLE 1-347: FIELDS IN MEMCTRL_MR3_VAL

Field Name	Bit	Access	Description	Default
MR3_VAL	15:0	R/W	Value to be programmed into mode register 3 / extended mode register 3 during SDRAM initialization.	0x0000

1.8.6.14 ICPU_CFG:MEMCTRL:MEMCTRL_TERMRES_CTRL

Parent: ICPU_CFG:MEMCTRL

Instances: 1

TABLE 1-348: FIELDS IN MEMCTRL_TERMRES_CTRL

Field Name	Bit	Access	Description	Default
ODT_RD_EXT	11	R/W	Set this field to extend the ODT termination output by one clock during read operations.	0x0
ODT_RD_ENA	10:7	R/W	Set to enable ODT output during read operations. 0: Reading will not assert ODT 1: Assert ODT for CS0 read 2: Assert ODT for CS1 read 3: Assert ODT for any read Other values are reserved	0x0
ODT_WR_EXT	6	R/W	Set this field to extend the ODT termination output by one clock during write operations.	0x0

TABLE 1-348: FIELDS IN MEMCTRL_TERMRES_CTRL (CONTINUED)

Field Name	Bit	Access	Description	Default
ODT_WR_ENA	5:2	R/W	Set to assert ODT output(s) during write operations. 0: Writing will not assert ODT 1: Assert ODT for CS1 write 2: Assert ODT for CS0 write 3: Assert ODT for any write Others values are reserved	0x0
LOCAL_ODT_RD_EXT	1	R/W	Set this field to extend the local termination by one clock during read operations.	0x0
LOCAL_ODT_RD_ENA	0	R/W	Set to enable local termination during a read operation.	0x0

1.8.6.15 ICPU_CFG:MEMCTRL:MEMCTRL_DQS_DLY

Parent: ICPU_CFG:MEMCTRL

Instances: 2

This register is replicated two times, once for each Byte Lane (first replication corresponds to Byte Lane 0).

TABLE 1-349: FIELDS IN MEMCTRL_DQS_DLY

Field Name	Bit	Access	Description	Default
RESERVED	10:8	R/W	Must be set to its default.	0x3
RESERVED	7:5	R/W	Must be set to its default.	0x3
DQS_DLY	4:0	R/W	This field configures read-window delay as an offset in 1/4 clock cycles from the fixed read-delay configured in MEMCTRL_TIMING0.RD_DATA_XFR_DLY.	0x00

1.8.6.16 ICPU_CFG:MEMCTRL:MEMPHY_CFG

Parent: ICPU_CFG:MEMCTRL

Instances: 1

TABLE 1-350: FIELDS IN MEMPHY_CFG

Field Name	Bit	Access	Description	Default
PHY_FIFO_RST	7	R/W	Soft-reset to the FIFO blocks in the memory controller physical interface. Leave at default value. 0: PHY FIFOs is in working mode. 1: PHY FIFOs is forced in reset.	0x0
PHY_ODT_OE	4	R/W	Set to enable output drive of the ODT output.	0x0
PHY_CK_OE	3	R/W	Set to enable output drive of the CK/nCK and CKE outputs.	0x0
PHY_CL_OE	2	R/W	Set to enable output drive of the Command Lane outputs.	0x0
PHY_SSTL_ENA	1	R/W	Set this field to enable the SSTL mode for the memory controllers physical interfaces.	0x1
PHY_RST	0	R/W	Master reset to the memory controller physical interface. 0: PHY is in working mode. 1: PHY is forced in reset.	0x1

1.8.6.17 ICPU_CFG:MEMCTRL:MEMPHY_ZCAL

Parent: ICPU_CFG:MEMCTRL

Instances: 1

TABLE 1-351: FIELDS IN MEMPHY_ZCAL

Field Name	Bit	Access	Description	Default
ZCAL_PROG_ODT	8:5	R/W	Together with the external reference resistor this field configures the SSTL On-Die-Termination (ODT) impedance. This field must be configured prior to, or at the same time as, setting the ICPU_CFG::MEMPHY_ZCAL.ZCAL_ENA field. 2: 150ohms 3: 120ohms 5: 75ohms 7: 60ohms 8: 50ohms 11: 40ohms 13: 34ohms Other values are reserved.	0x3
ZCAL_PROG	4:1	R/W	Together with the external reference resistor this field configures the SSTL output drive-strength. This field must be configured prior to, or at the same time as, setting the ICPU_CFG::MEMPHY_ZCAL.ZCAL_ENA field. 2: 150ohms 3: 120ohms 5: 75ohms 7: 60ohms 8: 50ohms 11: 40ohms 13: 34ohms Other values are reserved.	0xB
ZCAL_ENA	0	One-shot	Set this field to start automatic SSTL output and ODT drive-strength calibration. This field is cleared when the automatic calibration has completed.	0x0

1.8.7 ICPU_CFG:TWI_DELAY

Parent: ICPU_CFG

Instances: 1

TABLE 1-352: REGISTERS IN TWI_DELAY

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
TWI_CONFIG	0x00000000	1	TWI hold time configuration	Page 168

1.8.7.1 ICPU_CFG:TWI_DELAY:TWI_CONFIG

Parent: ICPU_CFG:TWI_DELAY

Instances: 1

TABLE 1-353: FIELDS IN TWI_CONFIG

Field Name	Bit	Access	Description	Default
TWI_CNT_RELOAD	8:1	R/W	Configure the hold time delay to apply to SDA after SCK when transmitting from the device. This delay is expressed in a number of VCore System clock cycles. The delay value should be as close to 300ns as possible without going below 300ns. Set to (300ns/4.8ns + 2) = 65	0x00
TWI_DELAY_ENABLE	0	R/W	Set this field to enable hold time on the TWI SDA output. When enabled the TWI_CONFIG.TWI_CNT_RELOAD field determines the amount of hold time to apply to SDA.	0x0

1.8.8 ICPU_CFG:TWI_SPIKE_FILTER

Parent: ICPU_CFG

Instances: 1

TABLE 1-354: REGISTERS IN TWI_SPIKE_FILTER

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
TWI_SPIKE_FILTER_CFG	0x00000000	1	TWI spike filter configuration	Page 168

1.8.8.1 ICPU_CFG:TWI_SPIKE_FILTER:TWI_SPIKE_FILTER_CFG

Parent: ICPU_CFG:TWI_SPIKE_FILTER

Instances: 1

TABLE 1-355: FIELDS IN TWI_SPIKE_FILTER_CFG

Field Name	Bit	Access	Description	Default
SPIKE_FILTER_CFG	4:0	R/W	Configuration of the spike filter width on the SCL and SDA inputs. Filters spikes with a width of (SPIKE_FILTER_CFG+1)*SYSTEM_CLK or less.	0x00

1.8.9 ICPU_CFG:FDMA

Parent: ICPU_CFG

Instances: 1

For registers and fields in this group, which are replicated per channel; replication-index-0 correponds to extraction-channel 0, replication-index-1 corresponds to extraction-channel 1, and so on. The injection channels follows after the extraction channels.

TABLE 1-356: REGISTERS IN FDMA

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
FDMA_DCB_LLP	0x00000000	10 0x00000004	Pointer to next DCB	Page 169
FDMA_DCB_DATAP	0x00000028	10 0x00000004	Pointer to data block	Page 170
FDMA_DCB_DATAL	0x00000050	10 0x00000004	Length of data block	Page 170
FDMA_DCB_STAT	0x00000078	10 0x00000004	Status word	Page 170
FDMA_DCB_LLP_PREV	0x000000A0	10 0x00000004	Pointer to current DCB	Page 171
FDMA_CH_STAT	0x000000C8	1	Current channel status	Page 171
FDMA_CH_SAFE	0x000000CC	1	Current channel safe-status	Page 171
FDMA_CH_ACTIVATE	0x000000D0	1	Activate specific channels	Page 171
FDMA_CH_DISABLE	0x000000D4	1	Disable specific channels	Page 172
FDMA_CH_FORCEDIS	0x000000D8	1	Ungraceful disable of specific channels	Page 172
FDMA_CH_CNT	0x000000DC	10 0x00000004	Channel counters	Page 172
FDMA_CH_INJ_TOKEN_CNT	0x00000104	8 0x00000004	Injection channel token counter	Page 173
FDMA_CH_INJ_TO-KEN_TICK_RLD	0x00000124	8 0x00000004	Injection channel token tick counter reload value	Page 174
FDMA_CH_INJ_TO-KEN_TICK_CNT	0x00000144	8 0x00000004	Injection channel token tick counter	Page 174
FDMA_EVT_ERR	0x00000164	1	Error event	Page 174
FDMA_EVT_ERR_CODE	0x00000168	1	Additional error information	Page 175
FDMA_INTR_LLP	0x0000016C	1	LLP-event	Page 175
FDMA_INTR_LLP_ENA	0x00000170	1	LLP-event interrupt enable	Page 175
FDMA_INTR_FRM	0x00000174	1	FRM-event	Page 176
FDMA_INTR_FRM_ENA	0x00000178	1	FRM-event interrupt enable	Page 176
FDMA_INTR_SIG	0x0000017C	1	SIG-event	Page 176
FDMA_INTR_SIG_ENA	0x00000180	1	SIG-event interrupt enable	Page 176
FDMA_INTR_ENA	0x00000184	1	Channel interrupt enable	Page 176
FDMA_INTR_IDENT	0x00000188	1	Currently interrupting chan-nels	Page 177
FDMA_CH_CFG	0x0000018C	10 0x00000004	Channel specific configura-tions	Page 177
FDMA_GCFG	0x000001B4	1	General FDMA configurations	Page 178
FDMA_GSTAT	0x000001B8	1	General FDMA status	Page 178
FDMA_IDLECNT	0x000001BC	1	FDMA idle Counter	Page 179
FDMA_CONST	0x000001C0	1	Constants for this FDMA implementation.	Page 179

1.8.9.1 ICPU_CFG:FDMA:FDMA_DCB_LLP

Parent: ICPU_CFG:FDMA

Instances: 10

TABLE 1-357: FIELDS IN FDMA_DCB_LLP

Field Name	Bit	Access	Description	Default
LLP	31:0	R/W	This field is used by the FDMA for tracking lists of DCBs. This field is updated automatically when the FDMA load DCBs from memory. This field can only be modified when the channel is in safe mode, see ICPU_CFG::FDMA_CH_SAFE.CH_SAFE for more information.	0x00000000

1.8.9.2 ICPU_CFG:FDMA:FDMA_DCB_DATAP

Parent: ICPU_CFG:FDMA

Instances: 10

TABLE 1-358: FIELDS IN FDMA_DCB_DATAP

Field Name	Bit	Access	Description	Default
DATAP	31:0	R/O	For debug, current data-pointer.	0x00000000

1.8.9.3 ICPU_CFG:FDMA:FDMA_DCB_DATAL

Parent: ICPU_CFG:FDMA

Instances: 10

TABLE 1-359: FIELDS IN FDMA_DCB_DATAL

Field Name	Bit	Access	Description	Default
TOKEN	17	R/O	For debug, current token-indication.	0x0
DATAL	15:0	R/O	For debug, current data-length.	0x0000

1.8.9.4 ICPU_CFG:FDMA:FDMA_DCB_STAT

Parent: ICPU_CFG:FDMA

Instances: 10

This register is updated by the FDMA during extraction or injection. Software cannot rely on the value of this register.

TABLE 1-360: FIELDS IN FDMA_DCB_STAT

Field Name	Bit	Access	Description	Default
BLOCKO	31:20	R/O	Block offset in bytes, the value of this field is loaded from the DCB.	0x000
PD	19	R/O	Pruned/Done indication.	0x0
ABORT	18	R/O	Abort indication.	0x0
EOF	17	R/O	Set when the current DCB contains end-of-frame.	0x0
SOF	16	R/O	Set when the current DCB contains start-of-frame.	0x0

TABLE 1-360: FIELDS IN FDMA_DCB_STAT (CONTINUED)

Field Name	Bit	Access	Description	Default
BLOCKL	15:0	R/O	Block size in bytes, excluding offset (as specified in ICPU_CFG::FDMA_DCB_STAT.BLOCKO). For frames that span multiple DCBs, this field only shows the amount of data in the current DCB.	0x0000

1.8.9.5 ICPU_CFG:FDMA:FDMA_DCB_LLP_PREV

Parent: ICPU_CFG:FDMA

Instances: 10

TABLE 1-361: FIELDS IN FDMA_DCB_LLP_PREV

Field Name	Bit	Access	Description	Default
LLP_PREV	31:2	R/O	This field holds the pointer to current DCB (the previous ICPU_CFG::FDMA_DCB_LLP.LLP).	0x00000000

1.8.9.6 ICPU_CFG:FDMA:FDMA_CH_STAT

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-362: FIELDS IN FDMA_CH_STAT

Field Name	Bit	Access	Description	Default
CH_STAT	9:0	R/O	Shows status for all FDMA channels, there is one bit per channel. 0:Disabled 1:Updating, or Active	0x000

1.8.9.7 ICPU_CFG:FDMA:FDMA_CH_SAFE

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-363: FIELDS IN FDMA_CH_SAFE

Field Name	Bit	Access	Description	Default
CH_SAFE	9:0	R/O	When set it is safe for software to read/modify/write ICPU_CFG::FDMA_DCB_LLP.LLP, ICPU_CFG::FDMA_CH_CNT.CH_CNT_SIG, ICPU_CFG::FDMA_CH_CNT.CH_CNT_DCB, and ICPU_CFG::FDMA_CH_INJ_TOKEN_CNT.CH_INJ_TOKEN_CNT. There is one bit per channel. This field is set when a channel is a) disabled or b) active and scheduled for disabling.	0x3FF

1.8.9.8 ICPU_CFG:FDMA:FDMA_CH_ACTIVATE

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-364: FIELDS IN FDMA_CH_ACTIVATE

Field Name	Bit	Access	Description	Default
CH_ACTIVATE	9:0	One-shot	Enables specific FDMA channels, there is one bit per channel. Setting a bit in this field will clear a corresponding pending ICPU_CFG::FDMA_CH_DISABLE.CH_DISABLE request. Bits in this field are cleared immediately when set.	0x000

1.8.9.9 ICPU_CFG:FDMA:FDMA_CH_DISABLE

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-365: FIELDS IN FDMA_CH_DISABLE

Field Name	Bit	Access	Description	Default
CH_DISABLE	9:0	One-shot	Schedules specific FDMA channels to be disabled, there is one bit per channel. The channel will finish the current DCB and then disable (after writing the DCB status word). Bits in this field is cleared either when the channel disables or by writing ICPU_CFG::FDMA_CH_ACTIVATE.CH_ACTIVATE).	0x000

1.8.9.10 ICPU_CFG:FDMA:FDMA_CH_FORCEDIS

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-366: FIELDS IN FDMA_CH_FORCEDIS

Field Name	Bit	Access	Description	Default
CH_FORCEDIS	9:0	One-shot	Immediately disable specific FDMA channels, there is one bit per channel. Unlike ICPU_CFG::FDMA_CH_DISABLE using CH_FORCEDIS will not take the state of the channel into account, if the channel is actively extracting or injecting from/to QS there is no guarantee that it will be functional after disabling the channel.	0x000

1.8.9.11 ICPU_CFG:FDMA:FDMA_CH_CNT

Parent: ICPU_CFG:FDMA

Instances: 10

TABLE 1-367: FIELDS IN FDMA_CH_CNT

Field Name	Bit	Access	Description	Default
CH_CNT_FRM	31:16	R/W	This field is incremented every time the channel saves status for a DCB that has EOF. This counter can only be modified safely when the corresponding channel is disabled (see ICPU_CFG::FDMA_CH_STAT.CH_STAT for more information).	0x0000
CH_CNT_DCB	15:8	R/W	This field is incremented every time the channel loads a DCB. This counter can be modified safely while the corresponding channel is safe (see ICPU_CFG::FDMA_CH_SAFE.CH_SAFE for more information).	0x00
CH_CNT_SIG	7:0	R/W	This field is incremented every time the channel loads a DCB that has the SIG field set. The FDMA can generate interrupt whenever this counter is incremented (see ICPU_CFG::FDMA_INTR_SIG.INTR_SIG for more information). This counter can be modified safely while the corresponding channel is safe (see ICPU_CFG::FDMA_CH_SAFE.CH_SAFE for more information).	0x00

1.8.9.12 ICPU_CFG:FDMA:FDMA_CH_INJ_TOKEN_CNT

Parent: ICPU_CFG:FDMA

Instances: 8

TABLE 1-368: FIELDS IN FDMA_CH_INJ_TOKEN_CNT

Field Name	Bit	Access	Description	Default
CH_INJ_TOKEN_CNT	7:0	R/W	Every time a channel activates with a DCB that has the TOKEN field set this counter is decremented by one. Channels that loads a DCB with the TOKEN field set cannot activate unless this counter is different from zero. This counter can be written by software, or incremented automatically by using the token tick counter (see ICPU_CFG::FDMA_CH_INJ_TOKEN_TICK_CNT for more information). This counter can be modified safely when automatic incrementing is not enabled and the corresponding injection channel is in safe mode (see ICPU_CFG::FDMA_CH_INJ_TOKEN_CNT and ICPU_CFG::FDMA_CH_SAFE.CH_SAFE for more information).	0x00

1.8.9.13 ICPU_CFG:FDMA:FDMA_CH_INJ_TOKEN_TICK_RLD

Parent: ICPU_CFG:FDMA

Instances: 8

TABLE 1-369: FIELDS IN FDMA_CH_INJ_TOKEN_TICK_RLD

Field Name	Bit	Access	Description	Default
CH_INJ_TOKEN_TICK_RLD	31:0	R/W	Automatic incrementing of the token counter is enabled by setting this field different from 0. This field holds the reload value for the ICPU_CFG::FDMA_CH_INJ_TOKEN_TICK_CNT. Note: When changing the value of this field the same value should also be written to the ICPU_CH_INJ_TOKEN_TICK_CNT field, this is needed for speeding up token counter increments when changing from a high reload value to a low reload value. 0: Token tick counter is disabled n: Add one token every n * 200ns clock cycles	0x00000000

1.8.9.14 ICPU_CFG:FDMA:FDMA_CH_INJ_TOKEN_TICK_CNT

Parent: ICPU_CFG:FDMA

Instances: 8

TABLE 1-370: FIELDS IN FDMA_CH_INJ_TOKEN_TICK_CNT

Field Name	Bit	Access	Description	Default
CH_INJ_TOKEN_TICK_CNT	31:0	R/W	Down-counter, when enabled by ICPU_CFG::FDMA_CH_INJ_TOKEN_TICK_RLD this field is decremented by one every 200ns. When zero is reached one token will be added to ICPU_CFG::FDMA_CH_INJ_TOKEN_CNT and this counted will load the value from ICPU_CFG::FDMA_CH_INJ_TOKEN_TICK_RLD (subtract one and continue decrementing from that value).	0x00000000

1.8.9.15 ICPU_CFG:FDMA:FDMA_EVT_ERR

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-371: FIELDS IN FDMA_EVT_ERR

Field Name	Bit	Access	Description	Default
EVT_ERR	9:0	Sticky	Shows if an Error-event has occurred, there is one bit per channel. See ICPU_CFG::FDMA_EVT_ERR_CODE.EVT_ERR_CODE for description of errors for which the FDMA implements run-time checks.	0x000

1.8.9.16 ICPU_CFG:FDMA:FDMA_EVT_ERR_CODE

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-372: FIELDS IN FDMA_EVT_ERR_CODE

Field Name	Bit	Access	Description	Default
EVT_ERR_CODE	3:0	R/O	This field shows information about Error-events that has been recorded by the FDMA, this can be used for software development and debugging. If multiple errors happen in succession, only the newest of the err-codes is shown. 0:Default (no error has occurred) 1:CH_ACTIVATE set for channel w. DCB_LLP==NULL 2:Got DCB w. DATAP==NULL 3:Got extraction DCB w. DATAL==0 4:Got extraction DCB w. DATAL<=BLOCKO 5:Got injection DCB w. BLOCKL==0 6:Got injection DCB w. SOF for already active channel 7:Activate attempted for channel w. error indication. 8:Activate attempted for channel enabled for manual mode. 9:Manual mode enabled for channel in active FDMA mode.	0x0

1.8.9.17 ICPU_CFG:FDMA:FDMA_INTR_LLP

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-373: FIELDS IN FDMA_INTR_LLP

Field Name	Bit	Access	Description	Default
INTR_LLP	9:0	Sticky	Shows if an LLP-event has occurred, there is one bit per channel. See the data sheet for information on when this event can occur.	0x000

1.8.9.18 ICPU_CFG:FDMA:FDMA_INTR_LLP_ENA

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-374: FIELDS IN FDMA_INTR_LLP_ENA

Field Name	Bit	Access	Description	Default
INTR_LLP_ENA	9:0	R/W	Enables LLP-event to be propagated as interrupt, there is one bit per channel. See ICPU_CFG::FDMA_INTR_LLP.INTR_LLP for additional information.	0x000

1.8.9.19 ICPU_CFG:FDMA:FDMA_INTR_FRM

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-375: FIELDS IN FDMA_INTR_FRM

Field Name	Bit	Access	Description	Default
INTR_FRM	9:0	Sticky	Shows if a FRM-event has occurred, there is one bit per channel. See the data sheet for information on when this event can occur.	0x000

1.8.9.20 ICPU_CFG:FDMA:FDMA_INTR_FRM_ENA

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-376: FIELDS IN FDMA_INTR_FRM_ENA

Field Name	Bit	Access	Description	Default
INTR_FRM_ENA	9:0	R/W	Enables FRM-event to be propagated as interrupt, there is one bit per channel. See ICPU_CFG::FDMA_INTR_FRM.INTR_FRM for additional information.	0x000

1.8.9.21 ICPU_CFG:FDMA:FDMA_INTR_SIG

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-377: FIELDS IN FDMA_INTR_SIG

Field Name	Bit	Access	Description	Default
INTR_SIG	9:0	Sticky	Shows if a SIG-event has occurred, there is one bit per channel. See the data sheet for information on when this event can occur.	0x000

1.8.9.22 ICPU_CFG:FDMA:FDMA_INTR_SIG_ENA

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-378: FIELDS IN FDMA_INTR_SIG_ENA

Field Name	Bit	Access	Description	Default
INTR_SIG_ENA	9:0	R/W	Enables SIG-event to be propagated as interrupt, there is one bit per channel. See ICPU_CFG::FDMA_INTR_SIG.INTR_SIG for additional information.	0x000

1.8.9.23 ICPU_CFG:FDMA:FDMA_INTR_ENA

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-379: FIELDS IN FDMA_INTR_ENA

Field Name	Bit	Access	Description	Default
INTR_ENA	9:0	R/W	Enables propagation of enabled channel LLP-event, FRM-event and SIG-event as interrupt, there is one bit per channel. ERR-events are always propagated when interrupt is enabled for a channel.	0x3FF

1.8.9.24 ICPU_CFG:FDMA:FDMA_INTR_IDENT

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-380: FIELDS IN FDMA_INTR_IDENT

Field Name	Bit	Access	Description	Default
INTR_IDENT	9:0	R/O	Shows currently interrupting channels, there is one bit per channel.	0x000

1.8.9.25 ICPU_CFG:FDMA:FDMA_CH_CFG

Parent: ICPU_CFG:FDMA

Instances: 10

TABLE 1-381: FIELDS IN FDMA_CH_CFG

Field Name	Bit	Access	Description	Default
CH_INJ_GRP	6	R/W	This field is only applicable to injection channels. Use this field to map the injection channel to an injection group.	0x0
CH_PRIO	5:2	R/W	The FDMA implements a strict priority scheme between all channels - both injection and extraction. Observe: The FDMA does not directly control the order in which ports are serviced in the Queuing System. In order to adjust for this (and to avoid head of line blocking) all extraction channels are automatically assigned the highest priority of the extraction channels with available data. If multiple channels are configured with equal priorities then the following strict scheme is in place: Higher channel number takes priority over lower channel number. This implies that injection takes priority over extraction.	0x0

TABLE 1-381: FIELDS IN FDMA_CH_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
DONE_STOP_ENA	1	R/W	Set this field to automatically disable the channel after completing any DCB. The channel will disable after saving DCB status. An LLP-event will be generated at the same time as the channel is disabled. Be careful when using this feature, extraction channels may head-of-line block other extraction channels if not immediately re-activated.	0x0
DONEEOF_STOP_ENA	0	R/W	Set this field to automatically disable the channel after completing any DCB with EOF indication. The channel will disable after saving DCB status. An LLP-event will be generated at the same time as the channel is disabled. Be careful when using this feature, extraction channels may head-of-line block other extraction channels if not immediately re-activated.	0x0

1.8.9.26 ICPU_CFG:FDMA:FDMA_GCFG

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-382: FIELDS IN FDMA_GCFG

Field Name	Bit	Access	Description	Default
FRM_AT_OFF	12	R/W	Set this field to make the FDMA emit FRM event for extraction channels that are disabled because of LLP=NULL.	0x0
INJ_RF_WM	11:7	R/W	Injection resync FIFO fill-level watermark, when exceeded backpressure will be asserted towards SBA. The maximum fill-level for the FIFO is reported via ICPU_CFG::FDMA_GSTAT.INJ_RF_HIGH. n: backpressure when n+1 or more words in buffer.	0x0E
RESERVED	6:3	R/W	Must be set to its default.	0xA
PD_IGNORE	0	R/W	Set this field to make the FDMA ignore the value of the DCB's PD field when injecting frames. By default the FDMA will treat the PD field in the same way as ABORT.	0x0

1.8.9.27 ICPU_CFG:FDMA:FDMA_GSTAT

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-383: FIELDS IN FDMA_GSTAT

Field Name	Bit	Access	Description	Default
INJ_RF_HIGH	10:5	R/O	This field shows the highest fill level that the injection resync FIFO has experienced since reset of the injection logic. The depth of the FIFO is 32 words, reaching a fill-level of 33 (or more) means that overflow has occurred.	0x00

1.8.9.28 ICPU_CFG:FDMA:FDMA_IDLECNT

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-384: FIELDS IN FDMA_IDLECNT

Field Name	Bit	Access	Description	Default
IDLECNT	23:0	R/O	The counter is reset whenever a channel is enabled and when FDMA moves frame data to or from the queuing system. When the FDMA is idle this counter is incremented once every 200ns. The counter saturates at maximum value (approx 3.3 seconds of idle time).	0x000000

1.8.9.29 ICPU_CFG:FDMA:FDMA_CONST

Parent: ICPU_CFG:FDMA

Instances: 1

TABLE 1-385: FIELDS IN FDMA_CONST

Field Name	Bit	Access	Description	Default
CH_INJ_CNT	15:8	R/O	The number of injection channels.	0x08
CH_XTR_CNT	7:0	R/O	The number of extraction channels.	0x02

1.8.10 ICPU_CFG:PCIE

Parent: ICPU_CFG

Instances: 1

These are VCore based registers for configuration of PCIe endpoint support logic. PCIe configuration space registers are memory mapped via the PCIE region of the Chip Registers.

TABLE 1-386: REGISTERS IN PCIE

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PCIE_CFG	0x00000004	1	PCIe endpoint configuration	Page 180
PCIE_STAT	0x00000008	1	PCIe endpoint status	Page 180
PCIE_AUX_CFG	0x0000000C	1	Auxiliary power configuration	Page 181
PCIESLV_FDMA	0x00000028	1	FDMA access into PCIe address space	Page 181

TABLE 1-386: REGISTERS IN PCIE (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PCIESLV_SBA	0x0000002C	1	SBA access into PCIe address space	Page 181
PCIEPCS_CFG	0x00000030	1	PCIe PCS configuration	Page 182
PCIE_INTR	0x00000038	1	PCIe events	Page 183
PCIE_INTR_ENA	0x0000003C	1	PCIe interrupt enable	Page 183
PCIE_INTR_IDENT	0x00000040	1	Currently active PCIe interrupts	Page 183
PCIE_INTR_COMMON_CFG	0x00000044	1	PCIe outbound interrupt configuration	Page 183
PCIE_INTR_CFG	0x00000048	2 0x00000004	PCIe outbound MSI interrupt configuration	Page 184

1.8.10.1 ICPU_CFG:PCIE:PCIE_CFG

Parent: ICPU_CFG:PCIE

Instances: 1

TABLE 1-387: FIELDS IN PCIE_CFG

Field Name	Bit	Access	Description	Default
PCIE_BAR_WR_ENA	2	R/W	Set this field to enable write of PCIe BAR masks via PCIE register target. Only registers PCIE::BAR0, PCIE::BAR1, and PCIE::BAR2 may be written while this field is set. The minimum size for Memory and IO BARs are 64K (mask 0xFFFF). Note: The low 4 bits of all BARs can be written via the PCIe target when this field is not set.	0x0
LTSSM_DIS	1	R/W	Set this field to disable initialization of the PCIe link. By default the PCIe core will start up and try to achieve link when the SERDES is started, by setting this field before starting the SERDES it is possible to make changes to the PCIe configuration/registers prior to linking with the root complex.	0x0
MEM_RING_CORE_ENA	0	R/W	Set to add the PCIe core memories to the RAM integrity ring.	0x0

1.8.10.2 ICPU_CFG:PCIE:PCIE_STAT

Parent: ICPU_CFG:PCIE

Instances: 1

TABLE 1-388: FIELDS IN PCIE_STAT

Field Name	Bit	Access	Description	Default
PM_STATE	2:0	R/O	The current power management state of the PCIe core. 0: D0 1: D1 2: D2 3: D3 4: D0-Uninitialized	0x4

1.8.10.3 ICPU_CFG:PCIE:PCIE_AUX_CFG

Parent: ICPU_CFG:PCIE

Instances: 1

TABLE 1-389: FIELDS IN PCIE_AUX_CFG

Field Name	Bit	Access	Description	Default
AUX_POWER_VAL	0	R/W	Set to force "detection" of PCIe auxiliary power.	0x1

1.8.10.4 ICPU_CFG:PCIE:PCIESLV_FDMA

Parent: ICPU_CFG:PCIE

Instances: 1

TABLE 1-390: FIELDS IN PCIESLV_FDMA

Field Name	Bit	Access	Description	Default
FDMA_OFFSET	1:0	R/W	The FDMA has access to one 1GByte region (0xC0000000 though 0xFFFFFFFF) that maps accesses to PCIe interface. The value of this field is used for address-bits [31:30] towards the PCIe endpoint. Set this field to 1.	0x0

1.8.10.5 ICPU_CFG:PCIE:PCIESLV_SBA

Parent: ICPU_CFG:PCIE

Instances: 1

TABLE 1-391: FIELDS IN PCIESLV_SBA

Field Name	Bit	Access	Description	Default
SBA_BE	27:24	R/W	This field allows configuration of outbound PCIe-transaction Byte-Enable field. This is applied to all SBA (non-FDMA) initiated outbound PCIe accesses. This field is not used for TYPE=MRr/MWr/MRdLk accesses. Byte-enables are needed in order to support Zero-byte and non-contiguous byte IO and CFG transfers and Zero-byte Messages.	0x0
SBA_MSG_CODE	22:15	R/W	This field allows configuration of outbound PCIe-transaction MSG field. This is applied to all SBA (non-FDMA) initiated outbound PCIe accesses.	0x00
SBA_TC	14:12	R/W	This field allows configuration of outbound PCIe-transaction TC field. This is applied to all SBA (non-FDMA) initiated outbound PCIe accesses.	0x0
SBA_EP	8	R/W	This field allows configuration of outbound PCIe-transaction EP field. This is applied to all SBA (non-FDMA) initiated outbound PCIe accesses.	0x0
SBA_OFFSET	1:0	R/W	SBA masters (non-FDMA) has access to one 1GByte region (0xC0000000 though 0xFFFFFFFF) that maps accesses to PCIe interface. The value of this field is used for address-bits [31:30] towards the PCIe end-point. Set this field to 0.	0x0

1.8.10.6 ICPU_CFG:PCIE:PCIEPCS_CFG

Parent: ICPU_CFG:PCIE

Instances: 1

TABLE 1-392: FIELDS IN PCIEPCS_CFG

Field Name	Bit	Access	Description	Default
RESERVED	7:5	R/W	Must be set to its default.	0x2
WAKE_POL	2	R/W	Polarity of the PCIe WAKE output, WAKE is typically an active low output - but if an amplifier is needed for driving a large WAKE net then polarity may need to be changed. 0: Active low 1: Active high	0x0
WAKE_OE	1	R/W	Set to permanently drive PCIe WAKE output, by default the WAKE output is only driven when active and thusly allowing pull-resistor network. 0: Only drive output when active. 1: Always drive output.	0x0

TABLE 1-392: FIELDS IN PCIEPCS_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
BEACON_DIS	0	R/W	Set this field to disable outband PCIe beacon signaling when attempting to wake from D3. When beacon is disabled the WAKE# signal (available as alternate GPIO function) must be used instead.	0x0

1.8.10.7 ICPU_CFG:PCIE:PCIE_INTR

Parent: ICPU_CFG:PCIE

Instances: 1

TABLE 1-393: FIELDS IN PCIE_INTR

Field Name	Bit	Access	Description	Default
INTR_PM_STATE	0	Sticky	This event is set whenever the ICPU_CFG::PCIE_STAT.PM_STATE field is changed.	0x0

1.8.10.8 ICPU_CFG:PCIE:PCIE_INTR_ENA

Parent: ICPU_CFG:PCIE

Instances: 1

TABLE 1-394: FIELDS IN PCIE_INTR_ENA

Field Name	Bit	Access	Description	Default
INTR_PM_STATE_ENA	0	R/W	Set to enable propagation of the PM_STATE interrupt.	0x0

1.8.10.9 ICPU_CFG:PCIE:PCIE_INTR_IDENT

Parent: ICPU_CFG:PCIE

Instances: 1

TABLE 1-395: FIELDS IN PCIE_INTR_IDENT

Field Name	Bit	Access	Description	Default
INTR_PM_STATE_IDENT	0	R/O	Set if the PM_STATE interrupt is currently active.	0x0

1.8.10.10 ICPU_CFG:PCIE:PCIE_INTR_COMMON_CFG

Parent: ICPU_CFG:PCIE

Instances: 1

TABLE 1-396: FIELDS IN PCIE_INTR_COMMON_CFG

Field Name	Bit	Access	Description	Default
WAKEUP_ON_INTR_DIS	2	R/W	Set to disable wake-up on interrupt. By default the PCIe endpoint will attempt to wake up from powerdown when a change in interrupt state is detected.	0x0

TABLE 1-396: FIELDS IN PCIE_INTR_COMMON_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
LEGACY_MODE_INTR_SEL	1	R/W	Select the external interrupt from the VCore interrupt controller that must be used to generate PCIe legacy interrupt. 0: Use EXT_DST0 1: Use EXT_DST1	0x1
PCIE_INTR_ENA	0	R/W	Set to enable PCIe interrupts. The PCIe endpoint's MSI Capability Register Set must have been configured before enabling interrupts.	0x0

1.8.10.11 ICPU_CFG:PCIE:PCIE_INTR_CFG

Parent: ICPU_CFG:PCIE

Instances: 2

Replicated per EXT_DST interrupt.

TABLE 1-397: FIELDS IN PCIE_INTR_CFG

Field Name	Bit	Access	Description	Default
TRAFFIC_CLASS	14:12	R/W	Configure MSI interrupt traffic class for corresponding EXT_DST interrupt.	0x0
FALLING_VECTOR_VAL	11:7	R/W	Configure MSI interrupt vector for falling edge of corresponding EXT_DST interrupt.	0x00
RISING_VECTOR_VAL	6:2	R/W	Configure MSI interrupt vector for rising edge of corresponding EXT_DST interrupt.	0x00
INTR_FALLING_ENA	1	R/W	Set to enable MSI interrupt on falling edge of corresponding EXT_DST interrupt.	0x0
INTR_RISING_ENA	0	R/W	Set to enable MSI interrupt on rising edge of corresponding EXT_DST interrupt.	0x0

1.8.11 ICPU_CFG:MANUAL_XTRINJ

Parent: ICPU_CFG

Instances: 1

This group contains replicated register array for doing manual Extraction and Injection by use of the FDMA engine.

TABLE 1-398: REGISTERS IN MANUAL_XTRINJ

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MANUAL_XTR	0x00000000	4096 0x00000004	Manual extraction replicated register-array	Page 185
MANUAL_INJ	0x00004000	4096 0x00000004	Manual injection replicated register-array	Page 185
MANUAL_CFG	0x00008000	1	Manual extraction and injection configuration	Page 185
MANUAL_INTR	0x00008004	1	Manual extraction and injection interrupt indications	Page 186
MANUAL_INTR_ENA	0x00008008	1	Manual extraction and injection interrupt enables	Page 186

1.8.11.1 ICPU_CFG:MANUAL_XTRINJ:MANUAL_XTR

Parent: ICPU_CFG:MANUAL_XTRINJ

Instances: 4096

TABLE 1-399: FIELDS IN MANUAL_XTR

Field Name	Bit	Access	Description	Default
XTR	31:0	R/W	Manual extraction is done by reading from this block of registers. The manual extraction status word is accessed by reading the last word-address in this block. Manual extraction has to be enabled via ICPU_CFG::MANUAL_CFG.XTR_ENA.	0x00000000

1.8.11.2 ICPU_CFG:MANUAL_XTRINJ:MANUAL_INJ

Parent: ICPU_CFG:MANUAL_XTRINJ

Instances: 4096

TABLE 1-400: FIELDS IN MANUAL_INJ

Field Name	Bit	Access	Description	Default
INJ	31:0	R/W	Manual injection is done by writing to this block of registers. The manual injection status word is located at the first word-address in this block. Manual injection has to be enabled via ICPU_CFG::MANUAL_CFG.INJ_ENA.	0x00000000

1.8.11.3 ICPU_CFG:MANUAL_XTRINJ:MANUAL_CFG

Parent: ICPU_CFG:MANUAL_XTRINJ

Instances: 1

TABLE 1-401: FIELDS IN MANUAL_CFG

Field Name	Bit	Access	Description	Default
INJ_SWAP_ENA	3	R/W	Set to swap endianness of data injected to the MANUAL_INJ region. The manual injection status word is never swapped.	0x0
XTR_SWAP_ENA	2	R/W	Set to byte-swap endianness of data extracted from the MANUAL_XTR region. The manual extraction status word is never swapped.	0x0
INJ_ENA	1	R/W	Set to enable manual injection by using FDMA channel number 9. When manual injection is enabled; the FDMA cannot be used for regular FDMA injection operations (on any injection channel).	0x0
XTR_ENA	0	R/W	Set to enable manual extraction by using FDMA channel number 1. When manual extraction is enabled; the FDMA cannot be used for regular FDMA extraction operations (on any extraction channel).	0x0

1.8.11.4 ICPU_CFG:MANUAL_XTRINJ:MANUAL_INTR

Parent: ICPU_CFG:MANUAL_XTRINJ

Instances: 1

TABLE 1-402: FIELDS IN MANUAL_INTR

Field Name	Bit	Access	Description	Default
INTR_INJ_RDY	2	R/O	Set when there is room for more injection data-words in injection fifo.	0x0
INTR_XTR_ANY_RDY	1	R/O	Set when any extraction word is ready for extraction.	0x0
INTR_XTR_SOF_RDY	0	R/O	Set when there is an extraction word containing SOF ready for extraction.	0x0

1.8.11.5 ICPU_CFG:MANUAL_XTRINJ:MANUAL_INTR_ENA

Parent: ICPU_CFG:MANUAL_XTRINJ

Instances: 1

TABLE 1-403: FIELDS IN MANUAL_INTR_ENA

Field Name	Bit	Access	Description	Default
INTR_INJ_RDY_ENA	2	R/W	Set to enable FDMA interrupt while there is room for more injection data. This interrupt is asserted for as long as there is free space in the injection buffers.	0x0
INTR_XTR_ANY_RDY_ENA	1	R/W	Set to enable FDMA interrupt while any data is ready for manual extraction. This interrupt is asserted for as long as there is data ready in the extraction buffer.	0x0
INTR_XTR_SOF_RDY_ENA	0	R/W	Set to enable FDMA interrupt when a new frame is waiting to be extracted. This event is asserted when a frame-word with sof set is waiting to be extracted. If a previous frame is only partially extracted then no interrupt will be generated until the previous frame is completely extracted.	0x0

1.9 VCAP_CORE

TABLE 1-404: REGISTER GROUPS IN VCAP_CORE

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
VCAP_CORE_CFG	0x00000000	1	VCAP operations	Page 186
VCAP_CORE_CACHE	0x00000008	1	VCAP cache	Page 189
VCAP_CORE_MAP	0x0000038C	1	Mapping of cores to interfaces	Page 191
TCAM_BIST	0x000003C0	1	Build in test for TCAM	Page 192

1.9.1 VCAP_CORE:VCAP_CORE_CFG

Parent: VCAP_CORE

Instances: 1

TABLE 1-405: REGISTERS IN VCAP_CORE_CFG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
VCAP_UPDATE_CTRL	0x00000000	1	Initiation of read/write/move/ initialization operations	Page 187
VCAP_MV_CFG	0x00000004	1	Configuration for move/initial-ization	Page 189

1.9.1.1 VCAP_CORE:VCAP_CORE_CFG:VCAP_UPDATE_CTRL

Parent: VCAP_CORE:VCAP_CORE_CFG

Instances: 1

Operations on the VCAP cache is done via this register. The UPDATE_CMD field specifies the operation to perform when UPDATE_SHOT is set. For all of the operations it is possible to disable read/write of entries, actions, and/or counter by setting VCAP_UPDATE_CTRL.UPDATE_ENTRY_DIS, VCAP_UPDATE_CTRL.UPDATE_ACTION_DIS, and/or VCAP_UPDATE_CTRL.UPDATE_CNT_DIS respectively. Writing/moving to unimplemented addresses are ignored. Reading/moving from unimplemented addresses returns never-match for entries, and zeros from actions/ counters.

Active rules may only be written to empty (initialized) addresses. Software must not overwrite active rules (unless when initializing rules). To initialize a region of addresses use the init operation with CLEAR_CACHE bits set to '1'. Move operations automatically disable rules when moved; so it is OK when source and destination ranges overlap.

TABLE 1-406: FIELDS IN VCAP_UPDATE_CTRL

Field Name	Bit	Access	Description	Default
UPDATE_CMD	24:22	R/W	Write and read operations access VCAP memory at address specified by UPDATE_ADDR. Move up operation moves one or more VCAP addresses from a high address to a lower address, this is equivalent to decreasing priority of a rule. The starting address is specified by UPDATE_ADDR, the number of addresses (the range) that is moved is defined by VCAP_MV_CFG.MV_SIZE, the distance to move is defined by VCAP_MV_CFG. MV_NUM_POS. Move down operation moves one or more VCAP addresses from a low address to a higher address, this is equivalent to increasing priority of a rule. This operation is equivalent to "Move up" except for the direction that it moves addresses, see "Move up" for more details. Init operation writes the contents of the cache to one or more VCAP addresses. The starting address is specified by UPDATE_ADDR, the number of addresses (the range) that is written is defined by VCAP_MV_CFG.MV_SIZE. Setting CLEAR_CACHE at the same time as starting the operation will clear the cache and cause the init operation to initialize the range of addresses. 000: Write from cache to VCAP 001: Read from VCAP to cache 010: Move entry and/or action up (decreasing addresses) 011: Move entry and/or action down (increasing addresses) 100: Initialize VCAP with the cache-value	0x0
UPDATE_ENTRY_DIS	21	R/W	Set to disable update of entries for VCAP operations: For read-operations entry-cache will remain unchanged. For write/move/init operations the VCAP-entry will remain unchanged.	0x0
UPDATE_ACTION_DIS	20	R/W	Set to disable update of actions for VCAP operations: For read-operations action-cache will remain unchanged. For write/move/init operations the VCAP-action will remain unchanged.	0x0
UPDATE_CNT_DIS	19	R/W	Set to disable update of counter for VCAP operations: For read-operations counter-cache will remain unchanged. For write/init operations the VCAP-counter will remain unchanged. For move operations the destination VCAP-counters will be set to zeros.	0x0
UPDATE_ADDR	18:3	R/W	The address to access for VCAP operations.	0x0000

TABLE 1-406: FIELDS IN VCAP_UPDATE_CTRL (CONTINUED)

Field Name	Bit	Access	Description	Default
UPDATE_SHOT	2	One-shot	Set to initiate the operation specified in UPDATE_CMD. This bit is automatically cleared by hardware when the operation is finished. Software must not change write fields in the VCAP target while this field is set (while operation is active.)	0x0
CLEAR_CACHE	1	One-shot	Set to clear the cache. This field is cleared immediately by hardware (at the same time as clearing the cache). The contents of the cache will be set to disabled/empty.	0x0

1.9.1.2 VCAP_CORE:VCAP_CORE_CFG:VCAP_MV_CFG

Parent: VCAP_CORE:VCAP_CORE_CFG

Instances: 1

TABLE 1-407: FIELDS IN VCAP_MV_CFG

Field Name	Bit	Access	Description	Default
MV_NUM_POS	31:16	R/W	Specifies the distance during move operations. I.e. if this field is set to 4 for a move-down operation, then source address n is moved to destination address n+5. 0: Distance is one position 1: Distance is two positions n: Distance is n+1 positions	0x0000
MV_SIZE	15:0	R/W	Specifies the number of addresses to move/initialize during move/init operations. 0: Address VCAP_UPDATE_CTRL.UPDATE_ADDR is moved/initialized n: Addresses VCAP_UPDATE_CTRL.UPDATE_ADDR through VCAP_UPDATE_CTRL.UPDATE_ADDR+n are moved/initialized	0x0000

1.9.2 VCAP_CORE:VCAP_CORE_CACHE

Parent: VCAP_CORE

Instances: 1

TABLE 1-408: REGISTERS IN VCAP_CORE_CACHE

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
VCAP_ENTRY_DAT	0x00000000	64 0x00000004	Entry data cache	Page 190
VCAP_MASK_DAT	0x00000100	64 0x00000004	Entry mask cache	Page 190
VCAP_ACTION_DAT	0x00000200	64 0x00000004	Action cache	Page 190

TABLE 1-408: REGISTERS IN VCAP_CORE_CACHE (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
VCAP_CNT_DAT	0x00000300	32 0x00000004	Counter cache	Page 191
VCAP_TG_DAT	0x00000380	1	Entry type-group	Page 191

1.9.2.1 VCAP_CORE:VCAP_CORE_CACHE:VCAP_ENTRY_DAT

Parent: VCAP_CORE:VCAP_CORE_CACHE

Instances: 64

TABLE 1-409: FIELDS IN VCAP_ENTRY_DAT

Field Name	Bit	Access	Description	Default
ENTRY_DAT	31:0	R/W	The cache register that holds entry data. The register is replicated; index 0 is the 32 LSBs of the entry-data. Together with VCAP_MASK_DAT.MASK_-DAT this field defines match parameters for TCAM entries. Version 2 VCAPs allows programming of never-match, this is needed when disabling entries. Version 1 VCAPs converts match-off to match-any when reading/writing entries. Match-0: Entry=0, Mask=0 Match-1: Entry=1, Mask=0 Match-any (don't care): Entry=0, Mask=1 Match-off (never-match): Entry=1, Mask=1	0x00000000

1.9.2.2 VCAP_CORE:VCAP_CORE_CACHE:VCAP_MASK_DAT

Parent: VCAP_CORE:VCAP_CORE_CACHE

Instances: 64

TABLE 1-410: FIELDS IN VCAP_MASK_DAT

Field Name	Bit	Access	Description	Default
MASK_DAT	31:0	R/W	The cache register that holds entry mask. The register is replicated; index 0 is the 32 LSBs of the entry-mask. See VCAP_MASK_DAT.MASK_DAT for encoding information.	0x00000000

1.9.2.3 VCAP_CORE:VCAP_CORE_CACHE:VCAP_ACTION_DAT

Parent: VCAP_CORE:VCAP_CORE_CACHE

Instances: 64

TABLE 1-411: FIELDS IN VCAP_ACTION_DAT

Field Name	Bit	Access	Description	Default
ACTION_DAT	31:0	R/W	The cache register that holds action. The register is replicated; index 0 is the 32 LSBs of the action.	0x00000000

1.9.2.4 VCAP_CORE:VCAP_CORE_CACHE:VCAP_CNT_DAT

Parent: VCAP_CORE:VCAP_CORE_CACHE

Instances: 32

TABLE 1-412: FIELDS IN VCAP_CNT_DAT

Field Name	Bit	Access	Description	Default
CNT_DAT	31:0	R/W	The cache register that holds counter. The register is replicated; index 0 is the 32 LSBs of the counter. When the counter is 1 bit wide the counter operates as a 1 bit saturating counter; it is set by VCAP when a rule is matched by a key.	0x00000000

1.9.2.5 VCAP_CORE:VCAP_CORE_CACHE:VCAP_TG_DAT

Parent: VCAP_CORE:VCAP_CORE_CACHE

Instances: 1

TABLE 1-413: FIELDS IN VCAP_TG_DAT

Field Name	Bit	Access	Description	Default
TG_DAT	31:0	R/W	This cache register holds the TypeGroup id for each subword in the TCAM. TypeGroup ids are place back to back with subword 0 at the LSBs when VCAP supports multiple sub-words. This field applies only to version 1 VCAPs, for version 2 VCAPs it is not implemented and reading it will return zeros.	0x00000000

1.9.3 VCAP_CORE:VCAP_CORE_MAP

Parent: VCAP_CORE

Instances: 1

TABLE 1-414: REGISTERS IN VCAP_CORE_MAP

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
VCAP_CORE_IDX	0x00000000	1	Core index	Page 192
VCAP_CORE_MAP	0x00000004	1	Mapping of core	Page 192

1.9.3.1 VCAP_CORE:VCAP_CORE_MAP:VCAP_CORE_IDX

Parent: VCAP_CORE:VCAP_CORE_MAP

Instances: 1

TABLE 1-415: FIELDS IN VCAP_CORE_IDX

Field Name	Bit	Access	Description	Default
CORE_IDX	3:0	R/W	Set to index of specific core to access the mapping of that core via VCAP_CORE::VCAP_CORE_MAP.	0x0

1.9.3.2 VCAP_CORE:VCAP_CORE_MAP:VCAP_CORE_MAP

Parent: VCAP_CORE:VCAP_CORE_MAP

Instances: 1

TABLE 1-416: FIELDS IN VCAP_CORE_MAP

Field Name	Bit	Access	Description	Default
CORE_MAP	2:0	R/W	Configure ownership of core n (defined by VCAP_CORE::VCAP_CORE_IDX). When a core is mapped to a specific VCAP; lookups for that VCAP will be applied to the core. VCAP priority is still observed, a match in two cores will only cause the most significant rule to be "hit" (highest address.) After reset all cores are in power-save mode. TBD	0x0

1.9.4 VCAP_CORE:TCAM_BIST

Parent: VCAP_CORE

Instances: 1

TABLE 1-417: REGISTERS IN TCAM_BIST

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
TCAM_CTRL	0x00000000	1	Control of the TCAM	Page 192
TCAM_STAT	0x00000008	1	Status for the TCAM	Page 193

1.9.4.1 VCAP_CORE:TCAM_BIST:TCAM_CTRL

Parent: VCAP_CORE:TCAM_BIST

Instances: 1

TABLE 1-418: FIELDS IN TCAM_CTRL

Field Name	Bit	Access	Description	Default
TCAM_BIST	1	One-shot	Set this field to start manual BIST of the TCAM. This field will be cleared once BIST is complete. The BIST procedure requires that the TCAM is initialized before start, setting TCAM_INIT at the same time as setting this field will first initialize the TCAM and then run BIST.	0x0
TCAM_INIT	0	One-shot	Set this field to start manual initialization of the TCAM. This field is cleared once initialization is complete. The TCAM has random contents after reset and must be initialized prior to usage.	0x0

1.9.4.2 VCAP_CORE:TCAM_BIST:TCAM_STAT

Parent: VCAP_CORE:TCAM_BIST

Instances: 1

TABLE 1-419: FIELDS IN TCAM_STAT

Field Name	Bit	Access	Description	Default
BIST_ERR	2	R/O	Set if BIST failed.	0x0
BIST_BUSY	1	R/O	Set while BIST is running. When checking the BIST result this field must be cleared.	0x0
TCAM_RDY	0	R/O	Indicates the current operational state of the TCAM. '0': Busy with initialization. '1': Ready to be used.	0x0

1.10 PCIE

TABLE 1-420: REGISTER GROUPS IN PCIE

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
PCIE_TYPE0_HDR	0x00000000	1	PCIe Header Type 0	Page 193
PCIE_PM_CAP	0x00000040	1	PCIe Power Management Interface	Page 198
PCIE_MSI_CAP	0x00000050	1	PCIe Message Signaled Interrupts	Page 199
PCIE_CAP	0x00000070	1	PCIe Capability Register Set	Page 200
PCIE_AER_CAP	0x00000100	1	PCIe Advanced Error Capability and Control	Page 205
PCIE_PORT_LOGIC	0x00000700	1	PCIe Port Logic	Page 209

1.10.1 PCIE:PCIE_TYPE0_HDR

Parent: PCIE

Instances: 1

TABLE 1-421: REGISTERS IN PCIE_TYPE0_HDR

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
DEVICE_ID_VENDOR_ID	0x00000000	1	Word offset 0	Page 194
STATUS_COMMAND	0x00000004	1	Word offset 1	Page 194
CLASS_CODE_REVISION_ID	0x00000008	1	Word offset 2	Page 195
BIST_HEADER_TYPE_LATENCY_CACHE_LINE_SIZE	0x0000000C	1	Word offset 3	Page 195
BAR0	0x00000010	1	Word offset 4	Page 195
BAR1	0x00000014	1	Word offset 5	Page 196
BAR2	0x00000018	1	Word offset 6	Page 196
BAR3	0x0000001C	1	Word offset 7	Page 196
BAR4	0x00000020	1	Word offset 8	Page 196
BAR5	0x00000024	1	Word offset 9	Page 197
CARDBUS_CIS_PTR	0x00000028	1	Word offset 10	Page 197
SUBSYSTEM_ID_SUBSYSTEM_VENDOR_ID	0x0000002C	1	Word offset 11	Page 197
EXP_ROM_BASE_ADDR	0x00000030	1	Word offset 12	Page 197
PCI_CAP_PTR	0x00000034	1	Word offset 13	Page 198
MAX_LATENCY_MIN_GRANT_INTERRUPT_PIN_INTERRUPT_LINE	0x0000003C	1	Word offset 15	Page 198

1.10.1.1 PCIE:PCIE_TYPE0_HDR:DEVICE_ID_VENDOR_ID

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-422: FIELDS IN DEVICE_ID_VENDOR_ID

Field Name	Bit	Access	Description	Default
PCI_TYPE0_DEVICE_ID	31:16	R/W		0xB005
PCI_TYPE0_VENDOR_ID	15:0	R/W		0x101B

1.10.1.2 PCIE:PCIE_TYPE0_HDR:STATUS_COMMAND

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-423: FIELDS IN STATUS_COMMAND

Field Name	Bit	Access	Description	Default
DETECTED_PARITY_ERR	31	One-shot		0x0
SIGNALED_SYS_ERR	30	One-shot		0x0
RCVD_MASTER_ABORT	29	One-shot		0x0
RCVD_TARGET_ABORT	28	One-shot		0x0
SIGNALED_TARGET_ABORT	27	One-shot		0x0
DEV_SEL_TIMING	26:25	R/O		0x0

TABLE 1-423: FIELDS IN STATUS_COMMAND (CONTINUED)

Field Name	Bit	Access	Description	Default
MASTER_DPE	24	One-shot		0x0
FAST_B2B_CAP	23	R/O		0x0
FAST_66MHZ_CAP	21	R/O		0x0
CAP_LIST	20	R/O		0x1
INT_STATUS	19	One-shot		0x0
PCI_TYPE_RESERV	16:11	R/O		0x00
PCI_TYPE0_INT_EN	10	R/W		0x0
PCI_TYPE0_SERREN	8	R/W		0x0
PCI_TYPE_IDSEL_STEPPING	7	R/O		0x0
PCI_TYPE0_PARITY_ERR_EN	6	R/W		0x0
PCI_TYPE_VGA_PAL-ETTE_SNOOP	5	R/O		0x0
PCI_TYPE_MWI_ENABLE	4	R/O		0x0
PCI_TYPE0_SPECIAL_CY-CLE_OPERATION	3	R/O		0x0
PCI_TYPE0_BUS_MASTER_EN	2	R/W		0x0
PCI_TYPE0_MEM_SPACE_EN	1	R/W		0x0
PCI_TYPE0_IO_EN	0	R/W		0x0

1.10.1.3 PCIE:PCIE_TYPE0_HDR:CLASS_CODE_REVISION_ID

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-424: FIELDS IN CLASS_CODE_REVISION_ID

Field Name	Bit	Access	Description	Default
BASE_CLASS_CODE	31:24	R/W		0x02
SUBCLASS_CODE	23:16	R/W		0x80
PROGRAM_INTERFACE	15:8	R/W		0x00
REVISION_ID	7:0	R/W		0x00

1.10.1.4 PCIE:PCIE_TYPE0_HDR:BIST_HEADER_TYPE_LATENCY_CACHE_LINE_SIZE

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-425: FIELDS IN BIST_HEADER_TYPE_LATENCY_CACHE_LINE_SIZE

Field Name	Bit	Access	Description	Default
BIST	31:24	R/O		0x00
MULTI_FUNC	23	R/W		0x0
HEADER_TYPE	22:16	R/O		0x00
LATENCY_MASTER_TIMER	15:8	R/O		0x00
CACHE_LINE_SIZE	7:0	R/W		0x00

1.10.1.5 PCIE:PCIE_TYPE0_HDR:BAR0

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-426: FIELDS IN BAR0

Field Name	Bit	Access	Description	Default
BAR0_START	31:4	R/W		0x0000000
BAR0_PREFETCH	3	R/W		0x0
BAR0_TYPE	2:1	R/W		0x0
BAR0_MEM_IO	0	R/W		0x0

1.10.1.6 PCIE:PCIE_TYPE0_HDR:BAR1

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-427: FIELDS IN BAR1

Field Name	Bit	Access	Description	Default
BAR1_START	31:4	R/W		0x0000000
BAR1_PREFETCH	3	R/O		0x0
BAR1_TYPE	2:1	R/O		0x0
BAR1_MEM_IO	0	R/O		0x0

1.10.1.7 PCIE:PCIE_TYPE0_HDR:BAR2

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-428: FIELDS IN BAR2

Field Name	Bit	Access	Description	Default
BAR2_START	31:4	R/W		0x0000000
BAR2_PREFETCH	3	R/W		0x0
BAR2_TYPE	2:1	R/W		0x0
BAR2_MEM_IO	0	R/W		0x0

1.10.1.8 PCIE:PCIE_TYPE0_HDR:BAR3

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-429: FIELDS IN BAR3

Field Name	Bit	Access	Description	Default
BAR3_START	31:4	R/W		0x0000000
BAR3_PREFETCH	3	R/O		0x0
BAR3_TYPE	2:1	R/O		0x0
BAR3_MEM_IO	0	R/O		0x0

1.10.1.9 PCIE:PCIE_TYPE0_HDR:BAR4

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-430: FIELDS IN BAR4

Field Name	Bit	Access	Description	Default
BAR4_START	31:4	R/W		0x0000000
BAR4_PREFETCH	3	R/W		0x0
BAR4_TYPE	2:1	R/W		0x0
BAR4_MEM_IO	0	R/W		0x0

1.10.1.10 PCIE:PCIE_TYPE0_HDR:BAR5

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-431: FIELDS IN BAR5

Field Name	Bit	Access	Description	Default
BAR5_START	31:4	R/W		0x0000000
BAR5_PREFETCH	3	R/O		0x0
BAR5_TYPE	2:1	R/O		0x0
BAR5_MEM_IO	0	R/O		0x0

1.10.1.11 PCIE:PCIE_TYPE0_HDR:CARDBUS_CIS_PTR

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-432: FIELDS IN CARDBUS_CIS_PTR

Field Name	Bit	Access	Description	Default
CARDBUS_CIS_POINTER	31:0	R/W		0x00000000

1.10.1.12 PCIE:PCIE_TYPE0_HDR:SUBSYSTEM_ID_SUBSYSTEM_VENDOR_ID

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-433: FIELDS IN SUBSYSTEM_ID_SUBSYSTEM_VENDOR_ID

Field Name	Bit	Access	Description	Default
SUBSYS_DEV_ID	31:16	R/W		0x0000
SUBSYS_VENDOR_ID	15:0	R/W		0x101B

1.10.1.13 PCIE:PCIE_TYPE0_HDR:EXP_ROM_BASE_ADDR

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-434: FIELDS IN EXP_ROM_BASE_ADDR

Field Name	Bit	Access	Description	Default
EXP_ROM_BASE_ADDRESS	31:11	R/W		0x000000
ROM_BAR_ENABLE	0	R/O		0x0

1.10.1.14 PCIE:PCIE_TYPE0_HDR:PCI_CAP_PTR

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-435: FIELDS IN PCI_CAP_PTR

Field Name	Bit	Access	Description	Default
CAP_POINTER	7:0	R/W		0x40

1.10.1.15 PCIE:PCIE_TYPE0_HDR:MAX_LATENCY_MIN_GRANT_INTERRUPT_PIN_INTERRUPT_LINE

Parent: PCIE:PCIE_TYPE0_HDR

Instances: 1

TABLE 1-436: FIELDS IN MAX_LATENCY_MIN_GRANT_INTERRUPT_PIN_INTERRUPT_LINE

Field Name	Bit	Access	Description	Default
INT_PIN	15:8	R/W		0x01
INT_LINE	7:0	R/W		0xFF

1.10.2 PCIE:PCIE_PM_CAP

Parent: PCIE

Instances: 1

TABLE 1-437: REGISTERS IN PCIE_PM_CAP

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CAP_ID_NXT_PTR	0x00000000	1	Word offset 0	Page 198
CON_STATUS	0x00000004	1	Word offset 1	Page 199

1.10.2.1 PCIE:PCIE_PM_CAP:CAP_ID_NXT_PTR

Parent: PCIE:PCIE_PM_CAP

Instances: 1

TABLE 1-438: FIELDS IN CAP_ID_NXT_PTR

Field Name	Bit	Access	Description	Default
PME_SUPPORT	31:27	R/W		0x1B
D2_SUPPORT	26	R/W		0x0
D1_SUPPORT	25	R/W		0x1

TABLE 1-438: FIELDS IN CAP_ID_NXT_PTR (CONTINUED)

Field Name	Bit	Access	Description	Default
AUX_CURR	24:22	R/W		0x1
DSI	21	R/W		0x1
PME_CLK	19	R/O		0x0
PM_SPEC_VER	18:16	R/W		0x3
PM_NEXT_POINTER	15:8	R/W		0x50
PM_CAP_ID	7:0	R/O		0x01

1.10.2.2 PCIE:PCIE_PM_CAP:CON_STATUS

Parent: PCIE:PCIE_PM_CAP

Instances: 1

TABLE 1-439: FIELDS IN CON_STATUS

Field Name	Bit	Access	Description	Default
DATA_REG_ADD_INFO	31:24	R/O		0x00
BUS_PWR_CLK_CON_EN	23	R/O		0x0
B2_B3_SUPPORT	22	R/O		0x0
PME_STATUS	15	One-shot		0x0
DATA_SCALE	14:13	R/O		0x0
DATA_SELECT	12:9	R/O		0x0
PME_ENABLE	8	R/W		0x0
NO_SOFT_RST	3	R/W		0x0
POWER_STATE	1:0	R/W		0x0

1.10.3 PCIE:PCIE_MSI_CAP

Parent: PCIE

Instances: 1

TABLE 1-440: REGISTERS IN PCIE_MSI_CAP

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PCI_MSI_CAP_ID_NEXT_CTRL	0x00000000	1	Word offset 0	Page 199
MSI_LOWER_32	0x00000004	1	Word offset 1	Page 200
MSI_UPPER_32	0x00000008	1	Word offset 2	Page 200
MSI_PENDING_BIT	0x00000014	1	Word offset 5	Page 200

1.10.3.1 PCIE:PCIE_MSI_CAP:PCI_MSI_CAP_ID_NEXT_CTRL

Parent: PCIE:PCIE_MSI_CAP

Instances: 1

TABLE 1-441: FIELDS IN PCI_MSI_CAP_ID_NEXT_CTRL

Field Name	Bit	Access	Description	Default
PCI_PVM_SUPPORT	24	R/O		0x0

TABLE 1-441: FIELDS IN PCI_MSI_CAP_ID_NEXT_CTRL (CONTINUED)

Field Name	Bit	Access	Description	Default
PCI_MSI_64_BIT_ADDR_CAP	23	R/W		0x1
PCI_MSI_MULTIPLE_MSG_EN	22:20	R/W		0x0
PCI_MSI_MULTIPLE_MSG_CAP	19:17	R/W		0x2
PCI_MSI_ENABLE	16	R/W		0x0
PCI_MSI_CAP_NEXT_OFFSET	15:8	R/W		0x70
PCI_MSI_CAP_ID	7:0	R/O		0x05

1.10.3.2 PCIE:PCIE_MSI_CAP:MSI_LOWER_32

Parent: PCIE:PCIE_MSI_CAP

Instances: 1

TABLE 1-442: FIELDS IN MSI_LOWER_32

Field Name	Bit	Access	Description	Default
PCI_MSI_LOWER_32	31:2	R/W		0x00000000

1.10.3.3 PCIE:PCIE_MSI_CAP:MSI_UPPER_32

Parent: PCIE:PCIE_MSI_CAP

Instances: 1

TABLE 1-443: FIELDS IN MSI_UPPER_32

Field Name	Bit	Access	Description	Default
PCI_MSI_UPPER_32	31:0	R/W		0x00000000

1.10.3.4 PCIE:PCIE_MSI_CAP:MSI_PENDING_BIT

Parent: PCIE:PCIE_MSI_CAP

Instances: 1

TABLE 1-444: FIELDS IN MSI_PENDING_BIT

Field Name	Bit	Access	Description	Default
PCI_MSI_PENDING_BIT	31:0	R/O		0x00000000

1.10.4 PCIE:PCIE_CAP

Parent: PCIE

Instances: 1

TABLE 1-445: REGISTERS IN PCIE_CAP

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PCIE_CAP_ID_PCIE_NEXT_-CAP_PTR_PCIE_CAP	0x00000000	1	Word offset 0	Page 201
DEVICE_CAPABILITIES	0x00000004	1	Word offset 1	Page 201

TABLE 1-445: REGISTERS IN PCIE_CAP (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
DEVICE_CONTROL_DEVICE_STATUS	0x00000008	1	Word offset 2	Page 202
LINK_CAPABILITIES	0x0000000C	1	Word offset 3	Page 202
LINK_CONTROL_LINK_STATUS	0x00000010	1	Word offset 4	Page 203
DEVICE_CAPABILITIES2	0x00000024	1	Word offset 9	Page 203
DEVICE_CONTROL2_DEVICE_STATUS2	0x00000028	1	Word offset 10	Page 204
LINK_CAPABILITIES2	0x0000002C	1	Word offset 11	Page 204
LINK_CONTROL2_LINK_STATUS2	0x00000030	1	Word offset 12	Page 205

1.10.4.1 PCIE:PCIE_CAP:PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP

Parent: PCIE:PCIE_CAP

Instances: 1

TABLE 1-446: FIELDS IN PCIE_CAP_ID_PCIE_NEXT_CAP_PTR_PCIE_CAP

Field Name	Bit	Access	Description	Default
RSVD	30	R/O		0x0
PCIE_INT_MSG_NUM	29:25	R/W		0x00
PCIE_SLOT_IMP	24	R/W		0x0
PCIE_DEV_PORT_TYPE	23:20	R/O		0x0
PCIE_CAP	19:16	R/O		0x2
PCIE_CAP_NEXT_PTR	15:8	R/W		0x00
PCIE_CAP_ID	7:0	R/O		0x10

1.10.4.2 PCIE:PCIE_CAP:DEVICE_CAPABILITIES

Parent: PCIE:PCIE_CAP

Instances: 1

TABLE 1-447: FIELDS IN DEVICE_CAPABILITIES

Field Name	Bit	Access	Description	Default
PCIE_CAP_FLR_CAP	28	R/W		0x0
PCIE_CAP_ROLE_BASED_ERR_REPORT	15	R/W		0x1
PCIE_CAP_EP_L1_ACCPT_LATENCY	11:9	R/W		0x7
PCIE_CAP_EP_L0S_ACCPT_LATENCY	8:6	R/W		0x5
PCIE_CAP_EXT_TAG_SUPP	5	R/W		0x0
PCIE_CAP_PHANTOM_FUNC_SUPPORT	4:3	R/W		0x0
PCIE_CAP_MAX_PAYLOAD_SIZE	2:0	R/W		0x0

1.10.4.3 PCIE:PCIE_CAP:DEVICE_CONTROL_DEVICE_STATUS

Parent: PCIE:PCIE_CAP

Instances: 1

TABLE 1-448: FIELDS IN DEVICE_CONTROL_DEVICE_STATUS

Field Name	Bit	Access	Description	Default
PCIE_CAP_TRANS_PENDING	21	R/O		0x0
PCIE_CAP_AUX_POWER_DETECTED	20	R/O		0x1
PCIE_CAP_UNSUPPORTED_REQ_DETECTED	19	One-shot		0x0
PCIE_CAP_FATAL_ERR_DETECTED	18	One-shot		0x0
PCIE_CAP_NON_FATAL_ERR_DETECTED	17	One-shot		0x0
PCIE_CAP_CORR_ERR_DETECTED	16	One-shot		0x0
PCIE_CAP_INITIATE_FLR	15	R/W		0x0
PCIE_CAP_MAX_READ_REQ_SIZE	14:12	R/W		0x2
PCIE_CAP_EN_NO_SNOOP	11	R/O		0x0
PCIE_CAP_AUX_POWER_PM_EN	10	R/W		0x0
PCIE_CAP_PHANTOM_FUNC_EN	9	R/O		0x0
PCIE_CAP_EXT_TAG_EN	8	R/O		0x0
PCIE_CAP_MAX_PAYLOAD_SIZE_CS	7:5	R/W		0x0
PCIE_CAP_EN_REL_ORDER	4	R/W		0x1
PCIE_CAP_UNSUPPORT_REQ_REP_EN	3	R/W		0x0
PCIE_CAP_FATAL_ERR_REPORT_EN	2	R/W		0x0
PCIE_CAP_NON_FATAL_ERR_REPORT_EN	1	R/W		0x0
PCIE_CAP_CORR_ERR_REPORT_EN	0	R/W		0x0

1.10.4.4 PCIE:PCIE_CAP:LINK_CAPABILITIES

Parent: PCIE:PCIE_CAP

Instances: 1

TABLE 1-449: FIELDS IN LINK_CAPABILITIES

Field Name	Bit	Access	Description	Default
PCIE_CAP_PORT_NUM	31:24	R/W		0x00
PCIE_CAP_ASPM_OPT_COMPLIANCE	22	R/W		0x1
PCIE_CAP_LINK_BW_NOT_CAP	21	R/O		0x0

TABLE 1-449: FIELDS IN LINK_CAPABILITIES (CONTINUED)

Field Name	Bit	Access	Description	Default
PCIE_CAP_DLL_ACTIVE_REP_-CAP	20	R/O		0x0
PCIE_CAP_SUR-PRISE_DOWN_ERR_REP_CAP	19	R/O		0x0
PCIE_CAP_CLOCK_POW-ER_MAN	18	R/W		0x0
PCIE_CAP_L1_EXIT_LATENCY	17:15	R/W		0x0
PCIE_CAP_L0S_EXIT_LATENCY	14:12	R/W		0x3
PCIE_CAP_AC-TIVE_STATE_LINK_PM_SUP-PORT	11:10	R/W		0x3
PCIE_CAP_MAX_LINK_WIDTH	9:4	R/W		0x01
PCIE_CAP_MAX_LINK_SPEED	3:0	R/W		0x1

1.10.4.5 PCIE:PCIE_CAP:LINK_CONTROL_LINK_STATUS

Parent: PCIE:PCIE_CAP

Instances: 1

TABLE 1-450: FIELDS IN LINK_CONTROL_LINK_STATUS

Field Name	Bit	Access	Description	Default
PCIE_CAP_LINK_AUOT_B-W_STATUS	31	R/O		0x0
PCIE_CAP_LINK_B-W_MAN_STATUS	30	R/O		0x0
PCIE_CAP_DLL_ACTIVE	29	R/O		0x0
PCIE_CAP_SLOT_CLK_CONFIG	28	R/W		0x0
PCIE_CAP_LINK_TRAINING	27	R/O		0x0
PCIE_CAP_NEGO_LINK_WIDTH	24:20	R/O		0x01
PCIE_CAP_LINK_SPEED	19:16	R/O		0x1
PCIE_CAP_LINK_AUTO_B-W_INT_EN	11	R/O		0x0
PCIE_CAP_LINK_B-W_MAN_INT_EN	10	R/W		0x0
PCIE_CAP_EN_CLK_POW-ER_MAN	8	R/W		0x0
PCIE_CAP_EXTENDED_SYNCH	7	R/W		0x0
PCIE_CAP_COMMON_CLK_-CONFIG	6	R/W		0x0
PCIE_CAP_RETRAIN_LINK	5	R/O		0x0
PCIE_CAP_LINK_DISABLE	4	R/O		0x0
PCIE_CAP_RCB	3	R/O		0x0
PCIE_CAP_AC-TIVE_STATE_LINK_PM_CON-TROL	1:0	R/W		0x0

1.10.4.6 PCIE:PCIE_CAP:DEVICE_CAPABILITIES2

Parent: PCIE:PCIE_CAP

Instances: 1

TABLE 1-451: FIELDS IN DEVICE_CAPABILITIES2

Field Name	Bit	Access	Description	Default
PCIE_CAP_OBFF_SUPPORT	19:18	R/O		0x0
PCIE_CAP_TPH_CMPLT_SUP-PORT_1	13	R/O		0x0
PCIE_CAP_TPH_CMPLT_SUP-PORT_0	12	R/O		0x0
PCIE_CAP_LTR_SUPP	11	R/O		0x0
PCIE_-CAP_NO_RO_EN_PR2PR_PAR	10	R/W		0x0
PCIE_CAP_128_CAS_CPL_-SUPP	9	R/O		0x0
PCIE_CAP_64_ATOMIC_CPL_-SUPP	8	R/O		0x0
PCIE_CAP_32_ATOMIC_CPL_-SUPP	7	R/O		0x0
PCIE_CAP_ATOMIC_ROUT-ING_SUPP	6	R/O		0x0
PCIE_CAP_ARI_FORWARD_-SUPPORT	5	R/O		0x0
PCIE_CAP_CPL_TIMEOUT_DIS-ABLE_SUPPORT	4	R/O		0x1
PCIE_CAP_CPL_TIME-OUT_RANGE	3:0	R/W		0x0

1.10.4.7 PCIE:PCIE_CAP:DEVICE_CONTROL2_DEVICE_STATUS2

Parent: PCIE:PCIE_CAP

Instances: 1

TABLE 1-452: FIELDS IN DEVICE_CONTROL2_DEVICE_STATUS2

Field Name	Bit	Access	Description	Default
PCIE_CAP_ARI_FORWARD_-SUPPORT_CS	5	R/O		0x0
PCIE_CAP_CPL_TIMEOUT_DIS-ABLE	4	R/W		0x0

1.10.4.8 PCIE:PCIE_CAP:LINK_CAPABILITIES2

Parent: PCIE:PCIE_CAP

Instances: 1

TABLE 1-453: FIELDS IN LINK_CAPABILITIES2

Field Name	Bit	Access	Description	Default
PCIE_CAP_CROSS_LINK_SUP-PORT	8	R/O		0x0
PCIE_CAP_SUPPORT_LINK_-SPEED_VECTOR	7:1	R/O		0x01

1.10.4.9 PCIE:PCIE_CAP:LINK_CONTROL2_LINK_STATUS2

Parent: PCIE:PCIE_CAP

Instances: 1

TABLE 1-454: FIELDS IN LINK_CONTROL2_LINK_STATUS2

Field Name	Bit	Access	Description	Default
PCIE_CAP_LINK_EQ_REQ	21	One-shot		0x0
PCIE_CAP_EQ_CPL_P3	20	R/W		0x0
PCIE_CAP_EQ_CPL_P2	19	R/W		0x0
PCIE_CAP_EQ_CPL_P1	18	R/O		0x0
PCIE_CAP_EQ_CPL	17	R/O		0x0
PCIE_CAP_CURR_DEEMPHA-SIS	16	R/O		0x0

1.10.5 PCIE:PCIE_AER_CAP

Parent: PCIE

Instances: 1

TABLE 1-455: REGISTERS IN PCIE_AER_CAP

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
AER_EXT_CAP_HDR	0x00000000	1	Word offset 0	Page 205
UNCORR_ERR_STATUS	0x00000004	1	Word offset 1	Page 206
UNCORR_ERR_MASK	0x00000008	1	Word offset 2	Page 206
UNCORR_ERR_SEV	0x0000000C	1	Word offset 3	Page 207
CORR_ERR_STATUS	0x00000010	1	Word offset 4	Page 207
CORR_ERR_MASK	0x00000014	1	Word offset 5	Page 207
ADV_ERR_CAP_CTRL	0x00000018	1	Word offset 6	Page 208
HDR_LOG_REG_0	0x0000001C	1	Word offset 7	Page 208
HDR_LOG_REG_1	0x00000020	1	Word offset 8	Page 208
HDR_LOG_REG_2	0x00000024	1	Word offset 9	Page 208
HDR_LOG_REG_3	0x00000028	1	Word offset 10	Page 209

1.10.5.1 PCIE:PCIE_AER_CAP:AER_EXT_CAP_HDR

Parent: PCIE:PCIE_AER_CAP

Instances: 1

TABLE 1-456: FIELDS IN AER_EXT_CAP_HDR

Field Name	Bit	Access	Description	Default
NEXT_OFFSET	31:20	R/O		0x000
CAP_VERSION	19:16	R/O		0x2
CAP_ID	15:0	R/O		0x0001

1.10.5.2 PCIE:PCIE_AER_CAP:UNCORR_ERR_STATUS

Parent: PCIE:PCIE_AER_CAP

Instances: 1

TABLE 1-457: FIELDS IN UNCORR_ERR_STATUS

Field Name	Bit	Access	Description	Default
ATOMIC_EGRESS_-BLOCKED_ERR_STATUS	24	One-shot		0x0
INTERNAL_ERR_STATUS	22	One-shot		0x0
UNSUPPORTED_REQ_ER-R_STATUS	20	One-shot		0x0
ECRC_ERR_STATUS	19	One-shot		0x0
MALF_TLP_ERR_STATUS	18	One-shot		0x0
REC_OVERFLOW_ERR_STA-TUS	17	One-shot		0x0
UNEXP_CMPLT_ERR_STATUS	16	One-shot		0x0
CMPLT_ABORT_ERR_STATUS	15	One-shot		0x0
CMPLT_TIMEOUT_ERR_STA-TUS	14	One-shot		0x0
FC_PROTOCOL_ERR_STATUS	13	One-shot		0x0
POIS_TLP_ERR_STATUS	12	One-shot		0x0
SUR_DWN_ERR_STATUS	5	R/O		0x0
DL_PROTOCOL_ERR_STATUS	4	One-shot		0x0

1.10.5.3 PCIE:PCIE_AER_CAP:UNCORR_ERR_MASK

Parent: PCIE:PCIE_AER_CAP

Instances: 1

TABLE 1-458: FIELDS IN UNCORR_ERR_MASK

Field Name	Bit	Access	Description	Default
ATOMIC_EGRESS_-BLOCKED_ERR_MASK	24	R/O		0x0
INTERNAL_ERR_MASK	22	R/W		0x1
UNSUPPORTED_REQ_ER-R_MASK	20	R/W		0x0
ECRC_ERR_MASK	19	R/W		0x0
MALF_TLP_ERR_MASK	18	R/W		0x0
REC_OVERFLOW_ERR_MASK	17	R/W		0x0
UNEXP_CMPLT_ERR_MASK	16	R/W		0x0
CMPLT_ABORT_ERR_MASK	15	R/W		0x0
CMPLT_TIMEOUT_ERR_MASK	14	R/W		0x0
FC_PROTOCOL_ERR_MASK	13	R/W		0x0
POIS_TLP_ERR_MASK	12	R/W		0x0
SUR_DWN_ERR_MASK	5	R/O		0x0
DL_PROTOCOL_ERR_MASK	4	R/W		0x0

1.10.5.4 PCIE:PCIE_AER_CAP:UNCORR_ERR_SEV

Parent: PCIE:PCIE_AER_CAP

Instances: 1

TABLE 1-459: FIELDS IN UNCORR_ERR_SEV

Field Name	Bit	Access	Description	Default
ATOMIC_EGRESS_-BLOCKED_ERR_SEVERITY	24	R/O		0x0
INTERNAL_ERR_SEVERITY	22	R/W		0x1
UNSUPPORTED_REQ_ERR_SE-VERITY	20	R/W		0x0
ECRC_ERR_SEVERITY	19	R/W		0x0
MALF_TLP_ERR_SEVERITY	18	R/W		0x1
REC_OVERFLOW_ERR_SEVER-ITY	17	R/W		0x1
UNEXP_CMPLT_ERR_SEVER-ITY	16	R/W		0x0
CMPLT_ABORT_ERR_SEVER-ITY	15	R/W		0x0
CMPLT_TIMEOUT_ERR_SEVER-ITY	14	R/W		0x0
FC_PROTOCOL_ERR_SEVER-ITY	13	R/W		0x1
POIS_TLP_ERR_SEVERITY	12	R/W		0x0
SUR_DWN_ERR_SEVERITY	5	R/O		0x1
DL_PROTOCOL_ERR_SEVER-ITY	4	R/W		0x1

1.10.5.5 PCIE:PCIE_AER_CAP:CORR_ERR_STATUS

Parent: PCIE:PCIE_AER_CAP

Instances: 1

TABLE 1-460: FIELDS IN CORR_ERR_STATUS

Field Name	Bit	Access	Description	Default
CORRECTED_INT_ERR_STA-TUS	14	One-shot		0x0
ADVISORY_NON_FATAL_ER-R_STATUS	13	One-shot		0x0
RPL_TIMER_TIMEOUT_STATUS	12	One-shot		0x0
REPLAY_NO_ROLEOVER_STA-TUS	8	One-shot		0x0
BAD_DLLP_STATUS	7	One-shot		0x0
BAD_TLP_STATUS	6	One-shot		0x0
RX_ERR_STATUS	0	One-shot		0x0

1.10.5.6 PCIE:PCIE_AER_CAP:CORR_ERR_MASK

Parent: PCIE:PCIE_AER_CAP

Instances: 1

TABLE 1-461: FIELDS IN CORR_ERR_MASK

Field Name	Bit	Access	Description	Default
CORRECTED_INT_ERR_MASK	14	R/W		0x1
ADVISORY_NON_FATAL_ER-R_MASK	13	R/W		0x1
RPL_TIMER_TIMEOUT_MASK	12	R/W		0x0
REPLAY_NO_ROLE-OVER_MASK	8	R/W		0x0
BAD_DLLP_MASK	7	R/W		0x0
BAD_TLP_MASK	6	R/W		0x0
RX_ERR_MASK	0	R/W		0x0

1.10.5.7 PCIE:PCIE_AER_CAP:ADV_ERR_CAP_CTRL

Parent: PCIE:PCIE_AER_CAP

Instances: 1

TABLE 1-462: FIELDS IN ADV_ERR_CAP_CTRL

Field Name	Bit	Access	Description	Default
ECRC_CHECK_EN	8	R/W		0x0
ECRC_CHECK_CAP	7	R/O		0x1
ECRC_GEN_EN	6	R/W		0x0
ECRC_GEN_CAP	5	R/O		0x1
FIRST_ERR_POINTER	4:0	R/O		0x00

1.10.5.8 PCIE:PCIE_AER_CAP:HDR_LOG_REG_0

Parent: PCIE:PCIE_AER_CAP

Instances: 1

TABLE 1-463: FIELDS IN HDR_LOG_REG_0

Field Name	Bit	Access	Description	Default
FIRST_DWORD	31:0	R/O		0x00000000

1.10.5.9 PCIE:PCIE_AER_CAP:HDR_LOG_REG_1

Parent: PCIE:PCIE_AER_CAP

Instances: 1

TABLE 1-464: FIELDS IN HDR_LOG_REG_1

Field Name	Bit	Access	Description	Default
SECOND_DWORD	31:0	R/O		0x00000000

1.10.5.10 PCIE:PCIE_AER_CAP:HDR_LOG_REG_2

Parent: PCIE:PCIE_AER_CAP

Instances: 1

TABLE 1-465: FIELDS IN HDR_LOG_REG_2

Field Name	Bit	Access	Description	Default
THIRD_DWORD	31:0	R/O		0x00000000

1.10.5.11 PCIE:PCIE_AER_CAP:HDR_LOG_REG_3

Parent: PCIE:PCIE_AER_CAP

Instances: 1

TABLE 1-466: FIELDS IN HDR_LOG_REG_3

Field Name	Bit	Access	Description	Default
FOURTH_DWORD	31:0	R/O		0x00000000

1.10.6 PCIE:PCIE_PORT_LOGIC

Parent: PCIE

Instances: 1

TABLE 1-467: REGISTERS IN PCIE_PORT_LOGIC

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
ATU_REGION	0x00000200	1	Address translation region	Page 209
ATU_CFG1	0x00000204	1	Address translation configuration register 1	Page 210
ATU_CFG2	0x00000208	1	Address translation configuration register 2	Page 210
ATU_BASE_ADDR_LOW	0x0000020C	1	Address translation lower base address	Page 210
ATU_BASE_ADDR_HIGH	0x00000210	1	Address translation upper base address	Page 211
ATU_LIMIT_ADDR	0x00000214	1	Address translation limit address	Page 211
ATU_TGT_ADDR_LOW	0x00000218	1	Address translation lower target address	Page 211
ATU_TGT_ADDR_HIGH	0x0000021C	1	Address translation upper target address	Page 211

1.10.6.1 PCIE:PCIE_PORT_LOGIC:ATU_REGION

Parent: PCIE:PCIE_PORT_LOGIC

Instances: 1

The address translation unit supports 2 outbound regions. The registers PCIE::ATU_CFG1, PCIE::ATU_CFG2, PCIE::ATU_BASE_ADDR_LOW, PCIE::ATU_BASE_ADDR_HIGH, PCIE::ATU_LIMIT_ADDR, PCIE::ATU_TGT_ADDR_LOW, and PCIE::ATU_TGT_ADDR_HIGH all maps to the currently configured region (as configured in this register).

TABLE 1-468: FIELDS IN ATU_REGION

Field Name	Bit	Access	Description	Default
ATU_IDX	2:0	R/W	Selects region index, set to 0 or 1.	0x0

1.10.6.2 PCIE:PCIE_PORT_LOGIC:ATU_CFG1

Parent: PCIE:PCIE_PORT_LOGIC

Instances: 1

TABLE 1-469: FIELDS IN ATU_CFG1

Field Name	Bit	Access	Description	Default
ATU_ATTR	10:9	R/W	When the address of an outbound TLP is matched to this region, then the ATTR field of the TLP is changed to the value in this register.	0x0
ATU_TD	8	R/W	When the address of an outbound TLP is matched to this region, then the TD field of the TLP is changed to the value in this register.	0x0
ATU_TC	7:5	R/W	When the address of an outbound TLP is matched to this region, then the TC field of the TLP is changed to the value in this register.	0x0
ATU_TYPE	4:0	R/W	When the address of an outbound TLP is matched to this region, then the TYPE field of the TLP is changed to the value in this register. 0: MRd/MWr 1: MRdLk 2: IORd/IOWr 4: CfgRd0/CfgWr0 5: CfgRd1/CfgWr1 16-23: Msg/MsgD	0x00

1.10.6.3 PCIE:PCIE_PORT_LOGIC:ATU_CFG2

Parent: PCIE:PCIE_PORT_LOGIC

Instances: 1

TABLE 1-470: FIELDS IN ATU_CFG2

Field Name	Bit	Access	Description	Default
ATU_REGION_ENA	31	R/W	This bit must be set for address translation to take place.	0x0
ATU_MSG_CODE	7:0	R/W	When the address of an outbound TLP is matched to this region, and the translated TLP TYPE field is Msg or MsgD; then the Message field of the TLP is changed to the value in this register.	0x00

1.10.6.4 PCIE:PCIE_PORT_LOGIC:ATU_BASE_ADDR_LOW

Parent: PCIE:PCIE_PORT_LOGIC

Instances: 1

TABLE 1-471: FIELDS IN ATU_BASE_ADDR_LOW

Field Name	Bit	Access	Description	Default
ATU_BASE_ADDR_LOW	31:16	R/W	Bits 31:16 of the starting address of the address region to be translated.	0x0000

1.10.6.5 PCIE:PCIE_PORT_LOGIC:ATU_BASE_ADDR_HIGH

Parent: PCIE:PCIE_PORT_LOGIC

Instances: 1

TABLE 1-472: FIELDS IN ATU_BASE_ADDR_HIGH

Field Name	Bit	Access	Description	Default
ATU_BASE_ADDR_HIGH	31:0	R/W	Outbound: Not used. Inbound: Bits 63:32 of the starting address of the address region to be translated.	0x00000000

1.10.6.6 PCIE:PCIE_PORT_LOGIC:ATU_LIMIT_ADDR

Parent: PCIE:PCIE_PORT_LOGIC

Instances: 1

TABLE 1-473: FIELDS IN ATU_LIMIT_ADDR

Field Name	Bit	Access	Description	Default
ATU_LIMIT_ADDR	31:16	R/W	Bits 31:16 of the ending address of the address region to be translated.	0x0000
RESERVED_3	15:0	R/O		0xFFFF

1.10.6.7 PCIE:PCIE_PORT_LOGIC:ATU_TGT_ADDR_LOW

Parent: PCIE:PCIE_PORT_LOGIC

Instances: 1

TABLE 1-474: FIELDS IN ATU_TGT_ADDR_LOW

Field Name	Bit	Access	Description	Default
ATU_TGT_ADDR_LOW	31:16	R/W	Bits 31:16 of the new address of the translated region.	0x0000

1.10.6.8 PCIE:PCIE_PORT_LOGIC:ATU_TGT_ADDR_HIGH

Parent: PCIE:PCIE_PORT_LOGIC

Instances: 1

TABLE 1-475: FIELDS IN ATU_TGT_ADDR_HIGH

Field Name	Bit	Access	Description	Default
ATU_TGT_ADDR_HIGH	31:0	R/W	Bits 63:32 of the new address of the translated region. Set to 0 to force new address into 32bit PCIe memory space.	0x00000000

1.11 QSYS

TABLE 1-476: REGISTER GROUPS IN QSYS

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
SYSTEM	0x00011200	1	Switch configuration	Page 212
TIMED_FRAME_CFG	0x00011310	1		Page 216
RES_QOS_ADV	0x00011338	1	Advanced QoS Configuration	Page 219
RES_CTRL	0x00012000	1024 0x00000008	Watermarks and status for egress queue system	Page 220
DROP_CFG	0x0001137C	1	Watermarks for egress queue system	Page 222
MMGT	0x00011380	1	Memory manager status	Page 222
HSCH	0x00000000	548 0x00000080	Configuration of scheduling system and shapers	Page 223
HSCH_MISC	0x00011388	1	Miscellaneous scheduler configuration	Page 227

1.11.1 QSYS:SYSTEM

Parent: QSYS

Instances: 1

TABLE 1-477: REGISTERS IN SYSTEM

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PORT_MODE	0x00000000	13 0x00000004	Port configuration per device port	Page 213
SWITCH_PORT_MODE	0x00000034	12 0x00000004	Various switch port mode settings per switch port	Page 213
STAT_CNT_CFG	0x00000064	1	Statistics configuration	Page 214
EEE_CFG	0x00000068	11 0x00000004	Control Energy Efficient Ethernet operation per front port.	Page 214
EEE_THRES	0x00000094	1	Thresholds for delayed EEE queues	Page 215
IGR_NO_SHARING	0x00000098	1	Control shared memory users	Page 215
EGR_NO_SHARING	0x0000009C	1	Control shared memory users	Page 215

TABLE 1-477: REGISTERS IN SYSTEM (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
SW_STATUS	0x000000A0	12 0x00000004	Various status information per switch port	Page 215
EXT_CPU_CFG	0x000000D0	1	External CPU port configuration	Page 216
CPU_GROUP_MAP	0x000000D8	1	Map CPU extraction queues to CPU ports	Page 216

1.11.1.1 QSYS:SYSTEM:PORT_MODE

Parent: QSYS:SYSTEM

Instances: 13

These configurations exists per front port and for each of the two CPU ports (11+12).

TABLE 1-478: FIELDS IN PORT_MODE

Field Name	Bit	Access	Description	Default
DEQUEUE_DIS	1	R/W	Disable dequeuing from the egress queues. Frames are not discarded, but may become aged when dequeuing is re-enabled.	0x0
DEQUEUE_LATE	0	R/W	Delay dequeuing from the egress queues. This might be necessary for minimising flow control tails.	0x0

1.11.1.2 QSYS:SYSTEM:SWITCH_PORT_MODE

Parent: QSYS:SYSTEM

Instances: 12

TABLE 1-479: FIELDS IN SWITCH_PORT_MODE

Field Name	Bit	Access	Description	Default
PORT_ENA	14	R/W	Enable port for any frame transfer. Frames to or from a port with PORT_ENA cleared are discarded.	0x0
SCH_NEXT_CFG	13:11	R/W	Configures the time at which next frame for a port is decided. A low value can result in IFGs but that the arbitration be tween multiple queues can run true round-robin. A high value will result in back-to-back transmissions, but with an overshoot compared to shaper burst configurations and PFC blocking events. 0: At EOF cell 1: When one cell is yet to transmit n: When n cells are yet to be transmitted 7: When all cells are yet to be transmitted	0x1

TABLE 1-479: FIELDS IN SWITCH_PORT_MODE (CONTINUED)

Field Name	Bit	Access	Description	Default
INGRESS_DROP_MODE	9	R/W	When enabled for a port, frames -from- that port are discarded when the controlling watermarks are hit. If disabled - the frame will stay in memory until resources are available. If INGRESS_DROP_MODE or EGRESS_DROP_MODE applies for a frame copy, it will be discared.	0x1
TX_PFC_ENA	8:1	R/W	When set the MAC sends PRIO pause control frames in the Tx direction when congested.	0x00
TX_PFC_MODE	0	R/W	When set, a congested priority request pause of all lower priorities as well.	0x0

1.11.1.3 QSYS:SYSTEM:STAT_CNT_CFG

Parent: QSYS:SYSTEM

Instances: 1

TABLE 1-480: FIELDS IN STAT_CNT_CFG

Field Name	Bit	Access	Description	Default
TX_GREEN_CNT_MODE	5	R/W	Counter mode for the Tx priority counters for green frames (C_TX_GREEN_PRIO_x) 0: Count octets 1: Count frames	0x1
TX_YELLOW_CNT_MODE	4	R/W	Counter mode for the Tx priority counters for green frames (C_TX_YELLOW_PRIO_x) 0: Count octets 1: Count frames	0x1
DROP_GREEN_CNT_MODE	3	R/W	Counter mode for the drop counters for green frames (C_DR_GREEN_PRIO_x) 0: Count octets 1: Count frames	0x1
DROP_YELLOW_CNT_MODE	2	R/W	Counter mode for the drop counters for green frames (C_DR_YELLOW_PRIO_x) 0: Count octets 1: Count frames	0x1
DROP_COUNT_EGRESS	0	R/W	When set, a frame discarded due to lack of resources is counted on the egress port instead of the ingress. Side effect is a slower processing of multiple drops on the same frame, causing potential head-of-line blocking.	0x0

1.11.1.4 QSYS:SYSTEM:EEE_CFG

Parent: QSYS:SYSTEM

Instances: 11

TABLE 1-481: FIELDS IN EEE_CFG

Field Name	Bit	Access	Description	Default
EEE_FAST_QUEUES	7:0	R/W	Queues set in this mask activate the egress port immediately when any of the queues have data available.	0x00

1.11.1.5 QSYS:SYSTEM:EEE_THRES

Parent: QSYS:SYSTEM

Instances: 1

TABLE 1-482: FIELDS IN EEE_THRES

Field Name	Bit	Access	Description	Default
EEE_HIGH_BYTES	15:8	R/W	Maximum number of bytes in a queue before egress port is activated. Unit is 60 bytes.	0x00
EEE_HIGH_FRAMES	7:0	R/W	Maximum number of frames in a queue before the egress port is activated. Unit is 1 frame.	0x00

1.11.1.6 QSYS:SYSTEM:IGR_NO_SHARING

Parent: QSYS:SYSTEM

Instances: 1

TABLE 1-483: FIELDS IN IGR_NO_SHARING

Field Name	Bit	Access	Description	Default
IGR_NO_SHARING	11:0	R/W	Control whether frames received on the port may use shared resources. If ingress port or queue has reserved memory left to use, frame enqueuing is always allowed. 0: Use shared memory as well 1: Do not use shared memory	0x000

1.11.1.7 QSYS:SYSTEM:EGR_NO_SHARING

Parent: QSYS:SYSTEM

Instances: 1

TABLE 1-484: FIELDS IN EGR_NO_SHARING

Field Name	Bit	Access	Description	Default
EGR_NO_SHARING	11:0	R/W	Control whether frames forwarded to the port may use shared resources. If egress port or queue has reserved memory left to use, frame enqueuing is always allowed. 0: Use shared memory as well 1: Do not use shared memory	0x000

1.11.1.8 QSYS:SYSTEM:SW_STATUS

Parent: QSYS:SYSTEM

Instances: 12

TABLE 1-485: FIELDS IN SW_STATUS

Field Name	Bit	Access	Description	Default
EQ_AVAIL	7:0	R/O	Status bit per egress queue indicating whether data is ready for transmission.	0x00

1.11.1.9 QSYS:SYSTEM:EXT_CPU_CFG

Parent: QSYS:SYSTEM

Instances: 1

TABLE 1-486: FIELDS IN EXT_CPU_CFG

Field Name	Bit	Access	Description	Default
EXT_CPU_PORT	12:8	R/W	Select the port to use as the external CPU port.	0x08
EXT_CPUQ_MSK	7:0	R/W	Frames destined for a CPU extraction queue set in this mask are sent to the external CPU defined by EXT_CPU_PORT instead of the internal CPU.	0x00

1.11.1.10 QSYS:SYSTEM:CPU_GROUP_MAP

Parent: QSYS:SYSTEM

Instances: 1

TABLE 1-487: FIELDS IN CPU_GROUP_MAP

Field Name	Bit	Access	Description	Default
CPU_GROUP_MAP	7:0	R/W	Map the 8 CPU extraction queues to the two CPU ports. Bit <n> set to 1 directs CPU extraction queue <n> to CPU port 12. Bit <n> set to 0 directs CPU extraction queue <n> to CPU port 11.	0x00

1.11.2 QSYS:TIMED_FRAME_CFG

Parent: QSYS

Instances: 1

TABLE 1-488: REGISTERS IN TIMED_FRAME_CFG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
TFRM_MISC	0x00000000	1	Timed frame configuration	Page 217
TFRM_PORT_DLY	0x00000004	1	Interleaved transmission setup	Page 217
TFRM_TIMER_CFG_1	0x00000008	1	Configures timers for timed transmissions	Page 217
TFRM_TIMER_CFG_2	0x0000000C	1	Configures timers for timed transmissions	Page 218

TABLE 1-488: REGISTERS IN TIMED_FRAME_CFG (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
TFRM_TIMER_CFG_3	0x00000010	1	Configures timers for timed transmissions	Page 218
TFRM_TIMER_CFG_4	0x00000014	1	Configures timers for timed transmissions	Page 218
TFRM_TIMER_CFG_5	0x00000018	1	Configures timers for timed transmissions	Page 218
TFRM_TIMER_CFG_6	0x0000001C	1	Configures timers for timed transmissions	Page 218
TFRM_TIMER_CFG_7	0x00000020	1	Configures timers for timed transmissions	Page 219
TFRM_TIMER_CFG_8	0x00000024	1	Configures timers for timed transmissions	Page 219

1.11.2.1 QSYS:TIMED_FRAME_CFG:TFRM_MISC

Parent: QSYS:TIMED_FRAME_CFG

Instances: 1

TABLE 1-489: FIELDS IN TFRM_MISC

Field Name	Bit	Access	Description	Default
TIMED_CANCEL_SLOT	18:9	R/W	Specify slot of timed frame to cancel	0x000
TIMED_CANCEL_1SHOT	8	One-shot	Set this field to cancel a timed transmission. Auto cleared when complete.	0x0
RESERVED	6:0	R/W	Must be set to its default.	0x02

1.11.2.2 QSYS:TIMED_FRAME_CFG:TFRM_PORT_DLY

Parent: QSYS:TIMED_FRAME_CFG

Instances: 1

TABLE 1-490: FIELDS IN TFRM_PORT_DLY

Field Name	Bit	Access	Description	Default
TFRM_PORT_DLY_ENA	12:0	R/W	When multiple timed frames are ready for transmission at the same time, they are by default transmitted as fast as they can, resulting in a burst of frames. By enabling the interleave mode, timer 8 must run out between each frame being transmitted on a port. 0: Send frames in burst 1: Send frames interleaved	0x0000

1.11.2.3 QSYS:TIMED_FRAME_CFG:TFRM_TIMER_CFG_1

Parent: QSYS:TIMED_FRAME_CFG

Instances: 1

TABLE 1-491: FIELDS IN TFRM_TIMER_CFG_1

Field Name	Bit	Access	Description	Default
TFRM_TIMER_CFG_1	31:0	R/W	Configures timer 1. Default 3.3 ms. Unit: 198.2 ns	0x0000410A

1.11.2.4 QSYS:TIMED_FRAME_CFG:TFRM_TIMER_CFG_2

Parent: QSYS:TIMED_FRAME_CFG

Instances: 1

TABLE 1-492: FIELDS IN TFRM_TIMER_CFG_2

Field Name	Bit	Access	Description	Default
TFRM_TIMER_CFG_2	31:0	R/W	Configures timer 2. Default 10 us. Unit: 198.2 ns	0x00000033

1.11.2.5 QSYS:TIMED_FRAME_CFG:TFRM_TIMER_CFG_3

Parent: QSYS:TIMED_FRAME_CFG

Instances: 1

TABLE 1-493: FIELDS IN TFRM_TIMER_CFG_3

Field Name	Bit	Access	Description	Default
TFRM_TIMER_CFG_3	31:0	R/W	Configures timer 3. Default 100 us. Unit: 198.2 ns	0x000001F9

1.11.2.6 QSYS:TIMED_FRAME_CFG:TFRM_TIMER_CFG_4

Parent: QSYS:TIMED_FRAME_CFG

Instances: 1

TABLE 1-494: FIELDS IN TFRM_TIMER_CFG_4

Field Name	Bit	Access	Description	Default
TFRM_TIMER_CFG_4	31:0	R/W	Configures timer 4. Default 1 ms. Unit: 198.2 ns	0x000013B5

1.11.2.7 QSYS:TIMED_FRAME_CFG:TFRM_TIMER_CFG_5

Parent: QSYS:TIMED_FRAME_CFG

Instances: 1

TABLE 1-495: FIELDS IN TFRM_TIMER_CFG_5

Field Name	Bit	Access	Description	Default
TFRM_TIMER_CFG_5	31:0	R/W	Configures timer 5. Default 10 ms. Unit: 198.2 ns	0x0000C516

1.11.2.8 QSYS:TIMED_FRAME_CFG:TFRM_TIMER_CFG_6

Parent: QSYS:TIMED_FRAME_CFG

Instances: 1

TABLE 1-496: FIELDS IN TFRM_TIMER_CFG_6

Field Name	Bit	Access	Description	Default
TFRM_TIMER_CFG_6	31:0	R/W	Configures timer 6. Default 100 ms. Unit: 198.2 ns	0x0007B2DD

1.11.2.9 QSYS:TIMED_FRAME_CFG:TFRM_TIMER_CFG_7

Parent: QSYS:TIMED_FRAME_CFG

Instances: 1

TABLE 1-497: FIELDS IN TFRM_TIMER_CFG_7

Field Name	Bit	Access	Description	Default
TFRM_TIMER_CFG_7	31:0	R/W	Configures timer 7. Default 1sec. Unit: 198.2 ns	0x004CFCA1

1.11.2.10 QSYS:TIMED_FRAME_CFG:TFRM_TIMER_CFG_8

Parent: QSYS:TIMED_FRAME_CFG

Instances: 1

TABLE 1-498: FIELDS IN TFRM_TIMER_CFG_8

Field Name	Bit	Access	Description	Default
TFRM_TIMER_CFG_8	31:0	R/W	Configures timer 8. Default 198.2 ns. Unit: 198.2 ns	0x00000001

1.11.3 QSYS:RES_QOS_ADV

Parent: QSYS

Instances: 1

TABLE 1-499: REGISTERS IN RES_QOS_ADV

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
RED_PROFILE	0x00000000	16 0x00000004	Weighted Random Early Detection (WRED) configuration	Page 219
RES_QOS_MODE	0x00000040	1	Shared QOS resource mode	Page 220

1.11.3.1 QSYS:RES_QOS_ADV:RED_PROFILE

Parent: QSYS:RES_QOS_ADV

Instances: 16

Configuration of Weighted Random Early Detection (WRED) profile per QoS class per drop precedence level. Profiles 0-7 are for frames with QoS class 0-7 and drop precedence level 0. Profiles 8-15 are for frames with QoS class 0-7 and drop precedence level 1.

TABLE 1-500: FIELDS IN RED_PROFILE

Field Name	Bit	Access	Description	Default
WM_RED_LOW	15:8	R/W	When enqueuing a frame, RED is active if the ingress memory consumption by the frame's QoS class is above WM_RED_LEVEL. The probability of random early discarding is calculated as: (Memory consumption by the frame's QoS class - WM_RED_LOW)/(WM_RED_HIGH - WM_RED_LOW). Unit is 960 bytes.	0xFF
WM_RED_HIGH	7:0	R/W	See WM_RED_LOW. Unit is 960 bytes.	0xFF

1.11.3.2 QSYS:RES_QOS_ADV:RES_QOS_MODE

Parent: QSYS:RES_QOS_ADV

Instances: 1

TABLE 1-501: FIELDS IN RES_QOS_MODE

Field Name	Bit	Access	Description	Default
RES_QOS_RSRVD	7:0	R/W	When a QoS class is enabled in this mask, the class will have guaranteed shared space. The watermarks found in RES_CFG are used for setting the amount of space set aside.	0x00

1.11.4 QSYS:RES_CTRL

Parent: QSYS

Instances: 1024

TABLE 1-502: REGISTERS IN RES_CTRL

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
RES_CFG	0x00000000	1	Watermark configuration	Page 220
RES_STAT	0x00000004	1	Resource status	Page 221

1.11.4.1 QSYS:RES_CTRL:RES_CFG

Parent: QSYS:RES_CTRL

Instances: 1

The queue system tracks four resource consumptions:

Resource 0: Memory tracked per source

Resource 1: Frame references tracked per source

Resource 2: Memory tracked per destination

Resource 3: Frame references tracked per destination

Before a frame is added to the queue system, some conditions must be met:

- Reserved memory for the specific (SRC, PRIO) or for the specific SRC is available

OR

- Reserved memory for the specific (DST,PRIO) or for the specific DST is available

OR

- Shared memory is available

The frame reference resources are checked for availability like the memory resources. Enqueuing of a frame is allowed if both the memory resource check and the frame reference resource check succeed.

The extra resources consumed when enqueuing a frame are first taken from the reserved (SRC,PRIO), next from the reserved SRC, and last from the shared memory area. The same is done for DST. Both memory consumptions and frame reference consumptions are updated.

The register is laid out in the following way for source memory (resource 0):

Index 0-95: Q_RSRV - Reserved amount for (SRC,PRIO) at index 8*SRC+PRIO

Index 216-223: PRIO_SHR - Maximum allowed use of the shared buffer for PRIO at index PRIO+216

Index 224-235: P_RSRV - Reserved amount for SRC at index SRC+224.

Index 254: COL_SHR - Maximum allowed use of the shared buffer for frames with DP=1.

Index 255: COL_SHR Maximum allowed use of the shared buffer for source.

The layout is similar for resources 1, 2, and 3. Resource 1 uses indices 256-511, resource 2 uses indices 512-767, and resource 3 uses indices 768-1023.

Note, the default values depend on the index used.

The allocation unit for memory tracking is 60 bytes and the allocation unit for reference tracking is 1 frame reference. All frames are prepended with a 16-byte header.

TABLE 1-503: FIELDS IN RES_CFG

Field Name	Bit	Access	Description	Default
WM_HIGH	8:0	R/W	Watermark for resource. Note, the default value depends on the index. Bit 8: Selects multiplier unit for watermark. Bit 8 = 0: Multiply watermark value with 1, bit 8 = 1: Multiply watermark value with 16. Bits 7-0: Watermark value. Allocation unit is 60 bytes for memory and 1 frame reference for references.	0x000

1.11.4.2 QSYS:RES_CTRL:RES_STAT

Parent: QSYS:RES_CTRL

Instances: 1

TABLE 1-504: FIELDS IN RES_STAT

Field Name	Bit	Access	Description	Default
INUSE	23:12	R/W	Current consumption for corresponding watermark in RES_CFG.	0x000
MAXUSE	11:0	R/W	Maximum consumption since last read for corresponding watermark in RES_CFG.	0x000

1.11.5 QSYS:DROP_CFG

Parent: QSYS

Instances: 1

TABLE 1-505: REGISTERS IN DROP_CFG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
EGR_DROP_MODE	0x00000000	1	Configures egress ports for flowcontrol	Page 222

1.11.5.1 QSYS:DROP_CFG:EGR_DROP_MODE

Parent: QSYS:DROP_CFG

Instances: 1

TABLE 1-506: FIELDS IN EGR_DROP_MODE

Field Name	Bit	Access	Description	Default
EGRESS_DROP_MODE	11:0	R/W	When enabled for a port, frames -to- that port are discarded when the controlling watermarks are hit. If disabled - the frame will stay in memory until resources are available. If INGRESS_DROP_MODE or EGRESS_DROP_MODE applies for a frame copy, it will be discared.	0x000

1.11.6 QSYS:MMGT

Parent: QSYS

Instances: 1

TABLE 1-507: REGISTERS IN MMGT

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
EQ_CTRL	0x00000000	1	Egress queue status	Page 222

1.11.6.1 QSYS:MMGT:EQ_CTRL

Parent: QSYS:MMGT

Instances: 1

TABLE 1-508: FIELDS IN EQ_CTRL

Field Name	Bit	Access	Description	Default
FP_FREE_CNT	15:0	R/O	Number of free frame references.	0x0000

1.11.7 QSYS:HSCH

Parent: QSYS

Instances: 548

General purpose scheduling elements are used to form a hierarchy of queue scheduling. There are 192 elements.

The first 146 elements connect directly to frame queues. These elements have extra shapers on inputs 6 and 7, which can be used for strict/DWRR mixed priority schedulling. These shapers are configurable through this set of registers, at indexes 256+2*SE_NO (shaper 6) and indexes 256+2*SE_NO+1 (shaper 7). Only the CIR_CFG and CIR_STATE registers are valid for these indexes.

Example: To set the priority 7 shaper on scheduling element 67, access HSCH:391:CIR_CFG.

TABLE 1-509: REGISTERS IN HSCH

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CIR_CFG	0x00000000	1	Shaping configuration of the SE	Page 223
EIR_CFG	0x00000004	1	Excess rate configuration	Page 224
SE_CFG	0x00000008	1	Configuration of shaper and scheduling algorithm	Page 224
SE_DWRR_CFG	0x0000000C	12 0x00000004	Configuration of the DWRR costs	Page 224
SE_CONNECT	0x0000003C	1	Configuration of the connections between SEs	Page 225
SE_DLB_SENSE	0x00000040	1	Configuration of which fill levels in the queue system that the DLB shapers use to trigger excess information rate	Page 225
CIR_STATE	0x00000044	1	CIR status	Page 227
EIR_STATE	0x00000048	1	EIR status	Page 227

1.11.7.1 QSYS:HSCH:CIR_CFG

Parent: QSYS:HSCH

Instances: 1

TABLE 1-510: FIELDS IN CIR_CFG

Field Name	Bit	Access	Description	Default
CIR_RATE	20:6	R/W	Leak rate for this shaper. Unit is 100 kbps.	0x0000
CIR_BURST	5:0	R/W	Burst capacity of this shaper. Unit is 4 kilobytes. The shaper is disabled when CIR_BURST=0.	0x00

1.11.7.2 QSYS:HSCH:EIR_CFG

Parent: QSYS:HSCH

Instances: 1

TABLE 1-511: FIELDS IN EIR_CFG

Field Name	Bit	Access	Description	Default
EIR_RATE	21:7	R/W	Leak rate for this shaper. Unit is 100 kbps.	0x0000
EIR_BURST	6:1	R/W	Burst capacity of this shaper. Unit is 4 kilobytes. The dual leaky bucket shaper operates as a single leaky bucket shaper when EIR_BURST=0.	0x00
EIR_MARK_ENA	0	R/W	If a frame is scheduled with excess information rate, the frame color can be changed to yellow.	0x0

1.11.7.3 QSYS:HSCH:SE_CFG

Parent: QSYS:HSCH

Instances: 1

TABLE 1-512: FIELDS IN SE_CFG

Field Name	Bit	Access	Description	Default
SE_DWRR_CNT	9:6	R/W	Number of inputs running with DWRR algorithm, otherwise strict. Strict inputs always have the highest input index.	0x0
SE_RR_ENA	5	R/W	The DWRR algorithm is replaced with frame-based round robin.	0x0
SE_AVB_ENA	4	R/W	Enable AVB mode for this shaper, creating burst capacity only when data is available.	0x0
SE_FRM_MODE	3:2	R/W	Accounting mode for this shaper. 0: Line rate. Shape bytes including QSYS::HSCH_MISC_CFG.FRM_ADJ. 1: Data rate. Shape bytes excluding IPG. 2. Frame rate. Shape frames with rate unit = 100 fps and burst unit = 32.8 frames. 3: Frame rate. Shape framed with rate unit = 1 fps and burst unit = 0.3 frames.	0x0
SE_EXC_ENA	1	R/W	Allow bandwidth out of this element to exceed configured levels. Still - arbitrations always prefers inputs not exceeding configured levels.	0x0

1.11.7.4 QSYS:HSCH:SE_DWRR_CFG

Parent: QSYS:HSCH

Instances: 12

TABLE 1-513: FIELDS IN SE_DWRR_CFG

Field Name	Bit	Access	Description	Default
DWRR_COST	4:0	R/W	DWRR cost configuration	0x00

1.11.7.5 QSYS:HSCH:SE_CONNECT

Parent: QSYS:HSCH

Instances: 1

TABLE 1-514: FIELDS IN SE_CONNECT

Field Name	Bit	Access	Description	Default
SE_OUTP_IDX	24:17	R/W	The output port on this SE is connected to the SE selected by SE_OUTP_IDX. SE_OUTP_CON selects the input port number on the SE. If the SE_TERMINAL is set, the output port on this SE is connected to the egress port selected by SE_OUTP_IDX instead. The connections are automatically configured after reset to a source port fair strict priority scheme: SEs 0-7 connect to SE 146: Priority scheduler for port 0 SEs 8-15 connect to SE 147: Priority scheduler for port 1 ... SEs 96-103 connect to SE 158: Priority scheduler for CPU port 12 SEs 146+N connect to egress port N with SE_TERMINAL set.	0x00
SE_INP_IDX	16:9	R/W	The inputs on this SE are the output ports of the consequtive range of SEs starting at index SE_INP_IDX and ending at SE_INP_IDX+SE_INP_CNT-1. The queues connect 12 at a time to the first 146 SEs, and the SE_INP_IDX does not apply for those.	0x00
SE_OUTP_CON	8:5	R/W	The input port on the next SE, which this SE connects to. The next SE is selected by SE_OUTP_IDX.	0x0
SE_INP_CNT	4:1	R/W	Number of input ports on to this SE. Default values matches the default scheduling hierarchy described in the datasheet.	0xC
SE_TERMINAL	0	R/W	If set, this SE is connected to egress port SE_OUTP_IDX	0x0

1.11.7.6 QSYS:HSCH:SE_DLB_SENSE

Parent: QSYS:HSCH

Instances: 1

TABLE 1-515: FIELDS IN SE_DLB_SENSE

Field Name	Bit	Access	Description	Default
SE_DLB_PRIO	13:11	R/W	QoS class used when SE_DLB_PRIO_ENA is set.	0x0

TABLE 1-515: FIELDS IN SE_DLB_SENSE (CONTINUED)

Field Name	Bit	Access	Description	Default
SE_DLB_SPORT	10:7	R/W	Source port used when SE_DLB_SPORT_ENA is set.	0x0
SE_DLB_DPORT	6:3	R/W	Destination port used when SE_DLB_DPORT_ENA is set.	0x0
SE_DLB_PRIO_ENA	2	R/W	Enable priority awareness by the DLB shaper. If set, the DLB shaper allows excess information rate when the egress buffer use for QoS class SE_DLB_PRIO has reached threshold BUF_PRIO_SHR_E[SE_DLB_PRIO] minus 3000 bytes. If both SE_DLB_PRIO_ENA and SE_DLB_SPORT_ENA are set, the excess information rate is alllowed when the ingress buffer use for QoS class per source port has reached threshold BUF_Q_RSRV_I[SE_DLB_PRIO, SE_DLB_SPORT] minus 3000 bytes. If both SE_DLB_PRIO_ENA and SE_DLB_DPORT_ENA are set, the excess information rate is alllowed when the egress buffer use for QoS class per destination port has reached threshold BUF_Q_RSRV_E[SE_DLB_PRIO, SE_DLB_DPORT] minus 3000 bytes. If multiple awareness functions (SE_DLB_PRIO_ENA, SE_DLB_SPORT_ENA, SE_DLB_DPORT_ENA) are enabled, all relevant thresholds must be exceeded before excess information rate is allowed.	0x0
SE_DLB_SPORT_ENA	1	R/W	Enable source port awareness by the DLB shaper. If set, the DLB shaper allows excess information rate when the ingress buffer use for source port SE_DLB_SPORT has reached threshold BUF_P_RSRV_I[SE_DLB_SPORT] minus 3000 bytes. If multiple awareness functions (SE_DLB_PRIO_ENA, SE_DLB_SPORT_ENA, SE_DLB_DPORT_ENA) are enabled, all relevant thresholds must be exceeded before excess information rate is allowed.	0x0

TABLE 1-515: FIELDS IN SE_DLB_SENSE (CONTINUED)

Field Name	Bit	Access	Description	Default
SE_DLB_DPORT_ENA	0	R/W	Enable destination port awareness by the DLB shaper. If set, the DLB shaper allows excess information rate when the egress buffer use for destination port SE_DL-B_SPORT has reached threshold BUF_P_RSRV_E[SE_DLB_DPORT] minus 3000 bytes. If multiple awareness functions (SE_DL-B_PRIO_ENA, SE_DLB_SPORT_ENA, SE_DLB_DPORT_ENA) are enabled, all rel-evant thresholds must be exceeded before excess information rate is allowed.	0x0

1.11.7.7 QSYS:HSCH:CIR_STATE

Parent: QSYS:HSCH

Instances: 1

TABLE 1-516: FIELDS IN CIR_STATE

Field Name	Bit	Access	Description	Default
CIR_LVL	25:4	R/W	Current fill level. Unit is 0.5 bits.	0x000000

1.11.7.8 QSYS:HSCH:EIR_STATE

Parent: QSYS:HSCH

Instances: 1

TABLE 1-517: FIELDS IN EIR_STATE

Field Name	Bit	Access	Description	Default
EIR_LVL	21:0	R/W	Current fill level. Unit is 0.5 bits.	0x000000

1.11.8 QSYS:HSCH_MISC

Parent: QSYS

Instances: 1

TABLE 1-518: REGISTERS IN HSCH_MISC

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
HSCH_MISC_CFG	0x00000000	1	Common config for HSCH and policer module	Page 227

1.11.8.1 QSYS:HSCH_MISC:HSCH_MISC_CFG

Parent: QSYS:HSCH_MISC

Instances: 1

TABLE 1-519: FIELDS IN HSCH_MISC_CFG

Field Name	Bit	Access	Description	Default
SE_CONNECT_VLD	8	R/W	Set to one when the SE connection configuration is valid. Set to zero when reconfiguring SE inter connections	0x1
FRM_ADJ	7:3	R/W	Values to add each frame when frame length adjustment is in use.	0x14
QSHP_EXC_ENA	1	R/W	When set closed queue shapers will be schedulled as excessed, and can be scheduled if no other inputs are available.	0x0

1.12 REW

TABLE 1-520: REGISTER GROUPS IN REW

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
PORT	0x00000000	13 0x00000080	Per port configurations for Rewriter	Page 228
COMMON	0x00000690	1	Common configurations for Rewriter	Page 231

1.12.1 REW:PORT

Parent: REW

Instances: 13

TABLE 1-521: REGISTERS IN PORT

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PORT_VLAN_CFG	0x00000000	1	Port VLAN configuration	Page 228
TAG_CFG	0x00000004	1	Tagging configuration	Page 229
PORT_CFG	0x00000008	1	Special port configuration	Page 229
DSCP_CFG	0x0000000C	1	DSCP updates	Page 230
PCP_DEI_QOS_MAP_CFG	0x00000010	16 0x00000004	Mapping of DP level and QoS class to PCP and DEI values	Page 230
PTP_CFG	0x00000050	1	Precision time protocol configuration	Page 231
PTP_DLY1_CFG	0x00000054	1	Asymmetric delay	Page 231

1.12.1.1 REW:PORT:PORT_VLAN_CFG

Parent: REW:PORT

Instances: 1

TABLE 1-522: FIELDS IN PORT_VLAN_CFG

Field Name	Bit	Access	Description	Default
PORT_TPID	31:16	R/W	Tag Protocol Identifier for port.	0x0000
PORT_DEI	15	R/W	DEI value for port.	0x0
PORT_PCP	14:12	R/W	PCP value for port.	0x0
PORT_VID	11:0	R/W	VID value for port.	0x001

1.12.1.2 REW:PORT:TAG_CFG

Parent: REW:PORT

Instances: 1

TABLE 1-523: FIELDS IN TAG_CFG

Field Name	Bit	Access	Description	Default
TAG_CFG	8:7	R/W	Enable VLAN port tagging. 0: Port tagging disabled. 1: Tag all frames, except when VID=PORT_VLAN_CFG.PORT_VID or VID=0. 2: Tag all frames, except when VID=0. 3: Tag all frames.	0x0
TAG_TPID_CFG	6:5	R/W	Select TPID EtherType in port tag. 0: Use 0x8100. 1: Use 0x88A8. 2: Use custom value from PORT_VLAN_CFG.PORT_TPID. 3: Use PORT_VLAN_CFG.PORT_TPID, unless ingress tag was a C-tag (EtherType = 0x8100)	0x0
TAG_VID_CFG	4	R/W	Select VID in port tag. 0: Use classified VID. 1: Use PORT_VLAN_CFG.PORT_VID.	0x0
TAG_PCP_CFG	3:2	R/W	Select PCP in port tag. 0: Classified PCP 1: PORT_PCP 2: DP and QoS mapped to PCP (PCP_DEI_QOS_MAP_CFG) 3: QoS class	0x0
TAG_DEI_CFG	1:0	R/W	Select DEI in port tag. 0: Classified DEI 1: PORT_DEI 2: DP and QoS mapped to DEI (PCP_DEI_QOS_MAP_CFG) 3: DP level	0x0

1.12.1.3 REW:PORT:PORT_CFG

Parent: REW:PORT

Instances: 1

TABLE 1-524: FIELDS IN PORT_CFG

Field Name	Bit	Access	Description	Default
ES0_ENA	5	R/W	Enable ES0 lookup.	0x0
FCS_UPDATE_NONCPU_CFG	4:3	R/W	FCS update mode for frames not received on the CPU port. 0: Update FCS if frame data has changed 1: Never update FCS 2: Always update FCS	0x0
FCS_UPDATE_CPU_ENA	2	R/W	If set, update FCS for all frames injected by the CPU. If cleared, never update the FCS.	0x1
FLUSH_ENA	1	R/W	If set, all frames destined for the egress port are discarded.	0x0
AGE_DIS	0	R/W	Disable frame ageing for this egress port.	0x0

1.12.1.4 REW:PORT:DSCP_CFG

Parent: REW:PORT

Instances: 1

TABLE 1-525: FIELDS IN DSCP_CFG

Field Name	Bit	Access	Description	Default
DSCP_REWR_CFG	1:0	R/W	Egress DSCP rewrite. 0: No update of DSCP value in frame. 1: Update with DSCP value from analyzer. 2: Update with DSCP value from analyzer remapped through DSCP_REMAP_CFG. 3. Update with DSCP value from analyzer remapped based on drop precedence level through DSCP_REMAP_CFG or DSCP_REMAP_DP1_CFGl.	0x0

1.12.1.5 REW:PORT:PCP_DEI_QOS_MAP_CFG

Parent: REW:PORT

Instances: 16

TABLE 1-526: FIELDS IN PCP_DEI_QOS_MAP_CFG

Field Name	Bit	Access	Description	Default
DEI_QOS_VAL	3	R/W	Map the frame's DP level and QoS class to a DEI value. DEI = PCP_DEI_QOS_MAP_CFG[8*DP level + QoS class].DEI_QOS_VAL. This must be enabled in TAG_CFG.TAG_DEI_CFG.	0x0
PCP_QOS_VAL	2:0	R/W	Map the frame's DP level and QoS class to a PCP value. PCP = PCP_DEI_QOS_MAP_CFG[8*DP level + QoS class].PCP_QOS_VAL. This must be enabled in TAG_CFG.TAG_PCP_CFG.	0x0

1.12.1.6 REW:PORT:PTP_CFG

Parent: REW:PORT

Instances: 1

TABLE 1-527: FIELDS IN PTP_CFG

Field Name	Bit	Access	Description	Default
PTP_BACKPLANE_MODE	7	R/W	Backplane mode for PTP. If set, the frame's receive timestamp is written into the PTP header (4 reserved bytes at offset 16).	0x0
PTP_1STEP_DIS	2	R/W	Overrules the one-step and the origin PTP commands from IS2. This disables updating the correction field or the origin timestamp field in the PTP frame.	0x0
PTP_2STEP_DIS	1	R/W	Overrules the two-step PTP command from IS2. This effectively disables saving the frame's departure time into the timestamp FIFO queue.	0x0

1.12.1.7 REW:PORT:PTP_DLY1_CFG

Parent: REW:PORT

Instances: 1

TABLE 1-528: FIELDS IN PTP_DLY1_CFG

Field Name	Bit	Access	Description	Default
PTP_DLY1_VAL	31:0	R/W	Delay to add to frame's residence time. This is applicable to one-step PTP and it is enabled by setting the IS2 action REW_OP[5] to 1. Unit is ns. Value is signed.	0x00000000

1.12.2 REW:COMMON

Parent: REW

Instances: 1

TABLE 1-529: REGISTERS IN COMMON

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
DSCP_REMAP_DP1_CFG	0x00000000	64 0x00000004	Remap table of DSCP values for frames with drop precedence set	Page 231
DSCP_REMAP_CFG	0x00000100	64 0x00000004	Remap table of DSCP values	Page 232

1.12.2.1 REW:COMMON:DSCP_REMAP_DP1_CFG

Parent: REW:COMMON

Instances: 64

TABLE 1-530: FIELDS IN DSCP_REMAP_DP1_CFG

Field Name	Bit	Access	Description	Default
DSCP_REMAP_DP1_VAL	5:0	R/W	One to one DSCP remapping table common for all ports. This table is used if ANA::DSCP_CFG[DSCP].DSCP_RE-WR_ENA=3 and DP=1.	0x00

1.12.2.2 REW:COMMON:DSCP_REMAP_CFG

Parent: REW:COMMON

Instances: 64

TABLE 1-531: FIELDS IN DSCP_REMAP_CFG

Field Name	Bit	Access	Description	Default
DSCP_REMAP_VAL	5:0	R/W	One to one DSCP remapping table common for all ports. This table is used if ANA::DSCP_CFG[DSCP].DSCP_RE-WR_ENA=2 or if DSCP_CFG[DSCP].DSCP_REWR_ENA=3 and DP=0.	0x00

1.13 SBA

TABLE 1-532: REGISTER GROUPS IN SBA

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
SBA	0x00000000	1	Shared bus arbiter registers	Page 232

1.13.1 SBA:SBA

Parent: SBA

Instances: 1

Configurations for the shared bus of the VCore System.

TABLE 1-533: REGISTERS IN SBA

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PL_CPU	0x00000000	1	Master 1 arbitration priority	Page 233
PL_PCIE	0x00000004	1	Master 2 arbitration priority	Page 233
PL_CSR	0x00000008	1	Master 3 arbitration priority	Page 233
WT_EN	0x0000004C	1	Weighted-token arbitration scheme enable	Page 233
WT_TCL	0x00000050	1	Clock tokens refresh period	Page 234
WT_CPU	0x00000054	1	Master 1 clock tokens	Page 234
WT_PCIE	0x00000058	1	Master 2 clock tokens	Page 234

TABLE 1-533: REGISTERS IN SBA (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
WT_CSR	0x0000005C	1	Master 3 clock tokens	Page 234

1.13.1.1 SBA:SBA:PL_CPU

Parent: SBA:SBA

Instances: 1

TABLE 1-534: FIELDS IN PL_CPU

Field Name	Bit	Access	Description	Default
PL1	3:0	R/W	Arbitration priority for the master. When multiple masters request the bus at the same time, the one with the highest priority is granted bus access. Values 0x1 through 0xF, higher values are prioritized over lower values.	0xE

1.13.1.2 SBA:SBA:PL_PCIE

Parent: SBA:SBA

Instances: 1

TABLE 1-535: FIELDS IN PL_PCIE

Field Name	Bit	Access	Description	Default
PL2	3:0	R/W	See SBA::PL1 for description.	0xD

1.13.1.3 SBA:SBA:PL_CSR

Parent: SBA:SBA

Instances: 1

TABLE 1-536: FIELDS IN PL_CSR

Field Name	Bit	Access	Description	Default
PL3	3:0	R/W	See SBA::PL1 for description.	0xC

1.13.1.4 SBA:SBA:WT_EN

Parent: SBA:SBA

Instances: 1

When weighted token arbitration is enabled, each master on the shared bus is granted a configurable number of tokens at the start of each refresh period. The length of each refresh period is configurable. In each clock-cycle that a master uses the bus, the token counter for that master decreases. Once all tokens are spent, the master is forced to a low priority. A master with tokens remaining, always takes priority over masters with no tokens remaining.

TABLE 1-537: FIELDS IN WT_EN

Field Name	Bit	Access	Description	Default
WT_EN	0	R/W	Set this field to enable weighted-token arbitration scheme.	0x0

1.13.1.5 SBA:SBA:WT_TCL

Parent: SBA:SBA

Instances: 1

TABLE 1-538: FIELDS IN WT_TCL

Field Name	Bit	Access	Description	Default
WT_TCL	15:0	R/W	Refresh period length for the weighted-token arbitration scheme.	0xFFFF

1.13.1.6 SBA:SBA:WT_CPU

Parent: SBA:SBA

Instances: 1

TABLE 1-539: FIELDS IN WT_CPU

Field Name	Bit	Access	Description	Default
WT_CL1	15:0	R/W	Number of tokens to grant the master at the start of each refresh period for weighted-token arbitration scheme. If configured with a value of zero, the master is considered to have infinite tokens.	0x000F

1.13.1.7 SBA:SBA:WT_PCIE

Parent: SBA:SBA

Instances: 1

TABLE 1-540: FIELDS IN WT_PCIE

Field Name	Bit	Access	Description	Default
WT_CL2	15:0	R/W	See SBA::WT_CL1 for description.	0x000F

1.13.1.8 SBA:SBA:WT_CSR

Parent: SBA:SBA

Instances: 1

TABLE 1-541: FIELDS IN WT_CSR

Field Name	Bit	Access	Description	Default
WT_CL3	15:0	R/W	See SBA::WT_CL1 for description.	0x000F

1.14 SIMC

TABLE 1-542: REGISTER GROUPS IN SIMC

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
SIMC	0x00000000	1	SI Master Controller	Page 235

1.14.1 SIMC:SIMC

Parent: SIMC

Instances: 1

TABLE 1-543: REGISTERS IN SIMC

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CTRLR0	0x00000000	1	Control Register 0	Page 235
CTRLR1	0x00000004	1	Control Register 1	Page 237
SIMCEN	0x00000008	1	SIMC Enable	Page 237
SER	0x00000010	1	Slave Enable	Page 237
BAUDR	0x00000014	1	Baud Rate Select	Page 238
TXFTLR	0x00000018	1	Transmit FIFO Threshold Level	Page 238
RXFTLR	0x0000001C	1	Receive FIFO Threshold level	Page 238
TXFLR	0x00000020	1	Transmit FIFO Level	Page 239
RXFLR	0x00000024	1	Receive FIFO Level	Page 239
SR	0x00000028	1	Status Register	Page 239
IMR	0x0000002C	1	Interrupt Mask	Page 239
ISR	0x00000030	1	Interrupt Status	Page 240
RISR	0x00000034	1	Raw Interrupt Status	Page 240
TXOICR	0x00000038	1	Transmit FIFO Overflow Interrupt Clear	Page 241
RXOICR	0x0000003C	1	Receive FIFO Overflow Interrupt Clear	Page 241
RXUICR	0x00000040	1	Receive FIFO Underflow Interrupt Clear	Page 241
DR	0x00000060	36 0x00000004	Transmit/Receive FIFO	Page 241
RX_SAMPLE_DLY	0x000000F0	1	RXD Sample Delay	Page 242

1.14.1.1 SIMC:SIMC:CTRLR0

Parent: SIMC:SIMC

Instances: 1

This register controls the serial data transfer. This register can only be written when master is disabled (SIMC::SIMCEN.SIMCEN = 0).

TABLE 1-544: FIELDS IN CTRLR0

Field Name	Bit	Access	Description	Default
SRL	11	R/W	Shift Register Loop. Used for testing purposes only. Set to connect the transmit shift register output to the receive shift register input. 0: Normal Mode Operation 1: Test Mode Operation	0x0
TMOD	9:8	R/W	Selects the mode of transfer for serial communication. In transmit-only mode, data received from the external device is not valid and is not stored in the receive FIFO memory; it is overwritten on the next transfer. In receive-only mode, transmitted data are not valid. After the first write to the transmit FIFO, the same word is retransmitted for the duration of the transfer. In transmit-and-receive mode, both transmit and receive data are valid. The transfer continues until the transmit FIFO is empty. Data received from the external device are stored into the receive FIFO memory, where it can be accessed by the host processor. 0: Transmit and Receive. 1: Transmit Only. 2: Receive Only. 3: Reserved.	0x0
SCPOL	7	R/W	Valid when the frame format (FRF) is set to Motorola SPI. Used to select the polarity of the inactive serial clock, which is held inactive when the master is not actively transferring data on the serial bus. 0: Inactive state of serial clock is low. 1: Inactive state of serial clock is high.	0x0
SCPH	6	R/W	Valid when the frame format (FRF) is set to Motorola SPI. The serial clock phase selects the relationship of the serial clock with the slave select signal. When SCPH = 0, data are captured on the first edge of the serial clock. When SCPH = 1, the serial clock starts toggling one cycle after the slave select line is activated, and data are captured on the second edge of the serial clock. 0: Serial clock toggles in middle of first data bit. 1: Serial clock toggles at start of first data bit.	0x0
FRF	5:4	R/W	Selects which serial protocol transfers the data. Note: In addition to this field, software must also configure ICPU_CFG::GENERAL_CTRL.SIMC_SSP_ENA. 0: Motorola SPI 1: Texas Instruments SSP 2-3: Reserved	0x0

TABLE 1-544: FIELDS IN CTRLR0 (CONTINUED)

Field Name	Bit	Access	Description	Default
DFS	3:0	R/W	Selects the data frame length. See SIMC::DR register description for how to read/write words of less than 16 bit. 0-2: Reserved. n: n+1 bit serial data transfer.	0x7

1.14.1.2 SIMC:SIMC:CTRLR1

Parent: SIMC:SIMC

Instances: 1

Control register 1 controls the end of serial transfers when in receive-only mode. This register can only be written when master is disabled (SIMC::SIMCEN.SIMCEN = 0).

TABLE 1-545: FIELDS IN CTRLR1

Field Name	Bit	Access	Description	Default
NDF	15:0	R/W	When SIMC::CTRLR0.TMOD = 2, this register field sets the number of data frames to be continuously received by the master. The master continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables receiving up to 64 KB of data in a continuous transfer.	0x0000

1.14.1.3 SIMC:SIMC:SIMCEN

Parent: SIMC:SIMC

Instances: 1

TABLE 1-546: FIELDS IN SIMCEN

Field Name	Bit	Access	Description	Default
SIMCEN	0	R/W	Set to enable master operations. When disabled, all serial transfers are halted immediately. Transmit and receive FIFO buffers are cleared when disabled. It is impossible to program some of the master control registers when enabled. Note: The SI Master Controller must own the SI interface before it is enabled, see ICPU_CFG::GENERAL_CTRL.IF_SI_OWNER for more information.	0x0

1.14.1.4 SIMC:SIMC:SER

Parent: SIMC:SIMC

Instances: 1

The register enables the individual slave select output lines from the master. 16 slave-select output pins are available on the master. This register can only be written when master is disabled and not busy.

TABLE 1-547: FIELDS IN SER

Field Name	Bit	Access	Description	Default
SER	15:0	R/W	Each bit in this register corresponds to a slave select line from the master. When a bit in this register is set, the corresponding slave select line from the master is activated when a serial transfer begins. Setting or clearing bits in this register have no effect on the corresponding slave select outputs until a transfer is started. Before beginning a transfer, enable the bit in this register that corresponds to the slave device with which the master wants to communicate. When not operating in broadcast mode, only one bit in this field should be set. 1: Selected 0: Not Selected	0x0000

1.14.1.5 SIMC:SIMC:BAUDR

Parent: SIMC:SIMC

Instances: 1

The register derives the frequency of the serial clock that regulates the data transfer. The 16-bit field in this register defines the SI divider value. This register can only be written when master is disabled (SIMC::SIMCEN.SIMCEN = 0).

TABLE 1-548: FIELDS IN BAUDR

Field Name	Bit	Access	Description	Default
SCKDV	15:0	R/W	The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (si_-clk) is disabled. The frequency of the si_clk is derived from the following equation: Fsclk_out = Fsystem_clk/SCKDV where SCKDV is any even value between 2 and 65534 and Fsystem_clk is 250MHz.	0x0000

1.14.1.6 SIMC:SIMC:TXFTLR

Parent: SIMC:SIMC

Instances: 1

TABLE 1-549: FIELDS IN TXFTLR

Field Name	Bit	Access	Description	Default
TFT	2:0	R/W	When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered. The transmit FIFO depth is 8, do not program value exceeding 7.	0x0

1.14.1.7 SIMC:SIMC:RXFTLR

Parent: SIMC:SIMC

Instances: 1

TABLE 1-550: FIELDS IN RXFTLR

Field Name	Bit	Access	Description	Default
RFT	5:0	R/W	When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered. The receive FIFO depth is 40, do not program value exceeding 39.	0x00

1.14.1.8 SIMC:SIMC:TXFLR

Parent: SIMC:SIMC

Instances: 1

TABLE 1-551: FIELDS IN TXFLR

Field Name	Bit	Access	Description	Default
TXTFL	2:0	R/O	Contains the number of valid data entries in the transmit FIFO.	0x0

1.14.1.9 SIMC:SIMC:RXFLR

Parent: SIMC:SIMC

Instances: 1

TABLE 1-552: FIELDS IN RXFLR

Field Name	Bit	Access	Description	Default
RXTFL	5:0	R/O	Contains the number of valid data entries in the receive FIFO.	0x00

1.14.1.10 SIMC:SIMC:SR

Parent: SIMC:SIMC

Instances: 1

TABLE 1-553: FIELDS IN SR

Field Name	Bit	Access	Description	Default
RFF	4	R/O	Set when receive FIFO is full.	0x0
RFNE	3	R/O	Set when receive FIFO has one or more data-word.	0x0
TFE	2	R/O	Set when transmit FIFO is empty.	0x1
TFNF	1	R/O	Set when transmit FIFO has room for one or more data-word.	0x1
BUSY	0	R/O	Set when serial transfer is in progress. Cleared when master is idle or disabled.	0x0

1.14.1.11 SIMC:SIMC:IMR

Parent: SIMC:SIMC

Instances: 1

TABLE 1-554: FIELDS IN IMR

Field Name	Bit	Access	Description	Default
RESERVED	5	R/W	Must be set to its default.	0x1
RXFIM	4	R/W	Set to enable Receive FIFO Full Interrupt	0x1
RXOIM	3	R/W	Set to enable Receive FIFO Overflow Interrupt	0x1
RXUIM	2	R/W	Set to enable Receive FIFO Underflow Interrupt	0x1
TXOIM	1	R/W	Set to enable Transmit FIFO Overflow Interrupt	0x1
TXEIM	0	R/W	Set to enable Transmit FIFO Empty Interrupt	0x1

1.14.1.12 SIMC:SIMC:ISR

Parent: SIMC:SIMC

Instances: 1

If any bit is set in this register, then the SI Master Controller is indicating interrupt towards the VCore Interrupt Controller.

TABLE 1-555: FIELDS IN ISR

Field Name	Bit	Access	Description	Default
RXFIS	4	R/O	Receive FIFO Full Interrupt Status, this field is masked by SIMC::IMR.RXFIM. This interrupt is based on programmable fill level, see SIMC::RXFTLR for more information.	0x0
RXOIS	3	R/O	Receive FIFO Overflow Interrupt Status, this field is masked by SIMC::IMR.RXOIM.	0x0
RXUIS	2	R/O	Receive FIFO Underflow Interrupt Status, this field is masked by SIMC::IMR.RXUIM.	0x0
TXOIS	1	R/O	Transmit FIFO Overflow Interrupt Status, this field is masked by SIMC::IMR.TXOIM.	0x0
TXEIS	0	R/O	Transmit FIFO Empty Interrupt Status, this field is masked by SIMC::IMR.TXEIM. This interrupt is based on programmable fill level, see SIMC::TXFTLR for more information.	0x0

1.14.1.13 SIMC:SIMC:RISR

Parent: SIMC:SIMC

Instances: 1

TABLE 1-556: FIELDS IN RISR

Field Name	Bit	Access	Description	Default
RXFIR	4	R/O	Current status of Receive FIFO Full Interrupt before masking	0x0
RXOIR	3	R/O	Current status of Receive FIFO Overflow Interrupt before masking	0x0
RXUIR	2	R/O	Current status of Receive FIFO Underflow Interrupt before masking	0x0

TABLE 1-556: FIELDS IN RISR (CONTINUED)

Field Name	Bit	Access	Description	Default
TXOIR	1	R/O	Current status of Transmit FIFO Overflow Interrupt before masking	0x0
TXEIR	0	R/O	Current status of Transmit FIFO Empty Interrupt before masking	0x0

1.14.1.14 SIMC:SIMC:TXOICR

Parent: SIMC:SIMC

Instances: 1

TABLE 1-557: FIELDS IN TXOICR

Field Name	Bit	Access	Description	Default
TXOICR	0	R/O	This field is set when Transmit FIFO Overflow Interrupt is active, interrupt is cleared by reading this register.	0x0

1.14.1.15 SIMC:SIMC:RXOICR

Parent: SIMC:SIMC

Instances: 1

TABLE 1-558: FIELDS IN RXOICR

Field Name	Bit	Access	Description	Default
RXOICR	0	R/O	This field is set when Receive FIFO Overflow Interrupt is active, interrupt is cleared by reading this register.	0x0

1.14.1.16 SIMC:SIMC:RXUICR

Parent: SIMC:SIMC

Instances: 1

TABLE 1-559: FIELDS IN RXUICR

Field Name	Bit	Access	Description	Default
RXUICR	0	R/O	This field is set when Receive FIFO Underflow Interrupt is active, interrupt is cleared by reading this register.	0x0

1.14.1.17 SIMC:SIMC:DR

Parent: SIMC:SIMC

Instances: 36

16-bit read/write buffer for the transmit/receive FIFOs. When the register is read, data in the receive FIFO buffer is accessed. When it is written to, data are moved into the transmit FIFO buffer; a write can occur only when SIMC::SIMCEN.SIMCEN = 1. FIFOs are reset when SIMC::SIMCEN.SIMCEN = 0. This register is replicated to allow burst access to fifo's; the replication index is not used when accessing the FIFO.

TABLE 1-560: FIELDS IN DR

Field Name	Bit	Access	Description	Default
DR	15:0	R/W	Data is aligned to bit 0 (right-justified) when accessing less than 16 bit data-words. Read = Receive FIFO buffer. Write = Transmit FIFO buffer.	0x0000

1.14.1.18 SIMC:SIMC:RX_SAMPLE_DLY

Parent: SIMC:SIMC

Instances: 1

This register controls the number of VCore system clock cycles that are delayed -from the default sample time- before the actual sample of the rxd input signal occurs. It is impossible to write to this register when the SSI is enabled; the SSI is enabled and disabled by writing to the SIMCEN register.

TABLE 1-561: FIELDS IN RX_SAMPLE_DLY

Field Name	Bit	Access	Description	Default
RSD	7:0	R/W	This field is used to delay the sample of the rxd input signal. Each value represents a single VCore system clock delay on the sample of the rxd signal. If this field is programmed with a value that exceeds 25, a zero (0) delay will be applied to the rxd sample.	0x00

1.15 SYS

TABLE 1-562: REGISTER GROUPS IN SYS

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
SYSTEM	0x00000508	1	Switch configuration	Page 242
PAUSE_CFG	0x00000608	1	Watermarks for egress queue system	Page 246
MMGT	0x0000069C	1	Memory manager status	Page 249
STAT	0x00000000	192 0x00000004	Frame statistics	Page 249
PTP	0x000006B8	1	Precision Time Protocol configuration	Page 250

1.15.1 SYS:SYSTEM

Parent: SYS

Instances: 1

TABLE 1-563: REGISTERS IN SYSTEM

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
RESET_CFG	0x00000000	1	Core reset control	Page 243
VLAN_ETYPE_CFG	0x00000008	1	S-tag Ethernet Type	Page 243
PORT_MODE	0x0000000C	13 0x00000004	Per device port configuration	Page 243
FRONT_PORT_MODE	0x00000040	11 0x00000004	Various Ethernet port configurations per front port	Page 245
FRM_AGING	0x0000006C	1	Frame aging configuration	Page 245
STAT_CFG	0x00000070	1	Statistics configuration	Page 245
REW_MAC_HIGH_CFG	0x000000A8	11 0x00000004	Mac address to patch into frames transmitted	Page 246
REW_MAC_LOW_CFG	0x000000D4	11 0x00000004	Mac address to patch into frames transmitted	Page 246

1.15.1.1 SYS:SYSTEM:RESET_CFG

Parent: SYS:SYSTEM

Instances: 1

Controls reset and initialization of the switching core. Proper startup sequence is:

- Enable memories
- Initialize memories
- Enable core

TABLE 1-564: FIELDS IN RESET_CFG

Field Name	Bit	Access	Description	Default
CORE_ENA	2	R/W	Switch core is enabled when this field is set.	0x0
MEM_ENA	1	R/W	Core memory controllers are enabled when this field is set.	0x0
MEM_INIT	0	One-shot	Initialize core memories. Field is automatically cleared when operation is complete (approx. 40 us).	0x0

1.15.1.2 SYS:SYSTEM:VLAN_ETYPE_CFG

Parent: SYS:SYSTEM

Instances: 1

TABLE 1-565: FIELDS IN VLAN_ETYPE_CFG

Field Name	Bit	Access	Description	Default
VLAN_S_TAG_ETYPE_VAL	15:0	R/W	Custom Ethernet Type for S-tags. Tags with TPID = 0x88A8 are always recognized as S-tags.	0x88A8

1.15.1.3 SYS:SYSTEM:PORT_MODE

Parent: SYS:SYSTEM

Instances: 13

These configurations exists per front port and for each of the two CPU ports (11+12).

TABLE 1-566: FIELDS IN PORT_MODE

Field Name	Bit	Access	Description	Default
DATA_WO_TS	6:5	R/W		0x0
INCL_INJ_HDR	4:3	R/W	Set the mode for the formatting of incoming frames. If INCL_INJ_HDR>0, incoming frames are expected to contain the selected prefix followed by the 16-byte CPU injection header as the first part of the frame. Frames are forwarded based on the contents in the CPU injection header instead of normal forwarding. Three different prefixes are supported: - No prefix. - Short prefix: 0x8880000A. - Long prefix: any DMAC, any SMAC, EtherType=0x8880, payload=0x000A. In modes 2 and 3, if the incoming frame's format does not comply with the prefix, then sticky bit INJ_HDR_PREFIX_ERR is set. A non-complying frame is discarded. 0: No CPU injection header (normal frames) 1: CPU injection header without prefix 2: CPU injection header with short prefix 3: CPU injection header with long prefix	0x0
INCL_XTR_HDR	2:1	R/W	Set the mode for the formatting of outgoing frames. If INCL_XTR_HDR>0, outgoing frames are prepended the selected prefix followed by the 16-byte CPU extraction header as the first part of the frame. Inserting the CPU extraction header prevents other rewriter operations on the same frame. Three different prefixes are supported: - No prefix. - Short prefix: 0x8880000A. - Long prefix: DMAC=0xFFFFFFFFFFFF, SMAC=0xFEFFFFFFFFFF, EtherType=0x8880, payload=0x000A. 0: No CPU extraction header (normal frames) 1: CPU extraction header without prefix 2: CPU extraction header with short prefix 3: CPU extraction header with long prefix	0x0
INJ_HDR_ERR	0	Sticky	If set, a frame has been received with prefix not complying with the setting in INCL_INJ_HDR.	0x0

1.15.1.4 SYS:SYSTEM:FRONT_PORT_MODE

Parent: SYS:SYSTEM

Instances: 11

TABLE 1-567: FIELDS IN FRONT_PORT_MODE

Field Name	Bit	Access	Description	Default
HDX_MODE	0	R/W	Enables the queue system to support the half-duplex mode. Must be set for a port when enabled for half-duplex mode (MAC_-MODE_ENA.FDX_ENA cleared).	0x0

1.15.1.5 SYS:SYSTEM:FRM_AGING

Parent: SYS:SYSTEM

Instances: 1

TABLE 1-568: FIELDS IN FRM_AGING

Field Name	Bit	Access	Description	Default
AGE_TX_ENA	20	R/W	If set, frames exceeding the frame aging time while waiting head-of-line in a port due to a link partner signaling pause are allowed to be aged. Note that frames aged in this case are not counted by the normal frame aging counter C_TX_AGED.	0x1
MAX_AGE	19:0	R/W	Frames are aged and removed from the queue system when the frame's age timer becomes two. The frame age timer is increased for all frames whenever the configured time, MAX_AGE, has passed. The unit is 6.5us. Effectively, this means that a frame is aged when the frame has waited in the queue system between one or two times the period specified by MAX_AGE. A value of zero disables frame aging.	0x00000

1.15.1.6 SYS:SYSTEM:STAT_CFG

Parent: SYS:SYSTEM

Instances: 1

TABLE 1-569: FIELDS IN STAT_CFG

Field Name	Bit	Access	Description	Default
STAT_CLEAR_SHOT	12:10	One-shot	Set STAT_CLEAR_SHOT to clear counters in the counter group for the port selected by STAT_VIEW. Auto-cleared when complete (1us). Multiple counter groups can be cleared at the same time by setting multiple bits in STAT_CLEAR_SHOT. Bit 0: Group 0 - Rx counters. Bit 1: Group 1 - Tx counters. Bit 2: Group 2 - Drop counters.	0x0
STAT_VIEW	3:0	R/W	Selects the port, which counters are readable through the SYS:STAT:CNT register or can be cleared through STAT_CLEAR_SHOT.	0x0

1.15.1.7 SYS:SYSTEM:REW_MAC_HIGH_CFG

Parent: SYS:SYSTEM

Instances: 11

TABLE 1-570: FIELDS IN REW_MAC_HIGH_CFG

Field Name	Bit	Access	Description	Default
REW_MAC_HIGH	15:0	R/W	Upper part of MAC address used when replacing source MAC address. VCAP_IS2 action SMAC_REPLACE_ENA enables replacement of the source MAC address	0x0000

1.15.1.8 SYS:SYSTEM:REW_MAC_LOW_CFG

Parent: SYS:SYSTEM

Instances: 11

TABLE 1-571: FIELDS IN REW_MAC_LOW_CFG

Field Name	Bit	Access	Description	Default
REW_MAC_LOW	31:0	R/W	Lower part of MAC address used when replacing source MAC address. VCAP_IS2 action SMAC_REPLACE_ENA enables replacement of the source MAC address	0x00000000

1.15.2 SYS:PAUSE_CFG

Parent: SYS

Instances: 1

TABLE 1-572: REGISTERS IN PAUSE_CFG

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PAUSE_CFG	0x00000000	12 0x00000004	Watermarks for flow control condition per switch port.	Page 247
PAUSE_TOT_CFG	0x00000030	1	Configure total memory pause condition	Page 247
ATOP	0x00000034	12 0x00000004	Tail dropping level	Page 248
ATOP_TOT_CFG	0x00000064	1	Total raw memory use before tail dropping is activated	Page 248
MAC_FC_CFG	0x00000068	11 0x00000004	MAC Flow Control Configuration Register	Page 248

1.15.2.1 SYS:PAUSE_CFG:PAUSE_CFG

Parent: SYS:PAUSE_CFG

Instances: 12

TABLE 1-573: FIELDS IN PAUSE_CFG

Field Name	Bit	Access	Description	Default
PAUSE_START	18:10	R/W	Start pausing ingress stream when the amount of memory consumed by the port exceeds this watermark. The TOTPAUSE condition must also be met. See RES_CFG	0x1FF
PAUSE_STOP	9:1	R/W	Stop pausing ingress stream when the amount of memory consumed by the port is below this watermark. See RES_CFG.	0x1FF
PAUSE_ENA	0	R/W	Enable pause feedback to the MAC, allowing transmission of pause frames or HDX collisions to limit ingress data rate.	0x0

1.15.2.2 SYS:PAUSE_CFG:PAUSE_TOT_CFG

Parent: SYS:PAUSE_CFG

Instances: 1

TABLE 1-574: FIELDS IN PAUSE_TOT_CFG

Field Name	Bit	Access	Description	Default
PAUSE_TOT_START	17:9	R/W	Assert TOTPAUSE condition when total memory allocation is above this watermark. See RES_CFG	0x000
PAUSE_TOT_STOP	8:0	R/W	Deassert TOTPAUSE condition when total memory allocation is below this watermark. See RES_CFG	0x000

1.15.2.3 SYS:PAUSE_CFG:ATOP

Parent: SYS:PAUSE_CFG

Instances: 12

TABLE 1-575: FIELDS IN ATOP

Field Name	Bit	Access	Description	Default
ATOP	8:0	R/W	When a source port consumes more than this level in the packet memory, frames are tail dropped, unconditionally of destination. See RES_CFG	0x1FF

1.15.2.4 SYS:PAUSE_CFG:ATOP_TOT_CFG

Parent: SYS:PAUSE_CFG

Instances: 1

TABLE 1-576: FIELDS IN ATOP_TOT_CFG

Field Name	Bit	Access	Description	Default
ATOP_TOT	8:0	R/W	Tail dropping is activate on a port when the port use has exceeded the ATOP watermark for the port, and the total memory use has exceeded this watermark. See RES_CFG	0x1FF

1.15.2.5 SYS:PAUSE_CFG:MAC_FC_CFG

Parent: SYS:PAUSE_CFG

Instances: 11

TABLE 1-577: FIELDS IN MAC_FC_CFG

Field Name	Bit	Access	Description	Default
FC_LINK_SPEED	27:26	R/W	Configures the link speed. This is used to evaluate the time specification in incoming pause frames. 0: 2500 Mbps 1: 1000 Mbps 2: 100 Mbps 3: 10 Mbps	0x1
FC_LATENCY_CFG	25:20	R/W	Accepted reaction time for link partner after the port has transmitted a pause frame. Frames starting after this latency are aborted. Unit is 64 byte times.	0x07
ZERO_PAUSE_ENA	18	R/W	If set, a zero-delay pause frame is transmitted when flow control is deasserted. '0': Don't send zero pause frame. '1': Send zero pause frame.	0x0
TX_FC_ENA	17	R/W	When set the MAC will send pause control frames in the Tx direction. '0': Don't send pause control frames '1': Send pause control frames	0x0

TABLE 1-577: FIELDS IN MAC_FC_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
RX_FC_ENA	16	R/W	When set the MAC obeys received pause control frames '0': Don't obey received pause control frames '1': Obey received pause control frames.	0x0
PAUSE_VAL_CFG	15:0	R/W	Pause timer value inserted in generated pause frames. 0: Insert timer value 0 in TX pause frame. ... N: Insert timer value N in TX pause frame.	0x0000

1.15.3 SYS:MMGT

Parent: SYS

Instances: 1

TABLE 1-578: REGISTERS IN MMGT

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
MMGT	0x00000000	1	Packet memory status	Page 249

1.15.3.1 SYS:MMGT:MMGT

Parent: SYS:MMGT

Instances: 1

TABLE 1-579: FIELDS IN MMGT

Field Name	Bit	Access	Description	Default
FREECNT	15:0	R/O	Number of 192-byte free memory words.	0x0000

1.15.4 SYS:STAT

Parent: SYS

Instances: 192

TABLE 1-580: REGISTERS IN STAT

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CNT	0x00000000	1	Counter values	Page 249

1.15.4.1 SYS:STAT:CNT

Parent: SYS:STAT

Instances: 1

TABLE 1-581: FIELDS IN CNT

Field Name	Bit	Access	Description	Default
CNT	31:0	R/W	Counter values. The counters are layed-out in three counter groups: Group 0: 0-63: Receive counters for port specified in STAT_CFG.STAT_VIEW. Group 1: 64-127: Transmit counters for port specified in STAT_CFG.STAT_VIEW. Group 2: 128-191: Drop counters for port specified in STAT_CFG.STAT_VIEW. QSYS::STAT_CNT_CFG and ANA::AGENC-TRL control whether bytes or frames are counted for specific counters. Counters are cleared through STAT_CFG.STAT_CLEAR_-SHOT.	0x00000000

1.15.5 SYS:PTP

Parent: SYS

Instances: 1

TABLE 1-582: REGISTERS IN PTP

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PTP_STATUS	0x00000000	1	Stored timestamp and time-stamp queue status	Page 250
PTP_TXSTAMP	0x00000004	1	Timestamp value	Page 251
PTP_NXT	0x00000008	1	Advancing the timestamp queue	Page 251
PTP_CFG	0x0000000C	1	System configuration of PTP	Page 251

1.15.5.1 SYS:PTP:PTP_STATUS

Parent: SYS:PTP

Instances: 1

TABLE 1-583: FIELDS IN PTP_STATUS

Field Name	Bit	Access	Description	Default
PTP_OVFL	28	R/O	If set, the timestamp queue has overflown implying a timestamp entry could not be enqueued. The PTP_OVFL bit is not cleared until the timestamp queue is completely empty.	0x0
PTP_MESS_VLD	27	R/O	A timestamp entry is ready for reading. PTP_MESS_ID, PTP_MESS_TXPORT, and PTP_DELAY contain the data of the time-stamp entry.	0x0
PTP_MESS_ID	26:21	R/O	Timestamp identifier for head-of-line time-stamp entry.	0x00

TABLE 1-583: FIELDS IN PTP_STATUS (CONTINUED)

Field Name	Bit	Access	Description	Default
PTP_MESS_TXPORT	20:16	R/O	The transmit port for the head-of-line time-stamp entry.	0x00
PTP_MESS_SEQ_ID	15:0	R/O	Timestamp sequence identifier for head-of-line timestamp entry.	0x0000

1.15.5.2 SYS:PTP:PTP_TXSTAMP

Parent: SYS:PTP

Instances: 1

TABLE 1-584: FIELDS IN PTP_TXSTAMP

Field Name	Bit	Access	Description	Default
PTP_TXSTAMP_SEC	31	R/O	The timestamp value for the head-of-line timestamp entry. The timestamp value is the frame's departure time plus DEV:PORT_-MODE:TX_PATH_DELAY.TX_PATH_DE-LAY. This is the LSB of the TOD_SEC value at time of event.	0x0
PTP_TXSTAMP	29:0	R/O	The timestamp value for the head-of-line timestamp entry. The timestamp value is the frame's departure time plus DEV:PORT_-MODE:TX_PATH_DELAY.TX_PATH_DE-LAY. Unit is ns.	0x00000000

1.15.5.3 SYS:PTP:PTP_NXT

Parent: SYS:PTP

Instances: 1

TABLE 1-585: FIELDS IN PTP_NXT

Field Name	Bit	Access	Description	Default
PTP_NXT	0	One-shot	Advance to the next timestamp entry. Registers PTP_STATUS and PTP_DELAY points to the next entry.	0x0

1.15.5.4 SYS:PTP:PTP_CFG

Parent: SYS:PTP

Instances: 1

TABLE 1-586: FIELDS IN PTP_CFG

Field Name	Bit	Access	Description	Default
PTP_STAMP_WID	7:2	R/W	Determines how many LSbits from the time-stamp value are used by the timestamp transfer function.	0x20

TABLE 1-586: FIELDS IN PTP_CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
PTP_CF_ROLL_MODE	1:0	R/W	Configures how rollover protection is done when doing add/subtract transfer. 0: The four LSbits of CF sub-nano is filled out with the MSbits of the timestamp. 1: The LSbit of the CF sub-nano field is set to the MSbit of the timestamp. 2: The CF bit 62 is set to the MSbit of the timestamp. 3: Reserved.	0x0

1.16 TWI

TABLE 1-587: REGISTER GROUPS IN TWI

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
TWI	0x00000000	1	Two-Wire Interface controller	Page 252

1.16.1 TWI:TWI

Parent: TWI

Instances: 1

TABLE 1-588: REGISTERS IN TWI

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CFG	0x00000000	1	TWI configuration	Page 253
TAR	0x00000004	1	Target address	Page 254
SAR	0x00000008	1	Slave address	Page 255
DATA_CMD	0x00000010	1	Rx/Tx data buffer and command	Page 255
SS_SCL_HCNT	0x00000014	1	Standard speed TWI clock SCL high count	Page 256
SS_SCL_LCNT	0x00000018	1	Standard speed TWI clock SCL low count	Page 257
FS_SCL_HCNT	0x0000001C	1	Fast speed TWI clock SCL high count	Page 257
FS_SCL_LCNT	0x00000020	1	Fast speed TWI clock SCL low count	Page 257
INTR_STAT	0x0000002C	1	Interrupt status	Page 258
INTR_MASK	0x00000030	1	Interrupt mask	Page 258
RAW_INTR_STAT	0x00000034	1	Raw interrupt status	Page 259
RX_TL	0x00000038	1	Receive FIFO threshold	Page 261
TX_TL	0x0000003C	1	Transmit FIFO threshold	Page 262
CLR_INTR	0x00000040	1	Clear combined and individual interrupt	Page 262
CLR_RX_UNDER	0x00000044	1	Clear RX_UNDER interrupt	Page 262

TABLE 1-588: REGISTERS IN TWI (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
CLR_RX_OVER	0x00000048	1	Clear RX_OVER interrupt	Page 263
CLR_TX_OVER	0x0000004C	1	Clear TX_OVER interrupt	Page 263
CLR_RD_REQ	0x00000050	1	Clear RD_REQ interrupt	Page 263
CLR_TX_ABRT	0x00000054	1	Clear TX_ABRT interrupt	Page 263
CLR_RX_DONE	0x00000058	1	Clear RX_DONE interrupt	Page 263
CLR_ACTIVITY	0x0000005C	1	Clear ACTIVITY interrupt	Page 264
CLR_STOP_DET	0x00000060	1	Clear STOP_DET interrupt	Page 264
CLR_START_DET	0x00000064	1	Clear START_DET interrupt	Page 264
CLR_GEN_CALL	0x00000068	1	Clear GEN_CALL interrupt	Page 264
CTRL	0x0000006C	1	TWI control	Page 265
STAT	0x00000070	1	TWI status	Page 265
TXFLR	0x00000074	1	Transmit FIFO level	Page 266
RXFLR	0x00000078	1	Receive FIFO level	Page 266
TX_ABRT_SOURCE	0x00000080	1	Transmit abort source	Page 267
SDA_SETUP	0x00000094	1	SDA setup	Page 268
ACK_GEN_CALL	0x00000098	1	Acknowledge general call	Page 269
ENABLE_STATUS	0x0000009C	1	Enable status	Page 269

1.16.1.1 TWI:TWI:CFG

Parent: TWI:TWI

Instances: 1

TABLE 1-589: FIELDS IN CFG

Field Name	Bit	Access	Description	Default
SLAVE_DIS	6	R/W	This bit controls whether the TWI controller has its slave disabled. If this bit is set (slave is disabled), the controller functions only as a master and does not perform any action that requires a slave. '0': slave is enabled '1': slave is disabled	0x1

TABLE 1-589: FIELDS IN CFG (CONTINUED)

Field Name	Bit	Access	Description	Default
RESTART_ENA	5	R/W	Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several operations. When RESTART is disabled, the master is prohibited from performing the following functions: * Change direction within a transfer (split) * Send a START BYTE * Combined format transfers in 7-bit addressing modes * Read operation with a 10-bit address * Send multiple bytes per transfer By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple transfers. If the above operations are performed, it will result in setting RAW_INTR_STAT.R_TX_ABRT. '0': disable '1': enable	0x1
MASTER_10BITADDR	4	R/W	Controls whether transfers starts in 7- or 10-bit addressing mode when acting as a master. '0': 7-bit addressing '1': 10-bit addressing	0x0
SLAVE_10BITADDR	3	R/W	Controls whether the the TWI controller responds to 7- or 10-bit addresses in slave mode. In 7-bit mode; transactions that involve 10-bit addressing are ignored and only the lower 7 bits of the SAR register are compared. '0': 7-bit addressing. '1': 10-bit addressing.	0x0
SPEED	2:1	R/W	These bits control at which speed the TWI controller operates; its setting is relevant only in master mode. Hardware protects against illegal values being programmed by software. '1': standard mode (100 kbit/s) '2': fast mode (400 kbit/s)	0x2
MASTER_ENA	0	R/W	This bit controls whether the TWI master is enabled. '0': master disabled '1': master enabled	0x1

1.16.1.2 TWI:TWI:TAR

Parent: TWI:TWI

Instances: 1

TABLE 1-590: FIELDS IN TAR

Field Name	Bit	Access	Description	Default
GC_OR_START_ENA	11	R/W	This bit indicates whether software performs a General Call or START BYTE command. '0': ignore bit 10 GC_OR_START and use TAR normally '1': perform special TWI command as specified in GC_OR_START bit	0x0
GC_OR_START	10	R/W	If TAR.GC_OR_START_ENA is set to 1, then this bit indicates whether a General Call or START byte command is to be performed. '0': General Call Address - after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting RAW_INTR_STAT.R_TX_ABRT. The TWI controller remains in General Call mode until the TAR.GC_OR_START_ENA field is cleared. '1': START BYTE	0x0
TAR	9:0	R/W	This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits. If the TAR and SAR are the same, loopback exists but the FIFOs are shared between master and slave, so full loopback is not feasible. Only one direction loopback mode is supported (simplex), not duplex. A master cannot transmit to itself; it can transmit to only a slave.	0x055

1.16.1.3 TWI:TWI:SAR

Parent: TWI:TWI

Instances: 1

TABLE 1-591: FIELDS IN SAR

Field Name	Bit	Access	Description	Default
SAR	9:0	R/W	The SAR holds the slave address when the TWI is operating as a slave. For 7-bit addressing, only SAR[6:0] is used. This register can be written only when the TWI interface is disabled (ENABLE = 0).	0x055

1.16.1.4 TWI:TWI:DATA_CMD

Parent: TWI:TWI

Instances: 1

TABLE 1-592: FIELDS IN DATA_CMD

Field Name	Bit	Access	Description	Default
CMD	8	R/W	This bit controls whether a read or a write is performed. This bit does not control the direction when the TWI acts as a slave. It controls only the direction when it acts as a master. When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a "don't care" because writes to this register are not required. In slave-transmitter mode, a "0" indicates that CPU data is to be transmitted and as DATA. When programming this bit, remember the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (RAW_INTR_STAT.R_TX_ABRT), unless TAR.GC_OR_START_ENA has been cleared. If a "1" is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRT interrupt occurs. NOTE: It is possible that while attempting a master TWI read transfer, a RD_REQ interrupt may have occurred simultaneously due to a remote TWI master addressing this controller. In this type of scenario, the TWI controller ignores the DATA_CMD write, generates a TX_ABRT interrupt, and waits to service the RD_REQ interrupt. '1' = Read '0' = Write	0x0
DATA	7:0	R/W	This register contains the data to be transmitted or received on the TWI bus. If you are writing to this register and want to perform a read, this field is ignored by the controller. However, when you read this register, these bits return the value of data received on the TWI interface.	0x00

1.16.1.5 TWI:TWI:SS_SCL_HCNT

Parent: TWI:TWI

Instances: 1

The clock for the TWI controller is the VCore system clock. This field must be set accordingly to the VCore system frequency; value = (4us / VCore clock period) - 8.

Example: a 178.6MHz clock correspond to a period of 5.6ns, for this frequency this field must not be set lower than (round up): 707 = (4us / 5.6ns) - 8.

TABLE 1-593: FIELDS IN SS_SCL_HCNT

Field Name	Bit	Access	Description	Default
SS_SCL_HCNT	15:0	R/W	This register sets the SCL clock divider for the high-period in standard speed. This value must result in a high period of no less than 4us.	0x033A

1.16.1.6 TWI:TWI:SS_SCL_LCNT

Parent: TWI:TWI

Instances: 1

The clock for the TWI controller is the VCore system clock. This field must be set accordingly to the VCore system frequency; value = (4.7us / VCore clock period) - 1.

Example: a 178.6MHz clock correspond to a period of 5.6ns, for this frequency this field must not be set lower than (round up): 839 = (4.7us / 5.6ns) - 1.

TABLE 1-594: FIELDS IN SS_SCL_LCNT

Field Name	Bit	Access	Description	Default
SS_SCL_LCNT	15:0	R/W	This register sets the SCL clock divider for the low-period in standard speed. This value must result in a value no less than 4.7us.	0x03D3

1.16.1.7 TWI:TWI:FS_SCL_HCNT

Parent: TWI:TWI

Instances: 1

The clock for the TWI controller is the VCore system clock. This field must be set accordingly to the VCore system frequency; value = (0.6us / VCore clock period) - 8.

Example: a 178.6MHz clock correspond to a period of 5.6ns, for this frequency this field must not be set lower than (round up): 100 = (0.6us / 5.6ns) - 8.

TABLE 1-595: FIELDS IN FS_SCL_HCNT

Field Name	Bit	Access	Description	Default
FS_SCL_HCNT	15:0	R/W	This register sets the SCL clock divider for the high-period in fast speed. This value must result in a value no less than 0.6us.	0x0075

1.16.1.8 TWI:TWI:FS_SCL_LCNT

Parent: TWI:TWI

Instances: 1

The clock for the TWI controller is the VCore system clock. This field must be set accordingly to the VCore system frequency; value = (1.3us / VCore clock period) - 1.

Example: a 178.6MHz clock correspond to a period of 5.6ns, for this frequency this field must not be set lower than (round up): 232 = (1.3us / 5.6ns) - 1.

TABLE 1-596: FIELDS IN FS_SCL_LCNT

Field Name	Bit	Access	Description	Default
FS_SCL_LCNT	15:0	R/W	This register sets the SCL clock divider for the low-period in fast speed. This value must result in a value no less than 1.3us.	0x010E

1.16.1.9 TWI:TWI:INTR_STAT

Parent: TWI:TWI

Instances: 1

Each field in this register has a corresponding mask field in the INTR_MASK register. These fields are cleared by reading the matching interrupt clear register. The unmasked raw versions of these fields are available in the RAW_INTR_STAT register.

See RAW_INTR_STAT for a description of these fields

TABLE 1-597: FIELDS IN INTR_STAT

Field Name	Bit	Access	Description	Default
GEN_CALL	11	R/O		0x0
START_DET	10	R/O		0x0
STOP_DET	9	R/O		0x0
ACTIVITY	8	R/O		0x0
RX_DONE	7	R/O		0x0
TX_ABRT	6	R/O		0x0
RD_REQ	5	R/O		0x0
TX_EMPTY	4	R/O		0x0
TX_OVER	3	R/O		0x0
RX_FULL	2	R/O		0x0
RX_OVER	1	R/O		0x0
RX_UNDER	0	R/O		0x0

1.16.1.10 TWI:TWI:INTR_MASK

Parent: TWI:TWI

Instances: 1

These fields mask the corresponding interrupt status fields (RAW_INTR_STAT). They are active high; a value of 0 prevents the corresponding field in RAW_INTR_STAT from generating an interrupt.

TABLE 1-598: FIELDS IN INTR_MASK

Field Name	Bit	Access	Description	Default
M_GEN_CALL	11	R/W		0x1
M_START_DET	10	R/W		0x0
M_STOP_DET	9	R/W		0x0
M_ACTIVITY	8	R/W		0x0
M_RX_DONE	7	R/W		0x1
M_TX_ABRT	6	R/W		0x1
M_RD_REQ	5	R/W		0x1

TABLE 1-598: FIELDS IN INTR_MASK (CONTINUED)

Field Name	Bit	Access	Description	Default
M_TX_EMPTY	4	R/W		0x1
M_TX_OVER	3	R/W		0x1
M_RX_FULL	2	R/W		0x1
M_RX_OVER	1	R/W		0x1
M_RX_UNDER	0	R/W		0x1

1.16.1.11 TWI:TWI:RAW_INTR_STAT

Parent: TWI:TWI

Instances: 1

Unlike the INTR_STAT register, these fields are not masked so they always show the true status of the TWI controller.

TABLE 1-599: FIELDS IN RAW_INTR_STAT

Field Name	Bit	Access	Description	Default
R_GEN_CALL	11	R/O	Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling TWI controller or when the CPU reads bit 0 of the CLR_GEN_CALL register. The TWI controller stores the received data in the Rx buffer.	0x0
R_START_DET	10	R/O	Indicates whether a START or RESTART condition has occurred on the TWI regardless of whether the TWI controller is operating in slave or master mode.	0x0
R_STOP_DET	9	R/O	Indicates whether a STOP condition has occurred on the TWI controller regardless of whether the TWI controller is operating in slave or master mode.	0x0
R_ACTIVITY	8	R/O	This bit captures TWI activity and stays set until it is cleared. There are four ways to clear it: * Disabling the TWI controller * Reading the CLR_ACTIVITY register * Reading the CLR_INTR register * VCore system reset Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the TWI controller module is idle, this bit remains set until cleared, indicating that there was activity on the bus.	0x0
R_RX_DONE	7	R/O	When the TWI controller is acting as a slave-transmitter, this bit is set to 1 if the master does not acknowledge a transmitted byte. This occurs on the last byte of the transmission, indicating that the transmission is done.	0x0

TABLE 1-599: FIELDS IN RAW_INTR_STAT (CONTINUED)

Field Name	Bit	Access	Description	Default
R_TX_ABRT	6	R/O	This bit is set to 1 when the TWI controller is acting as a master is unable to complete a command that the processor has sent. The conditions that set this field are: * No slave acknowledges the address byte. * The addressed slave receiver does not acknowledge a byte of data. * Attempting to send a master command when configured only to be a slave. * When CFG.RESTART_ENA is set to 0 (RESTART condition disabled), and the processor attempts to issue a TWI function that is impossible to perform without using RESTART conditions. * High-speed master code is acknowledged (this controller does not support high-speed). * START BYTE is acknowledged. * General Call address is not acknowledged. * When a read request interrupt occurs and the processor has previously placed data in the Tx buffer that has not been transmitted yet. This data could have been intended to service a multi-byte RD_REQ that ended up having fewer numbers of bytes requested. *The TWI controller loses arbitration of the bus between transfers and is then accessed as a slave-transmitter. * If a read command is issued after a General Call command has been issued. Disabling the TWI reverts it back to normal operation. * If the CPU attempts to issue read command before a RD_REQ is serviced. Anytime this bit is set, the contents of the transmit and receive buffers are flushed.	0x0
R_RD_REQ	5	R/O	This bit is set to 1 when the TWI controller acts as a slave and another TWI master is attempting to read data from this controller. The TWI controller holds the TWI bus in a wait state (SCL=0) until this interrupt is serviced, which means that the slave has been addressed by a remote master that is asking for data to be transferred. The processor must respond to this interrupt and then write the requested data to the DATA_CMD register. This bit is set to 0 just after the required data is written to the DATA_CMD register.	0x0

TABLE 1-599: FIELDS IN RAW_INTR_STAT (CONTINUED)

Field Name	Bit	Access	Description	Default
R_TX_EMPTY	4	R/O	This bit is set to 1 when the transmit buffer is at or below the threshold value set in the TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold. When ENABLE is 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer activity, then with ENABLE_STATUS.BUSY=0, this bit is set to 0.	0x0
R_TX_OVER	3	R/O	Set during transmit if the transmit buffer is filled to TX_BUFFER_DEPTH and the processor attempts to issue another TWI command by writing to the DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ENABLE_STATUS.BUSY goes to 0, this interrupt is cleared.	0x0
R_RX_FULL	2	R/O	Set when the receive buffer reaches or goes above the RX_TL threshold in the RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (ENABLE=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the ENABLE field is programmed with a 0, regardless of the activity that continues.	0x0
R_RX_OVER	1	R/O	Set if the receive buffer is completely filled to RX_BUFFER_DEPTH and an additional byte is received from an external TWI device. The TWI controller acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (ENABLE=0), this bit keeps its level until the master or slave state machines go into idle, and when ENABLE_STATUS.BUSY goes to 0, this interrupt is cleared.	0x0
R_RX_UNDER	0	R/O	Set if the processor attempts to read the receive buffer when it is empty by reading from the DATA_CMD register. If the module is disabled (ENABLE=0), this bit keeps its level until the master or slave state machines go into idle, and when ENABLE_STATUS.BUSY goes to 0, this interrupt is cleared.	0x0

1.16.1.12 TWI:TWI:RX_TL

Parent: TWI:TWI

Instances: 1

TABLE 1-600: FIELDS IN RX_TL

Field Name	Bit	Access	Description	Default
RX_TL	2:0	R/W	Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in RAW_INTR_STAT register). The valid range is 0-7. A value of 0 sets the threshold for 1 entry, and a value of 7 sets the threshold for 8 entries.	0x0

1.16.1.13 TWI:TWI:TX_TL

Parent: TWI:TWI

Instances: 1

TABLE 1-601: FIELDS IN TX_TL

Field Name	Bit	Access	Description	Default
TX_TL	2:0	R/W	Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in RAW_INTR_STAT register). The valid range is 0-7. A value of 0 sets the threshold for 0 entries, and a value of 7 sets the threshold for 7 entries.	0x0

1.16.1.14 TWI:TWI:CLR_INTR

Parent: TWI:TWI

Instances: 1

TABLE 1-602: FIELDS IN CLR_INTR

Field Name	Bit	Access	Description	Default
CLR_INTR	0	R/O	Read this register to clear the combined interrupt, all individual interrupts, and the TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the TX_ABRT_SOURCE register for an exception to clearing TX_ABRT_SOURCE.	0x0

1.16.1.15 TWI:TWI:CLR_RX_UNDER

Parent: TWI:TWI

Instances: 1

TABLE 1-603: FIELDS IN CLR_RX_UNDER

Field Name	Bit	Access	Description	Default
CLR_RX_UNDER	0	R/O	Read this register to clear the R_RX-_UNDER interrupt (bit 0) of the RAW_IN-TR_STAT register.	0x0

1.16.1.16 TWI:TWI:CLR_RX_OVER

Parent: TWI:TWI

Instances: 1

TABLE 1-604: FIELDS IN CLR_RX_OVER

Field Name	Bit	Access	Description	Default
CLR_RX_OVER	0	R/O	Read this register to clear the R_RX_OVER interrupt (bit 1) of the RAW_INTR_STAT register.	0x0

1.16.1.17 TWI:TWI:CLR_TX_OVER

Parent: TWI:TWI

Instances: 1

TABLE 1-605: FIELDS IN CLR_TX_OVER

Field Name	Bit	Access	Description	Default
CLR_TX_OVER	0	R/O	Read this register to clear the R_TX_OVER interrupt (bit 3) of the RAW_INTR_STAT register.	0x0

1.16.1.18 TWI:TWI:CLR_RD_REQ

Parent: TWI:TWI

Instances: 1

TABLE 1-606: FIELDS IN CLR_RD_REQ

Field Name	Bit	Access	Description	Default
CLR_RD_REQ	0	R/O	Read this register to clear the R_RD_REQ interrupt (bit 5) of the RAW_INTR_STAT register.	0x0

1.16.1.19 TWI:TWI:CLR_TX_ABRT

Parent: TWI:TWI

Instances: 1

TABLE 1-607: FIELDS IN CLR_TX_ABRT

Field Name	Bit	Access	Description	Default
CLR_TX_ABRT	0	R/O	Read this register to clear the R_TX_ABRT interrupt (bit 6) of the RAW_INTR_STAT register, and the TX_ABRT_SOURCE register. Refer to Bit 9 of the TX_ABRT_SOURCE register for an exception to clearing TX_ABRT_SOURCE.	0x0

1.16.1.20 TWI:TWI:CLR_RX_DONE

Parent: TWI:TWI

Instances: 1

TABLE 1-608: FIELDS IN CLR_RX_DONE

Field Name	Bit	Access	Description	Default
CLR_RX_DONE	0	R/O	Read this register to clear the R_RX_DONE interrupt (bit 7) of the RAW_INTR_STAT register.	0x0

1.16.1.21 TWI:TWI:CLR_ACTIVITY

Parent: TWI:TWI

Instances: 1

TABLE 1-609: FIELDS IN CLR_ACTIVITY

Field Name	Bit	Access	Description	Default
CLR_ACTIVITY	0	R/O	Reading this register clears the ACTIVITY interrupt if the TWI controller is not active anymore. If the TWI controller is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the R_ACTIVITY interrupt (bit 8) of the RAW_INTR_STAT register.	0x0

1.16.1.22 TWI:TWI:CLR_STOP_DET

Parent: TWI:TWI

Instances: 1

TABLE 1-610: FIELDS IN CLR_STOP_DET

Field Name	Bit	Access	Description	Default
CLR_STOP_DET	0	R/O	Read this register to clear the R_STOP_DET interrupt (bit 9) of the RAW_INTR_STAT register.	0x0

1.16.1.23 TWI:TWI:CLR_START_DET

Parent: TWI:TWI

Instances: 1

TABLE 1-611: FIELDS IN CLR_START_DET

Field Name	Bit	Access	Description	Default
CLR_START_DET	0	R/O	Read this register to clear the R_START_DET interrupt (bit 10) of the RAW_INTR_STAT register.	0x0

1.16.1.24 TWI:TWI:CLR_GEN_CALL

Parent: TWI:TWI

Instances: 1

TABLE 1-612: FIELDS IN CLR_GEN_CALL

Field Name	Bit	Access	Description	Default
CLR_GEN_CALL	0	R/O	Read this register to clear the R_GEN_CALL interrupt (bit 11) of RAW_INTR_STAT register.	0x0

1.16.1.25 TWI:TWI:CTRL

Parent: TWI:TWI

Instances: 1

TABLE 1-613: FIELDS IN CTRL

Field Name	Bit	Access	Description	Default
ENABLE	0	R/W	Controls whether the TWI controller is enabled. Software can disable the controller while it is active. However, it is important that care be taken to ensure that the controller is disabled properly. When TWI controller is disabled, the following occurs: * The TX FIFO and RX FIFO get flushed. * The interrupt bits in the RAW_INTR_STAT register are cleared. * Status bits in the INTR_STAT register are still active until the TWI controller goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the controller stops the current transfer at the end of the current byte and does not acknowledge the transfer. '0': Disables TWI controller '1': Enables TWI controller	0x0

1.16.1.26 TWI:TWI:STAT

Parent: TWI:TWI

Instances: 1

TABLE 1-614: FIELDS IN STAT

Field Name	Bit	Access	Description	Default
SLV_ACTIVITY	6	R/O	Slave FSM Activity Status. When the Slave Finite State Machine (FSM) is not in the IDLE state, this bit is set. '0': Slave FSM is in IDLE state so the Slave part of the controller is not Active '1': Slave FSM is not in IDLE state so the Slave part of the controller is Active	0x0

TABLE 1-614: FIELDS IN STAT (CONTINUED)

Field Name	Bit	Access	Description	Default
MST_ACTIVITY	5	R/O	Master FSM Activity Status. When the Master Finite State Machine (FSM) is not in the IDLE state, this bit is set. '0': Master FSM is in IDLE state so the Master part of the controller is not Active '1': Master FSM is not in IDLE state so the Master part of the controller is Active	0x0
RFF	4	R/O	Receive FIFO Completely Full. When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. '0': Receive FIFO is not full '1': Receive FIFO is full	0x0
RFNE	3	R/O	Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty. This bit can be polled by software to completely empty the receive FIFO. '0': Receive FIFO is empty '1': Receive FIFO is not empty	0x0
TFE	2	R/O	Transmit FIFO Completely Empty. When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. '0': Transmit FIFO is not empty '1': Transmit FIFO is empty	0x1
TFNF	1	R/O	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. '0': Transmit FIFO is full '1': Transmit FIFO is not full	0x1
BUS_ACTIVITY	0	R/O	TWI Activity Status.	0x0

1.16.1.27 TWI:TWI:TXFLR

Parent: TWI:TWI

Instances: 1

TABLE 1-615: FIELDS IN TXFLR

Field Name	Bit	Access	Description	Default
TXFLR	2:0	R/O	Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO.	0x0

1.16.1.28 TWI:TWI:RXFLR

Parent: TWI:TWI

Instances: 1

TABLE 1-616: FIELDS IN RXFLR

Field Name	Bit	Access	Description	Default
RXFLR	2:0	R/O	Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.	0x0

1.16.1.29 TWI:TWI:TX_ABRT_SOURCE

Parent: TWI:TWI

Instances: 1

TABLE 1-617: FIELDS IN TX_ABRT_SOURCE

Field Name	Bit	Access	Description	Default
ABRT_SLVRD_INTX	15	R/W	When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 to DATA_CMD.CMD.	0x0
ABRT_SLV_ARBLOST	14	R/W	Slave lost the bus while transmitting data to a remote master. TX_ABRT_SOURCE[12] is set at the same time. Note: Even though the slave never "owns" the bus, something could go wrong on the bus. This is a fail safe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then the TWI controller no longer own the bus.	0x0
ABRT_SLVFLUSH_TXFIFO	13	R/W	Slave has received a read command and some data exists in the TX FIFO so the slave issues a TX_ABRT interrupt to flush old data in TX FIFO.	0x0
ARB_LOST	12	R/W	Master has lost arbitration, or if TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Note: the TWI controller can be both master and slave at the same time.	0x0
ABRT_MASTER_DIS	11	R/W	User tries to initiate a Master operation with the Master mode disabled.	0x0
ABRT_10B_RD_NORSTRT	10	R/W	The restart is disabled (RESTART_ENA bit (CFG[5]) = 0) and the master sends a read command in 10-bit addressing mode.	0x0

TABLE 1-617: FIELDS IN TX_ABRT_SOURCE (CONTINUED)

Field Name	Bit	Access	Description	Default
ABRT_SBYTE_NORSTRT	9	R/W	To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (CFG[5]=1), the SPECIAL bit must be cleared (TAR[11]), or the GC_OR_START bit must be cleared (TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted. '1': The restart is disabled (RESTART_ENA bit (CFG[5]) = 0) and the user is trying to send a START Byte.	0x0
ABRT_SBYTE_ACKDET	7	R/W	Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).	0x0
ABRT_GCALL_READ	5	R/W	TWI controller in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (DATA_CMD[9] is set to 1).	0x0
ABRT_GCALL_NOACK	4	R/W	TWI controller in master mode sent a General Call and no slave on the bus acknowledged the General Call.	0x0
ABRT_TXDATA_NOACK	3	R/W	This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).	0x0
ABRT_10ADDR2_NOACK	2	R/W	Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.	0x0
ABRT_10ADDR1_NOACK	1	R/W	Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.	0x0
ABRT_7B_ADDR_NOACK	0	R/W	Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.	0x0

1.16.1.30 TWI:TWI:SDA_SETUP

Parent: TWI:TWI

Instances: 1

This field must be set accordingly to the VCore system frequency; value = 100ns / VCore clock period.

Example: a 178.6MHz clock correspond to a period of 5.6ns, for this frequency and fast TWI speed this field must not be set lower than (round up): 18 = 100ns / 5.6ns. For normal TWI speed this field must not be set lower than (round up): 45 = 250ns / 5.6ns.

TABLE 1-618: FIELDS IN SDA_SETUP

Field Name	Bit	Access	Description	Default
SDA_SETUP	7:0	R/W	This register controls the amount of time delay (in terms of number of VCore clock periods) introduced in the rising edge of SCL, relative to SDA changing, when the TWI controller services a read request in a slave-receiver operation. The minimum for fast mode is 100ns, for normal mode the minimum is 250ns.	0x64

1.16.1.31 TWI:TWI:ACK_GEN_CALL

Parent: TWI:TWI

Instances: 1

TABLE 1-619: FIELDS IN ACK_GEN_CALL

Field Name	Bit	Access	Description	Default
ACK_GEN_CALL	0	R/W	ACK General Call. When set to 1, the TWI controller responds with a ACK when it receives a General Call. Otherwise, the controller responds with a NACK.	0x1

1.16.1.32 TWI:TWI:ENABLE_STATUS

Parent: TWI:TWI

Instances: 1

TABLE 1-620: FIELDS IN ENABLE_STATUS

Field Name	Bit	Access	Description	Default
SLV_FIFO_FILLED_AND_-FLUSHED	2	R/O	Slave FIFO Filled and Flushed. This bit indicates if a Slave-Receiver operation has been aborted with at least 1 data byte received from a TWI transfer due to the setting of ENABLE from 1 to 0. When read as 1, the TWI controller is deemed to have been actively engaged in an aborted TWI transfer (with matching address) and the data phase of the TWI transfer has been entered, even though the data byte has been responded with a NACK. When read as 0, the TWI controller is deemed to have been disabled when the TWI bus is idle.	0x0

TABLE 1-620: FIELDS IN ENABLE_STATUS (CONTINUED)

Field Name	Bit	Access	Description	Default
SLV_RX_ABORTED	1	R/O	Slave-Receiver Operation Aborted. This bit indicates if a Slave-Receiver operation has been aborted due to the setting of the ENABLE register from 1 to 0. When read as 1, the TWI controller is deemed to have forced a NACK during any part of a TWI transfer, irrespective of whether the TWI address matches the slave address set in the TWI controller (SAR register). When read as 0, the TWI controller is deemed to have been disabled when the TWI bus is idle.	0x0
BUSY	0	R/O	When read as 1, the TWI controller is deemed to be actively involved in an TWI transfer, irrespective of whether being in an address or data phase for all master or slave modes. When read as 0, the TWI controller is deemed completely inactive.	0x0

1.17 UART

TABLE 1-621: REGISTER GROUPS IN UART

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
UART	0x00000000	1	UART	Page 270

1.17.1 UART:UART

Parent: UART

Instances: 1

TABLE 1-622: REGISTERS IN UART

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
RBR_THR	0x00000000	1	Receive buffer / transmit holding / divisor (low)	Page 271
IER	0x00000004	1	Interrupt enable / divisor (high)	Page 271
IIR_FCR	0x00000008	1	Interrupt identification / FIFO control register	Page 272
LCR	0x0000000C	1	Line control	Page 273
MCR	0x00000010	1	Modem control	Page 274
LSR	0x00000014	1	Line status	Page 275
MSR	0x00000018	1	Modem status	Page 277
SCR	0x0000001C	1	Scratchpad	Page 278
USR	0x0000007C	1	UART status	Page 278

1.17.1.1 UART:UART:RBR_THR

Parent: UART:UART

Instances: 1

When the LCR.DLAB is set, this register is the lower 8 bits of the 16-bit Divisor register that contains the baud rate divisor for the UART.

The output baud rate is equal to the VCore system clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (VCore clock freq) / (16 * divisor). Note that with the Divisor set to zero, the baud clock is disabled and no serial communications occur. In addition, once this register is set, wait at least 0.1us before transmitting or receiving data.

TABLE 1-623: FIELDS IN RBR_THR

Field Name	Bit	Access	Description	Default
RBR_THR	7:0	R/W	Use this register to access the Rx and Tx FIFOs. When reading: The data in this register is valid only if LSR.DR is set. If FIFOs are disabled (IIR_FCR.FIFOE), the data in this register must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. When FIFOs are enabled (IIR_FCR.FIFOE), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data is lost and an overrun error occurs. When writing: Data should only be written to this register when the LSR.THRE indicates that there is room in the FIFO. If FIFOs are disabled (IIR_FCR.FIFOE), writes to this register while LSR.THRE is zero, causes the register to be overwritten. When FIFOs are enabled (IIR_FCR.FIFOE) and LSR.THRE is set, 16 characters may be written to this register before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.	0x00

1.17.1.2 UART:UART:IER

Parent: UART:UART

Instances: 1

When the LCR.DLAB is set, this register is the upper 8 bits of the 16-bit Divisor register that contains the baud rate divisor for the UART. For more information and a description of how to calculate the baud rate, see RBR_THR.

TABLE 1-624: FIELDS IN IER

Field Name	Bit	Access	Description	Default
PTIME	7	R/W	Programmable THRE interrupt mode enable. This is used to enable or disable the generation of THRE interrupt. 0: Disabled 1: Enabled	0x0

TABLE 1-624: FIELDS IN IER (CONTINUED)

Field Name	Bit	Access	Description	Default
EDSSI	3	R/W	Enable modem status interrupt. This is used to enable or disable the generation of Modem Status interrupt. This is the fourth highest priority interrupt. 0: Disabled 1: Enabled	0x0
ELSI	2	R/W	Enable receiver line status interrupt. This is used to enable or disable the generation of Receiver Line Status interrupt. This is the highest priority interrupt. 0: Disabled 1: Enabled	0x0
ETBEI	1	R/W	Enable transmit holding register empty interrupt. This is used to enable or disable the generation of Transmitter Holding Register Empty interrupt. This is the third highest priority interrupt. 0: Disabled 1: Enabled	0x0
ERBFI	0	R/W	Enable received data available interrupt. This is used to enable or disable the generation of Received Data Available interrupt and the Character Timeout interrupt (if FIFOs are enabled). These are the second highest priority interrupts. 0: Disabled 1: Enabled	0x0

1.17.1.3 UART:UART:IIR_FCR

Parent: UART:UART

Instances: 1

This register has special meaning when reading, here the lowest 4 bits indicate interrupting sources. The encoding is as follows:

0110; type: Receiver line status, priority: Highest. Overrun/parity/ framing errors or break interrupt. Cleared by reading LSR.

0100; type: Received data available, priority: Second. RCVR FIFO trigger level reached. Cleared when FIFO drops below the trigger level.

1100; type: Character timeout indication, priority: Second. No characters in or out of the RCVR FIFO during the last four character times and there is at least 1 character in it during this time. Cleared by reading the receiver buffer register.

0010; type: Transmit holding register empty, priority: Third. Transmitter holding register empty (Prog. THRE Mode disabled) or XMIT FIFO at or below threshold (Prog. THRE Mode enabled). Cleared by reading the IIR register (if source of interrupt); or, writing into THR (THRE Mode disabled) or XMIT FIFO above threshold (THRE Mode enabled).

0000; type: Modem status, priority: Fourth. Clear to send. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt. Cleared by reading the Modem status register.

0111; type: Busy detect indication, priority: Fifth. Master has tried to write to the Line Control register while the UART is busy (USR[0] is set to one). Cleared by reading the UART status register.

0001: No interrupting sources.

TABLE 1-625: FIELDS IN IIR_FCR

Field Name	Bit	Access	Description	Default
FIFOSE_RT	7:6	R/W	When reading this field, the current status of the FIFO is returned; 00 for disabled or 11 for enabled. Writing this field selects the trigger level in the receive FIFO at which the Received Data Available interrupt is generated (see encoding.) In auto flow control mode, it is used to determine when to generate back-pressure using the RTS signal. 00: 1 character in the Rx FIFO 01: Rx FIFO 1/4 full 10: Rx FIFO 1/2 full 11: Rx FIFO 2 less than full	0x1
TET	5:4	R/W	Tx empty trigger. When the THRE mode is enabled (IER.PTIME), this field selects the empty threshold level at which the THRE Interrupts are generated. 00: Tx FIFO empty 01: 2 characters in the Tx FIFO 10: Tx FIFO 1/4 full 11: Tx FIFO 1/2 full	0x0
XFIFOR	2	R/W	This description is valid for writes only. Reading this field has special meaning; for more information, see the general register description. Tx FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is self-clearing. It is not necessary to clear this bit.	0x0
RFIFOR	1	R/W	This description is valid for writes only. Reading this field has special meaning; for more information, see the general register description. Rx FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is self-clearing. It is not necessary to clear this bit.	0x0
FIFOE	0	R/W	This description is valid for writes only. Reading this field has special meaning; for more information, see the general register description. FIFO Enable. This enables or disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed, both the XMIT and RCVR controller portion of FIFOs are reset.	0x0

1.17.1.4 UART:UART:LCR

Parent: UART:UART

Instances: 1

Writes can be made to this register, with the exception of the BC field, only when UART is not busy, that is, when USR.BUSY is zero. This register can always be read.

TABLE 1-626: FIELDS IN LCR

Field Name	Bit	Access	Description	Default
DLAB	7	R/W	Divisor latch access bit. This bit is used to enable reading and writing of the Divisor registers (RBR_THR and IER) to set the baud rate of the UART. To access other registers, this bit must be cleared after initial baud rate setup.	0x0
BC	6	R/W	Break control bit.This bit is used to cause a break condition to be transmitted to the receiving device. If set to one, the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the serial output is forced low until the Break bit is cleared.	0x0
EPS	4	R/W	Even parity select. This bit is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.	0x0
PEN	3	R/W	Parity enable. This bit is used to enable or disable parity generation and detection in both transmitted and received serial characters. 0: Parity disabled 1: Parity enabled	0x0
STOP	2	R/W	Number of stop bits. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR.DLS), one and a half stop bits are transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0: 1 stop bit 1: 1.5 stop bits when LCR.DLS is zero, otherwise, 2 stop bits	0x0
DLS	1:0	R/W	Data length select. This is used to select the number of data bits per character that the peripheral transmits and receives. The following settings specify the number of bits that may be selected. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	0x0

1.17.1.5 UART:UART:MCR

Parent: UART:UART

Instances: 1

TABLE 1-627: FIELDS IN MCR

Field Name	Bit	Access	Description	Default
AFCE	5	R/W	Auto flow control enable. This mode requires that FIFOs are enabled and that MCR.RTS is set. 0: Auto flow control mode disabled 1: Auto flow control mode enabled	0x0
LB	4	R/W	Loopback Bit. This is used to put the UART into a diagnostic mode for test purposes. The transmit line is held high, while serial transmit data is looped back to the receive line internally. In this mode, all the interrupts are fully functional. In addition, in loopback mode, the modem control input CTS is disconnected, and the modem control output RTS is looped back to the input internally.	0x0
RTS	1	R/W	Request to send. This is used to directly control the Request to Send (RTS) output. The RTS output is used to inform the partner that the UART is ready to exchange data. The RTS is still controlled from this field when Auto RTS Flow Control is enabled (MCR.AFCE), but the output can be forced high by the flow control mechanism. If this field is cleared, the UART permanently indicates backpressure to the partner. 0: RTS is set high 1: RTS is set low	0x0

1.17.1.6 UART:UART:LSR

Parent: UART:UART

Instances: 1

TABLE 1-628: FIELDS IN LSR

Field Name	Bit	Access	Description	Default
RFE	7	R/W	Receiver FIFO error bit. This bit is only valid when FIFOs are enabled. This is used to indicate whether there is at least one parity error, framing error, or break indication in the FIFO. This bit is cleared when the LSR is read, the character with the error is at the top of the receiver FIFO, and there are no subsequent errors in the FIFO. 0: No error in Rx FIFO 1: Error in Rx FIFO	0x0
TEMT	6	R/W	Transmitter empty bit. If FIFOs are enabled, this bit is set whenever the Transmitter Shift Register and the FIFO are both empty.	0x1

TABLE 1-628: FIELDS IN LSR (CONTINUED)

Field Name	Bit	Access	Description	Default
THRE	5	R/W	If FIFO (IIR_FCR.FIFOE) and THRE mode are enabled (IER.PTIME), this bit indicates that the Tx FIFO is full. Otherwise, this bit indicates that the Tx FIFO is empty.	0x1
BI	4	R/W	Break interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. It is set whenever the serial input is held in a logic 0 state for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all-zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.	0x0
FE	3	R/W	Framing error bit. This is used to indicate the a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. A framing error is associated with a received character. Therefore, in FIFO mode, an error is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues to receive the other bit, that is, data and/or parity, and then stops. Note that this field is set if a break interrupt has occurred, as indicated by Break Interrupt (LSR.BI). This field is cleared on read. 0: No framing error 1: Framing error	0x0
PE	2	R/W	Parity error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable bit (LCR.PEN) is set. A parity error is associated with a received character. Therefore, in FIFO mode, an error is revealed when the character with the parity error arrives at the top of the FIFO. Note that this field is set if a break interrupt has occurred, as indicated by Break Interrupt (LSR.BI). This field is cleared on read. 0: No parity error 1: Parity error	0x0

TABLE 1-628: FIELDS IN LSR (CONTINUED)

Field Name	Bit	Access	Description	Default
OE	1	R/W	Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In non-FIFO mode, the OE bit is set when a new character arrives before the previous character was read. When this happens, the data in the RBR is overwritten. In FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. This field is cleared on read. 0: No overrun error 1: Overrun error	0x0
DR	0	R/W	Data ready. This is used to indicate that the receiver contains at least one character in the receiver FIFO. This bit is cleared when the RX FIFO is empty. 0: No data ready 1: Data ready	0x0

1.17.1.7 UART:UART:MSR

Parent: UART:UART

Instances: 1

TABLE 1-629: FIELDS IN MSR

Field Name	Bit	Access	Description	Default
CTS	4	R/O	Clear to send. This field indicates the current state of the modem control line, CTS. When the Clear to Send input (CTS) is asserted, it is an indication that the partner is ready to exchange data with the UART. 0: CTS input is deasserted (logic 0) 1: CTS input is asserted (logic 1)	0x0
DCTS	0	R/O	Delta clear to send. This is used to indicate that the modem control line, CTS, has changed since the last time the MSR was read. Reading the MSR clears the DCTS bit. Note: If the DCTS bit is not set, the CTS signal is asserted, and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed, if the CTS signal remains asserted. A read of the MSR after reset can be performed to prevent unwanted interrupts. 0: No change on CTS since the last read of the MSR 1: Change on CTS since the last read of the MSR	0x0

1.17.1.8 UART:UART:SCR

Parent: UART:UART

Instances: 1

TABLE 1-630: FIELDS IN SCR

Field Name	Bit	Access	Description	Default
SCR	7:0	R/W	This register is for programmers to use as a temporary storage space. It has no functional purpose for the UART.	0x00

1.17.1.9 UART:UART:USR

Parent: UART:UART

Instances: 1

TABLE 1-631: FIELDS IN USR

Field Name	Bit	Access	Description	Default
BUSY	0	R/O	UART busy. 0: UART is idle or inactive 1: UART is busy (actively transferring data)	0x0

1.18 PHY

TABLE 1-632: REGISTER GROUPS IN PHY

Register Group Name	Offset within Target	Instances and Address Spacing	Description	Details
PHY_STD	0x00000000	1	IEEE Standard and Main Registers	Page 278
PHY_EXT1	0x00000080	1	Extended Page 1 Registers	Page 299
PHY_EXT2	0x000000FC	1	Extended Page 2 Registers	Page 305
PHY_GP	0x00000168	1	General Purpose Registers	Page 309
PHY_EEE	0x000001E0	1	Clause 45 Registers to Support Energy Efficient	Page 313

1.18.1 PHY:PHY_STD

Parent: PHY

Instances: 1

The following section lists the standard register set for the PHY.

TABLE 1-633: REGISTERS IN PHY_STD

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_CTRL	0x00000000	1	Control (Address 0)	Page 280
PHY_STAT	0x00000004	1	Status (Address 1)	Page 281

TABLE 1-633: REGISTERS IN PHY_STD (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_IDF1	0x00000008	1	PHY Identifier Number 1 (Address 2)	Page 281
PHY_IDF2	0x0000000C	1	PHY Identifier Number 2 (Address 3)	Page 281
PHY_AUTONEG_ADVERTIS-MENT	0x00000010	1	Auto-Negotiation Advertise-ment (Address 4)	Page 282
PHY_AUTONEG_LP_ABILITY	0x00000014	1	Auto-Negotiation Link Partner Base Page Ability (Address 5)	Page 282
PHY_AUTONEG_EXP	0x00000018	1	Auto-Negotiation Expansion (Address 6)	Page 283
PHY_AUTONEG_NEXTPAGE_TX	0x0000001C	1	Auto-Negotiation Next-Page Transmit (Address 7)	Page 283
PHY_AUTONEG_LP_NEXT-PAGE_RX	0x00000020	1	Auto-Negotiation Next-Page Receive (Address 8)	Page 284
PHY_CTRL_1000BT	0x00000024	1	1000BASE-T Control (Address 9)	Page 284
PHY_STAT_1000BT	0x00000028	1	1000BASE-T Status (Address 10)	Page 285
MMD_ACCESS_CFG	0x00000034	1	MMD Access Control Register (Address 13)	Page 285
MMD_ADDR_DATA	0x00000038	1	MMD Address or Data Regis-ter (Address 14)	Page 285
PHY_STAT_1000BT_EXT1	0x0000003C	1	1000BASE-T Status Exten-sion Number 1 (Address 15)	Page 286
PHY_STAT_100BTX	0x00000040	1	100BASE-TX Status (Address 16)	Page 286
PHY_STAT_1000BT_EXT2	0x00000044	1	1000BASE-T Status Exten-sion Number 2 (Address 17)	Page 287
PHY_BYPASS_CTRL	0x00000048	1	Bypass Control (Address 18)	Page 287
PHY_ERROR_CNT1	0x0000004C	1	Error Counter Number 1 (Address 19)	Page 288
PHY_ERROR_CNT2	0x00000050	1	Error Counter Number 2 (Address 20)	Page 289
PHY_ERROR_CNT3	0x00000054	1	Error Counter Number 3 (Address 21)	Page 289
PHY_CTRL_STAT_EXT	0x00000058	1	Extended Control and Status (Address 22)	Page 289
PHY_CTRL_EXT1	0x0000005C	1	Extended Control Number 1 (Address 23)	Page 290
PHY_CTRL_EXT2	0x00000060	1	Extended Control Number 2 (Address 24)	Page 291
PHY_INT_MASK	0x00000064	1	Interrupt Mask (Address 25)	Page 292
PHY_INT_STAT	0x00000068	1	Interrupt Status (Address 26)	Page 293
PHY_AUX_CTRL_STAT	0x00000070	1	Auxiliary Control and Status (Address 28)	Page 295
PHY_LED_MODE_SEL	0x00000074	1	LED Mode Select (Address 29)	Page 296

TABLE 1-633: REGISTERS IN PHY_STD (CONTINUED)

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_LED_BEHAVIOR_CTRL	0x00000078	1	LED Behavior Control (Address 30)	Page 297
PHY_MEMORY_PAGE_ACCESS	0x0000007C	1	Memory Page Access (Address 31)	Page 298

1.18.1.1 PHY:PHY_STD:PHY_CTRL

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-634: FIELDS IN PHY_CTRL

Field Name	Bit	Access	Description	Default
SOFTWARE_RESET_ENA	15	R/W	Initiate software reset. This field is cleared as part of this operation. After enabling this field, you must wait at least 4 us before PHY registers can be accessed again.	0x0
LOOPBACK_ENA	14	R/W	Enable loopback mode. The loopback mechanism works at the current speed. If the link is down (see PHY_STAT.LINK_STATUS), SPEED_SEL_LSB_CFG and SPEED_SEL_MSB_CFG determine the operating speed of the loopback.	0x0
SPEED_SEL_LSB_CFG	13	R/W	Least significant bit of the speed selection, along with SPEED_SEL_MSB_CFG, this field determines the speed when auto-negotiation is disabled (See AUTONEG_ENA). 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved	0x0
AUTONEG_ENA	12	R/W	Enable auto-negotiation. When cleared, the speed and duplex-mode are determined by SPEED_SEL_LSB_CFG, SPEED_SEL_MSB_CFG, and DUPLEX_MODE_CFG.	0x1
POWER_DOWN_ENA	11	R/W	Enable power-down mode. This disables PHY operation until this bit is cleared or the PHY is reset.	0x0
ISOLATE_ENA	10	R/W	Isolate the PHY from the integrated MAC.	0x0
AUTONEG_RESTART_ENA	9	R/W	Restart an auto-negotiation cycle; the PHY clears this field when auto-negotiation is restarted.	0x0
DUPLEX_MODE_CFG	8	R/W	Configure duplex mode when auto-negotiation is disabled (see AUTONEG_ENA). 0: Half-duplex 1: Full-duplex	0x0
COLLISION_TEST_ENA	7	R/W	Enable collision indication test-mode, when enabled the PHY indicate collision when the MAC transmits data to the PHY.	0x0
SPEED_SEL_MSB_CFG	6	R/W	See SPEED_SEL_LSB_CFG.	0x1

1.18.1.2 PHY:PHY_STD:PHY_STAT

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-635: FIELDS IN PHY_STAT

Field Name	Bit	Access	Description	Default
MODE_100BT4	15	R/O	The PHY is not 100BASE-T4 capable.	0x0
MODE_100BX_FDX	14	R/O	The PHY is 100BASE-X FDX capable.	0x1
MODE_100BX_HDX	13	R/O	The PHY is 100BASE-X HDX capable.	0x1
MODE_10BT_FDX	12	R/O	The PHY is 10BASE-T FDX capable.	0x1
MODE_10BT_HDX	11	R/O	The PHY is 10BASE-T HDX capable.	0x1
MODE_100BT2_FDX	10	R/O	The PHY is not 100BASE-T2 FDX capable.	0x0
MODE_100BT2_HDX	9	R/O	The PHY is not 100BASE-T2 HDX capable.	0x0
EXT_STATUS	8	R/O	Extended status information are available; see the PHY_STAT_EXT register.	0x1
PREAMBLE_SUPPRESS	6	R/O	The PHY accepts management frames with preamble suppressed.	0x1
AUTONEG_COMPLETE	5	R/O	This field is set when auto-negotiation is completed and cleared during active auto-negotiation cycles.	0x0
REMOTE_FAULT	4	R/O	This field is set when the PHY detects a remote fault condition and cleared on register read.	0x0
AUTONEG_ABILITY	3	R/O	The PHY is capable of auto-negotiation.	0x1
LINK_STAT	2	R/O	This field is cleared when the link is down. It is set when the link is up and a previous link-down indication was read from the register.	0x0
JABBER_DETECT	1	R/O	This field is set when the PHY detects a jabber condition and cleared on register read.	0x0
EXT_CAPABILITY	0	R/O	The PHY provides an extended set of capabilities.	0x1

1.18.1.3 PHY:PHY_STD:PHY_IDF1

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-636: FIELDS IN PHY_IDF1

Field Name	Bit	Access	Description	Default
OUI_MS	15:0	R/O	Vitesse's organizationally unique identifier bits 3 through 18.	0x0007

1.18.1.4 PHY:PHY_STD:PHY_IDF2

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-637: FIELDS IN PHY_IDF2

Field Name	Bit	Access	Description	Default
OUI_LS	15:10	R/O	Vitesse's organizationally unique identifier bits 19 through 24.	0x01
MODEL_NUMBER	9:4	R/O	The device model number.	0x2D
REVISION_NUMBER	3:0	R/O	The device revision number.	0x0

1.18.1.5 PHY:PHY_STD:PHY_AUTONEG_ADVERTISMENT

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-638: FIELDS IN PHY_AUTONEG_ADVERTISMENT

Field Name	Bit	Access	Description	Default
NEXT_PAGE_ENA	15	R/W	Advertises desire to engage in next-page exchange. When this field is set, next-page control is returned to the user for additional next-pages following the 1000BASE-T next-page exchange.	0x0
REMOTE_FAULT_CFG	13	R/W	Transmit Remote Fault.	0x0
ASYM_PAUSE_CFG	11	R/W	Advertise asymmetric pause capability.	0x0
SYM_PAUSE_CFG	10	R/W	Advertise symmetric pause capability.	0x0
ADV_100BT4_CFG	9	R/W	Advertise 100BASE-T4 capability.	0x0
ADV_100BX_FDX_CFG	8	R/W	Advertise 100BASE-X FDX capability.	0x1
ADV_100BX_HDX_CFG	7	R/W	Advertise 100BASE-X HDX capability.	0x1
ADV_10BT_FDX_CFG	6	R/W	Advertise 10BASE-T FDX capability.	0x1
ADV_10BT_HDX_CFG	5	R/W	Advertise 10BASE-T HDX capability.	0x1
SELECTOR_FIELD_CFG	4:0	R/W	Select types of message send by auto-negotiation.	0x01

1.18.1.6 PHY:PHY_STD:PHY_AUTONEG_LP_ABILITY

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-639: FIELDS IN PHY_AUTONEG_LP_ABILITY

Field Name	Bit	Access	Description	Default
LP_NEXT_PAGE	15	R/O	Link partner advertises desire to engage in next-page exchange.	0x0
LP_ACKNOWLEDGE	14	R/O	Link partner advertises that link code word was successfully received.	0x0
LP_REMOTE_FAULT	13	R/O	Link partner advertises remote fault.	0x0
LP_ASYM_PAUSE	11	R/O	Link partner advertises asymmetric pause capability.	0x0
LP_SYM_PAUSE	10	R/O	Link partner advertises symmetric pause capability.	0x0
LP_100BT4	9	R/O	Link partner advertises 100BASE-T4 capability.	0x0

TABLE 1-639: FIELDS IN PHY_AUTONEG_LP_ABILITY (CONTINUED)

Field Name	Bit	Access	Description	Default
LP_100BX_FDX	8	R/O	Link partner advertises 100BASE-X FDX capability.	0x0
LP_100BX_HDX	7	R/O	Link partner advertises 100BASE-X HDX capability.	0x0
LP_10BT_FDX	6	R/O	Link partner advertises 10BASE-T FDX capability.	0x0
LP_10BT_HDX	5	R/O	Link partner advertises 10BASE-T HDX capability.	0x0
LP_SELECTOR_FIELD	4:0	R/O	Link partner advertises select type of message send by auto-negotiation.	0x00

1.18.1.7 PHY:PHY_STD:PHY_AUTONEG_EXP

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-640: FIELDS IN PHY_AUTONEG_EXP

Field Name	Bit	Access	Description	Default
PARALLEL_DET_FAULT	4	R/O	This field is set when the PHY detects a Receive Link Integrity Test Failure condition and cleared on register read.	0x0
LP_NEXT_PAGE_ABLE	3	R/O	Set if link partner is next-page capable.	0x0
NEXT_PAGE_ABLE	2	R/O	The PHY is next-page capable.	0x1
NEXT_PAGE_RECEIVED	1	R/O	This field is set when the PHY receives a valid next-page and cleared on register read.	0x0
LP_AUTONEG_ABLE	0	R/O	Set if link partner is auto-negotiation capable.	0x0

1.18.1.8 PHY:PHY_STD:PHY_AUTONEG_NEXTPAGE_TX

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-641: FIELDS IN PHY_AUTONEG_NEXTPAGE_TX

Field Name	Bit	Access	Description	Default
NEXT_PAGE_CFG	15	R/W	Set to indicate that more pages will follow; clear if current page is the last.	0x0
MESSAGE_PAGE_CFG	13	R/W	Set to indicate that this is a message page; clear if the current page consists of unformatted code.	0x1
ACKNOWLEDGE2_CFG	12	R/W	Set to indicate ability to comply with the request of the last received page.	0x0
TOGGLE	11	R/O	Alternates between 0 and 1 for each transmitted page.	0x0
MESSAGE_FIELD_CFG	10:0	R/W	Contains page information - either message or unformatted code. MESSAGE_PAGE_CFG must indicate if this page contains either a message or unformatted code.	0x001

1.18.1.9 PHY:PHY_STD:PHY_AUTONEG_LP_NEXTPAGE_RX

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-642: FIELDS IN PHY_AUTONEG_LP_NEXTPAGE_RX

Field Name	Bit	Access	Description	Default
LP_NEXT_PAGE_RX	15	R/O	Set by link partner to indicate that more pages follow. When cleared, this is the last of the next-pages.	0x0
LP_ACKNOWLEDGE_RX	14	R/O	Set by link partner to acknowledge the reception of last message.	0x0
LP_MESSAGE_PAGE	13	R/O	Set by Link partner if this page contains a message. When cleared this page contains unformatted code.	0x0
LP_ACKNOWLEDGE2	12	R/O	Set by link partner to indicate that it is able to act on transmitted information.	0x0
LP_TOGGLE	11	R/O	Will alternate between 0 and 1 for each received page. Used to check for errors.	0x0
LP_MESSAGE_FIELD	10:0	R/O	Contains page information, MESSAGE_PAGE indicates if this page contains either a message or unformatted code.	0x000

1.18.1.10 PHY:PHY_STD:PHY_CTRL_1000BT

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-643: FIELDS IN PHY_CTRL_1000BT

Field Name	Bit	Access	Description	Default
TX_TEST_MODE_CFG	15:13	R/W	Configure 1000BASE-T test modes; this field is only valid in 1000BASE-T mode. Other encodings are reserved and must not be selected. 0: Normal operation 1: Transmit waveform test. 2: Transmit jitter test in master mode. 3: Transmit jitter test in slave mode. 4: Transmit distortion test.	0x0
MS_MANUAL_CFG_ENA	12	R/W	Enable manual configuration of master/slave value.	0x0
MS_MANUAL_CFG	11	R/W	Configure if the PHY should configure itself as either master or slave during master/slave negotiations. This field is only valid when MS_MANUAL_CFG_ENA is set. 0: Configure as slave. 1: Configure as master.	0x0
PORT_TYPE_CFG	10	R/W	Set to indicate multi-port device, clear to indicate single-port device.	0x1
ADV_1000BT_FDX_CFG	9	R/W	Set to advertise 1000BASE-T FDX capability.	0x1
ADV_1000BT_HDX_CFG	8	R/W	Set to advertise 1000BASE-T HDX capability.	0x1

1.18.1.11 PHY:PHY_STD:PHY_STAT_1000BT

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-644: FIELDS IN PHY_STAT_1000BT

Field Name	Bit	Access	Description	Default
MS_CFG_FAULT	15	R/O	This field is set when the PHY detects a master/slave configuration fault condition and cleared on register read.	0x0
MS_CFG_RESOLUTION	14	R/O	This field indicates the result of a master/slave Negotiation. 0: Local PHY is resolved to slave. 1: Local PHY is resolved to master.	0x1
LOCAL_RECEIVER_STAT	13	R/O	The status of the local receiver (loc_rcvr_status as defined in IEEE Std. 802.3). 0: Local receiver status is NOT_OK. 1: Local receiver status is OK.	0x0
REMOTE_RECEIVER_STAT	12	R/O	The status of the remote receiver (rem_rcvr_status as defined in IEEE Std. 802.3). 0: Remote receiver status is NOT_OK. 1: Remote receiver status is OK.	0x0
LP_1000BT_FDX	11	R/O	Set if link partner advertises 1000BASE-T FDX capability.	0x0
LP_1000BT_HDX	10	R/O	Set if link partner advertises 1000BASE-T HDX capability.	0x0
IDLE_ERR_CNT	7:0	R/O	Counts each occurrence of rxerror_status = Error (rx_error_status as defined in IEEE Std. 802.3. This field is cleared on read and saturates at all-ones.	0x00

1.18.1.12 PHY:PHY_STD:MMD_ACCESS_CFG

Parent: PHY:PHY_STD

Instances: 1

The bits in this register of the main register space are a window to the EEE registers as defined in IEEE 802.3az Clause 45.

TABLE 1-645: FIELDS IN MMD_ACCESS_CFG

Field Name	Bit	Access	Description	Default
MMD_FUNCTION	15:14	R/W	Function. 0: Address 1: Data, no post increment 2: Data, post increment for read and write 3: Data, post increment for write only	0x0
MMD_DVAD	4:0	R/W	Device address as defined in IEEE 802.3az table 45-1.	0x00

1.18.1.13 PHY:PHY_STD:MMD_ADDR_DATA

Parent: PHY:PHY_STD

Instances: 1

The bits in this register of the main register space are a window to the EEE registers as defined in IEEE 802.3az Clause 45.

TABLE 1-646: FIELDS IN MMD_ADDR_DATA

Field Name	Bit	Access	Description	Default
MMD_ADDR_DATA	15:0	R/W	If MMD_ACCESS_CFG.MMD_FUNCTION is 0, MMD_ADDR_DATA specifies the address of register of the device that is specified by MMD_ACCESS_CFG.MMD_DVAD. Otherwise, MMD_ADDR_DATA specifies the data to be written to or read from the register.	0x0000

1.18.1.14 PHY:PHY_STD:PHY_STAT_1000BT_EXT1

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-647: FIELDS IN PHY_STAT_1000BT_EXT1

Field Name	Bit	Access	Description	Default
MODE_1000BX_FDX	15	R/O	The PHY is not 1000BASE-X FDX capable.	0x0
MODE_1000BX_HDX	14	R/O	The PHY is not 1000BASE-X HDX capable.	0x0
MODE_1000BT_FDX	13	R/O	The PHY is 1000BASE-T FDX capable.	0x1
MODE_1000BT_HDX	12	R/O	The PHY is 1000BASE-T HDX capable.	0x1

1.18.1.15 PHY:PHY_STD:PHY_STAT_100BTX

Parent: PHY:PHY_STD

Instances: 1

These fields are only valid in 100BASE-T mode.

TABLE 1-648: FIELDS IN PHY_STAT_100BTX

Field Name	Bit	Access	Description	Default
DESCRAM_LOCKED	15	R/O	This field is set when the 100BASE-TX descrambler is in lock and cleared when it is out of lock.	0x0
DESCRAM_ERR	14	R/O	This field is set when the PHY detects a descrambler error condition and cleared on register read.	0x0
LINK_DISCONNECT	13	R/O	This field is set when the PHY detects a 100BASE-TX link disconnect condition and cleared on register read.	0x0
LINK_STAT_100	12	R/O	This field is set when the 100BASE-TX link status is active and cleared when inactive.	0x0
RECEIVE_ERR	11	R/O	This field is set when the PHY detects a receive error condition and cleared on register read.	0x0
TRANSMIT_ERR	10	R/O	This field is set when the PHY detects a transmit error condition and cleared on register read.	0x0

TABLE 1-648: FIELDS IN PHY_STAT_100BTX (CONTINUED)

Field Name	Bit	Access	Description	Default
SSD_ERR	9	R/O	This field is set when the PHY detects a Start-of-Stream Delimiter Error condition and cleared on register read.	0x0
ESD_ERR	8	R/O	This field is set when the PHY detects an End-of-Stream Delimiter Error condition and cleared on register read.	0x0

1.18.1.16 PHY:PHY_STD:PHY_STAT_1000BT_EXT2

Parent: PHY:PHY_STD

Instances: 1

These fields are only valid in 1000BASE-T mode.

TABLE 1-649: FIELDS IN PHY_STAT_1000BT_EXT2

Field Name	Bit	Access	Description	Default
DESCRAM_LOCKED_1000	15	R/O	This field is set when the 1000BASE-T descrambler is in lock and cleared when it is out of lock.	0x0
DESCRAM_ERR_1000	14	R/O	This field is set when the PHY detects a Descrambler Error condition and cleared on register read.	0x0
LINK_DISCONNECT_1000	13	R/O	This field is set when the PHY detects a 1000BASE-T link disconnect condition and cleared on register read.	0x0
LINK_STAT_1000	12	R/O	This field is set when the 1000BASE-T link status is active and cleared when inactive.	0x0
RECEIVE_ERR_1000	11	R/O	This field is set when the PHY detects a Receive Error condition and cleared on register read.	0x0
TRANSMIT_ERR_1000	10	R/O	This field is set when the PHY detects a Transmit Error condition and cleared on register read.	0x0
SSD_ERR_1000	9	R/O	This field is set when the PHY detects a Start-of-Stream Delimiter Error condition and cleared on register read.	0x0
ESD_ERR_1000	8	R/O	This field is set when the PHY detects an End-of-Stream Delimiter Error condition and cleared on register read.	0x0
CARRIER_EXT_ERR_1000	7	R/O	This field is set when the PHY detects a 1000BASE-T Carrier Extension Error condition and cleared on register read.	0x0
BCM5400_ERR_1000	6	R/O	This field is set when the PHY detects a non-compliant BCM5400 condition. This field is only valid when the 1000BASE-T descrambler is in locked state (see DESCRAM_LOCKED_1000).	0x0
MDI_CROSSOVER_ERR	5	R/O	This field is set when the PHY detects an MDI crossover error condition.	0x0

1.18.1.17 PHY:PHY_STD:PHY_BYPASS_CTRL

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-650: FIELDS IN PHY_BYPASS_CTRL

Field Name	Bit	Access	Description	Default
TX_DIS	15	R/W	Disable the PHY transmitter. When set, the analog blocks are powered down and zeros are send to the DAC.	0x0
ENC_DEC_4B5B	14	R/W	If set, bypass the 4B5B encoder/decoder.	0x0
SCRAMBLER	13	R/W	If set, bypass the scrambler.	0x0
DESCRAMBLER	12	R/W	If set, bypass the descrambler.	0x0
PCS_RX	11	R/W	If set, bypass the PCS receiver.	0x0
PCS_TX	10	R/W	If set, bypass the PCS transmit.	0x0
LFI_TIMER	9	R/W	If set, bypass the link fail inhibit (LFI) timer.	0x0
FORCED_SPEED_AUTO_MDIX-_DIS	7	R/W	Bit for disabling HP AutoMDIX in forced 10/100 speeds, even though auto-negotiation is disabled. 0: The HP Auto-MDIX function is enabled. 1: Default value. The HP Auto-MDIX function is disabled. Use the default value when in auto-negotiation mode.	0x1
PAIR_SWAP_DIS	5	R/W	Disable automatic pair swap correction. This is a sticky field; see PHY_C-TRL_STAT_EXT.STICKY_RESET_ENA.	0x0
POL_INV_DIS	4	R/W	Disable automatic polarity inversion correction. This is a sticky field; see PHY_C-TRL_STAT_EXT.STICKY_RESET_ENA.	0x0
PARALLEL_DET_DIS	3	R/W	When cleared, the PHY ignores its advertised abilities when performing parallel detect. This is a sticky field; see PHY_C-TRL_STAT_EXT.STICKY_RESET_ENA.	0x1
PULSE_SHAPING_DIS	2	R/W	If set, disable the pulse shaping filter.	0x0
AUTO_NP_EXCHANGE_DIS	1	R/W	Disable automatic exchange of 1000BASE-T next pages. If this feature is disabled, you have the responsibility of sending next pages, determining capabilities, and configuration of the PHY after successful exchange of pages. This is a sticky field; see PHY_C-TRL_STAT_EXT.STICKY_RESET_ENA.	0x0

1.18.1.18 PHY:PHY_STD:PHY_ERROR_CNT1

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-651: FIELDS IN PHY_ERROR_CNT1

Field Name	Bit	Access	Description	Default
RX_ERR_CNT	7:0	R/O	Counter containing the number of packets received with errors for 100/1000BASE-TX. The counter saturates at 255 and it is cleared when read.	0x00

1.18.1.19 PHY:PHY_STD:PHY_ERROR_CNT2

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-652: FIELDS IN PHY_ERROR_CNT2

Field Name	Bit	Access	Description	Default
FALSE_CARRIER_CNT	7:0	R/O	Counter containing the number of false carrier incidents for 100/1000BASE-TX. The counter saturates at 255 and it is cleared when read.	0x00

1.18.1.20 PHY:PHY_STD:PHY_ERROR_CNT3

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-653: FIELDS IN PHY_ERROR_CNT3

Field Name	Bit	Access	Description	Default
LINK_DIS_CNT	7:0	R/O	Counter containing the number of copper media link disconnects. The counter saturates at 255 and it is cleared when read.	0x00

1.18.1.21 PHY:PHY_STD:PHY_CTRL_STAT_EXT

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-654: FIELDS IN PHY_CTRL_STAT_EXT

Field Name	Bit	Access	Description	Default
LINK_10BT_FORCE_ENA	15	R/W	When this field is set, the PHY link integrity state machine is bypassed, and the PHY is forced into link pass status. This is a sticky field; see PHY_CTRL_EXT.STICKY_RESET_ENA.	0x0
JABBER_DETECT_DIS	14	R/W	Disable jabber detect function. When this is disabled, the PHY allows transmission requests to be arbitrarily long without shutting down the transmitter. When cleared, the PHY shuts down the transmitter after the specified time limit specified by IEEE. This is a sticky field; see PHY_CTRL_EXT.STICKY_RESET_ENA.	0x0
ECHO_10BT_DIS	13	R/W	When this field is set, the state of the TX_EN pin does not echo onto the CRS pin, which effectively disables CRS from being asserted in half-duplex operation. When cleared, the TX_EN pin is echoed onto the CRS pin. This applies only in 10BASE-T mode. This is a sticky field; see PHY_CTRL_EXT.STICKY_RESET_ENA.	0x1

TABLE 1-654: FIELDS IN PHY_CTRL_STAT_EXT (CONTINUED)

Field Name	Bit	Access	Description	Default
SQE_10BT_DIS	12	R/W	Disable SQE (Signal Quality Error) pulses on the MAC interface. This applies only in 10BASE-T mode. This is a sticky field; see PHY_CTRL_EXT.STICKY_RESET_ENA.	0x1
SQUELCH_10BT_CFG	11:10	R/W	Configure squelch control (this only applies in the 10BASE-T mode). This is a sticky field; see PHY_CTRL_EXT.STICKY_RESET_ENA. 0: The PHY uses the squelch threshold levels prescribed by the IEEE 10BASE-T specification. 1: In this mode, the squelch levels are decreased, which may improve the bit error rate performance on long loops 2: In this mode, the squelch levels are increased, which may improve the bit error rate in high-noise environments 3: Reserved.	0x0
STICKY_RESET_ENA	9	R/W	When set, all fields described as sticky retain their value during software reset. When cleared, all fields marked as sticky are reset to their default values during software reset. This does not affect hardware resets. This is a super-sticky field, which means that it always retain its value during software reset.	0x1
EOF_ERR	8	R/O	When set, this field indicates that a defective EOF (End Of Frame) sequence was received since the last time this field was read. This field is cleared on read.	0x0
LINK_10BT_DISCONNECT	7	R/O	When set, this field indicates that the carrier integrity monitor has broken the 10BASE-T connection since the last read of this bit. This field is cleared on read.	0x0
LINK_10BT_STAT	6	R/O	This field is set when a 10BASE-T link is active. Cleared when inactive.	0x0
BROADCAST_WRITE_ENA	0	R/W	Enable any MII write operation (regardless of destination PHY) to be interpreted as a write to this PHY. This only applies to writes; read-operations are still interpreted with correct address. This is particularly useful when similar settings should be propagated to multiple PHYs. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0

1.18.1.22 PHY:PHY_STD:PHY_CTRL_EXT1

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-655: FIELDS IN PHY_CTRL_EXT1

Field Name	Bit	Access	Description	Default
FAR_END_LOOPBACK_ENA	3	R/W	Enable far end loopback in this PHY. In this mode all incoming traffic on the media interface is retransmitted back to the link partner. In addition, the incoming data also appears on the internal Rx interface to the MAC. Any data send to the PHY from the internal MAC is ignored when this mode is active.	0x0

1.18.1.23 PHY:PHY_STD:PHY_CTRL_EXT2

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-656: FIELDS IN PHY_CTRL_EXT2

Field Name	Bit	Access	Description	Default
EDGE_RATE_CFG	15:13	R/W	Control the transmit DAC slew rate in 100BASE-TX mode only. The difference between each setting is approximately 200ps to 300ps, with the +3 setting resulting in the slowest edge rate, and the -4 setting resulting in the fastest edge rate. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. 011: +5 Edge rate (slowest). 010: +4 Edge rate. 001: +3 Edge rate. 000: +2 Edge rate. 111: +1 Edge rate. 110: Nominal edge rate. 101: -1 Edge rate. 100: -2 Edge rate (fastest).	0x1
PICMG_REDUCED_POWER_ENA	12	R/W	Enable PICMC reduce power mode: In this mode, portions of the DSP processor are turned off, which reduces the PHY's operating power. The DSP performance characteristics in this mode are configured to support the channel characteristics specified in the PICMC 2.16 and PICMC 3.0 specifications. The application of this mode is in environments that have a high signal to noise ratio on the media. For example, Ethernet over backplane, or where cable length is short (less than 10m). When this field is cleared, the PHY operates in normal DSP mode. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
RESERVED	11:6	R/W	Must be set to its default.	0x01

TABLE 1-656: FIELDS IN PHY_CTRL_EXT2 (CONTINUED)

Field Name	Bit	Access	Description	Default
JUMBO_PKT_ENA	5:4	R/W	Controls the symbol buffering for the receive synchronization FIFO used in 1000BASE-T mode. Other encodings are reserved and must not be selected. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. Note: When set, the default maximum packet values are based on 100 ppm driven reference clock to the device. Controlling the ppm offset between the MAC and the PHY as specified in the field encoding description results in a higher jumbo packet length. 00: Normal IEEE 1518-byte packet length. 01: 9-kilobyte jumbo packet length (12 kilobytes with 60 ppm or better reference clock). 10: 12-kilobyte jumbo packet length (16 kilobytes with 70 ppm or better reference clock). 11: Reserved.	0x0
RESERVED	3:1	R/W	Must be set to its default.	0x6
CON_LOOPBACK_1000BT_ENA	0	R/W	Set PHY into 1000BASE-T connector loopback mode. When enabled, the PHY only works with a connector loopback.	0x0

1.18.1.24 PHY:PHY_STD:PHY_INT_MASK

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-657: FIELDS IN PHY_INT_MASK

Field Name	Bit	Access	Description	Default
PHY_INT_ENA	15	R/W	Enable global PHY interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
SPEED_STATE_CHANGE_INT_ENA	14	R/W	Set to unmask speed change interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
LINK_STATE_CHANGE_INT_ENA	13	R/W	Set to unmask link state/energy detected change interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
FDX_STATE_CHANGE_INT_ENA	12	R/W	Set to unmask FDX change interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
AUTONEG_ERR_INT_ENA	11	R/W	Set to unmask auto-negotiation error interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
AUTONEG_DONE_INT_ENA	10	R/W	Set to unmask auto-negotiation-done/interlock done interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0

TABLE 1-657: FIELDS IN PHY_INT_MASK (CONTINUED)

Field Name	Bit	Access	Description	Default
INLINE_POW_DET_INT_ENA	9	R/W	Set to unmask In-line Powered Device Detected interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
SYMBOL_ERR_INT_ENA	8	R/W	Set to unmask Symbol Error interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
FAST_LINK_FAIL_INT_ENA	7	R/W	Set to unmask fast link failure interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
WOL_INT_ENA	6	R/W	Set to unmask Wake-On-Lan interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
EXTENDED_INT_ENA	5	R/W	Set to unmask EXTENDED interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
Reserve	4	R/W	Reserved	0x0
FALSE_CARRIER_INT_ENA	3	R/W	Set to unmask False Carrier interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
LINK_SPEED_DOWNSHIFT_INT_ENA	2	R/W	Set to unmask link speed downshift interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
MASTER_SLAVE_INT_ENA	1	R/W	Set to unmask master/slave interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
RX_ER_INT_ENA	0	R/W	Set to unmask RX_ER interrupt. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0

1.18.1.25 PHY:PHY_STD:PHY_INT_STAT

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-658: FIELDS IN PHY_INT_STAT

Field Name	Bit	Access	Description	Default
PHY_INT_PEND	15	R/O	Set when an unacknowledged 'global' PHY interrupt is pending, the cause of the interrupt can be determined by examining the other fields of this register. This field is set no matter the state of PHY_INT_MASK.PHY_INT_ENA. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
SPEED_STATE_CHANGE_INT_PEND	14	R/O	Set when a speed interrupt is pending, this is activated when the operating speed of the PHY changes (requires that auto-negotiation is enabled; see PHY_CTRL.AUTONEG_ENA). This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0

TABLE 1-658: FIELDS IN PHY_INT_STAT (CONTINUED)

Field Name	Bit	Access	Description	Default
LINK_STATE_CHANGE_INT_PEND	13	R/O	Set when a Link State/Energy Detected interrupt is pending. This interrupt occurs when the link status of the PHY changes, or if ActiPHY mode is enabled and energy is detected on the media (see PHY_AUX_CTRL_STAT.ACTIPHY_ENA). This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
FDX-_STATE_CHANGE_INT_PEND	12	R/O	Set when an FDX interrupt is pending. FDX interrupt is caused when the FDX/HDX state of the PHY changes (requires that auto-negotiation is enabled; see PHY_CTRL.AUTONEG_ENA). This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
AUTONEG_ERR_INT_PEND	11	R/O	Set when an auto-negotiation Error interrupt is pending, this is caused when an error is detected by the auto-negotiation state machine. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
AUTONEG_DONE_INT_PEND	10	R/O	Set when an auto-negotiation-Done/Interlock Done interrupt is pending, this is caused when the Auto-negotiation finishes a negotiation process. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
INLINE_POW_DET_INT_PEND	9	R/O	Set when an In-line Powered Device Detected interrupt is pending. This interrupt is caused when a device requiring in-line power is detected (requires that detection is enabled; see PHY_CTRL_EXT4.INLINE_-DETECT_ENA). This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
SYMBOL_ERR_INT_PEND	8	R/O	Set when a Symbol Error interrupt is pending, this is caused by detection of a symbol error by the descrambler. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
FAST_LINK_FAIL_INT_PEND	7	R/O	Set when a fast link failure interrupt is pending. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
WOL_INT_PEND	6	R/O	Set when a Wake-On-Lan interrupt is pending. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
EXTENDED_INT_PEND	4	R/O	Set when an Extended interrupt is pending. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
FALSE_CARRIER_INT_PEND	3	R/O	Set when a False Carrier interrupt is pending. False Carrier interrupt is generated when the PHY detects a false carrier. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
LINK_SPEED_DOWN-SHIFT_INT_PEND	2	R/O	Set when a link speed downshift interrupt is pending. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0

TABLE 1-658: FIELDS IN PHY_INT_STAT (CONTINUED)

Field Name	Bit	Access	Description	Default
MASTER_SLAVE_ER-R_INT_PEND	1	R/O	Set when a master/slave interrupt is pending. This interrupt is set when a master/slave resolution error us detected. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0
RX_ER_INT_PEND	0	R/O	Set when a RX_ER interrupt is pending. This interrupt is set when an RX_ER condition occurs. This field is self-clearing; i.e. interrupt is acknowledged on read.	0x0

1.18.1.26 PHY:PHY_STD:PHY_AUX_CTRL_STAT

Parent: PHY:PHY_STD

Instances: 1

Copied fields have the same default values as their source fields.

TABLE 1-659: FIELDS IN PHY_AUX_CTRL_STAT

Field Name	Bit	Access	Description	Default
AUTONEG_COMPLETE_AUX	15	R/O	A read-only copy of PHY_STAT.AUTONEG_COMPLETE. Repeated here for convenience. See note for this register.	0x0
AUTONEG_STAT	14	R/O	When set the auto-negotiation function has been disabled (in PHY_C-TRL.AUTONEG_ENA.)	0x0
NO_MDI_X_IND	13	R/O	When this field is set, the auto-negotiation state machine has determined that cross-over does not exist in the signal path. This field is only valid after 'descrambler lock' has been achieved (see PHY_STAT_1000BT_EXT.DESCRAM_LOCKED) and 'automatic pair swap correction' is enabled (see PHY_BYPASS_C-TRL.PAIR_SWAP_DISABLE).	0x0
CD_PAIR_SWAP	12	R/O	When this field is set, the PHY has determined that the subchannel cable pairs C and D were swapped between the far-end transmitter and the receiver. In this case, the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE).	0x0
A_POL_INVERSION	11	R/O	When set, this field indicates that the polarity of pair A was inverted between the far-end transmitter and the receiver. In this case the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE). 0: Polarity is swapped on pair A. 1: Polarity is not swapped on pair A.	0x0

TABLE 1-659: FIELDS IN PHY_AUX_CTRL_STAT (CONTINUED)

Field Name	Bit	Access	Description	Default
B_POL_INVERSION	10	R/O	When set, this field indicates that the polarity of pair B was inverted between the far-end transmitter and the receiver. In this case the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE). 0: Polarity is swapped on pair B. 1: Polarity is not swapped on pair B.	0x0
C_POL_INVERSION	9	R/O	When set, this field indicates that the polarity of pair C was inverted between the far-end transmitter and the receiver. In this case the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE) and in 1000BASE-T mode. 0: Polarity is swapped on pair C. 1: Polarity is not swapped on pair C.	0x0
D_POL_INVERSION	8	R/O	When set, this field indicates that the polarity of pair D was inverted between the far-end transmitter and the receiver. In this case the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE) and in 1000BASE-T mode. 0: Polarity is swapped on pair D. 1: Polarity is not swapped on pair D.	0x0
ACTIPHY_LINK_TIMER_MSB_CFG	7	R/W	Most significant bit of the link status time-out timer. Together with ACTIPHY_LINK_TIMER_LSB_CFG, this field determines the duration from losing the link to the ActiPHY enters low power state. 0: 1 seconds. 1: 2 seconds. 2: 3 seconds. 3: 4 seconds.	0x0
ACTIPHY_ENA	6	R/W	Enable ActiPHY power management mode. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
FDX_STAT	5	R/O	This field indicates the actual FDX/HDX operating mode of the PHY. 0: Half-duplex. 1: Full-duplex.	0x0
SPEED_STAT	4:3	R/O	This field indicates the actual operating speed of the PHY. 0: Speed is 10BASE-T. 1: Speed is 100BASE-TX. 2: Speed is 1000-BASE-T. 3: Reserved.	0x0
ACTIPHY_LINK_TIMER_LSB_CFG	2	R/W	See ACTIPHY_LINK_TIMER_MSB_CFG.	0x1

1.18.1.27 PHY:PHY_STD:PHY_LED_MODE_SEL

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-660: FIELDS IN PHY_LED_MODE_SEL

Field Name	Bit	Access	Description	Default
RESERVED	15:12	R/W	Must be set to its default.	0x8
LED1_MODE_SEL	7:4	R/W	Select from LED modes 0 through 15. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x2
LED0_MODE_SEL	3:0	R/W	Select from LED modes 0 through 15. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. 0: Link/Activity 1: Link1000/Activity 2: Link100/Activity 3: Link10/Activity 4: Link100/1000/Activity 5: Link10/1000/Activity 6: Link10/100/Activity 7: Reserved 8: Duplex/Collision 9: Collision 10: Activity 11: Reserved 12: Auto-Negotiation Fault 13: Reserved 14: Force LED Off 15: Force LED On	0x1

1.18.1.28 PHY:PHY_STD:PHY_LED_BEHAVIOR_CTRL

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-661: FIELDS IN PHY_LED_BEHAVIOR_CTRL

Field Name	Bit	Access	Description	Default
PULSING_ENA	12	R/W	Enable LED pulsing with programmable duty cycle. The duty cycle is programmed in PHY_GP::PHY_ENHANCED_LED_CTRL.LED_PULSE_DUTY. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. 0: Normal operation. 1: LEDs pulse with a 5 kHz, programmable duty cycle when active.	0x0

TABLE 1-661: FIELDS IN PHY_LED_BEHAVIOR_CTRL (CONTINUED)

Field Name	Bit	Access	Description	Default
BLINK_RATE_CFG	11:10	R/W	Configure blink rate of LEDs when applicable. If pulse stretching has been selected rather than blink, this controls the stretch-period rather than frequency. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. 00: 2.5 Hz blink rate/400 ms pulse-stretch. 01: 5 Hz blink rate/200 ms pulse-stretch. 10: 10 Hz blink rate/100 ms pulse-stretch. 11: 20 Hz blink rate/50 ms pulse-stretch. The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports.	0x1
LED1_PULSE_STRETCH_ENA	6	R/W	Enable pulse-stretch behavior instead of blinking for LED1. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
LED0_PULSE_STRETCH_ENA	5	R/W	Enable pulse-stretch behavior instead of blinking for LED0. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
LED1_COMBINE_DIS	1	R/W	Disabling of the LED1 combine feature. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. 0: Combine enabled (link/activity, duplex/collision). 1: Disable combination (link only, duplex only).	0x0
LED0_COMBINE_DIS	0	R/W	Disabling of the LED0 combine feature. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. 0: Combine enabled (link/activity, duplex/collision). 1: Disable combination (link only, duplex only).	0x0

1.18.1.29 PHY:PHY_STD:PHY_MEMORY_PAGE_ACCESS

Parent: PHY:PHY_STD

Instances: 1

TABLE 1-662: FIELDS IN PHY_MEMORY_PAGE_ACCESS

Field Name	Bit	Access	Description	Default
PAGE_ACCESS_CFG	4:0	R/W	This bit controls the mapping of PHY registers 0x10 through 0x1E. When changing pages, all registers in the range 0x10 through 0x1E are replaced - even if the new memory-page does not define all addresses in the range 0x10 through 0x1E. 0: Register Page 0 is mapped (standard set). 1: Register Page 1 is mapped (extended set 1). 2: Register Page 2 is mapped (extended set 2). 16: Register Page 16 is mapped (general purpose).	0x00

1.18.2 PHY:PHY_EXT1

Parent: PHY

Instances: 1

Set register 0x1F to 0x0001 to make the extended set of registers visible in the address range 0x10 through 0x1E. Set register 0x1F to 0x0000 to revert back to the standard register set.

TABLE 1-663: REGISTERS IN PHY_EXT1

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_CRC_GOOD_CNT	0x00000048	1	CRC Good Counter (Address 18E1)	Page 299
PHY_EXT_MODE_CTRL	0x0000004C	1	Extended Mode Control (Address 19E1)	Page 300
PHY_CTRL_EXT3	0x00000050	1	Extended Control Number 3 (Address 20E1)	Page 300
PHY_CTRL_EXT4	0x0000005C	1	Extended Control Number 4 (Address 23E1)	Page 301
PHY_VERIPHY_CTRL1	0x00000060	1	VeriPHY Control Number 1 (Address 24E1)	Page 302
PHY_VERIPHY_CTRL2	0x00000064	1	VeriPHY Control Number 2 (Address 25E1)	Page 302
PHY_VERIPHY_CTRL3	0x00000068	1	VeriPHY Control Number 3 (Address 26E1)	Page 302
PHY_1000BT_EPG1	0x00000074	1	1000BASE-T Ethernet Packet Generator Number 1 (Address 29E1)	Page 303
PHY_1000BT_EPG2	0x00000078	1	1000BASE-T Ethernet Packet Generator Number 2 (Address 30E1)	Page 304

1.18.2.1 PHY:PHY_EXT1:PHY_CRC_GOOD_CNT

Parent: PHY:PHY_EXT1

Instances: 1

TABLE 1-664: FIELDS IN PHY_CRC_GOOD_CNT

Field Name	Bit	Access	Description	Default
PACKET_SINCE_LAST_READ	15	R/O	Packet received since last read. This is a self-clearing bit.	0x0
CRC_GOOD_PKT_CNT	13:0	R/O	Counter containing the number of packets with valid CRCs; this counter does not saturate and rolls over. This is a self-clearing field.	0x0000

1.18.2.2 PHY:PHY_EXT1:PHY_EXT_MODE_CTRL

Parent: PHY:PHY_EXT1

Instances: 1

TABLE 1-665: FIELDS IN PHY_EXT_MODE_CTRL

Field Name	Bit	Access	Description	Default
LED1_EXT_MODE_ENA	13	R/W	Enable extended LED mode for LED1. For available LED modes, see LED0_EXT_-MODE_ENA.	0x0
LED0_EXT_MODE_ENA	12	R/W	Enable extended LED mode for LED0. If set, the available LED modes selected in PHY_LED_MODE_SEL.LED0_MODE_SEL are: 0-3: Reserved 4: Force LED Off. 5: Force LED On. LED pulsing is disabled in this mode. 6: Fast Link Fail. 7-15: Reserved.	0x0
LED_BLINK_SUPPRESS	11	R/W	Suppress LED blink after reset. 0: Suppress LED blink after COMA_MODE is deasserted. 1: Blink LEDs after COMA_MODE is deasserted.	0x0
FORCE_MDI_CROSS-OVER_ENA	3:2	R/W	Force MDI crossover. 00: Normal HP Auto-MDIX operation. 01: Reserved. 10: Copper media forced to MDI. 11: Copper media forced MDI-X.	0x0

1.18.2.3 PHY:PHY_EXT1:PHY_CTRL_EXT3

Parent: PHY:PHY_EXT1

Instances: 1

TABLE 1-666: FIELDS IN PHY_CTRL_EXT3

Field Name	Bit	Access	Description	Default
RESERVED	15	R/O	Must be set to its default.	0x1

TABLE 1-666: FIELDS IN PHY_CTRL_EXT3 (CONTINUED)

Field Name	Bit	Access	Description	Default
ACTIPHY_SLEEP_TIMER	14:13	R/W	This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. 00: 1 second. 01: 2 seconds. 10: 3 seconds. 11: 4 seconds.	0x1
ACTIPHY_WAKEUP_TIMER	12:11	R/W	This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. 00: 160 ms. 01: 400 ms. 10: 800 ms. 11: 2 seconds.	0x0
NO_PREAMBLE_10BT_ENA	5	R/W	If set, 10BASE-T asserts RX_DV indication when data is presented to the receiver even without a preamble preceding it.This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
SPEED_DOWNSHIFT_ENA	4	R/W	Enables automatic downshift the auto-negotiation advertisement to the next lower available speed after the number of failed 1000BASE-T auto-negotiation attempts specified in SPEED_DOWNSHIFT_CFG. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
SPEED_DOWNSHIFT_CFG	3:2	R/W	Configures the number of unsuccessful 1000BASE-T auto-negotiation attempts that are required before the auto-negotiation advertisement is downshifted to the next lower available speed. This field applies only if automatic downshift of speed is enabled (see SPEED_DOWNSHIFT_ENA). This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA. 00: Downshift after 2 failed attempts. 01: Downshift after 3 failed attempts. 10: Downshift after 4 failed attempts. 11: Downshift after 5 failed attempts.	0x1
SPEED_DOWNSHIFT_STAT	1	R/O	This status field indicates that a downshift is required in order for link to be established. If automatic downshifting is enabled (see SPEED_DOWNSHIFT_ENA), the current link speed is a result of a downshift.	0x0

1.18.2.4 PHY:PHY_EXT1:PHY_CTRL_EXT4

Parent: PHY:PHY_EXT1

Instances: 1

The reset value of the address fields (PHY_ADDR) corresponds to the PHY in which it resides.

TABLE 1-667: FIELDS IN PHY_CTRL_EXT4

Field Name	Bit	Access	Description	Default
PHY_ADDR	15:11	R/O	This field contains the PHY address of the current PHY port.	0x00

TABLE 1-667: FIELDS IN PHY_CTRL_EXT4 (CONTINUED)

Field Name	Bit	Access	Description	Default
INLINE_POW_DET_ENA	10	R/W	Enables detection of inline powered device as part of the auto-negotiation process. This is a sticky field; see PHY_CTRL_STAT_EXT.STICKY_RESET_ENA.	0x0
INLINE_POW_DET_STAT	9:8	R/O	This field shows the status if a device is connected to the PHY that requires inline power. This field is only valid if inline powered device detection is enabled (see INLINE_POW_DET_ENA). 00: Searching for devices. 01: Device found that requires inline power. 10: Device found that does not require inline power. 11: Reserved.	0x0
CRC_1000BT_CNT	7:0	R/O	This field indicates how many packets are received that contain a CRC error. This field is cleared on read and saturates at all ones.	0x00

1.18.2.5 PHY:PHY_EXT1:PHY_VERIPHY_CTRL1

Parent: PHY:PHY_EXT1

Instances: 1

TABLE 1-668: FIELDS IN PHY_VERIPHY_CTRL1

Field Name	Bit	Access	Description	Default
VERIPHY_TRIGGER	15	R/W	Set to trigger a VeriPHY operation. This field is cleared by hardware when acknowledged.	0x0
VERIPHY_RES_VALID	14	R/O	This field indicates whether VeriPHY results are valid.	0x0
PAIR_A_DIST	13:8	R/O	Loop length or distance to anomaly for pair A (1, 2). Resolution is 3 meters.	0x00
PAIR_B_DIST	5:0	R/O	Loop length or distance to anomaly for pair B (3, 6). Resolution is 3 meters.	0x00

1.18.2.6 PHY:PHY_EXT1:PHY_VERIPHY_CTRL2

Parent: PHY:PHY_EXT1

Instances: 1

TABLE 1-669: FIELDS IN PHY_VERIPHY_CTRL2

Field Name	Bit	Access	Description	Default
PAIR_C_DIST	13:8	R/O	Loop length or distance to anomaly for pair C (4, 5). Resolution is 3 meters.	0x00
PAIR_D_DIST	5:0	R/O	Loop length or distance to anomaly for pair D (7, 8). Resolution is 3 meters.	0x00

1.18.2.7 PHY:PHY_EXT1:PHY_VERIPHY_CTRL3

Parent: PHY:PHY_EXT1

Instances: 1

TABLE 1-670: FIELDS IN PHY_VERIPHY_CTRL3

Field Name	Bit	Access	Description	Default
PAIR_A_TERMINATION_STAT	15:12	R/O	Termination fault for pair A (1, 2). See PAIR_D_TERMINATION_STAT for encoding.	0x0
PAIR_B_TERMINATION_STAT	11:8	R/O	Termination fault for pair B (3, 6). See PAIR_D_TERMINATION_STAT for encoding.	0x0
PAIR_C_TERMINATION_STAT	7:4	R/O	Termination fault for pair C (4, 5). See PAIR_D_TERMINATION_STAT for encoding.	0x0
PAIR_D_TERMINATION_STAT	3:0	R/O	Termination fault for pair D (7, 8). 0000: Correctly terminated pair 0001: Open pair 0010: Shorted pair 0100: Abnormal termination 1000: Cross-pair short to pair A 1001: Cross-pair short to pair B 1010: Cross-pair short to pair C 1011: Cross-pair short to pair D	0x0

1.18.2.8 PHY:PHY_EXT1:PHY_1000BT_EPG1

Parent: PHY:PHY_EXT1

Instances: 1

TABLE 1-671: FIELDS IN PHY_1000BT_EPG1

Field Name	Bit	Access	Description	Default
EPG_ENA	15	R/W	Enables the Ethernet packet generator. When this field is set, the EPG is selected as the driving source for the PHY transmit signals, and the MAC transmit pins are disabled.	0x0
EPG_RUN_ENA	14	R/W	Begin transmission of Ethernet packets. Clear to stop the transmission of packets. If a transmission is in progress, the transmission of packets is stopped after the current packet is transmitted. This field is valid only when the EPG is enabled (see EPG_ENA).	0x0
TRANSMIT_DURATION_CFG	13	R/W	Configure the duration of the packet generation. When set, the EPG continuously transmits packets as long as field EPG_RUN_ENA is set. When cleared, the EPG transmits 30,000,000 packets when field EPG_RUN_ENA is set, after which time, field EPG_RUN_ENA is automatically cleared. This field is latched when packet generation begins by setting EPG_RUN_ENA in this register.	0x0

TABLE 1-671: FIELDS IN PHY_1000BT_EPG1 (CONTINUED)

Field Name	Bit	Access	Description	Default
PACKET_LEN_CFG	12:11	R/W	This field selects the length of packets to be generated by the EPG. This field is latched when generation of packets begins by setting EPG_RUN_ENA in this register. 00: 125-byte packets. 01: 64-byte packets. 10: 1518-byte packets. 11: 10,000-byte packets.	0x0
INTER_PACKET_GAB_CFG	10	R/W	This field configures the inter packet gab for packets generated by the EPG. This field is latched when generation of packets begins by setting EPG_RUN_ENA in this register. 0: 96 ns inter-packet gap. 1: 9,192 ns inter-packet gap.	0x0
DEST_ADDR_CFG	9:6	R/W	This field configures the low nibble of the most significant byte of the destination MAC address. The rest of the destination MAC address is all-ones. For example, setting this field to 0x2 results in packets generated with a destination MAC address of 0xF2FFFFFFFFFF. This field is latched when generation of packets begins by setting EPG_RUN_ENA in this register.	0x1
SRC_ADDR_CFG	5:2	R/W	This field configures the low nibble of the most significant byte of the source MAC address. The rest of the source MAC address is all-ones. For example, setting this field to 0xE results in packets generated with a source MAC address of 0xFEFFFFFFFFFF. This field is latched when generation of packets begins by setting EPG_RUN_ENA in this register.	0x0
PAYLOAD_TYPE	1	R/W	Payload type. 0: Fixed based on payload pattern. 1: Randomly generated payload pattern.	0x0
BAD_FCS_ENA	0	R/W	When this field is set, the EPG generates packets containing an invalid Frame Check Sequence (FCS). When cleared, the EPG generates packets with a valid FCS. This field is latched when generation of packets begins by setting EPG_RUN_ENA in this register.	0x0

1.18.2.9 PHY:PHY_EXT1:PHY_1000BT_EPG2

Parent: PHY:PHY_EXT1

Instances: 1

TABLE 1-672: FIELDS IN PHY_1000BT_EPG2

Field Name	Bit	Access	Description	Default
PACKET_PAYLOAD_CFG	15:0	R/W	Each packet generated by the EPG contains a repeating sequence of this field as payload. This field is latched when generation of packets begins by setting PHY_1000BT_EPG1.EPG_RUN_ENA.	0x0000

1.18.3 PHY:PHY_EXT2

Parent: PHY

Instances: 1

Set register 0x1F to 0x0002 to make the extended set of registers visible in the address range 0x10 through 0x1E. Set register 0x1F to 0x0000 to revert back to the standard register set.

TABLE 1-673: REGISTERS IN PHY_EXT2

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_PMD_TX_CTRL	0x00000040	1	Cu PMD Transmit Control (Address 16E2)	Page 305
PHY_EEE_CTRL	0x00000044	1	EEE and LED Control (Address 17E2)	Page 306
PHY_WOL_MAC_ADDR0	0x00000048	1	Wake-On-LAN MAC address [15:0]	Page 306
PHY_WOL_MAC_ADDR1	0x0000004C	1	Wake-On-LAN MAC address [31:16]	Page 307
PHY_WOL_MAC_ADDR2	0x00000050	1	Wake-On-LAN MAC address [47:32]	Page 307
PHY_SECURE_ON_PASSWD0	0x00000054	1	Secure-On password [15:0]	Page 307
PHY_SECURE_ON_PASSWD1	0x00000058	1	Secure-On password [31:16]	Page 307
PHY_SECURE_ON_PASSWD2	0x0000005C	1	Secure-On password [47:32]	Page 307
PHY_WOL_MDINT_CTRL	0x00000060	1		Page 308
PHY_EXT_INT_MASK	0x00000064	1	Extended Interrupt mask	Page 308
PHY_EXT_INT_STAT	0x00000068	1	Extended Interrupt Status	Page 308

1.18.3.1 PHY:PHY_EXT2:PHY_PMD_TX_CTRL

Parent: PHY:PHY_EXT2

Instances: 1

This register consists of the bits that provide control over the amplitude settings for the transmit side Cu PMD interface. These bits provide the ability to make small adjustments in the signal amplitude to compensate for minor variations in the magnetic from different vendors. Extreme caution must be exercised when changing these settings from the default values as they have a direct impact on the signal quality. Changing these settings also affects the linearity and harmonic distortion of the transmitted signals. Please contact the Vitesse Applications Support team for further help with changing these values.

TABLE 1-674: FIELDS IN PHY_PMD_TX_CTRL

Field Name	Bit	Access	Description	Default
SIG_AMPL_1000BT	15:12	R/W	1000BT signal amplitude trim.	0x0
SIG_AMPL_100BTX	11:8	R/W	100BASE-TX signal amplitude trim.	0x0
SIG_AMPL_10BT	7:4	R/W	10BASE-T signal amplitude trim.	0x5
SIG_AMPL_10BTE	3:0	R/W	10BASE-Te signal amplitude trim.	0x0

1.18.3.2 PHY:PHY_EXT2:PHY_EEE_CTRL

Parent: PHY:PHY_EXT2

Instances: 1

TABLE 1-675: FIELDS IN PHY_EEE_CTRL

Field Name	Bit	Access	Description	Default
EEE_10BTE_ENA	15	R/W	Enable energy efficient (IEEE 802.3az) 10BASE-Te operating mode.	0x0
FORCE_1000BT_ENA	5	R/W	Enable 1000BT force mode to allow PHY to link up in 1000BT mode without forcing master/slave when PHY_STD::PHY_CTRL.SPEED_SEL_LSB_CFG=0 and PHY_STD::PHY_CTRL.SPEED_SEL_MSB_CFG=1.	0x0
FORCE_LPI_TX_ENA	4	R/W	Force transmit LPI. 0: Transmit idles being received from the MAC. 1: Enable the EPG to transmit LPI on the MDI instead of normal idles when receiving normal idles from the MAC.	0x0
EEE_LPI_TX_100BTX_DIS	3	R/W	Disable transmission of EEE LPI on transmit path MDI in 100BASE-TX mode when receiving LPI from MAC.	0x0
EEE_LPI_RX_100BTX_DIS	2	R/W	Disable transmission of EEE LPI on receive path MAC interface in 100BASE-TX mode when receiving LPI from the MDI.	0x0
EEE_LPI_TX_1000BT_DIS	1	R/W	Disable transmission of EEE LPI on transmit path MDI in 1000BT mode when receiving LPI from MAC.	0x0
EEE_LPI_RX_1000BT_DIS	0	R/W	Disable transmission of EEE LPI on receive path MAC interface in 1000BT mode when receiving LPI from the MDI.	0x0

1.18.3.3 PHY:PHY_EXT2:PHY_WOL_MAC_ADDR0

Parent: PHY:PHY_EXT2

Instances: 1

Wake-On-LAN MAC address [15:0]

TABLE 1-676: FIELDS IN PHY_WOL_MAC_ADDR0

Field Name	Bit	Access	Description	Default
WOL_MAC_ADDR0	15:0	R/W	Wake-On-LAN MAC address bits [15:0]	0x0000

1.18.3.4 PHY:PHY_EXT2:PHY_WOL_MAC_ADDR1

Parent: PHY:PHY_EXT2

Instances: 1

Wake-On-LAN MAC address [31:16]

TABLE 1-677: FIELDS IN PHY_WOL_MAC_ADDR1

Field Name	Bit	Access	Description	Default
WOL_MAC_ADDR1	15:0	R/W	Wake-On-LAN MAC address bits [31:16]	0x0000

1.18.3.5 PHY:PHY_EXT2:PHY_WOL_MAC_ADDR2

Parent: PHY:PHY_EXT2

Instances: 1

Wake-On-LAN MAC address [47:32]

TABLE 1-678: FIELDS IN PHY_WOL_MAC_ADDR2

Field Name	Bit	Access	Description	Default
WOL_MAC_ADDR2	15:0	R/W	Wake-On-LAN MAC address bits [47:32]	0x0000

1.18.3.6 PHY:PHY_EXT2:PHY_SECURE_ON_PASSWD0

Parent: PHY:PHY_EXT2

Instances: 1

Secure-On password [15:0]

TABLE 1-679: FIELDS IN PHY_SECURE_ON_PASSWD0

Field Name	Bit	Access	Description	Default
SECURE_ON_PASSWD0	15:0	R/W	Secure-On password for Wake-on-LAN bits [15:0]	0x0000

1.18.3.7 PHY:PHY_EXT2:PHY_SECURE_ON_PASSWD1

Parent: PHY:PHY_EXT2

Instances: 1

Secure-On password [31:16]

TABLE 1-680: FIELDS IN PHY_SECURE_ON_PASSWD1

Field Name	Bit	Access	Description	Default
SECURE_ON_PASSWD1	15:0	R/W	Secure-On password for Wake-on-LAN bits [31:16]	0x0000

1.18.3.8 PHY:PHY_EXT2:PHY_SECURE_ON_PASSWD2

Parent: PHY:PHY_EXT2

Instances: 1

Secure-On password [47:32]

TABLE 1-681: FIELDS IN PHY_SECURE_ON_PASSWD2

Field Name	Bit	Access	Description	Default
SECURE_ON_PASSWD2	15:0	R/W	Secure-On password for Wake-on-LAN bits [47:32]	0x0000

1.18.3.9 PHY:PHY_EXT2:PHY_WOL_MDINT_CTRL

Parent: PHY:PHY_EXT2

Instances: 1

TABLE 1-682: FIELDS IN PHY_WOL_MDINT_CTRL

Field Name	Bit	Access	Description	Default
SEC_ON_ENA	13	R/W	Secure-On enable	0x0
SEC_ON_PWD_LEN	12	R/W	Secure-On password length 0: 6 byte password, 1: 4 byte password	0x0
MAGIC_PKT_ADD_REP_CNT	11:8	R/W	Address repetition count in the Magic packet. 0x0: =1, 0xF:=16	0xF
MDINT_CTRL	1	R/W	MDINT signal control. 0: Interrupt signal from both ports are combined and then driven onto both MDINT pins. 1: Interrupt signals from Port 0 are indicated on MDINT_0 and interrupt signals from Port 1 are indicated on MDINT_1	0x0

1.18.3.10 PHY:PHY_EXT2:PHY_EXT_INT_MASK

Parent: PHY:PHY_EXT2

Instances: 1

Extended Interrupt mask

TABLE 1-683: FIELDS IN PHY_EXT_INT_MASK

Field Name	Bit	Access	Description	Default
RX_FIFO_ERR_INT_ENA	13	R/W	Rx FIFO overflow/underflow interrupt mask	0x0
TX_FIFO_ERR_INT_ENA	12	R/W	Tx FIFO overflow/underflow interrupt mask	0x0
RR_SWC_COMPLETE_INT_ENA	4	R/W	RR switch over complete interrupt mask	0x0
EEE_LINK_FAIL_INT_ENA	3	R/W	EEE link fail interrupt mask	0x0
EEE_RX_TQ_INT_ENA	2	R/W	EEE Rx TQ timer interrupt mask	0x0
EEE_WAIT_TS_INT_ENA	1	R/W	EEE wait quiet/Rx TS timer interrupt mask	0x0
EEE_WAKE_ERR_INT_ENA	0	R/W	EEE wake error interrupt mask	0x0

1.18.3.11 PHY:PHY_EXT2:PHY_EXT_INT_STAT

Parent: PHY:PHY_EXT2

Instances: 1

Extended Interrupt Status

TABLE 1-684: FIELDS IN PHY_EXT_INT_STAT

Field Name	Bit	Access	Description	Default
RX_FIFO_ERR_INT_STAT	13	R/O		0x0
TX_FIFO_ERR_INT_STAT	12	R/O	Tx FIFO overflow/underflow interrupt status	0x0
EEE_LINK_FAIL_INT_STAT	3	R/O	EEE link fail interrupt status	0x0
EEE_RX_TQ_INT_STAT	2	R/O	EEE Rx TQ timer interrupt status	0x0
EEE_WAIT_TS_INT_STAT	1	R/O	EEE wait quiet/Rx TS timer interrupt status	0x0
EEE_WAKE_ERR_INT_STAT	0	R/W	EEE wake error interrupt mask	0x0

1.18.4 PHY:PHY_GP

Parent: PHY

Instances: 1

Set register 0x1F to 0x0010 to access the general purpose registers. This sets all 32 registers to the general purpose register space. Set register 0x1F to 0x0000 to revert back to the standard register set.

TABLE 1-685: REGISTERS IN PHY_GP

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_COMA_MODE_CTRL	0x00000038	1	Coma Mode Control (Address 14G)	Page 309
PHY_RCVD_CLK0_CTRL	0x0000005C	1	Recovered Clock 0 Control (Address 23G)	Page 310
PHY_RCVD_CLK1_CTRL	0x00000060	1	Recovered Clock 1 Control (Address 24G)	Page 311
PHY_ENHANCED_LED_CTRL	0x00000064	1	Enhanced LED Control (Address 25G)	Page 312
PHY_GLOBAL_INT_STAT	0x00000074	1	Global Interrupt Status (Address 29G)	Page 312

1.18.4.1 PHY:PHY_GP:PHY_COMA_MODE_CTRL

Parent: PHY:PHY_GP

Instances: 1

TABLE 1-686: FIELDS IN PHY_COMA_MODE_CTRL

Field Name	Bit	Access	Description	Default
COMA_MODE_OE	13	R/W	COMA_MODE output enable. Active low. 0: COMA_MODE pin is an output. 1: COMA_MODE pin is an input.	0x0
COMA_MODE_OUTPUT	12	R/W	COMA_MODE output data.	0x0
COMA_MODE_INPUT	11	R/O	COMA_MODE input data.	0x0

TABLE 1-686: FIELDS IN PHY_COMA_MODE_CTRL (CONTINUED)

Field Name	Bit	Access	Description	Default
LED_TRISTATE_ENA	9	R/W	Tri-state enable for LEDs. 0: Drive LED bus output signals to high and low values as appropriate. 1: Tri-state LED output signals instead of driving them high. This allows those signals to be pulled above VDDIO using an external pull-up resistor.	0x0

1.18.4.2 PHY:PHY_GP:PHY_RCVD_CLK0_CTRL

Parent: PHY:PHY_GP

Instances: 1

TABLE 1-687: FIELDS IN PHY_RCVD_CLK0_CTRL

Field Name	Bit	Access	Description	Default
RCVD_CLK0_ENA	15	R/W	Enable RCVRD_CLK[0].	0x0
CLK_SRC_SEL0	14:11	R/W	Clock source select. 0000: PHY0 0001: PHY1 0010: PHY2 0011: PHY3 0100: PHY4 0101: PHY5 0110: PHY6 0111: PHY7 1000: PHY8 1001: PHY9 1010: PHY10 1011: PHY11 1100-1111: Reserved	0x0
CLK_FREQ_SEL0	10:8	R/W	Clock frequency select. 000: 25 MHz output clock 001: 125 MHz output clock 010: 31.25 MHz output clock 011-111: Reserved	0x0
CLK_SQUELCH_LVL0	5:4	R/W	Select clock squelch level. Note that a clock from the Cu PHY will be output on the recovered clock output in this mode when the link is down. 00: Automatically squelch clock to low when the link is not up, is unstable, is up in a mode that does not support the generation of a recovered clock (1000BASE-T master or 10BASE-T), or is up in EEE mode (100BASE-TX or 1000BASE-T slave). 01: Same as 00 except that the clock is also generated in 1000BASE-T master and 10BASE-T link-up modes. This mode also generates a recovered clock output in EEE mode during reception of LP_IDLE. 10: Squelch only when the link is not up. 11: Disable clock squelch.	0x0

TABLE 1-687: FIELDS IN PHY_RCVD_CLK0_CTRL (CONTINUED)

Field Name	Bit	Access	Description	Default
CLK_SEL_PHY0	2:0	R/W	Clock selection for specified PHY. 000: Reserved. 001: Copper PHY recovered clock 010: Copper PHY transmitter TCLK 011-111: Reserved.	0x0

1.18.4.3 PHY:PHY_GP:PHY_RCVD_CLK1_CTRL

Parent: PHY:PHY_GP

Instances: 1

TABLE 1-688: FIELDS IN PHY_RCVD_CLK1_CTRL

Field Name	Bit	Access	Description	Default
RCVD_CLK1_ENA	15	R/W	Enable RCVRD_CLK[1].	0x0
CLK_SRC_SEL1	14:11	R/W	Clock source select. 0000: PHY0 0001: PHY1 0010: PHY2 0011: PHY3 0100: PHY4 0101: PHY5 0110: PHY6 0111: PHY7 1000: PHY8 1001: PHY9 1010: PHY10 1011: PHY11 1100-1111: Reserved	0x0
CLK_FREQ_SEL1	10:8	R/W	Clock frequency select. 000: 25 MHz output clock 001: 125 MHz output clock 010: 31.25 MHz output clock 011-111: Reserved	0x0
CLK_SQUELCH_LVL1	5:4	R/W	Select clock squelch level. Note that a clock from the Cu PHY will be output on the recovered clock output in this mode when the link is down. 00: Automatically squelch clock to low when the link is not up, is unstable, is up in a mode that does not support the generation of a recovered clock (1000BASE-T master or 10BASE-T), or is up in EEE mode (100BASE-TX or 1000BASE-T slave). 01: Same as 00 except that the clock is also generated in 1000BASE-T master and 10BASE-T link-up modes. This mode also generates a recovered clock output in EEE mode during reception of LP_IDLE. 10: Squelch only when the link is not up. 11: Disable clock squelch.	0x0

TABLE 1-688: FIELDS IN PHY_RCVD_CLK1_CTRL (CONTINUED)

Field Name	Bit	Access	Description	Default
CLK_SEL_PHY1	2:0	R/W	Clock selection for specified PHY. 000: Reserved. 001: Copper PHY recovered clock 010: Copper PHY transmitter TCLK 011-111: Reserved.	0x0

1.18.4.4 PHY:PHY_GP:PHY_ENHANCED_LED_CTRL

Parent: PHY:PHY_GP

Instances: 1

TABLE 1-689: FIELDS IN PHY_ENHANCED_LED_CTRL

Field Name	Bit	Access	Description	Default
LED_PULSE_DUTY	15:8	R/W	LED pulsing duty cycle control. Programmable control for LED pulsing duty cycle when PHY_STD::PHY_LED_BEHAVIOR_CTRL.PULSING_ENA is set to 1. Valid settings are between 0 and 198. A setting of 0 corresponds to a 0.5% duty cycle and 198 corresponds to a 99.5% duty cycle. Intermediate values change the duty cycle in 0.5% increments.	0x00

1.18.4.5 PHY:PHY_GP:PHY_GLOBAL_INT_STAT

Parent: PHY:PHY_GP

Instances: 1

TABLE 1-690: FIELDS IN PHY_GLOBAL_INT_STAT

Field Name	Bit	Access	Description	Default
RESERVED	12	R/O	Must be set to its default.	0x1
PHY11_INT_SRC	11	R/O	Indicates that PHY11 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY11.	0x1
PHY10_INT_SRC	10	R/O	Indicates that PHY10 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY10.	0x1
PHY9_INT_SRC	9	R/O	Indicates that PHY9 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY9.	0x1
PHY8_INT_SRC	8	R/O	Indicates that PHY8 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY8.	0x1
PHY7_INT_SRC	7	R/O	Indicates that PHY7 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY7.	0x1

TABLE 1-690: FIELDS IN PHY_GLOBAL_INT_STAT (CONTINUED)

Field Name	Bit	Access	Description	Default
PHY6_INT_SRC	6	R/O	Indicates that PHY6 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY6.	0x1
PHY5_INT_SRC	5	R/O	Indicates that PHY5 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY5.	0x1
PHY4_INT_SRC	4	R/O	Indicates that PHY4 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY4.	0x1
PHY3_INT_SRC	3	R/O	Indicates that PHY3 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY3.	0x1
PHY2_INT_SRC	2	R/O	Indicates that PHY2 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY2.	0x1
PHY1_INT_SRC	1	R/O	Indicates that PHY1 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY1.	0x1
PHY0_INT_SRC	0	R/O	Indicates that PHY0 is the source of the interrupt when this bit is cleared. This bit is set high when reading register PHY_INT_STAT in PHY0.	0x1

1.18.5 PHY:PHY_EEE

Parent: PHY

Instances: 1

Access to these registers is through the IEEE standard registers MMD_ACCESS_CFG and MMD_ADDR_DATA.

TABLE 1-691: REGISTERS IN PHY_EEE

Register Name	Offset within Register Group	Instances and Address Spacing	Description	Details
PHY_PCS_STATUS1	0x00000000	1	PCS Status 1 (Address 3.1)	Page 313
PHY_EEE_CAPABILITIES	0x00000004	1	EEE Capabilities (Address 3.20)	Page 314
PHY_EEE_WAKE_ERR_CNT	0x00000008	1	EEE Wake Error Counter (Address 3.22)	Page 314
PHY_EEE_ADVERTISEMENT	0x0000000C	1	EEE Advertisement (Address 7.60)	Page 315
PHY_EEE_LP_ADVERTISE-MENT	0x00000010	1	EEE Link Partner Advertise-ment (Address 7.61)	Page 315

1.18.5.1 PHY:PHY_EEE:PHY_PCS_STATUS1

Parent: PHY:PHY_EEE

Instances: 1

Status of the EEE operation from the PCS for the link that is currently active.

TABLE 1-692: FIELDS IN PHY_PCS_STATUS1

Field Name	Bit	Access	Description	Default
TX_LPI_RECV	11	R/O	0: LPI not received 1: Tx PCS has received LPI	0x0
RX_LPI_RECV	10	R/O	1: Rx PCS has received LPI 0: LPI not received	0x0
TX_LPI_INDICATION	9	R/O	1: Tx PCS is currently receiving LPI 0: PCS is not currently receiving LPI	0x0
RX_LPI_INDICATION	8	R/O	1: Rx PCS is currently receiving LPI 0: PCS is not currently receiving LPI	0x0
PCS_RECV_LINK_STAT	2	R/O	1: PCS receive link up 0: PCS receive link down	0x0

1.18.5.2 PHY:PHY_EEE:PHY_EEE_CAPABILITIES

Parent: PHY:PHY_EEE

Instances: 1

Indicate the capability of the PCS to support EEE functions for each PHY type.

TABLE 1-693: FIELDS IN PHY_EEE_CAPABILITIES

Field Name	Bit	Access	Description	Default
EEE_1000BT	2	R/O	Set if EEE is supported for 1000BASE-T. 1: EEE is supported for 1000BASE-T 0: EEE is not supported for 1000BASE-T	0x0
EEE_100BTX	1	R/O	Set if EEE is supported for 100BASE-TX. 1: EEE is supported for 100BASE-TX 0: EEE is not supported for 100BASE-TX	0x0

1.18.5.3 PHY:PHY_EEE:PHY_EEE_WAKE_ERR_CNT

Parent: PHY:PHY_EEE

Instances: 1

This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and can occur during a refresh or a wakeup as defined by the PHY. This 16-bit counter is reset to all zeros when the EEE wake error counter is read or when the PHY undergoes hardware or software reset.

TABLE 1-694: FIELDS IN PHY_EEE_WAKE_ERR_CNT

Field Name	Bit	Access	Description	Default
EEE_WAKE_ERR_CNT	15:0	R/O	Count of wake time faults for a PHY.	0x0000

1.18.5.4 PHY:PHY_EEE:PHY_EEE_ADVERTISEMENT

Parent: PHY:PHY_EEE

Instances: 1

Defines the EEE advertisement that is sent in the unformatted next page following a EEE technology message code.

TABLE 1-695: FIELDS IN PHY_EEE_ADVERTISEMENT

Field Name	Bit	Access	Description	Default
EEE_1000BT_ADV	2	R/W	Set if EEE is supported for 1000BASE-T. 1: Advertise that the 1000BASE-T has EEE capability. 0: Do not advertise that the 1000BASE-T has EEE capability.	0x0
EEE_100BTX_ADV	1	R/W	Set if EEE is supported for 100BASE-TX. 1: Advertise that the 100BASE-TX has EEE capability 0: Do not advertise that the 100BASE-TX has EEE capability	0x0

1.18.5.5 PHY:PHY_EEE:PHY_EEE_LP_ADVERTISEMENT

Parent: PHY:PHY_EEE

Instances: 1

All the bits in the EEE LP Advertisement register are read only. A write to the EEE LP advertisement register has no effect. When the AN process has been completed, this register will reflect the contents of the link partner's EEE advertisement register.

TABLE 1-696: FIELDS IN PHY_EEE_LP_ADVERTISEMENT

Field Name	Bit	Access	Description	Default
EEE_1000BT_LP_ADV	2	R/O	Set if EEE is supported for 1000BASE-T by link partner. 1: Link partner is advertising EEE capability for 1000BASE-T 0: Link partner is not advertising EEE capability for 1000BASE-T	0x0
EEE_100BTX_LP_ADV	1	R/O	Set if EEE is supported for 100BASE-TX by link partner. 1: Link partner is advertising EEE capability for 100BASE-TX 0: Link partner is not advertising EEE capability for 100BASE-TX	0x0

APPENDIX A: REVISION HISTORY

This section describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

A.1 Revision A - 11/2022

In this revision, the document was migrated to Microchip template.

A.2 Revision 4.2 - 03/2019

The following is a summary of the changes in revision 4.2 of this document:

- VeriPHY descriptions were updated. For functional details of the VeriPHY suite and operating instructions, see the *ENT-AN0125 PHY, Integrated PHY-Switch VeriPHY - Cable Diagnostics Application Note*.

A.3 Revision 4.1

In revision 4.1 of this document, the register list was updated. For more information, see Section 1.0, Registers.

A.4 Revision 4.0

The following is a summary of the changes in revision 4.0 of this document:

- The Fields in PORT_MISC table was updated. For more information, see, Table 1-80.
- The REV_ID was updated. For more information, see Table 1-121

A.5 Revision 2.0

Revision 2.0 was the first publication of this document.

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