# VSC7514

# User Guide

# VSC7514EV Hardware Manual

08 2016

Microsemi
Power Matters.™

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# Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 01-01

Revision 01-01 changed VCore-III operating frequency to 500MHz, DDR3 operating frequency to 312.5MHz, and updated chapter 8.5.

## 1.2 01-00

Revision 01-00 was the first production-level publication of this document.

## 1.3 00-01

Revision 00-01 was the first publication of this document, for internal review.

# Contents

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# 2 Introduction

This hardware manual describes the design of the VSC7514EV reference board, demonstrating the VSC7514 Ocelot Ethernet switch device.

## 2.1 Audience

The audience for this document is primarily hardware and software engineers that want to get an overview of designing products based on the VSC7514 device.

## 2.2 References

### 2.2.1 Microsemi documents

- VSC7514 product datasheet, http://www.microsemi.com/products/ethernet-solutions/ethernet-switches/vsc7514-10-port-layer-2-layer-3-gigabit-ethernet-switch
- Serial GPIO user's guide, http://ethernet.microsemi.com/products/download.php?fid=4865&number=vsc7428
- VSC7514EV reference design hardware collateral, http://www.microsemi.com/products/ethernet-solutions/ethernet-switches/vsc7514-10-port-layer-2-layer-3-gigabit-ethernet-switch

### 2.2.2 IEEE standards

- IEEE802.1D, Media Access Control Bridges
- IEEE802.1Q, Virtual Bridged Local Area Networks
- IEEE802.3, CSMA/CD Access Method and Physical Layer Specification
- IEEE1588-2008, Precision Clock Synchronization Protocol

### 2.2.3 Optical module standards

- SFP MSA, ftp://ftp.seagate.com/sff/INF-8074.PDF

## 2.3 Terms and abbreviations

The following table lists any special terms and abbreviations used in this document.

**Table 1 Terms and abbreviations**

| Term | Description |
|---|---|
| AMS | Automatic Media-Sense |
| EMI | Electromagnetic Interference, emissions |
| JTAG | Joint Test Access Group, IEEE1149 |
| LVDS | Low Voltage Differential Signaling |
| LVTTL | Low Voltage TTL |
| NPI | Node Processor Interface |

| Term | Description |
|---|---|
| PCS | Physical Coding Sublayer |
| PHY | Physical layer device |
| PTP | Precision Time Protocol, IEEE1588 |
| SFP | Small Form-factor Pluggable transceiver |
| SI | Serial Interface, SPI |
| Sync-E | Synchronous Ethernet, ITU-T G.8262/Y.1362 |

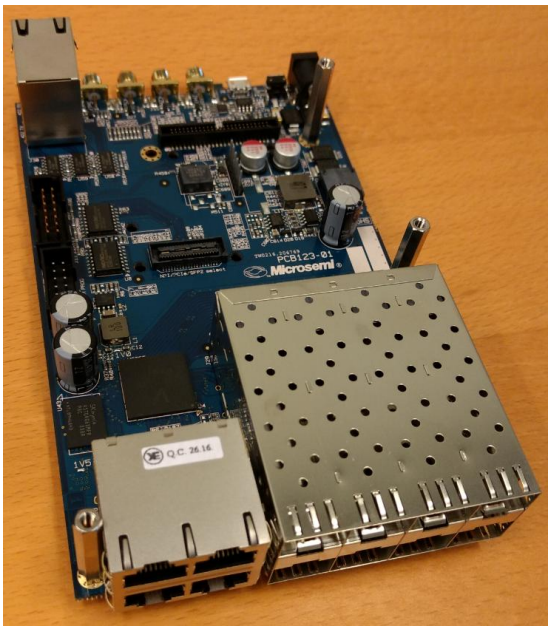
# 3 Features

## 3.1 VSC7514EV

The VSC7514EV reference board's use case is as a managed switch, exposing the main interfaces and features of VSC7514:

- Four 10/100/1000BASE-T (RJ45) Ethernet copper ports (PHYs integrated with VSC7514)
- Eight 100M/1Gbit/s Ethernet SFP ports (connected to VSC7514 through SERDES) – two of the SFP ports are dual-media ports tied to two of the copper ports – three of the SFP ports are also 2.5Gbit/s capable
- One optional additional 10/100/1000BASE-T (RJ45) Ethernet port (VSC8221 PHY connected to VSC7514 through SGMII)
- By default VSC7514 is managed by the embedded MIPS CPU system with on-board DDR3, NOR and NAND Flash devices…
- … but optionally an external master CPU system can connect to the VSC7514 slave through PCIe, SPI or the NPI port (using VRAP for inband management)
- Four SMAs, and an RS422 interface, for PTP and Sync-E applications …
- … and support for a range of Microsemi Sync-E modules through the Sync-E feature connector
- Serial port for accessing the command line interface (CLI) software debugger, implemented through an on-board serial-to-USB converter (so connecting to a PC through a USB cable)
- Reset button with one-shot reset (so button state can be read by firmware after board reset, e.g. for a "reset to factory defaults" function)
- System status LED, port status LEDs
- 12Vdc power in socket

**Figure 1 VSC7514EV**



## 3.2 CPU system

### 3.2.1 Embedded VCore-III CPU system

- Embedded MIPS 32-bit processor operating at 500MHz.
- External memories include 32MBytes SPI boot NOR Flash, 256MBytes SPI NAND Flash, 512MBytes DDR3 SDRAM (x16)
- Some GPIO, e.g. for connecting to the 8 SFP ports of VSC7514EV and for LED control are implemented through the serial GPIO engine (using inexpensive 74-series external shift registers)

### 3.2.2 External CPU system options

Instead of using the embedded VCore-III CPU system booting from on-board SPI Flash, an external CPU system can connect to and control the VSC7514 configured as a slave device switch through either:

- Node Processor Interface (NPI) port (VSC7514 NPI interface is SERDES, available to external CPU board as 1000Base-T/RJ45 through a VSC8221-based PHY add-on module connected to the NPI/PCIe feature connector)
- Serial Interface (SI, SPI)
- PCIe (VSC7514 PCIe port is exposed in the NPI/PCIe feature connector and available throuag an add-on module as a cabled connection to an external CPU module)

### 3.2.3 Management and user I/O

- NPI port (extra LAN port) e.g. for accessing local management via 10/100/1000BASE-T Ethernet – the NPI port resides on a small add-on module
- Serial port converted to USB on-board, for accessing CLI debugger and local management
- Reset button
- System status LED (tri-color green/yellow/red) and port status LED (tri-color green/yellow/red) per network port (e.g. for link and activity information), all LEDs controlled through the serial LED interface (using 74-series external shift registers)

## 3.3 Module slots and feature connectors

### 3.3.1 SFP module slots

VS7514EV has eight SFP slots for 100M/1G/2.5G SFP transceivers. The SFP slots connect to VSC7514 through SERDES.

- SFP1 and SFP2 connect directly to VSC7514 SERDES ports S0 and S1 (100M/1G capable). Together with VSC7514 1000Base-T ports P0 and P1 they provide two dual-media ports.
- SFP3, SFP4 and SFP5 connect directly to VSC7514 SERDES ports S2, S3 and S4 (100M/1G capable).
- SFP6 connects to either VSC7514 SERDES port S5 (100M/1G capable) or S8 (100M/1G/2.5G capable) through the NPI/PCIe feature connector:
    - When an NPI PHY module is mounted on this feature connector, S5 connects to a VSC8221 NPI PHY on the module, and the module feeds S8 back to the main VSC7514EV reference board for connection to SFP6 (100M/1G/2.5G capable in this case).

- When a PCIe module is mounted on this feature connector, S8 connects to a connector on the module for cabled PCIe, and the module feeds S5 back to the main VSC7514EV reference board for connection to SFP6 (100M/1G capable in this case).

- SFP7 and SFP8 connect directly to VSC7514 SERDES ports S6 and S7 (100M/1G/2.5G capable).

### 3.3.2 SI (serial interface) feature connector

Interface for an external CPU master to access a VSC7514 slave's SI (SPI) interface.

### 3.3.3 NPI/PCIe feature connector

Interface for an external CPU master to access a VSC7514 slave's PCIe interface on VSC7514 SERDES S8, either connected through a cable using a small adaptor board exposing the VSC7514 PCIe slave interface in a standard PCIe cable connector or e.g. through an add-on CPU module connecting directly to the VSC7514 PCIe slave interface.

This feature connector can also be used for an add-on module containing an NPI PHY interface, connecting to VSC7514 SERDES S5.

Note that the add-on module connecting to the NPI/PCIe feature connector is responsible for feeding the VSC7514 SERDES port (S5 or S8) not used for NPI/PCIe duties on the module back to the main VSC7514EV reference board for connection to the mainboard's SFP6. If no module is added on the NPI/PCIe feature connector, the mainboard's SFP6 is thus left unconnected.

## 3.4 Timing and synchronization

### 3.4.1 Sync-E

VSC7514EV supports Sync-E through an add-on board. Presently two such add-on boards exist, more to come.

The Sync-E add-on board delivers a reference clock to the VSC7514. The clock source can be either a free-running oscillator or a clock recovered from a network port and supplied to the Sync-E add-on board by the VSC7514. The Sync-E device on the add-on board prioritizes and selects the clock source under software control and attenuates jitter before presenting the resulting clock to the switch reference board.

Sync-E is managed as part of the general switch management software.

### 3.4.2 PTP/IEEE1588v2

PTP interfacing is available through network ports (with accurate timestamping available in the VSC7514 switch supporting e.g. LTE-advanced), through ITU-T G.8275 compliant RS422 1 PPS + ToD input and output ports, and through SMAs.

VSC7514EV can be configured as boundary clock, transparent clock, PTP master and PTP slave. It supports both one-step and two–step operations, as well as PTP over MPLS-TP and IP/MPLS.

The free-running OCXO providing base clock to the VSC7514 offers Stratum-3 holdover.

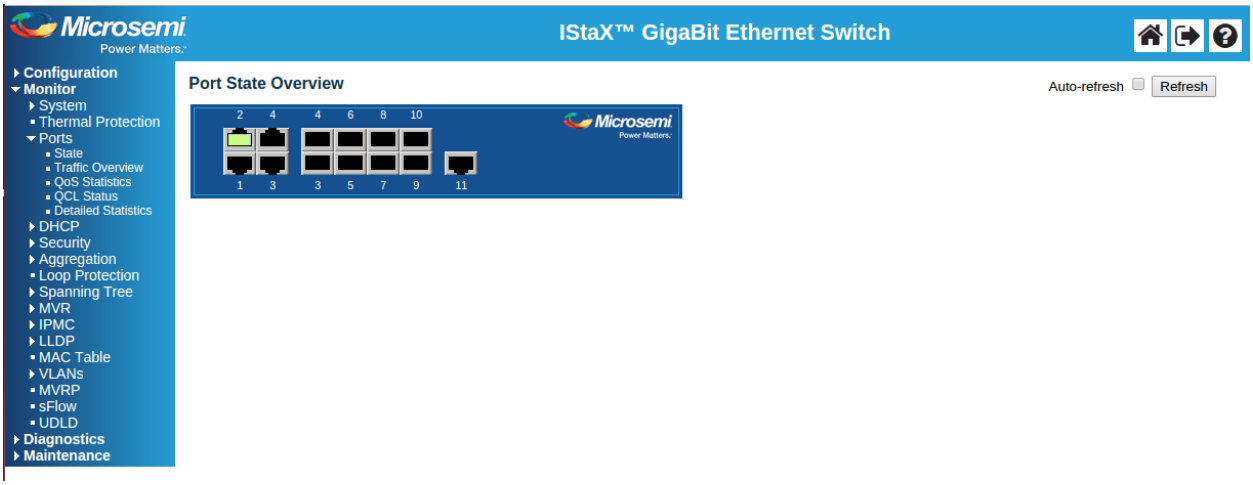
# 4 Quick start guide

## 4.1 Management software

The VSC7514EV reference board can be managed either locally through a USB/RS232 serial port using a command line interface (CLI) or remotely using a browser-based graphical user interface (web GUI).

### 4.1.1 Web GUI

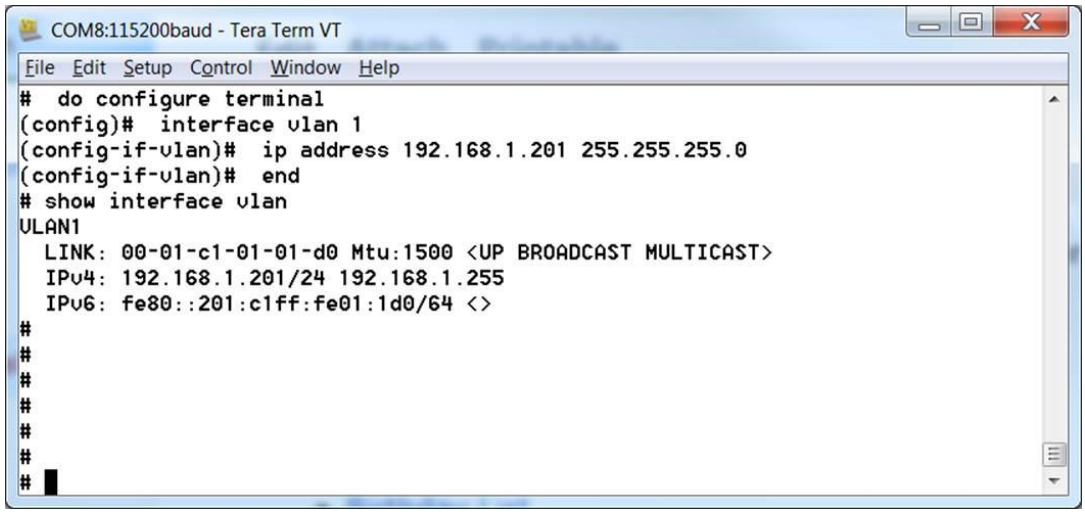
**Figure 2 Web GUI screenshot**




The web GUI is available from e.g. a laptop connected to a network port. Ensure that laptop and switch are on the same subnet, start the laptop's browser, point the browser at the switch's IP address, enter login credentials (default username "admin" (no quotes), default password blank (i.e. empty)), and something similar to Figure 2 will appear. Help screens are available through the question mark button top right.

### 4.1.2 CLI debugger

**Figure 3 CLI screenshot**




The CLI debugger is available through the serial port's µUSB connector. The reference board can be connected to a PC USB port using e.g. the cable supplied with the system and will show up there as a serial port. Set the serial port to 115200 baud, 8 data bits, no parity, 1 stop bit, no flow control. As for the web GUI, the default username is "admin" (no quotes) and the default password is blank (i.e. empty). Help screens are available through the "?" or "help" commands. One important use of the CLI is to determine the IP address of a switch through the "show interface vlan" command - this is the IP address the web GUI is available through. An example of the entering of the "show interface vlan" command is available in Figure 3.

## 4.2 Tour-de-board

**Figure 4 Annotated photo of VSC7514**

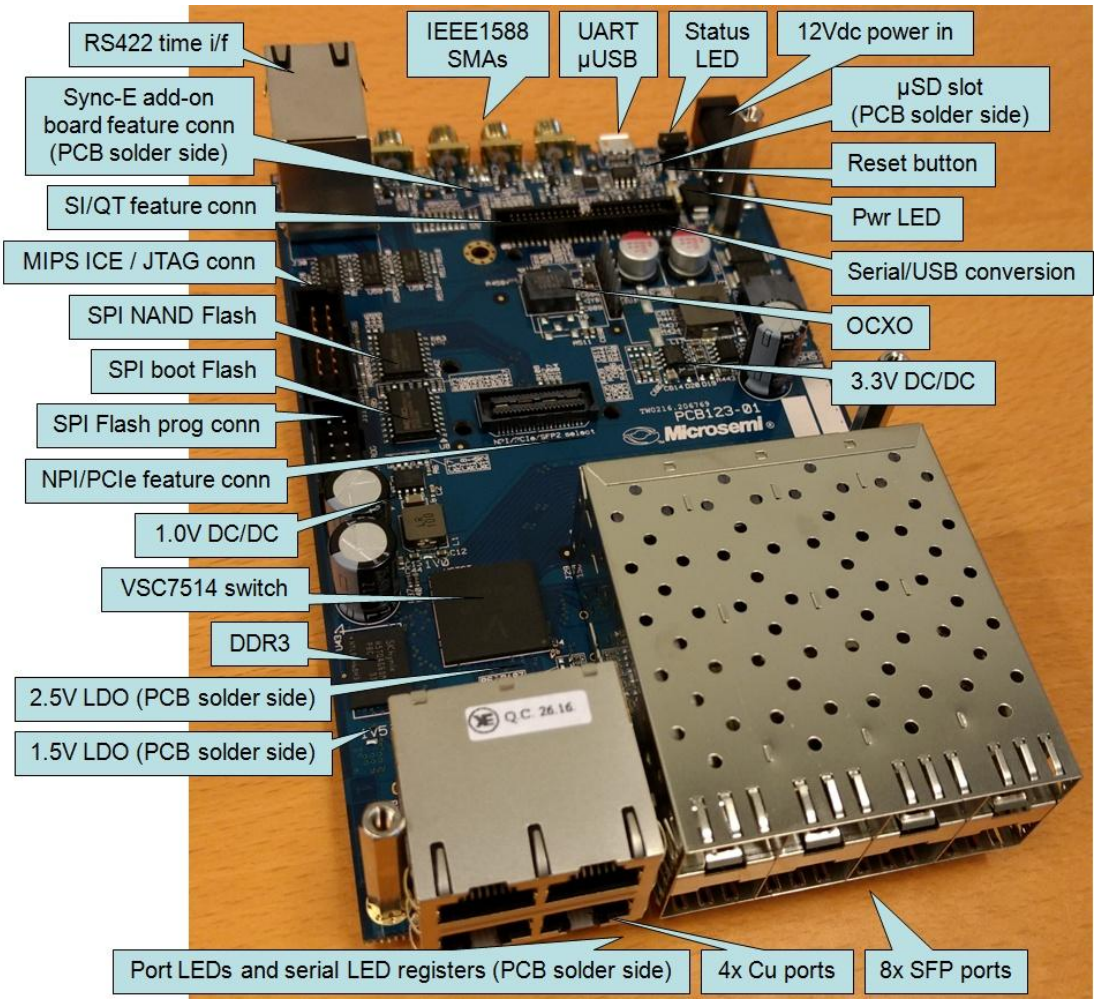



**Figure 5 Front bracket layout for VSC7514EV**

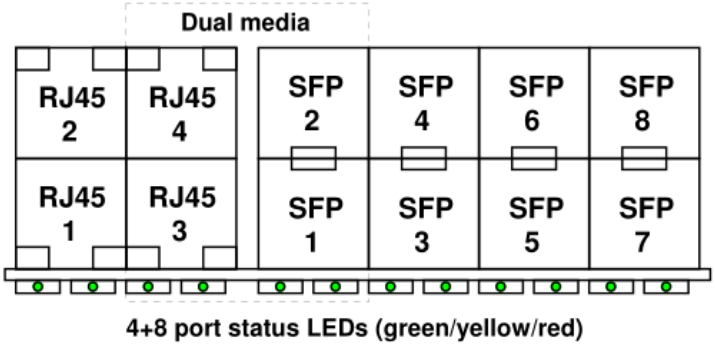
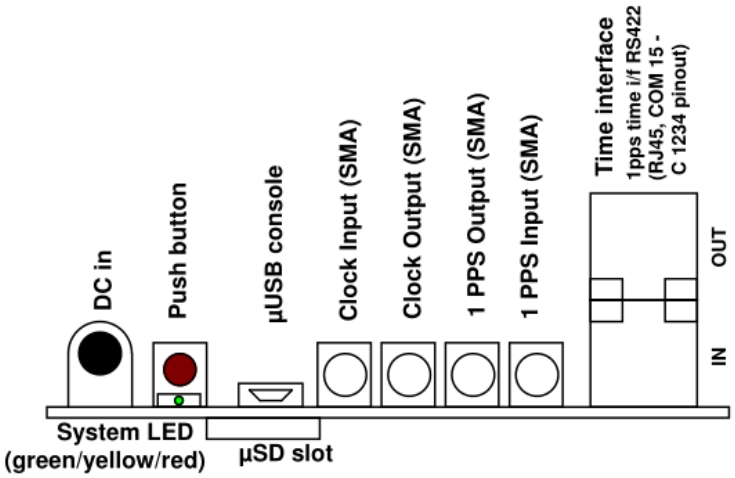


**Figure 6 Rear bracket layout for VSC7514EV**




## 4.3 Connectors

### 4.3.1 Power input

12Vdc, 2.5 mm center pin power jack.

### 4.3.2 MIPS ICE / JTAG

Standard MIPS ICE connector, for e.g. a Mentor MAJIC JTAG probe with CA-MIPS14 cable or the more recent Mentor Sourcery probe.

Note that VSC7514 is strapped for connection to an ICE (its JTAG_ICE_nEn pin is pulled low) – if the ICE connector is to be used for boundary scan JTAG then the JTAG_ICE_nEn signal must be strapped high e.g. through the ICE/JTAG connector.

### 4.3.3 SPI boot Flash programming

The SPI boot Flash can be programmed from an external programmer through a pin header.

### 4.3.4 NPI/PCIe feature connector

The NPI/PCIe feature connector is host to either the NPI PHY module or the PCIe module.

### 4.3.5 SI/QT feature connector

The SI (serial interface, SPI) bus of the VSC7514 is available in a 0.05” pitch pin header.

This feature connector has dual duty as connection point for the Microsemi QuickTest manufacturing test module, allowing for measurements of power supplies, resets etc.

### 4.3.6 4x2 SFP ports

Connecting to VSC7514 SERDES ports.

### 4.3.7 2x2 RJ45 ports

Connecting to VSC7514 PHY ports.

### 4.3.8 µUSB (serial) port

The reference board can be connected directly to a PC USB port using the cable supplied with the system (or a standard USB-to-µUSB cable as used e.g. with many smartphones) to access the command line interface (CLI) debugger.

The reference board contains an on-board serial-to-USB converter, when connected to a PC the PC will detect this USB device and allow setup of e.g. baud rate - from there on the port will behave like a PC serial port e.g. including a COMx port number. On the PC, set the new COM port for 115200 baud, 8 data bits, no parity, 1 stop bit, no flow control, and point the terminal program of choice to the new COM port.

USB driver software (Windows, Mac, Linux) for the FTDI FT234XD serial-to-USB converter is available at http://www.ftdichip.com/Products/ICs/FT234XD.html.

### 4.3.9 RS422 serial PTP port

The reference board has a serial port available for PTP connections. It terminates in two RJ45 connectors, one “input” and one “output”.

In addition to the RS422 serial port RX/TX signals (for exchanging PTP info packets), the connectors include 1pps PTP input (in the “input” connector), output (in the “output” connector) and loopback (output from “input” (PTP slave) connector, input to “output” (PTP master) connector) signals.

### 4.3.10 SMA connectors

The reference board has four SMA connectors on the rear of the device of which two are used as inputs and two as outputs.

One of the input connectors is available for 1 PPS into VSC7514 and the other for various frequencies e.g. 1.544, 2.048, 10 MHz into the optional Sync-E add-on module. Note: The SMA inputs are LVTTL and are 3V3 tolerant. They are not e.g. 5V tolerant.

One of the two output connectors is used for 1 PPS from VSC7514 and the other for various frequencies e.g. 1.544, 2.048 and 10 MHz from the optional Sync-E add-on module.

### 4.3.11 Sync-E feature connector

The reference board has a feature connector for an optional Sync-E add-on board.

## 4.4 Buttons

### 4.4.1 Reset

A reset button is available on the front of the reference board. When pressed it sinks an input of the voltage supervisor, creating a hard board reset. It functions as a one-shot, so pressing it causes a reset and it can afterwards be sampled by firmware to determine if it is still pressed during boot, e.g. causing a “reset to factory defaults”.

## 4.5 LEDs

### 4.5.1 Power LED

A power LED is available, powered by the local 3.3V DC/DC converter (which is also the supply voltage monitored by the reset circuitry).

### 4.5.2 System status LED

A tri-color (individual green/red controls, both on equals yellow) LED is available on the reference board front. It is controlled by switch firmware through the VSC7514 serial LED engine. It is yellow during reset.

### 4.5.3 Port status LEDs

The reference board has 4 (“2x2 RJ45”) + 8 (“4x2 SFP”) tri-color (individual green/red controls, both on equals yellow) port status LEDs available on the front.

The port status LEDs are controlled by firmware through the VSC7514 serial LED engine.

# 5 Hardware description

## 5.1 Block diagram

Figure 7 depicts the block diagram of the VSC7514EV reference board.

The design is based on the VSC7514 switch and exposes most interfaces of this device, e.g. four 1000Base-T ports, eight SFP module slots (two of these dual-media), and Sync-E and PTP interfaces.

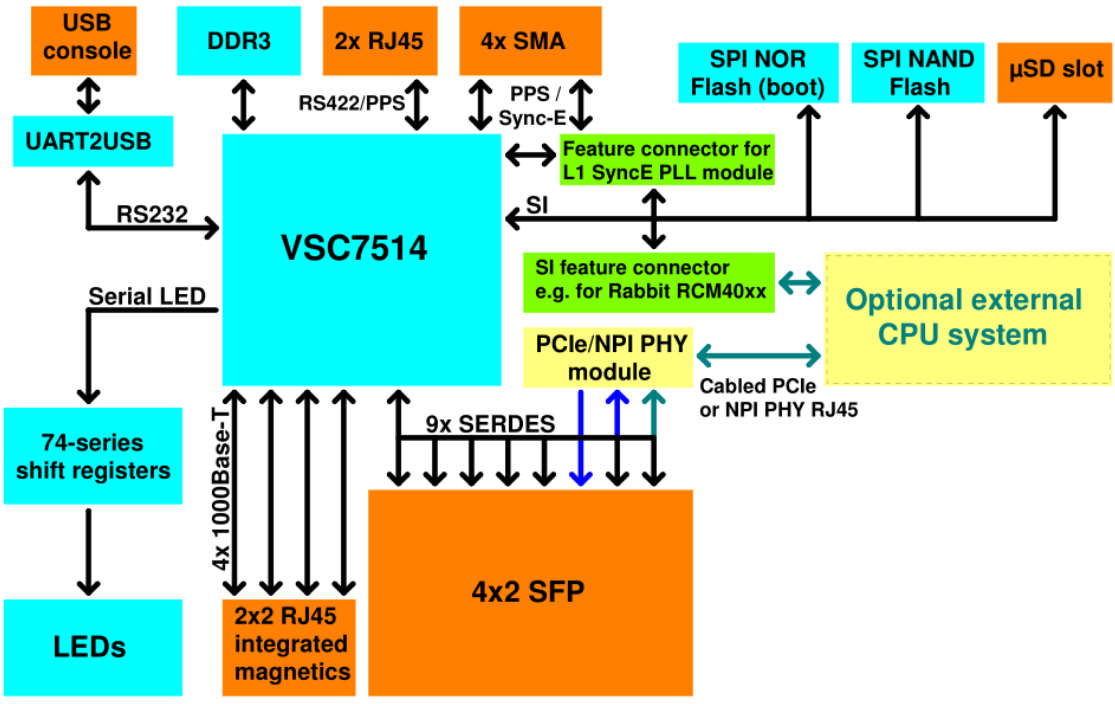
VSC7514 includes the VCore-III MIPS-based CPU, which is connected to external Flash (SPI NOR Flash for booting application firmware, SPI NAND Flash for bulk storage (not bootable)) and DDR3 SDRAM memories. Optionally, an external CPU system can be connected through the NPI port or through the SI or PCIe interfaces.

VSC7514EV features four SMA connectors which can be used for IEEE1588 and Sync-E applications, and a 1PPS in/out time interface complying with ITU G.703. A Sync-E feature connector allows for adding a L1 Sync-E PLL module.

The VSC7514 serial GPIO/LED engine interfaces to external 74-series shift registers controlling system and port status LEDs.

The VSC7514 console port is exposed in a µUSB connector through a serial-to-USB converter.

**Figure 7 System functional block diagram for VSC7514EV**




## 5.2 CPU system

VSC7514 has an embedded VCore-III MIPS-based CPU operating at 500MHz. Furthermore it can act as a slave device on an external CPU's serial or PCIe bus.

The internal VCore-III CPU is by default configured as master, booting from SPI Flash. The following sections describing the CPU system assume a master VSC7514 except where otherwise stated.

A VSC7514 can optionally be configured as slave, either using on-board strapping resistors or through the SI or PCIe feature connectors, for connection to an external CPU system through the SI and PCIe feature connectors.

### 5.2.1 External memories

#### DDR3 SDRAM

The VSC7514 DDR3 SDRAM interface is 16 bits wide and typically operates at a clock rate of 312.5MHz, requiring a RAM device of speed grade 800Mtransfers/sec (400MHz clock) or better.

As default, the reference boards are equipped with 512MBytes of DDR3 SDRAM. Other densities can easily be substituted, e.g. 128MBytes, depending on the application.

#### SPI bulk NAND Flash

As default, the reference boards are equipped with 256MBytes of NAND SPI Flash. Other densities can easily be substituted, depending on the application. Note that the VCore-III CPU system can not boot from NAND Flash, so some amount of NOR Flash is required for boot-strapping when VCore-III is configured as a master.

#### SPI boot NOR Flash

As default, the reference boards are equipped with 32MBytes of NOR SPI boot Flash. Other densities can easily be substituted, e.g. 2MBytes, depending on the application.

#### SPI boot NOR Flash programming

The SPI boot Flash can be programmed from an external programmer through a 2x5 pin 0.1” pitch header. This includes a reset signal through which the programmer can keep VSC7514 in reset, in which state it will release control of its SI_DO output so that the programmer can take over while programming the SPI Flash. With the introduction of SPI Flash devices with a density above 128Mbit/16MBytes also comes a need for the SPI Flash to have a reset input – this SPI Flash reset input is exposed in the programming header allowing the programmer to (1) assert reset to the system to output disable VSC7514 SI signals and (2) deassert reset to the Flash to allow programming it.

**Table 2 SPI boot Flash programming connector**

| Signal | Direction | Pin | Pin | Direction | Signal |
|---|---|---|---|---|---|
| SI_CLK - SPI clock signal | Switch<- Probe | 1 | 2 | | Gnd |
| SI_DI - SPI data from SPI Flash | Switch-> Probe | 3 | 4 | | nRESET_FLASH – reset signal from probe to Flash, keep high during Flash programming |
| n/c | | 5 | 6 | Probe<- Switch | 3V3 |
| SI_nCS0 - SPI chipselect signal | Switch<- Probe | 7 | 8 | Probe-> Switch | nSYSRESETin - reset signal from probe to switch, keep low during Flash programming |

| Signal | Direction | Pin | Pin | Direction | Signal |
|---|---|---|---|---|---|
| SI_DO - SPI data to SPI Flash | Switch<- Probe | 9 | 10 | | Gnd |

### 5.2.2 NPI/PCIe

The slave PCIe interface of the VSC7514 is exposed in a Samtec QSE-020 NPI/PCIe feature connector. A small adaptor board can expose the PCIe interface in a standard PCIe cable connector, or “shim” adaptor boards can expose the PCIe interface physically compatible to e.g. existing Qseven or COMexpress CPU modules, or add-on CPU modules can be designed for direct connection to this feature connector.

The VCore-III mode configuration signals are included in the NPI/PCIe feature connector, allowing add-on modules to strap VCore-III as applicable, e.g. as PCIe slave. The PCIe module supplied with the system straps VSC7514 for PCIe slave operation, so that it can be used “plug and play” with an external PCIe master.

The NPI/PCIe feature connector includes four pins of 12V, allowing an external CPU module to pull up to 4A of 12V from the reference board host.

The NPI/PCIe feature connector is also used to host the NPI PHY module. Thus it includes both the VSC7514 S5 port used for NPI duties and the VSC7514 S8 port used for PCIe duties. When used for PCIe, the module connecting to the NPI/PCIe feature connector must feed the VSC7514 S5 port back to the main board for connection to the front SFP6. When used for NPI, the module connecting to the NPI/PCIe feature connector must feed the VSC7514 S8 port back to the main board for connection to the front SFP6.

The NPI/PCIe feature connector signal pins are detailed in Table 3.

**Table 3 NPI/PCIe feature connector signal description**

| Description | Pin | Pin | Description |
|---|---|---|---|
| PCIe_R_N, extCPU->switch S8 (or fed back to reference board SFP6) | 1 | 2 | 12V |
| PCIe_R_P, extCPU->switch S8 (or fed back to reference board SFP6) | 3 | 4 | 12V |
| 3V3 | 5 | 6 | nSYSRESET, reference board reset signal |
| PCIe SB_RTN, grounded by reference board host | 7 | 8 | PCIe CPRSNT#, grounded by reference board host |
| PCIe_CLK_N, 50R terminated by reference board host | 9 | 10 | 12V |
| PCIe_CLK_P, 50R terminated by reference board host | 11 | 12 | 12V |
| MII_MDIO, management bus interface towards NPI PHY | 13 | 14 | PCIe CPWRON, n/c on reference board host |
| nSYSRESETin, allows extCPU to reset reference board host | 15 | 16 | PCIe_T_N, switch S8 ->extCPU (or fed back to reference board SFP6) |
| MII_MDC, management bus interface towards NPI PHY | 17 | 18 | PCIe_T_P, switch S8 ->extCPU (or fed back to reference board SFP6) |
| SI_DO | 19 | 20 | VCORE_CFG3 |
| SI_DI | 21 | 22 | VCORE_CFG2 |

| Description | Pin | Pin | Description |
|---|---|---|---|
| SI_CLK | 23 | 24 | VCORE_CFG1 |
| SI_nCS0 | 25 | 26 | VCORE_CFG0 |
| RS232_TXD | 27 | 28 | nINT_PHY, interrupt signal towards reference board, open collector |
| RS232_RXD | 29 | 30 | SPI_nCSflash |
| GND | 31 | 32 | n/c |
| SFP6_T_P, reference board SFP6 transmit data (towards SFP) | 33 | 34 | NPI_T_P, switch S5 ->NPI PHY (or fed back to reference board SFP6) |
| SFP6_T_N, reference board SFP6 transmit data (towards SFP) | 35 | 36 | NPI_T_N, switch S5 ->NPI PHY (or fed back to reference board SFP6) |
| SFP6_R_N, reference board SFP6 receive data (towards VSC7514) | 37 | 38 | NPI_R_N, NPI PHY->switch (or fed back to reference board SFP6) |
| SFP6_R_P, reference board SFP6 receive data (towards VSC7514) | 39 | 40 | NPI_R_P, NPI PHY->switch (or fed back to reference board SFP6) |

### 5.2.3 SI

The SI (serial interface, SPI) bus of the VSC7514 is used for both devices on-board the reference boards and devices located on optional modules or add-on boards. It consists of the usual SPI clock, data out and data in signals, and a dedicated chipselect per device.

#### SI chipselects

The VSC7514 SI bus is connected to several SPI slaves with individual chipselects. Only SI_nCS0 is a dedicated pin on VSC7514, others are available as alternate functions on VSC7514 GPIO pins.

- SI_nCS0 controls the SPI boot NOR Flash. Its connection is through a series resistor so that an external CPU master connected through the SI feature connector can connect to either VSC7514 (as slave) or the SPI boot Flash at will.
- SI_nCS1/GPIO8 controls the SPI bus of the SPI NAND Flash.
- SI_nCS2/GPIO9 controls the SPI bus of the Sync-E module.

#### SI feature connector

The SI feature connector is a 2x25 pin 0.05” pitch boxed pin header. It can be used to connect to the VSC7514 SI bus.

The SI feature connector is also used for the QuickTest board diagnostics add-on module, monitoring a selection of signals useful in mainboard bring-up and manufacturing testing. The QuickTest related signals are simply labeled as such in Table 4.

**Table 4 SI feature connector signal description**

| Description | Pin | Pin | Description |
|---|---|---|---|
| 3V3 | 1 | 2 | GND |
| QuickTest | 3 | 4 | QuickTest |
| QuickTest | 5 | 6 | QuickTest |
| GND | 7 | 8 | GND |
| QuickTest | 9 | 10 | QuickTest |

| Description | Pin | Pin | Description |
|---|---|---|---|
| QuickTest | 11 | 12 | QuickTest |
| QuickTest | 13 | 14 | QuickTest |
| QuickTest | 15 | 16 | QuickTest |
| QuickTest | 17 | 18 | QuickTest |
| QuickTest | 19 | 20 | QuickTest |
| QuickTest | 21 | 22 | QuickTest |
| QuickTest | 23 | 24 | RS232_RXD |
| RS232_TXD | 25 | 26 | SI_DI, input to VSC7514 |
| SI_DO, output from VSC7514 | 27 | 28 | nMODULE_INT |
| QuickTest | 29 | 30 | QuickTest |
| SI_CLK | 31 | 32 | QuickTest |
| QuickTest | 33 | 34 | nSYSRESET_IN |
| SI_nCS0 | 35 | 36 | QuickTest |
| QuickTest | 37 | 38 | QuickTest |
| QuickTest | 39 | 40 | VCORE_CFG0 |
| VCORE_CFG1 | 41 | 42 | VCORE_CFG2 |
| VCORE_CFG3 | 43 | 44 | QuickTest |
| I2C_SCL | 45 | 46 | QuickTest |
| I2C_SDA | 47 | 48 | SPI_nCSflash |
| QuickTest | 49 | 50 | GND |

## 5.3 Network ports

- Four 10/100/1000BASE-T RJ45 front ports are connected to VSC7514 1000Base-T ports.
- Eight 100M/1000M/2.5G SFP front ports are connected to VSC7514 SERDES ports. SFP I2C is available through an external multiplexer controlled through MUX_SEL[2:0] signals. Other SFP out-of-band control signals are connected through serial GPIO as detailed in section 5.5.
- One 10/100/1000BASE-T RJ45 port is available when using the NPI PHY module.

**Table 5 VSC7514EV physical port summary**

| VSC7514EV board physical port | VSC7514 physical pins | VSC7514 port number / device | Additional information |
|---|---|---|---|
| RJ45 #1 | P2 | 2 | "Internal" MIIM address DEVCPU_GCB:PHY:PHY_CFG.PHY_ADDR+2 |
| RJ45 #2 | P3 | 3 | "Internal" MIIM address DEVCPU_GCB:PHY:PHY_CFG.PHY_ADDR+3 |
| RJ45 #3 | P0 | 0 | "Internal" MIIM address DEVCPU_GCB:PHY:PHY_CFG.PHY_ADDR+0 |
| RJ45 #4 | P1 | 1 | "Internal" MIIM address DEVCPU_GCB:PHY:PHY_CFG.PHY_ADDR+1 |

| VSC7514EV board physical port | VSC7514 physical pins | VSC7514 port number / device | Additional information |
|---|---|---|---|
| SFP #1 | S0 | 0 | Dual-media with RJ45 #3,<br>100M/1G capable,<br>I2C through MUX_SEL[2:0]=000 |
| SFP #2 | S1 | 1 | Dual-media with RJ45 #4,<br>100M/1G capable,<br>I2C through MUX_SEL[2:0]=001 |
| SFP #3 | S2 | 4 | I2C through MUX_SEL[2:0]=010,<br>100M/1G capable |
| SFP #4 | S3 | 6 | I2C through MUX_SEL[2:0]=011,<br>100M/1G capable |
| SFP #5 | S4 | 9 | I2C through MUX_SEL[2:0]=100,<br>100M/1G capable |
| SFP #6 (with NPI PHY module) | S8 | 10 | I2C through MUX_SEL[2:0]=101,<br>100M/1G/2.5G capable |
| SFP #6 (with PCIe module) | S5 | 10 | I2C through MUX_SEL[2:0]=101,<br>100M/1G capable |
| SFP #7 | S6 | 7 | I2C through MUX_SEL[2:0]=110,<br>100M/1G/2.5G capable |
| SFP #8 | S7 | 8 | I2C through MUX_SEL[2:0]=111,<br>100M/1G/2.5G capable |
| NPI (only with NPI PHY module) | S4 | 9 | "External" MIIM address 0x1C |
| PCIe (only with PCIe module) | S8 | n/a | |

### 5.3.1 PHYs

The twisted pair interfaces on the copper PHYs of VSC7514EV are fully compliant with the IEEE802.3 specification for CAT-5 media. The Microsemi PHYs, unlike other traditional Gigabit PHYs, integrate all passive components required to connect the PHYs' CAT-5 interface to an external 1:1 transformer and common mode choke. This reduces the number of components in a design and greatly simplifies the layout of this interface.

The ports support auto-negotiation and can automatically detect the speed and duplex mode of a link and provide the appropriate connection in 10BASE-T half-duplex, 10BASE-T full duplex, 100BASE-T half-duplex, 100BASE-T full duplex or 1000BASE-T full duplex.

The ports include Automatic Crossover Detection functionality for all three speeds (HP Auto MDI/MDI-X function). They also include the ability to detect and correct polarity errors on all MDI pairs. These functions are normally enabled, but can be disabled.

The ports support the IEEE standard range of 1m to 100m twisted pair cable.

1000Base-T mode requires Category 5 enhanced cable in accordance to the cabling specifications defined by IEEE802.3-2005.

100BASE-TX mode requires Category 5 cable and 10BASE-T requires Category 3 cable as specified in ISO/IEC 11801.

### TVS diodes

The port-side signals (4 differential signals) comprising each of the 8 copper port interfaces of the mainboard can optionally be further protected from over-voltage events such as ESD, cable-discharge or lightning-induced transients by mounting TVS3V3L4U TVS diodes. Note that the capacitance of protection devices such as TVS diodes will add to the capacitance of PCB traces and e.g. EMI caps, and that the accumulated capacitance may impact e.g. IEEE template compliance.

## 5.3.2 SFP interfaces

VSC7514EV has eight front port SFP module slots connected directly to the VSC7514 switch. These can host 2.5Gbit/s, 1000BASE-X or 100BASE-FX SFP plugs, in this case PHY and SFP interface via a SERDES protocol - or copper SFP plugs via an SGMII protocol.

Note that the connection between VSC7514 and SFP6 is provided through the NPI/PCIe module, to allow for 5x1G+3x2.5G capable SFPs when using VSC7514EV in non-PCIe mode, and 6x1G+2x2.5G capable SFPs when using VSC7514EV in PCIe mode (where the PCIe port use the 2.5G capable VSC7514 SERDES port S8 otherwise used for SFP6 duties).

SFPs have the inherent “feature” of occupying a specific I2C slave address, which is an issue when several SFPs are to be connected to a single I2C master. VSC7514EV includes an I2C clock multiplexer in the form of a low-cost 74HC4051 device. Through this multiplexer one SFP I2C slave at a time is connected to the VSC7514 I2C master.

The semi-static control signals (LossOfSignal, TxFault, TxDisable, ModuleDetect and RateSelect) of the SFPs are connected to VSC7514 serial GPIOs as detailed in Table 6.

# 5.4 GPIO

The reference board uses the VSC7514 GPIO pins as detailed in Table 6.

**Table 6 VSC7514EV/VSC7514 GPIO**

| GPIO | Signal | Description |
|---|---|---|
| GPIO_0 | SGPIO_CLK | Serial GPIO/LED controller clock output |
| GPIO_1 | SGPIO_DO | Serial GPIO/LED controller data output |
| GPIO_2 | SGPIO_DI | Serial GPIO controller data input |
| GPIO_3 | SGPIO_LD | Serial GPIO/LED controller load output |
| GPIO_4 | nINT | Output from VSC8221 PHY and Sync-E add-on module towards VSC7514 |
| GPIO_5 | PUSHBUTTONn | Input from the reset push button, as the reset function has a one-shot the signal can be sampled by firmware e.g. during boot |
| GPIO_6 | RS232_RXD | Data received from USB-connected management serial port |
| GPIO_7 | RS232_TXD | Data transmitted to USB-connected management serial port |
| GPIO_8 | SPI_nCS_NAND | SPI chipselect signal towards NAND Flash |
| GPIO_9 | SPI_nCS_SYNCE | SPI chipselect signal towards Sync-E add-on module |
| GPIO_10 | MODULE_LDSV | PTP load/save signal from Sync-E add-on module |
| GPIO_11 | RS422SMA_LDSV | PTP load/save signal from RS422 PTP interface or SMA |
| GPIO_12 | RS422_RXD | Data received from RS422 PTP serial port |
| GPIO_13 | RS422_TXD | Data transmitted to RS422 PTP serial port |

| GPIO | Signal | Description |
|---|---|---|
| GPIO_14 | MII_MDC | Management bus clock |
| GPIO_15 | MII_MDIO | Management bus data |
| GPIO_16 | I2C_SDA | Data line in the I2C serial interface |
| GPIO_17 | I2C_SCL | Clock line in the I2C serial interface |
| GPIO_18 | PPS | PTP 1PPS output towards external PPS buffer |
| GPIO_19 | DDR3_RESETn | Reset signal for DDR3 interface |
| GPIO_20 | RCVRD_CLK0 | Recovered clock output from VSC7514 towards Sync-E add-on module |
| GPIO_21 | RCVRD_CLK1 | Recovered clock output from VSC7514 towards Sync-E add-on module |

## 5.5 Serial GPIO/LED

VSC7514 incorporates a novel serial GPIO mechanism.

Through four pins a serial GPIO controller interfaces to 74-series shift registers on the board to provide a flexible GPIO mechanism. It is documented in the Serial GPIO user's guide and in the VSC7514 datasheet.

Instead of 74-series shift registers, the external circuitry can of course be implemented in e.g. a central PLD, but the parallel inputs and outputs of this would then have to be routed across the board between the PLD and individual endpoints – using shift registers it is only the four VSC7514 serial GPIO signals which need to be routed "long distance", the shift registers can be distributed across the board as applicable.

On VSC7514EV the serial GPIO controller is used both to control port and system status LEDs and to connect to SFP out-of-band control signals.

The port and system status LEDs are tri-color – one pin controls a green LED, another pin controls a red LED, when both green and red LED parts are turned on simultaneously the LED shows a yellowish color.

Serial GPIO controller setup: Enable ports [23:0]. Enable bits 1:0. The individual bits in the serial GPIO output and input frames are used as detailed in Table 7.

**Table 7 Serial GPIO/LED**

| Port/bit | Output used for | Input used for |
|---|---|---|
| p0b0 | RJ45#3 (VSC7514 P0) / SFP#1 (VSC7514 S0) green LED (0=on, 1=off) | SFP#1 LOS |
| p0b1 | RJ45#3 (VSC7514 P0) / SFP#1 (VSC7514 S0) red LED (0=on, 1=off) | SFP#1 MODDETn |
| p1b0 | RJ45#4 (VSC7514 P1) / SFP#2 (VSC7514 S1) green LED (0=on, 1=off) | SFP#2 LOS (or resistor strapping option for µSD card CardDetect for VSC7514 config d) |
| p1b1 | RJ45#4 (VSC7514 P1) / SFP#2 (VSC7514 S1) red LED (0=on, 1=off) | SFP#2 MODDETn |
| p2b0 | RJ45#0 (VSC7514 P2) green LED (0=on, 1=off) | SFP#1 TXFAULT |
| p2b1 | RJ45#0 (VSC7514 P2) red LED (0=on, 1=off) | SFP#2 TXFAULT |
| p3b0 | RJ45#1 (VSC7514 P3) green LED (0=on, 1=off) | SFP#3 TXFAULT |
| p3b1 | RJ45#1 (VSC7514 P3) red LED (0=on, 1=off) | SFP#4 TXFAULT |
| p4b0 | SFP#3 (VSC7514 S2) green LED (0=on, 1=off) | SFP#3 LOS |

| Port/bit | Output used for | Input used for |
|---|---|---|
| p4b1 | SFP#3 (VSC7514 S2) red LED (0=on, 1=off) | SFP#3 MODDETn |
| p5b0 | Only used with resistor strapping option for VSC7514 config d | µSD card CardDetect (or resistor strapping option for SFP#2 LOS for VSC7514 config d) |
| p5b1 | Only used with resistor strapping option for VSC7514 config d | SFP#5 TXFAULT |
| p6b0 | SFP#4 (VSC7514 S3) green LED (0=on, 1=off) | SFP#4 LOS |
| p6b1 | SFP#4 (VSC7514 S3) red LED (0=on, 1=off) | SFP#4 MODDETn |
| p7b0 | SFP#7 (VSC7514 S6) green LED (0=on, 1=off) | SFP#7 LOS |
| p7b1 | SFP#7 (VSC7514 S6) red LED (0=on, 1=off) | SFP#7 MODDETn |
| p8b0 | SFP#8 (VSC7514 S7) green LED (0=on, 1=off) | SFP#8 LOS |
| p8b1 | SFP#8 (VSC7514 S7) red LED (0=on, 1=off) | SFP#8 MODDETn |
| p9b0 | SFP#5 (VSC7514 S4) green LED (0=on, 1=off) | SFP#5 LOS |
| p9b1 | SFP#5 (VSC7514 S4) red LED (0=on, 1=off) | SFP#5 MODDETn |
| p10b0 | SFP#6 (VSC7514 S8/S5) green LED (0=on, 1=off) | SFP#6 LOS |
| p10b1 | SFP#6 (VSC7514 S8/S5) red LED (0=on, 1=off) | SFP#6 MODDETn |
| p11b0 | System status LED green (0=on, 1=off) | SFP#6 TXFAULT |
| p11b1 | System status LED red (0=on, 1=off) | SFP#7 TXFAULT |
| p12b0 | LED_SEL_CU3 (0=SFP1 LED on, 1=CU3 LED on) | SFP#8 TXFAULT |
| p12b1 | LED_SEL_CU4 (0=SFP2 LED on, 1=CU4 LED on) | *not used* |
| p13b0 | MUX_SEL0 (selector for SFP I2C mux'ing) | *not used* |
| p13b1 | MUX_SEL1 (selector for SFP I2C mux'ing) | *not used* |
| p14b0 | MUX_SEL2 (selector for SFP I2C mux'ing) | *not used* |
| p14b1 | SPI_CS_SD (SPI chipselect towards µSD, 0=µSD deselected, 1=µSD selected) | *not used* |
| p15b0 | RS422_SLVOE (output enable for PTP slave RS422 PPS signal) | *not used* |
| p15b1 | RS422_MSTOE (output enable for PTP master RS422 PPS signal) | *not used* |
| p16b0 | SFP1_RATESEL | *not used* |
| p16b1 | SFP2_RATESEL | *not used* |
| p17b0 | SFP3_RATESEL | *not used* |
| p17b1 | SFP4_RATESEL | *not used* |
| p18b0 | SFP5_RATESEL | *not used* |
| p18b1 | SFP6_RATESEL | *not used* |
| p19b0 | SFP7_RATESEL | *not used* |
| p19b1 | SFP8_RATESEL | *not used* |
| p20b0 | SFP1_TXDISn (0=TX disable, 1=TX enable) | *not used* |
| p20b0 | SFP2_TXDISn (0=TX disable, 1=TX enable) | *not used* |
| p21b0 | SFP3_TXDISn (0=TX disable, 1=TX enable) | *not used* |
| p21b1 | SFP4_TXDISn (0=TX disable, 1=TX enable) | *not used* |

| Port/bit | Output used for | Input used for |
|---|---|---|
| p22b0 | SFP5_TXDISn (0=TX disable, 1=TX enable) | *not used* |
| p22b1 | SFP6_TXDISn (0=TX disable, 1=TX enable) | *not used* |
| p23b0 | SFP7_TXDISn (0=TX disable, 1=TX enable) | *not used* |
| p23b1 | SFP8_TXDISn (0=TX disable, 1=TX enable) | *not used* |

## 5.6 UARTs, USB for management and RS422 for PTP

The VSC7514 VCore-III CPU has two on-chip serial UARTs, available as alternate functions on GPIO pins.

UART1 is used as console port and connected through an FTDI FT234XD serial-to-USB converter to a µUSB connector on the reference board front. The FTDI FT234XD is reset when USB bus power is not available, to ensure that it awakens smoothly when connected through a USB cable to e.g. a PC.

UART2 is connected to two RJ45-terminated RS422 connectors through ISL3180E transceivers. Signal levels on the RJ45 pins are standard RS422 levels.

Over temperature, ISL3180E has well-defined propagation delays in both RX and TX directions.

The RJ45 connectors expose both the UART2 signals used for PTP information and 1PPS PTP signals. The latter include a 1pps output (in the “output” connector), a 1PPS load/save input (in the “input” connector), and a feedback path by which the PTP slave can feed back the PTP master’s 1PPS signal to the PTP master, hence allowing the PTP master to determine the transmission delay of RS422 transceivers and UTP cable between the PTP RJ45s.

**Table 8 RJ45 connector pinout for UART2 / RS422, “input”**

| Pin | Direction | Signal |
|---|---|---|
| 1 | Switch -> connector | FEEDBACK_TxN |
| 2 | Switch -> connector | FEEDBACK_TxP |
| 3 | Connector->switch | 1PPS_RxN |
| 4 | n/a | Ground |
| 5 | n/a | Ground |
| 6 | Connector->switch | 1PPS_RxP |
| 7 | Connector->switch | UART_RxN |
| 8 | Connector->switch | UART_RxP |

**Table 9 RJ45 connector pinout for UART2 / RS422, “output”**

| Pin | Direction | Signal |
|---|---|---|
| 1 | Connector->switch | FEEDBACK_RxN |
| 2 | Connector->switch | FEEDBACK_RxP |
| 3 | Switch -> connector | 1PPS_TxN |
| 4 | n/a | Ground |
| 5 | n/a | Ground |
| 6 | Switch -> connector | 1PPS_TxP |
| 7 | Switch -> connector | UART_TxN |

| Pin | Direction | Signal |
|---|---|---|
| 8 | Switch -> connector | UART_TxP |

## 5.7 I2C

SFP plugs include an I2C EEPROM used for identification. All SFPs reside on the same I2C address, thus a multi-SFP system needs an I2C segment per SFP in order to avoid I2C address conflicts.

VSC7514 contains an I2C multiplexer targeted at this issue, using separate I2C_SCL lines per I2C segment and a single shared I2C_SDA signal – these separate I2C_SCL lines are available as alternate functions on VSC7514 GPIO pins.

But as VSC7514EV has eight SFP ports and uses the VSC7514 GPIO resources for other purposes, a discrete I2C_SCL multiplexer is used in this design. The multiplexer part is an inexpensive 74HC4051 device, controlled by firmware through the three signals MUX_SEL[2:0]. MUX_SEL[2:0] determine which SFP I2C slave the VSC7514 I2C master is connected to, through the multiplexer. MUX_SEL[2:0] could have resided on VSC7514 GPIO pins, but as VSC7514EV uses these for other purposes MUX_SEL[2:0] are three serial GPIO outputs as detailed in Table 7. Note that there is an inherent latency from when firmware sets the relevant bits in the VSC7514 serial GPIO controller until they are output as part of a serial GPIO output frame ending up at the MUX_SEL[2:0] outputs of the serial GPIO shift register.

Mapping from MUX_SEL[2:0] to SFP ports is straightforward, see Table 10 for details.

**Table 10 MUX_SEL[2:0] to SFP I2C mapping**

| MUX_SEL[2:0] | SFP I2C |
|---|---|
| 000 | SFP #1 |
| 001 | SFP #2 |
| 010 | SFP #3 |
| 011 | SFP #4 |
| 100 | SFP #5 |
| 101 | SFP #6 |
| 110 | SFP #7 |
| 111 | SFP #8 |

I2C addresses are allocated according to Table 11.

**Table 11 I2C addresses**

| I2C address | Device |
|---|---|
| 1010xxx | SFP transceiver |

Other addresses can be used freely.

## 5.8 Interrupts

VSC7514 has dedicated interrupt inputs as alternate functions on GPIOs. These are used as depicted in Table 12.

**Table 12 Interrupt inputs**

| Interrupt | GPIO | Description |
|---|---|---|
| nINT | GPIO_4, IRQ0 | Shared (open collector) interrupt, used by Sync-E add-on module and VSC8221 single PHY (the latter only when the NPI module is added to the NPI/PCIe feature connector) |
| - | GPIO_5, IRQ1 | Not used in this reference design |

## 5.9 Reset

A MAX811 power watchdog monitors the 3.3 V supply and generates reset when applicable. The other supply voltages are not monitored.

A reset can also be triggered by the reset button mounted on the front of the reference board, by the SPI boot Flash programming header, or by the SI and NPI/PCIe feature connectors.

The reset button triggers a one-shot circuit on its path to the power watchdog button input, hence it is possible to keep the button pressed through a reset and have firmware detect that it is still pressed during boot, e.g. to trigger a “restore factory defaults” firmware function.

## 5.10 Reference clock, Synchronization and PTP

The reference board uses single-ended reference and recovered clocks, as single-ended clock buffers typically offer a cost advantage to differential clock buffers. Note that most of the reference clock recipients can also accept differential clocks, and that differential clocks (buffers and PCB traces) typically emit less radiated noise than single-ended clocks, so in some applications differential clocks may be a better option. Differentially distributed clocks may also offer the advantage of less jitter than single-ended clocks.

Signal level for the VSC7514 reference clock signal is LVCMOS33, with a resistor divider placed at VSC7514 converting the signal to a pseudo-differential clock as required by the VSC7514’s REFCLK_p/n differential input. Any changes to this should be thoroughly simulated on post-layout data – reference clock signal integrity is vital to the performance of the two clock signal consumers.

### 5.10.1 Default reference clock source

By default, a 25MHz OCXO is used as base frequency provider for the VSC7514. Using an OCXO with its superior frequency stability is a requirement for some IEEE1588 applications. VSC7514 is configured for a 25MHz reference clock input by pulling pins RefClk_Sel[1:0] low and RefClk_Sel[2] high.

### 5.10.2 Sync-E applications

For Sync-E applications the VSC7514EV reference board features a Sync-E feature connector.

A Sync-E add-on board mounted on this receives recovered network clocks from the VSC7514’s PHYs, selects one of them based on software-controlled prioritization (or a free-running clock when no recovered clocks are available), jitter attenuates the selected clock, and provides it back to the VSC7514EV reference board for distribution to the VSC7438/VSC7468 and PHYs.

When a Sync-E module is present, the OCXO clock towards the VSC7514 is output disabled, allowing the ClkOut_0 signal from the Sync-E module to drive the VSC7514 reference clock input. As ClkOut_0 is specified to be 125MHz, VSC7514 must be strapped for 125MHz operation when a Sync-

E module is present – this is handled by a resistor from the Sync-E module interface PRESENT_n signal to the VSC7514 REFCLK_SEL[2] pin.

The Sync-E feature connector for the switch reference board is type Samtec QSE-040-01-L-D-A , and the corresponding Sync-E feature connector for the Sync-E add-on board is type Samtec QTE-040-01-L-D-A.

The VCore-III I2C and SPI interfaces are provided in the Sync-E feature connector for interfacing to control interfaces of Sync-E devices located on add-on boards.

The Sync-E feature connector pin list is detailed in Table 13, and the Sync-E add-on board is further specified in RDR0017.

**Table 13 Sync-E feature connector**

| Signal | Direction | Pin | Pin | Direction | Signal |
|---|---|---|---|---|---|
| n/a | | 1 | 2 | | n/a |
| VSC7514 recovered clock 0 | Switch-> Module | 3 | 4 | | n/a |
| n/a | | 5 | 6 | | n/a |
| VSC7514 recovered clock 1 | Switch-> Module | 7 | 8 | | n/a |
| Gnd | | 9 | 10 | | Gnd |
| n/a | | 11 | 12 | | n/a |
| CLK_SMA_I | Switch-> Module | 13 | 14 | | n/a |
| n/a | | 15 | 16 | | n/a |
| MODULE_PPS | Switch-> Module | 17 | 18 | | n/a |
| Gnd | | 19 | 20 | | Gnd |
| n/a | | 21 | 22 | | n/a |
| n/a | | 23 | 24 | | n/a |
| n/a | | 25 | 26 | | n/a |
| n/a | | 27 | 28 | | n/a |
| Gnd | | 29 | 30 | | Gnd |
| n/a | | 31 | 32 | | n/a |
| n/a | | 33 | 34 | | n/a |
| n/a | | 35 | 36 | | n/a |
| n/a | | 37 | 38 | | n/a |
| Gnd | | 39 | 40 | | Gnd |
| n/a (FreeClkIn) | (Switch-> Module) | 41 | 42 | | n/a |
| ClkOut0 | Switch <-Module | 43 | 44 | | n/a |
| Gnd | | 45 | 46 | | n/a |
| n/a | | 47 | 48 | | n/a |
| Gnd | | 49 | 50 | | n/a |
| n/a | | 51 | 52 | | n/a |
| Gnd | | 53 | 54 | | n/a |
| n/a | | 55 | 56 | | n/a |

| Signal | Direction | Pin | Pin | Direction | Signal |
|---|---|---|---|---|---|
| Gnd | | 57 | 58 | | Gnd |
| SPI_EN_n | Switch-> Module | 59 | 60 | Module<-Switch | SPI_MOSI |
| SPI_CLK | Switch-> Module | 61 | 62 | Module-> Switch | SPI_MISO |
| Gnd | | 63 | 64 | | Gnd |
| I2C_SDA | Switch<-> Module | 65 | 66 | Module-> Switch | LATE_RESET_n |
| I2C_SCL | Switch<-> Module | 67 | 68 | Module-> Switch | INT_n |
| VCC_3V3 | Switch-> Module | 69 | 70 | Module-> Switch | PRESENT_n |
| VCC_3V3 | Switch-> Module | 71 | 72 | | Gnd |
| n/a | | 73 | 74 | | n/a |
| n/a | | 75 | 76 | | n/a |

### 5.10.3 Precision Time Protocol support

VSC7514EV supports PTP on the copper and SFP front ports directly connected to VSC7514 – the NPI port available through the NPI PHY add-on module is not part of the PTP scheme.

The VSC7514 1PPS output is routed to a fan-out buffer with well-defined propagation delay and then on to the connectors exposing PTP signals, e.g. the RS422 UART interface and the SMAs.

VSC7514 Load/Save inputs originate from either the RS422 UART PTP interface (if configured as PTP slave then originating from far-end PTP master, if configured as PTP master then feedback from far-end slave used to determine round-trip delay), from the SMAs or from the Sync-E add-on module.

### 5.10.4 SMA connectors

VSC7514EV has 2 input and 2 output SMA connectors connected as detailed in Table 14.

By default the various input / output frequencies are 10 MHz. If other frequencies are wanted e.g. 1.544 or 2.048 MHz this is controlled by VSC7514 firmware.

**Table 14 Default SMA connector inputs and outputs**

| Input | Sourced to | Note |
|---|---|---|
| 1 PPS<br>J34 | VSC7514<br>RS422SMA_LDSV<br>(GPIO 11) | External 1 PPS to VSC7514 |
| Various freq. J31 | CLK_SMA_I to Sync-E feature connector | External reference frequency to Sync-E add-on module |
| **Output** | **Sourced from** | **Note** |
| 1 PPS<br>J36 | VSC7514 PPS (GPIO 18, through fan-out buffer) | 1 PPS from VSC7514 |
| Various freq. J33 | ClkOut_1 from Sync-E feature connector | Output for monitoring Sync PLL on Sync-E add-on module |

Note that the SMA input is 3.3V LVCMOS tolerant and *not* e.g. 5 VLVCMOS tolerant.

## 5.11 JTAG

The JTAG signals from the VSC7514 are connected to a 2x7 pin 0.1” pitch boxed pin header complying with MIPS ICE connector specification as depicted in Table 15. Note that the optional RTCK/DINT signals are not supported.

The JTAG chain consists of connector TDI -> VSC7514 -> connector TDO.

**Table 15 MIPS ICE / JTAG connector**

| Signal | Direction | Pin | Pin | Direction | Signal |
|---|---|---|---|---|---|
| TRST* - Test Reset Input | Switch<-Probe | 1 | 2 | Switch<-Probe | VCore_ICE_nEN |
| TDI - Test Data Input | Switch<-Probe | 3 | 4 | | Gnd |
| TDO - Test Data Output | Switch->Probe | 5 | 6 | | Gnd |
| TMS - Test Mode Select Input | Switch<-Probe | 7 | 8 | | Gnd |
| TCK - Test Clock Input | Switch<-Probe | 9 | 10 | | Gnd |
| RST* - System Reset | Switch<-Probe | 11 | 12 | n/a | (RTCK - Return Test Clock Input) |
| (DINT - Debug Interrupt) | n/a | 13 | 14 | Probe<-Switch | VIO - Voltage Sense for I/O |

Though its default connection is to the VCore-III MIPS ICE interface within VSC7514, this connector can also be used for boundary scan JTAG. Note that the VSC7514 VCore_ICE_nEn needs to be pulled high to enter boundary scan JTAG mode – on VSC7514EV, VCore_ICE_nEn is pulled down as default leaving VSC7514 in its ICE JTAG mode.

## 5.12 Power supply

Table 16 lists a summary of the power consumption for VSC7514EV. Note that as VSC7514 characterization had not been concluded at the time this was written, the power consumption figures are estimated max values at specific operating conditions that are provided here only to dimension the power generation circuits. Consult the specific device datasheets for the most accurate power consumption figures.

**Table 16 VSC7514EV power**

| | Supply | Max amps | Max watts |
|---|---|---|---|
| **VSC7514** | | | |
| VDD_CORE | 1.0 | 2.020 | 2.02 |
| VDD_A | 1.0 | 0.316 | 0.32 |
| VDD_AL | 1.0 | 0.129 | 0.13 |
| VDD_AH | 2.5 | 0.500 | 1.25 |
| VDD_H | 2.5 | 0.025 | 0.06 |
| VDD_IO | 2.5 | 0.020 | 0.05 |
| VDD_S | 1.0 | 0.140 | 0.14 |
| VDD_DDR | 1.5 | 0.100 | 0.15 |
| *Total power for VSC7514* | | | *4.12* |
| **DDR3 RAM** | | | |
| DDR device | 1.5 | 0.230 | 0.35 |
| 0V75 generation | 1.5 | 0.008 | 0.01 |

| | Supply | Max amps | Max watts |
|---|---|---|---|
| *Total power for DDR* | | | *0.36* |
| **Misc** | | | |
| LEDs | 3.3 | 0.039 | 0.13 |
| SI NOR+NAND Flash | 3.3 | 0.045 | 0.15 |
| 8x SFP | 3.3 | 2.424 | 8.00 |
| NPI PHY | 3.3 | 0.303 | 1.00 |
| Sync-E module | 3.3 | 0.750 | 2.48 |
| OCXO | 3.3 | 0.121 | 0.40 |
| SGPIO, RS422, misc | 3.3 | 0.100 | 0.33 |
| *Total power for misc* | | | *12.48* |
| **Supply summary** | | | |
| 1.0V supply from 12V | 1.0 | 2.605 | 2.61 |
| Power dissipation in supply (@80% efficiency) | | | 0.52 |
| 1.5V supply from 3.3V | 1.5 | 0.338 | 0.51 |
| Power dissipation in supply (linear regulator, loss included in 3.3V supply) | | | 0.34 |
| 2.5V supply from 3.3V | 2.5 | 0.545 | 1.36 |
| Power dissipation in supply (linear regulator, loss included in 3.3V supply) | | | 0.27 |
| 3.3V supply from 12V (including source to 1.5V/2.5V linear regulators) | 3.3 | 4.665 | 15.39 |
| Power dissipation in supply (@80% efficiency) | | | 3.08 |
| 12V from DC input | 12.0 | 1.800 | 21.60 |

VSC7514EV contains regulators for:

- 1.0V@2.6A – VSC7514 core and SERDES
- 3.3V@4.7A – Flash, SFPs, LEDs, oscillator, source for 2.5V and 1.5V LDOs
- 2.5V@0.5A – VSC7514 digital IO and 1000Base-T
- 1.5V@0.3A – DDR3 core and IO and VSC7514 DDR IO

1.0V and 3.3V are generated by DC/DC converters from the 12Vdc input.

1.5V and 2.5V are generated by linear regulators from the local 3.3V supply.

# 6 Environmental requirements

VSC7514EV is designed to operate within the following temperatures (case and airflow dependent):

- Operating temperature: -40° to +40°C
- Storage temperature: -40° to +70°C
- Operating humidity: 10 % to 95 % relative humidity, non condensing

# 7 Layout

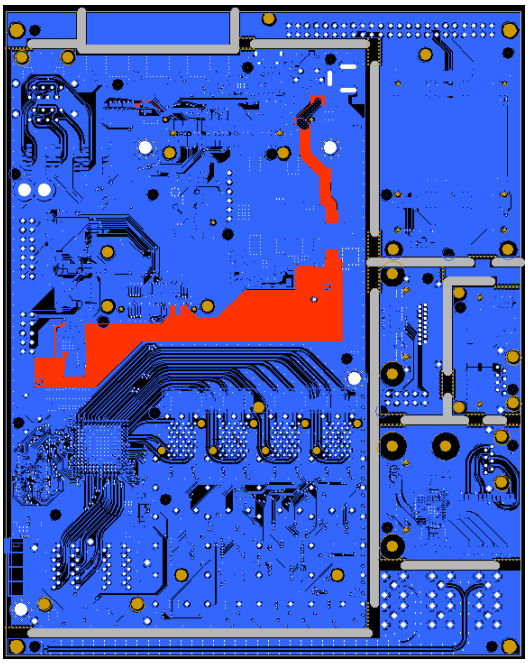
The VSC7514 device's package pinout is specifically optimized for low-cost PCB designs. As a result, the VSC7514EV reference board requires only four PCB layers. Layer 1 (top) contains signal traces as well as some power distribution planes, layer 2 is a solid ground plane, layer 3 contains power distribution, and layer 4 (bottom) additional routing and some power distribution planes. The solid ground plane layer is also used to remove heat from components and it must (also for this reason) be ensured that good connection between outer layer ground fills and the ground plane on layer 2 is established.

## 7.1 Power distribution

### 7.1.1 12V

The 12V power supply comes in from external PSU, passes over-voltage protecting tranzorbers and through a common-mode choke, lives mostly on layer 1 for use by the 1.0V and 3.3V DC/DC supplies, carrying a calculated total current of 1.8A.

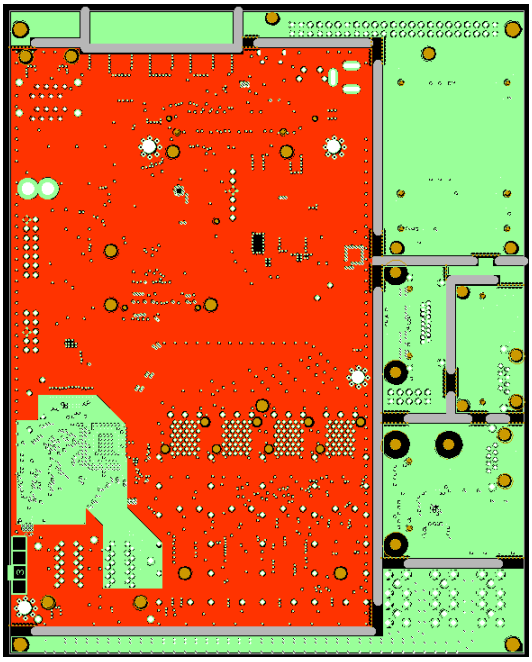
**Figure 8 12V distribution, layer 1**



### 7.1.2 3.3V

The 3.3V power supply is distributed mainly on layer 3 to devices as diverse as LEDs, Flash, LDO supplies and SFP modules. At 4.7A current, this is the highest-current path of the design, hence the distribution plane is as wide as possible. In order to compensate for the DC drop voltage in the plane, the DC/DC senses the voltage at the SFPs, through a 0 ohm resistor to ensure a discrete PCB trace.

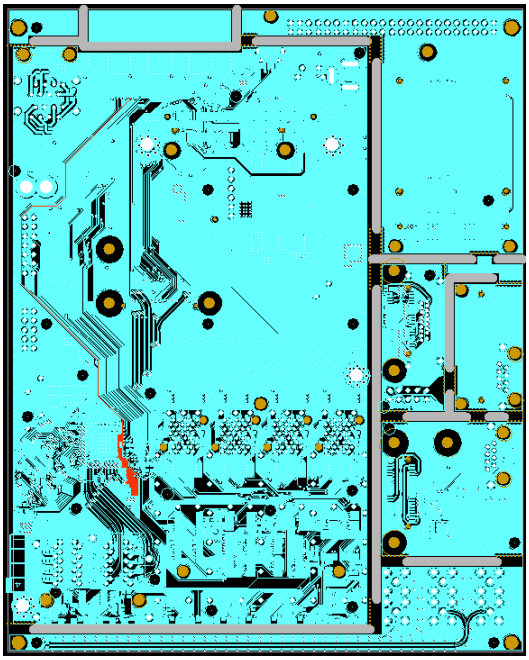
**Figure 9 3.3V distribution, layer 3**



### 7.1.3 2.5V

The 2.5V supply is led from the series regulator circuit to the VSC7514 switch. At 0.5A current, this is a fairly low-current path.

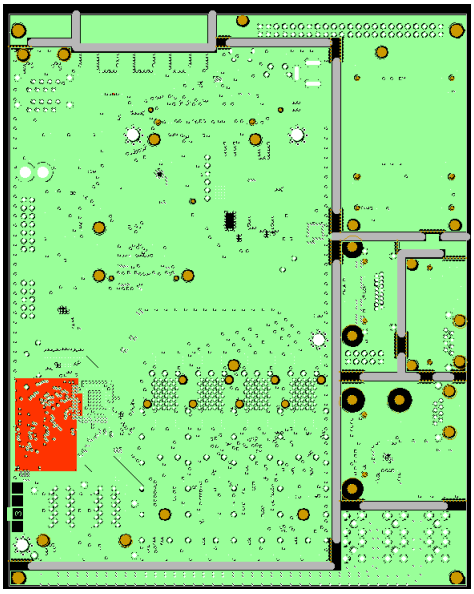
**Figure 10 2.5V distribution, layer 4**



### 7.1.4 1.5V

The 1.5V supply is led from the series regulator circuit to the VSC7514 switch and DDR3 device. At 0.3A current, this is a fairly low-current path.

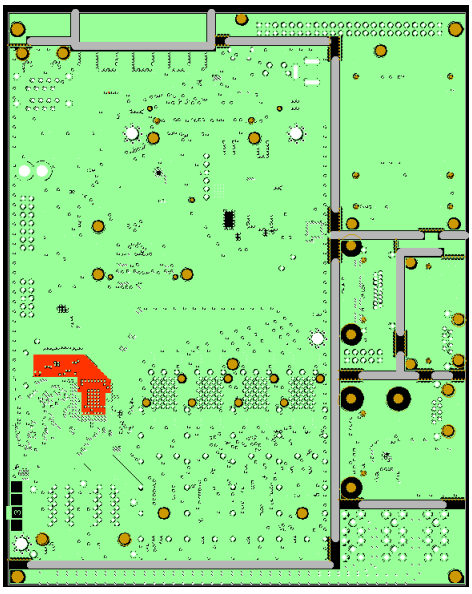
**Figure 11 1.5V distribution, layer 3**



### 7.1.5 1.0V

The 1.0V supply is led from the DC/DC circuit to the core and IO supplies of the VSC7514 switch. At 2.6A current, this is one of the highest-current paths of the design, hence the distribution plane is as wide as possible. In order to compensate for the DC drop voltage in the plane, the DC/DC senses the voltage close to VSC7514, through a 0 ohm resistor to ensure a discrete PCB trace.

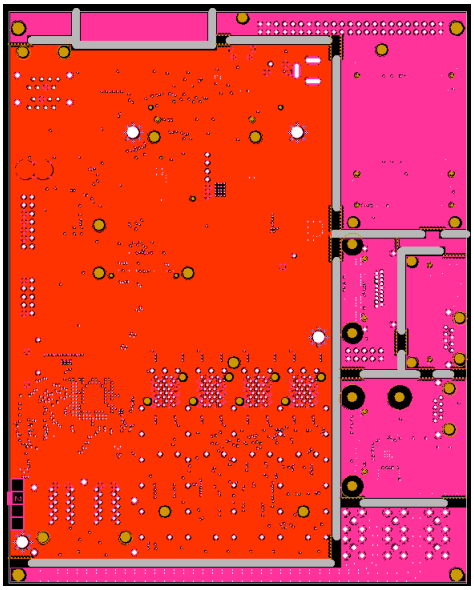
**Figure 12 1.0V distribution, layer 3**



### 7.1.6 Ground

A solid ground plane on layer 2 ensures that all signals on layer 1 have a good reference plane. In addition, the outer layers have ground fill areas for copper balancing purposes.

**Figure 13 Ground distribution, layer 2**



## 7.2 Critical nets' routing

Note that any net can be critical under the wrong circumstances – this is a minimum selection of nets that should be reviewed/simulated/measured thoroughly.

Also note the general PCB layout recommendations of chapter 9.

### 7.2.1 SERDES

**Figure 14 SERDES routing, layer 1**

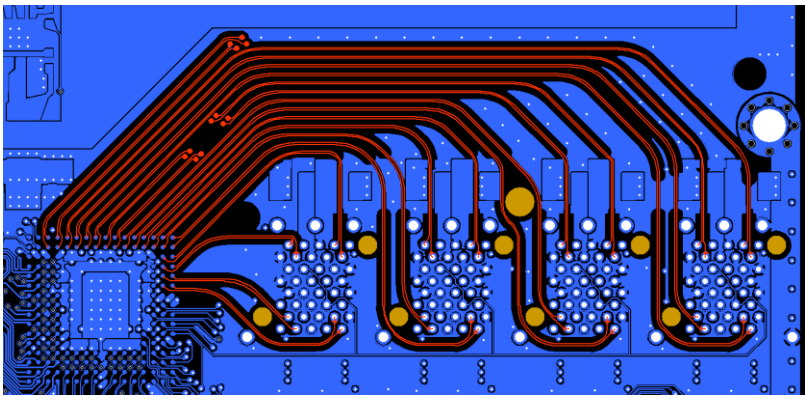
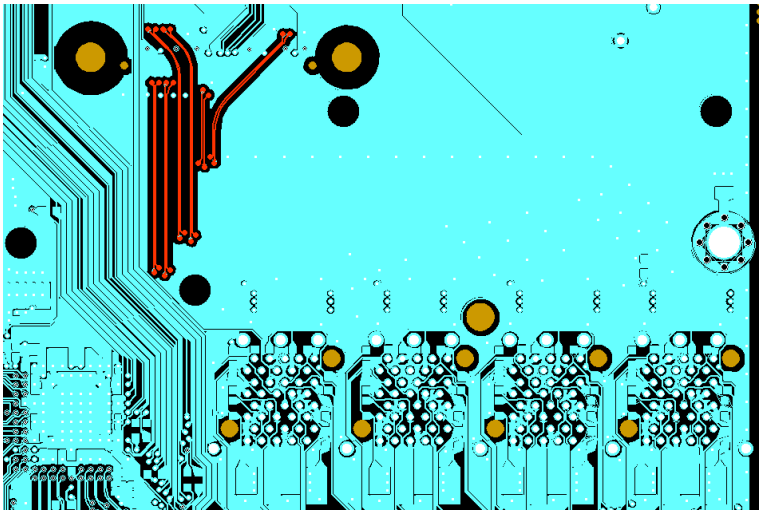


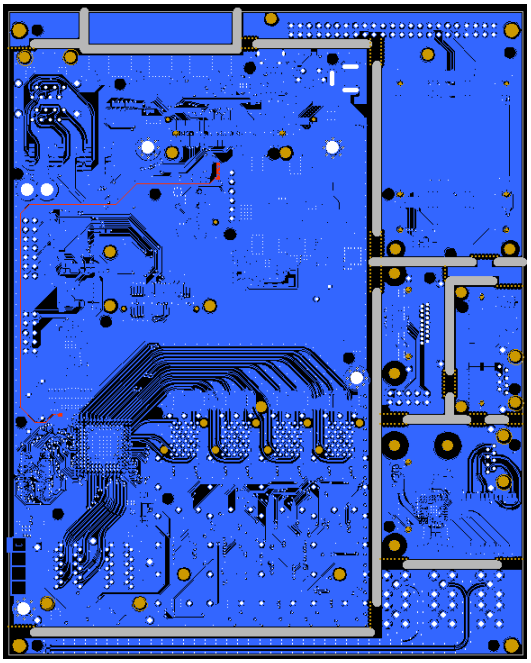
**Figure 15 SERDES routing, layer 4**



The SERDES signals are high bandwidth signals, up to 2.5Gbit/s. They are routed as differential pairs between VSC7515 switch and SFP connectors, for S5 and S8 with a detour to the NPI/PCIe feature connector. Signal traces are kept as short as possible, and intra-pair skews (p/n differences) are kept as close to 0 as possible.

### 7.2.2 Reference clock

**Figure 16 Reference clock routing, layer 1**



The reference clock signal is critical as e.g. clock jitter has a significant impact on device performance. The reference clock signal is routed from oscillator/buffer/Sync-E module to VSC7514 switch, with source series termination resistor placed at the driver. Signal traces are kept as short as possible and without vias.

### 7.2.3 Other clocks

Other clock signals include SI_CLK, MDC, I2C_SCL and SLED_CLK. Though not necessarily high frequency, these clock signals have fast risetimes so should be treated with care.

## 7.3 Component locations

**Figure 17 VSC7514EV component layout, top side**

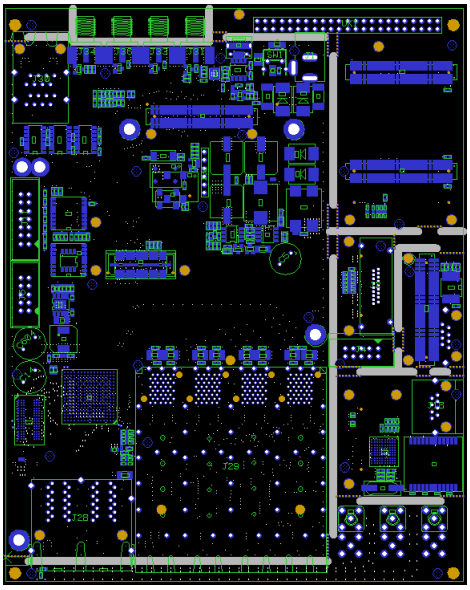
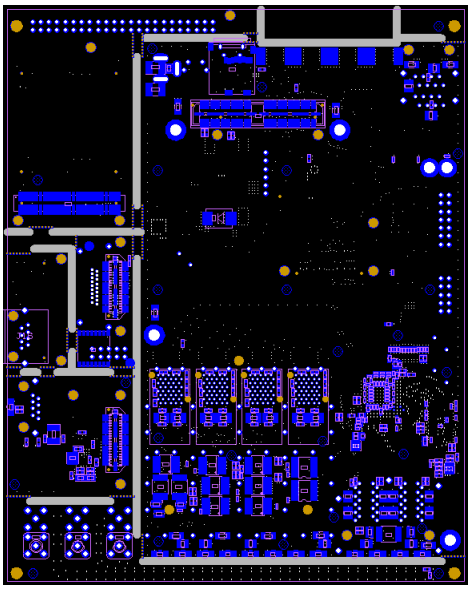
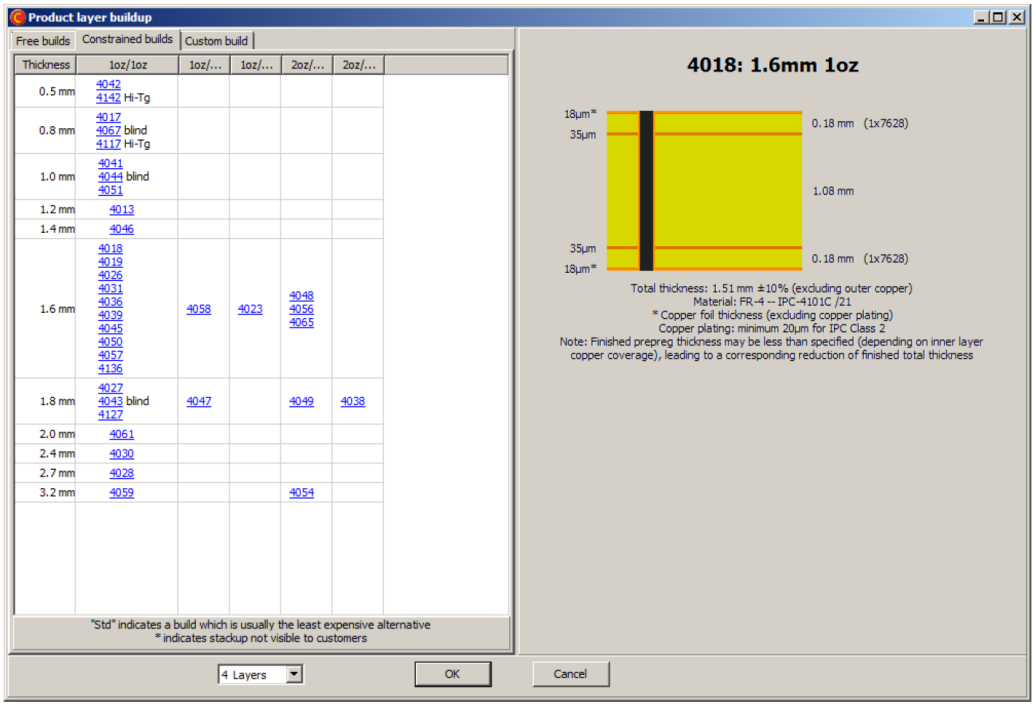


**Figure 18 VSC7514EV component layout, bottom side**



## 7.4 PCB stack-up

The board is a 4-layer impedance-controlled PCB. The stack-up of the layers is shown below.




## 7.5 PCB trace widths and clearance

| | |
|---|---|
| Board thickness | 1.6mm ± 10% |
| Characteristic impedance single ended | 70 ohm |
| Characteristic impedance differential signals | 100 ohm |
| Single ended trace width | 125um |
| Single ended trace to trace clearance | 125um |
| 100ohm differential trace width | 125um |
| 100ohm differential trace to trace clearance | 125um |

**Figure 19 Single-ended trace impedance calculations**

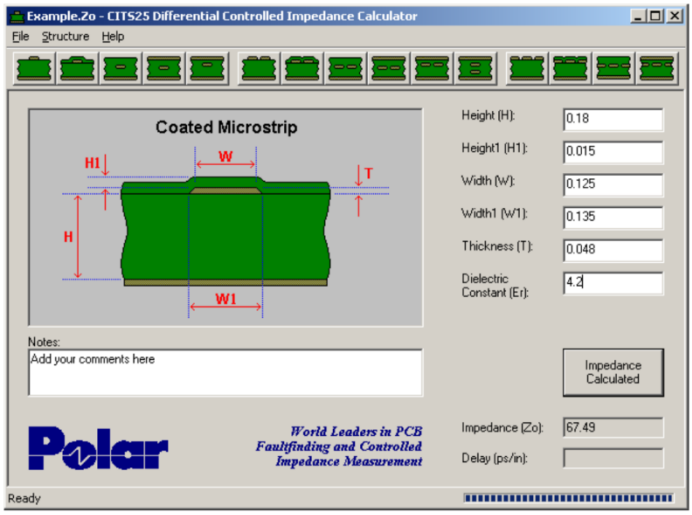
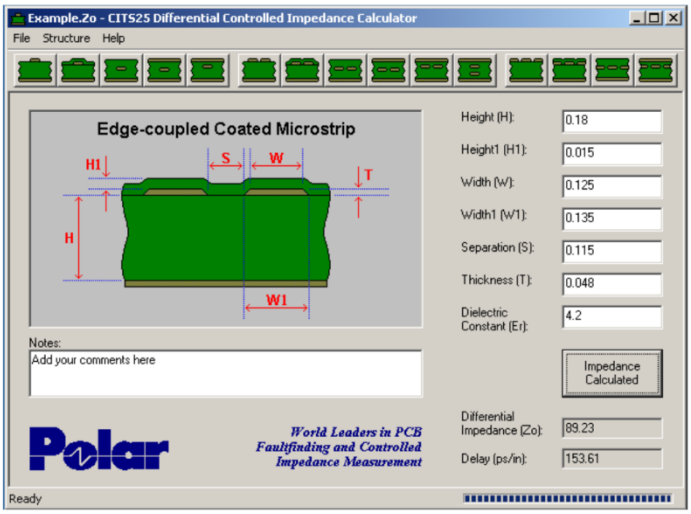



**Figure 20 Differential trace (SERDES etc.) impedance calculations**




Our experience is that the Polar tool's calculation of differential impedance is approx 10 ohms off, so that this geometry results in a differential impedance close to 100 ohms.

# 8 Schematic review checklist

This section describes the things board designers should check extra carefully when making a schematic. Note that this section is meant only to supplement the Design Guidelines section in the devices' datasheets. Ask your friendly Microsemi FAE for updated datasheets, device errata and schematics checklists and study these carefully before committing a design.

## 8.1 Reset control checklist

nReset (active low) must be de-asserted no less than 20ms after the power supplies and the reference clock are valid. For this reason a POR/delay circuit must be used on the nReset pin. The MAX811 can be used to provide the POR delay after valid power supplies and clock.

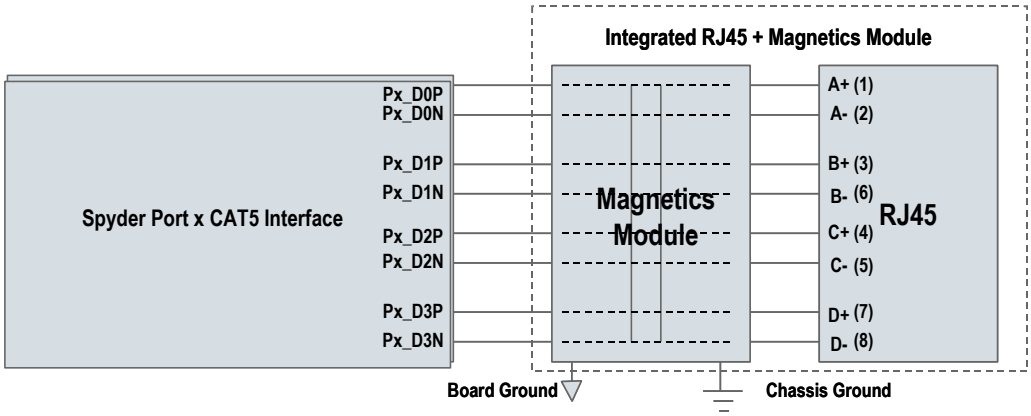
## 8.2 Reference clock checklist

The free-running reference clock can e.g. be a 25MHz or 125MHz +/-50 ppm clock source. Note the device datasheet's requirements for maximum clock jitter, which must be accounted for in board design when e.g. selecting clock source (oscillator) and clock distribution (buffer) components.

## 8.3 CAT5 media interface checklist

8 pins per port i.e. a total of 32 pins constitute the CAT5 media interface of VSC7514. These are named as Px_DyP and Px_DyN, where x is the port number 0-24 and y is the CAT5 cable pair 0-3.

Pairs 0-3 correspond to pairs A-D of the CAT5 cable respectively. Detailed connections of the CAT5 interface are shown below.




To pass the IEEE standard ESD tolerance tests it is important that the Board Ground and Chassis Ground be isolated across the Magnetic Module. However, it is recommended that a placeholder for a 0.1uf capacitor be included in the design for reducing EMI if needed. The magnetic module used is very important to ensure good EMI performance. Contact a Microsemi FAE to get the latest list of compatible magnetic modules.

Several different magnetic options exist, with different number of ferrite cores in the design, depending on the EMI performance needed. Microsemi recommends a magnetic module that includes one or more common mode chokes. The centre taps on the PHY side should be connected to board ground through 100nF capacitors.

## 8.4 Control signal checklist

- JTAG Interface
  - When JTAG is not being used, the JTAG_nTRST must be pulled down using a 1k resistor for normal operation.
- General Purpose I/Os
  - VSC7514 provides 22 GPIO pins, all with optional overlaid/alternate functions and some with additional strapping duties.
- Analog Bias Pins PHY
  - Ref_Rext: The resistor connected to this pin sets the internal reference bias of the PHY. A 2k, 1% resistor must be used.
  - Ref_Filt: The capacitor connected to this pin filters the internal reference bias.

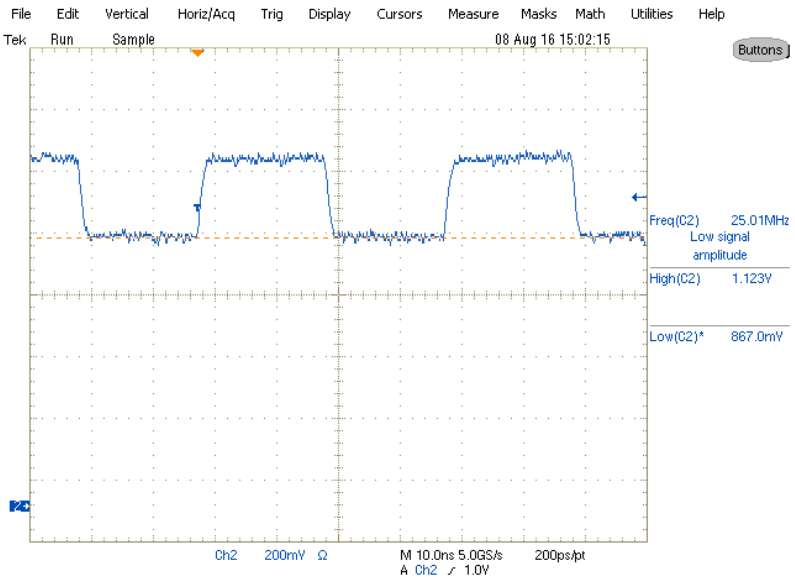
## 8.5 Using a single-ended signal to drive the differential reference clock input buffer

Though the VSC7514 reference clock input is differential with LVDS levels, it is possible to use it with a single-ended clock source. This is done by setting one differential input to a common-mode voltage and shaping the single-ended signal driving the other differential input so that it toggles around this common-mode voltage with a voltage swing comparable to LVDS. The reference clock differential input buffer will see this as a valid differential signal.

As the differential reference clock input has internal nominally 50R terminations to 1.0V (one 50R from REFCLK_P to 1.0V, one 50R from REFCLK_N to 1.0V), setting the REFCLK_N input to the common-mode voltage is achieved simply with a decoupling capacitor to ground – this ensures a 1.0V level on the REFCLK_N input.

Shaping the single-ended clock signal from an LVCMOS33 clock source to the levels required by the REFCLK_P input is achieved through a resistor divider. Note that because of the internal termination resistors in the reference clock input buffer, the 220R/430R external resistors proposed by the VSC7514 datasheet for dividing the clock signal do not simply decrease the voltage level on the REFCLK_P input to nominally 3.3V*430R/(220R+430R) = 2.2V – instead, the voltage level on the REFCLK_P input when voltage V is applied to the input of the 220R/430R resistor divider can be calculated as (Rbot*Rint*V+Rtop*Rbot*1.0V)/(Rtop*Rbot+Rbot*Rint+Rtop*Rint). With Rtop=220R, Rbot=430R and Rint=50R, then for V=3.3V the voltage level on the REFCLK_P input is calculated as 1.30V and for V=0V the voltage level on the REFCLK_P input is calculated as 0.74V, so a swing of approx ±250mV around the common-mode voltage 1.0V.

An actual measurement of a REFCLK_P input from a 3.3V single-ended source divided by 220R/430R resistors is shown below:




As the REFCLK_N input is set at 1.0V, the result seen by the reference clock input buffer is a pseudo-differential input with a peak-peak level of approx 250mV.

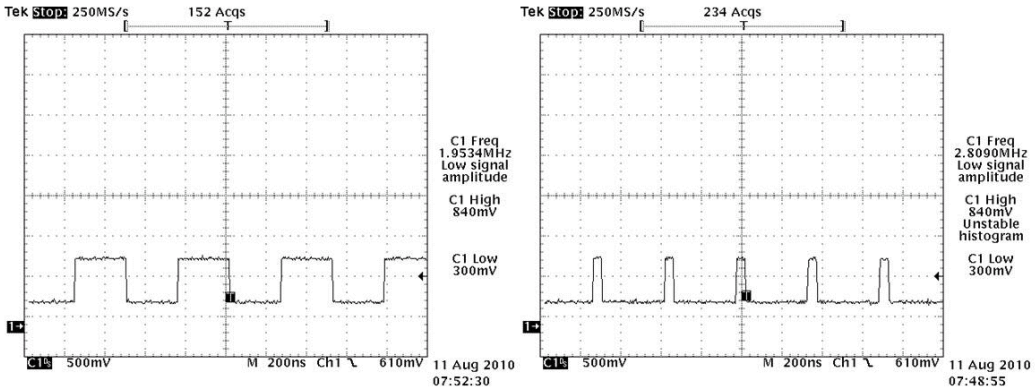
The voltage on any of the REFCLK pins should never exceed approx 1.25V, as that would trigger the input buffers' ESD protection diodes. Consult the devices' datasheets for exact values of this limit.

Note that differences in clock source output voltage levels, clock source output impedance, routing etc. may induce changes to the external voltage divider. The value of the dividing resistors is not important per se – what is important is the resulting signal as seen by the REFCLK_P input. This should be toggling around 1.0V with a swing as big as possible - a swing of ±200mV around the 1.0V common-mode voltage is safe regarding the ESD protection diode induced limits and also is big enough to offer reasonable noise margin.

Rise time of the signal presented to the REFCLK_P input is important. A decrease in rise time will result in less jitter seen by the REFCLK_P input. Consult the devices' datasheets for details and exact limits on rise time.

### 8.5.1 Monitoring PLL status

When debugging issues related to reference clock and PLL, the PLL's status can be monitored on a test signal output on the HS_TST_P pin. When the PLL is locked, implying that the reference clock input is sampled correctly, this test signal output toggles with a duty cycle of 50% - when the PLL is not locked it toggles with a duty cycle of 12.5%.




If the HS_TST_P signal is not available the health of the PLL can be induced from monitoring the MDC signal. When the PLL is locked this toggles with a frequency of 2.5MHz, when the PLL is not locked it toggles with a frequency of 4MHz. Note that after reset firmware can of course configure MDC for other frequencies.

# 9 Layout checklist

- Standard high-speed design layout techniques must be followed:
  - Minimize the number of signal vias.
  - No 90 deg bends - 45 deg bends or better curved traces can be used.
  - Traces must refer to a single power or ground plane, do not let high-speed traces pass plane splits on an adjacent layer.
  - In order to minimize crosstalk, the characteristic impedances of signals should be determined predominantly by the distance to the reference plane and not the distance to the neighboring traces.
  - Allow as much clearance between traces as possible, do not let two traces neighbor at a fixed low distance for extended lengths of trace.
  - Reduce trace length as much as possible, especially for high-speed single-ended signals (e.g. DDR) and very high-speed differential signals (e.g. QSGMII, XFI/SFI).
- Special care must be taken for the high-speed differential pairs (XFI/SFI/QSGMII/XAUI/SERDES/SGMII/PCIe etc.):
  - Must be routed as 100 ohms differential traces.
  - Allow as much clearance as possible between differential pairs, the well-known rule-of-thumb of “3*W” (W=width of trace) is absolute minimum, allow for 5*W or even 10*W clearance wherever possible to minimize crosstalk.
  - If guard traces or planes are used between individual pairs, use the same clearance constraints trace-to-plane as pair-to-pair (e.g. 3*W, 5*W or 10*W) to reduce the impact of the guard on the impedance of especially the trace (be that P or N) closest to the guard. Tie the guard to the inner layer ground plane frequently along the way – untied guards are good antennas.
  - Intra-pair skew (delta between lengths of P and N traces) must be as low as possible. E.g. for a 10Gbit/sec trace, an intra-pair skew of 3mm translates into 20ps or 20% of a bit, causing the differential receiver to read the signal with excessive jitter. “Nonchalance and high-speed don’t match”.
  - Inter-pair skew (delta between lengths of individual pairs) is typically less important. E.g. a XAUI interface can align lanes with up to 40 bits (12.8 ns / 2 meters) of inter-pair skew.
- 10/100/1000BASE-T signals are sensitive analog signals - that will be transmitted on up to 100 meters of UTP cable:
  - They must be routed from the PHY to magnetics, and from magnetics to the RJ45 connector, as four 100 ohm differential pairs for each port.
  - It is important to keep these signals away from noise sources. Differential (and some common mode) noise picked up by the signals between PHY and magnetics will end up as radiated emissions on the UTP cable. Differential as well as common mode noise picked up by the signals between magnetics and RJ45 connector will end up as radiated emissions on the UTP cable.

- It is also important to keep the two traces that make up a differential pair same length, as any difference in length will result in differential-to-common mode conversion of the signal and this will also end up as radiated emissions on the UTP cable.

- Low-bandwidth serial interfaces have fast edges too:
  - Even though the effective bandwidths of these interfaces are pretty low, it is important to avoid reflections on the multidrop clocks (MDC, I2C_SCL, SGPIO_CLK and SPI_CLK). Route the clock nets daisy-chained from the source to first consumer, then to the next consumer etc. and finally to the parallel termination network.
  - The pull-ups on MDIO and I2C_SDA must be present and can be placed where convenient.
- All power supplies must be routed as planes. Additional constraints:
  - Limit via sharing (where several power pins are connected to a single via) – ideally each power pin should be connected to its associated power plane through a dedicated via.
  - Surface mount local decoupling capacitors must be used and should be placed as close to the power supply pins as possible.
  - Analog supplies must be isolated from the remaining board supplies using ferrite beads.
  - Use a single ground point for the REF_REXT/REF_FILT resistor and capacitor.
- Simulate the completed design, and possibly selected signals during layout:
  - Simulate power integrity, e.g. power drops / current densities. Even though Microsemi devices are low power, small voltage drops on e.g. a 1.0V supply quickly add up to several percent of nominal voltage. If power integrity simulation shows issues, you can possibly solve them by using wider planes, or by using thicker planes (e.g. ½ oz -> 2 oz copper), or in some cases by using a remote sense point (located at the power consumer) for the DC/DC converter circuit.
  - Simulate signal integrity. DDR / SGMII / SERDES / XAUI / QSGMII / SFI / XFI signals are high speed, in some cases so high speed that it makes more sense to simulate on the layout file than to measure on the actual board. If a full simulation is not possible, then simulating e.g. a single lane of a multi-lane interface can still provide valuable insight. Microsemi supplies IBIS or IBIS-AMI models for its devices' high-speed inputs/outputs. Use the more accurate IBIS-AMI models when available, both for the target signal and for e.g. neighboring crosstalk aggressors.