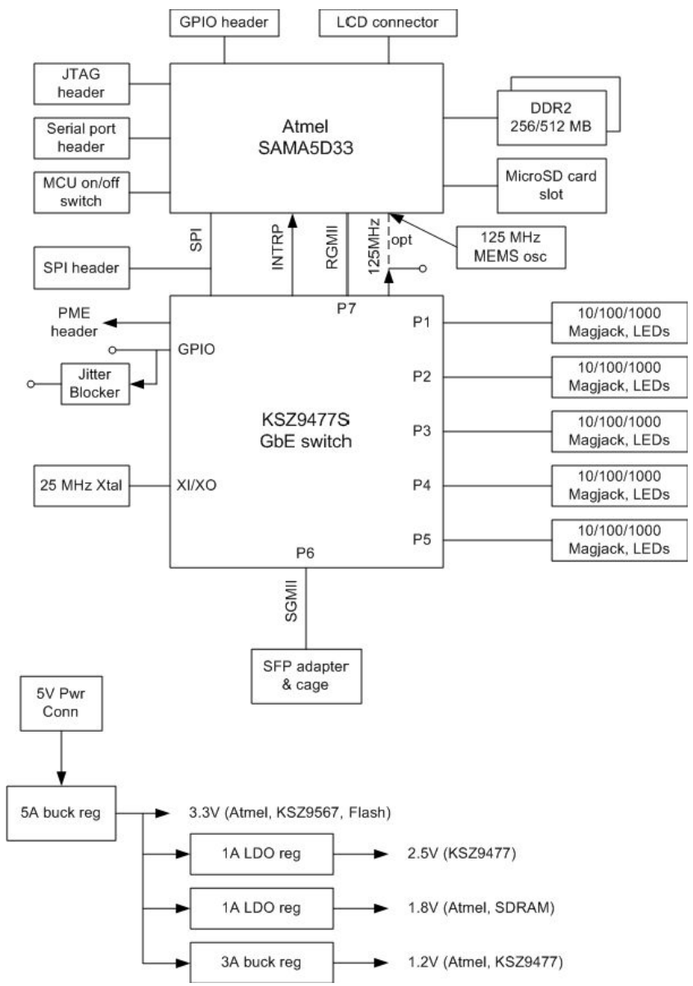
KSZ9477 EVB/Demo Board with Atmel SAMA5D3 SoC

Table of Contents

Revision History

Revision	Date	Revision Summary	Author
A00	6/23/2016	Pre-release	Kelly Maas
B	12/15/2016	Release	Kelly Maas
B1	3/9/2017	Update KSZ9477 SGMII pin names, update notes	Kelly Maas

Block Diagram



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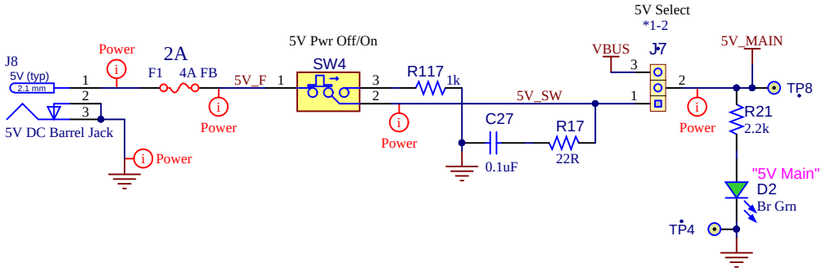
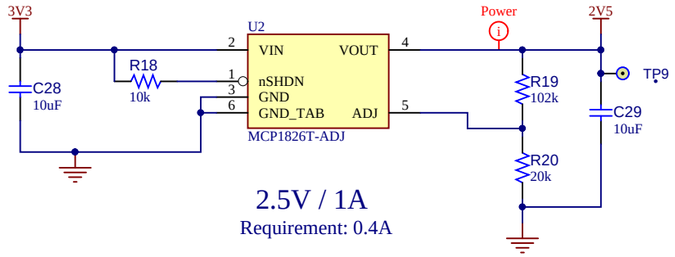
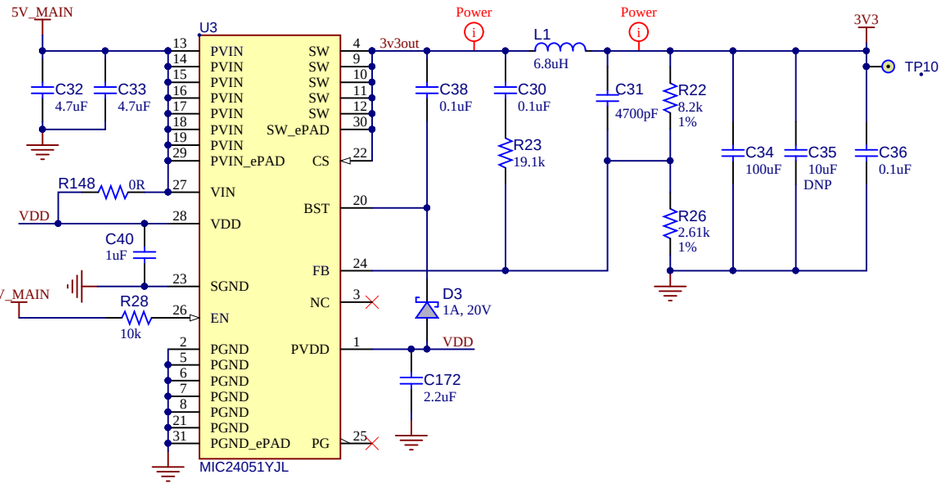
Description: KSZ9477 EVB_Demo Board with SAMA5D3 SoC			
Page Title: Title Page			
Project Name: KSZ9477 EVB_Demo		PN: UNG_8071	
Size: B	Date: 3/30/2017	Designer: Kelly Maas	Sheet 1 of 8	Rev B1

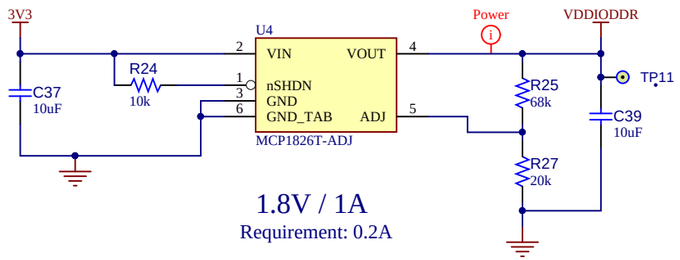




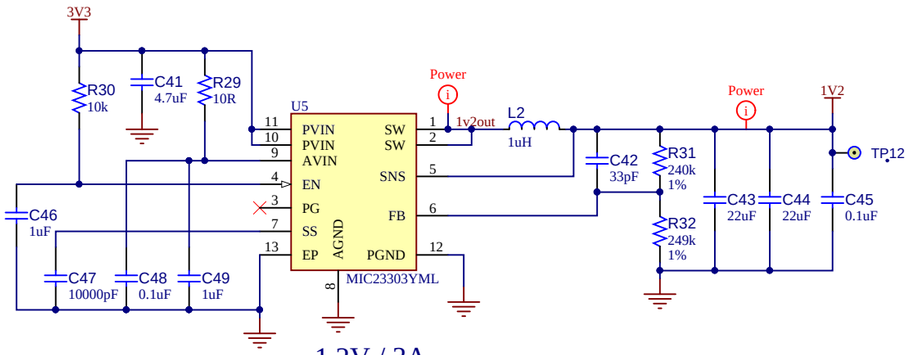
2.5V / 1A
Requirement: 0.4A



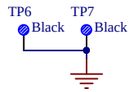
3.3V / 6A
Requirement: 2A



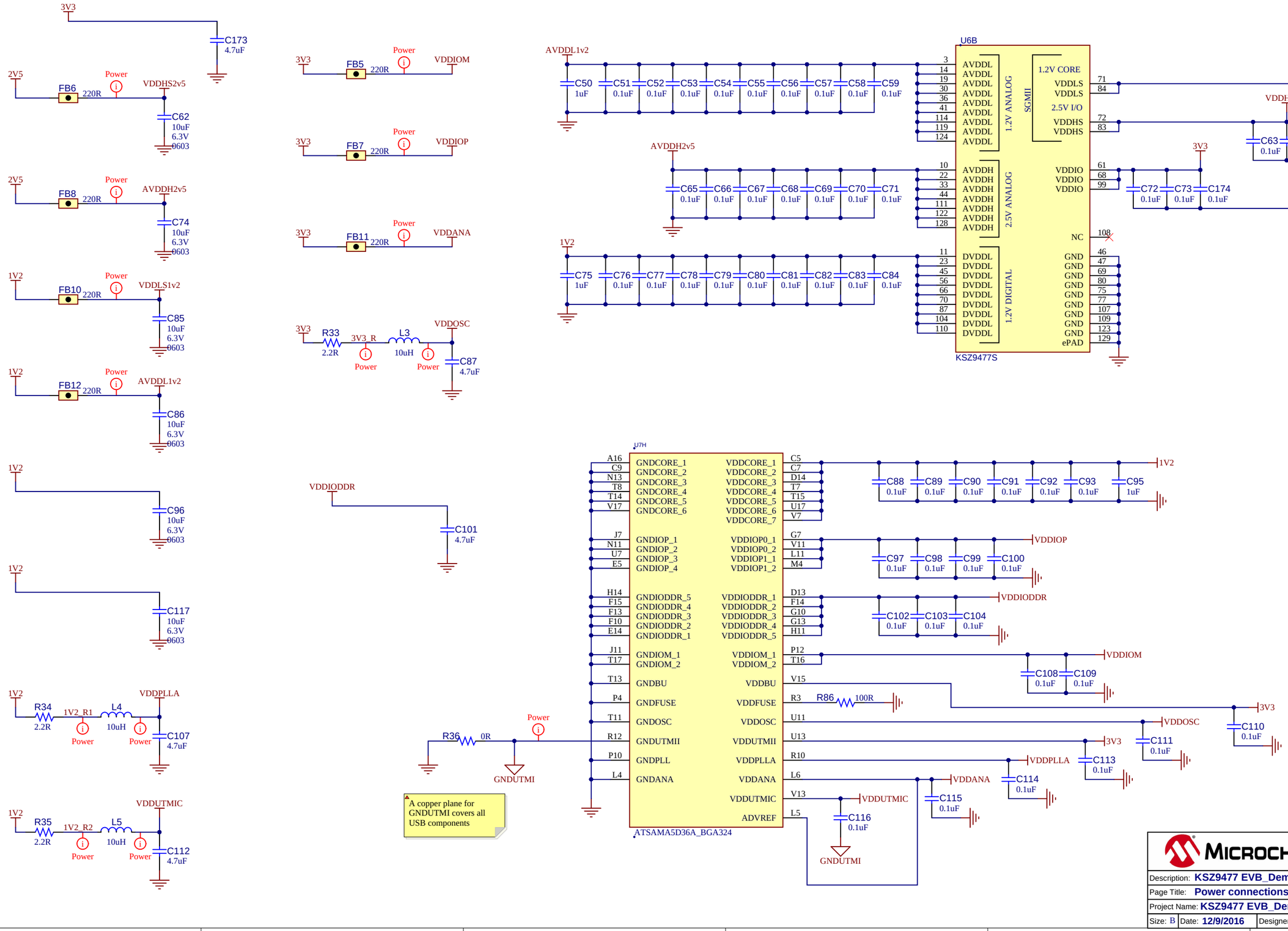
1.8V / 1A
Requirement: 0.2A



1.2V / 3A
Requirement: 1.6A



MICROCHIP	Microchip Technology, Inc. USB/Network Group - UNG www.Microchip.com	Designed with Altium Altium.com	
Description: KSZ9477 EVB_Demo Board with SAMA5D3 SoC			
Page Title: Board Power I/O and Regulators			
Project Name: KSZ9477 EVB_Demo		PN: UNG_8071	
Size: B	Date: 12/16/2016	Designer: Kelly Maas	Sheet 2 of 8	Rev B1



Microchip Technology, Inc.	Designed with Altium
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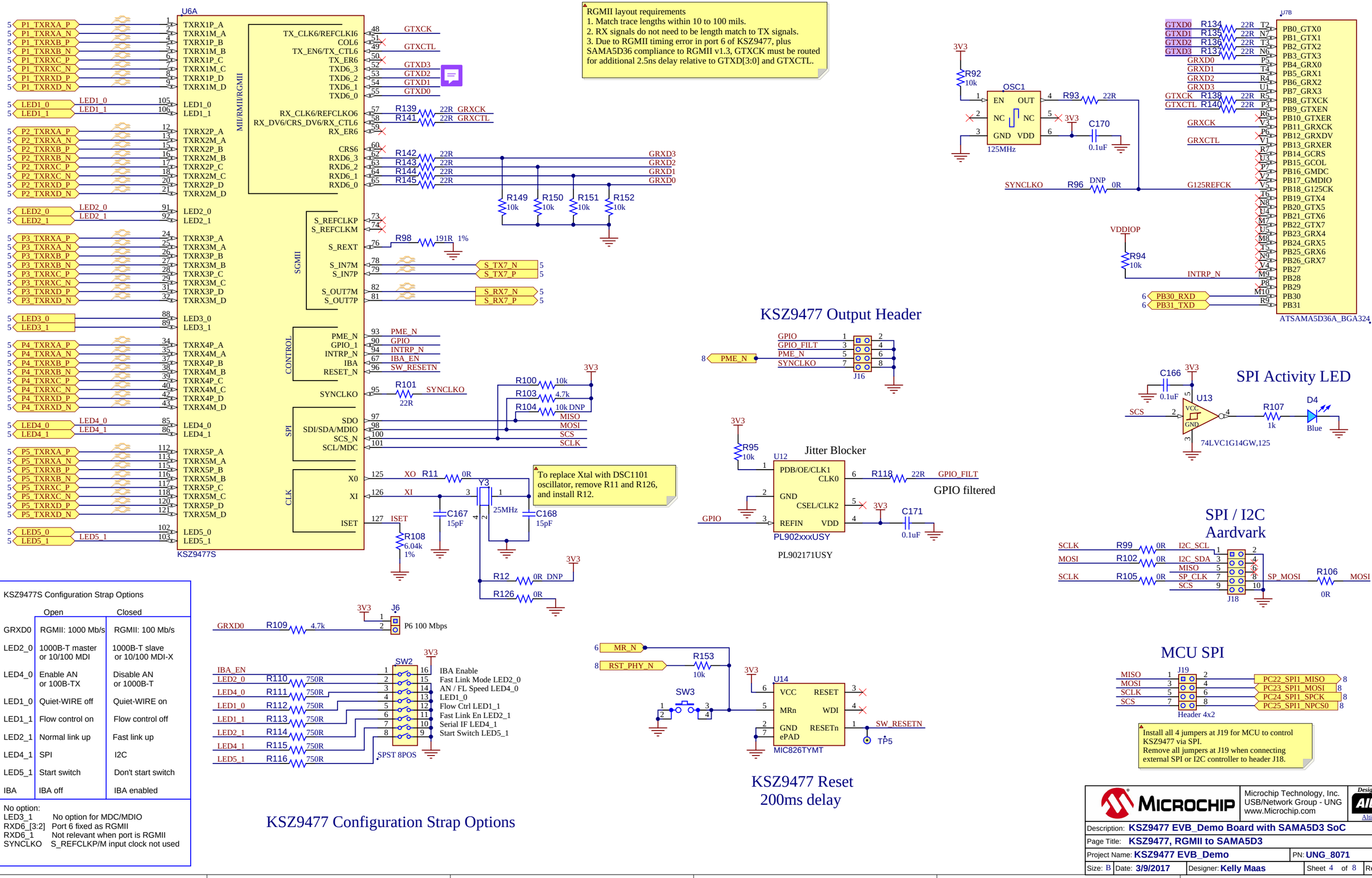
Description: KSZ9477 EVB_Demo Board with SAMA5D3 SoC	
Page Title: Power connections for switch and SoC	
Project Name: KSZ9477 EVB_Demo	PN: UNG_8071
Size: B | Date: 12/9/2016 | Designer: Kelly Maas	Sheet 3 of 8 | Rev B1


U6A
KSZ9477S
P1_TXRXA_P
P1_TXRXA_N
P1_TXRXB_P
P1_TXRXB_N
P1_TXRXC_P
P1_TXRXC_N
P1_TXRXD_P
P1_TXRXD_N
LED1_0
LED1_1
P2_TXRXA_P
P2_TXRXA_N
P2_TXRXB_P
P2_TXRXB_N
P2_TXRXC_P
P2_TXRXC_N
P2_TXRXD_P
P2_TXRXD_N
LED2_0
LED2_1
P3_TXRXA_P
P3_TXRXA_N
P3_TXRXB_P
P3_TXRXB_N
P3_TXRXC_P
P3_TXRXC_N
P3_TXRXD_P
P3_TXRXD_N
LED3_0
LED3_1
P4_TXRXA_P
P4_TXRXA_N
P4_TXRXB_P
P4_TXRXB_N
P4_TXRXC_P
P4_TXRXC_N
P4_TXRXD_P
P4_TXRXD_N
LED4_0
LED4_1
P5_TXRXA_P
P5_TXRXA_N
P5_TXRXB_P
P5_TXRXB_N
P5_TXRXC_P
P5_TXRXC_N
P5_TXRXD_P
P5_TXRXD_N
LED5_0
LED5_1
TXRX1P_A
TXRX1M_A
TXRX1P_B
TXRX1M_B
TXRX1P_C
TXRX1M_C
TXRX1P_D
TXRX1M_D
LED1_0
LED1_1
TXRX2P_A
TXRX2M_A
TXRX2P_B
TXRX2M_B
TXRX2P_C
TXRX2M_C
TXRX2P_D
TXRX2M_D
LED2_0
LED2_1
TXRX3P_A
TXRX3M_A
TXRX3P_B
TXRX3M_B
TXRX3P_C
TXRX3M_C
TXRX3P_D
TXRX3M_D
LED3_0
LED3_1
TXRX4P_A
TXRX4M_A
TXRX4P_B
TXRX4M_B
TXRX4P_C
TXRX4M_C
TXRX4P_D
TXRX4M_D
LED4_0
LED4_1
TXRX5P_A
TXRX5M_A
TXRX5P_B
TXRX5M_B
TXRX5P_C
TXRX5M_C
TXRX5P_D
TXRX5M_D
LED5_0
LED5_1
MII/RMII/RGMII
TX_CLK6/REFCLKI6
COL6
TX_EN6/TX_CTL6
TX_ER6
TXD6_3
TXD6_2
TXD6_1
TXD6_0
RX_CLK6/REFCLKO6
RX_DV6/CRS_DV6/RX_CTL6
RX_ER6
CRS6
RXD6_3
RXD6_2
RXD6_1
RXD6_0
GTXCK
GTXCTL
GTXD3
GTXD2
GTXD1
GTXD0
R139 22R GRXCK
R141 22R GRXCTL
R142 22R GRXD3
R143 22R GRXD2
R144 22R GRXD1
R145 22R GRXD0
R149 10k
R150 10k
R151 10k
R152 10k
SGMII
S_REFCLKP
S_REFCLKM
S_REXT
S_IN7M
S_IN7P
S_OUT7M
S_OUT7P
R98 191R 1%
S_TX7_N
S_TX7_P
S_RX7_N
S_RX7_P
CONTROL
PME_N
GPIO_1
INTRP_N
IBA
RESET_N
SYNCLKO
PME_N
GPIO
INTRP_N
IBA_EN
SW_RESETN
R101 22R
SPI
SDO
SDI/SDA/MDIO
SCS_N
SCL/MDC
MISO
MOSI
SCS
SCLK
R100 10k
R103 4.7k
R104 10k DNP
3V3
CLK
X0
XI
ISET
XO
XI
R11 0R
Y3
25MHz
C167 15pF
C168 15pF
R108 6.04k 1%
R12 0R DNP
R126 0R
To replace Xtal with DSC1101 oscillator, remove R11 and R126, and install R12.
RGMII layout requirements
1. Match trace lengths within 10 to 100 mils.
2. RX signals do not need to be length match to TX signals.
3. Due to RGMII timing error in port 6 of KSZ9477, plus SAMA5D36 compliance to RGMII v1.3, GTXCK must be routed for additional 2.5ns delay relative to GTXD[3:0] and GTXCTL.
KSZ9477 Output Header
J16
Jitter Blocker
U12
PDB/OE/CLK1
CLK0
GND
CSEL/CLK2
REFIN
VDD
PL902xxxUSY
PL902171USY
R95 10k
R118 22R
GPIO_FILT
GPIO filtered
C171 0.1uF
OSC1
125MHz
R92 10k
R93 22R
C170 0.1uF
SYNCLKO
R96 DNP 0R
G125REFCK
VDDIOP
R94 10k
INTRP_N
U7B
ATSAMA5D36A_BGA324
GTXD0 R134 22R
GTXD1 R135 22R
GTXD2 R136 22R
GTXD3 R137 22R
GRXD0
GRXD1
GRXD2
GRXD3
GTXCK R138 22R
GTXCTL R140 22R
GRXCK
GRXCTL
PB0_GTX0
PB1_GTX1
PB2_GTX2
PB3_GTX3
PB4_GRX0
PB5_GRX1
PB6_GRX2
PB7_GRX3
PB8_GTXCK
PB9_GTXEN
PB10_GTXER
PB11_GRXCK
PB12_GRXDV
PB13_GRXER
PB14_GCRS
PB15_GCOL
PB16_GMDC
PB17_GMDIO
PB18_G125CK
PB19_GTX4
PB20_GTX5
PB21_GTX6
PB22_GTX7
PB23_GRX4
PB24_GRX5
PB25_GRX6
PB26_GRX7
PB27
PB28
PB29
PB30
PB31
PB30_RXD
PB31_TXD
SPI Activity LED
C166 0.1uF
U13
74LVC1G14GW,125
SCS
R107 1k
D4
Blue
SPI / I2C
Aardvark
J18
SCLK R99 0R I2C_SCL
MOSI R102 0R I2C_SDA
SCLK R105 0R SP_CLK
MISO
SCS
SP_MOSI
R106 0R
MOSI
KSZ9477S Configuration Strap Options
Open
Closed
GRXD0 RGMII: 1000 Mb/s RGMII: 100 Mb/s
LED2_0 1000B-T master or 10/100 MDI 1000B-T slave or 10/100 MDI-X
LED4_0 Enable AN or 100B-TX Disable AN or 1000B-T
LED1_0 Quiet-WIRE off Quiet-WIRE on
LED1_1 Flow control on Flow control off
LED2_1 Normal link up Fast link up
LED4_1 SPI I2C
LED5_1 Start switch Don't start switch
IBA IBA off IBA enabled
No option:
LED3_1 No option for MDC/MDIO
RXD6_[3:2] Port 6 fixed as RGMII
RXD6_1 Not relevant when port is RGMII
SYNCLKO S_REFCLKP/M input clock not used
KSZ9477 Configuration Strap Options
J6
GRXD0 R109 4.7k
P6 100 Mbps
SW2
SPST 8POS
IBA_EN
LED2_0 R110 750R
LED4_0 R111 750R
LED1_0 R112 750R
LED1_1 R113 750R
LED2_1 R114 750R
LED4_1 R115 750R
LED5_1 R116 750R
IBA Enable
Fast Link Mode LED2_0
AN / FL Speed LED4_0
LED1_0
Flow Ctrl LED1_1
Fast Link En LED2_1
Serial IF LED4_1
Start Switch LED5_1
MR_N
RST_PHY_N
R153 10k
SW3
U14
MIC826TYMT
VCC
MRn
GND
ePAD
RESET
WDI
RESETn
SW_RESETN
TP5
KSZ9477 Reset
200ms delay
MCU SPI
J19
Header 4x2
MISO
MOSI
SCLK
SCS
PC22_SPI1_MISO
PC23_SPI1_MOSI
PC24_SPI1_SPCK
PC25_SPI1_NPCS0
Install all 4 jumpers at J19 for MCU to control KSZ9477 via SPI.
Remove all jumpers at J19 when connecting external SPI or I2C controller to header J18.
MICROCHIP
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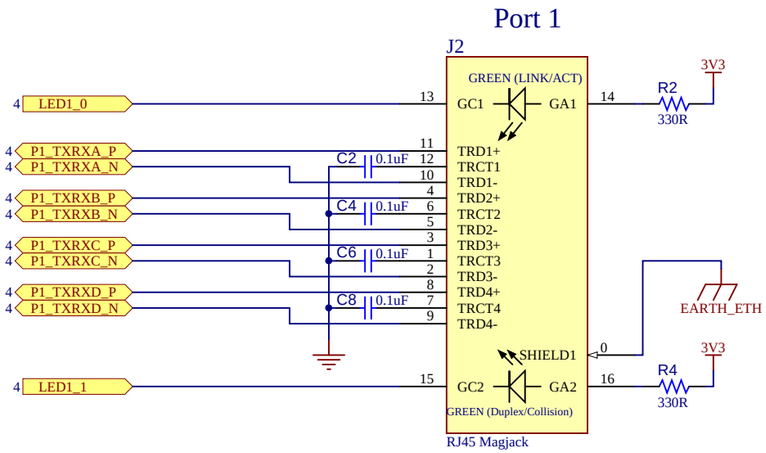
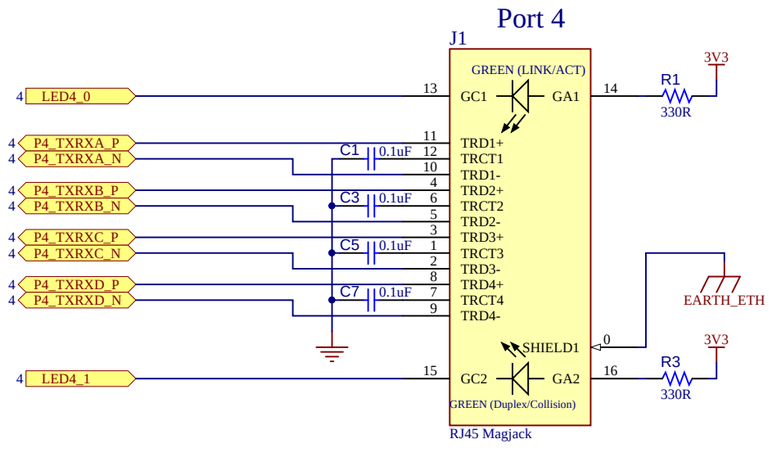
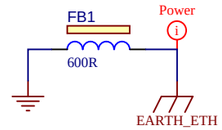
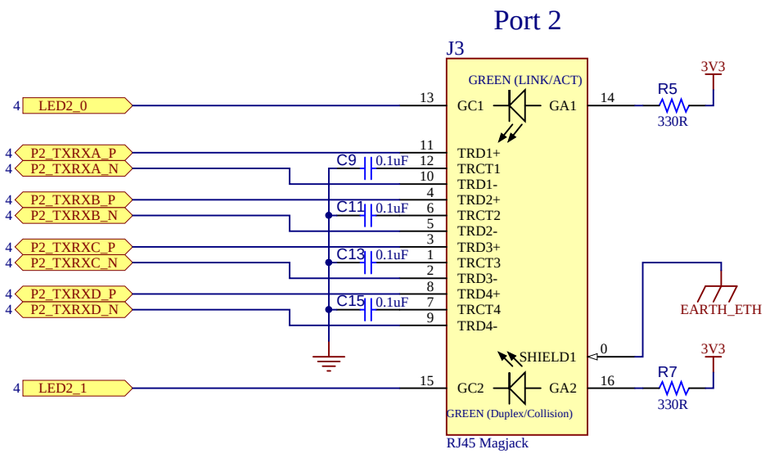
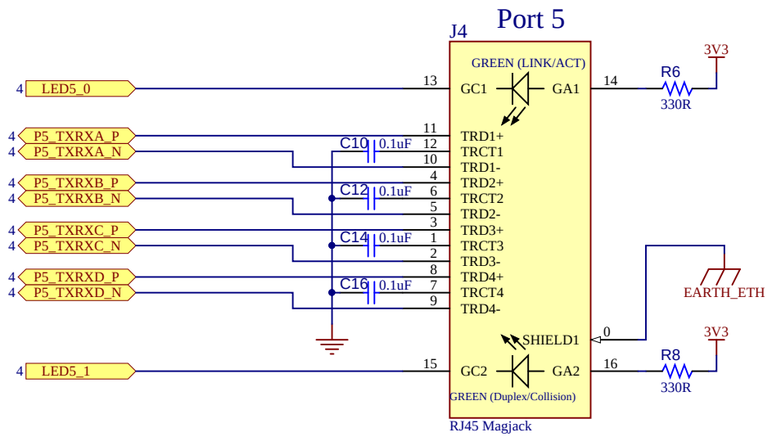
Description: KSZ9477 EVB_Demo Board with SAMA5D3 SoC
Page Title: KSZ9477, RGMII to SAMA5D3
Project Name: KSZ9477 EVB_Demo
PN: UNG_8071
Size: B
Date: 3/9/2017
Designer: Kelly Maas
Sheet 4 of 8
Rev B1



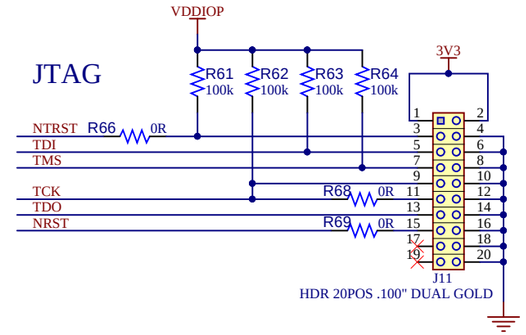


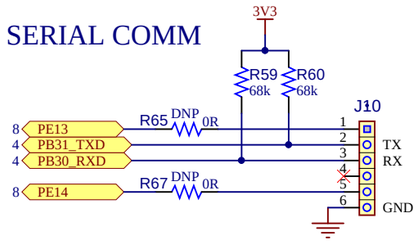




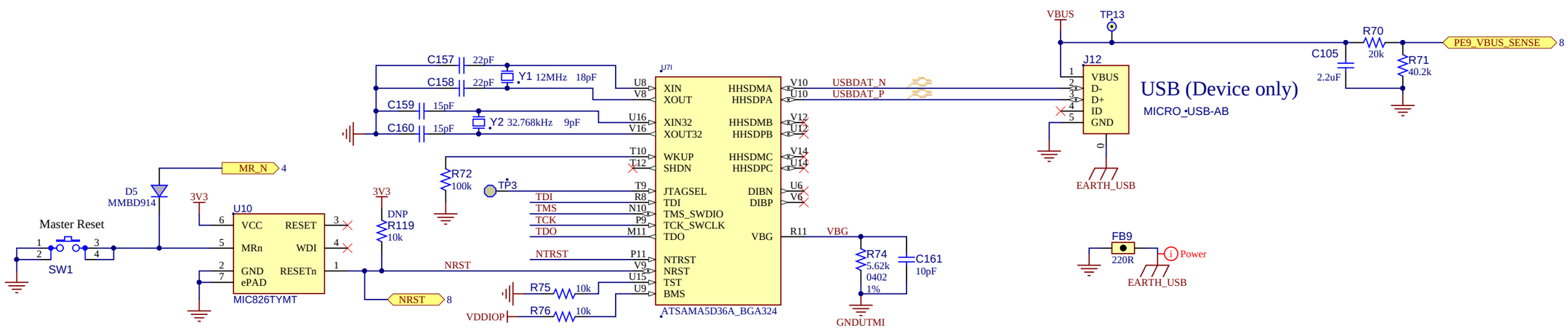


MICROCHIP	Microchip Technology, Inc. USB/Network Group - UNG www.Microchip.com	Designed with Altium Altium.com	
Description: KSZ9477 EVB_Demo Board with SAMA5D3 SoC			
Page Title: Ethernet ports and SGMII SFP			
Project Name: KSZ9477 EVB_Demo		PN: UNG_8071	
Size: B	Date: 2/16/2017	Designer: Kelly Maas	Sheet 5 of 8 Rev B1

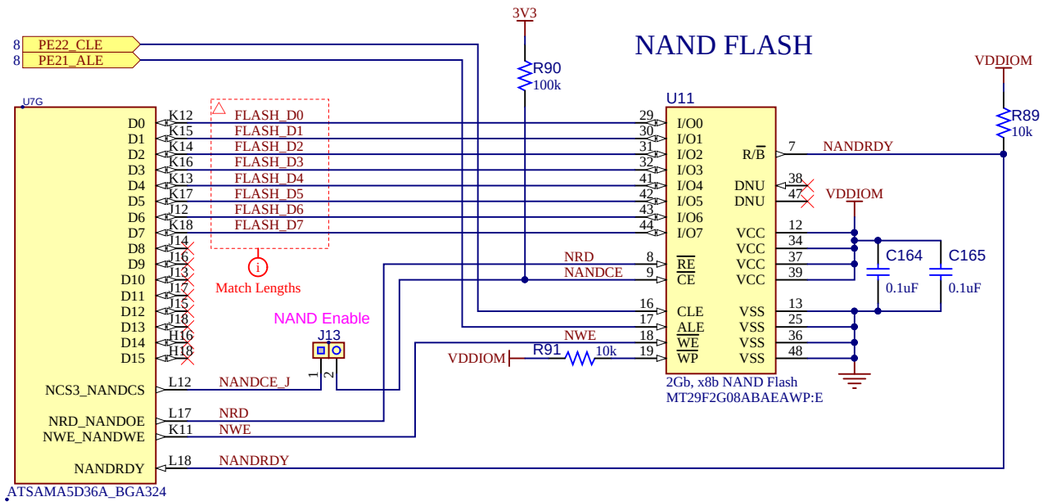


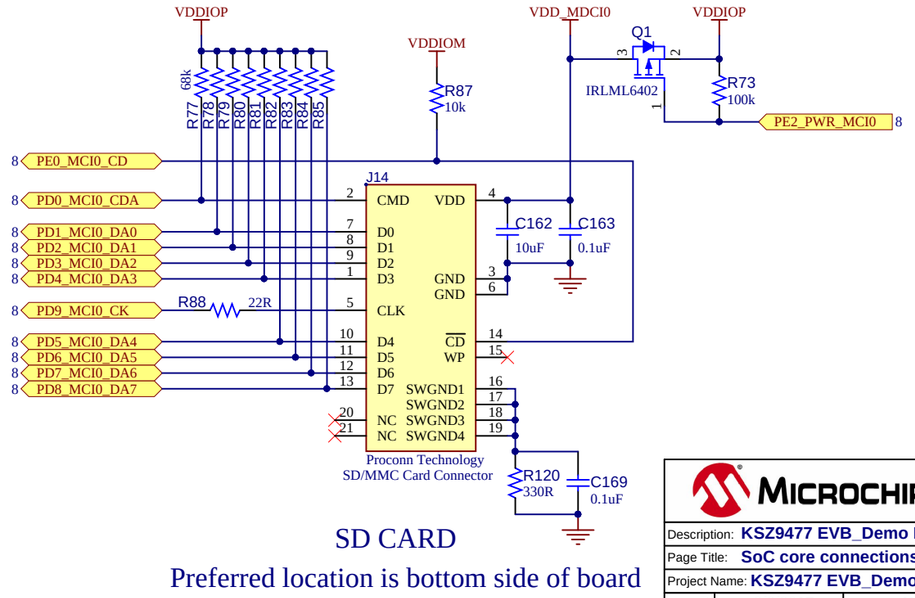


SAMA5D36 is not currently using pins 1 and 5 of J10



Reset / 200ms delay





SD CARD

Preferred location is bottom side of board

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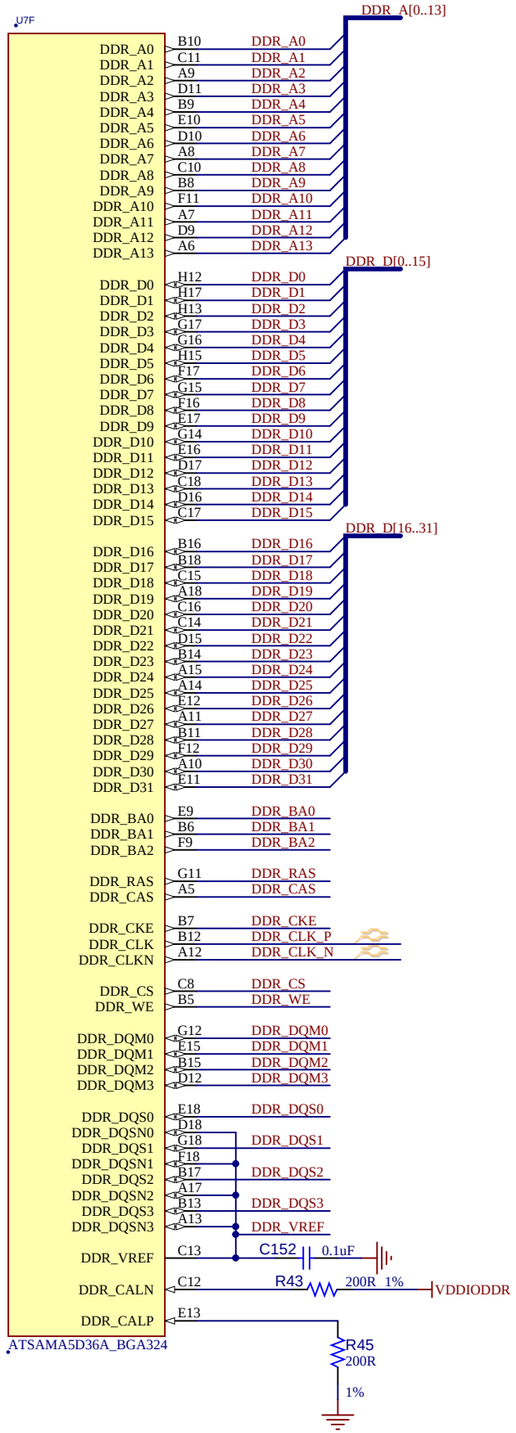
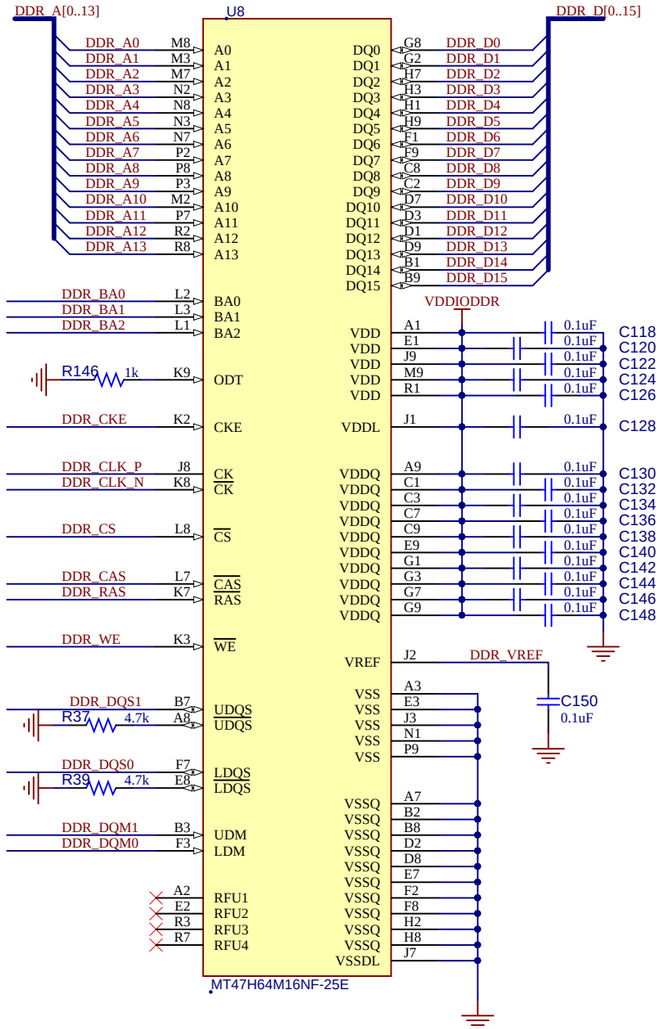
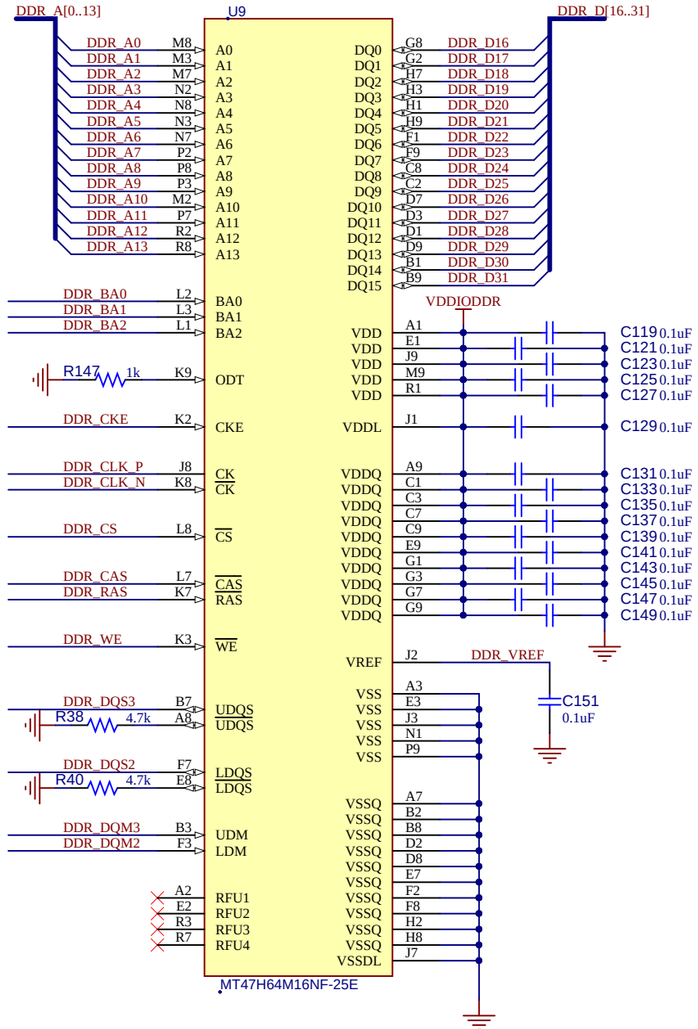
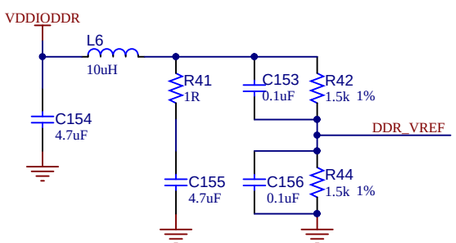
Description: KSZ9477 EVB_Demo Board with SAMA5D3 SoC	
Page Title: SoC core connections, NAND Flash, SD Card	
Project Name: KSZ9477 EVB_Demo	PN: UNG_8071
Size: B Date: 3/9/2017 Designer: Kelly Maas	Sheet 6 of 8 Rev B1

DDR2 SDRAM





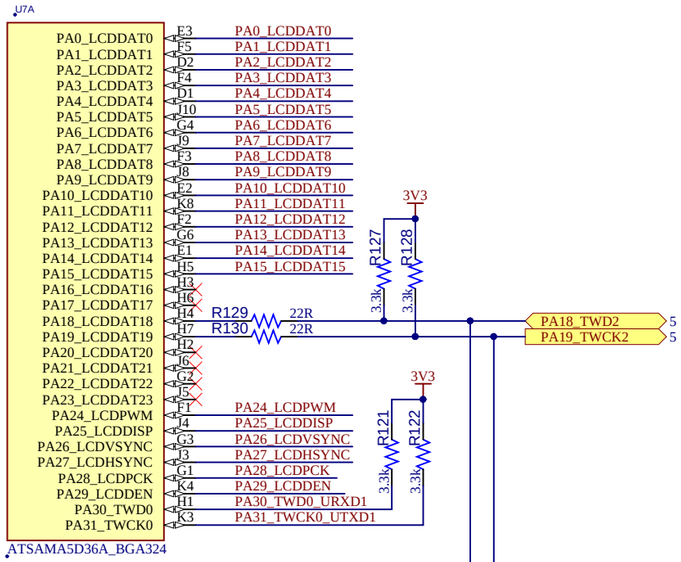


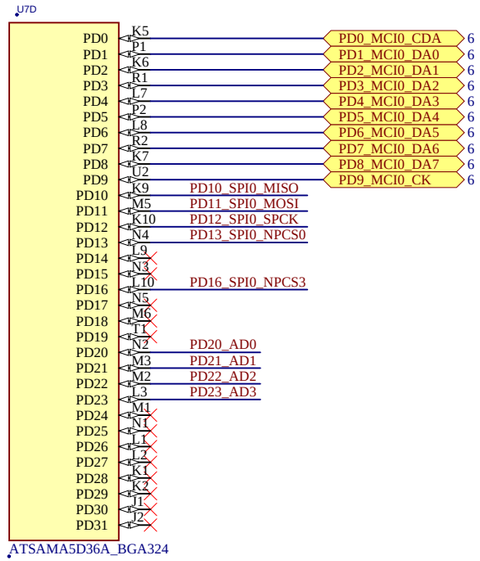


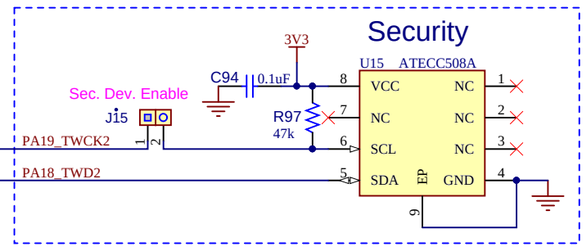
Keep nets as short as possible. Therefore DDR2 devices have to be placed as close as possible to SAMA5D3.
The layout EBI DDR2 should use controlled impedance traces of Z0= 50ohm.

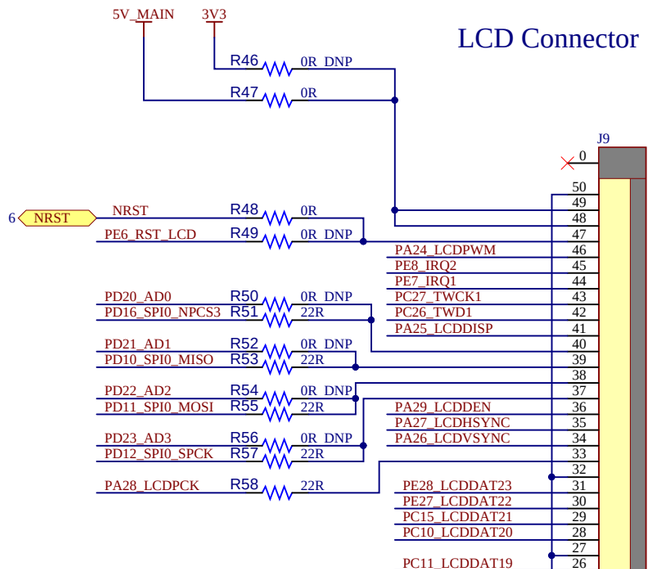
Address, control and data traces may not exceed 1.3 inches (33mm).
Address, control and data traces must be length matched to within 0.1 inch (2.54mm).
Address, control and data traces must match the data group trace lengths to within 0.25 inch (6.35mm).

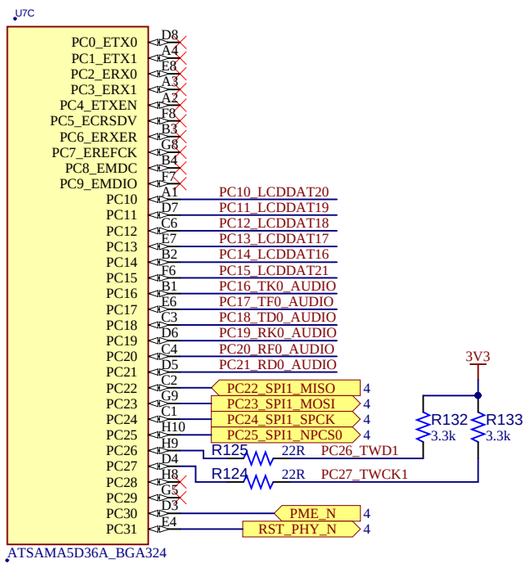
MICROCHIP	Microchip Technology, Inc. USB/Network Group - UNG www.Microchip.com	Designed with Altium Altium.com	
Description: KSZ9477 EVB_Demo Board with SAMA5D3 SoC			
Page Title: DDR2 SDRAM			
Project Name: KSZ9477 EVB_Demo		PN: UNG_8071	
Size: B	Date: 12/6/2016	Designer: Kelly Maas	Sheet 7 of 8 Rev B1

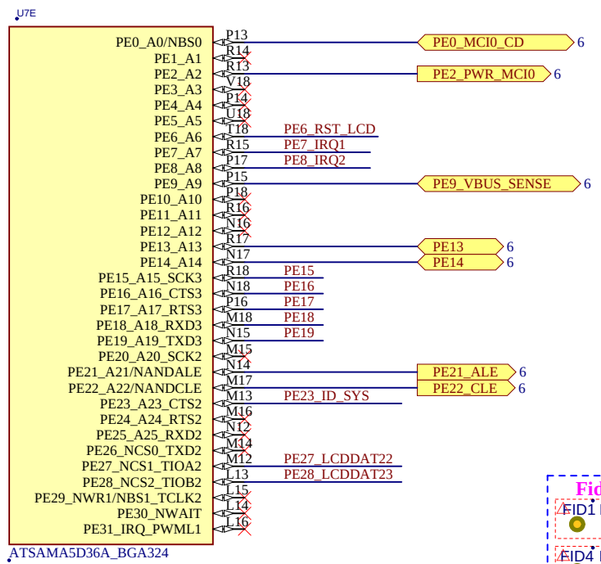


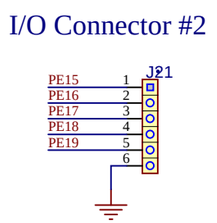


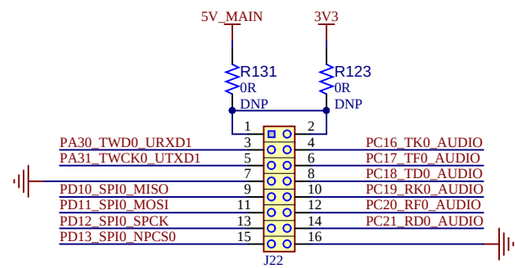


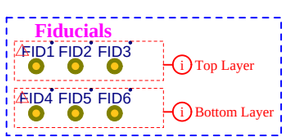


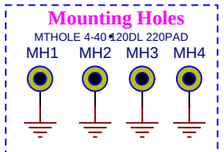












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Description:	KSZ9477 EVB_Demo Board with SAMA5D3 SoC		
Page Title:	SoC GPIO, LCD Connector, misc headers		
Project Name:	KSZ9477 EVB_Demo	PN:	UNG_8071
Size: B	Date: 12/9/2016	Designer: Kelly Maas	Sheet 8 of 8	Rev B1