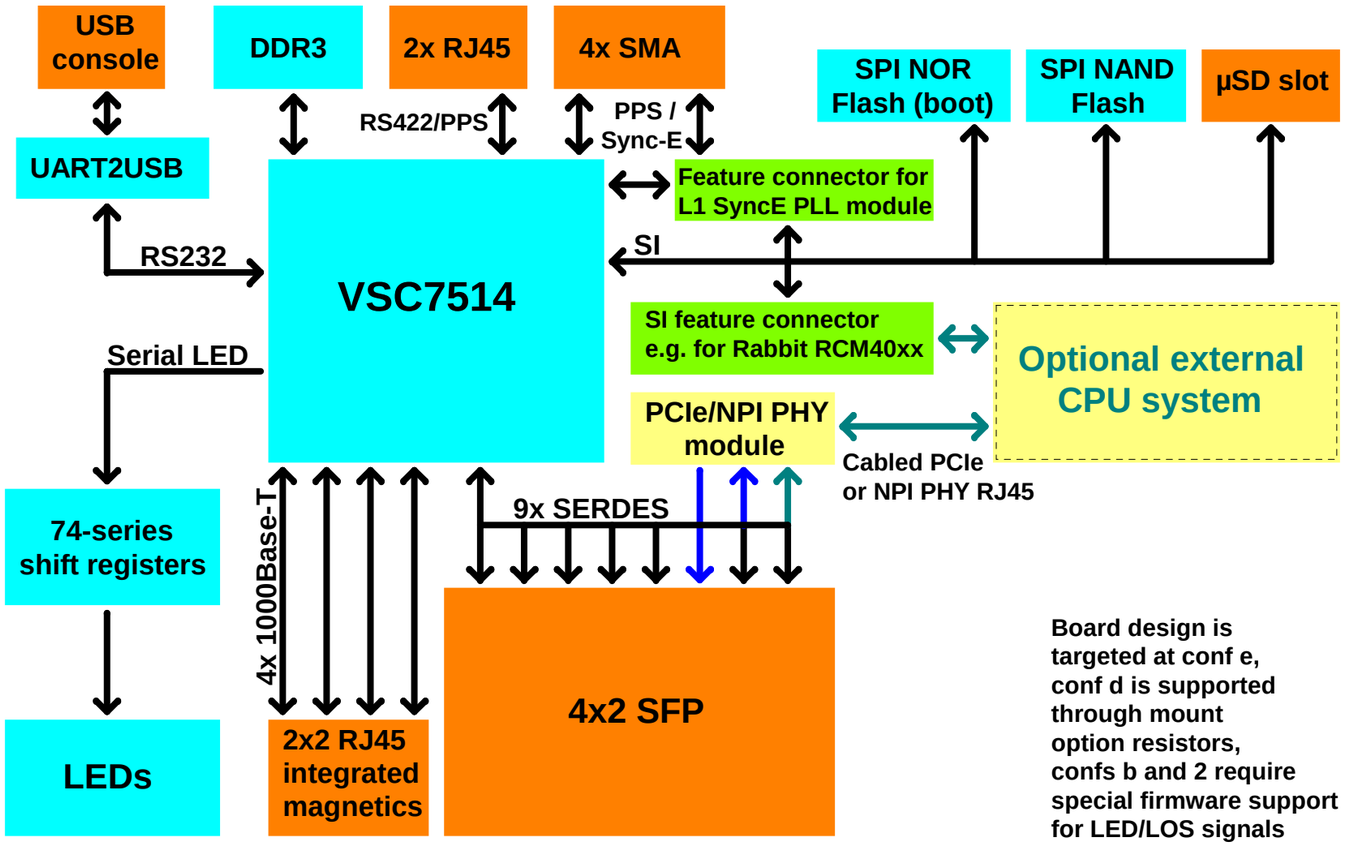
Block diagram of VSC7514 managed 10+1 port switch



Board design is targeted at conf e, conf d is supported through mount option resistors, confs b and 2 require special firmware support for LED/LOS signals

Table of contents

Revision history

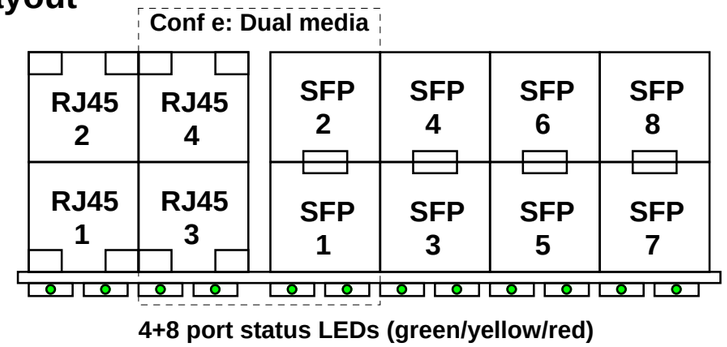
Version:	Date:	Author:	Main change(s):
01-00	2016-01-14	MAG	First release
01-01	2016-02-10	MAG	Swapped R1/R8 (2V5 LDO)
01-02	2016-05-24	MAG	Changes to U10 3V3/RESET, added R100/R101
01-03	2016-07-28	MAG	Added 2V8 Flash supply
02-00	2016-08-15	MAG	Changed VSC7514 reference clock input circuit

Port/SERDES/device mapping - per VSC7514 config...

PCIe/NPI	4x RJ45		8x SFP			
Conf e: S5 NPI PHY, S8 SFP6 Conf d: S8 PCIe, S5 SFP6 Conf b: S8 PCIe, S5 SFP6 Conf 2: S5 NPI PHY, S8 SFP6	Conf e: P3/D3 Conf d: P3/D3 Conf b: P3/D3 Conf 2: P3/D3	Conf e: P1/D1 Conf d: P1/D1 Conf b: P1/D1 Conf 2: P1/D1	Conf e: S1/D1 Conf d: S1/D5 Conf b: S1/D1 Conf 2: S1/D1	Conf e: S3/D6 Conf d: S3/D6 Conf b: S3/D3 Conf 2: S3/D3	Conf e: S8/D10 Conf d: S5/D10 Conf b: S5/D5 Conf 2: S8/D10	Conf e: S7/D8 Conf d: S7/D8 Conf b: S7/D8 Conf 2: S7/D8
	Conf e: P2/D2 Conf d: P2/D2 Conf b: P2/D2 Conf 2: P2/D2	Conf e: P0/D0 Conf d: P0/D0 Conf b: P0/D0 Conf 2: P0/D0	Conf e: S0/D0 Conf d: S0/D0 Conf b: S0/D0 Conf 2: S0/D0	Conf e: S2/D4 Conf d: S2/D4 Conf b: S2/D2 Conf 2: S2/D2	Conf e: S4/D9 Conf d: S4/D9 Conf b: S4/D4 Conf 2: S4/D4	Conf e: S6/D7 Conf d: S6/D7 Conf b: S6/D7 Conf 2: S6/D7

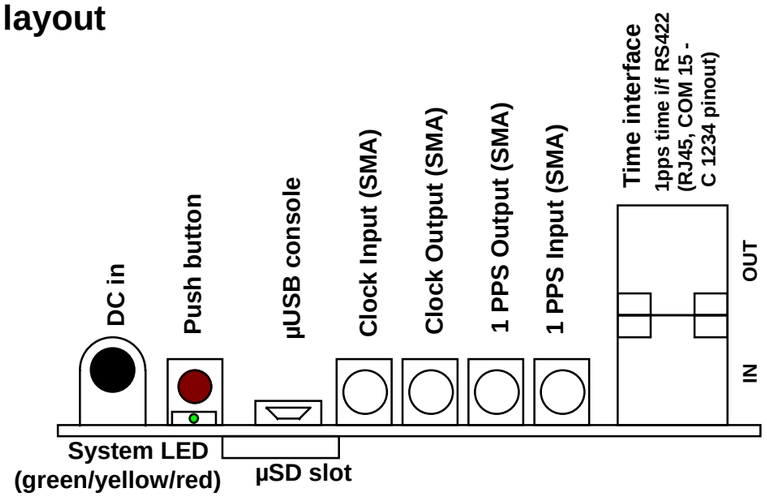
SLED/LOS												
LED: D2	LED: D3	LED: Gated D0	LED: Gated D1	LED: Gated D0 LOS: D0	LED: Gated D1 LOS: D1 (option for D5)	LED: D4 LOS: D4	LED: D6 LOS: D6	LED: D9 LOS: D9	LED: D10 LOS: D10	LED: D7 LOS: D7	LED: D8 LOS: D8

Front layout



4+8 port status LEDs (green/yellow/red)

Rear layout



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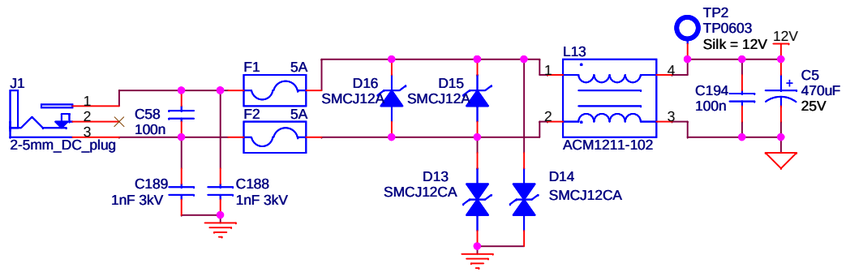
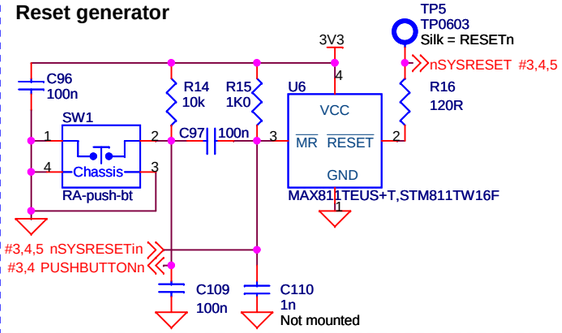
Title: Block diagram		
Size: A4	Document Number: PCB123	Rev: 02-00
Date: Tuesday, August 16, 2016	Sheet 1 of 6	

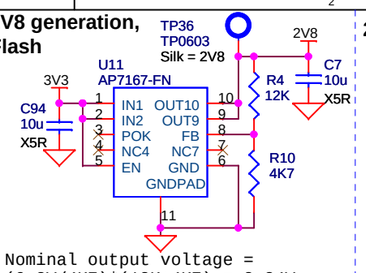
2.5mm center pin DC jack for external PSU



Reset generator

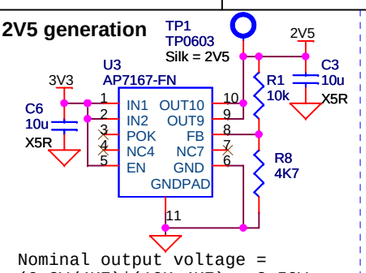


2V8 generation, Flash



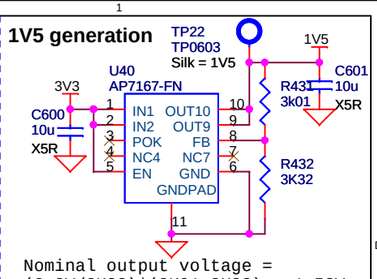
Nominal output voltage = (0.8V/4K7)*(12K+4K7) = 2.84V
Ambient temperature = 70*C,
current = 0.06A, Theta-JA = 40*C/W
=> junction temperature = 71*C

2V5 generation



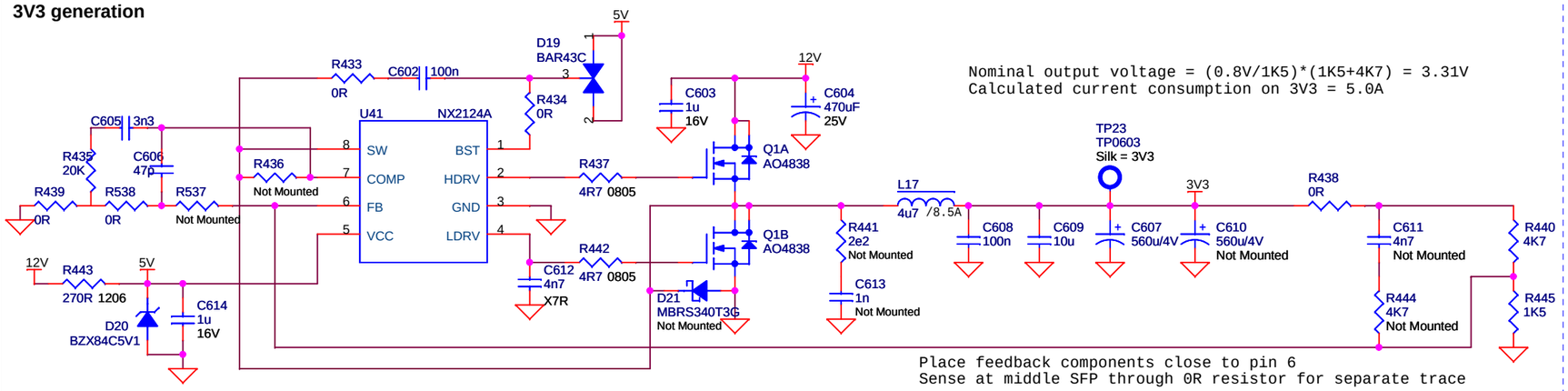
Nominal output voltage = (0.8V/4K7)*(10K+4K7) = 2.50V
Ambient temperature = 50*C,
current = 0.6A, Theta-JA = 40*C/W
=> junction temperature = 74*C

1V5 generation



Nominal output voltage = (0.8V/3K32)*(3K01+3K32) = 1.52V
Ambient temperature = 50*C,
current = 0.4A, Theta-JA = 40*C/W
=> junction temperature = 79*C

3V3 generation

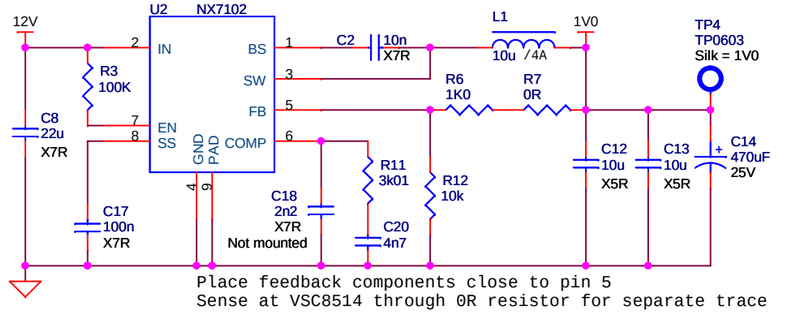


Nominal output voltage = (0.8V/1K5)*(1K5+4K7) = 3.31V
Calculated current consumption on 3V3 = 5.0A

Place feedback components close to pin 6
Sense at middle SFP through 0R resistor for separate trace

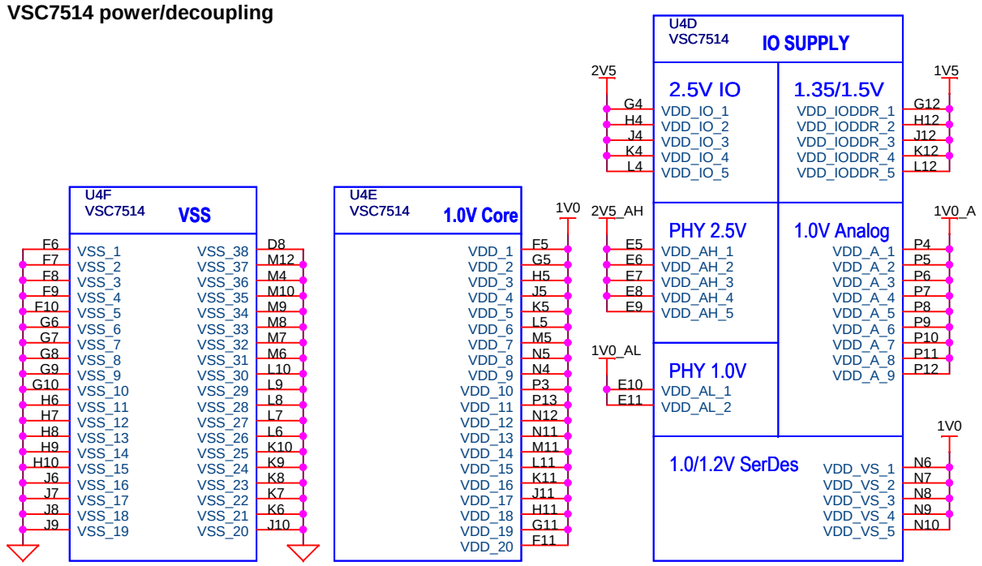
1V0 generation

Nominal output voltage = (0.925V/10K)*(1K+10K) = 1.02V
Calculated current consumption on 1V0 = 3.0A

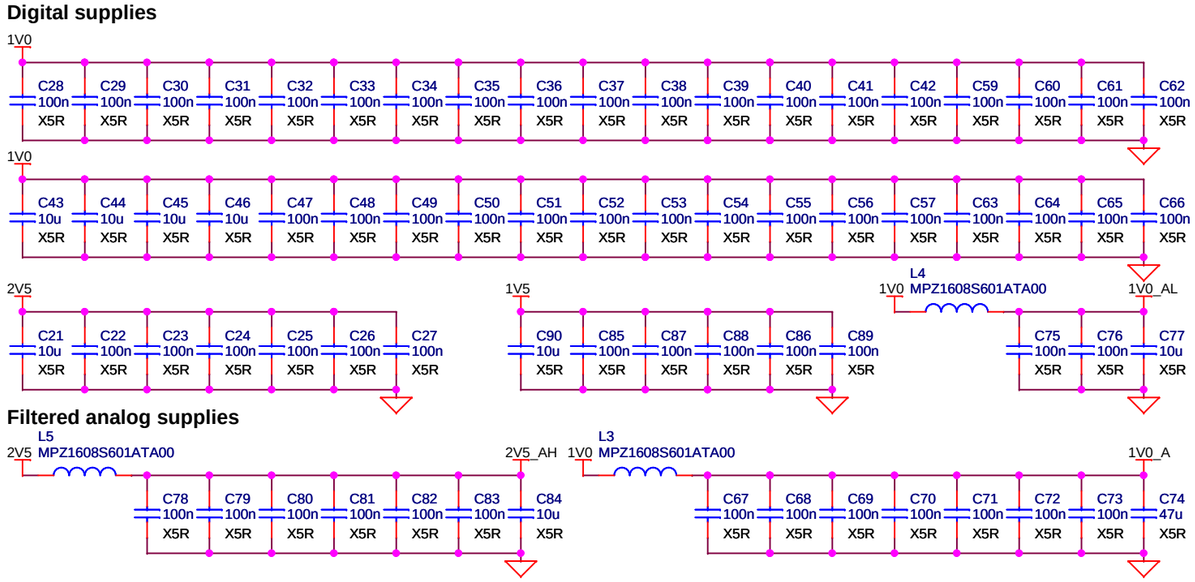


Place feedback components close to pin 5
Sense at VSC8514 through 0R resistor for separate trace

VSC7514 power/decoupling

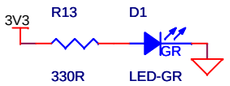


Digital supplies

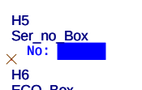


Filtered analog supplies

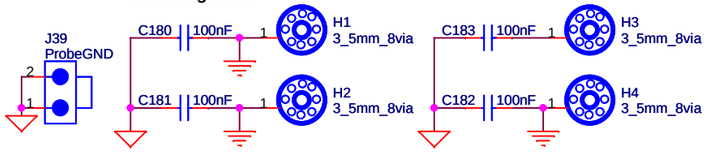
Power ON indicator



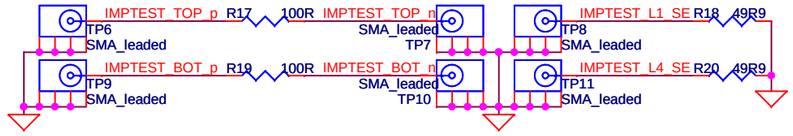
Silkscreen



Mounting holes



Impedance test traces



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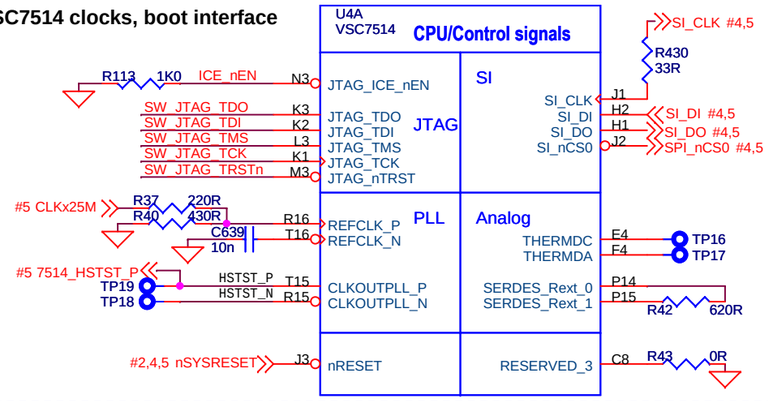
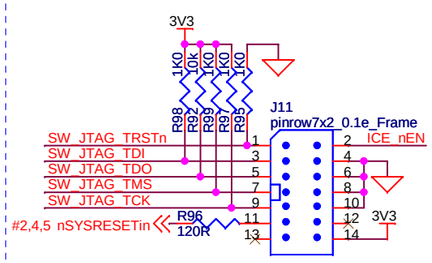
Title	Power inlet, voltage conversion, VSC7514 power/decoup, reset	
Size A3	Document Number PCB123	Rev 02-00
Date: Monday, August 15, 2016	Sheet 2 of 6	

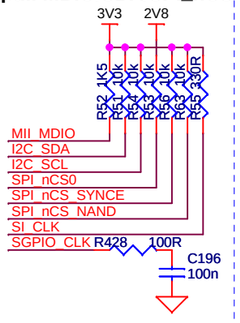
VSC7514 clocks, boot interface



VCore-III ICE / JTAG connector



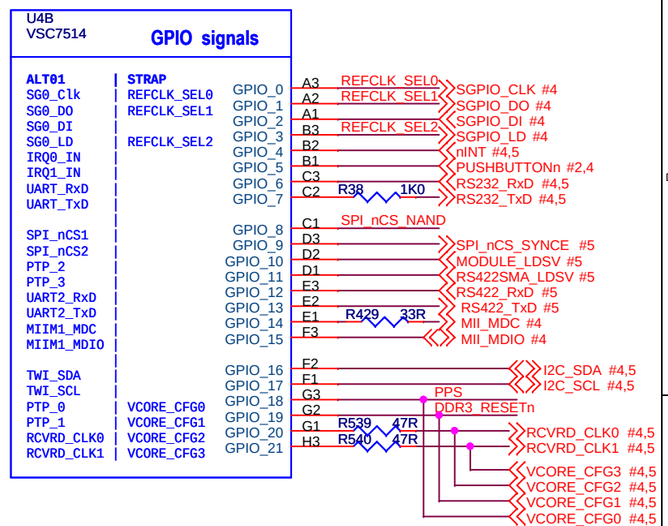
End termination of multidrop clocks, pull MDIO/SDA/SPI_nCS



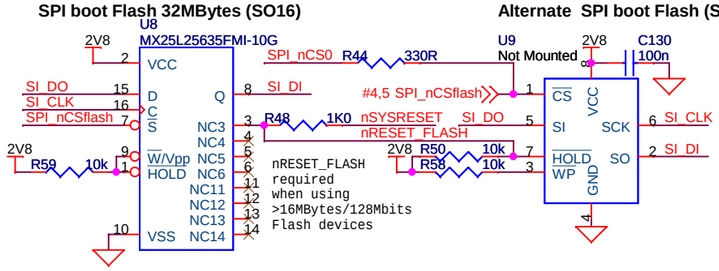
VSC7514 GPIO

VSC7514 GPIO alternate functions

GPIO #	ALT "10"	ALT "11"
0		
1		
2		
3		
4	IRQ0_OUT	TWI_SCL_MUX13
5	IRQ1_OUT	PCI_Wake
6	TWI_SCL_MUX0	
7	TWI_SCL_MUX1	
8	TWI_SCL_MUX2	IRQ0_OUT
9	TWI_SCL_MUX3	IRQ1_OUT
10	TWI_SCL_MUX4	SFP0_SD
11	TWI_SCL_MUX5	SFP1_SD
12	TWI_SCL_MUX6	SFP2_SD
13	TWI_SCL_MUX7	SFP3_SD
14	TWI_SCL_MUX8	SFP4_SD
15	TWI_SCL_MUX9	SFP5_SD
16		SPI_nCS3
17	TWI_SCL_MUX10	SPI_nCS4
18	TWI_SCL_MUX11_AD	
19	TWI_SCL_MUX12_AD	
20	TACHO	TWI_SCL_MUX14_AD
21	PWM	TWI_SCL_MUX15_AD

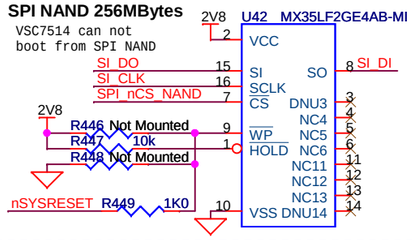


SPI boot Flash 32MBytes (SO16)

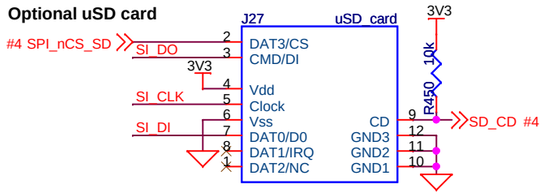


Alternate SPI boot Flash (SO8)

SPI NAND 256MBytes

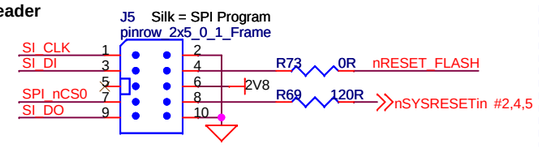


Optional uSD card



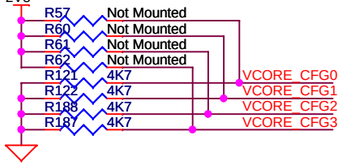
SPI boot Flash programming header

nSYSRESETin must be low during programming of SPI Flash, to output disable VSC7514 SI bus. nRESET_FLASH must be high during programming of SPI Flash, to enable SPI Flash which would otherwise be reset by nSYSRESET.



VSC7514 boot mode strapping

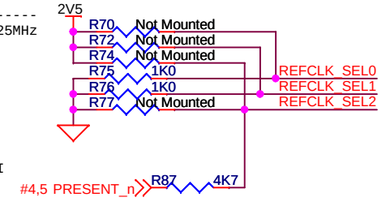
VCore_Cfg[3:0]	VCore-III CPU Behavior
==> 0 0 0 0	MIPS (or 8051 boots) from SI interface. The MIPS is Little Endian.
0 0 0 1	8051 IROM boot. Reserved for port-bringup.
0 0 1 0	8051 IROM boot. Reserved for port-bringup.
0 0 1 1	8051 IROM boot. Reserved for port-bringup.
0 1 0 0	8051 IROM boot. Reserved for port-bringup.
0 1 0 1	8051 IROM boot. Reserved for port-bringup.
0 1 1 0	8051 IROM boot. Reserved for port-bringup.
0 1 1 1	8051 IROM boot. Reserved for port-bringup.
1 0 0 0	8051 IROM boot. NPI:1G FDX NoFC, VRAP.
1 0 0 1	8051 IROM boot. PCIe
1 0 1 0	No boot. SI slave and MIIM slave @ address 0 (GPIO alternative).
1 0 1 1	No boot. SI slave and MIIM slave @ address 31 (GPIO alternative).
1 1 0 0	MIPS or 8051 boots from SI interface. The MIPS is Big Endian.
1 1 0 1	Reserved.
1 1 1 0	8051 boots from SI interface (the MIPS is disabled).
1 1 1 1	No boot. SI slave is enabled.



VSC7514 PLL strapping

REFCLK_SEL[2:0]	Frequency	Comment
SyncE => 0 0 0	125MHz	The default mode. Normal operation mode with 125MHz
0 0 1	156.25MHz	Normal operation mode with 156.25MHz ref clock
0 1 0	250MHz	Normal operation mode with 250MHz ref clock
0 1 1	N/A	Reserved
OCXO ==> 1 0 0	25MHz	Normal operation mode with 25MHz ref clock
1 0 1	N/A	Reserved
1 1 0	N/A	Reserved
1 1 1	N/A	Reserved

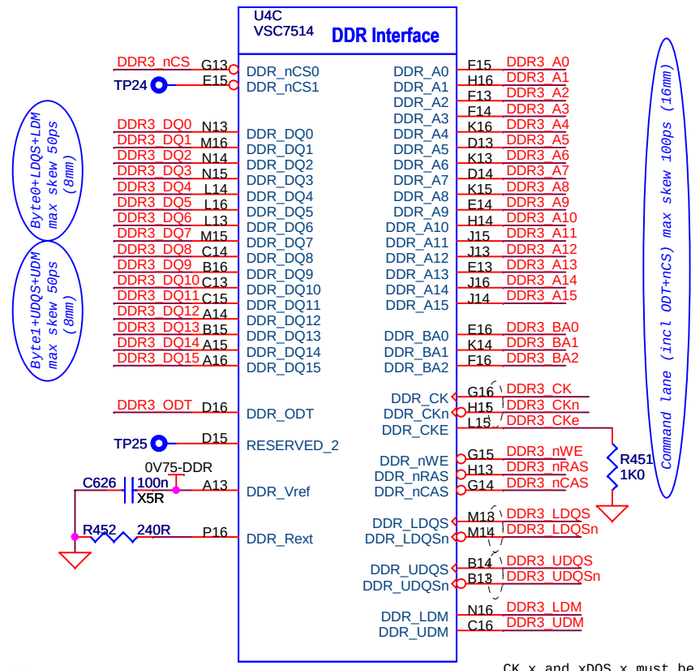
Due to VSC7514 jitter requirements, don't use 25MHz REFCLK as base for QSGMII



Board I2C address table

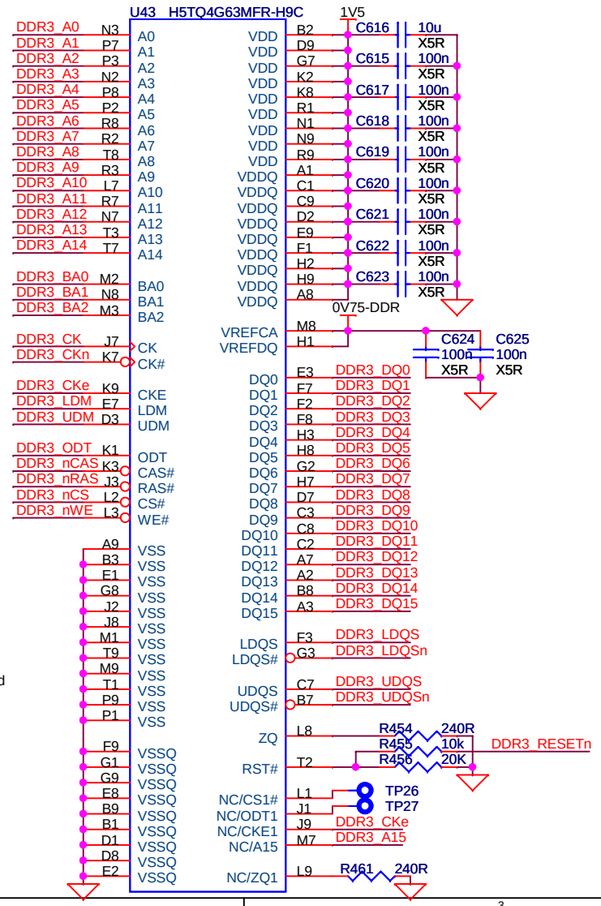
Address	I2C slave
1010xxx	SFP transceiver

VSC7514 DDR3 RAM Interface

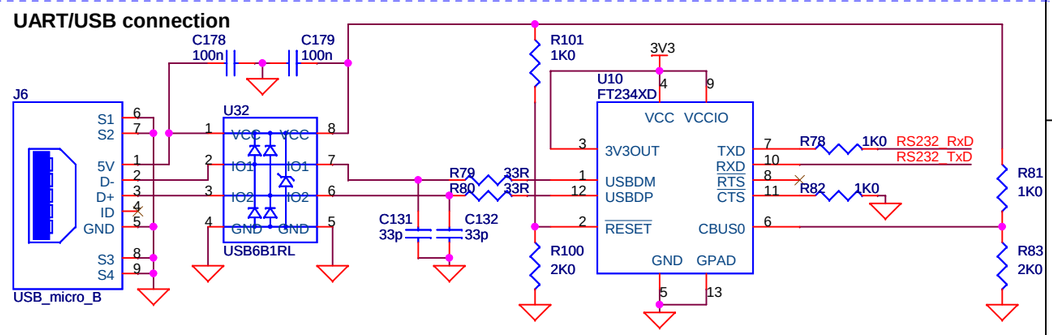


CK_x and xDQS_x must be routed as 100R differential pairs

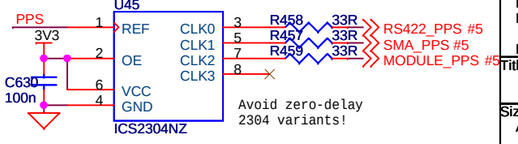
DDR3 RAM 256Mx16 (4Gbits/512MBytes)



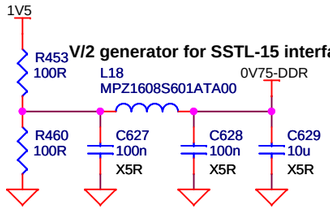
UART/USB connection



Fanout of 1PPS with tightly specified tpd



V/2 generator for SSTL-15 interface



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Title: VSC7514 memory (SPI boot Flash, DDR3, NAND), GPIO, strapping

Size	Document Number	Rev
A3	PCB123	02-00

Date: Tuesday, August 16, 2016 Sheet 3 of 6

VSC7514 ports

U4G VSC7514 — Dual Media

REF_FILT (B8), REF_Rext (A8); C140 1uF X5R; R149 2K0

Dual Media Fiber or copper Port 0: S0_TXP/S0_TXN, S0_RXP/S0_RXN, P0_D0P/N … P0_D3P/N

Dual Media Fiber or copper Port 1: S1_TXP/S1_TXN, S1_RXP/S1_RXN, P1_D0P/N … P1_D3P/N

TP20 F12 RESERVED_0; TP21 E12 RESERVED_1

U4H VSC7514 — Dual Media

Dual Media Fiber or copper Port 2: S2_TXP/S2_TXN, S2_RXP/S2_RXN, P2_D0P/N … P2_D3P/N

Dual Media Fiber or copper Port 3: S3_TXP/S3_TXN, S3_RXP/S3_RXN, P3_D0P/N … P3_D3P/N

U4I VSC7514 — SerDes

PORT 4 1G: S4_TXP/S4_TXN, S4_RXP/S4_RXN

PORT 5 1G: S5_TXP/S5_TXN, S5_RXP/S5_RXN

PORT 6 2.5G/QSGMII: S6_TXP/S6_TXN, S6_RXP/S6_RXN

PORT 7 2.5G: S7_TXP/S7_TXN, S7_RXP/S7_RXN

PORT 8 2.5G/PCIe: S8_TXP/S8_TXN, S8_RXP/S8_RXN

SERDES usage:
- 1Gbps: S0=SFP1, S1=SFP2, S2=SFP3, S3=SFP4, S4=SFP5
- 2.5Gbps: S6=SFP7, S7=SFP8
- Config e: S5 (1Gbps) connects to NPI on breakoff and S8 (2.5Gbps) connects to SFP6 through breakoff
- Config d: S5 (1Gbps) connects to SFP6 through breakoff and S8 (2.5Gbps) connects to PCIe on breakoff board

Connection to external CPU system through PCIe (and/or 2nd SFP connection, and/or NPI PHY)

J8 Samtec_QSE-020_Socket

S8_RXN, S8_RXP, S8_RTN; R104 49R9 PCIe_CLK_N; R107 49R9 PCIe_CLK_P; R108 Not Mounted; #3 MII_MDIO; #3 MII_MDC; #3,5 SI_DO; #3,5 SI_DI; #3,5 SI_CLK; #3,5 SPI_nCS0; #3,5 RS232_TxD; #3,5 RS232_RxD; #2,3,5 nSYSRESETin

SFP6_TxD_p/n, SFP6_RxD_p/n (to SFP6)

12V; CPRSNT#; CPURON; nSYSRESET #2,3,5; S8_TXN, S8_TXP; VCORE_CFG3 #3,5; VCORE_CFG2 #3,5; VCORE_CFG1 #3,5; VCORE_CFG0 #3,5; nINT #3,5; SPI_nCSflash #3,5; (was EXTCPUPRESENTn); S5_TXP, S5_TXN, S5_RXN, S5_RXP (from VSC7514)

MII_MDC was VCORE_CFG4 (future)
MII_MDIO was VCORE_CFG5 (future)
nINT_PHY was NPIMUXSEL
nSYSRESET was PCIeWAKE
S4_xxx was XCPU_A/B
SFP2_xxx was XCPU_C/D

RJ45[4:1]

Integrated magnetics

J28A Left, Down; J28B Left, Up; J28C; J28D — JXC0-0376NL

RTx1DN/DP/CN/CP/BN/BP/AN/AP, RTx2DN/DP/CN/CP/BN/BP/AN/AP, RTx3DN/DP/CN/CP/BN/BP/AN/AP, RTx4DN/DP/CN/CP/BN/BP/AN/AP

C642/C641, C651/C652, C661/C662, C675/C676 100n / 10n; 75 Ω; 1000pF, 3kV; 2x 0.1uF

TVS protection on 1000BASE-T signals

U16–U21 TVS3V3L4U

TVS protection on LED signals

#2,3 PUSHBUTTONn; U39 TVS3V3L4U; U34–U38 TVS3V3L4U; p11b1, p11b0, p9b1, p9b0, p7b1, p7b0, p4b1, p4b0, p2b1, p2b0, p0b1, p0b0 → p10b1, p10b0, p8b1, p8b0, p6b1, p6b0, p4b0, p3b1, p3b0, p1p5b1source, p1p5b0source

U55 TVS3V3L4U; LED_SEL_CU3, LED_SEL_CU4 → LED_SEL_SFP2, LED_SEL_SFP1

SFP[8:1]

J29A SFP_2x4 — SFP1_RxD_n/p, SFP1_TxD_p/n, I2C_SDA, SFP1_SCL, SFP1_TXFAULT, SFP1_TXDISABLE, SFP1_MODDETn, SFP1_RATESEL, SFP1_LOS; R462–R468 4K7; L19 LQH3C1R0M04L21; C631 100n, C632 100n, C633 10u, C634 100n

J29B SFP_2x4 — SFP2_RxD_n/p, SFP2_TxD_p/n, I2C_SDA, SFP2_SCL, SFP2_TXFAULT, SFP2_TXDISABLE, SFP2_MODDETn, SFP2_RATESEL, SFP2_LOS; R463–R469 4K7; L20 LQH3C1R0M04L22; C635 100n, C636 100n, C637 10u, C638 100n

J28E JXC0-0376NL

J29C SFP_2x4 — SFP3_RxD_n/p, SFP3_TxD_p/n, I2C_SDA, SFP3_SCL, SFP3_TXFAULT, SFP3_TXDISABLE, SFP3_MODDETn, SFP3_RATESEL, SFP3_LOS; R472–R476 4K7; L23 LQH3C1R0M04L25; C648 100n, C643 100n, C644 10u, C649 100n

J29D SFP_2x4 — SFP4_RxD_n/p, SFP4_TxD_p/n, I2C_SDA, SFP4_SCL, SFP4_TXFAULT, SFP4_TXDISABLE, SFP4_MODDETn, SFP4_RATESEL, SFP4_LOS; R473–R477 4K7; L24 LQH3C1R0M04L26; C650 100n, C645 100n, C646 10u, C647 100n

J29E SFP_2x4 — SFP5_RxD_n/p, SFP5_TxD_p/n, I2C_SDA, SFP5_SCL, SFP5_TXFAULT, SFP5_TXDISABLE, SFP5_MODDETn, SFP5_RATESEL, SFP5_LOS; R478–R484 4K7; L27 LQH3C1R0M04L29; C653 100n, C654 100n, C655 10u, C656 100n

J29F SFP_2x4 — SFP6_RxD_n/p, SFP6_TxD_p/n, I2C_SDA, SFP6_SCL, SFP6_TXFAULT, SFP6_TXDISABLE, SFP6_MODDETn, SFP6_RATESEL, SFP6_LOS; R479–R485 4K7; L28 LQH3C1R0M04L30; C657 100n, C658 100n, C659 10u, C660 100n

J29G SFP_2x4 — SFP7_RxD_n/p, SFP7_TxD_p/n, I2C_SDA, SFP7_SCL, SFP7_TXFAULT, SFP7_TXDISABLE, SFP7_MODDETn, SFP7_RATESEL, SFP7_LOS; R486–R492 4K7; L31 LQH3C1R0M04L33; C663 100n, C664 100n, C665 10u, C666 100n

J29H SFP_2x4 — SFP8_RxD_n/p, SFP8_TxD_p/n, I2C_SDA, SFP8_SCL, SFP8_TXFAULT, SFP8_TXDISABLE, SFP8_MODDETn, SFP8_RATESEL, SFP8_LOS; R487–R493 4K7; L32 LQH3C1R0M04L34; C667 100n, C668 100n, C669 10u, C670 100n

J29I SFP_2x4 — SHIELD_1 … SHIELD_54; C701 100nF X7R; C671–C674 100nF X7R

Serial GPIO inputs

SILK = VSC7514 Config d: SFP2_LOS R494 Not Mounted P5B0_IN; SILK = VSC7514 Config e: #3 SD_CD R496 0R; SD_CD R495 Not Mounted P1B0_IN; SFP2_LOS R497 0R

U47 74HC165 — SFP8_TXFAULT, SFP7_TXFAULT, SFP6_TXFAULT, SFP6_MODDETn, SFP6_LOS, SFP5_MODDETn, SFP5_LOS, SFP8_MODDETn, SFP8_LOS; #3 SGPIO_CLK, #3 SGPIO_LD

U46 74HC165 — SFP7_MODDETn, SFP7_LOS, SFP4_MODDETn, SFP4_LOS, SFP5_TXFAULT, P5B0_IN, SFP3_MODDETn, SFP3_LOS; SGPIO_CLK, SGPIO_LD

U48 74HC165 — SFP4_TXFAULT, SFP3_TXFAULT, SFP2_TXFAULT, SFP1_TXFAULT, SFP2_MODDETn, P1B0_IN, SFP1_MODDETn, SFP1_LOS; SGPIO_CLK, SGPIO_LD; SGPIO_DI #3

Serial GPIO outputs

U51 74AHC594 — SLED_DO, SGPIO_LD, SGPIO_CLK, nSYSRESET; p12b0 R488 180R LED_SEL_CU3; p12b1 R489 180R LED_SEL_CU4; p13b0 MUX_SEL0; p13b1 MUX_SEL1; p14b0 MUX_SEL2; p14b1 SPI_CS_SD; p15b0 RS422_SLVOE; p15b1 RS422_MSTOE

U52 74AHC594 — p16b0 SFP1_RATESEL, p16b1 SFP2_RATESEL, p17b0 SFP3_RATESEL, p17b1 SFP4_RATESEL, p18b0 SFP5_RATESEL, p18b1 SFP6_RATESEL, p19b0 SFP7_RATESEL, p19b1 SFP8_RATESEL

U53 74AHC594 — p20b0 SFP1_TXDISn, p20b1 SFP2_TXDISn, p21b0 SFP3_TXDISn, p21b1 SFP4_TXDISn, p22b0 SFP5_TXDISn, p22b1 SFP6_TXDISn, p23b0 SFP7_TXDISn, p23b1 SFP8_TXDISn

As '594 resets low and SFP TXDISABLE input is active high, inverting '240 buffers required to output disable SFPs during reset

U50 74HC240 — SFP1_TXDISABLE … SFP8_TXDISABLE

Serial LED outputs

#3 SGPIO_DO; U12/U13/U14 74HC164PW

SILK = VSC7514 Config e: p1p5b0source R500 180R p1p5b0; p1p5b1source R501 180R p1p5b1

R505/R507 SILK = VSC7514 Config d: R502 320R p4b0; R503 320R p4b1; R505 Not Mounted p1p5b0; R507 Not Mounted p1p5b1; R504 320R p6b0; R506 320R p6b1; R508 320R p7b0; R509 320R p7b1

RP4A 180R p0b0; RP4B 180R p0b1; RP4C 180R p1b0; RP4D 180R p1b1; RP5A 320R p2b0; RP5B 320R p2b1; RP5C 320R p3b0; RP5D 320R p3b1; RP8A 320R p8b0; RP8B 320R p8b1; RP8C 320R p9b0; RP8D 320R p9b1; RP9A 320R p10b0; RP9B 320R p10b1; RP9C 320R p11b0; RP9D 320R p11b1; SLED_DO

nSYSRESET, SGPIO_CLK

Some signals need to be high during reset but '594 resets low, hence inverting '240 buffers

p12b0, p12b1, RS422_SLVOE, RS422_MSTOE, SPI_CS_SD, #3,5 PRESENT_n

U54 74HC240 — R510 180R LED_SEL_SFP1; R511 180R LED_SEL_SFP2; SILK = VSC7514 Config e: RS422_1588_SLVOEn #5; RS422_1588_MSTOEn #5; SPI_nCS_SD #3; PRESENT #5

C677–C685 100n

Port status LEDs

SILK = VSC7514 Config d: R508 Not Mounted

RJ45#2/P3/D3: p3b0, p3b1, D2 LTST-S326 Green/Red
RJ45#1/P2/D2: p2b0, p2b1, D6 LTST-S326 Green/Red
RJ45#4/P1/D1: p1b0, p1b1, D9 LTST-S326 Green/Red
RJ45#3/P0/D0: p0b0, p0b1, D3 LTST-S326 Green/Red
SFP3/S2/D4: p4b0, p4b1, D8 LTST-S326 Green/Red
SFP2/S1/(config e:D7 config d:D5): p1p5b0, p1p5b1, D7 LTST-S326 Green/Red
SFP1/S0/D0: p0b0, p0b1, D10 LTST-S326 Green/Red
SFP4/S3/D6: p6b0, p6b1, D4 LTST-S326 Green/Red
SFP5/S4/D9: p9b0, p9b1, D11 LTST-S326 Green/Red
SFP6/(config e:S8/ config d:S5)/D10: p10b0, p10b1, D11 LTST-S326 Green/Red
SFP7/S8/D7: p7b0, p7b1, D23 LTST-S326 Green/Red
SFP8/S7/D8: p8b0, p8b1, D22 LTST-S326 Green/Red

System status LED

p11b0, p11b1, D12 LTST-S326 Green/Red

Enable SLED ports 10:0 as port status LEDs (see note on LED for details...) and SLED port 11 as system status LED.
Enable two bits per port, bit[1:0]=00 => yellow, 01 => red, 10 => green, 11 => off.
Enable SGPIO output ports 23:12 as LED_SEL_x (dual-media), MUX_SELx (I2C), RS422_x0E (IEEE1588 RS422), SFP control signals
Use SGPIO input ports 12:0 as SFP control signals and CardDetect from uSD slot.

I2C MUXing

U49 74HC4051 — MUX_SEL0, MUX_SEL1, MUX_SEL2; I2C_SDA, I2C_SDA #3,5; I2C_SCL #3,5; SFP1_SCL … SFP8_SCL

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Title: Ethernet ports, SGPIO, LEDs

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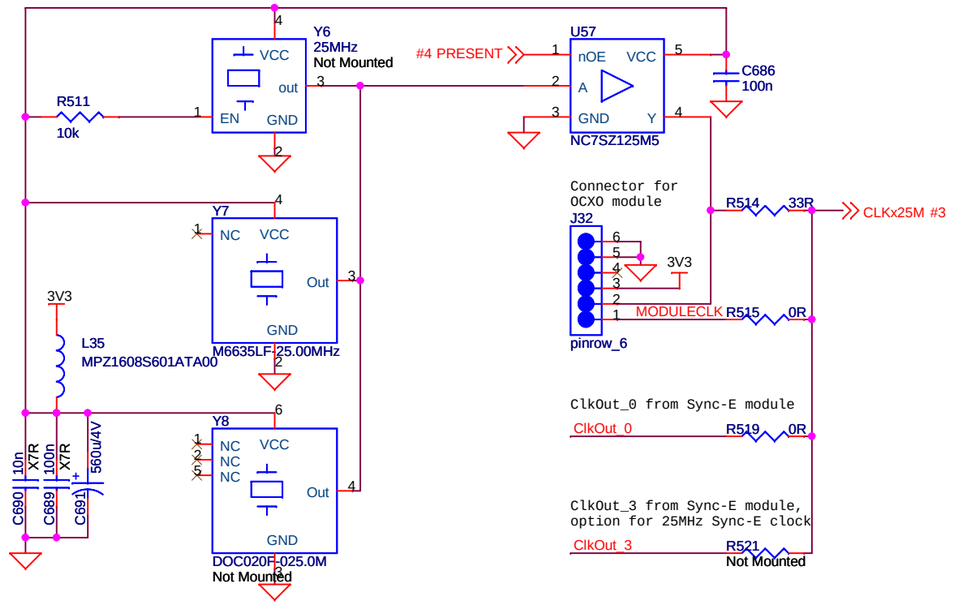
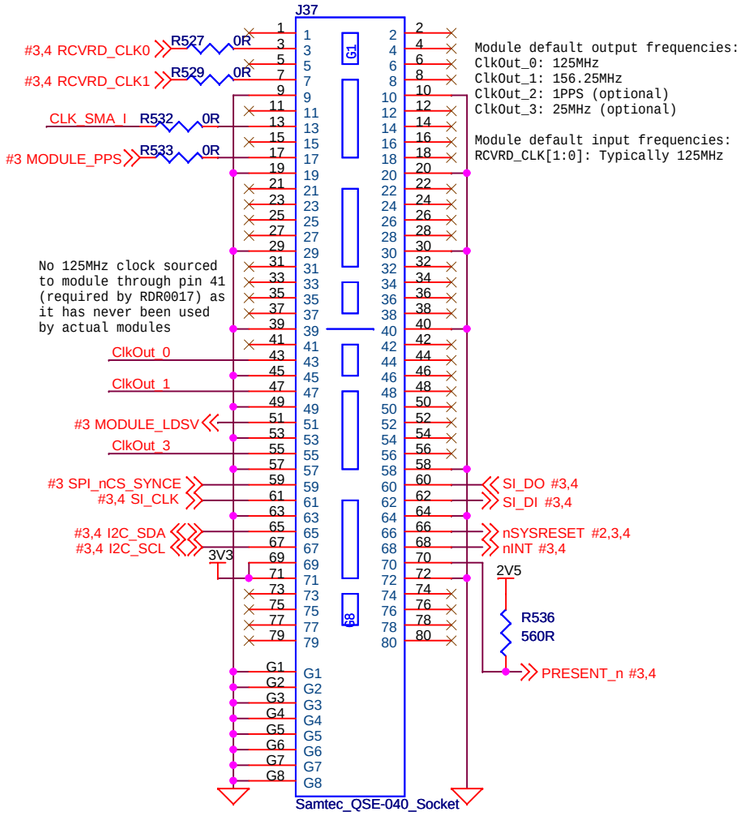
A fine selection of (VC)OCXOs and plain oscillator - mount only one at a time

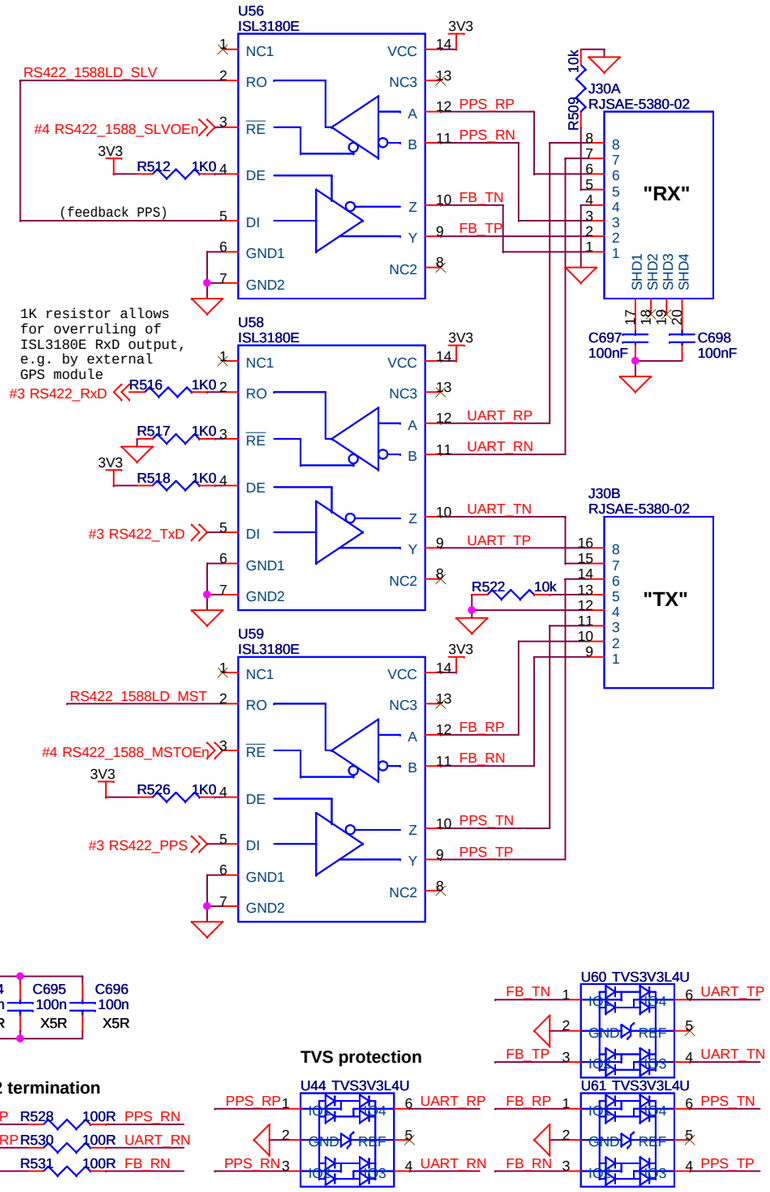


Buffering/enabling of OCXO-sourced 25MHz clock - or entry path for 25MHz clock from OCXO module - or entry path for 125MHz clock from Sync-E module

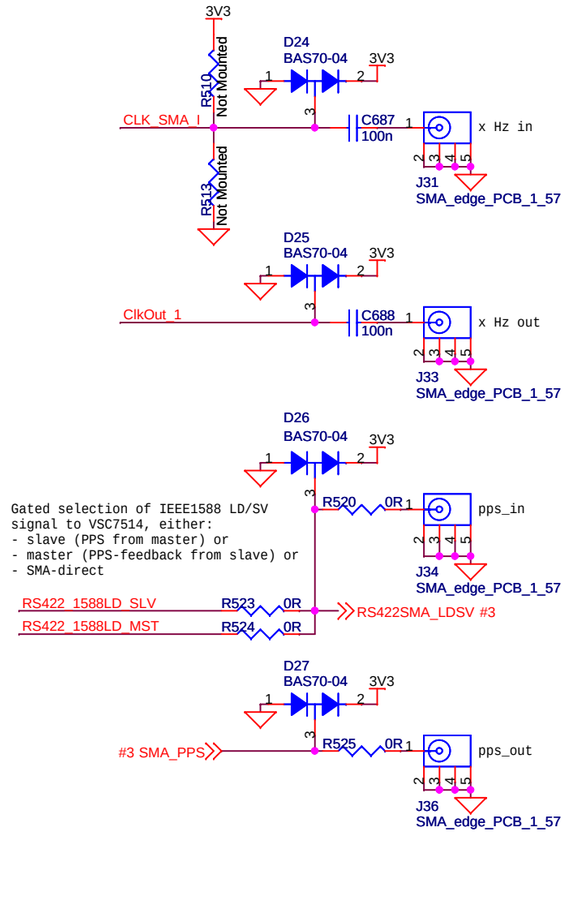
Sync-E feature connector (for Sync-E add-on module as specified in RDR0017)



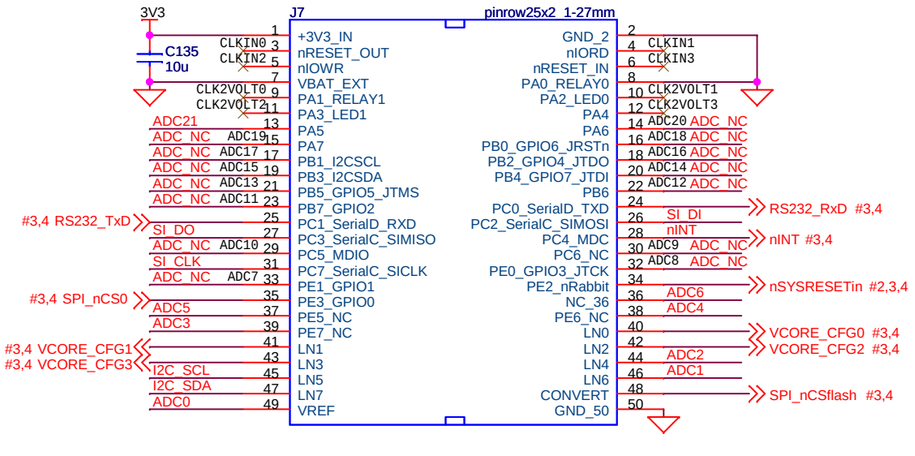
1PPS Time Interface - RS422, RJ45 G.703 pinout



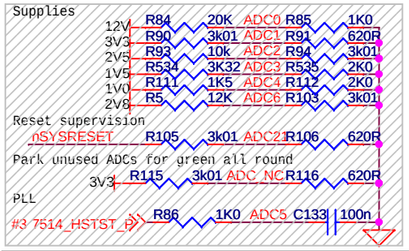
SMA I/O for Synchronization



Optional receptacle for Rabbit RCM40xx CPU module (for connecting external CPU to VSC7514 SI)



Rabbit connector has double duty as connector for Microsemi QuickTest module, enabling test of selected PCB signals (definitely optional!). ADC nominal input voltage 0.57V.



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Title: Clock, IEEE1588, Sync-E

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A3	PCB123	02-00

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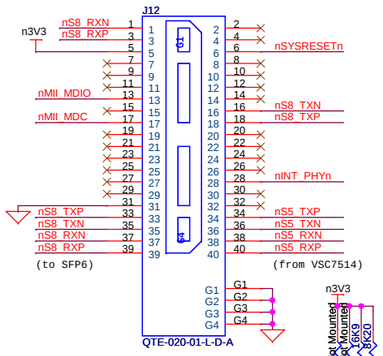
Breakoff board for connecting NPI PHY to mainboard S5 (SFP6 is 2.5Gbps S8)

Samtec connector towards mainboard, feedthrough of S8 to SFP6

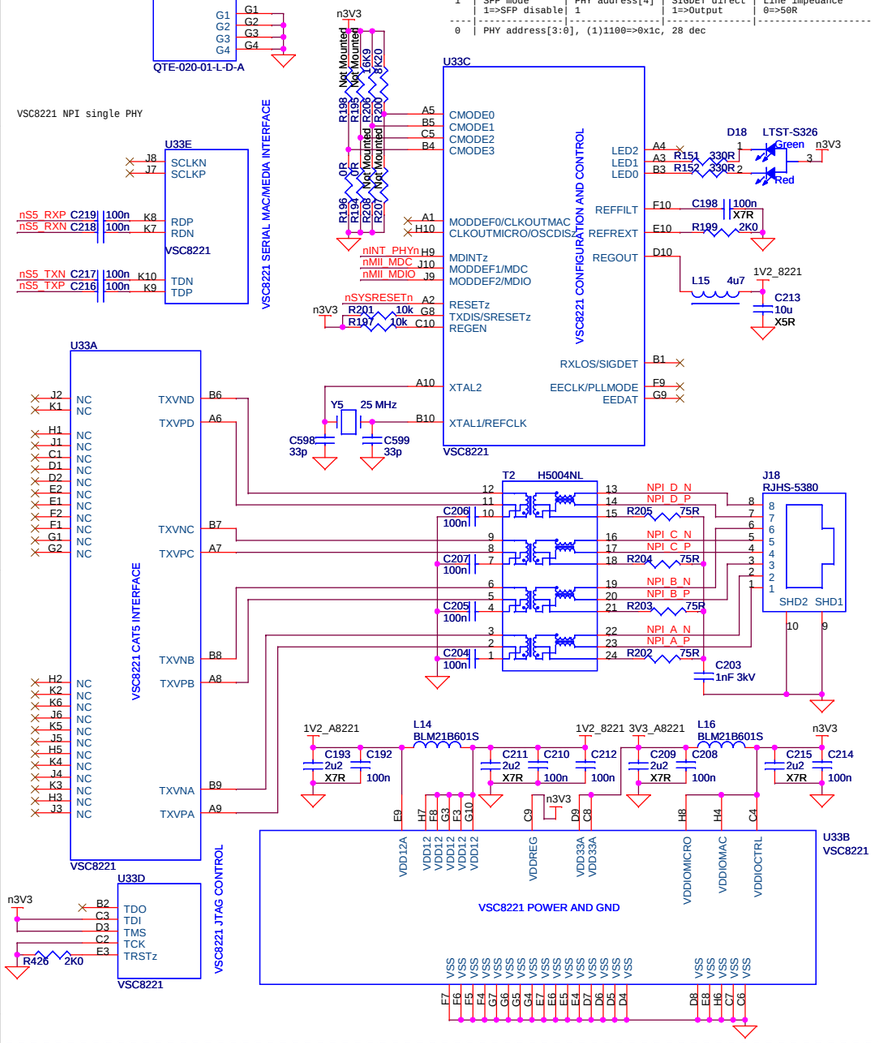


CMODE pull-up/pull-down to digital translation

With CMODE pin tied to	. with 1% . res val	Set bit| 3 to:	Set bit| 2 to:	Set bit| 1 to:	Set bit| 0 to:
GND	0	0	0	0	0
GND	2.26k	0	0	0	1
GND	4.02k	0	0	1	0
GND	5.90k	0	0	1	1
GND	8.25k	0	1	0	0
GND	12.1k	0	1	0	1
GND	16.9k	0	1	1	0
GND	22.6k	0	1	1	1
3V3	0	1	0	0	0
3V3	2.26k	1	0	0	1
3V3	4.02k	1	0	1	0
3V3	5.90k	1	0	1	1
3V3	8.25k	1	1	0	0
3V3	12.1k	1	1	0	1
3V3	16.9k	1	1	1	0
3V3	22.6k	1	1	1	1

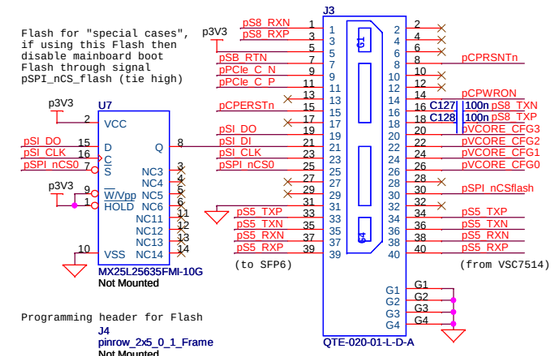
VSC8221 CMODE strapping

Pin	Bit 3 control	Bit 2 control	Bit 1 control	Bit 0 (LSB) control
3	LED control[1]| 0=>link/act	SQE enable| 0=>SQE disabled	Reserved| -	Autoneg ctrl[1]| 0=>10/100/10000base
2	Operating mode[3:0], 0000=>SERDES to CAT5, SCLK disabled			
1	SFP mode| 1=>SFP disable	PHY address[4]| 1	SIGDET direct| 1=>Output	Line impedance| 0=>50R
0	PHY address[3:0], (1)1100=>0x1c, 28 dec			



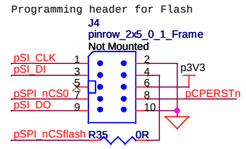
Breakoff board for connecting PCIe cable to mainboard S8 (SFP6 is 1Gbps S5)

Samtec connector towards mainboard, feedthrough of S5 to SFP6

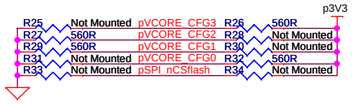


Flash for "special cases", if using this Flash then disable mainboard boot Flash through signal pSPI_nCS_flash (tie high)

Programming header for Flash

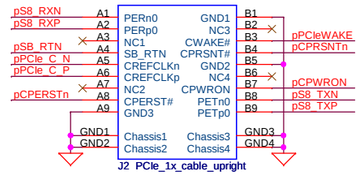


Override VCORE_CFG of mainboard, for plug&play PCIe



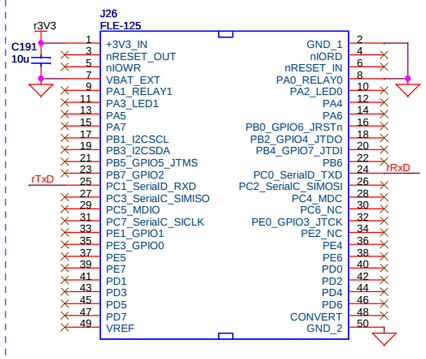
No PCIeWAKE from this mainboard (use in-band beacon instead)

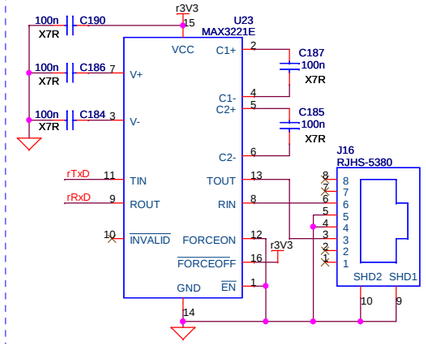
PCIe 1x cable connector for S8 from mainboard



Note, PCIe interface for use in controlled lab environment, so
(1) no power domain isolation,
(2) high-impedance when powered off not guaranteed for CWAKE#, CPRSNT#, CPERST#,
(3) spread spectrum clocked PCIe hosts not supported

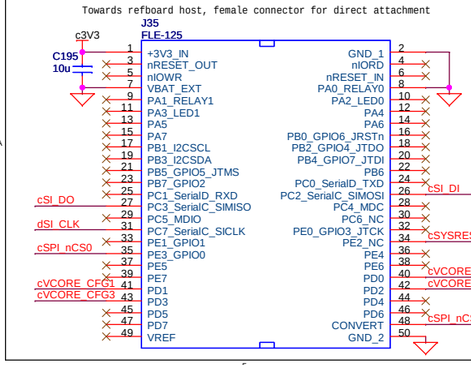
Breakoff board with RS232 port for old-school management



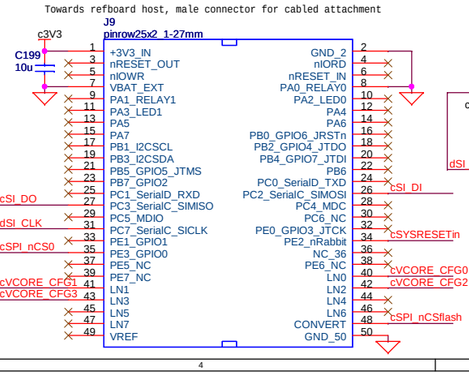


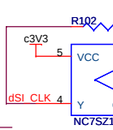
Breakoff board with connectors for a Rabbit/BeagleBone (use only one at a time!) external CPU module as master towards a refboard strapped as SI slave

Towards refboard host, female connector for direct attachment

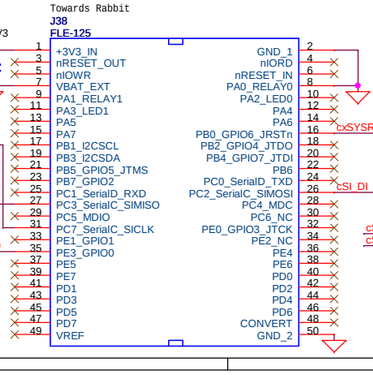


Towards refboard host, male connector for cabled attachment

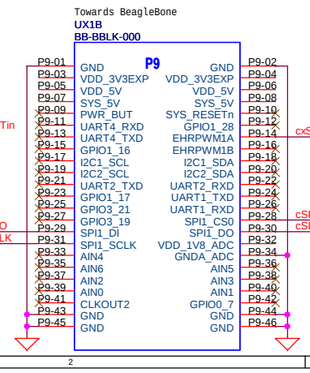




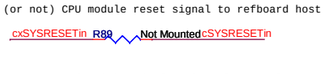
Towards Rabbit



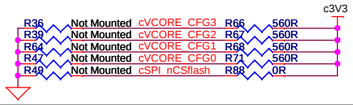
Towards BeagleBone



Transfer (or not) CPU module reset signal to refboard host



Override VCORE_CFG of mainboard, for plug&play SI slave



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Title: Breakoffs for PCIe, NPI PHY and 6th SFP source selection - and RS232

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