

Block diagram of VSC7514 managed 10+1 port switch

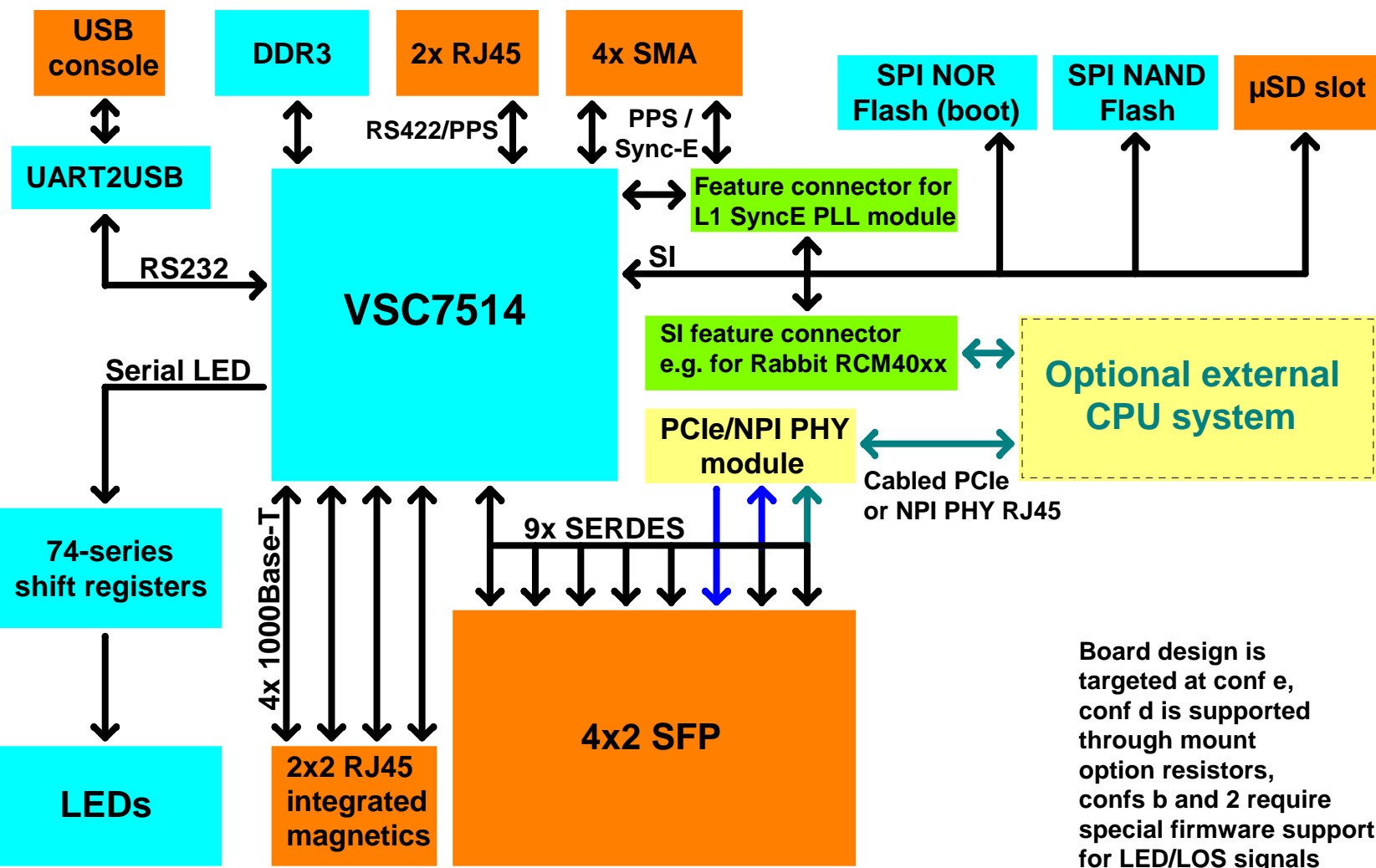


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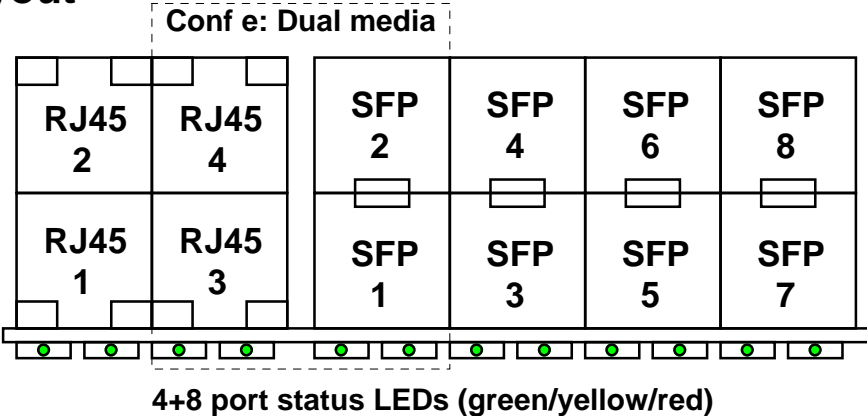
Revision history

Version:	Date:	Author:	Main change(s):
01-00	2016-01-14	MAG	First release
01-01	2016-02-10	MAG	Swapped R1/R8 (2V5 LDO)
01-02	2016-05-24	MAG	Changes to U10 3V3/RESET, added R100/R101
01-03	2016-07-28	MAG	Added 2V8 Flash supply
02-00	2016-08-15	MAG	Changed VSC7514 reference clock input circuit

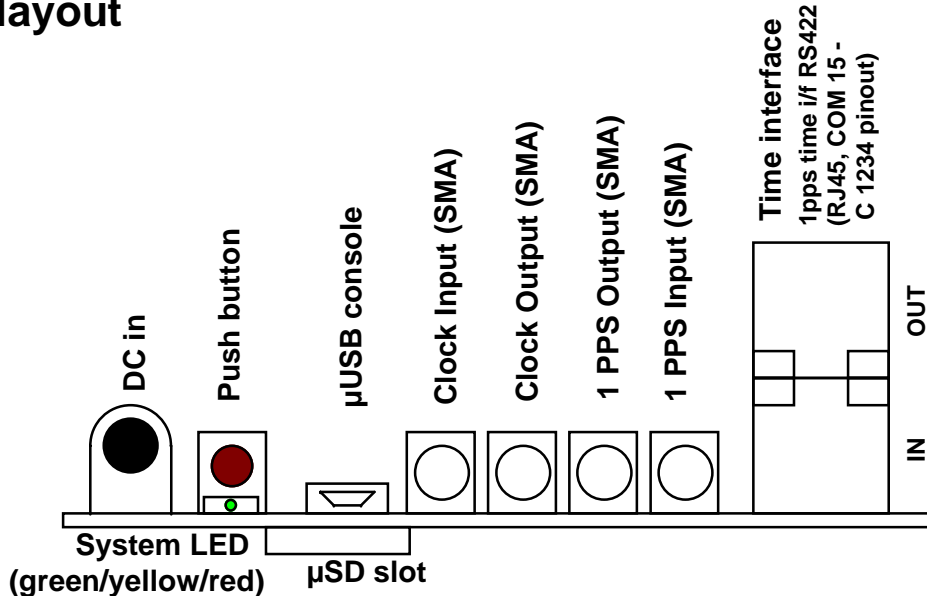
Port/SERDES/device mapping - per VSC7514 config...

PCIe/NPI	4x RJ45	8x SFP
Conf e: S5 NPI PHY, S8 SFP6 Conf d: S8 PCIe, S5 SFP6 Conf b: S8 PCIe, S5 SFP6 Conf 2: S5 NPI PHY, S8 SFP6	Conf e: P3/D3 Conf d: P3/D3 Conf b: P3/D3 Conf 2: P3/D3 Conf e: P1/D1 Conf d: P1/D1 Conf b: P1/D1 Conf 2: P1/D1	Conf e: S1/D1 Conf d: S1/D5 Conf b: S1/D1 Conf 2: S1/D1 Conf e: S3/D6 Conf d: S3/D6 Conf b: S3/D3 Conf 2: S3/D3 Conf e: S8/D10 Conf d: S5/D10 Conf b: S5/D5 Conf 2: S8/D10 Conf e: S7/D8 Conf d: S7/D8 Conf b: S7/D8 Conf 2: S7/D8
	SLED/LOS LED: D2 LED: D3 LED: Gated D0 LED: Gated D1	LED: Gated D0 LOS: D0 LED: Gated D1 LOS: D1 (option for D5) LED: D4 LOS: D4 LED: D6 LOS: D6 LED: D9 LOS: D9 LED: D10 LOS: D10 LED: D7 LOS: D7 LED: D8 LOS: D8

Front layout



Rear layout



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Title

Block diagram

Size
A4

Document Number
PCB123

Rev
02-00

Date:

Tuesday, August 16, 2016

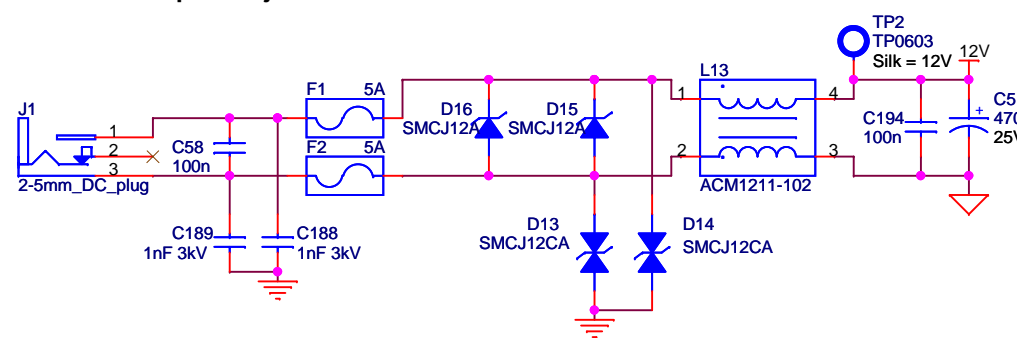
Sheet

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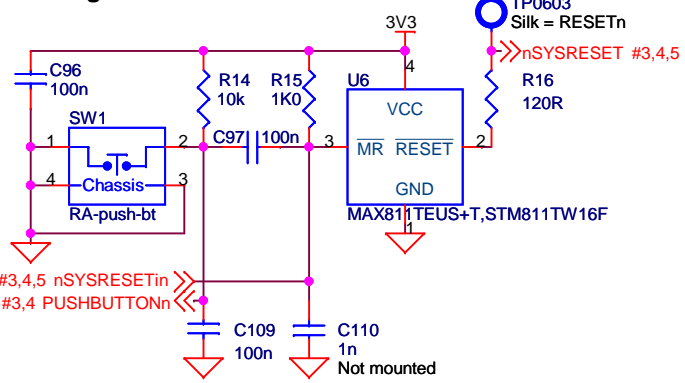
of

6

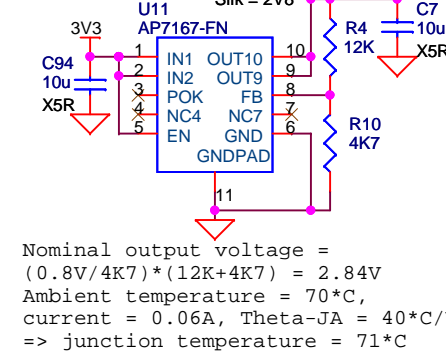
2.5mm center pin DC jack for external PSU



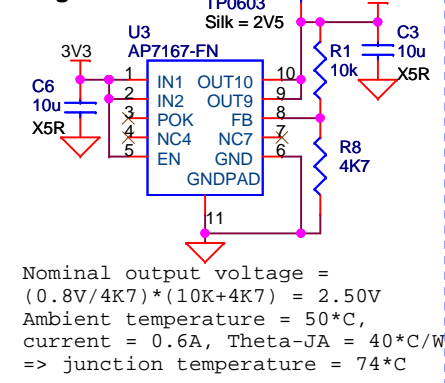
Reset generator



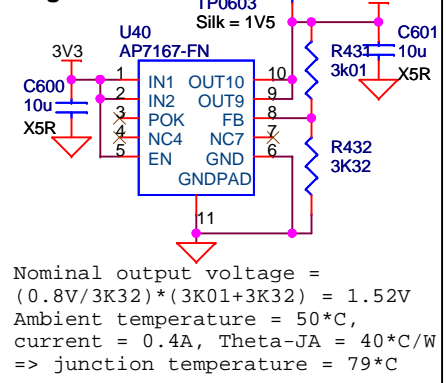
2V8 generation, Flash



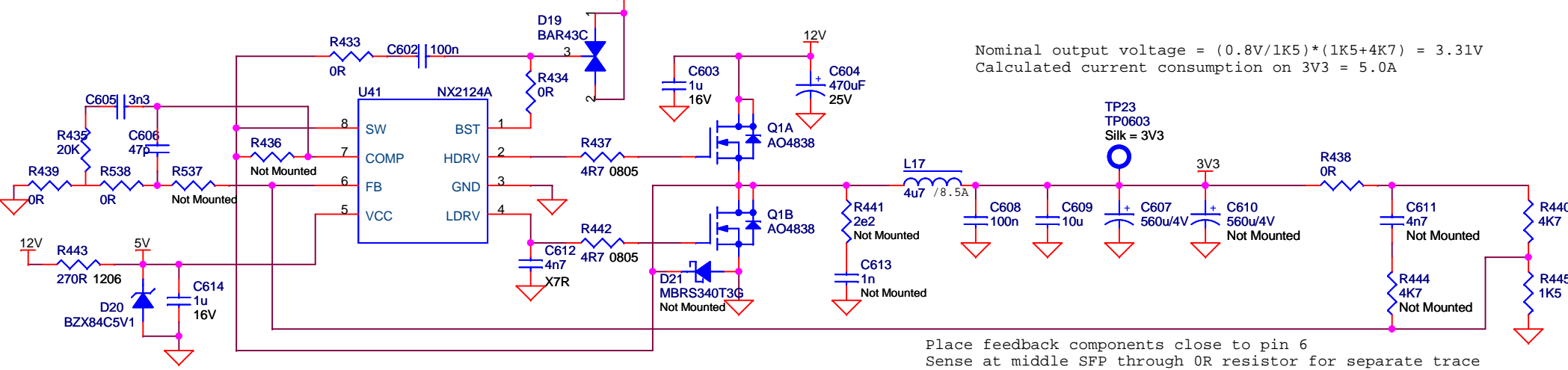
2V5 generation



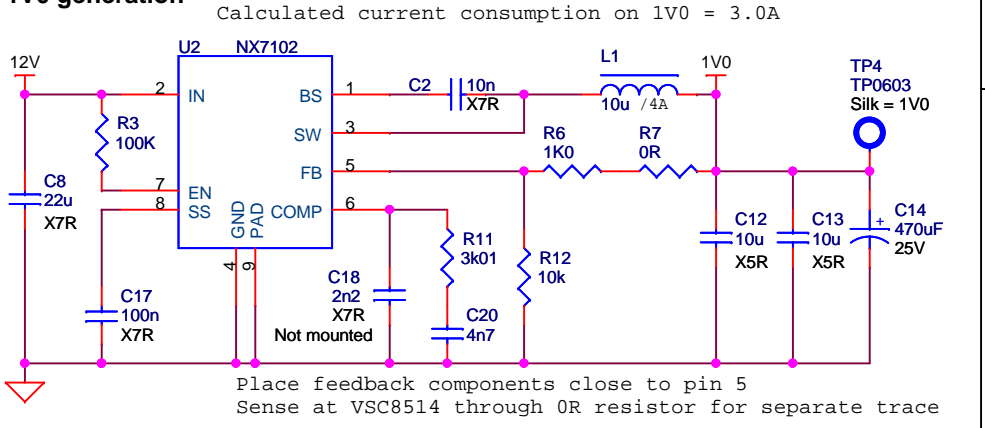
1V5 generation



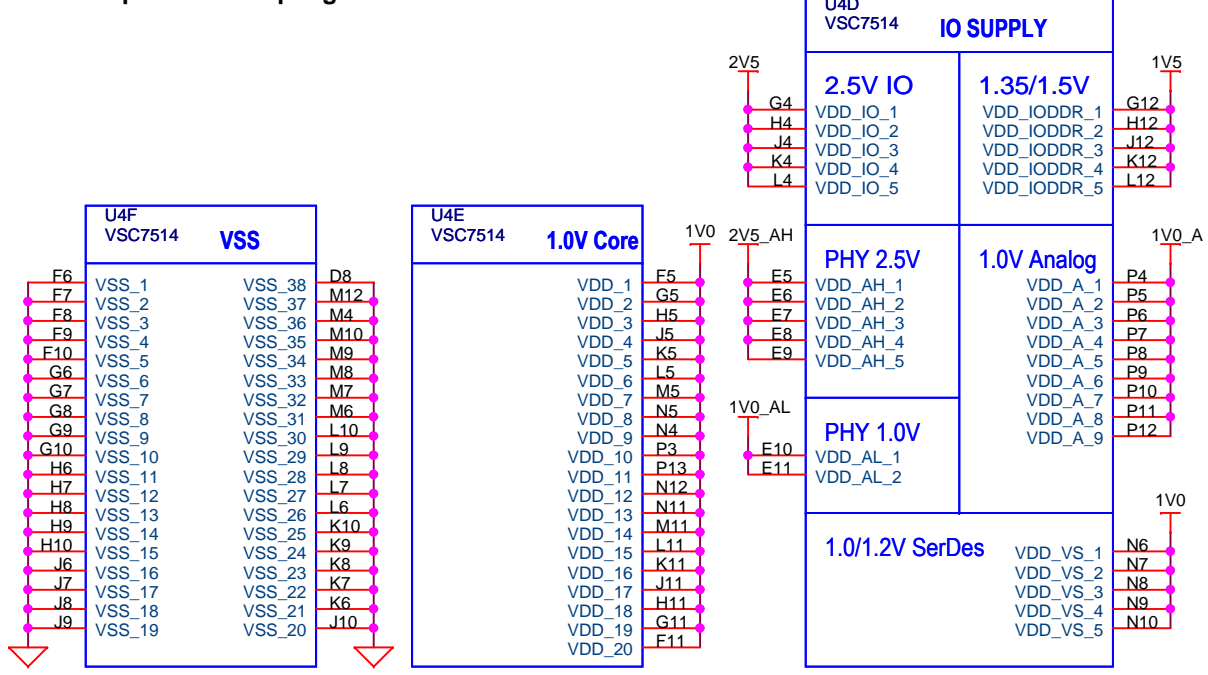
3V3 generation



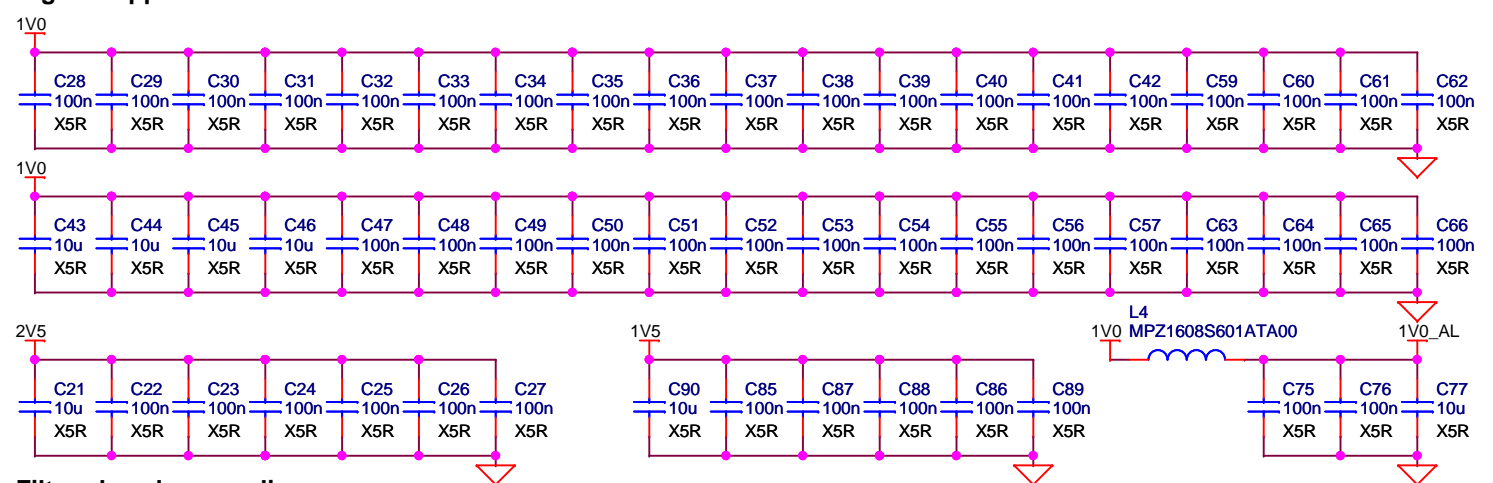
1V0 generation



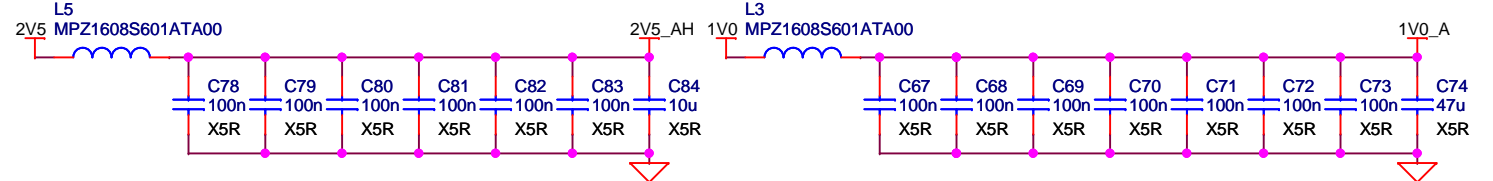
VSC7514 power/decoupling



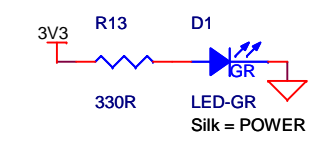
Digital supplies



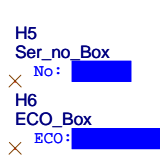
Filtered analog supplies



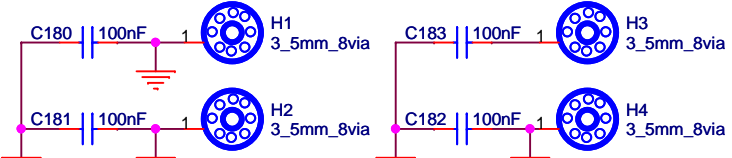
Power ON indicator



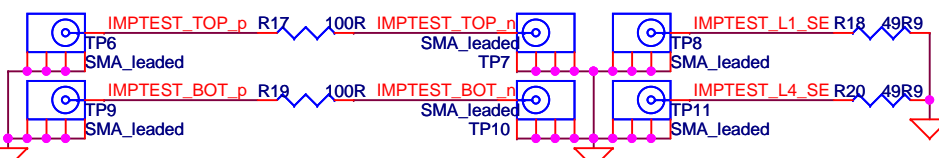
Silkscreen



Mounting holes



Impedance test traces



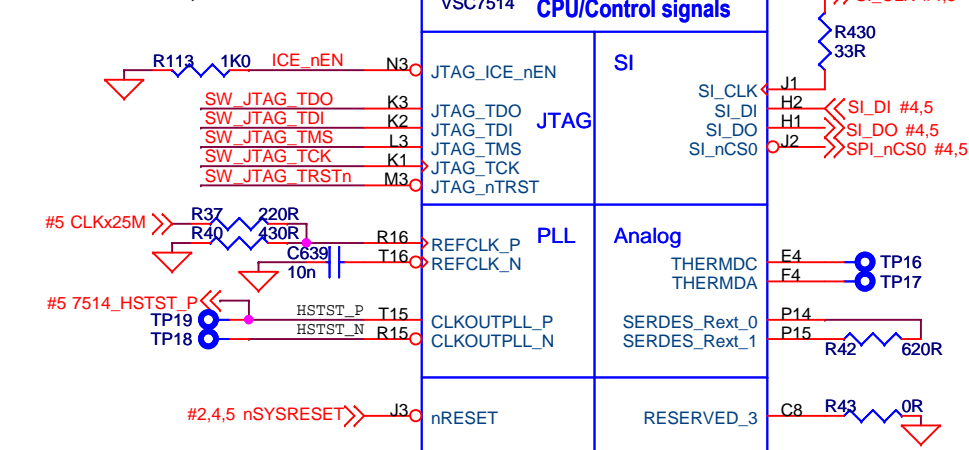
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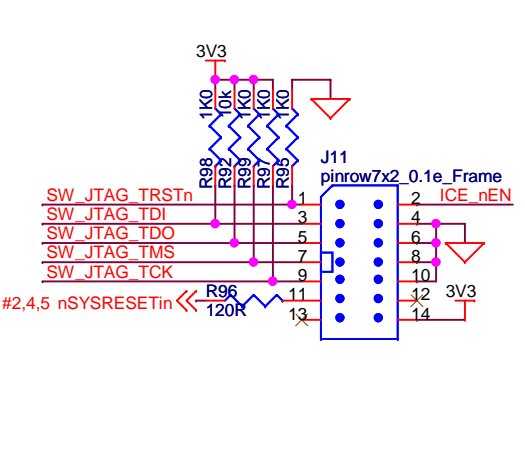
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MAG
Title: Power inlet, voltage conversion, VSC7514 power/decoup, reset
Size: A3
Document Number: PCB123
Date: Monday, August 15, 2016
Sheet: 2 of 6
Rev: 02-00

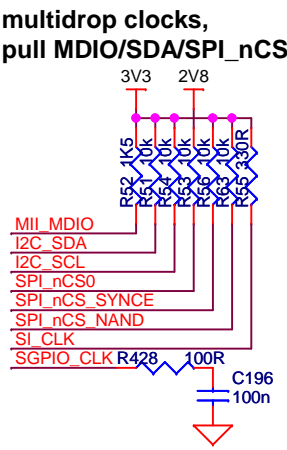
VSC7514 clocks, boot interface



VCore-III ICE / JTAG connector

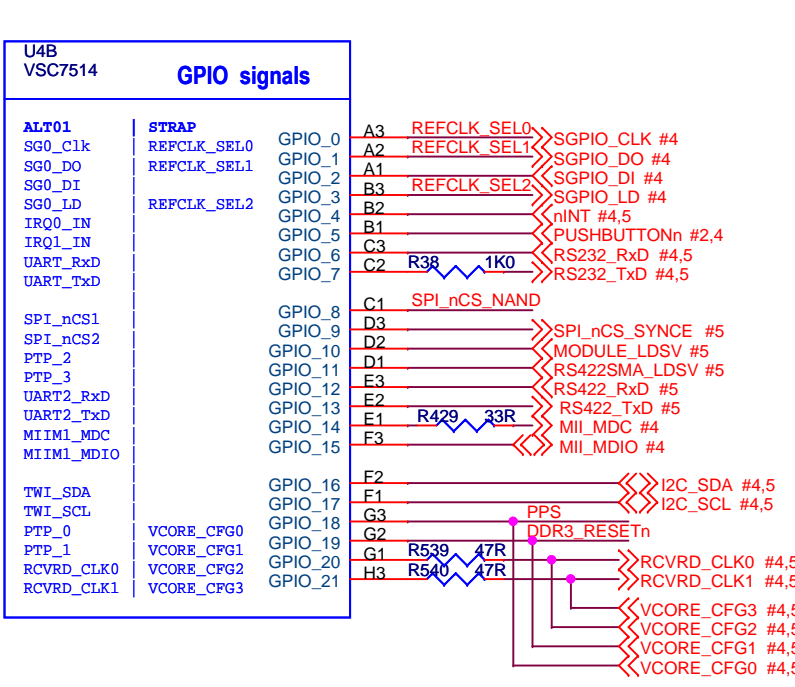


End termination of multidrop clocks, pull MDIO/SDA/SPI_nCS

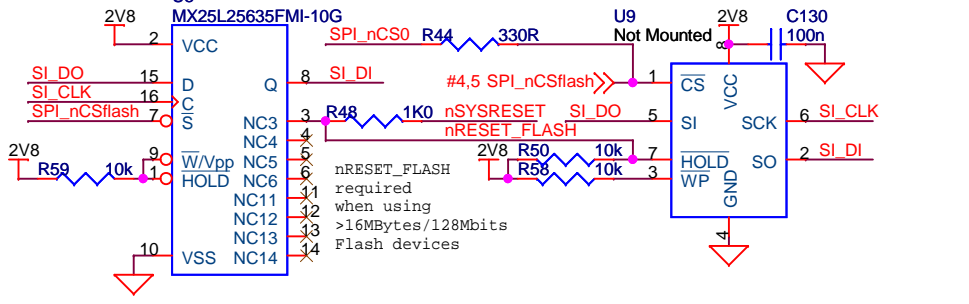


VSC7514 GPIO

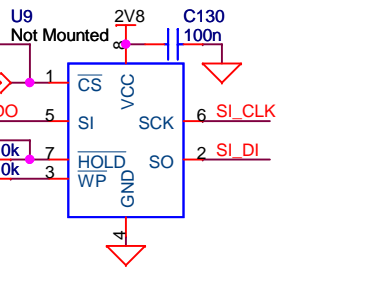
VSC7514 GPIO alternate functions		
GPIO #	ALT "10"	ALT "11"
0		
1		
2		
3		
4	IRQ0_OUT	TWI_SCL_MUX13
5	IRQ1_OUT	PCI_Wake
6	TWI_SCL_MUX0	
7	TWI_SCL_MUX1	
8		IRQ0_OUT
9	TWI_SCL_MUX2	IRQ1_OUT
10	TWI_SCL_MUX3	SFP0_SD
11	TWI_SCL_MUX4	SFP1_SD
12	TWI_SCL_MUX5	SFP2_SD
13	TWI_SCL_MUX6	SFP3_SD
14	TWI_SCL_MUX7	SFP4_SD
15	TWI_SCL_MUX8	SFP5_SD
16		
17		SPI_nCS3
18	TWI_SCL_MUX10	SPI_nCS4
19	TWI_SCL_MUX11_AD	
20	TACHO	TWI_SCL_MUX14_AD
21	PWM	TWI_SCL_MUX15_AD



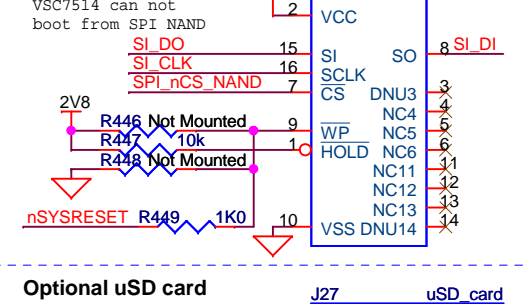
SPI boot Flash 32MBytes (SO16)



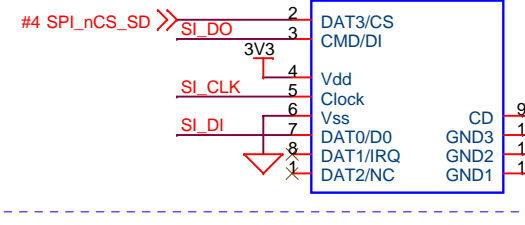
Alternate SPI boot Flash (SO8)



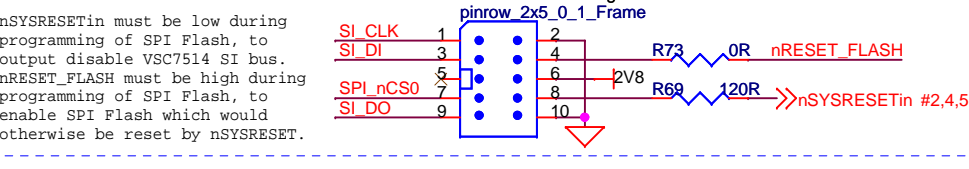
SPI NAND 256MBytes



Optional uSD card

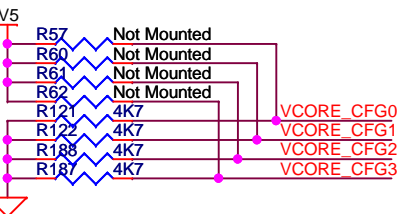


SPI boot Flash programming header



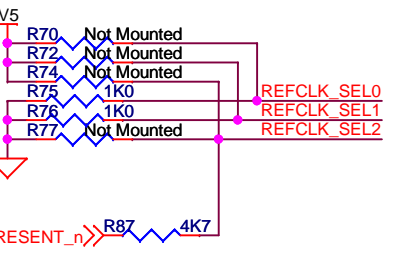
VSC7514 boot mode strapping

VCore_Cfg[3:0]	VCore-III CPU Behavior
0 0 0 0	MIPS (or 8051 boots) from SI interface. The MIPS is Little Endian.
0 0 0 1	8051 IROM boot. Reserved for port-bringup.
0 0 1 0	8051 IROM boot. Reserved for port-bringup.
0 0 1 1	8051 IROM boot. Reserved for port-bringup.
0 1 0 0	8051 IROM boot. Reserved for port-bringup.
0 1 0 1	8051 IROM boot. Reserved for port-bringup.
0 1 1 0	8051 IROM boot. Reserved for port-bringup.
0 1 1 1	8051 IROM boot. Reserved for port-bringup.
1 0 0 0	8051 IROM boot. NPI:1G FDX NoFC, VRAP.
1 0 0 1	8051 IROM boot. PCIe
1 0 1 0	No boot. SI slave and MIIM slave @ address 0 (GPIO alternative).
1 0 1 1	No boot. SI slave and MIIM slave @ address 31 (GPIO alternative).
1 1 0 0	MIPS or 8051 boots from SI interface. The MIPS is Big Endian.
1 1 0 1	Reserved.
1 1 1 0	8051 boots from SI interface (the MIPS is disabled).
1 1 1 1	No boot. SI slave is enabled.



VSC7514 PLL strapping

REFCLK_SEL[2:0]	Frequency	Comment
0 0 0	125MHz	The default mode. Normal operation mode with 125MHz
0 0 1	156.25MHz	Normal operation mode with 156.25MHz ref clock
0 1 0	250MHz	Normal operation mode with 250MHz ref clock
0 1 1	N/A	Reserved
1 0 0	25MHz	Normal operation mode with 25MHz ref clock
1 0 1	N/A	Reserved
1 1 0	N/A	Reserved
1 1 1	N/A	Reserved

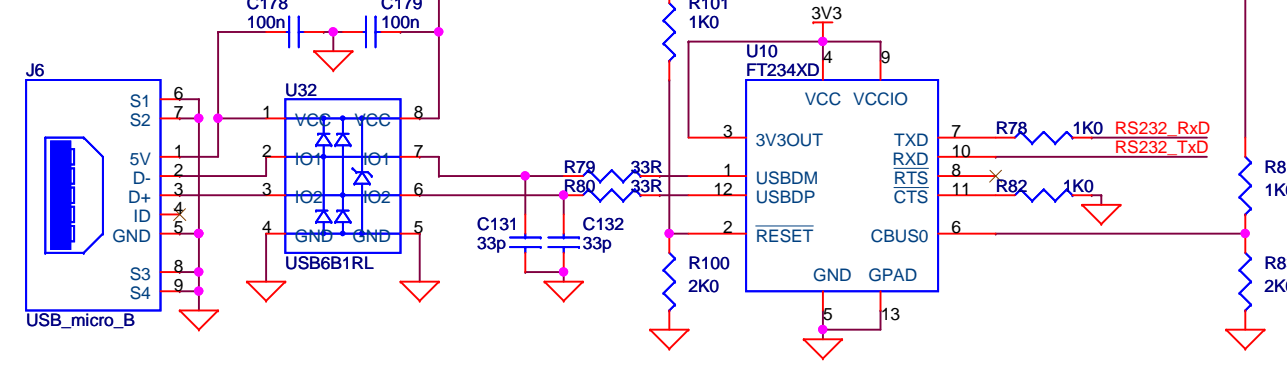


Due to VSC7514 jitter requirements, don't use 25MHz REFCLK as base for QSGMII

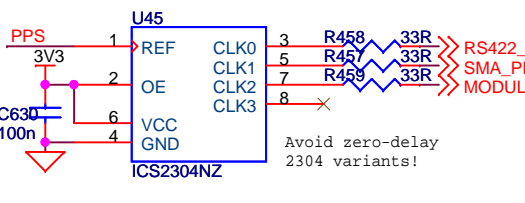
Board I2C address table

Address	I2C slave
1010xxx	SFP transceiver

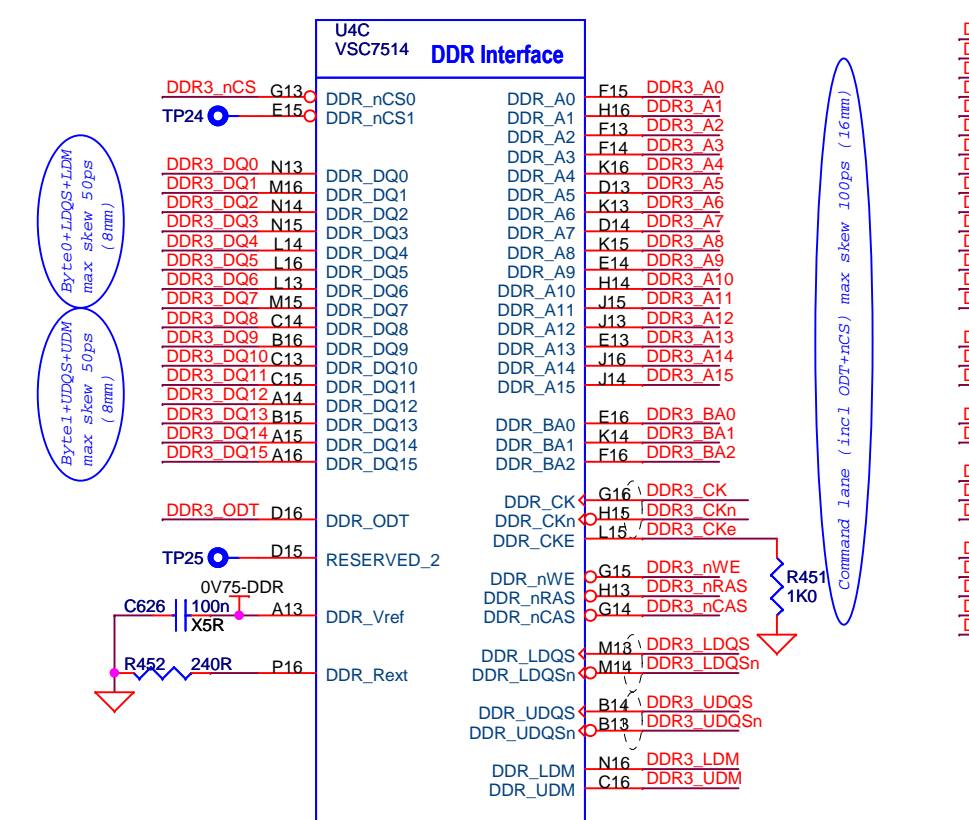
UART/USB connection



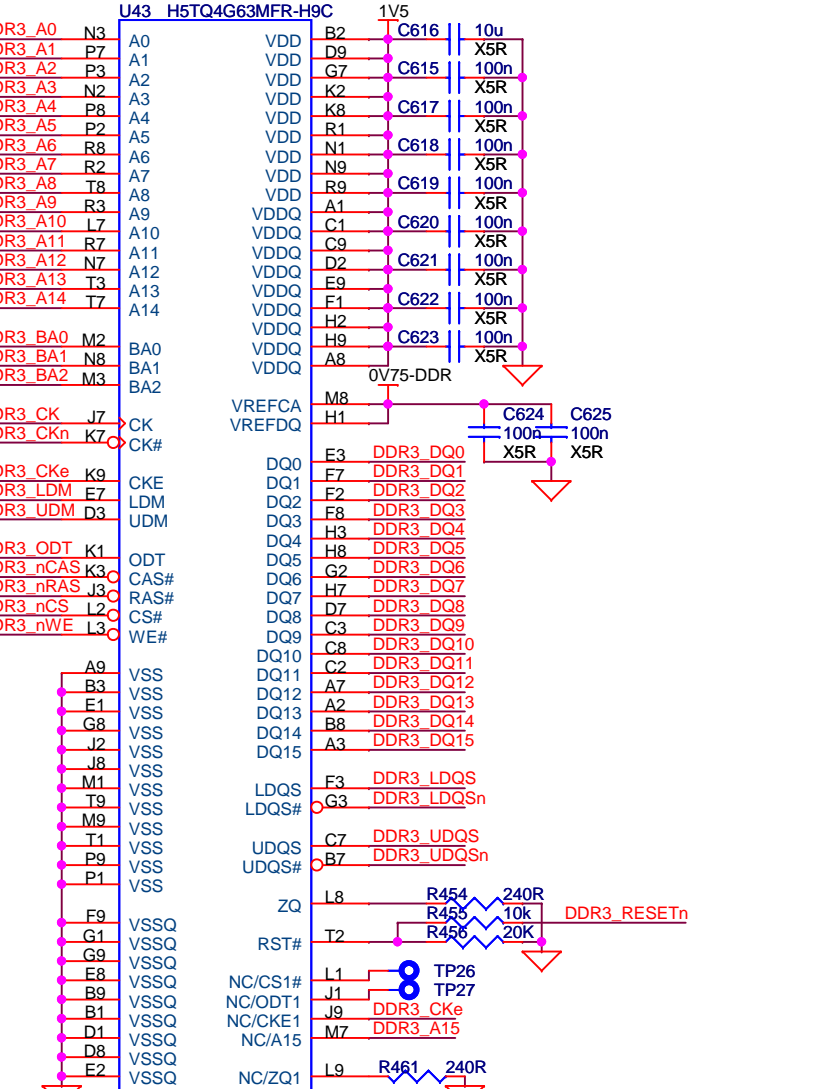
Fanout of 1PPS with tightly specified tpd



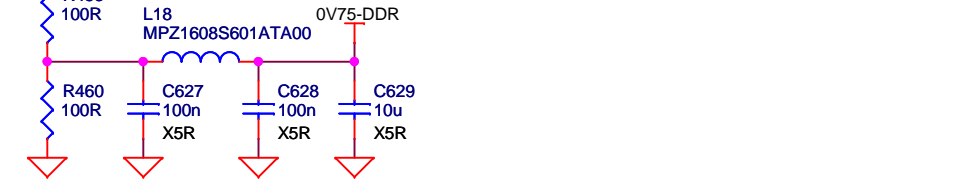
VSC7514 DDR3 RAM Interface



DDR3 RAM 256Mx16 (4Gbits/512MBytes)



V/2 generator for SSTL-15 interface

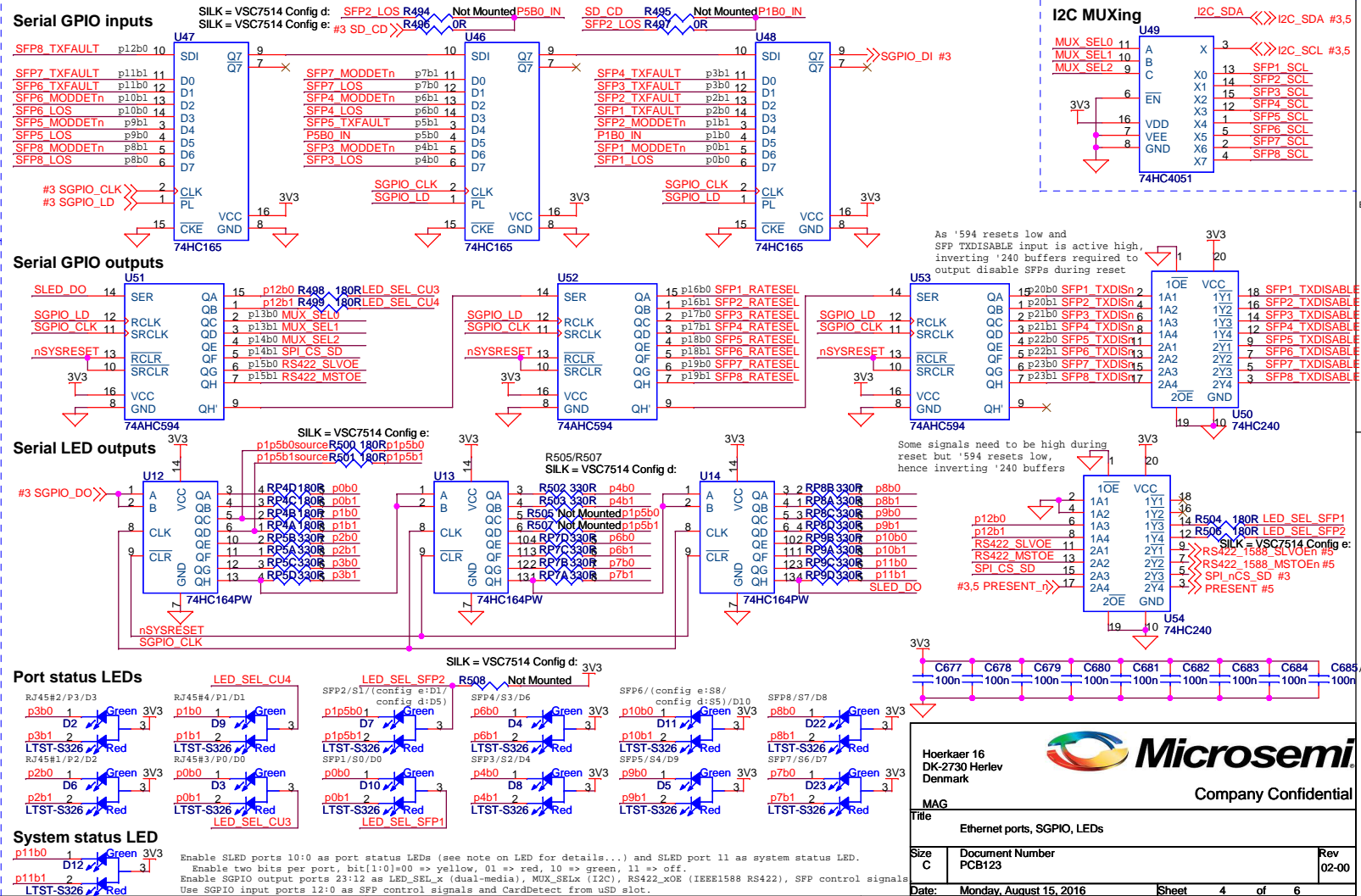
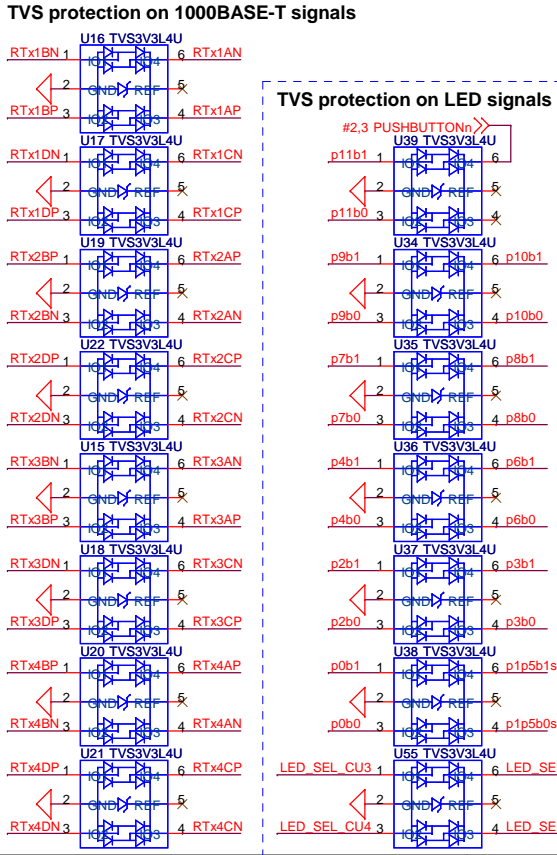
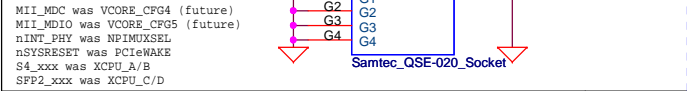


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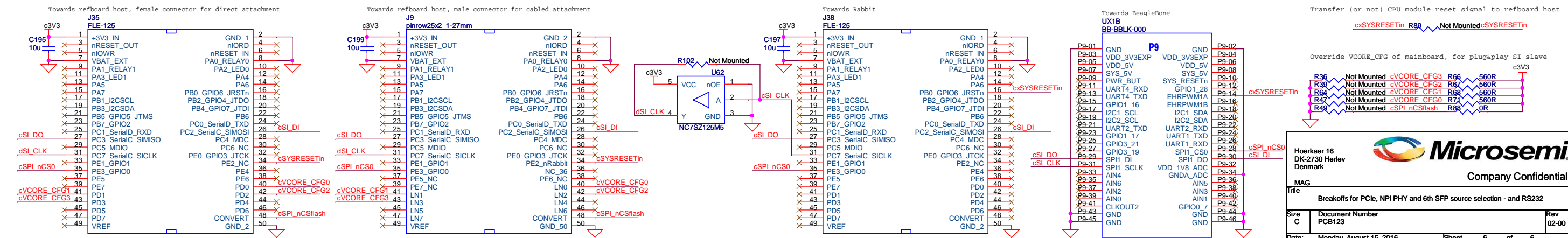
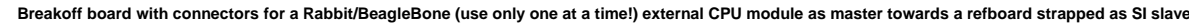
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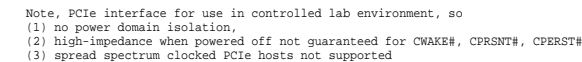
Title VSC7514 memory (SPI boot Flash, DDR3, NAND), GPIO, strapping		
Size A3	Document Number PCB123	Rev 02-00
Date: Tuesday, August 16, 2016	Sheet 3	of 6



Samtec connector towards mainboard, feedthrough of S8 to SFP



Samtec connector towards mainboard, feedthrough of S5 to SFP



J26

