VSC7511/12

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC7511/12. These checklist items should be followed when utilizing the VSC7511/12 in a new design. A summary of these items is provided in Section 13.0, "Hardware Checklist Summary," on page 15. Detailed information on these subjects can be found in the corresponding section:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Reference Clock"
- Section 5.0, "CPU System"
- Section 6.0, "Port Configuration"
- Section 7.0, "Internal Copper PHY Ports"
- Section 8.0, "SerDes Interfaces"
- Section 9.0, "Serial GPIO Controller"
- Section 10.0, "Other Interfaces"
- Section 11.0, "System Reset"
- Section 12.0, "SyncE and PTP"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The VSC7511/12 implementor should have the following documents on hand:

- *VSC7511 Data Sheet*
- *VSC7512 Data Sheet*
- *Microsemi VSC5634EV Ocelot Unmanaged Hardware Manual User Guide*

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.
- If the customer plans to use Microchip turnkey software package, Microchip recommends to use one of its reference design schematics as a basis and retain the reference design's use of GPIO (parallel as well as serial) whenever possible to minimize software changes. Keep a log of the major changes (for example, port numbering, PHY addresses, GPIO, and SGPIO) and provide this log when there is design review or when starting software customization.

2.3 Strapping Pins

Some of the GPIO pins are used as strapping pins at power-up for configuring PLL reference clock frequency and for selecting CPU start-up modes. See Figure 2-1 and Table 2-1 for the description of the strapping pins and the corresponding configurations and modes. 1K-4.7K resistors are recommended for pulling the strapping high or low accordingly.

FIGURE 2-1: STRAPPING PINS OVERLAID WITH GPIO PINS

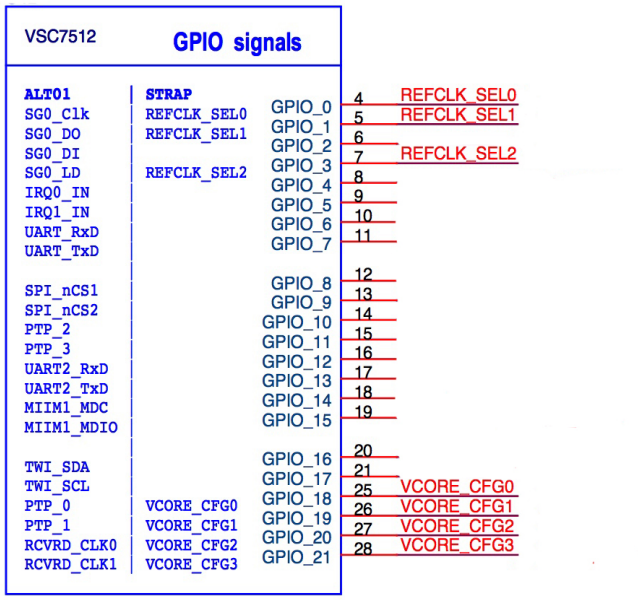


TABLE 2-1: VSC7511/12 STRAPPING PIN DESCRIPTIONS

Pin	Description
REFCLK_CONF[2:0]	Configuration of reference clock frequency for PLL 000: 125 MHz 001: 156.25 MHz 010: 250 MHz 100: 25 MHz Other values are reserved and must not be used.
VCORE_CFG[3:0]	1010: No boot. SI slave and MIIM slave enabled with MIIM address 0. 1011: No boot. SI slave and MIIM slave enabled with MIIM address 31. 1110: VCORE-Ie boots from SI interface. 1111: No boot. SI slave is enabled.

2.4 Ground

- Create at least one unbroken ground plane (GND).
- The center exposed pad underneath the VSC7511/12 must be connected to the digital ground plane. It is also the main thermal path for heat dissipation from the die. The heat dissipation is through the exposed pads, through the thermal vias to the copper planes in the PCB. Make sure to use at least 5*5 grid thermal vias in the exposed pad to increase the power capability and thermal conductivity of the connection.

3.0 POWER

3.1 Power Supply

- VSC7511/12 requires power at:
  - 2.5V for I/O circuits on **VDD_IO** pins.
  - 2.5V for internal copper PHY analog circuits on **VDD_AH** pins.
  - 1.0V for internal copper PHY analog circuits on **VDD_AL** pins.
  - 1.0V for internal core on **VDD** pins.
  - 1.0V for internal analog circuits on **VDD_A** pins.
  - 1.0V or 1.2V for all the Serializer/Deserializer (SerDes) interfaces on **VDD_VS** pins.
- Each power supply voltage should have both bulk and high-frequency decoupling capacitors. Recommended bulk decoupling capacitors are 10 µF, but 47 µF should be used for VDD_A due to initial load during power-up. High-frequency decoupling capacitors that are 0.1 µF are also recommended. Surface mount decoupling capacitors should be placed as close to the power supply pins as possible.
- Analog supplies must be isolated from the remaining board supplies using ferrite beads.

3.2 Power Supply Sequencing

- During power-on and power-off, **VDD_A** and **VDD_VS** must never be more than 300 mV above **VDD**.
- **VDD_VS** must be powered even if the associated interfaces are not used. These power supplies must not remain at ground or left floating.
- There is no sequencing requirements for **VDD_IO**.

4.0 REFERENCE CLOCK

The reference clock of the device can be a 25 MHz, 125 MHz, 156.25 MHz, or 250 MHz clock signal. The frequency is selected through REFCLK_CONF[2:0] described in Table 2-1.

The reference clock can be either a differential reference clock or a single-ended clock. Note of the device data sheet's requirements for maximum clock jitter, which must be accounted for in board design when selecting clock source (oscillator) and clock distribution (buffer) components.

4.1 Differential Clock

When the differential clock is used, the input is best compatible with low voltage differential signaling (LVDS) signal. Each P/N pin of the clock input has an internal 50R termination to 0.7V that results in a 100R differential termination from P to N, inherently biased to 2/3 VDD. AC coupling is recommended to meet the reference clock input specification on common-mode voltage using the internal termination as biasing.

The data sheet prescribes an upper voltage limit on the P/N signals of 1200 mV. This is due to the ESD clamp diodes on the inputs. Because of the termination or biasing to 2/3 VDD (typically the common-mode voltage), this imposes a limit on the single-ended swing for P or N of 2*(1200 mV-700 mV) = 1000 mV. Some low voltage positive emitter-couple logic (LVPECL) might have a larger differential swing than 400 mV, so it should be attenuated using resistor dividers to meet the input specification for voltage swing.

To meet the QSGMII requirements, a differential reference clock of minimum 125 MHz is recommended.

4.2 Single-Ended REFCLK Input

Although the VSC7511/12 reference clock input is differential, it is also possible to use a single-ended clock source. This can be done by setting one differential input to a common-mode voltage and shaping the single-ended signal driving the other differential input, so that it toggles around this common-mode voltage with a voltage swing comparable to LVDS. The reference clock differential input buffer sees this as a valid differential signal. An external resistor network is required to do so. The resistor network limits the amplitude and adjusts the center of the swing. Figure 4-1 and Figure 4-2 show the resistor network and the recommended values for the resistors for 3.3V and 2.5V CMOS single-ended clock signals.

FIGURE 4-1: RESISTOR NETWORK FOR 3.3V CMOS SINGLE-ENDED CLOCK

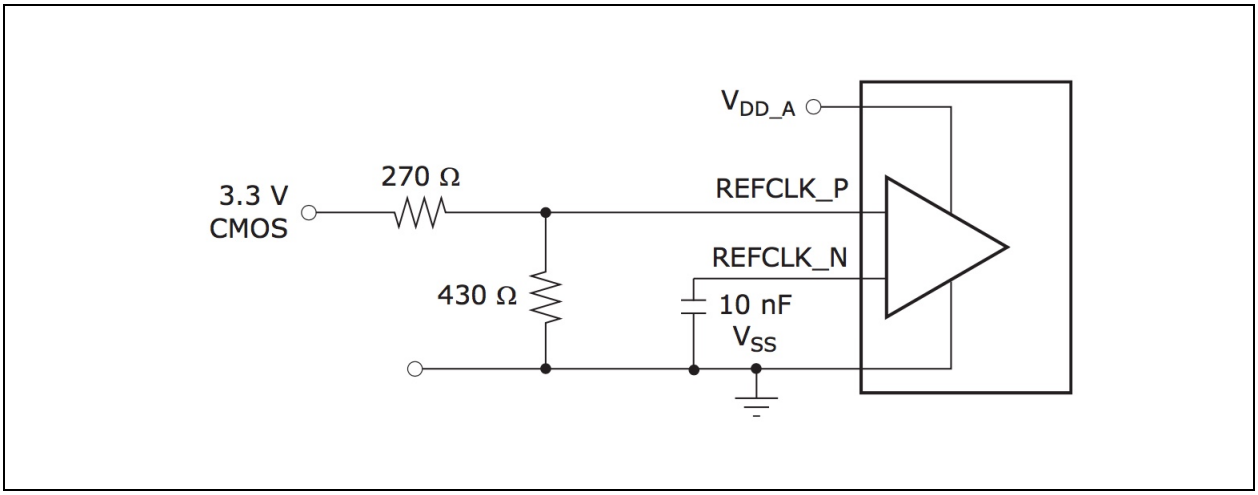
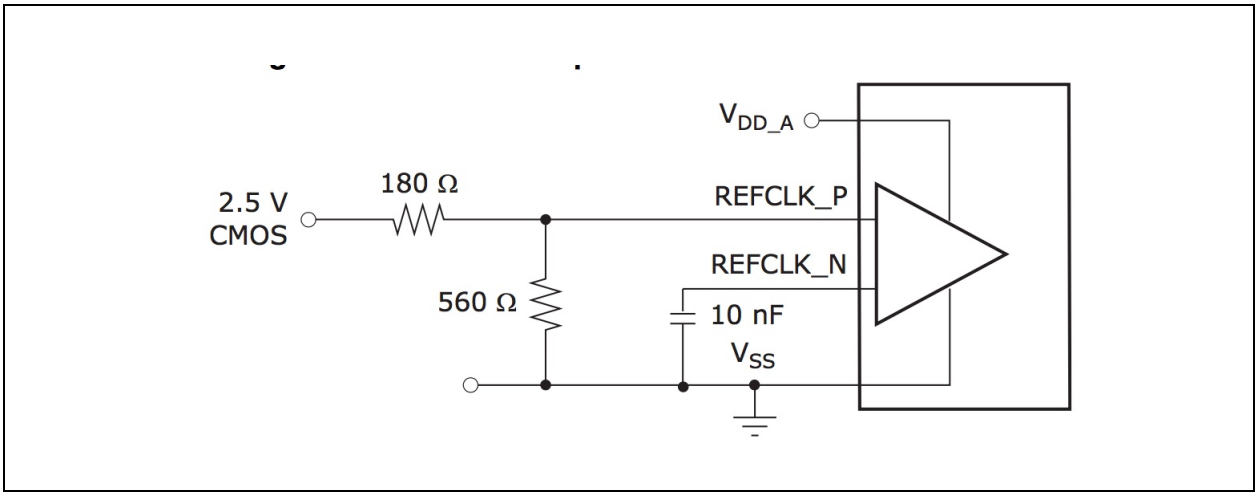


FIGURE 4-2: RESISTOR NETWORK FOR 2.5V SINGLE-ENDED CLOCK



5.0 CPU SYSTEM

VSC7511/12 can be managed by either the internal VCORE-Ie CPU or an external CPU. The selection between internal or external CPU is based on VCORE_CFG[3:0] strapping pins described in Section 2.3, "Strapping Pins".

The internal VCORE-Ie CPU is based on a fast 8051-compatible microprocessor. It is enabled and boots from the SPI Flash when VCORE_CFG[3:0] strapping is configured to 1110. When VCORE_CFG[3:0] strapping is configured to 1010, 1011, or 1111, the internal CPU is disabled. An external CPU can be connected to VSC7511/12 through MIIM slave interface or SPI interface. The external CPU can either manage the switch all by itself or load an image to the internal RAM of the internal CPU to boot the internal CPU.

5.1 Internal CPU Auto Boot Mode

The switch supports four SPI chip-select pins, but only SI_nCS0 can be used for the internal CPU to boot from Flash. A 64 KB SPI Flash is required to store the firmware.

A Flash programming header in Microchip reference design is used to support on-PCB Flash programming. Pin 8 of the Flash programmer header is nSYSRESETin that is an input to the reset generator. The purpose of this signal is to make nSYSRESET output low during Flash programming, so that VSC7511/12 is held in reset and does not drive the SPI signals. Otherwise, both VSC7512 and the Flash programmer drive the SPI signals that will cause Flash programming failure.

SPI_nCSx and SPI_CLK signals are recommended to be pulled up, so the two signals will be high when the switch is not driving them.

Note: VSC7511/12 is a 2.5V input/output (I/O) device, and the output high voltage (Voh) from the switch can be as low as 1.7V at worst cases. This might not meet the input high voltage (Vih) requirement of an SPI Flash with 3.3V power supply. It is recommended to use a Flash memory with lower power supply voltage (2.8V for example), or to put a buffer with voltage translation on the SPI bus between VSC7511/12 and the Flash memories.

5.2 External CPU Mode

Some of the VCORE_CFG strapping options (see Table 2-1) disable the internal CPU and allow an external CPU to control the switch through either the SPI slave interface or the MIIM slave interface.

5.2.1 SPI SLAVE INTERFACE

The SPI slave interface is enabled when VCORE_CFG[3:0] is 1010, 1011, or 1111. The SPI slave interface shares the same pins as the SPI boot controller interface. Among the chip selection signals, only SI_nCS0 supports Slave mode.

When the external CPU uses the SPI slave interface to read switch registers, VSC7511/12 must prepare read data after receiving the last address bit. The access time of the register that is read must be satisfied before shifting out the first bit of read data, so there must be a delay between the last address bit and the first data bit. Below are some ways to satisfy the needed delay:

- Use SI_CLK with a period of minimum twice the access time for the register target. For example, for normal switch core targets (single master): 1/(2 × 1 µs) = 500 kHz (maximum)
- Pause the SI_CLK between shifting of serial address bit 0 and the first data bit with enough time to satisfy the access time for the register target.
- Configure the device to send out padding bytes before transmitting the read data to satisfy the access time for the register target. For example, 1 dummy byte allows enough read time for the SI clock to run up to 6 MHz in a single master system.

5.2.2 SLAVE MIIM INTERFACE

The MIIM slave interface is enabled when VCORE_CFG[3:0] is 1010 (for address 0) or 1011 (for address 31). The MIIM slave pins on the device are overlaid functions on the GPIO interface. MIIM_SLV_MDIO is recommended to be pulled high through a 1.5K resistor.

5.2.3 PCIE® INTERFACE

The PCIe® interface can also be used for an external CPU to read or write switch registers. The PCIe interface can be enabled by the firmware.

AC coupling is recommended on the PCIe link between the switch and the external CPU.

6.0 PORT CONFIGURATION

6.1 VSC7512 Port Configuration

VSC7512 has up to four internal copper PHY ports and five SerDes (two 1G SerDes and three 6G SerDes) interfaces. Internally, VSC7512 is an 11-port switch. The copper PHY and SerDes interfaces are mapped to the 11 switch ports and a PCIe interface through the port multiplexer (MUX). The configuration of the port MUX is done through the MACRO_CTRL::HW_CFG register. Table 6-1 lists the definition of that register.

TABLE 6-1: REGISTER DESCRIPTION OF HW_CFG FOR VSC7512

Bit	Name	Access	Description	Default
6	DEV2G5_10_MODE	R/W	Configure mode of device DEV2G5_10. This can be connected to SerDes1G_5 or SerDes6G_2. Setting PCIE_ENA prevents DEV2G5_10 to be connected to SerDes6G_2. 0: DEV2G5_10 is connected to SerDes6G_2. 1: DEV2G5_10 is connected to SerDes1G_5.	0x0
5	DEV1G_9_MODE	R/W	Configure mode of device DEV1G_9. This can be connected to SerDes1G_4 or be disconnected. 0: DEV1G_9 is disconnected. 1: DEV1G_9 is connected to SerDes1G_4.	0x0
4	RESERVED	R/W	Must be set to the default value.	0x0
3	RESERVED	R/W	Must be set to the default value.	0x0
2	RESERVED	R/W	Must be set to the default value.	0x0
1	PCIE_ENA	R/W	Set to enable PCIe mode for SerDes6G_2. 0: Disable PCIe 1: Enable PCIe	0x0
0	QSGMII_ENA	R/W	Set bit 0 to enable QSGMII mode for devices DEV1G_4, DEV1G_5, DEV1G_6, and DEV1G_7 via SerDes6G_0. 0: Disable QSGMII 1: Enable QSGMII	0x0

Some of the typical configurations of the switch are shown in the Table 6-2.

TABLE 6-2: VSC7512 TYPICAL PORT CONFIGURATION

SerDes/CuPHY No SerDes Type			0 Cu	1 Cu	2 Cu	3 Cu	4 1G	5 1G	6 6G	7 6G	8 6G	Max BW Incl NPI
Configuration	VSC7512	D0-D10										
2	8 + NPI	4 x Cu + 2 x 1G SGMII + 2 x 2.5G SGMII + 2.5G NPI	D0	D1	D2	D3	D4	D5	D7	D8	D10	13.5
b	8 + PCIe	4 x Cu + 2 x 1G SGMII + 2 x 2.5G SGMII + PCIe	D0	D1	D2	D3	D4	D5	D7	D8	PCIe	11
0	10 + NPI	4 x Cu + 1 x 1G SGMII + 1 x QSGMII + 1 x 2.5G SGMII + 2.5G NPI	D0	D1	D2	D3	D9		Q0	D8	D10	14
c	11 + PCIe	4 x Cu + 2 x 1G SGMII + 1 x QSGMII + 1 x 2.5G SGMII + PCIe	D0	D1	D2	D3	D9	D10	Q0	D8	PCIe	12.5

- Config 2 in Table 6-2 represents a 4-Cu + 5-SerDes switch. This is the default configuration (HW_CFG = 0x0) of the switch, where:
  - the QSGMII and the PCIe are disabled.
  - the first four switch ports connect to the internal copper PHY (Cu0-Cu3).
  - SerDes S4-S8 map to switch ports D4, D5, D7, D8, and D10.
- Config b is enabled by setting only HW_CFG = 0x2 to enable PCIe. When the PCIe is enabled, it overrules bit 6 of HW_CFG. The PCIe interface can only be enabled on SerDes S8.
- Config 0 is a 4-Cu + 3-SerDes + 1-QSGMII switch. This configuration is enabled by enabling the QSGMII interface (HW_CFG = 0x21). The QSGMII interface can only be enabled on S6. When the QSGMII is enabled, it is always mapped to switch ports D4, D5, D6, and D7. It is recommended to enable TX for all four ports in the QSGMII even when not all of them are actually connected to the external PHY for timing consideration.
- Config c is enabled by setting HW_CFG to 0x63.

6.2 VSC7511 Port Configuration

VSC7511 has up to four internal copper PHY ports and five SerDes (four 1G SerDes and one 6G SerDes) interfaces, but not all of the copper PHY and SerDes interfaces can be enabled to work at the same time. Internally, VSC7511 is a 5-port switch. The number of 1G copper PHY ports and 1G SerDes ports combination is limited to be no more than four. The 6G SerDes port can be configured as a 2.5G NPI port or a PCIe interface. The copper PHY and SerDes interfaces are mapped to the five switch ports and a PCIe interface through the port MUX. The configuration of the port MUX is done through register MACRO_CTRL::HW_CFG. Table 6-3 shows the definition of that register.

TABLE 6-3: REGISTER DESCRIPTION OF HW_CFG FOR VSC7511

Bit	Name	Access	Description	Default
6	DEV2G5_10_MODE	R/W	Configure mode of device DEV2G5_10. This can be connected to SerDes1G_5 or SerDes6G_2. Setting PCIE_ENA prevents DEV2G5_10 to be connected to SerDes6G_2. 0: DEV2G5_10 is connected to SerDes6G_2. 1: DEV2G5_10 is connected to SerDes1G_5.	0x0
5	DEV1G_9_MODE	R/W	Configure mode of device DEV1G_9. This can be connected to SerDes1G_4 or be disconnected. 0: DEV1G_9 is disconnected. 1: DEV1G_9 is connected to SerDes1G_4.	0x0
4	RESERVED	R/W	Must be set to the default value.	0x0
3	RESERVED	R/W	Must be set to the default value.	0x0
2	RESERVED	R/W	Must be set to the default value.	0x0
1	PCIE_ENA	R/W	Set to enable PCIe mode for SerDes6G_2. 0: Disable PCIe 1: Enable PCIe	0x0
0	RESERVED	R/W	Must be set to the default value.	0x0

Some of the typical configurations of the switch are shown in Table 6-4.

TABLE 6-4: VSC7511 TYPICAL PORT CONFIGURATION

SerDes/CuPHY No SerDes Type			0 Cu	1 Cu	2 Cu	3 Cu	4 1G	5 1G	6 1G	7 1G	8 6G	Max BW Incl NPI
Configuration	**VSC7511**	**D0-D10**										
2	4 + NPI	4 x 1G (select from Cu0-Cu3 and/or S4-S7) + 2.5G NPI	D0	D1	D2	D3	D4	D5	D7	D8	D10	6.5
b	4 + PCIe	4 x 1G (select from Cu0-Cu3 and/or S4-S7) + PCIe	D0	D1	D2	D3	D4	D5	D7	D8	PCIe	4
d	4 + PCIe	4 x 1G (select from Cu0-Cu3 and/or S4-S7) + PCIe	D0	D1	D2	D3	D9	D10	D7	D8	PCIe	4
e	4 + NPI	4 x 1G (select from Cu0-Cu3 and/or S4-S7) + 2.5G NPI	D0	D1	D2	D3	D9	D5	D7	D8	D10	6.5

Note 1: The way to select between copper or SerDes is to enable or disable the copper port in the PHY_ENA register.

- Config 2 in Table 6-4 represents a 4-1G (copper or SerDes) + a 2.5G NPI switch. This is the default configuration (HW_CFG = 0x0) of the switch.
- Config b is a 4-1G (copper or SerDes) + a PCIe switch enabled by setting only HW_CFG = 0x2 to enable PCIe. When the PCIe is enabled, it overrules bit 6 of HW_CFG. The PCIe interface can only be enabled on SerDes S8.
- Config d is another 4-1G (copper or SerDes) + a PCIe switch with different port mapping. It is enabled by setting HW_CFG to 0x62.
- Config e is another 4-1G (copper or SerDes) + a 2.5G NPI switch with different port mapping than Config 2. It is enabled by setting HW_CFG to 0x60.

7.0 INTERNAL COPPER PHY PORTS

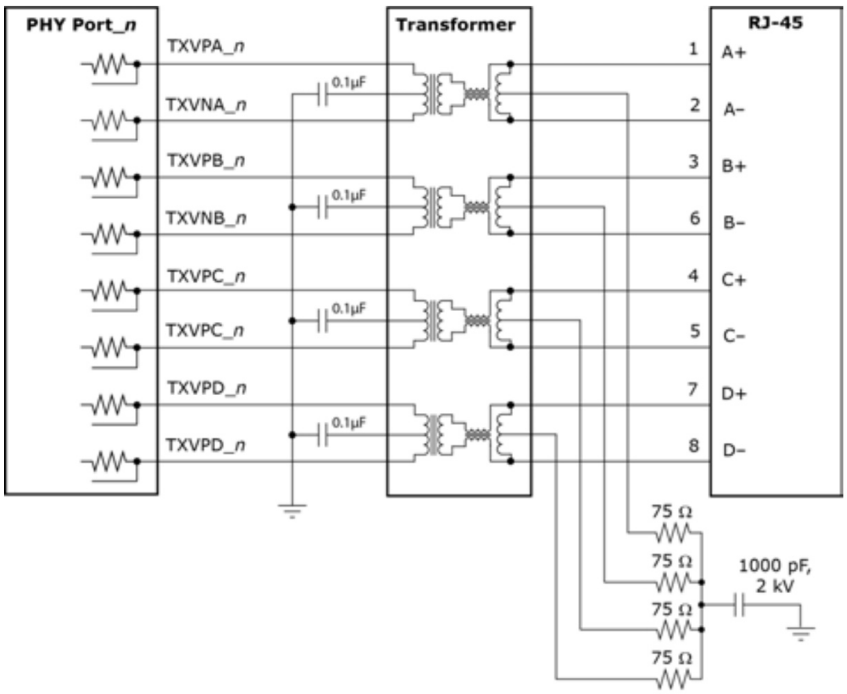
Four internal copper Gigabit (GbE) PHYs are available in VSC7511/12, and more external PHYs can be supported on the QSGMII interface or SGMII interfaces.

7.1 Copper PHY MDI Interface

Figure 7-1 shows the recommended connection from the internal copper PHY to the transformer. The internal copper PHY uses voltage-mode line driver technology, so no center tap voltage is required at the transformer. Each of the four center taps is recommended to be connected to GND through a separate 0.1 µF capacitor because the common-mode voltage on each pair might be different. The PHY has integrated termination resistors so no external terminations are needed.

Note: The PHY has integrated termination resistors, so no external terminations are needed. It is recommended to use a minimum of 8-core magnetics with a common mode choke (CMC) at the RJ45/cable side.

FIGURE 7-1: TRANSFORMER CONNECTIONS FOR INTERNAL COPPER PHY PORTS



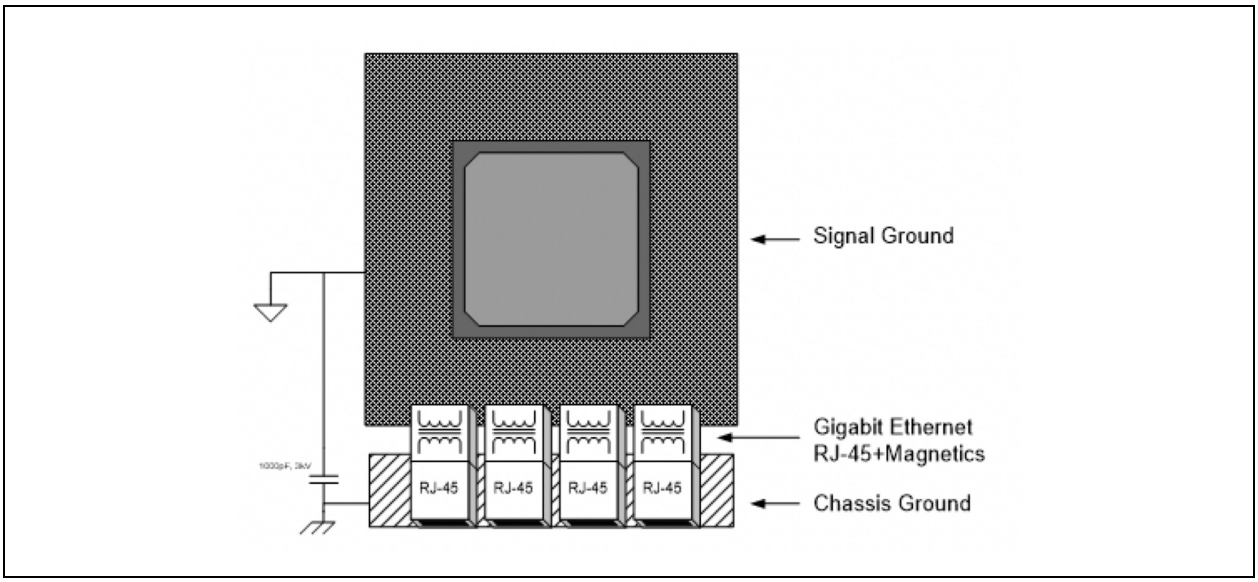
The MDI interface is organized into four differential pairs (A, B, C, and D) for each PHY port. Pairs C and D are only used in Gigabit speed. When routing these pairs on a PCB, the characteristics must match one of the following:

- Route each single-ended trace with a characteristic impedance of 50Ω referenced to ground.
- Route each positive and negative trace on each port as differential pairs with 100Ω characteristic differential impedance.

7.2 Chassis Ground

To isolate the board from ESD events and to prevent a common-mode noise ground path, a separate chassis ground region should be allocated. This separate chassis ground, as shown in Figure 7-2, should be electrically connected to the external chassis and to the shield ground of the RJ45 connectors.

FIGURE 7-2: RECOMMENDED SEPARATE CHASSIS GROUND



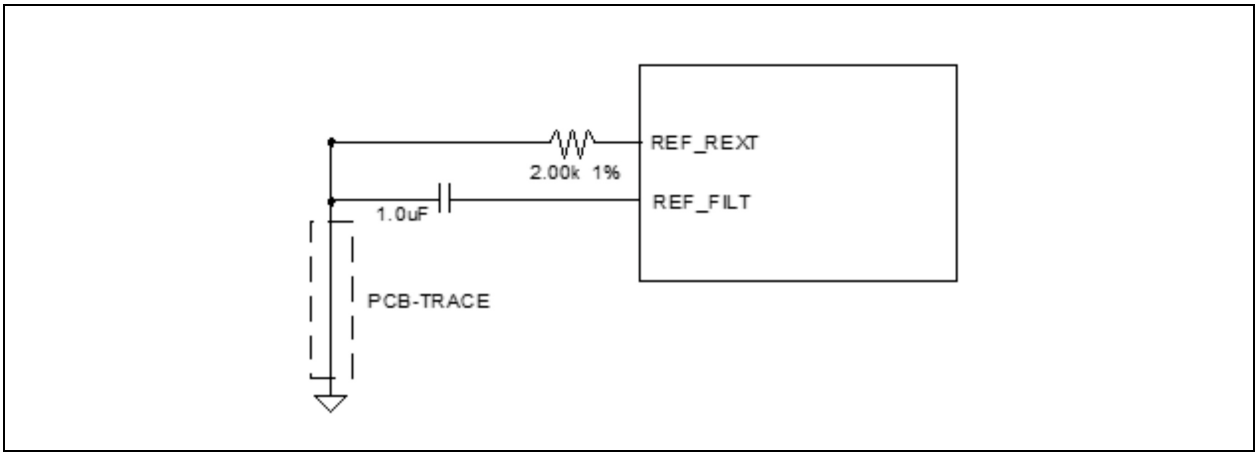
7.3 Voltage Reference Pins

For proper operation of the internal copper PHY, the switch must generate an on-chip band gap reference voltage at the REF_FILT pin. To generate that reference voltage, the following components are required for each VSC7511/12 in the system:

- 2.0 kΩ reference resistor, 1% tolerance, minimum 1/16 W connected to the REF_REXT pin
- 1 µF capacitor, 10% tolerance or better connected to the REF_FILT pin

For best performance, special consideration of the ground connection of the voltage reference circuit is necessary to prevent bus drops that would cause reference voltage inaccuracy. The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace (instead of connecting individually to a common ground plane), as shown in Figure 7-3. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to VSC7511/12.

FIGURE 7-3: VOLTAGE REFERENCE CIRCUIT



8.0 SERDES INTERFACES

As shown in Table 6-1 and Table 6-2, VSC7511/12 supports two 1G SerDes interfaces and three 6G SerDes interfaces. All of the SerDes interfaces can connect small form-factor pluggable (SFP) modules directly to support 100FX, 1000BX, and 2.5G fiber optical ports (on the 6G SerDes). They can also be configured as SGMII to connect to the external PHY. The 1G and 6G SerDes can also support MAC-to-MAC and backplane connection.

A bias resistor of 620Ω ±1% between SerDes_Rext_[1:0] is always needed even if none of the above SerDes interfaces are enabled in the design.

8.1 SFP Port

Since there are internal AC-coupling capacitors in the SFP modules, the connection from a VSC7511/12 SerDes to the SFP modules can be DC coupling.

SFP control signals can be supported by the GPIO pins on the switch. RX_LOS signal from the modules should be connected to one of the six SFPx_SD inputs to support hardware-based signal detection for the physical coding sub-layer (PCS) module of those SFP ports. The SFPx_SD inputs pins are overlaid on GPIO pins.

Alternatively, the SFP I/O control signals can all be supported by the serial GPIO controller through the four SGPIO pins (overlaid on GPIO_0-GPIO_3). There are rules to map RX_LOS signals to the SGPIO bits. See Section 9.0, "Serial GPIO Controller" on the SGPIO controller.

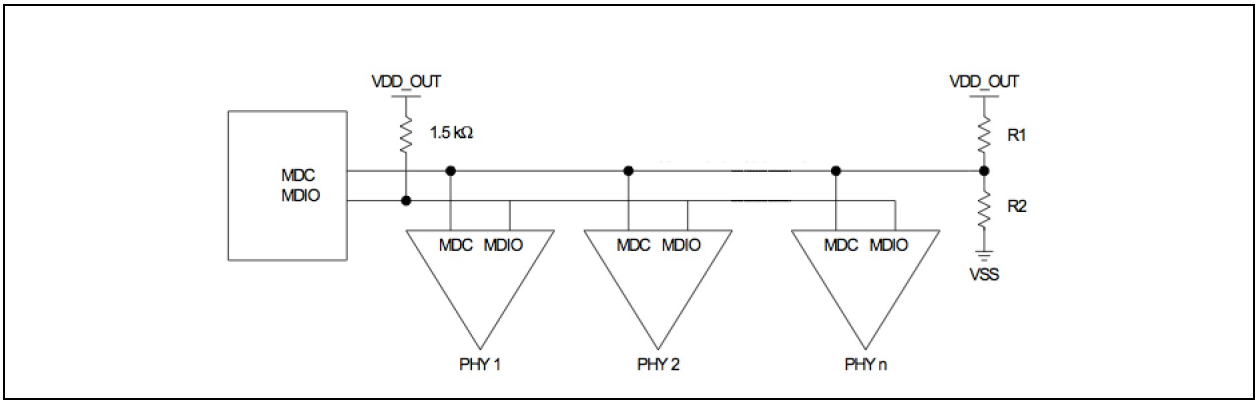
8.2 External PHY

When the SerDes interfaces are used to connect to the external PHY, then AC coupling is recommended between the switch and the external PHY. Take caution in naming the RX and TX pairs on the switch and PHY. Normally, RX is the output pair and TX is the input pair on a PHY. This is different from how they are named on a switch. Make sure that the output pair from the switch is connected to the input pair of the PHY and vice versa.

In order for the software to access the external PHY registers, MIIM interface should be connected from VSC7511/12 to the external PHY. VSC7511/12 supports two MIIM interfaces: MIIM0 and MIIM1. MIIM0 is an internal bus to access the internal PHY only. MIIM1 should be used to access the external PHY.

Because MDIO is an open drain output, MDIO should be pulled high with the resistor around 1.5 KΩ. When connecting MDC/MDIO to multiple PHYs, the layout scheme in Figure 8-1 with end termination is recommended. The MIIM controller uses PHY address to select one of the external PHY, so the PHY addresses must be configured differently for each PHY on the same MIIM bus.

FIGURE 8-1: CONNECTING MDC/MDIO TO MULTIPLE PHYS



8.3 MAC-to-MAC Connection

AC coupling is recommended on the MAC-to-MAC connection especially when the receiving end is a non-Microchip device. VSC7511/12 has internal 100R termination and biasing. Check if termination and biasing are required if the receiving end is a non-Microchip device. Make sure that the signal direction and polarity are correct. It is recommended to simulate the high-speed signals like the QSGMII interface.

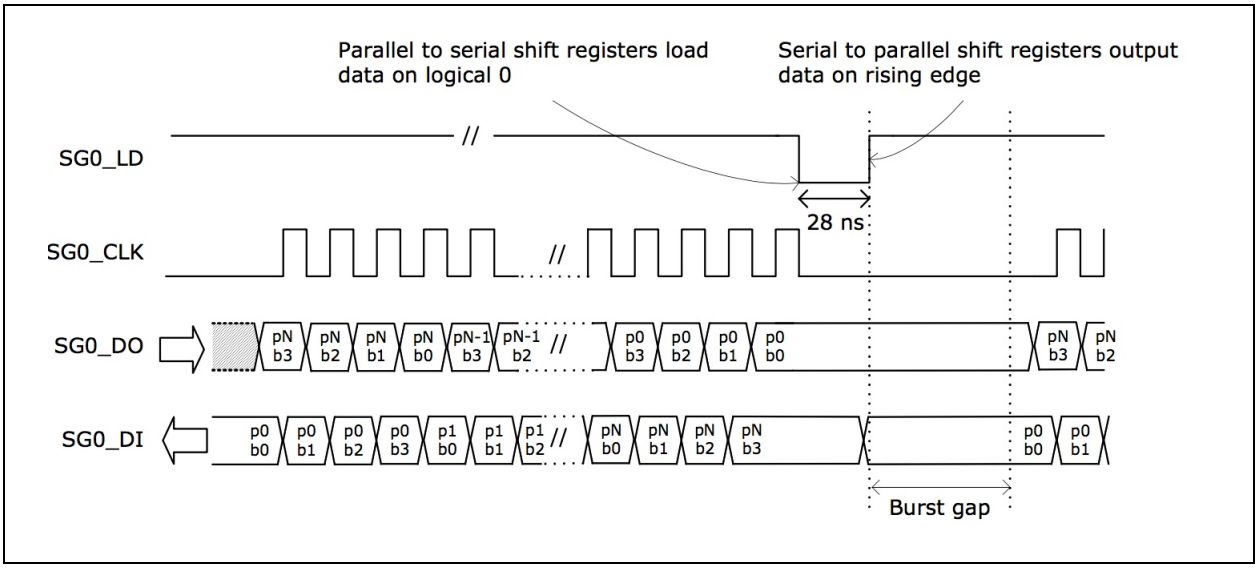
Signal detection can be omitted since MAC-to-MAC or backplane connection is always connected.

Unused SerDes interfaces can be left floating.

9.0 SERIAL GPIO CONTROLLER

The serial GPIO controller uses a 4-pin serial interface to extend the number of available general purpose I/O pins. The four SGPIO pins are overlaid on GPIO_0-GPIO_3. Figure 9-1 shows the I/O timing of the serial GPIO controller. Serial data are output on the SG_DO pin clocked by SG_CLK in bursts. After each burst, there is an assertion of the SG_LD signal. At the same time as shifting out serial outputs on SG_DO, the serial GPIO controller also samples the SG_DI input. The values sampled on SG_DI are made available to the software.

FIGURE 9-1: SGPIO TIMING



The maximum length of a burst is 128 bits data cycles organized by 32 ports with 4-bit port width. However, each SGPIO port can be enabled or disabled individually, and the port width (number of bits per port) is also centrally configurable. All enabled ports will have the same port width. The configuration of port enabling and port width applies to both serial input and output.

SG_LD can be used to ensure that outputs are stable when serial data are being shifted through the shift registers (for example, the TX_DIS output signals for the SFP modules). This can be done by using the SG_LD signal to load the serial data onto the parallel output pins after the burst has completed. 74HC595 is one of the shift registers that supports load input. If the serial GPIO controller is used for serial LED output, then SG_LD is optional because it is usually not detected when serial data are updated (shift through the chain). In that case, 74HC164 can also be used, which does not have the load input.

When a serial output bit is configured to support link/activity LED, it needs to know which switch port status to display on which SGPIO bit. This mapping is not completely software-programmable. The SGPIO controller uses a 1:1 mapping, which means SGPIO port 0 can only display link/activity for switch port 0, SGPIO port 1 can only display link/activity for switch port 1, and so on.

The serial input function of the SGPIO controller can automatically route Signal detection (RX_LOS) to the internal PCS block of a certain port. The signal detection function also uses 1:1 mapping between the switch port number and the SGPIO port number, and only bit 0 of each SGPIO port can be enabled for signal detection of the RX_LOS input.

There might be more serial output bits than serial input bits in a typical design especially when serial LED is supported. Since the port enabling and port width configuration are shared by the SGPIO output and input, the same number of serial bits in the output and input streams is present, which means the same number of external shift registers is required for both output and input chain. Hence, some shift registers are wasted on the serial input chain. To save the shift registers for the unused SGPIO input bits, the serial input bits can be looped – the SG_DI input signal is also connected to the serial input pins of the last shift register to create a loop, so that the bits in that loop can be duplicated and the length of the whole serial stream is expanded. Check the Microchip reference design and application note on the SGPIO for more details.

10.0 OTHER INTERFACES

10.1 UART

VSC7511/12 supports two UART interfaces. The first UART is overlaid on GPIO_6 and GPIO_7, and is used by the software as the command line interface for debugging. It is recommended to be made available through an RS-232 interface.

10.2 I^2C

The two-wire serial interface (TWI) is compatible with I^2C. It uses two pins that are overlaid on GPIO_16 and GPIO_17. The two pins are recommended to be pulled high. VSC7511/12 has built-in support for connecting to multiple I^2C devices that use the same address (for example, SFP modules). This is done using the multiplexed clock outputs (TWI_SCL_Mn) rather than TWI_SCL. Depending on which device it needs to communicate, the software can enable or disable the various clocks. TWI_SCL_Mn are overlaid pins on GPIO_6-GPIO_15 and GPIO_17-GPIO_21.

11.0 SYSTEM RESET

The nRESET and JTAG_nTRST inputs must be held low until all power supply voltages have reached their recommended operating condition values. When the JTAG interface is not used, JTAG_nTRST is recommended to be pulled low. nRESET (active low) must be deasserted no less than 20 ms after the power supply voltages have all reached their recommended values and the reference clock is stable. For this reason, a reset generator with Power-on Reset (POR)/ delay circuit must be used on the nRESET pin. It is also recommended to use a reset generator with a manual input so that the switch can be put into reset during on-PCB Flash programming. See Section 5.1, "Internal CPU Auto Boot Mode" for more details. While the reset signal resets the VSC7512 switch, it also resets the Flash memory, external PHY, shift registers for SGPIO, and other parts that must be put in known state.

12.0 SYNCE AND PTP

VSC7511/12 supports SyncE clock recovery from either the four internal copper PHY ports or any of the SerDes interfaces. The recovered clocks share the two recovered clock output pins overlaid on GPIO_20 and GPIO_21. For SyncE application, the two recovered clock output pins are connected to the inputs of an external digital phase locked loop (DPLL). The DPLL output is looped to the reference clock input of VSC7511/12. Make sure the DPLL outputs the correct clock signal for VSC7511/12 to boot after power-up.

VSC7511/12 also supports PTP application. GPIO_18 and GPIO_19 can be configured as PTP 1PPS input or output. They can also be configured to output a programmable clock signal. UART2 can be used to send or receive Time-of-day (ToD) frames. But for software consideration, VSC7511/12 is only recommended to do E2E transparent clock, which is already supported by the standard unmanaged software through compile option.

13.0 HARDWARE CHECKLIST SUMMARY

TABLE 13-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet and retain the reference design's use of GPIO as much as possible to minimize software efforts.		
	Section 2.3, "Strapping Pins"	Check VCORE_CFG[3:0] to match booting mode and REFCLKSEL[2:0] to match the reference clock frequency.		
Section 3.0, "Power"	Section 3.0, "Power"	Each power rail should have bulk and high-frequency decoupling capacitors.		
		Analog supplies should be isolated from digital supplies through ferrite beads.		
		Check the power sequencing.		
		Connect the exposed pad to GND through grid of thermal vias.		
Section 4.0, "Reference Clock"	Section 4.1, "Differential Clock"	Check that the differential clock is compatible with LDVS. See the data sheet for the specification on reference clock input voltage range.		
	Section 4.2, "Single-Ended REFCLK Input"	Check the resistor values of the resistor network.		
Section 5.0, "CPU System"	Section 5.1, "Internal CPU Auto Boot Mode"	Check the VCORE_CFG[3:0] strapping.		
		Check the SPI Flash. Voltage translation buffer might be needed.		
	Section 5.2, "External CPU Mode"	Check the VCORE_CFG[3:0] strapping.		
		Check the SPI slave or MIIM slave if used as management interface from the external CPU to VSC7511/12.		
Section 6.0, "Port Configuration"	Section 6.0, "Port Configuration"	Make sure the selected copper PHY ports and SerDes ports combination can be supported by VSC7511/12.		
Section 7.0, "Internal Copper PHY Ports"	Section 7.1, "Copper PHY MDI Interface"	Check the magnetic connection. No center tap voltage is allowed, and external termination resistors are not needed.		
	Section 7.2, "Chassis Ground"	Chassis ground is recommended.		
	Section 7.3, "Voltage Reference Pins"	Use 2.0 kΩ, 1% resistor for REF_REXT and 1 µF capacitor for REF_FILT. Use single-point grounding for REF_FILT and REF_REXT.		

TABLE 13-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 8.0, "SerDes Interfaces"	Section 8.0, "SerDes Interfaces"	Connect an external 620Ω ±1% resistor between SerDes_Rext_[1:0] for analog bias calibration.		
	Section 8.1, "SFP Port"	Make sure SerDes polarity is correct. Check the SFP control signals. RX_LOS is recommended to be connected to the switch (SFPx_SD inputs or SGPIO).		
	Section 8.2, "External PHY"	AC coupling is recommended. Check the signal directions. Check the MIIM connection and topology.		
	Section 8.3, "MAC-to-MAC Connection"	AC coupling is recommended. Check the signal directions.		
Section 9.0, "Serial GPIO Controller"	Section 9.0, "Serial GPIO Controller"	Check the switch port to SGPIO port mapping for the link/active LED output and RX_LOS signal input.		
Section 10.0, "Other Interfaces"	Section 10.1, "UART"	Make UART available for CLI debugging.		
	Section 10.2, "I^2C"	Pull high required. Use the multiplexed clockout for I^2C slave devices with same addresses (like SFP modules).		
Section 11.0, "System Reset"	Section 11.0, "System Reset"	Check that all the devices and the board are reset by the system reset output — switch, PHY, Flash, SGPIO shift registers, and so on. Put the switch into reset when the on-PCB Flash programming is performed.		
Section 12.0, "SyncE and PTP"	Section 12.0, "SyncE and PTP"	Check if an external DPLL is needed for SYNCE. Only E2E TC is recommended for VSC7511/12 when the internal CPU is used.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003283A (10-23-19)	Initial release	

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